

- Else if one input operand was positive and the other negative, its 2's-C value is calculated.
- Else if both operands were negative, the value passes unchanged.

17) Use the given designs as a template for your design. Here are a few major differences:

- Your structural DP will have different sized and connected modules/entities.
- Your behavioral CU will need to follow the sequence described by the ASM Chart of the SSRM in module21A, modified to reflect your design specifications.
- The example designs don't contain any 2's-C blocks.

18) Graded by TA:

- 6 points for the data path paper and pencil design(3p), and completed table below (3p) – **due for full points a week after the start of the lab!**
- 5 points for successfully compiled code of all necessary building blocks/components, except for top level module/entity – **due for full points a week after the start of the lab!**
- 4 points for successfully compiled top level module/entity (2p) and testbench code (2p).
- 25 points for successful verification of the following data sets – can be in the same timing diagram:

Generic multiplicand value pattern	Generic multiplier value pattern	Your signed multiplicand value	Your signed multiplier value	Your unsigned multiplicand value	Your unsigned multiplier value	Your unsigned final product	Your signed final product	Points
0000	0000	00000000	00000000	00000000	00000000	0000000000000000	0000000000000000	5
1111	1111	11111111	11111111	00000001	00000001	0000000000000001	0000000000000001	5
0101	0101	5461	5461	5461	5461	2982251	2982251	5
1010	1010	-5462	-5462	5462	5462	29832444	29832444	5
0101	1010	5461	-5462	5461	5462	29827982	29827982	5

For your multiplicand and multiplier values repeat the pattern from LSbit to MSbit as necessary.

19) Show your working, i.e. compiled and simulated, designs to the TA. The report for this lab will be combined with that for lab12, and will be upload in its own dropbox as the final lab report – see lab policy for details.

20) This concludes this week's lab.

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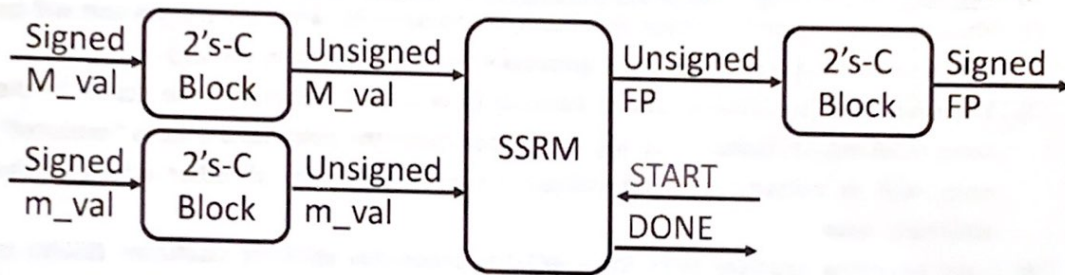
EEEE-220-Lab11

- 1) From mycourses download on your desktop this pdf file, dxp_SSLM_v.qar and dxp_SSLM_vhdl.qar. I will also provide a printed copy in class.
- 2) **Objective:** The objective of this lab exercise is to implement using a combination of structural (in the concurrent block of code) and behavioral (in the procedural block of code) description/model, a signed, two's complement, hereafter 2's-C, multiplier. Its operation follows that of a sequential, shift-right multiplier (SSRM), presented in module 21A and discussed in the lecture. It is comprised of a data path and a control unit. The 4-bit SSRM design covered in class serves as a paper and pencil design example.
- 3) You can use either VHDL or Verilog.
- 4) The final lab project demo and defenses are due for full points as described in the lab policy. Please plan accordingly.
- 5) You have to attend the lab to get any points for lab11 and lab12!!!
- 6) The datapath will be comprised of structural components, while the control unit will be implemented in a procedural block (*process* in VHDL or *always* in Verilog).
- 7) The structural (concurrent) and behavioral (procedural) blocks of code reside in the same module/architecture. During every clock cycle, the behavioral code is "executed" once, and its outputs are then evaluated concurrently with all other values of the structural code.
- 8) I am providing example code for a 4x4-bits sequential shift-left multiplier (SSLM) in Verilog and VHDL. These can and should be used as guidance on how to arrange and use mixed code.
- 9) Until then, you should start preparing the necessary modules for the structural datapath. You most probably will need to only resize them.
- 10) This lab uses the IDN assigned to you in lab6. Please type its decimal and binary values here: 58 0011 1010. Now, copy/paste this unsigned binary value in the table below. Circle with a **pen**, not a pencil, your individual design specifications. Alternatively, if you re-type this word document, highlight or bolden your specifications.
- 11) The next table contains the key to your individual design specifications:

Bit	Your Value	Value = '11'	Value = '10'	Value = '01'	Value = '00'	Comments
Bit7 6		---	---	Behavioral	Structural	2's-C Description of the Final Product
Bit5 4		Behavioral/Behavioral	Behavioral/Structural	Structural/Behavioral	Structural/Structural	2's-C Description of Multiplicand and multiplier
Bit3 2		15	14	13	12	Multiplicand width (M_val width)
Bit1 0		15	14	13	12	Multiplier width (m_val width)

12) Below is the generic block diagram of your design.

(Final will be 28 bits)



13) You need to perform a paper and pencil design of your data path (ONLY!). Copy the above diagram on a landscape oriented, letter sized, sheet of paper. Enter the sizes of all these busses. **The central SSRM block you have to re-draw at the detail level of the data path (DP) shown in module 21A.** It is best if you do this as a pre-lab activity, so that the TA can check and approve it at the beginning of the lab. The main goal is to ensure that you are following your design specifications and know what you have to design.

14) Identify the type and size of all necessary modules/entities.

15) The operation of the 2's-C blocks for M_val and m_val is as follows:

- If the MSbit is 0, the value passes unchanged.
- Else if the MSbit is 1, the 2's-C value is calculated. Reminder: The latter is equal to the 1's-C value + '1'.

16) The operation of the 2's-C block for the FP is as follows:

- If both input operands were positive, the value passes unchanged.