Errata 01 for MIPI D-PHY℠ Specification

Specification Version 2.1

Specification Dated 15 December 2016

Specification MIPI Board Adopted 28 December 2015

Errata 01 Dated 13 November 2017

Errata MIPI Board Approved 30 November 2017

* IMPORTANT NOTE TO IMPLEMENTERS *

- The changes listed in this Errata document will be made in the next edition of this MIPI Specification.
- Implementations should observe all changes listed here.
- The location of each change is also marked in the attached copy of the MIPI Specification. To reduce the risk of incorrect implementations, we suggest you consider discarding any previous copies of this MIPI Specification not so marked.
- This MIPI Specification as modified by the changes listed in this Errata document is also a MIPI Specification, as the MIPI Bylaws defines the term.
- **MIPI member companies' rights and obligations apply to the modified MIPI Specification as defined in the MIPI Membership Agreement and MIPI Bylaws.**

This Errata document includes 11 changes to the Board Adopted MIPI Specification for D-PHY v2.1.

These changes are listed below as separate Items, and are highlighted in the attached copy of the adopted Specification:

- Items 1 and 3 contain the key Technical corrections: the seed of the PRBS9 generator is changed, and Figure 28 is replaced with a new Figure 89 (which appears in a new Annex D, see Item 10).
- Item 7 addresses the fact that changing the seed results in a different PRBS9 bit sequence.
- Most of the other Items are Editorial, and necessitated by the key Technical Items.

Item	Spec Page Number	PDF Page Number	Correction
1	48	68	**Editorial or Technical:** Technical **Location:** Line 655 **Correction:** Change “000000001” to “011111111” **Reason:** Use same seed value as in Section 12.3, for consistency **Technical Impact:** Changes the bit sequence of the PRBS9 test pattern
2	48	68	**Editorial or Technical:** Editorial **Location:** Line 658 **Correction:** Change “…Data[7:0]. Data[7:0] is the output of the Q8 through Q1 registers, as shown in ***Figure 28***.” To “…Data[7:0]. Data[7:0] is shown in ***Annex D***.” **Reason:** Material has moved to new Annex (see Item 10) **Technical Impact:** None
3	48	68	**Editorial or Technical:** Technical **Location:** Line 662 **Correction:** Delete Figure 28, and replace all references to “***Figure 28***” with references to ”***Figure 89*** in ***Annex D***” **Reason:** Material has moved to a new Annex (see Item 10) **Technical Impact:** Clarification of tapping points, and location of LSB and MSB in figure
4	48	68	**Editorial or Technical:** Editorial **Location:** Line 665 **Correction:** Change “1000 0000 0001 0000” To “1111 1111 1000 0011” **Reason:** Updates the example to reflect technical changes made in Items 1, 6, 7, and 10 **Technical Impact:** None

5	104	124	**Editorial or Technical:** Editorial **Location:** Line 1372 **Correction:** Insert closing parenthesis ‘)‘ at end of line **Reason:** Copy editing error in adopted Specification **Technical Impact:** None
6	104	124	**Editorial or Technical:** Technical **Location:** Lines 1377 and 1378 **Correction:** Change “…[15:0] with a 16 bit seed register initialized 0x00FF:” To “…with a register initialized to 011111111 (Q9:Q1):” **Reason:** Remove reference to register size **Technical Impact:** Changes the bit sequence of the PRBS9 test pattern

7	104	124	**Editorial or Technical:** Technical **Location:** Lines 1379 through 1386 **Correction:** Replace line 1379 plus the entire PRBS9 test pattern with the ‘Replacement PRBS9 Test Pattern” shown below **Reason:** Result of change to the PRBS9 seed value and tapping points, as well as location of LSB and MSB in PRBS generator **Technical Impact:** Changes the bit sequence of the PRBS9 test pattern **Replacement PRBS9 Test Pattern:** 0b11111111_10000011_11011111_00010111_ 00110010_00001001_01001110_11010001_ 11100111_11001101_10001010_10010001_ 11000110_11010101_11000100_11000100_ 01000000_00100001_00011000_01001110_ 01010101_10000110_11110100_11011100_ 10001010_00010101_10100111_11101100_ 10010010_11011111_10010011_01010011_ 00110000_00011000_11001010_00110100_ 10111111_10100010_11000111_01011001_ 01100111_10001111_10111010_00001101_ 01101101_11011000_00101101_01111101_ 01010100_00001010_01010111_10010111_ 01110000_00111001_11010010_01111010_ 11101010_00100100_00110011_10000101_ 11101101_10011010_00011101_1110000/1_ 11111111_00000111_10111110_00101110_ 01100100_00010010_10011101_10100011_ 11001111_10011011_00010101_00100011_ 10001101_10101011_10001001_10001000_ 10000000_01000010_00110000_10011100_ 10101011_00001101_11101001_10111001_ 00010100_00101011_01001111_11011001_ 00100101_10111111_00100110_10100110_ 01100000_00110001_10010100_01101001_ 01111111_01000101_10001110_10110010_ 11001111_00011111_01110100_00011010_ 11011011_10110000_01011010_11111010_ 10101000_00010100_10101111_00101110_ 11100000_01110011_10100100_11110101_ 11010100_01001000_01100111_00001011_ 11011011_00110100_00111011_110000/11_ 11111110

8	104	124	**Editorial or Technical:** Editorial **Location:** Before line 1387 **Correction:** Insert "The repetition period is 511 bits, and it starts with eight ones of the PRBS9 sequence based on seed of 011111111 (Q9:Q1). In the PRBS9 sequence shown above, every repetition period is separated by a red slash ('/'), and every byte is separated by an underscore ('_')." **Reason:** Explains PRBS9 test pattern and improved formatting in the replacement PRBS9 test pattern (see Item 7) **Technical Impact:** None
9	104	124	**Editorial or Technical:** Editorial **Location:** Line 1391 **Correction:** Change 'data are' to 'data is' **Reason:** Grammar edit **Technical Impact:** None
10	144	164	**Editorial or Technical:** Both **Location:** After page 144 (i.e., after Annex C and before Participants section) **Correction:** Insert new Annex D as shown on the following page **Reason:** Revised description of the PRBS9 Generator, corrected PRBS9 seed value, and resulting change to PRBS9 test pattern is required **Technical Impact:** Changes the PRBS9 seed value and bit sequence of the PRBS9 test pattern
11	6	26	**Editorial or Technical:** Editorial **Location: After** line 161 **Correction:** Insert new document reference [ITUT01] as shown below **Reason:** The new Annex D cites ITU-150, and this Item provides the reference to the document. **Technical Impact:** None

[ITUT01] ITU-T Recommendation O.150, *Specifications of measuring equipment – Equipment for the measurement of digital and analogue/digital parameters – General requirements for instrumentation for performance measurements on digital transmission equipment*, <http://www.itu.int/rec/T-REC-O/en>, International Telecommunications Union, 5 October 1992.

Annex D Description of the PRBS9 Generator

The PRBS9 generator is used for calibration (***Section 6.13***) and for the HS Test Mode (***Section 12.3***). Per ITU-150 ***[ITUT01]***, the data stream is generated by a shift register set with the following feedback: $x^0 + x^5 + x^9$.

The generator is connected to the serializer as shown in ***Figure 89***.

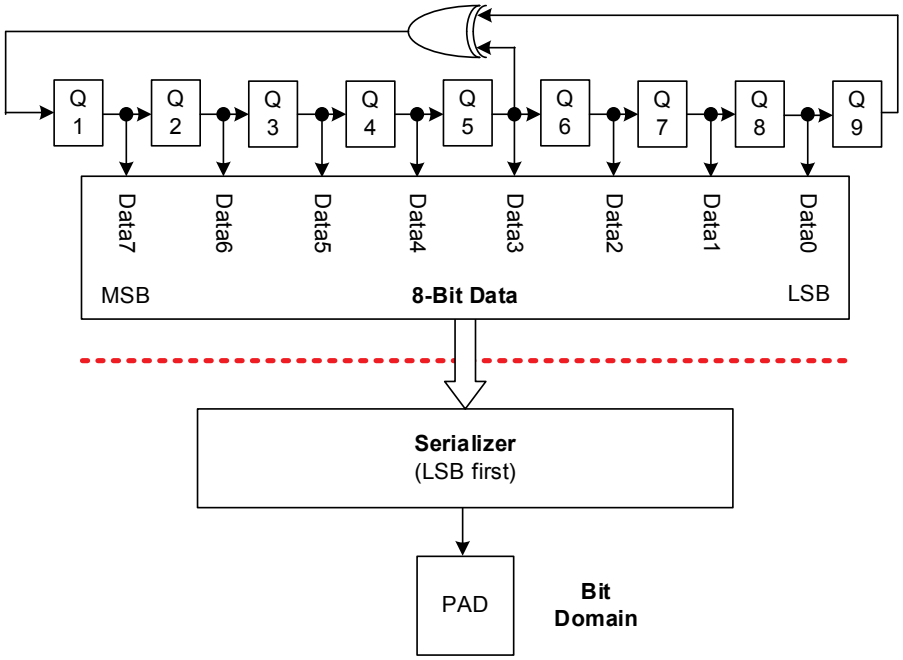

Figure 89 PRBS Generator and Connection to the Serializer

With the seed of 0b011111111 [Q9:Q1], the following data stream is produced (repetition length 511 bits):

```
0b11111111_10000011_11011111_00010111_00110010_00001001_01001110_11010001_
  11100111_11001101_10001010_10010001_11000110_11010101_11000100_11000100_
  01000000_00100001_00011000_01001110_01010101_10000110_11110100_11011100_
  10001010_00010101_10100111_11101100_10010010_11011111_10010011_01010011_
  00110000_00011000_11001010_00110100_10111111_10100010_11000111_01011001_
  01100111_10001111_10111010_00001101_01101101_11011000_00101101_01111101_
  01010100_00001010_01010111_10010111_01110000_00111001_11010010_01111010_
  11101010_00100100_00110011_10000101_11101101_10011010_00011101_1110000/1_
  11111111_00000111_10111110_00101110_01100100_00010010_10011101_10100011_
  11001111_10011011_00010101_00100011_10001101_10101011_10001001_10001000_
  10000000_01000010_00110000_10011100_10101011_00001101_11101001_10111001_
  00010100_00101011_01001111_11011001_00100101_10111111_00100110_10100110_
  01100000_00110001_10010100_01101001_01111111_01000101_10001110_10110010_
  11001111_00011111_01110100_00011010_11011011_10110000_01011010_11111010_
  10101000_00010100_10101111_00101110_11100000_01110011_10100100_11110101_
  11010100_01001000_01100111_00001011_11011011_00110100_00111011_110000/11_
  11111110
```

The repetition period is 511 bits, and it starts with eight ones of the PRBS9 sequence (based on seed of 0b011111111 [Q9:Q1]). In the PRBS9 sequence shown above, every repetition period is separated by a red slash (‘/’), and every byte is separated by an underscore (‘_’).

(End of new Annex D)

Specification for D-PHY℠

Version 2.1

15 December 2016

MIPI Board Adopted 28 March 2017

This document is a MIPI Specification. MIPI member companies' rights and obligations apply to this MIPI Specification as defined in the MIPI Membership Agreement and MIPI Bylaws.

Further technical changes to this document are expected as work continues in the PHY Working Group.

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Release History

Date	Version	Description
2016-03-08	v2.0	Initial Board adopted release.
2017-03-28	v2.1	Board approved release.

1 Introduction

This specification provides a flexible, low-cost, High-Speed serial interface solution for communication interconnection between components inside a mobile device. Traditionally, these interfaces are CMOS parallel busses at low bit rates with slow edges for EMI reasons. The D-PHY solution enables significant extension of the interface bandwidth for more advanced applications. The D-PHY solution can be realized with very low power consumption.

1.1 Scope

The scope of this document is to specify the lowest layers of High-Speed source-synchronous interfaces to be applied by MIPI Alliance application or protocol level specifications. This includes the physical interface, electrical interface, low-level timing and the PHY-level protocol. These functional areas taken together are known as D-PHY.

The D-PHY specification shall always be used in combination with a higher layer MIPI specification that references this specification. Any other use of the D-PHY specification is strictly prohibited, unless approved in advance by the MIPI Board of Directors.

The following topics are outside the scope of this document:

- **Explicit specification of signals of the clock generator unit.** Of course, the D-PHY specification does implicitly require some minimum performance from the clock signals. Intentionally, only the behavior on the interface pins is constrained. Therefore, the clock generation unit is excluded from this specification, and will be a separate functional unit that provides the required clock signals to the D-PHY in order to meet the specification. This allows all kinds of implementation trade-offs as long as these do not violate this specification. More information can be found in ***Section 5***.
- **Test modes, patterns, and configurations.** Obviously testability is very important, but because the items to test are mostly application specific or implementation related, the specification of tests is deferred to either the higher layer specifications or the product specification. Furthermore MIPI D-PHY compliance testing is not included in this specification.
- **Procedure to resolve contention situations.** The D-PHY contains several mechanisms to detect Link contention. However, certain contention situations can only be detected at higher levels and are therefore not included in this specification.
- **Ensure proper operation of a connection between different Lane Module types.** There are several different Lane Module types to optimally support the different functional requirements of several applications. This means that next to some base-functionality there are optional features which can be included or excluded. This specification only ensures correct operation for a connection between matched Lane Modules types, which means: Modules that support the same features and have complementary functionality. In case the two sides of the Lane are not the same type, and these are supposed to work correctly, it shall be ensured by the manufacturer(s) of the Lane Module(s) that the provided additional functionality does not corrupt operation. This can be easiest accomplished if the additional functionality can be disabled by other means independent of the MIPI D-PHY interface, such that the Lane Modules behave as if they were the same type.
- **ESD protection level of the IO.** The required level will depend on a particular application environment and product type.
- **Exact Bit-Error-Rate (BER) value.** The actual value of the achieved BER depends on the total system integration and the hostility of the environment. Therefore, it is impossible to specify a BER for individual parts of the Link. This specification allows for implementations with a BER<10^{-12}.
- **Specification of the PHY-Protocol Interface.** The D-PHY specification includes a PHY-Protocol Interface (PPI) annex that provides one possible solution for this interface. This annex is limited to the essential signals for normal operation in order to clarify the kind of signals needed at this

interface. For power reasons this interface will be internal for most applications. Practical implementations may be different without being inconsistent with the D-PHY specification.

- **Implementations.** This specification is intended to restrict the implementation as little as possible. Various sections of this specification use block diagrams or example circuits to illustrate the concept and are not in any way claimed to be the preferred or required implementation. Only the behavior on the D-PHY interface pins is normative.

D-PHY Specification evolution is primarily driven by the need to achieve higher data rates and better efficiency, while at the same time respecting backward compatibility. In this process the previous version of the specification is taken and modifications are added, without compromising backward compatibility. Each new version of the specification that is derived both preserves all the specification components of the previous version, and adds the new changes. Due to technology evolution, some parameters are changed to optimize for newer technologies.

It is recommended to always follow the latest version of the D-PHY Specification, irrespective of the targeted data rate. The product data sheet should mention both the targeted D-PHY Specification version and data rates. This will enable the system integrator to make proper decisions to achieve interoperability goals.

Regulatory compliance methods are not within the scope of this document. It is the responsibility of product manufacturers to ensure that their designs comply with all applicable regulatory requirements.

1.2 Purpose

The D-PHY specification is used by manufacturers to design products that adhere to MIPI Alliance interface specifications for mobile device such as, but not limited to, camera, display and unified protocol interfaces.

Implementing this specification reduces the time-to-market and design cost of mobile devices by standardizing the interface between products from different manufacturers. In addition, richer feature sets requiring high bit rates can be realized by implementing this specification. Finally, adding new features to mobile devices is simplified due to the extensible nature of the MIPI Alliance Specifications.

2 Terminology

2.1 Use of Special Terms

The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

> The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform to the Specification and from which no deviation is permitted (*shall* equals *is required to*).
>
> The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.
>
> The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.
>
> The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).
>
> The word *may* is used to indicate a course of action permissible within the limits of the Specification (*may* equals *is permitted to*).
>
> The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

All sections are normative, unless they are explicitly indicated to be informative.

2.2 Definitions

Bi-directional: A single Data Lane that supports communication in both the Forward and Reverse directions.

DDR Clock: Half rate clock used for dual-edged data transmission.

D-PHY: The source synchronous PHY defined in this document. D-PHYs communicate on the order of 500 Mbit/s hence the Roman numeral for 500 or “D.”

Escape Mode: An optional mode of operation for Data Lanes that allows low bit-rate commands and data to be transferred at very low power.

Forward Direction: The signal direction is defined relative to the direction of the High-Speed DDR clock. Transmission from the side sending the clock to the side receiving the clock is the Forward direction.

Lane: Consists of two complementary Lane Modules communicating via two-line, point-to-point Lane Interconnects. Sometimes Lane is also used to denote interconnect only. A Lane can be used for either Data or Clock signal transmission.

Lane Interconnect: Two-line, point-to-point interconnect used for both differential High-Speed signaling and Low-Power, single-ended signaling.

Lane Module: Module at each side of the Lane for driving and/or receiving signals on the Lane.

Line: An interconnect wire used to connect a driver to a receiver. Two Lines are required to create a Lane Interconnect.

Link: A connection between two devices containing one Clock Lane and at least one Data Lane. A Link consists of at least two PHYs and two Lane Interconnects.

Master: The Master side of a Link is defined as the side that transmits the High-Speed Clock. The Master side transmits data in the Forward direction.

PHY: A functional block that implements the features necessary to communicate over the Lane Interconnect. A PHY consists of one Lane Module configured as a Clock Lane, one or more Lane Modules configured as Data Lanes and a PHY Adapter Layer.

PHY Adapter: A protocol layer that converts symbols from an APPI to the signals used by a specific PHY PPI.

PHY Configuration: A set of Lanes that represent a possible Link. A PHY configuration consists of a minimum of two Lanes, one Clock Lane and one or more Data Lanes.

Reverse Direction: Reverse direction is the opposite of the forward direction. See the description for Forward Direction.

Slave: The Slave side of a Link is defined as the side that does not transmit the High-Speed Clock. The Slave side may transmit data in the Reverse direction.

Turnaround: Reversing the direction of communication on a Data Lane.

Unidirectional: A single Lane that supports communication in the Forward direction only.

2.3 Abbreviations

e.g.	For example (Latin: exempli gratia)
i.e.	That is (Latin: id est)

2.4 Acronyms

APPI	Abstracted PHY-Protocol Interface
BER	Bit Error Rate
CIL	Control and Interface Logic
DDR	Double Data Rate
DUT	Device Under Test
EMI	Electro Magnetic Interference
EoT	End of Transmission
HS	High-Speed; identifier for operation mode
HS-RX	High-Speed Receiver (Low-Swing Differential)
HS-TX	High-Speed Transmitter (Low-Swing Differential)
IO	Input-Output
ISTO	Industry Standards and Technology Organization
LP	Low-Power: identifier for operation mode
LP-CD	Low-Power Contention Detector
LPDT	Low-Power Data Transmission
LP-RX	Low-Power Receiver (Large-Swing Single-Ended)
LP-TX	Low-Power Transmitter (Large-Swing Single-Ended)
LPS	Low-Power State(s)
LSB	Least Significant Bit

LVLP	Low Voltage Low Power, an optional signal voltage range in LP mode
Mbps	Megabits per second
MSB	Most Significant Bit
PHY	Physical Layer
PLL	Phase-Locked Loop
PPI	PHY-Protocol Interface
RF	Radio Frequency
RX	Receiver
SE	Single-Ended
SoT	Start of Transmission
TLIS	Transmission-Line Interconnect Structure: physical interconnect realization between Master and Slave
TX	Transmitter
UI	Unit Interval, equal to the duration of any HS state on the Clock Lane
ULPS	Ultra-Low Power State

3 References

[MIPI01] *MIPI Alliance Specification for D-PHY*, Version 1.0, MIPI Alliance, Inc., 22 September 2009.

[MIPI02] *MIPI Alliance Specification for C-PHY*, Version 1.0, MIPI Alliance, Inc., 7 October 2014.

[ITUT01] - See Errata 01 Item 11

4 D-PHY Overview

D-PHY describes a source synchronous, high speed, low power, low cost PHY, especially suited for mobile applications. This D-PHY specification has been written primarily for the connection of camera and display applications to a host processor. Nevertheless, it can be applied to many other applications. It is envisioned that the same type of PHY will also be used in a dual-simplex configuration for interconnections in a more generic communication network. Operation and available data-rates for a Link are asymmetrical due to a master-slave relationship between the two sides of the Link. The asymmetrical design significantly reduces the complexity of the Link. Some features like bi-directional, half-duplex operation are optional. Exploiting this feature is attractive for applications that have asymmetrical data traffic requirements and when the cost of separate interconnects for a return channel is too high. While this feature is optional, it avoids mandatory overhead costs for applications that do not have return traffic requirements or want to apply physically distinct return communication channels.

4.1 Summary of PHY Functionality

The D-PHY provides a synchronous connection between Master and Slave. A practical PHY Configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the Master and terminating at the Slave. The data signals can either be unidirectional or bi-directional depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the Link.

The Link includes a High-Speed signaling mode for fast-data traffic and a Low-Power signaling mode for control purposes. Optionally, a Low-Power Escape mode can be used for low speed asynchronous data communication. High speed data communication appears in bursts with an arbitrary number of payload data bytes.

The PHY uses two wires per Data Lane plus two wires for the Clock Lane. This gives four wires for the minimum PHY configuration. In High-Speed mode each Lane is terminated on both sides and driven by a low-swing, differential signal. In Low-Power mode all wires are operated single-ended and non-terminated. For EMI reasons, the drivers for this mode shall be slew-rate controlled and current limited.

The actual maximum achievable bit rate in High-Speed mode is determined by the performance of transmitter, receiver and interconnect implementations. Therefore, the maximum bit rate is not specified in this document. However, this specification is primarily intended to define a solution for a data rate range of 80 to 1500 Mbps per Lane without deskew calibration, up to 2500 Mbps with deskew calibration, and up to 4500 Mbps with equalization. When the implementation supports a data rate greater than 1500 Mbps, it shall also support deskew capability. When a Phy implementation supports a data rate more than 2500 Mbps, it shall also support equalization, and Spread Spectrum Clocking shall be available. Although PHY Configurations are not limited to this range, practical constraints make it the most suitable range for the intended applications. For a fixed clock frequency, the available data capacity of a PHY Configuration can be increased by using more Data Lanes. Effective data throughput can be reduced by employing burst mode communication. The maximum data rate in Low-Power mode is 10 Mbps.

The features introduced by this specification (Spread Spectrum Clocking, Transmit Equalization, and Deskew) can be applied to any HS data rate.

4.2 Mandatory Functionality

All functionality that is specified in this document and which is not explicitly stated in ***Section 5.5*** shall be implemented for all D-PHY configurations.

5 Architecture

This section describes the internal structure of the PHY including its functions at the behavioral level. Furthermore, several possible PHY configurations are given. Each configuration can be considered as a suitable combination from a set of basic modules.

5.1 Lane Modules

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect.

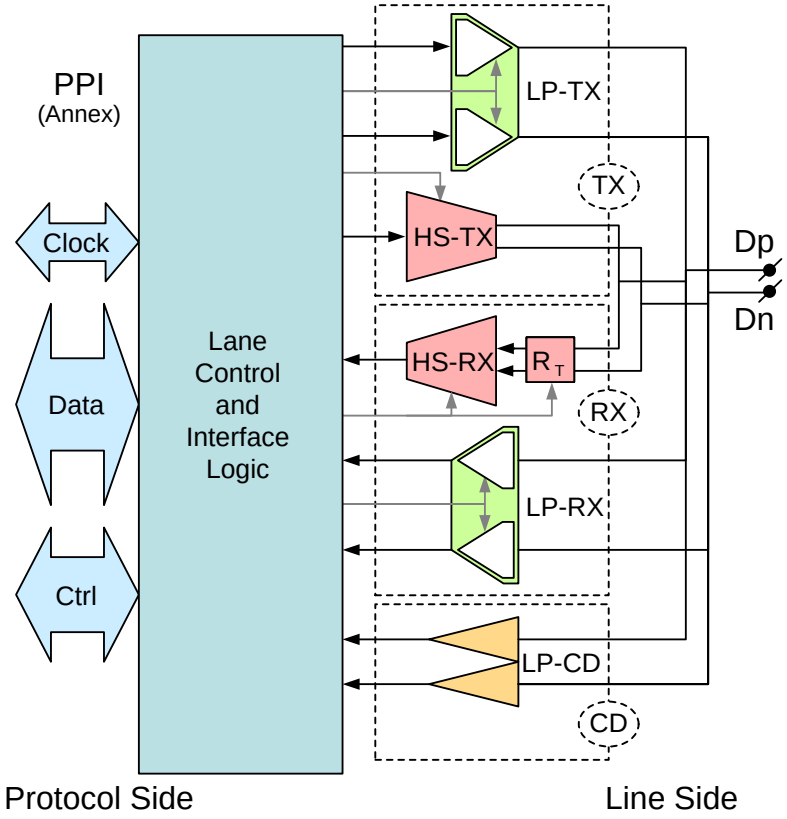

Figure 1 Universal Lane Module Functions

Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. An overview of all functions is shown in ***Figure 1***. High-Speed signals have a low voltage swing, e.g. 200 mV, while Low-Power signals have a large swing, e.g. 1.2V. High-Speed functions are used for High-Speed Data transmission. The Low-Power functions are mainly used for Control, but have other, optional, use cases. The I/O functions are controlled by a Lane Control and Interface Logic block. This block interfaces with the Protocol and determines the global operation of the Lane Module.

High-Speed functions include a differential transmitter (HS-TX) and a differential receiver (HS-RX).

A Lane Module may contain a HS-TX, a HS-RX, or both. A HS-TX and a HS-RX within a single Lane Module are never enabled simultaneously during normal operation. An enabled High-Speed function shall terminate the Lane on its side of the Lane Interconnect as defined in ***Section 9.1.1*** and ***Section 9.2.1***. If a

High-Speed function in the Lane Module is not enabled then the function shall be put into a high impedance state.

Low-Power functions include single-ended transmitters (LP-TX), receivers (LP-RX) and Low-Power Contention-Detectors (LP-CD). Low-Power functions are always present in pairs as these are single-ended functions operating on each of the two interconnect wires individually. An LP-TX may support an optional Low Voltage Low Power (LVLP) operation, in which the maximum voltage is limited in comparison to the normal Low-Power mode. An LP-RX that meets the VIH specification in ***Section 9.2.2*** supports LVLP operation.

Presence of High-Speed and Low-Power functions is correlated. That is, if a Lane Module contains a HS-TX it shall also contain a LP-TX. A similar constraint holds for HS-RX and LP-RX.

If a Lane Module containing a LP-RX is powered, that LP-RX shall always be active and continuously monitor line levels. A LP-TX shall only be enabled when driving Low-Power states. The LP-CD function is only required for bi-directional operation. If present, the LP-CD function is enabled to detect contention situations while the LP-TX is driving Low-Power states. The LP-CD checks for contention before driving a new state on the line except in ULPS.

The activities of LP-TX, HS-TX, and HS-RX in a single Lane Module are mutually exclusive, except for some short crossover periods. For detailed specification of the Line side Clock and Data signals, and the HS-TX, HS-RX, LP-TX, LP-RX and LP-CD functions, see ***Section 9*** and ***Section 10***.

For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched. This means for each HS and LP transmit or receive function on one side of the Lane Interconnect, a complementary HS or LP receive or transmit function must be present on the other side. In addition, a Contention Detector is needed in any Lane Module that combines TX and RX functions.

5.2 Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

5.3 High Frequency Clock Generation

In many cases a PLL Clock Multiplier is needed for the high frequency clock generation at the Master Side. The D-PHY specification uses an architectural model where a separate Clock Multiplier Unit outside the PHY generates the required high frequency clock signals for the PHY. Whether this Clock Multiplier Unit in practice is integrated inside the PHY is left to the implementer.

5.4 Clock Lane, Data Lanes and the PHY-Protocol Interface

A complete Link contains, beside Lane Modules, a PHY Adapter Layer that ties all Lanes, the Clock Multiplier Unit, and the PHY Protocol Interface together. ***Figure 2*** shows a PHY configuration example for a Link with two Data Lanes plus a separate Clock Multiplier Unit. The PHY Adapter Layer, though a component of a PHY, is not within the scope of this specification.

The logical PHY-Protocol interface (PPI) for each individual Lane includes a set of signals to cover the functionality of that Lane. As shown in ***Figure 2***, Clock signals may be shared for all Lanes. The reference clock and control signals for the Clock Multiplier Unit are not within the scope of this specification.

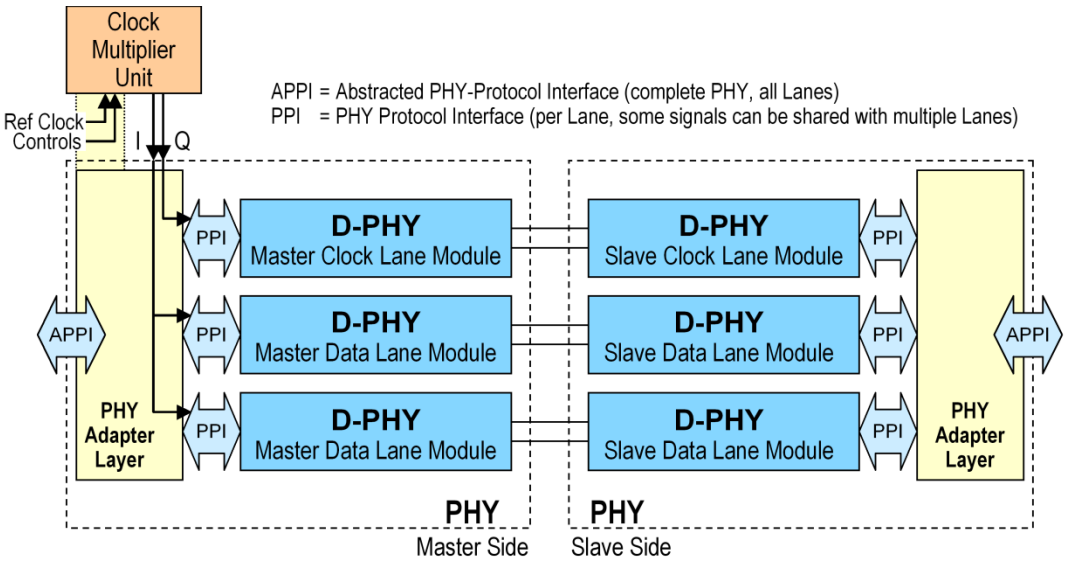

Figure 2 Two Data Lane PHY Configuration

5.5 Selectable Lane Options

A PHY configuration consists of one Clock Lane and one or more Data Lanes. All Data Lanes shall support High-Speed transmission and Escape mode in the Forward direction.

There are two main types of Data Lanes:

- Bi-directional (featuring Turnaround and some Reverse communication functionality)
- Unidirectional (without Turnaround or any kind of Reverse communication functionality)

Bi-directional Data Lanes shall include one or both of the following Reverse communication options:

- High-Speed Reverse data communication
- Low-Power Reverse Escape mode (including or excluding LPDT)

All Lanes shall include Escape mode support for ULPS and Triggers in the Forward direction. Other Escape mode functionality is optional; all possible Escape mode features are described in ***Section 6.6***. Applications shall define what additional Escape mode functionality is required and, for bi-directional Lanes, shall select Escape mode functionality for each direction individually.

This results in many options for complete PHY Configurations. The degrees of freedom are:

- Single or Multiple Data Lanes
- Bi-directional and/or Unidirectional Data Lane (per Lane)
- Supported types of Reverse communication (per Lane)
- Functionality supported by Escape mode (for each direction per Lane)
- Data transmission can be with 8-bit raw data (default) or using 8b9b encoded symbol (see Annex C)

Figure 3 is a flow graph of the option selection process. Practical configuration examples can be found in ***Section 5.7***.

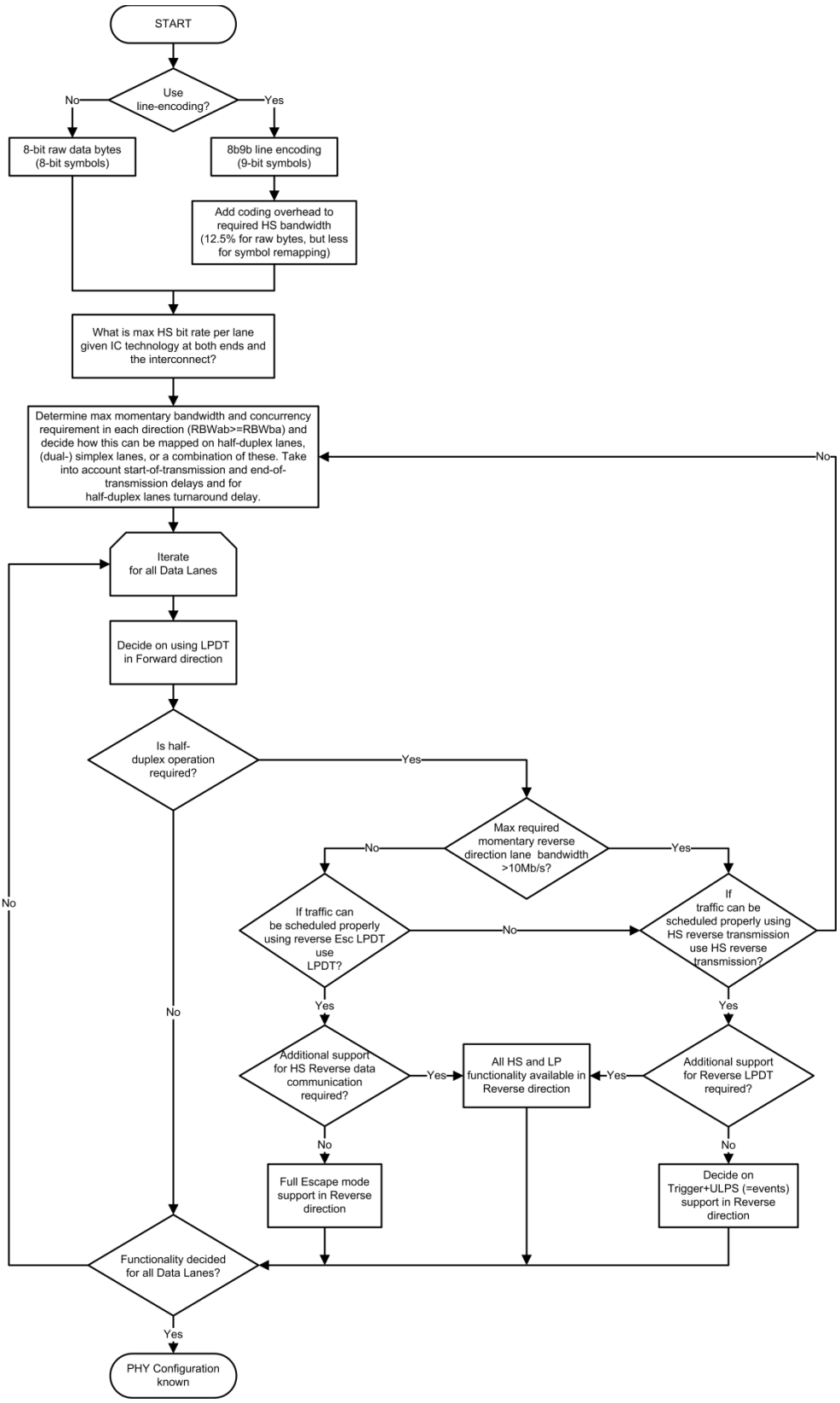

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Figure 3 Option Selection Flow Graph

5.6 Lane Module Types

The required functions in a Lane Module depend on the Lane type and which side of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. See ***Figure 3*** for more information on selecting Lane options.

Figure 4 shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane Types. The requirements for the 'Control and Interface Logic' (CIL) function depend on the Lane type and Lane side. ***Section 6*** and ***Annex A*** implicitly specify the contents of the CIL function. The actual realization is left to the implementer.

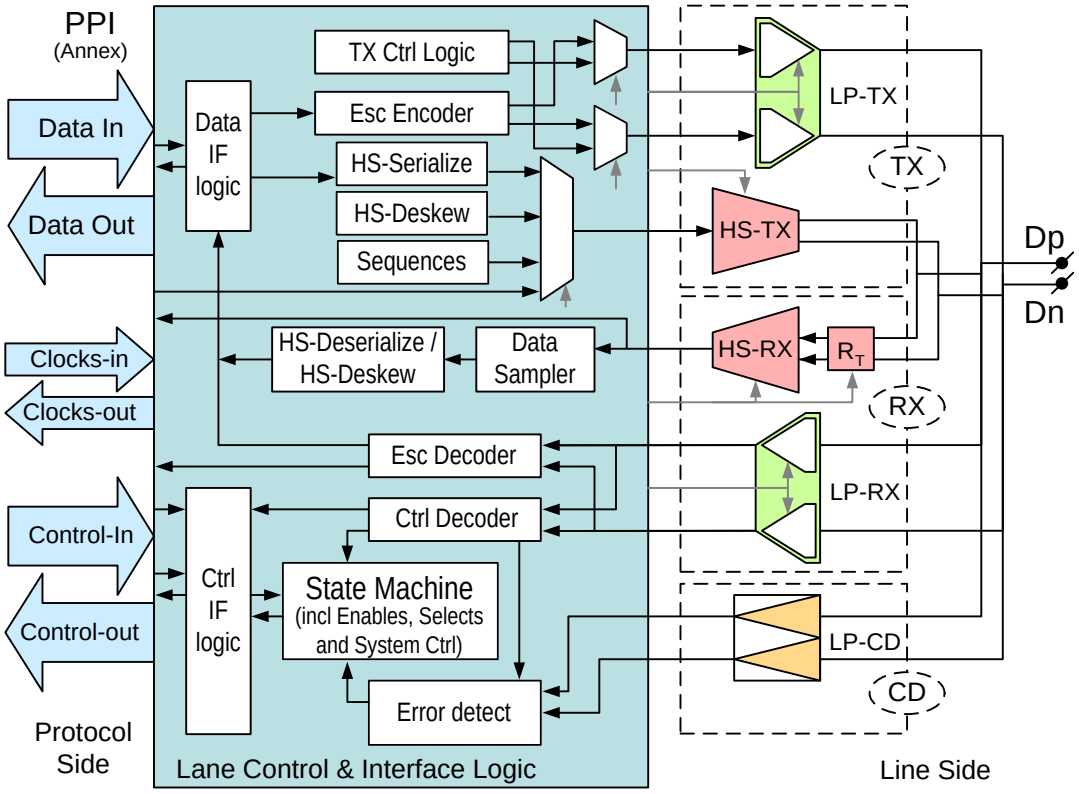


Figure 4 Universal Lane Module Architecture

Of course, stripped-down versions of the Universal Lane Module that just support the required functionality for a particular Lane type are possible. These stripped-down versions are identified by the acronyms in ***Table 1***. For simplification reasons, any of the four identification characters can be replaced by an X, which means that this can be any of the available options. For example, a CIL-MFEN is therefore a stripped-down CIL function for the Master Side of a Unidirectional Lane with Escape mode functionality only in the Forward direction. A CIL-SRXX is a CIL function for the Slave Side of a Lane with support for Bi-directional High-Speed communication and any allowed subset of Escape mode.

Note that a CIL-XFXN implies a unidirectional Link, while either a CIL-XRXX or CIL-XXXY block implies a bidirectional Link. Note that Forward 'Escape' (ULPS) entry for Clock Lanes is different than Escape mode entry for Data Lanes.

Table 1 Lane Type Descriptors

Prefix	Lane Interconnect Side	High-Speed Capabilities	Forward Direction Escape Mode Features Supported	Reverse Direction Escape Mode Features Supported[1]
CIL-	M – Master S – Slave X – Don't Care	F – Forward Only R – Reverse and Forward X – Don't Care[2]	A – All (including LPDT) E – events – Triggers and ULPS Only X – Don't Care	A – All (including LPDT) E – events – Triggers and ULPS Only N – None Y – Any (A, E, or A and E) X – Don't Care
		C – Clock	N – Not Applicable	N – Not Applicable

Note:

1. *"Any" is any combination of one or more functions.*
2. *Only valid for Data Lanes, means "F" or "R".*

The recommend PHY Protocol Interface contains Data-in and Data-out in byte format, Input and/or output Clock signals and Control signals. Control signals include requests, handshakes, test settings, and initialization. A proposal for a logical internal interface is described in Annex A. Although not a requirement it may be very useful to use the proposed PPI. For external use on IC's an implementation may multiplex many signals on the same pins. However, for power efficiency reasons, the PPI is normally within an IC.

5.6.1 Unidirectional Data Lane

For a Unidirectional Data Lane the Master Module shall contain at least a HS-TX, a LP-TX, and a CIL-MFXN function. The Slave side shall contain at least a HS-RX, a LP-RX and a CIL-SFXN.

5.6.2 Bi-directional Data Lanes

A bi-directional Data Lane Module includes some form of reverse communication; either High-Speed Reverse Communication, Reverse Escape mode, or both. The functions required depend on what methods of Reverse communication are included in the Lane Module.

5.6.2.1 Bi-directional Data Lane without High-Speed Reverse Communication

A bi-directional Data Lane Module without High-Speed Reverse Communication shall include a Reverse Escape mode. The Master-side Lane Module includes a HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MFXY. The Slave-side consists of a HS-RX, LP-RX, LP-TX, LP-CD and a CIL-SFXY.

5.6.2.2 Bi-directional Data Lane with High-Speed Reverse Communication

A bi-directional Data Lane Module with High-Speed Reverse Communication shall include a Reverse Escape mode. The Master-side Lane Module includes a HS-TX, HS-RX, LP-TX, LP-RX, LP-CD, and CIL-MRXX. The Slave-side consists of a HS-RX, HS-TX, LP-RX, LP-TX, LP-CD and a CIL-SRXX.

This type of Lane Module may seem suitable for both Master and Slave side but because of the asymmetry of the Link one side shall be configured as Master and the other side as Slave.

5.6.3 Clock Lane

For the Clock Lane, only a limited set of line states is used. However, for Clock Transmission and Low-Power mode the same TX and RX functions are required as for Unidirectional Data Lanes. A Clock Lane Module for the Master Side therefore contains a HS-TX, LP-TX, and a CIL-MCNN function, while the Slave Side Module includes a HS-RX, a LP-RX and a CIL-SCNN function.

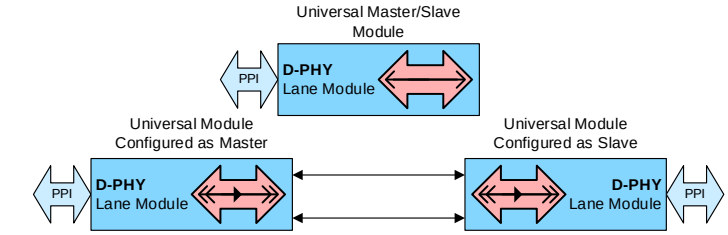
Note that the required functionality for a Clock Lane is similar, but not identical, to a Unidirectional Data Lane. The High-Speed DDR clock is transmitted in quadrature phase with Data signals instead of in-phase. In addition, the Clock Lane Escape mode entry is different than that used for Data Lanes. Furthermore, since a Clock Lane only supports ULPS, an Escape mode entry code is not required.

The internal clock signals with the appropriate phases are generated outside the PHY and delivered to the individual Lanes. The realization of the Clock generation unit is outside the scope of this specification. The quality of the internal clock signals shall be sufficient to meet the timing requirement for the signals as specified in ***Section 10***.

5.7 Configurations

This section outlines several common PHY configurations but should not be considered an exhaustive list of all possible arrangements. Any other configuration that does not violate the requirements of this document is also allowed.

In order to create an abstraction level, the Lane Modules are represented in this section by Lane Module Symbols. ***Figure 5*** shows the syntax and meaning of symbols.



Legend:

This	Other Options	Meaning
		Supported Directions for High-Speed Data Transmission (Bi-directional or Unidirectional)
		Clock Lane
		Supported Directions for Escape mode excluding LPDT (Bi-directional or Forward Only)
		Supported Directions for Escape mode including LPDT (Bi-directional, Forward Only or Reverse Only)
→	←	Clock Direction (by definition from Master to Slave, must point in the same direction as the "Clock Only Lane" arrow)
PPI		PPI: PHY-Protocol Interface

Figure 5 Lane Symbol Macros and Symbols Legend

For multiple Data Lanes a large variety of configurations is possible. ***Figure 6*** shows an overview of symbolic representations for different Lane types. The acronyms mentioned for each Lane type represent the functionality of each module in a short way. This also sets the requirements for the CIL function inside each Module.

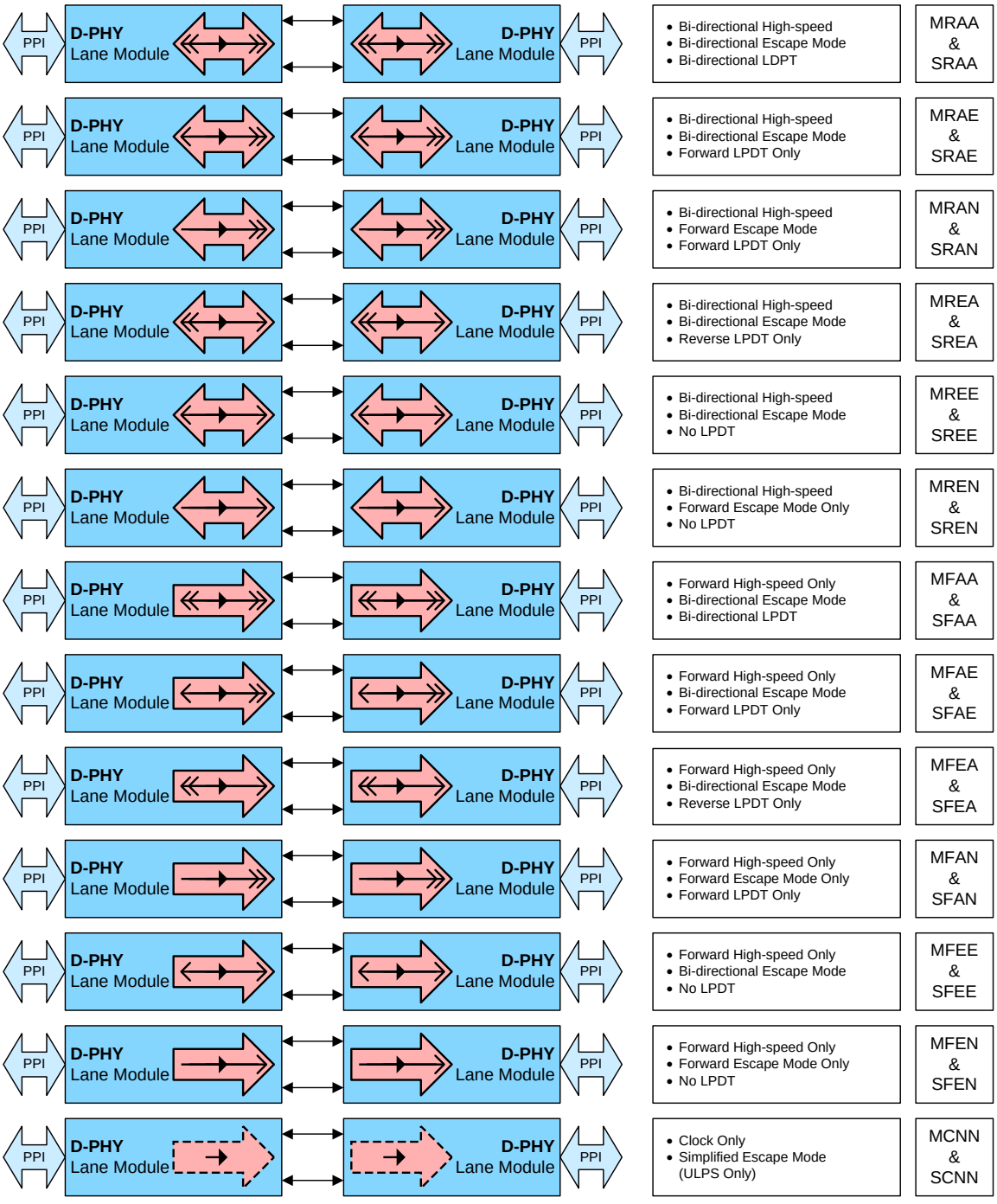


Figure 6 All Possible Data Lane Types and a Basic Unidirectional Clock Lane

5.7.1 Unidirectional Configurations

All unidirectional configurations are constructed with a Clock Lane and one or more Unidirectional Data Lanes. Two basic configurations can be distinguished: Single Data Lane and Multiple Data Lanes. For completeness a Dual-Simplex configuration is also shown. At the PHY level there is no difference between a Dual-Simplex configuration and two independent unidirectional configurations.

5.7.1.1 PHY Configuration with a Single Data Lane

This configuration includes one Clock Lane and one Unidirectional Data Lane from Master to Slave. Communication is therefore only possible in the Forward direction. ***Figure 7*** shows an example configuration without LPDT. This configuration requires four interconnect signal wires.

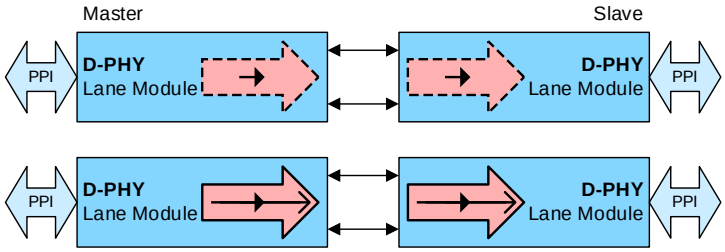


Figure 7 Unidirectional Single Data Lane Configuration

5.7.1.2 PHY Configuration with Multiple Data Lanes

This configuration includes one Clock Lane and multiple Unidirectional Data Lanes from Master to Slave. Bandwidth is extended, but communication is only possible in the Forward direction. The PHY specification does not require all Data Lanes to be active simultaneously. In fact, the Protocol layer controls all Data Lanes individually. ***Figure 8*** shows an example of this configuration for three Data Lanes. If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

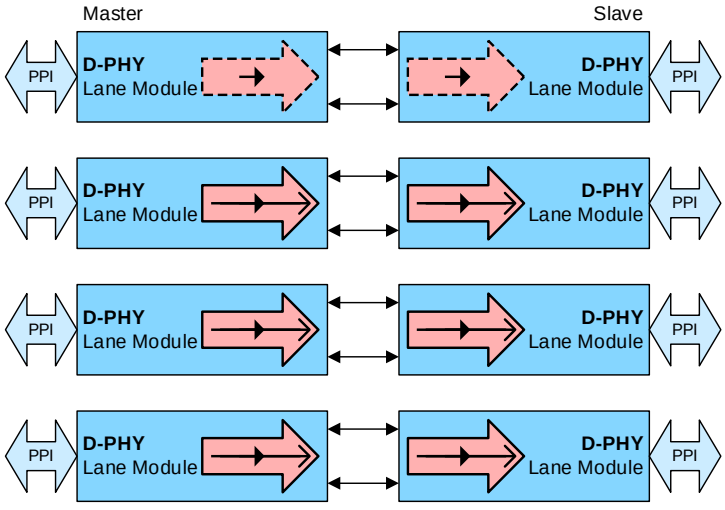


Figure 8 Unidirectional Multiple Data Lane Configuration without LPDT

5.7.1.3 Dual-Simplex (Two Directions with Unidirectional Lanes)

This case is the same as two independent (dual), unidirectional (simplex) Links: one for each direction. Each direction has its own Clock Lane and may contain either a single, or multiple, Data Lanes. Please note that the Master and Slave side for the two different directions are opposite. The PHY configuration for each

direction shall comply with the D-PHY specifications. As both directions are conceptually independent, the bit rates for each direction do not have to match. However, for practical implementations, it is attractive to match rates and share some internal signals as long as both Links fulfill all specifications externally. ***Figure 9*** shows an example of this dual PHY configuration.

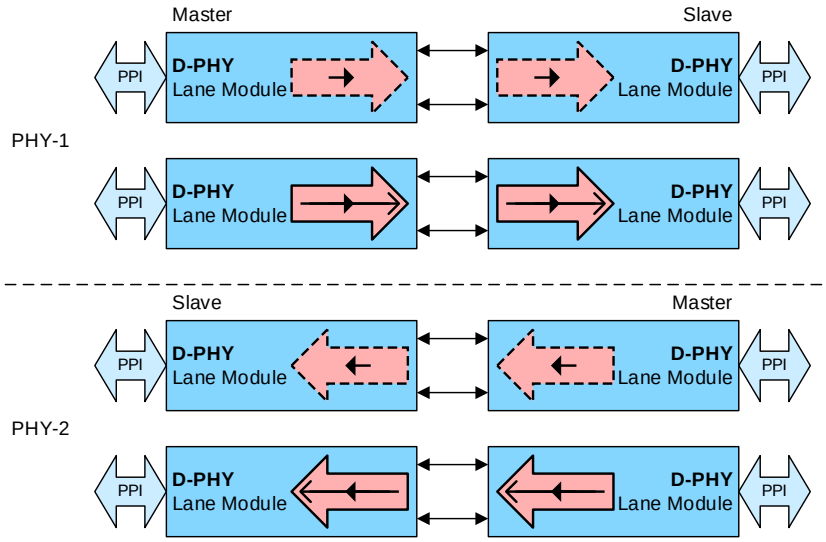


Figure 9 Two Directions Using Two Independent Unidirectional PHYs without LPDT

5.7.2 Bi-Directional Half-Duplex Configurations

Bi-directional configurations consist of a Clock Lane and one or more bi-directional Data Lanes. Half-duplex operation enables bi-directional traffic across shared interconnect wires. This configuration saves wires compared to the Dual-Simplex configuration. However, time on the Link is shared between Forward and Reverse traffic and Link Turnaround. The High-Speed bit rate in the Reverse direction is, by definition, one-fourth of the bit rate in the Forward direction. LPDT can have similar rates in the Forward and Reverse directions. This configuration is especially useful for cases with asymmetrical data traffic.

5.7.2.1 PHY Configurations with a Single Data Lane

This configuration includes one Clock Lane and one of any kind of bi-directional Data Lane. This allows time-multiplexed data traffic in both Forward and Reverse directions. ***Figure 10*** shows this configuration with a Data Lane that supports both High-Speed and Escape (without LPDT) communication in both directions. Other possibilities are that only one type of reverse communication is supported or LPDT is also included in one or both directions. All these configurations require four interconnect wires.

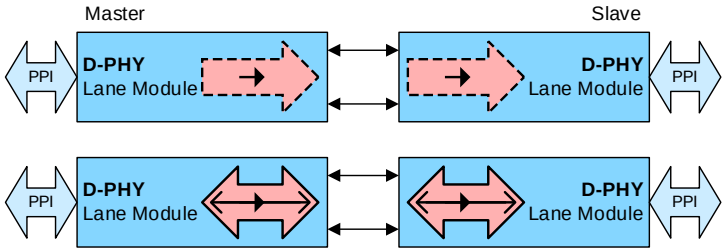


Figure 10 Bidirectional Single Data Lane Configuration

5.7.2.2 PHY Configurations with Multiple Data Lanes

This configuration includes one Clock Lane and multiple bi-directional Data Lanes. Communication is possible in both the Forward and Reverse direction for each individual Lane. The maximum available bandwidth scales with the number of Lanes for each direction. The PHY specification does not require all Data Lanes to be active simultaneously or even to be operating in the same direction. In fact, the Protocol layer controls all Data Lanes individually. ***Figure 11*** shows an example configuration with two Data Lanes. If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

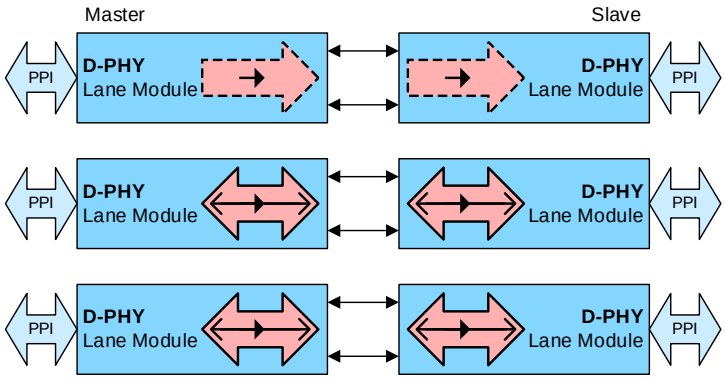


Figure 11 Bi-directional Multiple Data Lane Configuration

5.7.3 Mixed Data Lane Configurations

Instead of using only one Data Lane type, PHY configurations may combine different unidirectional and bi-directional Data Lane types. ***Figure 12*** shows an example configuration with one bi-directional and one unidirectional Data Lane, both without LPDT.

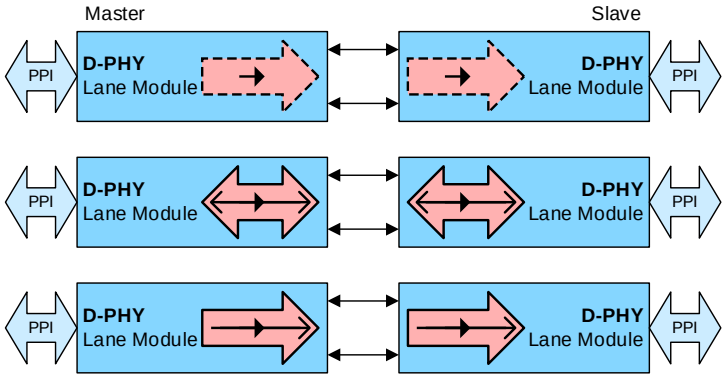


Figure 12 Mixed Type Multiple Data Lane Configuration

6 Global Operation

This section specifies operation of the D-PHY including signaling types, communication mechanisms, operating modes and coding schemes. Detailed specifications of the required electrical functions can be found in ***Section 9***.

6.1 Transmission Data Structure

During High-Speed, or Low-Power, transmission, the Link transports payload data provided by the protocol layer to the other side of the Link. This section specifies the restrictions for the transmitted and received payload data.

6.1.1 Data Units

The minimum payload data unit shall be one byte. Data provided to a TX and taken from a RX on any Lane shall be an integer number of bytes. This restriction holds for both High-Speed and Low-Power data transmission in any direction.

6.1.2 Bit order, Serialization, and De-Serialization

For serial transmission, the data shall be serialized in the transmitting PHY and de-serialized in the receiving PHY. The PHY assumes no particular meaning, value or order of incoming and outgoing data.

6.1.3 Encoding and Decoding

Line coding is not required by this specification. However, if line coding is used, it shall be implemented according to Annex C.

6.1.4 Data Buffering

Data transmission takes place on protocol request. As soon as communication starts, the protocol layer at the transmit side shall provide valid data as long as it does not stop its transmission request. For Lanes that use line coding, control symbols can also be inserted into the transmission. The protocol on the receive side shall take the data as soon as delivered by the receiving PHY. The signaling concept, and therefore the PHY protocol handshake, does not allow data throttling. Any data buffering for this purpose shall be inside the protocol layer.

6.2 Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential-0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

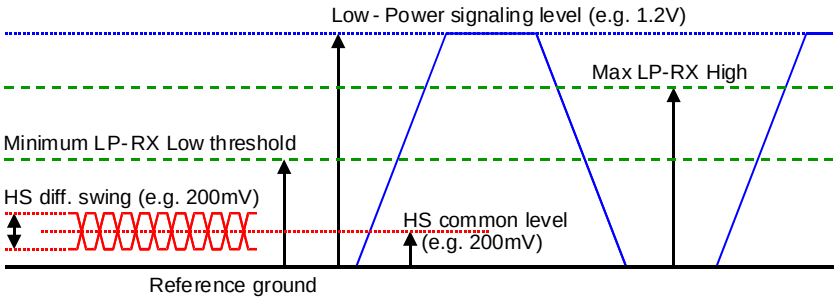


Figure 13 Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. ***Table 2*** lists all the states that can appear on a Lane during normal operation. Detailed specifications of electrical levels can be found in ***Section 9***.

All LP state periods shall be at least T_{LPX} in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least $2*T_{LPX}$, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Table 2 Lane State Descriptions

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

Note:

1. *During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.*
2. *If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11).*

6.3 Operating Modes: Control, High-Speed, and Escape

During normal operation a Data Lane will be either in Control or High-Speed mode. High-Speed Data transmission happens in bursts and starts from and ends at a Stop state (LP-11), which is by definition in Control mode. The Lane is only in High-Speed mode during Data bursts. The sequence to enter High-Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a LP-11 is received. The Escape mode can only be entered via a request within Control mode. The Data Lane shall always exit Escape mode and return to Control mode after detection of a Stop state. If not in High-Speed or Escape mode the Data Lane shall stay in Control mode. For Data Lanes and for Clock Lanes the Stop state serves as general standby state and may last for any period of time > T_{LPX}. Possible events starting from the Stop state are High-Speed Data Transmission request (LP-11, LP-01, LP-00), Escape mode request (LP-11, LP-10, LP-00, LP-01, LP-00) or Turnaround request (LP-11, LP-10, LP-00, LP-10, LP-00).

6.4 High-Speed Data Transmission

High-Speed Data Transmission occurs in bursts. To aid receiver synchronization, data bursts shall be extended on the transmitter side with a leader and trailer sequence and shall be eliminated on the receiver side. These leader and trailer sequences can therefore only be observed on the transmission lines.

Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a Data Lane shall remain in the Stop state, unless a Turnaround or Escape request is presented on the Lane. During a HS Data Burst the Clock Lane shall be in High-Speed mode, providing a DDR Clock to the Slave side.

6.4.1 Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

6.4.2 Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. ***Table 3*** describes the sequence of events on TX and RX side.

Table 3 Start-of-Transmission Sequence

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS\text{-}PREPARE}$	Observes transition form LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D\text{-}TERM\text{-}EN}$
Enables High-Speed driver and disables Low-Power drivers simultaneously.	
Drives HS-0 for a time $T_{HS\text{-}ZERO}$	Enables HS-RX and waits for timer $T_{HS\text{-}SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence ‘00011101’ beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence ‘011101’
Continues to Transmit High-Speed payload data	
	Receives payload data

6.4.3 End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. ***Table 4*** shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

Table 4 End-of-Transmission Sequence

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

6.4.4 HS Data Transmission Burst

Figure 14 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane. The handshake with the protocol-layer is described in Annex A.

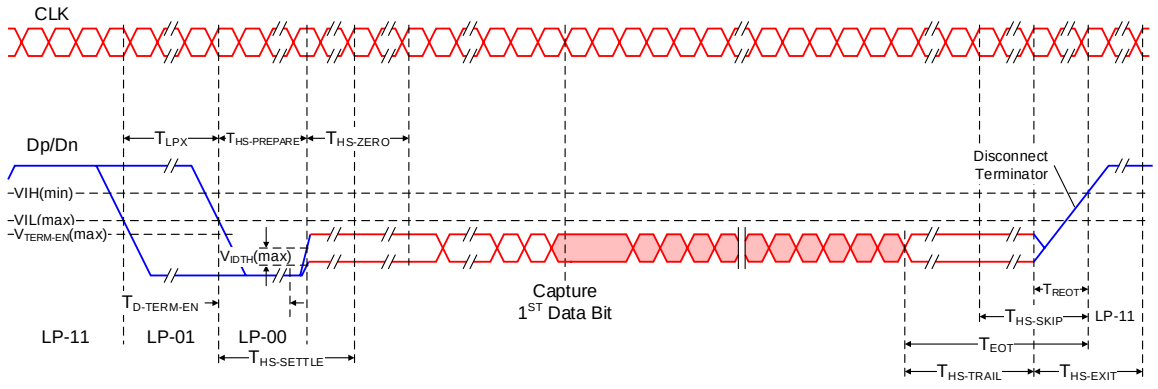


Figure 14 High-Speed Data Transmission in Bursts

460 ***Figure 15*** shows the state machine for High-Speed data transmission that is described in ***Table 5***.

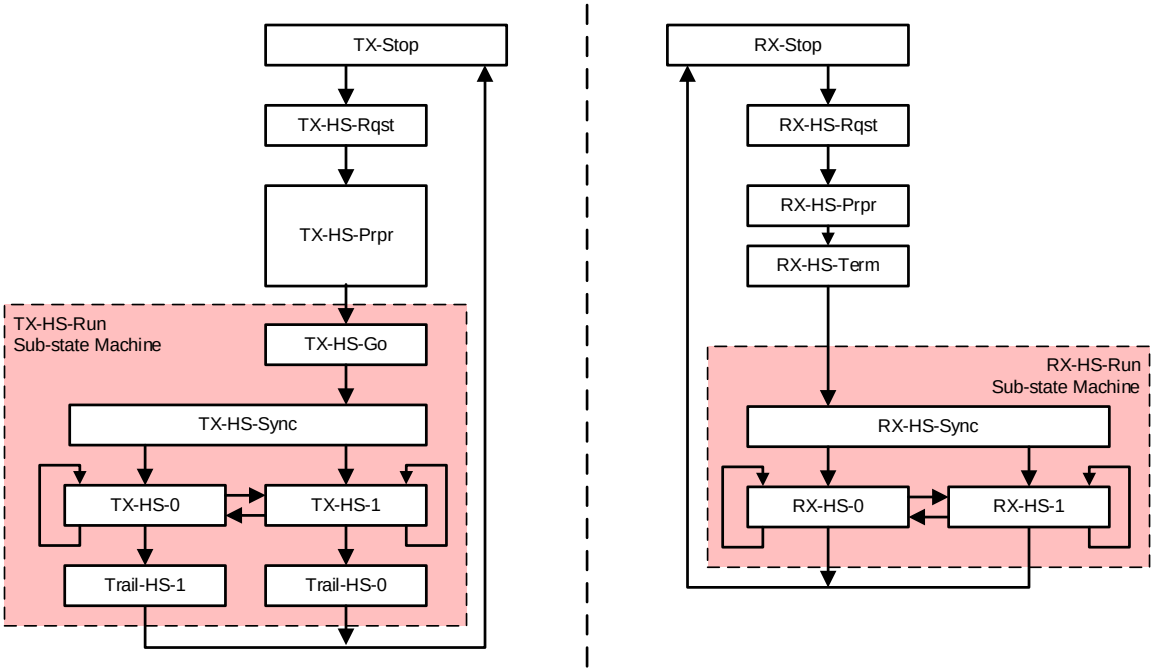


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Figure 15 TX and RX State Machines for High-Speed Data Transmission

462 **Table 5 High-Speed Data Transmission State Machine Description**

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-HS-Prpr	End of timed interval T_{LPX}
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{HS\text{-}PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-Sync	End of timed interval $T_{HS\text{-}ZERO}$
TX-HS-Sync	Transmit sequence HS-00011101	TX-HS-0	After Sync sequence if first payload data bit is 0
		TX-HS-1	After Sync sequence if first payload data bit is 1
TX-HS-0	Transmit HS-0	TX-HS-0	Send another HS-0 bit after a HS-0 bit
		TX-HS-1	Send a HS-1 bit after a HS-0 bit
		Trail-HS-1	Last payload bit is HS-0, trailer sequence is HS-1
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-1 bit after a HS-0 bit
		TX-HS-1	Send another HS-1 bit after a HS-1
		Trail-HS-0	Last payload bit is HS-1, trailer sequence is HS-0
Trail-HS-0	Transmit HS-0	TX-Stop	End of timed interval $T_{HS\text{-}TRAIL}$
Trail-HS-1	Transmit HS-1	TX-Stop	End of timed interval $T_{HS\text{-}TRAIL}$
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX- HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS- Prpr	Receive LP-00	RX-HS-Term	End of timed interval $T_{D\text{-}TERM\text{-}EN}$
RX-HS-Term	Receive LP-00	RX-HS-Sync	End of timed interval $T_{HS\text{-}SETTLE}$
RX-HS-Sync	Receive HS sequence …00000011101	RX-HS-0	Proper match found for Sync sequence in HS stream, the following bits are payload data. (When deskew is supported, bit errors in the Leader sequence are not tolerated.)
		RX-HS-1	
RX-HS-0	Receive HS-0	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11
RX-HS-1	Receive HS-1	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11

Note:

Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.5 Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround. Link Turnaround shall be handled completely in Control mode. ***Table 6*** lists the sequence of events during Turnaround.

Table 6 Link Turnaround Sequence

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Drives Stop state (LP-11)	Observes Stop state
Drives LP-Rqst state (LP-10) for a time T_{LPX}	Observes transition from LP-11 to LP-10 states
Drives Bridge state (LP-00) for a time T_{LPX}	Observes transition from LP-10 to LP-00 states
Drives LP-10 for a time T_{LPX}	Observes transition from LP-00 to LP-10 states
Drives Bridge state (LP-00) for a time $T_{TA\text{-}GO}$	Observes the transition from LP-10 to Bridge state and waits for a time $T_{TA\text{-}SURE}$. After correct completion of this time-out this side knows it is in control.
	Drives Bridge state (LP-00) for a period $T_{TA\text{-}GET}$
Stops driving the Lines and observes the Line states with its LP-RX in order to see an acknowledgement.	
	Drives LP-10 for a period T_{LPX}
Observes LP-10 on the Lines, interprets this as acknowledge that the other side has indeed taken control. Waits for Stop state to complete Turnaround procedure.	
	Drives Stop state (LP-11) for a period T_{LPX}
Observes transition to Stop state (LP-11) on the Lines, interprets this as Turnaround completion acknowledgement, switches to normal LP receive mode and waits for further actions from the other side	

Figure 16 shows the Turnaround procedure graphically.

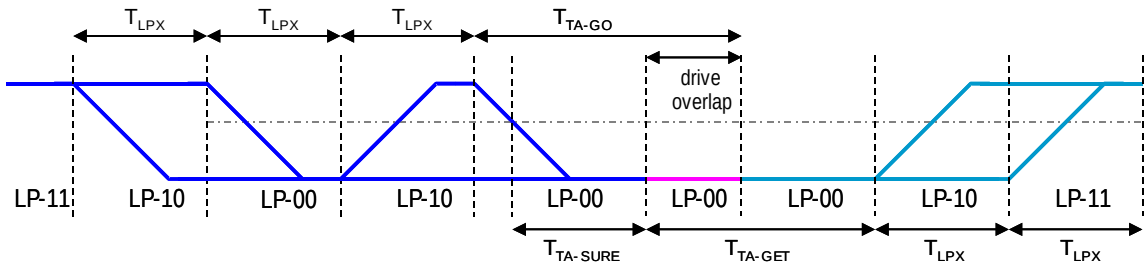

Figure 16 Turnaround Procedure

The Low-Power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low-Power State Periods, T_{LPX}, is constrained to ensure proper Turnaround behavior. See ***Table 14*** for the ratio of $T_{LPX(MASTER)}$ to $T_{LPX(SLAVE)}$.

The Turnaround procedure can be interrupted if the Lane is not yet driven into TX-LP-Yield by means of driving a Stop state. Driving the Stop state shall abort the Turnaround procedure and return the Lane to the Stop state. The PHY shall ensure against interruption of the procedure after the end of TX-TA-Rqst, RX-TA-Rqst, or TX-TA-GO. Once the PHY drives TX-LP-Yield, it shall not abort the Turnaround procedure. The Protocol may take appropriate action if it determines an error has occurred because the Turnaround procedure did not complete within a certain time. See ***Section 7.3.5*** for more details. ***Figure 17*** shows the Turnaround state machine that is described in ***Table 7***.

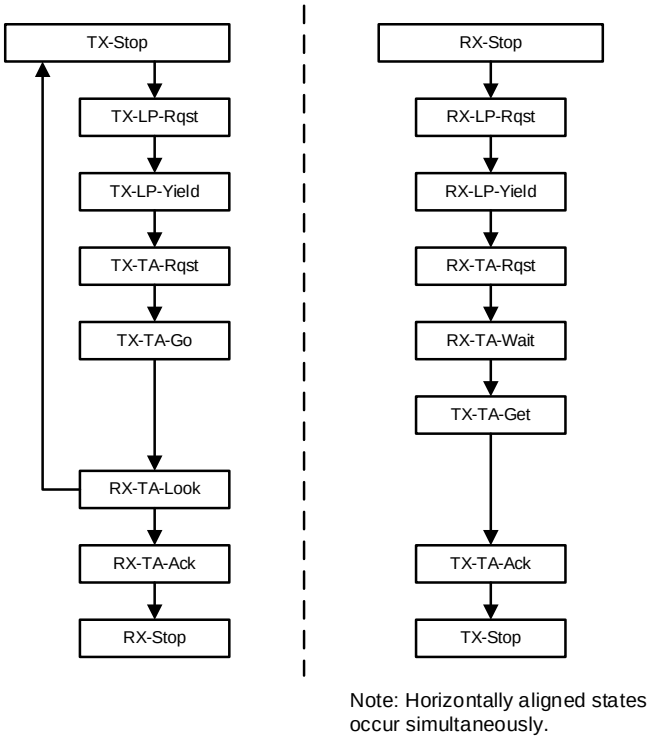

Figure 17 Turnaround State Machine

482 **Table 7 Turnaround State Machine Description**

State	Line Condition/State	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Turnaround
TX-LP-Rqst	Transmit LP-10	TX-LP-Yield	End of timed interval T_{LPX}
TX-LP-Yield	Transmit LP-00	TX-TA-Rqst	End of timed interval T_{LPX}
TX-TA-Rqst	Transmit LP-10	TX-TA-Go	End of timed interval T_{LPX}
TX-TA-Go	Transmit LP-00	RX-TA-Look	End of timed interval $T_{TA\text{-}GO}$
RX-TA-Look	Receive LP-00	RX-TA-Ack	Line transition to LP-10
RX-TA-Ack	Receive LP-10	RX-Stop	Line transition to LP-11
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Yield	Line transition to LP-00
RX-LP-Yield	Receive LP-00	RX-TA-Rqst	Line transition to LP-10
RX-TA-Rqst	Receive LP-10	RX-TA-Wait	Line transition to LP-00
RX-TA-Wait	Receive LP-00	TX-TA-Get	End of timed interval $T_{TA\text{-}SURE}$
TX-TA-Get	Transmit LP-00	TX-TA-Ack	End of timed interval $T_{TA\text{-}GET}$
TX-TA-Ack	Transit LP-10	TX-Stop	End of timed interval T_{LPX}

Note:

During RX-TA-Look, the protocol may cause the PHY to transition to TX-Stop.

During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.6 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all available features.

A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. ***Table 8*** lists all currently available Escape mode commands and actions. All unassigned commands are reserved for future expansion.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a Data Lane in this mode does not depend on the Clock Lane. The complete Escape mode action for a Trigger-Reset command is shown in ***Figure 18***.

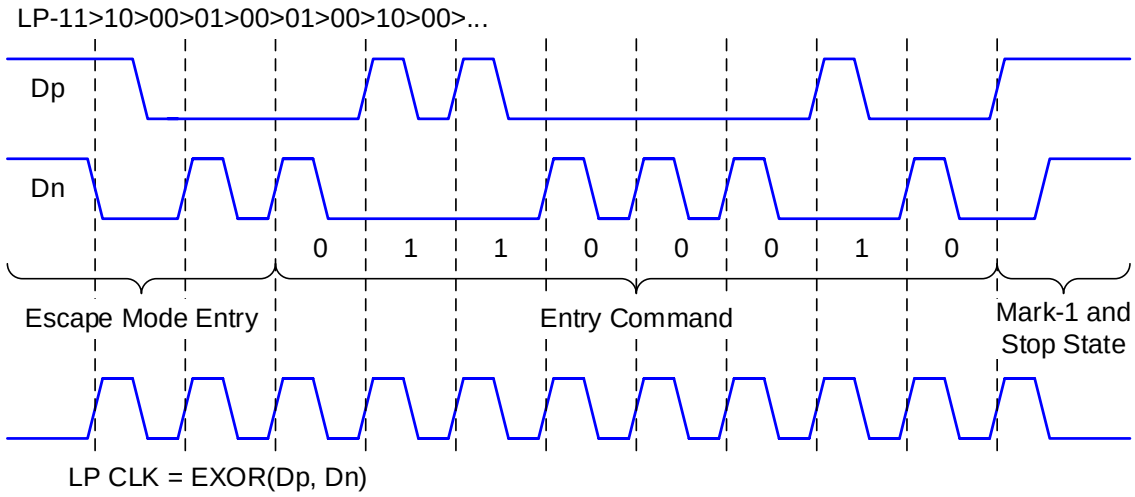

Figure 18 Trigger-Reset Command in Escape Mode

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a 'zero-bit' and it shall send a Mark-1 followed by a Space to transmit a 'one-bit'. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state. The Clock can be derived from the two Line signals, Dp and Dn, by means of an exclusive-OR function. The length of each individual LP state period shall be at least $T_{LPX,MIN}$.

Table 8 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Entry sequence for HS Test Mode	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

6.6.1 Remote Triggers

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface.

Figure 18 shows an example of an Escape mode Reset-Trigger action. The Lane enters Escape mode via the Escape mode Entry procedure. If the Entry Command Pattern matches the Reset-Trigger Command a Trigger is flagged to the protocol at the receive side via the logical PPI. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

Note that Trigger signaling including Reset-Trigger is a generic messaging system. The Trigger commands do not impact the behavior of the PHY itself. Therefore, Triggers can be used for any purpose by the Protocol layer.

6.6.2 Low-Power Data Transmission

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode.

Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. ***Figure 19*** shows a two-byte transmission with a pause period between the two bytes.

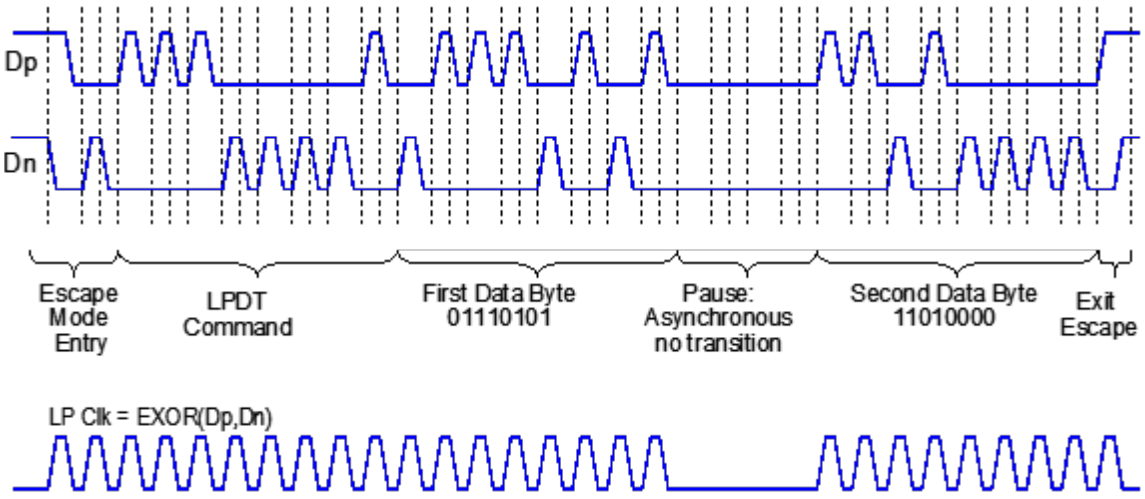

Figure 19 Two Data Byte Low-Power Data Transmission Example

Using LPDT, a Low-Power (Bit) Clock signal ($f_{MOMENTARY}$ < 20MHz) provided to the transmit side is used to transmit data. Data reception is self-timed by the bit encoding. Therefore, a variable clock rate can be allowed. At the end of LPDT the Lane shall return to the Stop state.

6.6.3 Ultra-Low Power State

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length T_{WAKEUP} followed by a Stop state. Annex A describes an example of an exit procedure and a procedure to control the length of time spent in the Mark-1 state.

6.6.4 Escape Mode State Machine

The state machine for Escape mode operation is shown in ***Figure 20*** and described in ***Table 9***.

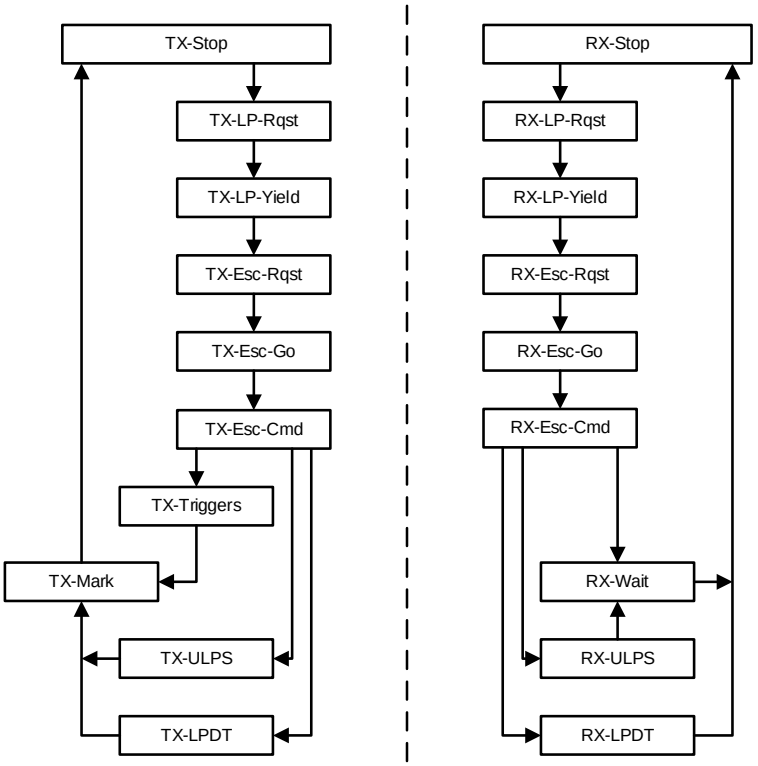

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Figure 20 Escape Mode State Machine

543 **Table 9 Escape Mode State Machine Description**

State	Line Condition/State	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Esc mode (PPI)
TX-LP-Rqst	Transmit LP-10	TX-LP-Yield	After time T_{LPX}
TX-LP-Yield	Transmit LP-00	TX-Esc-Rqst	After time T_{LPX}
TX-Esc-Rqst	Transmit LP-01	TX-Esc-Go	After time T_{LPX}
TX-Esc-Go	Transmit LP-00	TX-Esc-Cmd	After time T_{LPX}
TX-Esc-Cmd	Transmit sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	TX-Triggers	After a Trigger Command
		TX-ULPS	After Ultra-Low Power Command
		TX-LPDT	After Low-Power Data Transmission Command
TX-Triggers	Space state or optional dummy bytes for the purpose of generating clocks	TX-Mark	Exit of the Trigger State on request of Protocol (PPI)
TX-ULPS	Transmit LP-00	TX-Mark	End of ULP State on request of Protocol (PPI)
TX-LPDT	Transmit serialized, Spaced-One-Hot encoded payload data		After last transmitted data bit
TX-Mark	Mark-1	TX-Stop	Next driven state after time T_{LPX}, or T_{WAKEUP} if leaving ULP State
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Yield	Line transition to LP-00
RX-LP-Yield	Receive LP-00	RX-Esc-Rqst	Line transition to LP-01
RX-Esc-Rqst	Receive LP-01	RX-Esc-Go	Line transition to LP-00
RX-Esc-Go	Receive LP-00	RX-Esc-Cmd	Line transition out of LP-00
RX-Esc-Cmd	Receive sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	RX-Wait	After Trigger and Unrecognized Commands
		RX-ULPS	After Ultra-Low Power Command
		RX-LPDT	After Low-Power Data Transmission Command
RX-ULPS	Receive LP-00	RX-Wait	Line transition to LP-10
RX-LPDT	Receive serial, Spaced-One-Hot encoded payload data	RX-Stop	Line transition to LP-11 (Last state should be a Mark-1)
RX-Wait	Any, except LP-11	RX-Stop	Line transition to LP-11

Note:

During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.7 High-Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. Details of the Data-Clock relationship and timing specifications can be found in ***Section 10***.

A Clock Lane is similar to a Unidirectional Data Lane. However, there are some timing differences and a Clock Lane transmits a High-Speed DDR clock signal instead of data bits. Furthermore, the Low-Power mode functionality is defined differently for a Clock Lane than a Data Lane. A Clock Lane shall be unidirectional and shall not include regular Escape mode functionality. Only ULPS shall be supported via a special entry sequence using the LP-Rqst state. High-Speed Clock Transmission shall start from, and exit to, a Stop state.

The Clock Lane module is controlled by the Protocol via the Clock Lane PPI. The Protocol shall only stop the Clock Lane when there are no High-Speed transmissions active in any Data Lane.

The High-Speed Data Transmission start-up time of a Data Lane is extended if the Clock Lane is in Low-Power mode. In that case the Clock Lane shall first return to High-Speed operation before the Transmit Request can be handled.

The High-Speed Clock signal shall continue running for a period $T_{CLK\text{-}POST}$ after the last Data Lane switches to Low-Power mode and ends with a HS-0 state. The procedure for switching the Clock Lane to Low-Power mode is given in ***Table 10***. Note the Clock Burst always contains an even number of transitions as it starts and ends with a HS-0 state. This implies that the clock provides transitions to sample an even number of bits on any associated Data Lanes. Clock periods shall be reliable and according to the HS timing specifications. The procedure to return the Clock Lane to High-Speed Clock Transmission is given in ***Table 11***. Both Clock Start and Stop procedures are shown in ***Figure 21***.

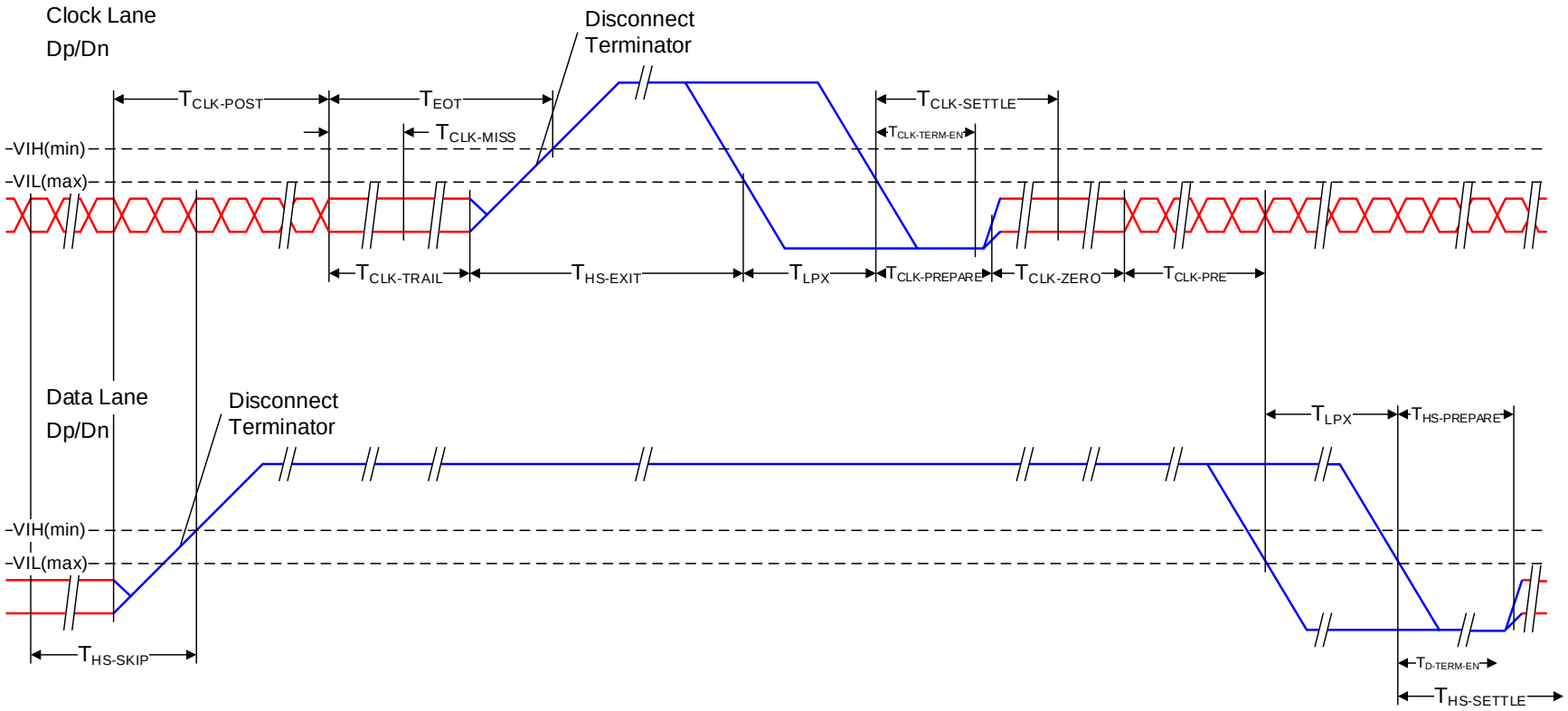

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Figure 21 Switching the Clock Lane between Clock Transmission and Low-Power Mode

568 **Table 10 Procedure to Switch Clock Lane to Low-Power Mode**

Master Side	Slave Side
Drives High-Speed Clock signal (Toggling HS-0/HS-1)	Receives High-Speed Clock signal (Toggling HS-0/HS-1)
Last Data Lane goes into Low-Power mode	
Continues to drives High-Speed Clock signal for a period $T_{CLK\text{-}POST}$ and ends with HS-0 state	
Drives HS-0 for a time $T_{CLK\text{-}TRAIL}$	Detects absence of Clock transitions within a time $T_{CLK\text{-}MISS}$, disables HS-RX then waits for a transition to the Stop state
Disables the HS-TX, enables LP-TX, and drives Stop state (LP-11) for a time $T_{HS\text{-}EXIT}$	
	Detects the Lines transitions to LP-11, disables HS termination, and enters Stop state

569 **Table 11 Procedure to Initiate High-Speed Clock Transmission**

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Req state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{CLK\text{-}PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines. Enables Line Termination after time $T_{CLK\text{-}TERM\text{-}EN}$
Enables High-Speed driver and disables Low-Power drivers simultaneously. Drives HS-0 for a time $T_{CLK\text{-}ZERO}$.	Enables HS-RX and waits for timer $T_{CLK\text{-}SETTLE}$ to expire in order to neglect transition effects
	Receives HS-signal
Drives the High-Speed Clock signal for time period $T_{CLK\text{-}PRE}$ before any Data Lane starts up	Receives High-Speed Clock signal

570 The Clock Lane state machine is shown in ***Figure 22*** and is described in ***Table 12***.

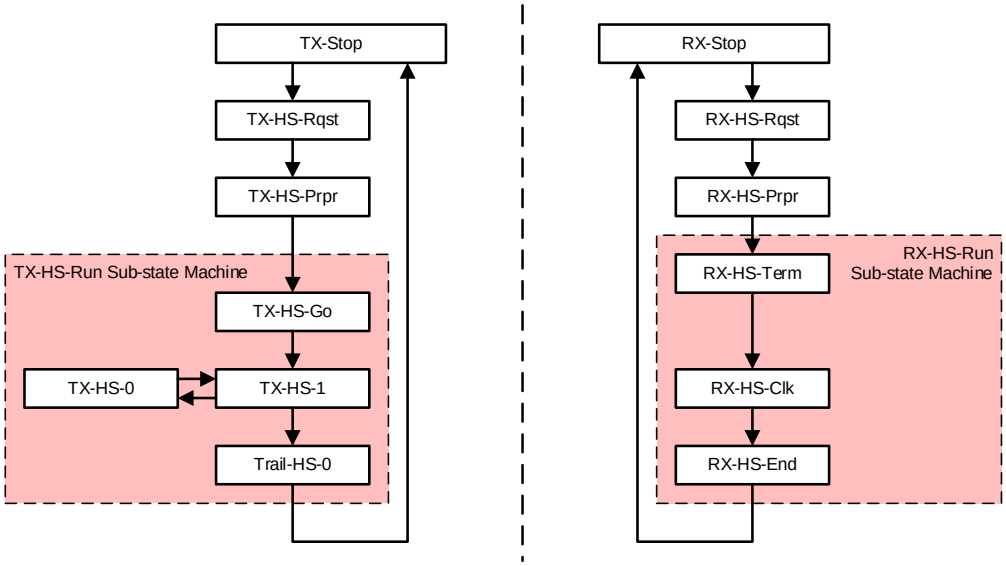

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Figure 22 High-Speed Clock Transmission State Machine

572 **Table 12 Description of High-Speed Clock Transmission State Machine**

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-HS-Prpr	End of timed interval T_{LPX}
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{CLK\text{-}PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-1	End of timed interval $T_{CLK\text{-}ZERO}$
TX-HS-0	Transmit HS-0	TX-HS-1	Send a HS-1 phase after a HS-0 phase: DDR Clock
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-0 phase after a HS-1 phase: DDR Clock
		Trail-HS-0	On request to put Clock Lane in Low-Power
Trail-HS-0	Transmit HS-0	TX-Stop	End of timed interval $T_{CLK\text{-}TRAIL}$
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX-HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS-Prpr	Receive LP-00	RX-HS-Term	End of timed interval $T_{CLK\text{-}TERM\text{-}EN}$
RX-HS-Term	Receive LP-00	RX-HS-Clk	End of timed interval $T_{CLK\text{-}SETTLE}$
RX-HS-Clk	Receive DDR-Q Clock signal	RX-Clk-End	Time-out $T_{CLK\text{-}MISS}$ on the period on the Clock Lane without Clock signal transitions
RX-HS-End	Receive HS-0	RX-HS-Stop	Line transition to LP-11

Note:

During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.8 Clock Lane Ultra-Low Power State

Although a Clock Lane does not include regular Escape mode, the Clock Lane shall support the Ultra-Low Power State.

A Clock Lane shall enter Ultra-Low Power State via a Clock Lane Ultra-Low Power State Entry procedure. In this procedure, starting from Stop state, the transmit side shall drive TX-ULPS-Rqst State (LP-10) and then drive TX-ULPS State (LP-00). After this, the Clock Lane shall enter Ultra-Low Power State. If an error occurs, and an LP-01 or LP-11 is detected immediately after the TX-ULPS-Rqst state, the Ultra-Low Power State Entry procedure shall be aborted, and the receive side shall wait for, or return to, the Stop state, respectively.

The receiving PHY shall flag the appearance of ULP State to the receive side Protocol. During this state the Lines are in the ULP State (LP-00). Ultra-Low Power State is exited by means of a Mark-1 TX-ULPS-Exit State with a length T_{WAKEUP} followed by a Stop State. Annex A describes an example of an exit procedure that allows control of the length of time spent in the Mark-1 TX-ULPS-Exit State.

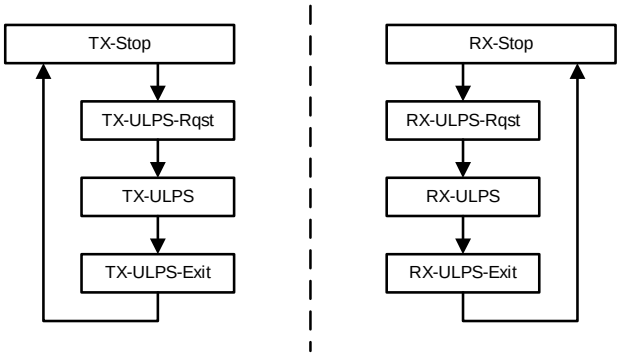

Figure 23 Clock Lane Ultra-Low Power State State Machine

Table 13 Clock Lane Ultra-Low Power State State Machine Description

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-ULPS-Rqst	On request of Protocol for Ultra-Low Power State
TX-ULPS-Rqst	Transmit LP-10	TX-ULPS	End of timed interval T_{LPX}
TX-ULPS	Transmit LP-00	TX-ULPS-Exit	On request of Protocol to leave Ultra-Low Power State
TX-ULPS-Exit	Transmit LP-10	TX-Stop	End of timed interval T_{WAKEUP}
RX-Stop	Receive LP-11	RX-ULPS-Rqst	Line transition to LP-10
RX-ULPS-Rqst	Receive LP-10	RX-ULPS	Line transition to LP-00
RX-ULPS	Receive LP-00	RX-ULPS-Exit	Line transition to LP-10
RX-ULPS-Exit	Receive LP-10	RX-Stop	Line transition to LP-11

Note:

During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.9 Global Operation Timing Parameters

Table 14 lists the ranges for all timing parameters used in this section. The values in the table assume a UI variation in the range defined by ΔUI (see ***Table 35***).

Transmitters shall support all transmitter-specific timing parameters defined in ***Table 14***.

Receivers shall support all Receiver-specific timing parameters in defined in ***Table 14***.

Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in ***Table 14*** for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver's datasheet.

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Table 14 Global Operation Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6, 8
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI			ns	5
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	5
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95		300	ns	6, 7
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	6
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI		6
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI		3, 5
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	5
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns	5

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85 ns + 6*UI		145 ns + 10*UI	ns	6
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns	6
$T_{HS-SYNC}$	Time that the transmitter drives the HS Data sync pattern	n*8			UI	3
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3, 5
T_{INIT}	See ***Section 6.11***.	100			µs	5
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	4, 5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns	5
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns	5
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2*T_{LPX}$	ns	5
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5

Note:

1. *The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.*
2. *If a > b then max(a, b) = a otherwise max(a, b) = b.*
3. *Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.*
4. *T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.*
5. *Transmitter-specific parameter.*
6. *Receiver-specific parameter.*
7. *The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.*
8. *During HS Test Mode the $T_{Clk-Miss}$ parameter should be used for re-initialization of pattern checkers. The device should only exit the HS Test mode in the cases described in **Section 12**.*

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6.10 System Power States

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State. For details on Ultra-Low Power State see ***Section 6.6.3*** and ***Section 6.8***. The transition between these modes shall be handled by the PHY.

6.11 Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer than T_{INIT}. The first Stop state longer than the specified T_{INIT} is called the Initialization period. The Master PHY itself shall be initialized by a system or Protocol input signal (PPI). The Master side shall ensure that a Stop State longer than T_{INIT} does not occur on the Lines before the Master is initialized. The Slave side shall ignore all Line states during an interval of unspecified length prior to the Initialization period. In multi-Lane configurations, all Lanes shall be initialized simultaneously.

Note that T_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for $T_{INIT,MASTER}$ and $T_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the D-PHY specification does place a minimum bound on the lengths of $T_{INIT,MASTER}$ and $T_{INIT,SLAVE}$, which each shall be no less than 100 µs. A protocol layer specification using the D-PHY specification may specify any values greater than this limit, for example, $T_{INIT,MASTER} \geq 1$ ms and $T_{INIT,SLAVE}$ = 500 to 800 µs.

Table 15 Initialization States

State	Entry Conditions	Exit State	Exit Conditions	Line Levels
Master Off	Power-down	Master Initialization	Power-up	Any LP level except Stop States for periods >100us
Master Init	Power-up or Protocol request	TX-Stop	A First Stop state for a period longer than $T_{INIT,MASTER}$ as specified by the Protocol	Any LP signaling sequence that ends with a long Initialization Stop state
Slave Off	Power-down	Any LP state	Power-up	Any
Slave Init	Power-up or Protocol request	RX-Stop	Observe Stop state at the inputs for a period $T_{INIT,SLAVE}$ as specified by the Protocol	Any LP signaling sequence which ends with the first long Initialization Stop period

6.12 Calibration

Receiver deskew shall be initiated by the transmitter for the DUT's supporting > 1.5 Gbps. The transmitter shall send a special deskew burst, as shown in ***Figure 24***. When operating above 1.5 Gbps or changing to any rate above 1.5 Gbps, an initial deskew sequence shall be transmitted before High-Speed Data Transmission in normal operation. When operating at or below 1.5 Gbps, the transmission of initial deskew sequence is optional. Periodic deskew is optional irrespective of data rate.

When changing states, for example from ULPS to HS, transmission of any deskew sequence is optional, provided HS operation resumes at a rate for which an initial deskew sequence has previously been transmitted.

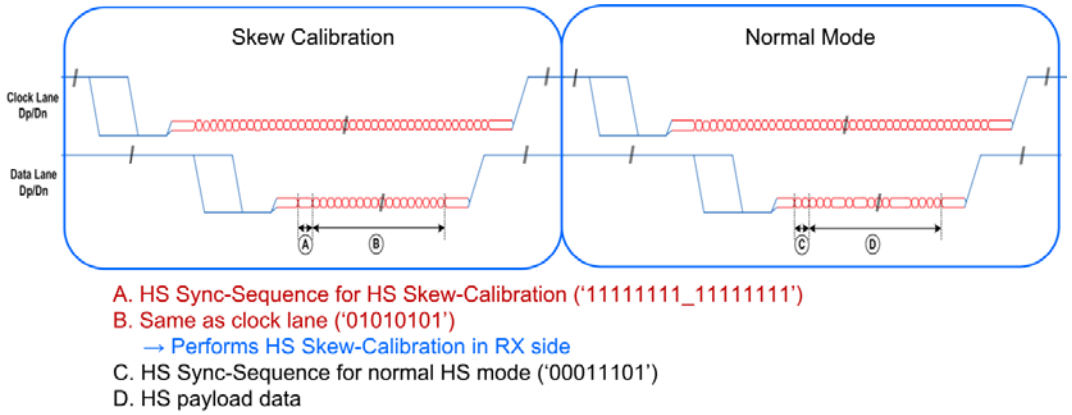


Figure 24 High-Speed Data Transmission in Skew-Calibration

The transmitter deskew burst shall use a sync pattern consisting of all one's, lasting a duration of 16 UI. After the sync pattern is sent, the payload shall be a clock pattern (01010101…) of minimum duration 2^{15} UI for initial deskew calibration, and of minimum duration 2^{10} UI for periodic calibration. See ***Figure 25*** and ***Figure 26***.

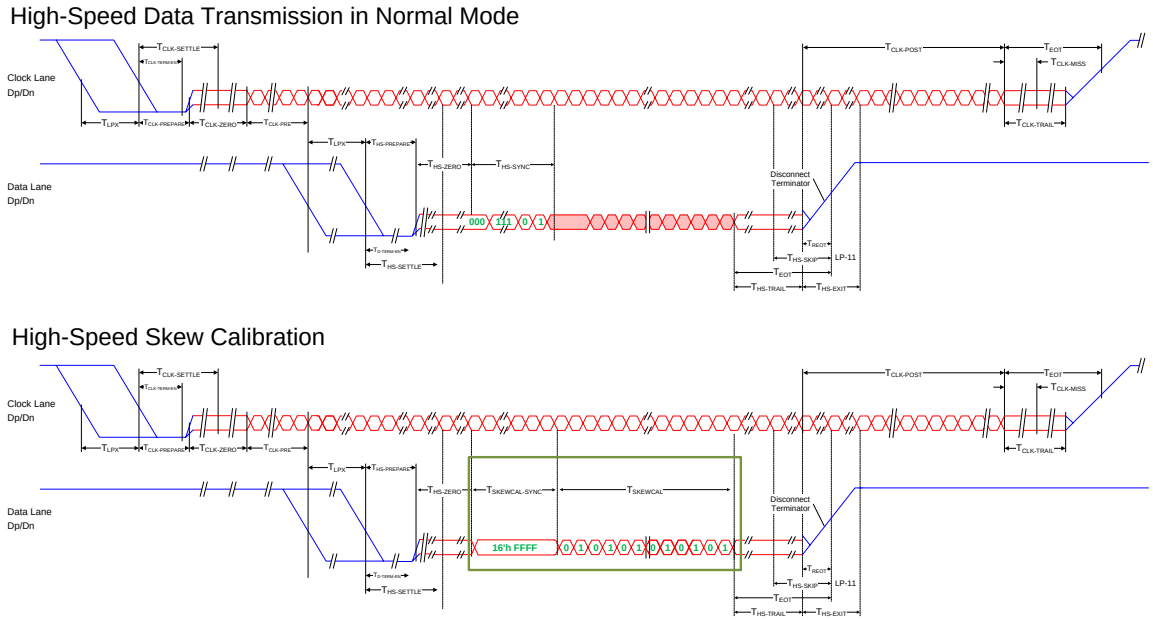
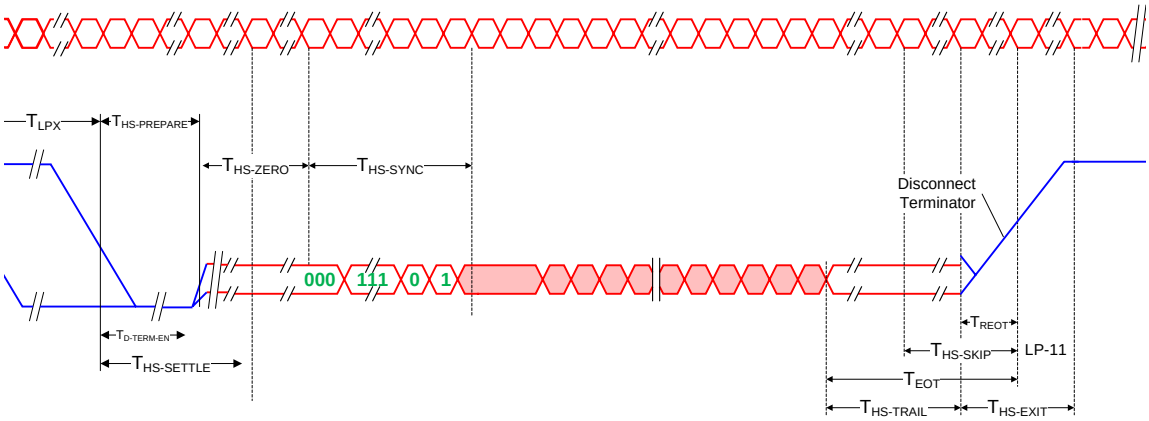


Figure 25 Normal Mode vs Skew Calibration

High-Speed Data Transmission in Normal Mode



High-Speed Skew Calibration

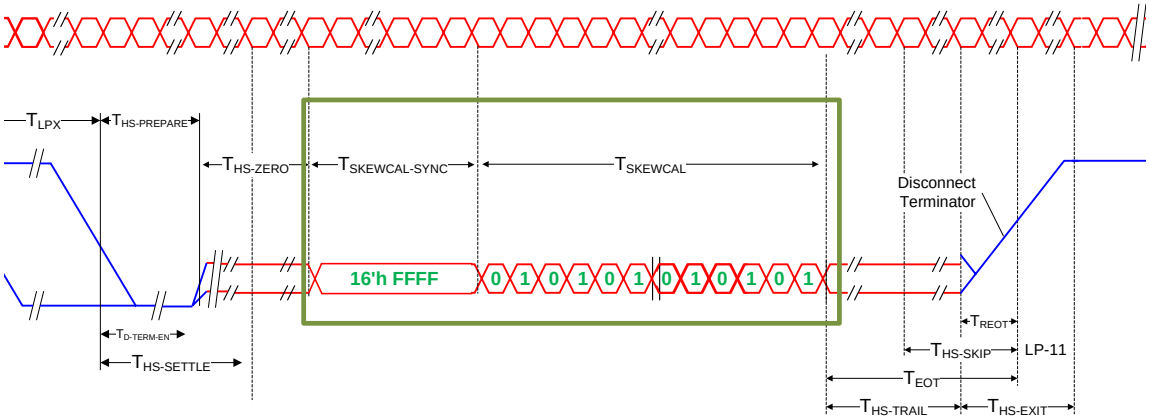


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Figure 26 Normal Mode vs Skew Calibration (Zoom-In)

The receiver shall detect the deskew sync pattern and initiate deskew calibration upon detection. The transmitter deskew sequence transmission shall be initiated under the transmitter configuration control on all active lanes simultaneously. The start-of-transmission sequence is described in ***Table 16***, and the end-of-transmission sequence is described in ***Table 17***.

Table 16 Start-of-Skew Calibration Sequence

TX Side	RX Side
Drives stop state (LP-11)	Observes stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the lines
Drives bridge state (LP-00) for time $T_{HS\text{-}PREPARE}$	Observes transition from LP-01 to LP-00 on the lines, and enables line termination after time $T_{D\text{-}TERMEN}$
Simultaneously enables high-speed driver and disables low-power drivers	
Drives HS-0 for a time $T_{HS\text{-}ZERO}$	Enables HS-RX and waits for timer $T_{HS\text{-}SETTLE}$ to expire in order to neglect transition effects
	Starts looking for leader sequence
Inserts the high-speed sync sequence for high-speed skew-calibration: ‘11111111_11111111’ beginning on a rising clock edge	
	Synchronizes upon recognition of leader sequence: ‘1111_1111’
Continues to transmit high speed data that is the same as the clock lane: ‘01010101’	
	Receives ‘01010101’ data
	Performs high-speed skew-calibration between clock and data lanes
	Finishes high-speed skew-calibration between clock and data lanes

Table 17 End-of-Skew Calibration Sequence

TX Side	RX Side
Completes transmission of ‘01010101’ data	Receives ‘01010101’ data
Toggles differential state immediately after last payload data bit and holds that state for a time $T_{HS\text{-}TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives the stop state (LP-11) for a time $T_{HS\text{-}EXIT}$	Detects the lines leaving LP-00 state and entering the stop state (LP-11), and disables termination
	Neglects bits of last period $T_{HS\text{-}SKIP}$ to hide transition effects
	Detects last transition of valid data, determines last valid data byte and skip trailer sequence
	Starts looking for leader sequence

Note:

During skew calibration time, high-speed skew calibration on the RX side has to finish. The TX side is not aware of the RX side completing calibration.

The $T_{SKEWCAL}$ maximum is 100 µsec at initial calibration and 10 µsec maximum for periodic calibration. The timing parameters are shown in ***Table 18***.

Table 18 Skew-Calibration Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{SKEWCAL\_SYNC}$	Time that the transmitter drives the skew-calibration sync pattern, $FFFF_H$		16		UI	
$T_{SKEWCAL}$	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode			100	µs	
		2^{15}			UI	
$T_{SKEWCAL}$	Time that the transmitter drives the skew-calibration pattern in the periodic skew-calibration mode			10	µs	
		2^{10}			UI	

For periodic deskew calibration, the transmitter shall finish the current burst before sending a deskew sequence.

During the Receiver deskew calibration, jittered signals are present at the input of the Receiver. The Receiver deskew block should function properly with Spread Spectrum clocking in active mode. The intent of periodic deskew is to fine tune the deskew established by the initial deskew sequence.

6.13 Alternate Calibration Sequence

The Alternate Calibration Sequence is intended to compensate for inter-symbol interference. It is used in combination with the Initial Skew Calibration. When operating above 2.5 Gbps, or changing to any data rate above 2.5 Gbps, an Alternate Calibration Sequence consisting of a leading HS0 pattern, a Calibration Sync and a Calibration Pattern shall be transmitted following any Initial Skew Calibration. This calibration is required at Link power up, and/or at Link re-initialization. For transmitters operating at or below 2.5 Gbps, the transmission of the Alternate Calibration Sequence is optional.

The Alternate Calibration Sequence can be disabled by system integrators if the receiver doesn't require or support this feature.

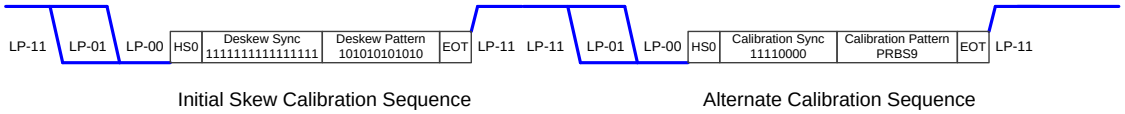

Figure 27 Initial Calibration Sequence Including Alternate Calibration Sequence

The Alternate Calibration Sequence shall use an Alternate Calibration Sync of duration T_{ALTCAL_SYNC}. After the Alternate Calibration Sync is sent, the payload shall be a PRBS9 sequence of a minimum duration of T_{ALTCAL}.

See Errata 01 Item 1

The PRBS9 sequence is defined by the polynomial $x^0 + x^5 + x^9$. The PRBS9 sequence generator shall be initialized prior to the Alternate Calibration using an initial 9-bit seed value of 000000001 (Q9:Q1). The first 8-bit word of the payload is the seed value contained in the PRBS9 sequence generator registers Q1 through Q8. The PRBS9 sequence generator is shifted 8 times before each successive 8-bit word is output on Data[7:0]. Data[7:0] is the output of the Q8 through Q1 registers, as shown in ***Figure 28***.

See Errata 01 Items 2 & 3

The same polynomial $x^0 + x^5 + x^9$ also applies for a 16-bit and 32-bit data interface. The PRBS9 sequence generator is shifted 16 or 32 times before each successive 16-bit or 32-bit word is output on Data[15:0] or Data[31:0], respectively.

See Errata 01 Item 3

The PRBS9 sequence generator as shown in ***Figure 28*** shall be supported for an 8-bit data interface example.

The order of transmission shall be LSB first. For example, the first two bytes with the initial seed is transmitted as 1000 0000 0001 0000.

See Errata 01 Item 4

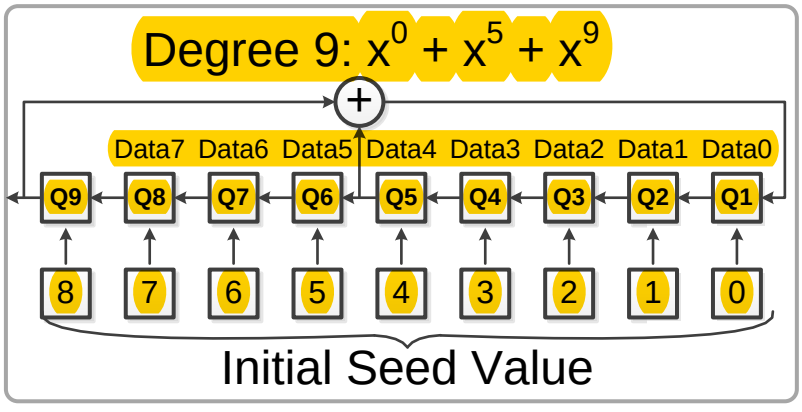

Figure 28 8-Bit PRBS9 Sequence Generator for an 8-Bit Data Interface Example

See Errata 01 Item 3

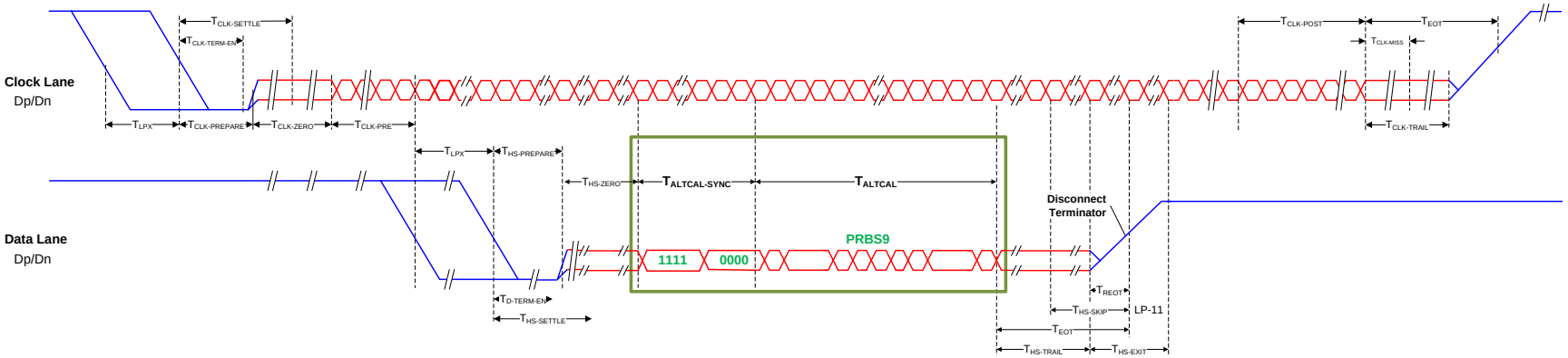

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Figure 29 Alternate Calibration Sequence Timing Diagram

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Table 19 Alternate Calibration Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ALTCAL_SYNC}	Time that the transmitter drives the Alternate Calibration Sync, 11110000	–	8	–	UI	–
T_{ALTCAL}	Time that the transmitter drives the Alternate Calibration Pattern	–	–	100	µs	–
		2^{15}	–	–	UI	–

6.14 Preamble Sequence

The Preamble Sequence is short in length and inserted at the beginning of every high speed payload with the objective of fine-tuning the clock-to-data skew due to variations in temperature and voltage. The Preamble Sequence is intended for data rates above 2.5 Gbps.

The Preamble Sequence consists of a programmable length Preamble pattern of duration $T_{PREAMBLE}$, and a fixed length Extended Sync pattern of duration $T_{EXTSYNC}$. The Extended Sync pattern is provided in order to prevent the Preamble pattern from being detected as a Leader sequence in case of certain 2-bit errors.

The Preamble Sequence shall be supported by transmitters and receivers operated above 2.5 Gbps. In this case, the Preamble Sequence shall be inserted in every HS burst when enabled.

Receivers operated above 2.5 Gbps shall detect the Extended Sync pattern and the Leader sequence.

The transmitter shall allow the Preamble pattern to be programmable within the range of $T_{PREAMBLE}$, in steps of 32 UI.

All Preamble patterns shall always be followed by the Extended Sync pattern before transmitting the Leader sequence. The Preamble pattern shall consist of a 101010 pattern of duration $T_{PREAMBLE}$, and shall default to the typical value.

The transmitter Preamble pattern length shall be configurable by system integrators, incuding the option to disable the Preamble and Extended Sync and to transmit only a HS Burst. The Extended Synch pattern shall consist of a HS-1 of duration $T_{EXTSYNC}$.

The transmitter shall transmit the Extended Sync pattern for all values of Preamble length.

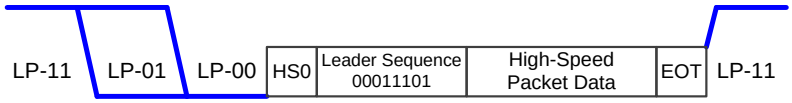


Figure 30 Normal High Speed Burst

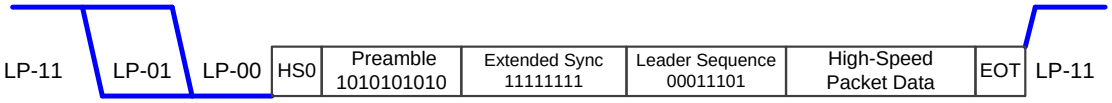


Figure 31 High Speed Burst with Preamble Sequence

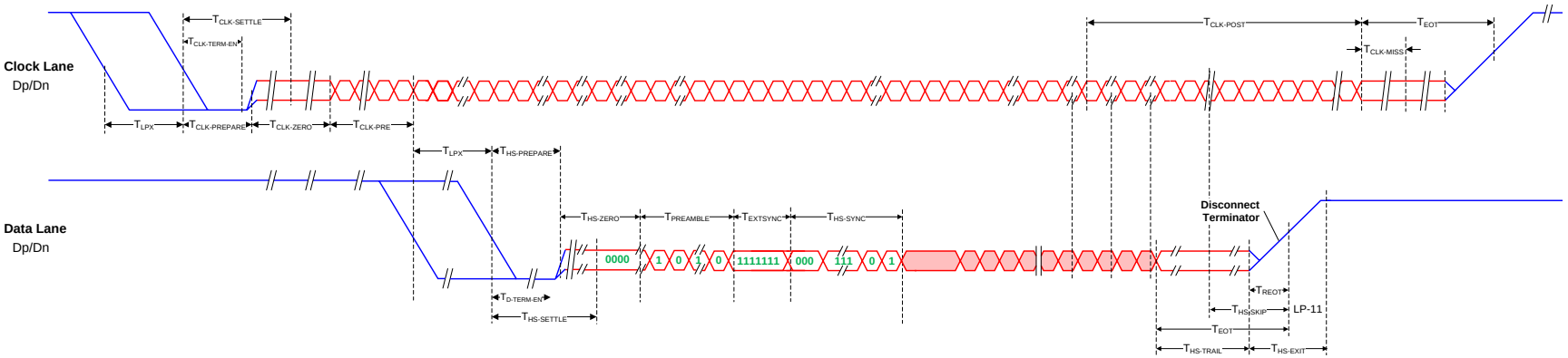


Figure 32 Preamble Timing Diagram

Table 20 Preamble Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{PREAMBLE}$	Time the Preamble pattern of 1010 is transmitted	32	32	512	UI	Programmable in steps of 32 UI
$T_{EXTSYNC}$	Time the Extended Sync pattern of HS-1 is transmitted.	–	8	–	UI	–

6.15 HS-Idle State

Support for the HS-Idle State is optional. The HS-Idle state may be used between two HS Data Bursts while remaining in HS signaling. When the HS-Idle state is used, there is no transition to LP signaling between two HS Data Bursts. The latency between two HS Data Bursts can be decreased by using the HS-Idle State, depending on the data rate and the HS-Idle timings. The HS-Idle State comprises the HS-Idle-Post, the HS-Idle-ClkHS0, and the HS-Idle-Pre sub-states, as shown in the state diagram in ***Figure 34***. A PHY can either enter HS-Idle State, or enter LP Stop State, for all its Data Lanes.

In the HS-Idle State, the Clock Lane shall stop in an HS-0 state after all Data Lanes have completed their Data Bursts and have transitioned to HS-0 states. HS-0 for the Clock Lane and for the Data Lanes in HS-Idle State shall be generated by the PHY. After the payload data is transmitted all Data Lanes shall signal an HS-0, irrespective of the polarity of the last payload bit. The RX state machine shall transition to the HS-Idle state if the Clock Lane receiver detects no clock activity for a period of $T_{CLK-MISS}$ and all Data Lanes are in HS-0. The RX state machine shall transition to the Stop state when all the Data Lanes are in LP-11.

The state transitions for the HS-Idle State are described in ***Table 22***. This table starts with the last bit of an HS Data Burst before transitioning in and out of the HS-Idle State. ***Table 22*** concludes with the first bits of an HS Data Burst after exit of the HS-Idle State.

The Clock Lane shall continue signaling for $T_{HS-IDLE-POST}$ after the HS Data Bursts are completed on all Lanes, in order to allow enough time to flush the receiver pipelines.

The HS-0 state on the Clock Lane shall be driven for a duration of $T_{HS-IDLE-CLKHS0}$.

The Clock Lane shall be active for a duration of $T_{HS-IDLE-PRE}$ before the next HS Data Burst.

The HS-Idle state shall exit to SoT. The start and end of the $T_{HS-IDLE-POST}$, $T_{HS-IDLE-CLKHS0}$, and $T_{HS-IDLE-PRE}$ timing parameters is shown in ***Figure 33***. The values of these timing parameters are defined in ***Table 21***. A transmitter shall support the default timing values at start-up. A system integrator may configure HS-Idle State parameters to different values, based on the receiver capability.

Table 21 HS-Idle State Timing Parameters

Timing	Min	Default	Max	Notes
$T_{HS-IDLE-POST}$	n*8 UI	256 UI	512 UI	1
$T_{HS-IDLE-CLKHS0}$	60 ns	60 ns	500 ns	2
$T_{HS-IDLE-PRE}$	n*8 UI	48 UI	96 UI	1

Note:

1. *Transmitter shall support programmability in n*8 UI (where n is the TX PPI bus width in bytes) steps from min to max. System integrator shall have access to program these as per application need.*
2. *For long HS-Idle state, where latency is not a limitation, legacy LP mode provides a more optimal power solution.*

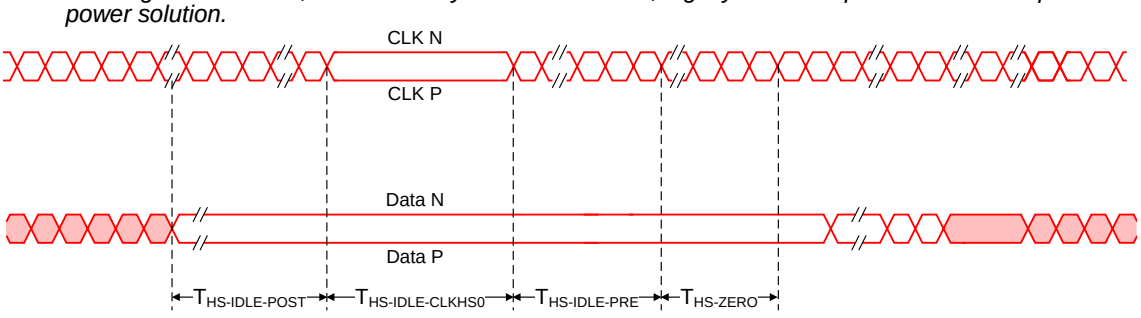


Figure 33 HS-Idle Timing Diagram Example

717

Table 22 HS-Idle State Machine Description

Data Lane State	Data Line Condition/State	Data Lane Exit State	Data Lane Exit Conditions	Clock Lane Condition	Clock Lane Exit Condition
TX-HS-0	Transmit HS-0	TX-HS-0	Send HS-0 TxHSIdleClkHS is high level	Toggling	–
TX-HS-1	Transmit HS-1	TX-HS-0	Send HS-0 TxHSIdleClkHS is high level	Toggling	–
HS-IDLE-POST	Transmit HS-0	TX-HS-0	Send TX-HS-0 for $T_{HS-IDLE-POST}$	Toggling	Send HS-0 when TxHSIdleClkHS is high level
HS-IDLE-CLKHS0	Transmit HS-0	TX-HS-0	Send TX-HS-0 for $T_{HS-IDLE-CLKHS0}$	Transmit HS-0	Start toggling when TxHSIdleClkHS is low level and TxHSIdleClkReadyHS is high level
HS-IDLE-PRE	Transmit HS-0	SOT HS-0	Send TX-HS-0 for $T_{HS-IDLE-PRE}$	Toggling	–
SOT HS-0	Transmit HS-0	TX-HS-Sync	Send TX-HS-0 for $T_{HS-ZERO}$	Toggling	–
Tx-HS-Sync	Transmit Leader sequence HS-00011101	TX-HS-0	Send HS-0 bit as first bit of payload	Toggling	–
–	–	TX-HS-1	Send HS-1 bit as first bit of payload	–	–
TX-HS-0	Transmit HS-0	TX-HS-0	Send another HS-0 bit after a HS-0 bit	Toggling	–
–	–	TX-HS-1	Send a HS-1 bit after a HS-0 bit	Toggling	–
TX-HS-1	Transmit HS-1	TX-HS-1	Send a HS-1 bit	Toggling	–
–	–	TX-HS-0	Send another HS-0 bit after a HS-1 bit	Toggling	–
RX-HS-0	Receive HS-0	RX-HS-0	Receive HS-0 in HS-Idle-Post	–	–
RX-HS-1	Receive HS-1	RX-HS-0	Receive HS-0 in HS-Idle Post	–	–
HS-IDLE-POST	Receive HS-0	RX-HS-0	End of timed interval $T_{HS-IDLE-POST}$	Toggling	Receive HS-0 (clock miss)
HS-IDLE-CLKHS0	Receive HS-0	RX-HS-0	End of timed interval $T_{HS-IDLE-CLKHS0}$	Receive HS-0	Receive toggling clock
HS-IDLE-PRE	Receive HS-0	SOT HS-0	End of timed interval $T_{HS-IDLE-PRE}$	Toggling	–
SOT HS-0	Receive HS-0	RX-HS-Sync	End of timed interval $T_{HS-ZERO}$	Toggling	–
RX-HS-Sync	Receive Leader sequence HS-00011101	RX-HS-0	Receive payload data bit	Toggling	–

Data Lane State	Data Line Condition/State	Data Lane Exit State	Data Lane Exit Conditions	Clock Lane Condition	Clock Lane Exit Condition
–	–	RX-HS-1	Receive payload data bit	–	–
RX-HS-0	Receive HS-0	RX-HS-0	Receive payload data bit	Toggling	–
–	–	RX-HS-1	Receive payload data bit	Toggling	–
RX-HS-1	Receive HS-1	RX-HS-1	Receive payload data bit	Toggling	–
–	–	RX-HS-0	Receive payload data bit	Toggling	–

6.16 Sync Patterns

718 ***Table 23*** lists all of the Sync Patterns, and the targeted usage for each one.

Table 23 Sync Pattern Definition

Sync Patterns	Usage	Note
00011101	High Speed Data	–
10010010	Followed by Control Code (16bit) + High Speed Data	1
1111111111111111	Skew Calibration	–
11110000	Alternate Calibration	–
1111111100011101	High Speed Data when preamble is enabled	–

719 ***Note:***

1. *Reserved for future use*

6.17 Global Operation Flow Diagram

All previously described aspects of operation, either including or excluding optional parts, are contained in Lane Modules. ***Figure 34*** shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

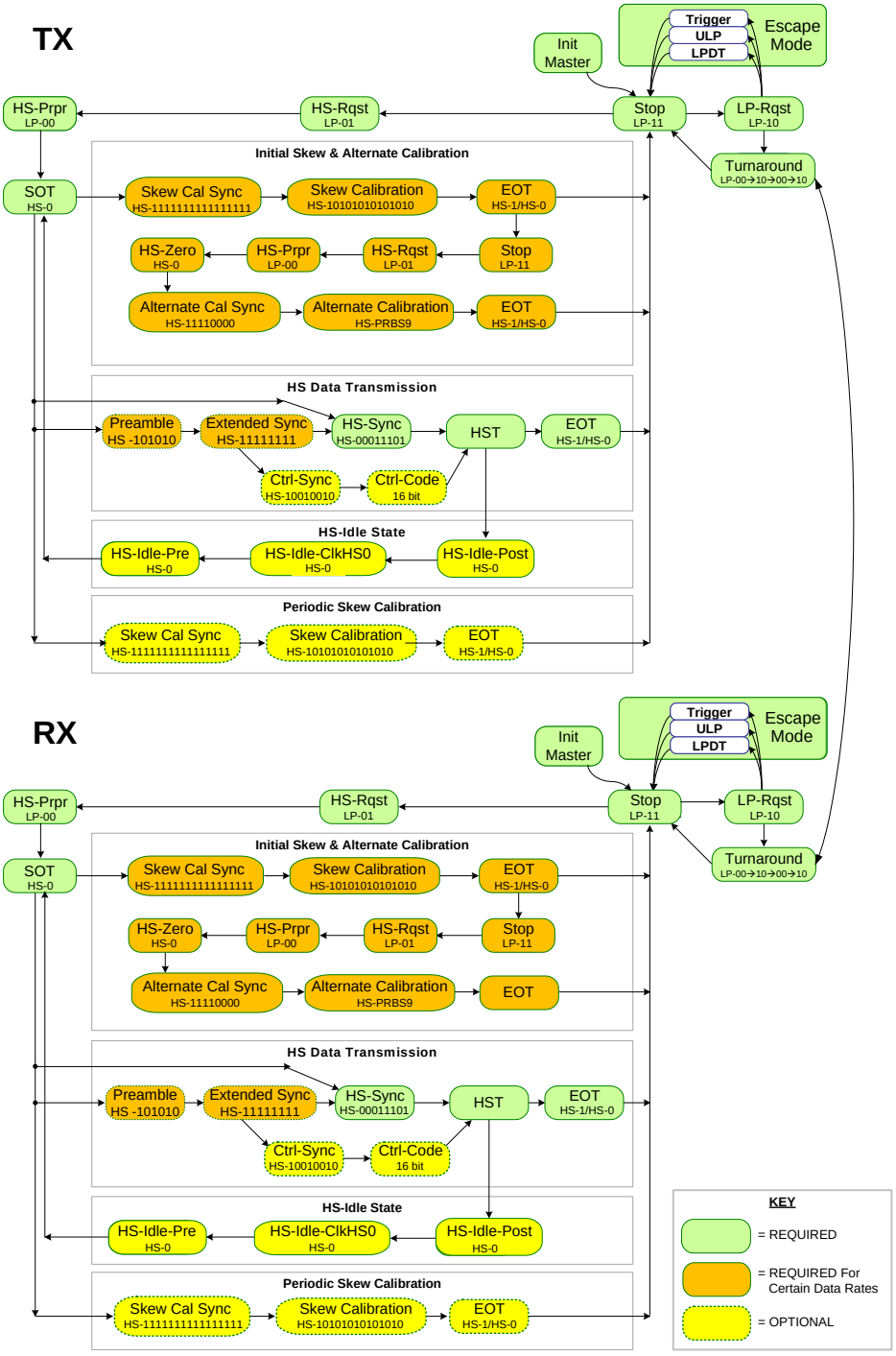


Figure 34 Data Lane Module State Diagram

Figure 35 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High-Speed clock transmission. The figure also shows the transition states as described previously.

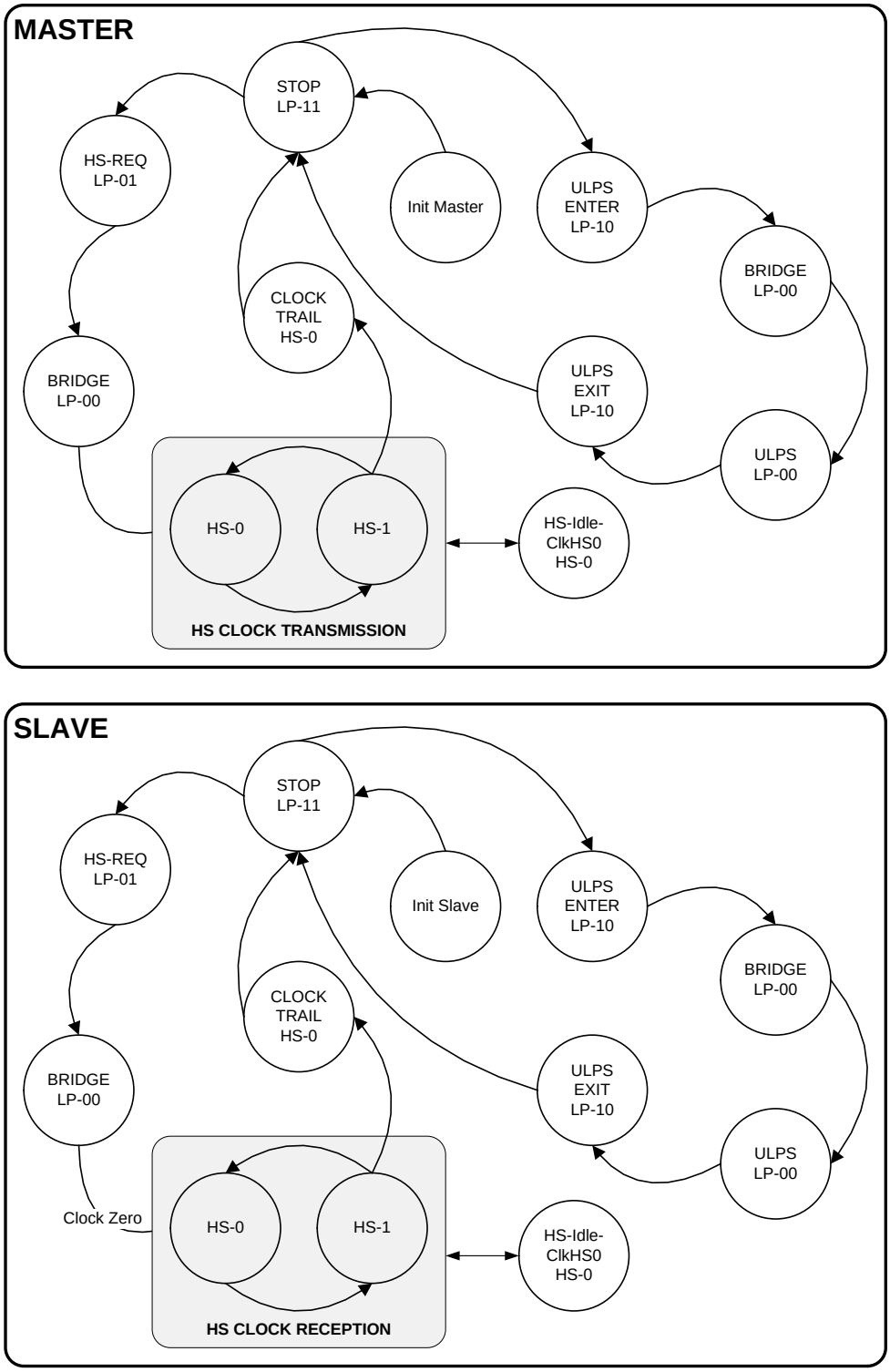


Figure 35 Clock Lane Module State Diagram

6.18 Data Rate Dependent Parameters (informative)

The high speed data transfer rate of the D-PHY may be programmable to values determined by a particular implementation. Any individual data transfer between SoT and EoT sequences must take place at a given, fixed rate. However, reprogramming the data rate of the D-PHY high speed transfer is allowed at initialization, before starting the exit from ULP state or in Stop state whenever the HS clock is not running. The method of data rate reprogramming is out of the scope of this document.

Many time parameter values in this document are specified as the sum of a fixed time and a particular number of High-Speed UIs. The parameters may need to be recomputed if the data rate, and therefore the UI value, is changed. These parameters, with their allowed values, are listed in ***Table 14***. For clarity, the parameter names and purposes are repeated here.

6.18.1 Parameters Containing Only UI Values

$T_{CLK\text{-}PRE}$ is the minimum number of High-Speed clock cycles the Master must send over the Clock Lane after it is restarted in HS mode and before any data transmission may begin. If a particular protocol at the Slave side requires more clock cycles then $T_{CLK\text{-}PRE}$, the Master side protocol should ensure that these are transmitted.

6.18.2 Parameters Containing Time and UI values

Several parameters are specified as the sum of an explicit time and a number of UI. The explicit time values, in general, are derived from the time needed to charge and discharge the interconnect to its specified values given the specified drive voltages and line termination values. As such, the explicit time values are not data rate dependent. It is conceivable to use the sum of an analog timer and a HS clock counter to ensure the implementation satisfies these parameters. If these explicit time values are implemented by counting HS clock cycles only, the count value is a function of the data rate and, therefore, must be changed when the data rate is changed.

$T_{D\text{-}TERM\text{-}EN}$ is the time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL,MAX}$.

$T_{HS\text{-}PREPARE}$, is the time to drive LP-00 before starting the HS transmission on a Data Lane.

$T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO,MIN}$ is the sum of the time to drive LP-00 in preparation for the start of HS transmission plus the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.

$T_{HS\text{-}TRAIL}$ is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.

$T_{HS\text{-}SKIP}$ is the time the receiver must “back up” and skip data to ignore the transition period of the EoT sequence.

$T_{CLK\text{-}POST,MIN}$ is the minimum time that the transmitter continues sending HS clocks after the last Data Lane has transitioned to LP mode following a HS transmission burst. If a particular receiver implementation requires more clock cycles than $T_{CLK\text{-}POST,MIN}$ to finish reception, the transmitter must supply sufficient clocks to accomplish the reception.

6.18.3 Parameters Containing Only Time Values

Several parameters are specified only as explicit time values. As in ***Section 6.18.2***, these explicit time values are typically derived from the time needed to charge and discharge the interconnect and are, therefore, not data rate dependent. It is conceivable to use an analog timer or a HS clock counter to ensure the implementation satisfies these parameters. However, if these time values are implemented by counting HS clock cycles only, the count value is a function of the data rate and, therefore, must be changed when the data rate is changed.

The following parameters are based on time values alone:

- $T_{HS-SKIP,MIN}$
- $T_{CLK-MISS,MAX}$
- $T_{CLK-TRAIL,MIN}$
- $T_{CLK-TERM-EN}$
- $T_{CLK-PREPARE}$

6.18.4 Parameters Containing Only Time Values That Are Not Data Rate Dependent

The remaining parameters in ***Table 14*** shall be complied with even when the High-Speed clock is off. These parameters include Low-Power and initialization state durations and LP signaling intervals. Though these parameters are not HS data rate dependent, some implementations of D-PHY may need to adjust these values when the data rate is changed.

6.19 Interoperability

Table 24 summarizes integration and downward compatibility for all possible combinations of the Tx's D-PHY Specification version and the Rx's D-PHY Specification version. The table shows the maximum operating speed for each possible combination, and indicates the four combinations that require deskew initialization. For example, a D-PHY v2.0 Tx and a D-PHY v1.2 Rx are compatible for speeds up to 1.5 Gbps without deskew initialization, and at speeds up to 2.5 Gbps if deskew initialization is used.

Table 24 D-PHY Version Integration and Downward Compatibility

		Rx D-PHY Specification Version									
		D-PHY v2.1		D-PHY v2.0		D-PHY v1.2		D-PHY v1.1		D-PHY v1.0	
		Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization
Tx D-PHY Specification Version	D-PHY v1.0	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–
	D-PHY v1.1	1.5	–	1.5	–	1.5	–	1.5	–	1.0	–
	D-PHY v1.2	2.5	Yes	2.5	Yes	2.5	Yes	1.5	–	1.0	–
		1.5	–	1.5	–	1.5	–				
	D-PHY v2.0	4.5	Yes	4.5	Yes	2.5	Yes	1.5	–	1.0	–
		1.5	–	1.5	–	1.5	–				
	D-PHY v2.1	4.5	Yes	4.5	Yes	2.5	Yes	1.5	–	1.0	–
		1.5	–	1.5	–	1.5	–				

Note:

Cells containing dashes ('–') indicate that Deskew Initialization is not required

7 Fault Detection

There are three different mechanisms to detect malfunctioning of the Link. Bus contention and error detection functions are contained within the D-PHY. These functions should detect many typical faults. However, some faults cannot be detected within the D-PHY and require a protocol-level solution. Therefore, the third detection mechanism is a set of application specific watchdog timers.

7.1 Contention Detection

If a bi-directional Lane Module and a Unidirectional Module are combined in one Lane, only unidirectional functionality is available. Because in this case the additional functionality of one bi-directional PHY Module cannot be reliably controlled from the limited functionality PHY side, the bi-directional features of the bi-directional Module shall be safely disabled. Otherwise in some cases deadlock may occur which can only be resolved with a system power-down and re-initialization procedure.

During normal operation one and only one side of a Link shall drive a Lane at any given time except for certain transition periods. Due to errors or system malfunction a Lane may end up in an undesirable state, where the Lane is driven from two sides or not driven at all. This condition eventually results in a state conflict and is called Contention.

All Lane Modules with LP bi-directionality shall include contention detection functions to detect the following contention conditions:

- Modules on both sides of the same line drive opposite LP levels against each other. In this case, the line voltage will settle to some value between $V_{OL,MIN}$ and $V_{OH,MAX}$. Because V_{IL} is greater than V_{IHCD}, the settled value will always be either higher than V_{IHCD}, lower than V_{IL}, or both. Refer to ***Section 8***. This ensures that at least one side of the link, possibly both, will detect the fault condition.
- The Module at one side drives LP-high while the other side drives HS-low on the same Line. In this case, the line voltage will settle to a value lower than V_{IL}. The contention shall be detected at the side that is transmitting the LP-high.

The first condition can be detected by the combination of LP-CD and LP-RX functions. The LP-RX function should be able to detect the second contention condition. Details on the LP-CD and LP-RX electrical specifications can be found in ***Section 9***. Except when the previous state was TX-ULPS, contention shall be checked before the transition to a new state. Contention detection in ULPS is not required because the bit period is not defined and a clock might not be available.

After contention has been detected, the Protocol shall take proper measures to resolve the situation.

7.2 Sequence Error Detection

If for any reason the Lane signal is corrupted the receiving PHY may detect signal sequence errors. Errors detected inside the PHY may be communicated to the Protocol via the PPI. This kind of error detection is optional, but strongly recommended as it enhances reliability. The following sequence errors can be distinguished:

- SoT Error
- SoT Sync Error
- EoT Sync Error
- Escape Entry Command Error
- LP Transmission Sync Error
- False Control Error

7.2.1 SoT Error

When deskew is not supported, the Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error and some multi-bit errors. Therefore the synchronization may be usable, but confidence in the payload data is lower. If this situation occurs, then an SoT Error is indicated.

When deskew is supported, bit errors are not tolerated in the Leader sequence. If there is an error in the Leader sequence, then the payload data is not reliable.

7.2.2 SoT Sync Error

If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected, a SoT Sync Error is indicated.

7.2.3 EoT Sync Error

The EoT Sync Error is indicated when the last bit of a transmission does not match a byte boundary. This error can only be indicated in case of EoT processing on detection of LP-11.

7.2.4 Escape Mode Entry Command Error

If the receiving Lane Module does not recognize the received Entry Command for Escape mode an Escape mode Entry Command Error is indicated.

7.2.5 LP Transmission Sync Error

At the end of a Low-Power Data transmission procedure, if data is not synchronized to a Byte boundary an Escape Sync Error signal is indicated.

7.2.6 False Control Error

If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape or Turnaround sequence, a False Control Error is indicated. This error is also indicated if a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).

7.3 Protocol Watchdog Timers (informative)

It is not possible for the PHY to detect all fault cases. Therefore, additional protocol-level time-out mechanisms are necessary in order to limit the maximum duration of certain modes and states.

7.3.1 HS RX Timeout

In HS RX mode if no EoT is received within a certain period the protocol should time-out. The timeout period can be protocol specific.

7.3.2 HS TX Timeout

The maximum transmission length in HS TX is bounded. The timeout period is protocol specific.

7.3.3 Escape Mode Timeout

A device may timeout during Escape mode. The timeout should be greater than the Escape mode Silence Limit of the other device. The timeout period is protocol specific.

7.3.4 Escape Mode Silence Timeout

A device may have a bounded length for LP TX-00 during Escape mode, after which the other device may timeout. The timeout period is protocol specific. For example, a display module should have an Escape mode Silence Limit, after which the host processor can timeout.

7.3.5 Turnaround Errors

A Turnaround procedure always starts from a Stop State. The procedure begins with a sequence of Low-Power States ending with a Bridge State (LP-00) during which drive sides are swapped. The procedure is finalized by the response including a Turn State followed by a Stop State driven from the other side. If the actual sequence of events violates the normal Turnaround procedure a "False Control Error" may be flagged to the Protocol. See ***Section 7.2.6***. The Turn State response serves as an acknowledgement for the correctly completed Turnaround procedure. If no acknowledgement is observed within a certain time period the Protocol should time-out and take appropriate action. This period should be larger than the maximum possible Turnaround time for a particular system. There is no time-out for this condition in the PHY.

8 Interconnect and Lane Configuration

The interconnect between transmitter and receiver carries all signals used in D-PHY communication. This includes both high speed, low voltage signaling I/O technology and low speed, low power signaling for control functions. For this reason, the physical connection shall be implemented by means of balanced, differential, point-to-point transmission lines referenced to ground. The total interconnect may consist of several cascaded transmission line segments, such as, printed circuit boards, flex-foils, and cable connections.

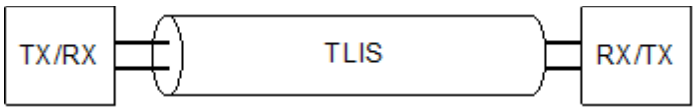


Figure 36 Point-to-point Interconnect

8.1 Lane Configuration

The complete physical connection of a Lane consists of a transmitter (TX), and/or receiver (RX) at each side, with some Transmission-Line-Interconnect-Structure (TLIS) in between. The overall Lane performance is therefore determined by the combination of these three elements. The split between these elements is defined to be on the module (IC) pins. This section defines both the required performance of the Transmission-Line-Interconnect-Structure for the signal routing as well as the I/O-cell Reflection properties of TX and RX. This way the correct overall operation of the Lane can be ensured.

With respect to physical dimensions, the Transmission-Line-Interconnect-Structure will typically be the largest part. Besides printed circuit board and flex-foil traces, this may also include elements such as vias and connectors.

8.2 Boundary Conditions

The reference characteristic impedance level is 100 Ohm differential, 50 Ohm single-ended per Line, and 25 Ohm common-mode for both Lines together. The 50 Ohm impedance level for single-ended operation is also convenient for test and characterization purposes.

This typical impedance level is required for all three parts of the Lane: TX, TLIS, and RX. The tolerances for characteristic impedances of the interconnect and the tolerance on line termination impedances for TX and RX are specified by means of S-parameter templates over the whole operating frequency range.

The differential channel is also used for LP single-ended signaling. Therefore, it is strongly recommended to apply only very loosely coupled differential transmission lines.

The flight time for signals across the interconnect shall not exceed two nanoseconds.

8.3 Definitions

The frequency ‘fh’ is the fundamental frequency of the operating data rate, e.g. for an operating data rate of 1Gb/s ‘fh’ is 500MHz.

The frequency ‘fh_{MAX}’ is a device specification and indicates the maximum supported fh for a particular device.

The frequency ‘$f_{LP,MAX}$’ is the maximum toggle frequency for Low-Power mode.

RF interference frequencies are denoted by ‘f_{INT}’, where $f_{INT,MIN}$ defines the lower bound for the band of relevant RF interferers.

The frequency f_{MAX} for devices supporting data rates up to 1.5 Gbps is defined by the maximum of ($1/5t_{F,MIN}$, $1/5t_{R,MIN}$), where t_R and t_F are the rise and fall times of the High-Speed signaling.

For devices supporting data rates of more than 1.5 Gbps, f_{MAX} is ¾ * data rate.

The frequency ‘fh_{MIN}’ is defined as fh_{MIN} = fh/10.

8.4 S-parameter Specifications

The required performance of the physical connection is specified by means of S-parameter requirements for TX, TLIS, and RX, for TLIS by mixed-mode, 4-port parameters, and for RX and TX by mixed-mode, reflection (return loss) parameters. The S-parameter limits are defined over the whole operating frequency range by means of templates.

The differential transmission properties are most relevant and therefore this specification uses mixed-mode parameters. As the performance needs depend on the targeted bit rates, most S-parameter requirements are specified on a normalized frequency axis with respect to bit rate. Only the parameters that are important for the suppression of external (RF) interference are specified on an absolute frequency scale. This scale extends up to f_{MAX}. Beyond this frequency the circuitry itself shall suppress the high-frequency interference signals sufficiently.

Only the overall performance of the TLIS and the maximum reflection of RX and TX are specified. This fully specifies the signal behavior at the RX/TX-module pins. The subdivision of losses, reflections and mode-conversion budget to individual physical fractions of the TLIS is left to the system designer. Annex B includes some rules of thumb for system design and signal routing guidelines.

8.5 Characterization Conditions

All S-parameter definitions are based on a 50 Ω impedance reference level. The characterization can be done with a measurement system, as shown in ***Figure 37***.

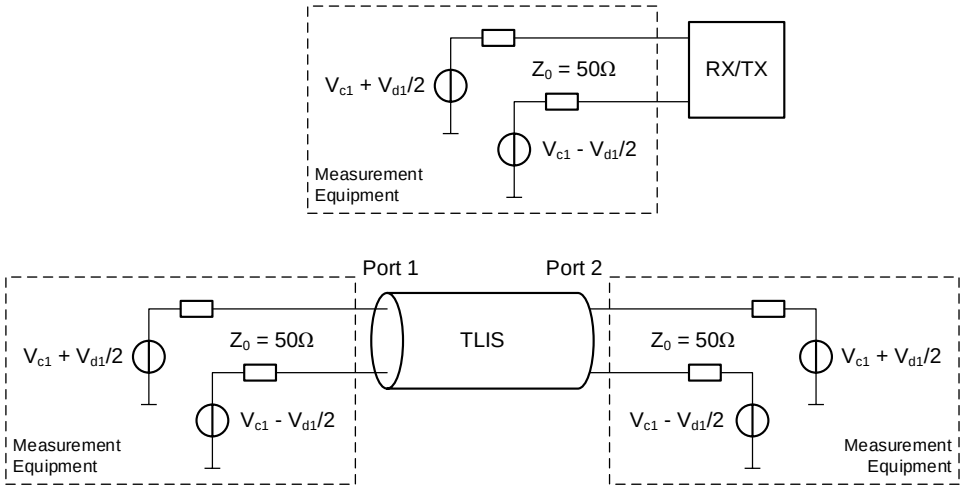


Figure 37 Set-up for S-parameter Characterization of RX, TX and TLIS

The syntax of S-parameters is S[measured-mode][driven-mode][measured-port][driven-port]. Examples: Sdd21of TLIS is the differential signal at port 2 due to a differential signal driven at port 1; Sdc22 is the measured differential reflected signal at port 2 due to a common signal driven at port 2.

8.6 Interconnect Specifications

The Transmission-Line Signal-Routing (TLSR) is specified by means of mixed-mode 4-port S-parameter behavior templates over the frequency range. This includes the differential and common-mode, insertion and return losses, and mode-conversion limitations.

8.6.1 Differential Characteristics

8.6.1.1 Differential Insertion Loss for Data Rate ≥ 80 Mbps and ≤ 1.5 Gbps

The differential transfer behavior (insertion loss) of the TLIS when supporting data rates ≥ 80 Mbps and ≤ 1.5 Gbps shall meet the Sdd21 template shown in ***Figure 38***, where i ≠ j.

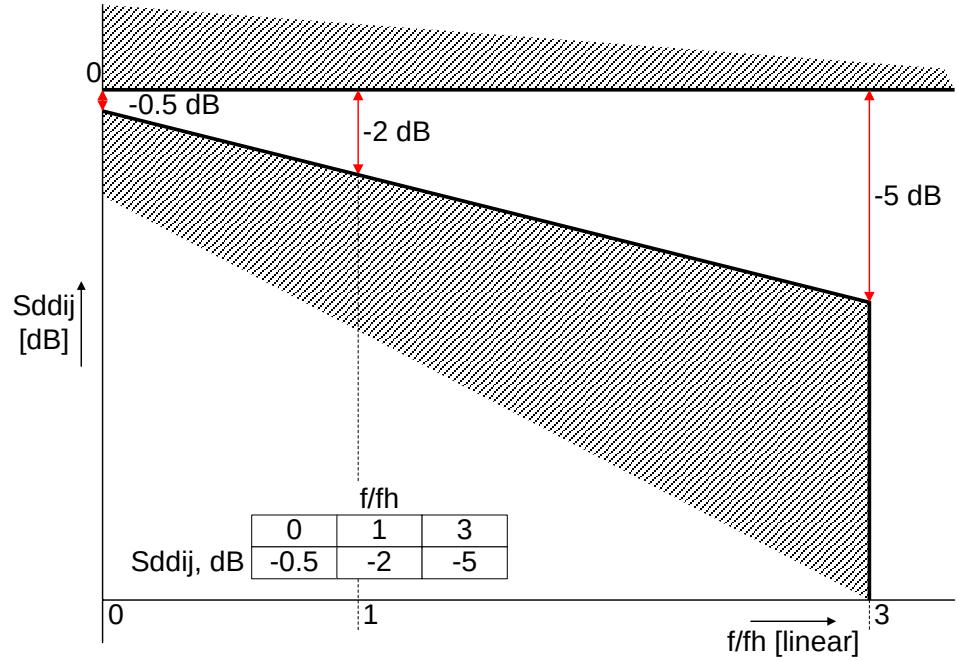
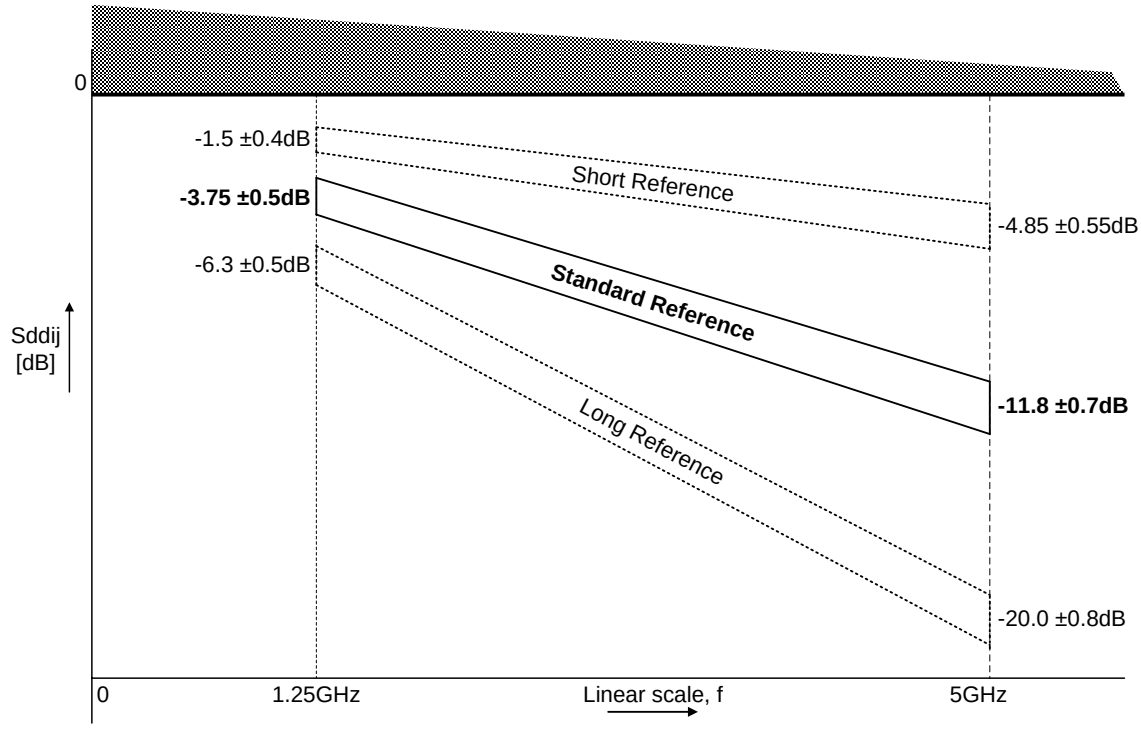


Figure 38 Template for Differential Insertion Losses, Data Rates ≥ 80 Mbps and ≤ 1.5 Gbps

8.6.1.2 Differential Insertion Loss for Data Rate > 1.5 Gbps and ≤ 4.5 Gbps

The differential transfer behavior (insertion loss) of the TLIS when supporting data rates > 1.5 Gbps and ≤ 4.5 Gbps shall meet the Sdd21 template shown in ***Figure 39***, where i ≠ j.



Frequency	1.25GHz	5.0GHz
Short Reference Sddij, dB	-1.5dB ±0.4dB	-4.85dB ±0.55dB
Standard Reference Sddij, dB	**-3.75dB ±0.5dB**	**-11.8dB ±0.7dB**
Long Reference Sddij, dB	-6.3dB ±0.5dB	-20.0dB ±0.8dB

Figure 39 Template for Differential Insertion Losses, Data Rates > 1.5 Gbps and ≤ 4.5 Gbps

Three Reference channels (Short, Standard & Long) are defined to support a wide range of display and camera applications.

Standard Reference channel is a default requirement and the transmitters/receivers shall support it.

Short Reference channel support is optional. In applications targeting lower interconnect loss, and when the Transmitter or the Receiver support the optional power saving modes, this channel can be referenced for better system power optimization.

Long Reference Channel support is optional. This is aimed at supporting higher loss interconnect like Chip-On-Glass (COG). In order to support such an interconnect, the data rate may need to be limited. COG interconnect is used for display panels and has reduced cost compared to other solutions. However, it increases the total loss of interconnect due to additional routing on the glass, bonding between the glass and PCB, and bonding between the glass and silicon. The maximum data rate recommended with the long channel is 2.5 Gbps.

Specific guidance on using these reference channels is provided in ***Section 10.4***.

8.6.1.3 Differential Reflection Loss for Data Rate ≥ 80 Mbps and ≤ 1.5 Gbps

When supported data rates are ≥ 80 Mbps and ≤ 1.5 Gbps, the differential reflection for both ports of the TLIS is specified by Sdd11 and Sdd22, and should match the template shown in ***Figure 40***. Not meeting the differential reflection coefficient might impact interoperability and operation.

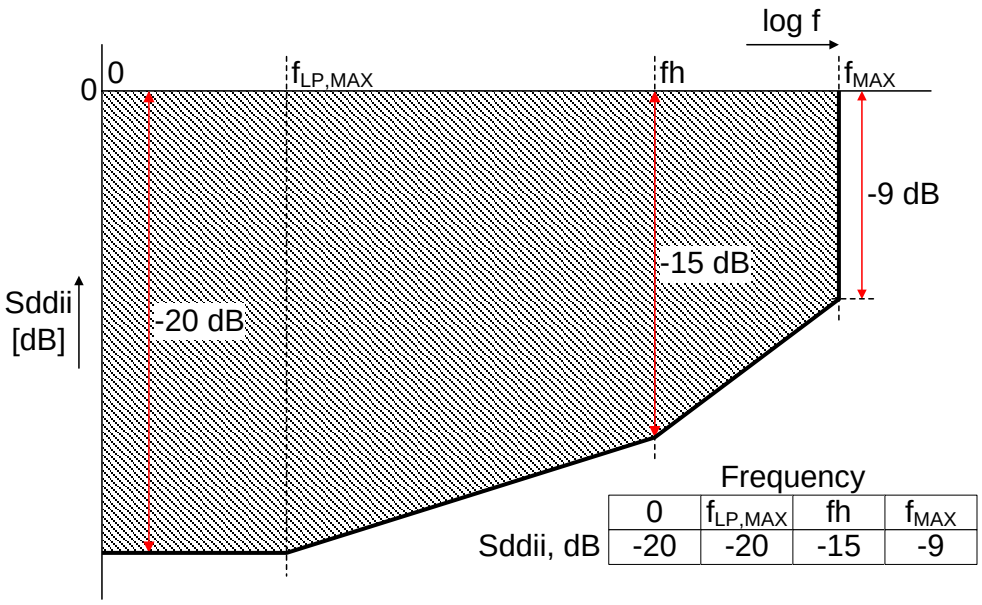


Figure 40 Template for Differential Reflection at Both Ports

8.6.1.4 Differential Reflection Loss for Data Rate >1.5 Gbps and ≤ 4.5 Gbps

When supported data rates are > 1.5 Gbps and ≤ 4.5 Gbps, the differential reflection for both ports of the TLIS is specified by Sdd11 and Sdd22, and should be better than -12 dB in the range from 0 to fmax. Not meeting the differential reflection coefficient might impact interoperability and operation.

8.6.2 Common-mode Characteristics

The common-mode insertion loss is implicitly specified by means of the differential insertion loss and the Intra-Lane cross coupling. The requirements for common-mode insertion loss are therefore equal to the differential requirements.

8.6.3 Intra-Lane Cross-Coupling

The two lines applied as a differential pair during HS transmission are also used individually for single-ended signaling during Low-Power mode. Therefore, the coupling between the two wires shall be restricted in order to limit single-ended cross coupling. The coupling between the two wires is defined as the difference of the S-parameters Scc21 and Sdd21 or Scc12 and Sdd12. In either case, the difference shall not exceed –20 dB for frequencies up to $10*f_{LP,MAX}$.

8.6.4 Mode-Conversion Limits

All mixed-mode, 4-port S-parameters for differential to common-mode conversion, and vice-versa, shall not exceed –26 dB for frequencies below f_{MAX}. This includes Sdc12, Scd21, Scd12, Sdc21, Scd11, Sdc11, Scd22, and Sdc22.

8.6.5 Inter-Lane Cross-Coupling

The common-mode and differential inter-Lane cross coupling between Lanes (clock and data) shall meet the requirements as shown in ***Figure 41*** and ***Figure 42***, respectively.

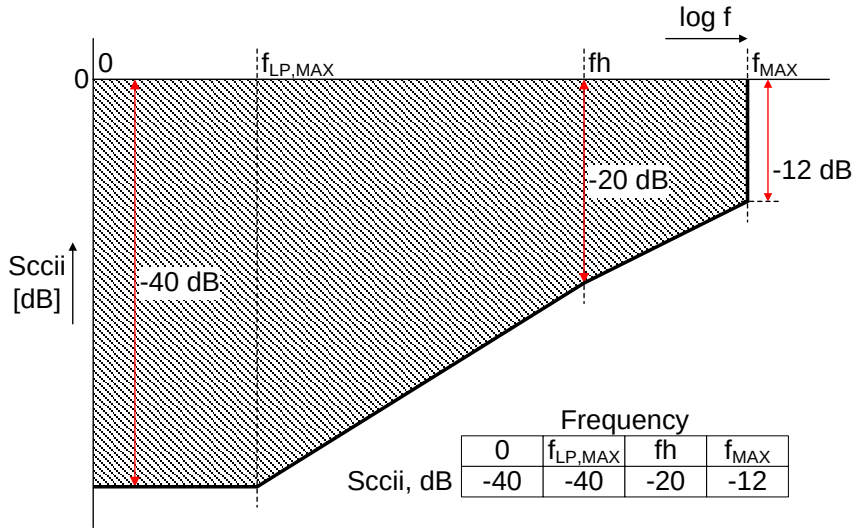


Figure 41 Inter-Lane Common-mode Cross-Coupling Template

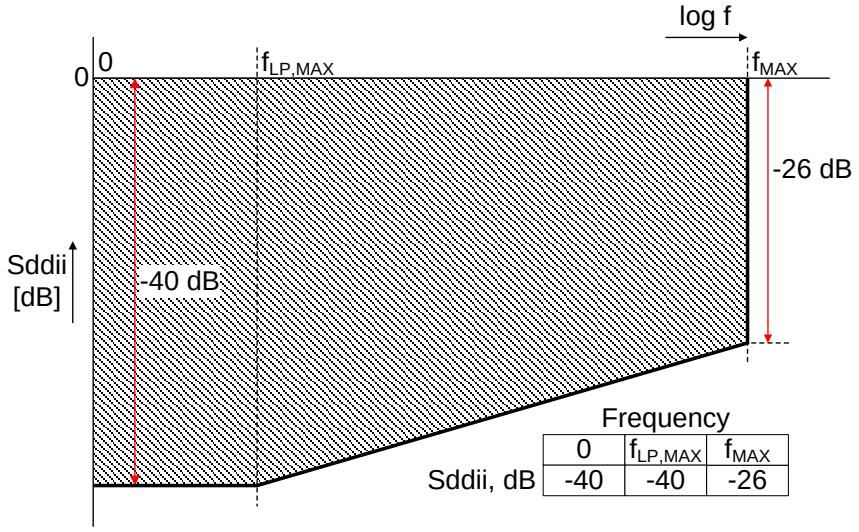


Figure 42 Inter-Lane Differential Cross-Coupling Template

8.6.6 Inter-Lane Static Skew

The difference in signal delay between any Data Lane and the Clock Lane shall be less than UI/50 for all frequencies up to, and including, fh when the supported data rate is less than or equal to 1.5 Gbps. For data rates higher than 1.5 Gbps, refer to ***Table 38***.

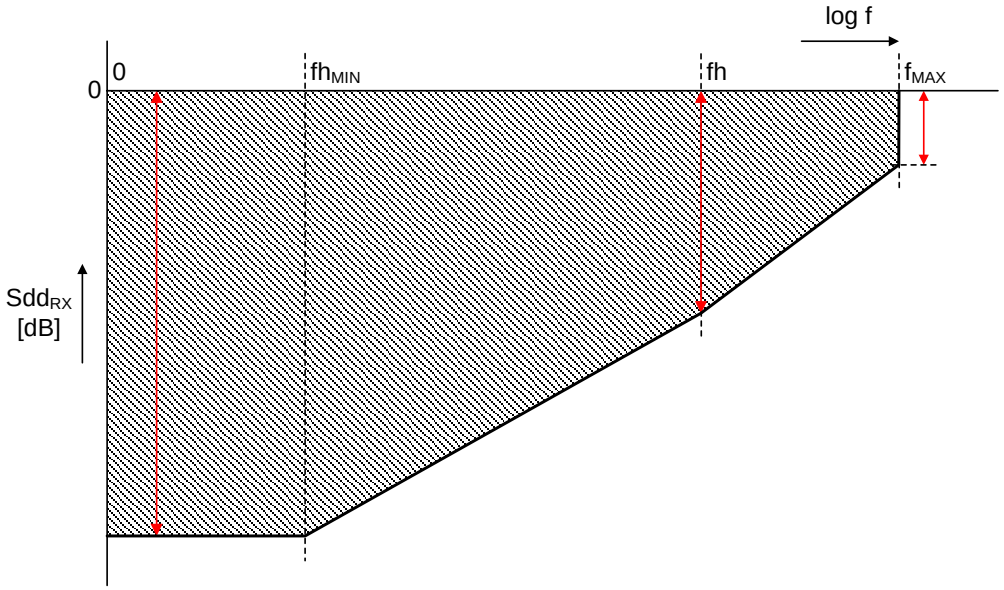
$$\frac{\left|Sdd12_{DATA}(\varphi) - Sdd12_{CLOCK}(\varphi)\right|}{\omega} < \frac{UI}{50}$$ Driver and Receiver Characteristics

8.7 Driver and Receiver Characteristics

Besides the TLIS the Lane consists of two RX-TX modules, one at each side. This paragraph specifies the reflection behavior (return loss) of these RX-TX modules in HS-mode. The signaling characteristics of all possible functional blocks inside the RX-TX modules can be found in ***Section 9***.

8.7.1 Differential Characteristics

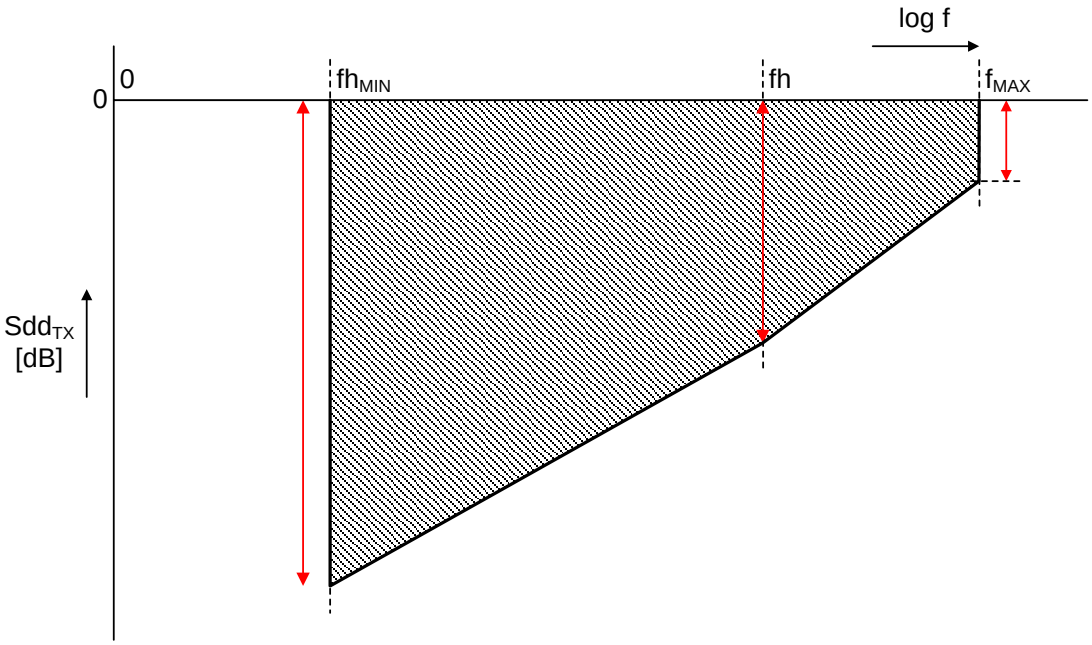
The differential reflection of a Lane Module in High-Speed RX mode is specified by the template shown in ***Figure 43***.



Frequency	0	fh_{MIN}	fh	f_{MAX}	PHY Data Rate Supported
Sdd_{RX}, dB	-15	-15	-8.5	-2.9	≥ 80 Mbps & ≤ 1.5 Gbps
Sdd_{RX}, dB	-15	-15	-4.5	-2.5	> 1.5 Gbps & ≤ 2.5 Gbps
Sdd_{RX}, dB	-15	-15	-2	-1	> 2.5 Gbps & ≤ 4.5 Gbps

Figure 43 Differential Reflection Template for Lane Module Receivers

The differential reflection of a Lane Module in High-Speed TX mode is specified by the template shown in ***Figure 44***.



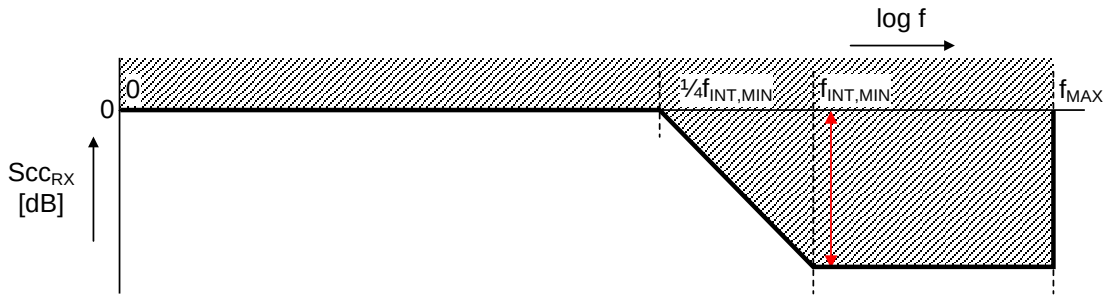
Frequency	fh$_{MIN}$	fh	f$_{MAX}$	PHY Data Rate Supported
Sdd$_{TX}$, dB	-15	-8.5	-2.9	≥ 80 Mbps & ≤ 1.5 Gbps
Sdd$_{TX}$, dB	-15	-4.5	-2.5	> 1.5 Gbps & ≤ 2.5 Gbps
Sdd$_{TX}$, dB	-15	-2	-1	> 2.5 Gbps & ≤ 4.5 Gbps

Figure 44 Differential Reflection Template for Lane Module Transmitters

8.7.2 Common-Mode Characteristics

The common-mode return loss specification is different for a High-Speed TX and RX mode, because the RX is not DC terminated to ground. The common-mode reflection of a Lane Module in High-Speed TX mode shall be less than -6 dB from $f_{LP,MAX}$ up to f_{MAX} for devices supporting data rates up to 1.5 Gbps, 2.5 dB for devices supporting data rates up to 2.5 Gbps, and -1 dB for devices supporting data rates up to 4.5 Gbps.

The common-mode reflection of a Lane Module in High-Speed RX mode shall conform to the limits specified by the template shown in ***Figure 45***. Assuming a high DC common-mode impedance, this implies a sufficiently large capacitor at the termination center tap. The minimum value allows integration. While the common-mode termination is especially important for reduced influence of RF interferers, the RX requirement limits reflection for the most relevant frequency band.



Frequency	0	¼$f_{INT,MIN}$	$f_{INT,MIN}$	f_{MAX}	PHY Data Rate Supported
Scc_{RX}, dB	0	0	-6	-6	≥ 80 Mbps & ≤ 1.5 Gbps
Scc_{RX}, dB	0	0	-2.5	-2.5	> 1.5 Gbps & ≤ 2.5 Gbps
Scc_{RX}, dB	0	0	-1	-1	> 2.5 Gbps & ≤ 4.5 Gbps

Figure 45 Template for RX Common-Mode Return Loss

8.7.3 Mode-Conversion Limits

The differential to common-mode conversion limits of RX shall be -26 dB up to f_{MAX}.

9 Electrical Characteristics

A PHY may contain the following electrical functions: a High-Speed Transmitter (HS-TX), a High-Speed Receiver (HS-RX), a Low-Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and a Low-Power Contention Detector (LP-CD). A PHY does not need to contain all electrical functions, only the functions that are required for a particular PHY configuration. The required functions for each configuration are specified in ***Section 5***. All electrical functions included in any PHY shall meet the specifications in this section. ***Figure 46*** shows the complete set of electrical functions required for a fully featured PHY transceiver.

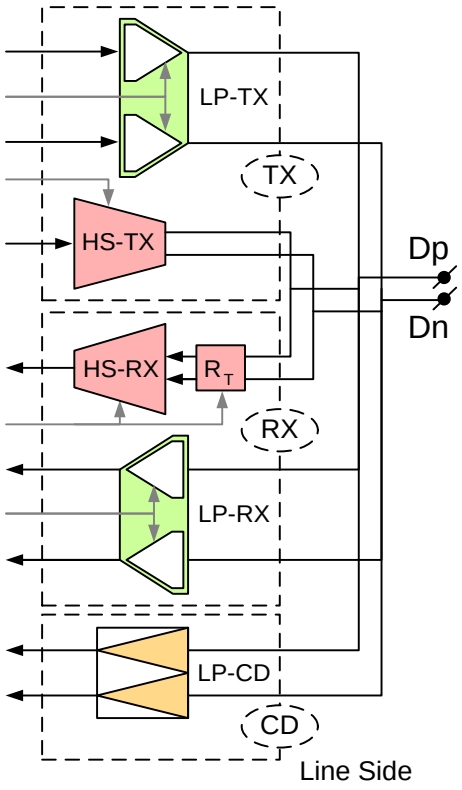


Figure 46 Electrical Functions of a Fully Featured D-PHY Transceiver

The HS transmitter and HS receiver are used for the transmission of the HS data and clock signals. The HS transmitter and receiver use low-voltage differential signaling for signal transmission. The HS receiver contains a switchable parallel termination.

The LP transmitter and LP receiver serve as a low power signaling mechanism. The LP transmitter is a push-pull driver and the LP receiver is an un-terminated, single-ended receiver.

The signal levels are different for differential HS mode and single-ended LP mode. ***Figure 47*** shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

All absolute voltage levels are relative to the ground voltage at the transmit side.

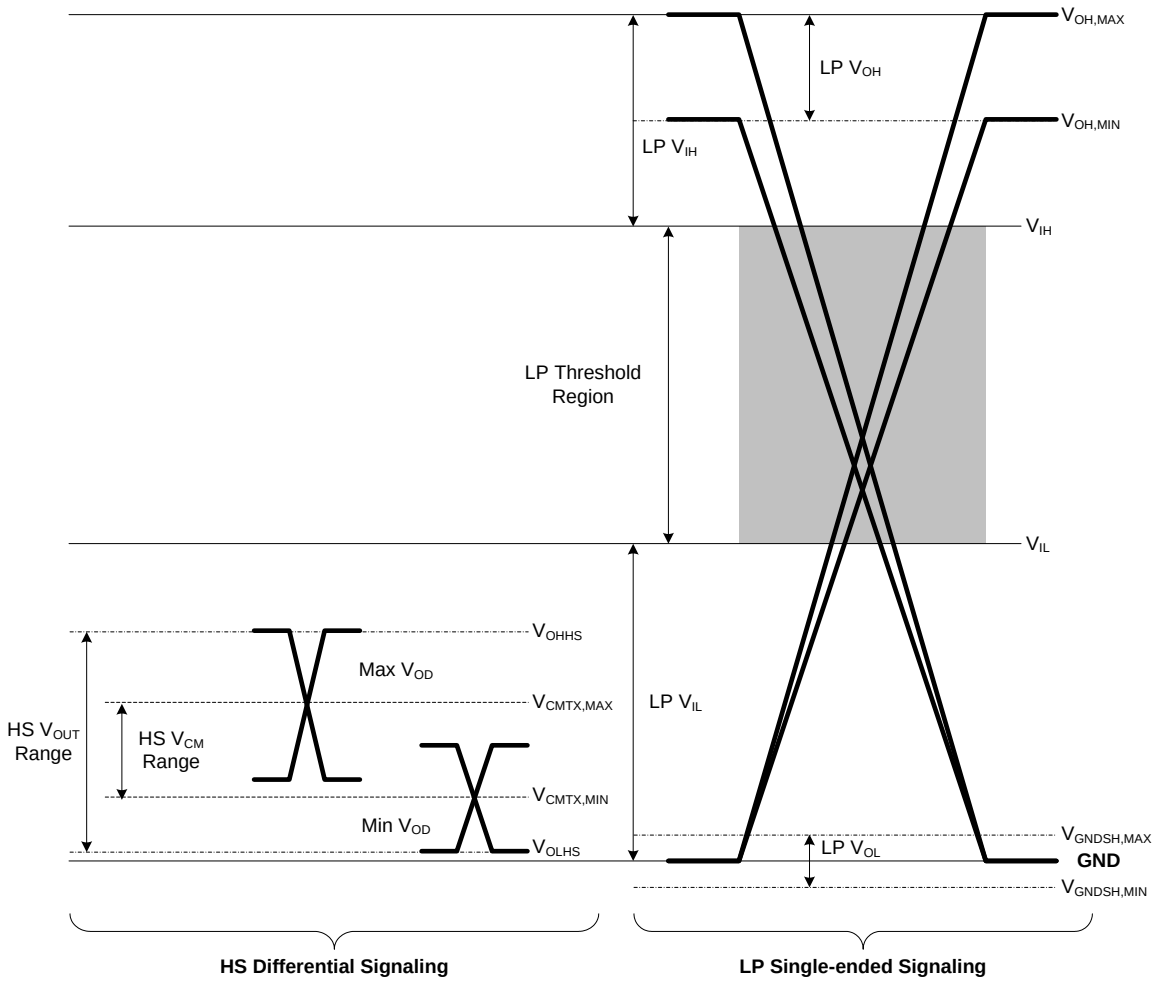


Figure 47 D-PHY Signaling Levels

A Lane switches between Low-Power and High-Speed mode during normal operation. Bidirectional Lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling certain electrical functions. These enable and disable events shall not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes shall be smooth to always ensure a proper detection of the Line signals.

9.1 Driver Characteristics

9.1.1 High-Speed Transmitter

9.1.1.1 Differential & Common Mode Swing

A HS differential signal driven on the Dp and Dn pins is generated by a differential output driver. For reference, Dp is considered as the positive side and Dn as the negative side. The Lane state is called Differential-1 (HS-1) when the potential on Dp is higher than the potential of Dn. The Lane state is called Differential-0 (HS-0), when the potential on Dp is lower than the potential of Dn. ***Figure 48*** shows an example implementation of a HS transmitter.

Note, this section uses Dp and Dn to reference the pins of a Lane Module regardless of whether the pins belong to a Clock Lane Module or a Data Lane Module.

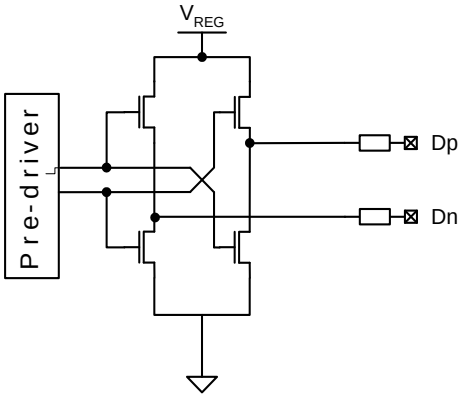


Figure 48 Example HS Transmitter

The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

The output voltages V_{DP} and V_{DN} at the Dp and Dn pins shall not exceed the High-Speed output high voltage V_{OHHS}. V_{OLHS} is the High-Speed output, low voltage on Dp and Dn and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}.

The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

V_{OD} and V_{CMTX} are graphically shown in ***Figure 49*** for ideal HS signals. ***Figure 50*** shows single-ended HS signals with the possible kinds of distortion of the differential output and common-mode voltages. V_{OD} and V_{CMTX} may be slightly different for driving a Differential-1 or a Differential-0 on the pins.

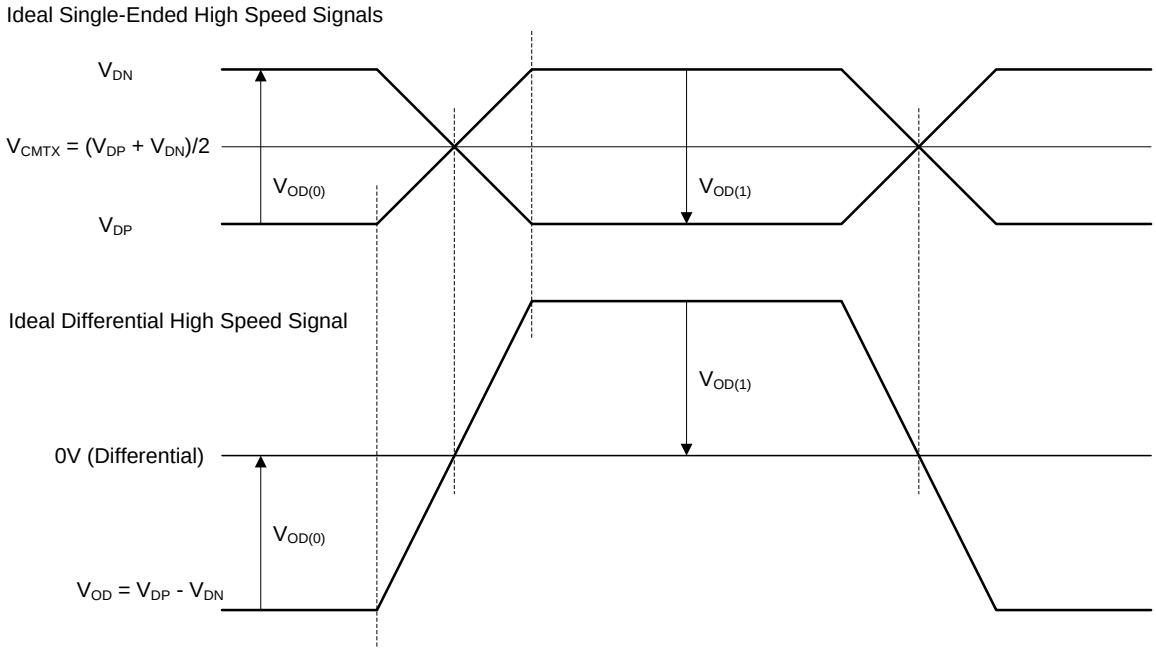


Figure 49 Ideal Single-Ended and Resulting Differential HS Signals

9.1.1.2 Differential Voltage Mismatch

The output differential voltage mismatch ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$. This is expressed by:

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

9.1.1.3 Static Common Mode Mismatch & Transient Common Mode Voltage

If $V_{CMTX(1)}$ and $V_{CMTX(0)}$ are the common-mode voltages for static Differential-1 and Differential-0 states respectively, then the common-mode reference voltage is defined by:

$$V_{CMTX,REF} = \frac{V_{CMTX(1)} + V_{CMTX(0)}}{2}$$

The transient common-mode voltage variation is defined by:

$$\Delta V_{CMTX}(t) = V_{CMTX}(t) - V_{CMTX,REF}$$

The static common-mode voltage mismatch between the Differential-1 and Differential-0 state is given by:

$$\Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

The transmitter shall send data such that the high frequency and low frequency common-mode voltage variations do not exceed $\Delta V_{CMTX(HF)}$ and $\Delta V_{CMTX(LF)}$, respectively. An example test circuit for the measurement of V_{OD} and V_{CMTX} is shown in ***Figure 51***.

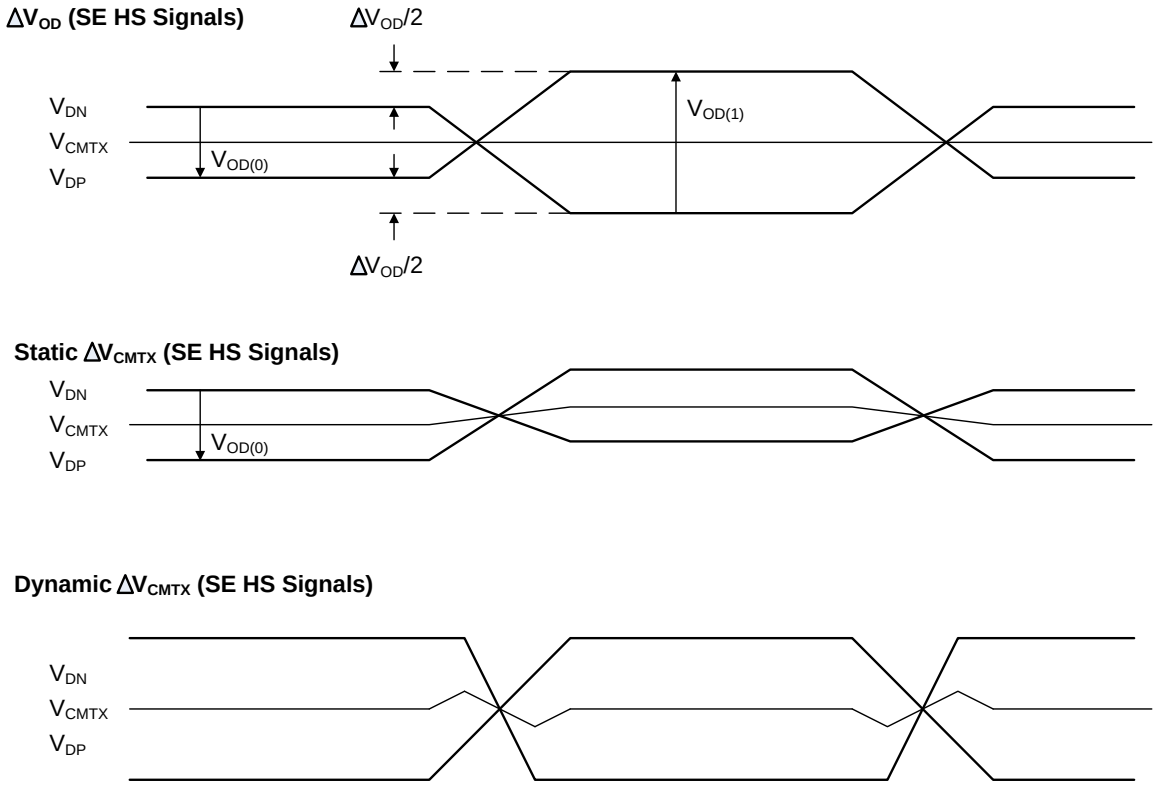


Figure 50 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

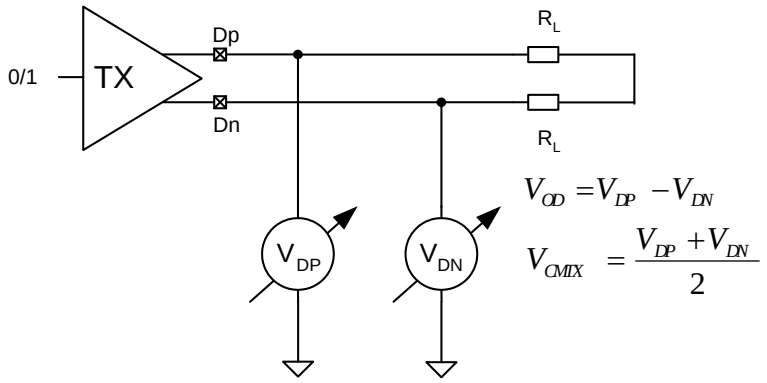


Figure 51 Example Circuit for VCMTX and VOD Measurements

9.1.1.4 Output Resistance

The single-ended output impedance of the transmitter at both the Dp and Dn pins is denoted by Z_{OS}. ΔZ_{OS} is the mismatch of the single ended output impedances at the Dp and Dn pins, denoted by Z_{OSDP} and Z_{OSDN}, respectively. This mismatch is defined as the ratio of the absolute value of the difference of Z_{OSDP} and Z_{OSDN} and the average of those impedances:

$$\Delta Z_{OS} = 2\frac{\left|Z_{OSDP} - Z_{OSDN}\right|}{Z_{OSDP} + Z_{OSDN}}$$

The output impedance Z_{OS} and the output impedance mismatch ΔZ_{OS} shall be compliant with ***Table 25*** for both the Differential-0 and Differential-1 states for all allowed loading conditions. It is recommended that implementations keep the output impedance during state transitions as close as possible to the steady state value. The output impedance Z_{OS} can be determined by injecting an AC current into the Dp and Dn pins and measuring the peak-to-peak voltage amplitude.

9.1.1.5 Rise/Fall Times

The rise and fall times, t_R and t_F, are defined as the transition time between 20% and 80% of the full HS signal swing. Full HS Swing can be calculated by driving a steady state pattern. The driver shall meet the t_R and t_F specifications for all allowable Z_{ID}. The specifications for TX common-mode return loss and the TX differential mode return loss can be found in ***Section 8***.

Rise/Fall Times are defined for a maximum data rate of 1.5 Gbps. For Data rates above 1.5 Gbps, the Eye diagram specification defined in ***Section 10.2.3*** governs the slew rate requirements of the transmitter.

It is recommended that a High-Speed transmitter that is directly terminated at its pins should not generate any overshoot in order to minimize EMI.

9.1.1.6 Half Swing Mode

In the Half Swing mode, differential swing of the transmitter is reduced to half that of the default swing specification. This is an optional mode that a transmitter can choose to support for power savings. Transmitter Half Swing mode can be used with the Receiver either in terminated or unterminated mode. Half Swing mode is defined for a termination ZID. There is no transmitter parameter defined for the operation with an unterminated receiver, due to the difficulty of measuring excess reflections on the line. Refer to the Receiver termination condition in ***Section 9.2.1***. A Transmitter with full swing operation shall not operate with a Receiver in unterminated mode due to the violation of V_{OHHS}.

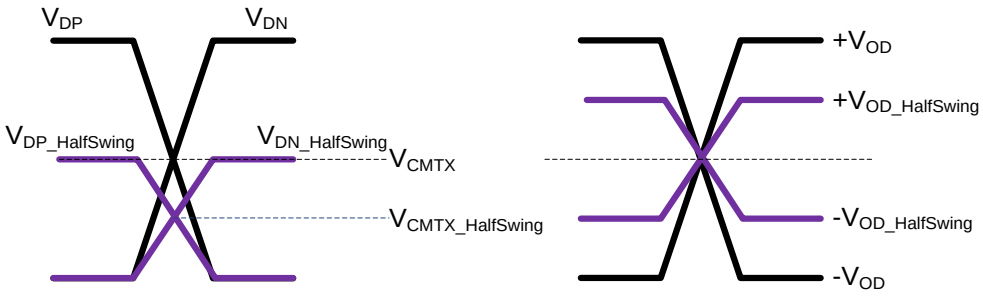


Figure 52 Common Mode and Differential Swing in Half Swing Mode versus Default

9.1.1.7 De-emphasis

To mitigate additional channel-induced ISI above 2.5Gbps, an HS-TX needs to use channel equalization in the form of de-emphasis. The transmitter de-emphasis has two taps, where the first tap is the cursor and the second tap is the first post-cursor. The taps are separated by UI and the transmitter de-emphasis ratio EQ_{TX} determines the de-emphasis level. Two de-emphasis ratios are defined.

Figure 53 shows an example transmit waveform with de-emphasis. After a logical bit transition, the amplitude of the differential output voltage signal $V_{DIF\_TX}(t)$ conforms to the differential AC output voltage amplitude V_{OD}. The next bit that retains the same logical state is reduced in amplitude. The differential AC output voltage amplitude with de-emphasis V_{OD_EQ} is defined as the reduced amplitude. EQ_{TX} is defined as the minus 20 log of the ratio of V_{OD_EQ} and V_{OD} as shown in the following equation:

$$EQ_{TX} = -20\log\left(\frac{V_{OD\_EQ}}{V_{OD}}\right)$$

Figure 53 De-emphasis Example

1082 **Table 25 HS Transmitter DC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
EQ_{TX1}	De-emphasis Option 1	2.5	3.5	4.5	dB	1
EQ_{TX2}	De-emphasis Option 2	6	7	8	dB	1
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	2
$V_{CMTX\_HalfSwing}$	HS transmit static common-mode voltage in Half Swing Mode	75	100	250	mV	2, 4
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	3
$\lvert V_{OD}\rvert$	HS transmit differential voltage	140	200	270	mV	2
$\lvert V_{OD\_HalfSwing}\rvert$	HS transmit differential voltage In Half Swing Mode	70	100	135	mV	2, 4
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0			14	mV	3
V_{OHHS}	HS output high voltage			360	mV	2
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			20	%	

Note:

1. *When the supported data rate is > 2.5 Gbps. Conformance requirements for the transmitter are defined through the eye diagram. The values for equalization in this table are informative.*
2. *Value when driving into load impedance anywhere in the ZID range.*
3. *A transmitter should minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.*
4. *Half Swing Mode is optional. It is an additional capability a transmitter can support for better system power optimization.*

1083 **Table 26 HS Transmitter AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1, 2
				0.35	UI	1, 3
		100			ps	4

Note:

1. *UI is equal to 1/(2*fh). See **Section 8.3** for the definition of fh.*
2. *Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).*
3. *Applicable when supporting maximum HS bit rates > 1 Gbps (UI ≤ 1 ns) but ≤ 1.5 Gbps (UI ≥ 0.667 ns).*
4. *Applicable when supporting maximum HS bit rates ≤ 1.5 Gbps. However, to avoid excessive radiation, bit rates < 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.*

9.1.2 Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of an LP transmitter is as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low. A Low-Power transmitter may additionally support the optional Low Voltage Low Power operation, in which the maximum output voltage is limited in comparison to the normal Low Power mode.

An example of an LP transmitter is shown in ***Figure 54***.

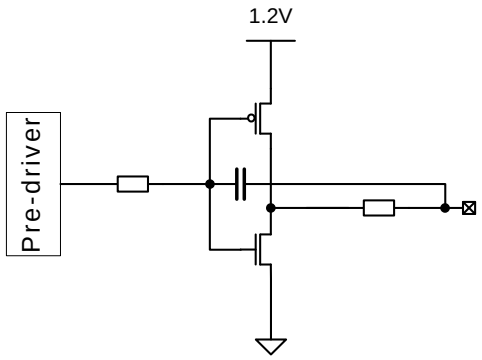


Figure 54 Example LP Transmitter

V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded. The LP transmitter shall not drive the pad pin potential statically beyond the maximum value of V_{OH}. The pull-up and pull-down output impedances of LP transmitters shall be as described in ***Figure 55*** and ***Figure 56***, respectively. The circuit for measuring V_{OL} and V_{OH} is shown in ***Figure 57***.

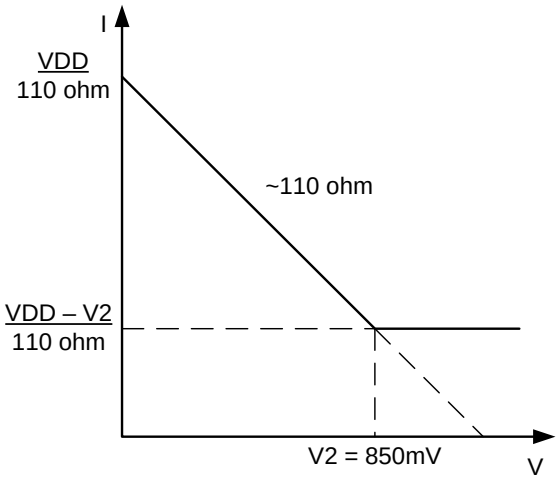


Figure 55 V-I Characteristic for LP Transmitter Driving Logic High

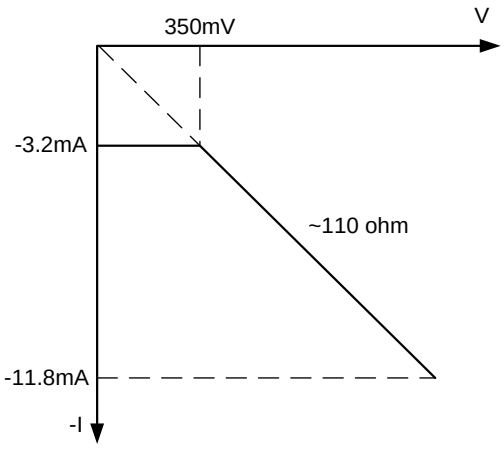


Figure 56 V-I Characteristic for LP Transmitter Driving Logic Low

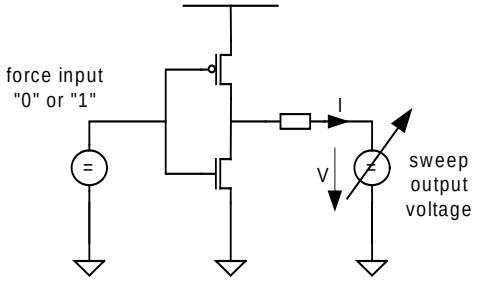


Figure 57 LP Transmitter V-I Characteristic Measurement Setup

The impedance Z_{OLP} is defined by:

$$Z_{OLP} = \left| \frac{V_{THEVENIN} - V_{PIN}}{I_{OUT}} \right|$$

The times T_{RLP} and T_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The LP transmitter output signal transitions shall meet the maximum and minimum slew rate specifications as shown in ***Table 28***. The intention of specifying a maximum slew rate value is to limit EMI.

Table 27 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	1
		0.95	–	1.3	V	2
		0.95	–	1.1	V	3
V_{OL}	Thevenin output low level	-50	–	50	mV	–
Z_{OLP}	Output impedance of LP transmitter	110	–	–	Ω	4, 5

Note:

1. *Applicable in normal Low Power mode when the supported data rate ≤1.5 Gbps.*
2. *Applicable in normal Low Power mode when the supported data rate > 1.5 Gbps.*
3. *Applicable for all data rates when Lane Module is in optional LVLP operation.*
4. *See **Figure 55** and **Figure 56**.*
5. *Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.*

1109 **Table 28 LP Transmitter AC Specifications**

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	5, 6
$T_{LP\text{-}PULSE\text{-}TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF				500	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 5pF				300	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 20pF				250	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 70pF				150	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)		30			mV/ns	1, 2, 3, 12
			25			mV/ns	1, 3, 13, 16
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30			mV/ns	1, 3, 9, 12
			25			mV/ns	1, 3, 13, 15
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30 – 0.075 * ($V_{O,INST}$ – 700)			mV/ns	1, 3, 10, 11, 12
			25 – 0.0625 * ($V_{O,INST}$ – 550)			mV/ns	1, 3, 10, 14, 13
C_{LOAD}	Load capacitance		0		70	pF	1

Note:

1. *C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 400 mV and 930 mV.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in **Section 9.2.2**.*
5. *The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance C_{CM} between 0 and 60 pF on the termination center tap at RX side of the Lane*
7. *This value represents a corner point in a piece-wise linear curve.*
8. *When the output voltage is in the range specified by $V_{PIN(absmax)}$.*
9. *When the output voltage is between 400 mV and 700 mV.*
10. *Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts.*
11. *When the output voltage is between 700 mV and 930 mV.*
12. *Applicable when the supported data rate ≤ 1.5 Gbps.*
13. *Applicable when the supported data rate > 1.5 Gbps.*
14. *When the output voltage is between 550 mV and 790 mV*
15. *When the output voltage is between 400 mV and 550 mV*
16. *When the output voltage is between 400 mV and 790 mV*

There are minimum requirements on the duration of each LP state. To determine the duration of the LP state, the Dp and Dn signal lines are each compared to a common trip-level. The result of these comparisons is then exclusive-ORed to produce a single pulse train. The output of this “exclusive-OR clock” can then be used to find the minimum pulse width output of an LP transmitter.

Using a common trip-level in the range [$V_{IL,MAX}$ + $V_{OL,MIN}$, $V_{IH,MIN}$ + $V_{OL,MAX}$], the exclusive-OR clock shall not contain pulses shorter than $T_{LP\text{-}PULSE\text{-}TX}$.

9.2 Receiver Characteristics

9.2.1 High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. A simplified diagram of an example implementation using a PMOS input stage is shown in ***Figure 58***.

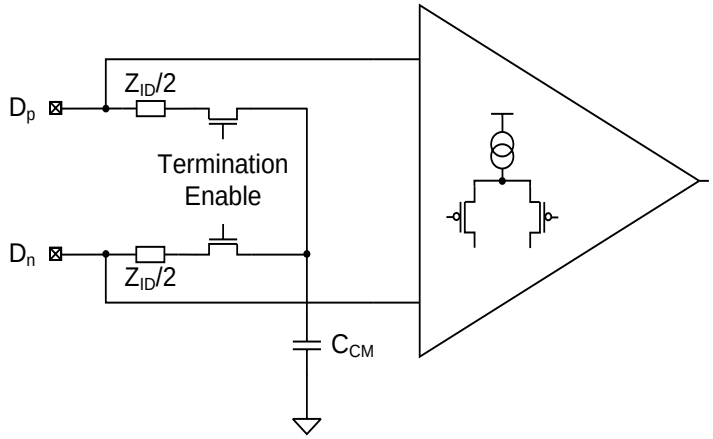


Figure 58 HS Receiver Implementation Example

The differential input high and low threshold voltages of the HS receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively. $V_{CMRX(DC)}$ is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its Dp and Dn input signal pins when both signal voltages, V_{DP} and V_{DN}, are within the common-mode voltage range and if the voltage difference of V_{DP} and V_{DN} exceeds either V_{IDTH} or V_{IDTL}. The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference $\Delta V_{CMRX(HF)}$ and $\Delta V_{CMRX(LF)}$.

During operation of the HS receiver, termination impedance Z_{ID} is required between the Dp and Dn pins of the HS receiver. Z_{ID} shall be disabled when the module is not in the HS receive mode. When transitioning from Low-Power Mode to HS receive mode the termination impedance shall not be enabled until the single-ended input voltages on both Dp and Dn fall below $V_{TERM-EN}$. To meet this requirement, a receiver does not need to sense the Dp and Dn lines to determine when to enable the line termination, rather the LP to HS transition timing can allow the line voltages to fall to the appropriate level before the line termination is enabled.

The RX common-mode return loss and the RX differential mode return loss are specified in ***Section 8***. C_{CM} is the common-mode AC termination, which ensures a proper termination of the receiver at higher frequencies. For higher data rates, C_{CM} is needed at the termination center tap in order to meet the common-mode reflection requirements.

When a Transmitter is in Half Swing mode, the receiver may choose to turn off the termination in High Speed mode for lower data rate operation. This is an optional mode that can be supported in addition to the default mode. A receiver in unterminated mode shall not operate with TX full swing.

1141 **Table 29 HS Receiver DC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	1, 2
Z_{ID}	Differential input impedance	80	100	125	Ω	3
Z_{ID_Open}	Differential input impedance in unterminated mode	10K	–	–	Ω	4

Note:

1. *Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.*
2. *This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz*
3. *Z_{ID} can be higher than 125 ohms in unterminated mode.*
4. *Unterminated mode for HS-RX is optional. This mode can only be used when a transmitter is in Half Swing mode. Z_{ID_OPEN} is defined for a differential voltage with maximum amplitude of $\lvert V_{OD\_Halfswing}\rvert$ and within the common voltage range of $V_{CMTX\_Halfswing}$.*

1142 **Table 30 HS Receiver AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV	2, 5
				50	mV	2, 6
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV	1, 4, 5
		-25		25	mV	1, 4, 6
V_{IDTH}	Differential input high threshold			70	mV	5
				40	mV	6
V_{IDTL}	Differential input low threshold	-70			mV	5
		-40			mV	6
V_{IHHS}	Single-ended input high voltage			460	mV	7
V_{ILHS}	Single-ended input low voltage	-40			mV	7
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
C_{CM}	Common-mode termination			60	pF	3

Note:

1. *Excluding 'static' ground shift of 50mV*
2. *$\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.*
3. *For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.*
4. *Voltage difference compared to the DC average common-mode potential.*
5. *For devices supporting data rates ≤ 1.5 Gbps.*
6. *For devices supporting data rates > 1.5 Gbps.*
7. *Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.*

9.2.2 Low-Power Receiver

1143 The Low-Power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to
1144 detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses
1145 and RF interference. It is recommended the implementer optimize the LP receiver design for low power.

1146 The input low-level voltage, V_{IL}, is the voltage at which the receiver is required to detect a low state in the
1147 input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power
1148 State. V_{IL} is larger than the maximum single-ended Line voltage during HS transmission. Therefore, an LP
1149 receiver shall detect low during HS signaling.

The input high-level voltage, V_{IH}, is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a hysteresis, The hysteresis voltage is defined as V_{HYST}.

The LP receiver shall reject any input signal smaller than e_{SPIKE}. Signal pulses wider than T_{MIN-RX} shall propagate through the LP receiver.

Furthermore, the LP receivers shall be tolerant of super-positioned RF interference on top of the wanted Line signals. This implies an input signal filter. The LP receiver shall meet all specifications for interference with peak amplitude V_{INT} and frequency f_{INT}. The interference shall not cause glitches or incorrect operation during signal transitions.

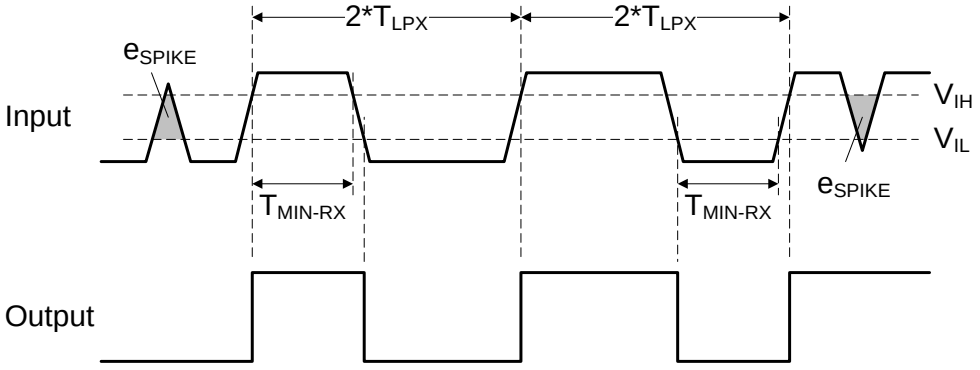


Figure 59 Input Glitch Rejection of Low-Power Receivers

Table 31 LP Receiver DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	740			mV	1
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Note:

1. *V_{IH} applies to all data rates from D-PHY v2.1 onwards. A D-PHY v2.0 or earlier LP receiver is compatible with a D-PHY v2.1 transmitter in LP mode.*

Table 32 LP Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Note:

1. *Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. eSpike generation will ensure the spike is crossing both $V_{IL,max}$ and $V_{IH,min}$ levels.*
2. *An impulse less than this will not change the receiver state.*
3. *In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.*
4. *An input pulse greater than this shall toggle the output.*

9.3 Line Contention Detection

The Low-Power receiver and a separate Contention Detector (LP-CD) shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-Power signal. This is required to detect line contention as described in ***Section 7.1***. The Low-Power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL}. Refer to ***Table 31***. The LP-CD shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD}. Refer to ***Table 33***. An LP low fault shall not be detected when the pin voltage is less than V_{ILCD}.

The general operation of a contention detector shall be similar to that of an LP receiver with lower threshold voltages. Although the DC specifications differ, the AC specifications of the LP-CD are defined to match those of the LP receiver and the LP-CD shall meet the specifications listed in ***Table 32*** except for T_{MIN-RX}. The LP-CD shall sufficiently filter the input signal to avoid false triggering on short events.

The LP-CD threshold voltages (V_{ILCD}, V_{IHCD}) are shown along with the normal signaling voltages in ***Figure 60***.

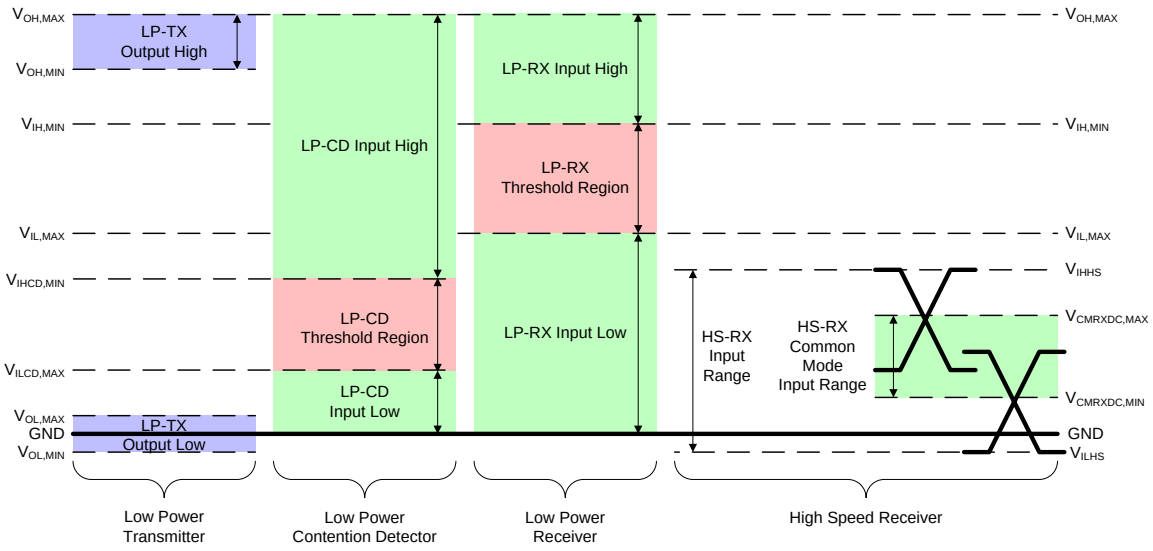


Figure 60 Signaling and Contention Voltage Levels

Table 33 Contention Detector (LP-CD) DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IHCD}	Logic 1 contention threshold	450			mV	
V_{ILCD}	Logic 0 contention threshold			200	mV	

9.4 Input Characteristics

No structure within the PHY may be damaged when a DC signal within the signal voltage range V_{PIN} is applied to a pad pin for an indefinite period of time. $V_{PIN(absmax)}$ is the maximum transient output voltage at the transmitter pin. The transmitter output voltage shall not exceed $V_{PIN,MAX}$ for a period greater than $T_{VPIN(absmax)}$. When the PHY is in the Low-Power receive mode the pad pin leakage current shall be I_{LEAK} when the pad signal voltage is within the signal voltage range of V_{PIN}. When a PHY is operated in the optional LVLP operating range, the pad pin leakage current shall be within the range defined by I_{LEAK} for pad signal voltages in the range of V_{PIN_LVLP}. The specification of I_{LEAK} assures interoperability of any PHY in the LP mode by restricting the maximum load current of an LP transmitter. An example test circuit for leakage current measurement is shown in ***Figure 61***.

The ground supply voltages shifts between a Master and a Slave shall be less than V_{GNDSH}.

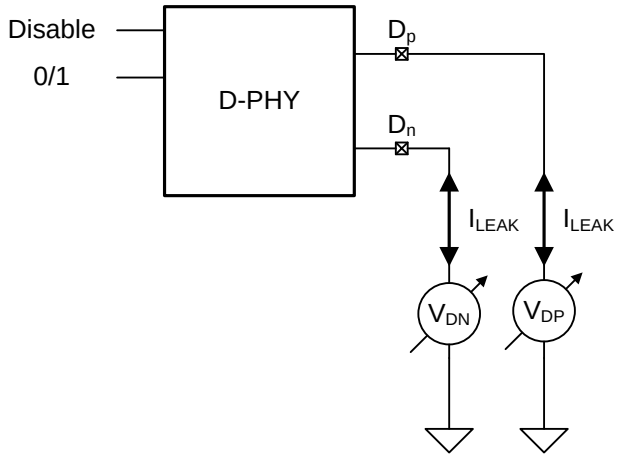


Figure 61 Pin Leakage Measurement Example Circuit

Table 34 Pin Characteristic Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50	–	1350	mV	–
V_{PIN_LVLP}	Pin signal voltage range in LVLP operation	-50	–	1150	mV	–
I_{LEAK}	Pin leakage current	-100	–	100	µA	1
V_{GNDSH}	Ground shift	-50	–	50	mV	
		-5	–	5	mV	2
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15	–	1.45	V	3, 4
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	–	–	20	ns	–

Note:

1. *When the Lane Module is in LP receive mode and the pad voltage is in the signal voltage range V_{PIN} for LP mode, or in the signal range V_{PIN_LVLP} for LVLP operation, I_{LEAK} should be well within the limits in LVLP operation.*
2. *Ground shift when operating in Half Swing mode.*
3. *The voltage overshoot and undershoot beyond the V_{PIN} range is only allowed for a duration of $T_{VPIN(absmax)}$ after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.*
4. *This value includes ground shift.*

10 High-Speed Data-Clock Timing

This section specifies the required timings on the High-Speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

Data transmission may occur at any rate greater than the minimum specified data bit rate.

Figure 62 shows an example PHY configuration including the compliance measurement planes for the specified timings. Note that the effect of signal degradation inside each package due to parasitic effects is included in the timing budget for the transmitter and receiver and is not included in the interconnect degradation budget. See ***Section 8*** for details.

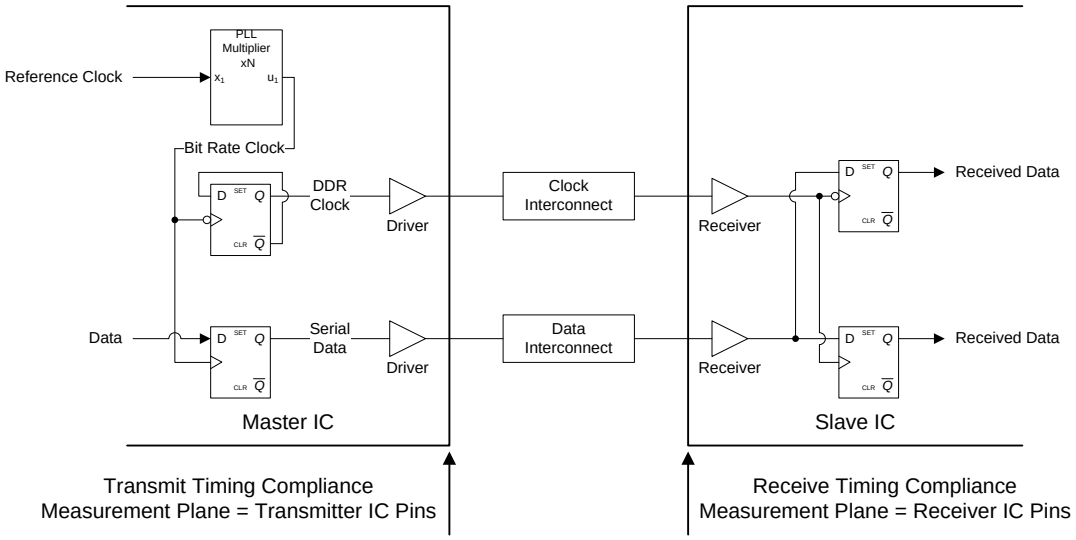


Figure 62 Conceptual D-PHY Data and Clock Timing Compliance Measurement Planes

10.1 High-Speed Clock Timing

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKp – CLKn, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in ***Figure 63***.

Note that the UI indicated in ***Figure 63*** is the instantaneous UI. Implementers shall specify a maximum data rate and corresponding maximum clock frequency, fh_{MAX}, for a given implementation. For a description of fh_{MAX}, see ***Section 8.3***.

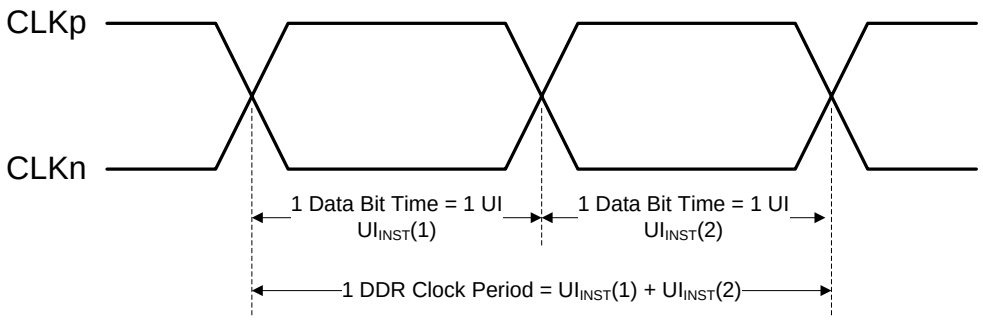


Figure 63 DDR Clock Definition

As can be seen in ***Figure 62***, the same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate instantaneous variations in UI for an ongoing burst defined by ΔUI. Being a forwarded clock link, the low frequency jitter is expected to be tracked up to a data rate/20. Example values are:

- 225 MHz at 4.5 Gbps,
- 125 MHz at 2.5 Gbps, or
- 75 MHz at 1.5 Gbps.

The high frequency jitter beyond a data rate/2 can be neglected.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall accommodate these instantaneous variations with appropriate logic. It is recommended that devices accommodate these instantaneous variations using some method, such as with appropriate FIFO logic outside of the PHY, or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations, or the data sink outside the PHY can be designed to be tolerant of UI variations.

A device shall conform with the Period Jitter limits.

- When SSC is disabled, the Period Jitter is defined as the peak-to-peak deviation of a clock period over the average of 32 k periods of continuous clock cycles.
- When SSC is enabled, the Period Jitter is defined as the peak-to-peak deviation of a clock period over the average clock cycle of one or more complete SSC modulation cycles.

The UI_{INST} specifications for the Clock signal are summarized in ***Table 35***.

Table 35 Clock Signal Specification

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1, 2
UI variation	ΔUI	-10%		10%	UI	
Period Jitter		-5%		5%		3

Note:

1. *This value corresponds to a minimum operating data rate of 80 Mbps. This instantaneous value does not take into account UI variations due to jitter or SSC modulation.*
2. *The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, devices should either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.*
3. *Applies when the DDR clock period within a single burst (i.e. clock rising edge to next rising edge) is ≥ 0.444ns and < 0.8ns.*

10.2 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in ***Figure 64***. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

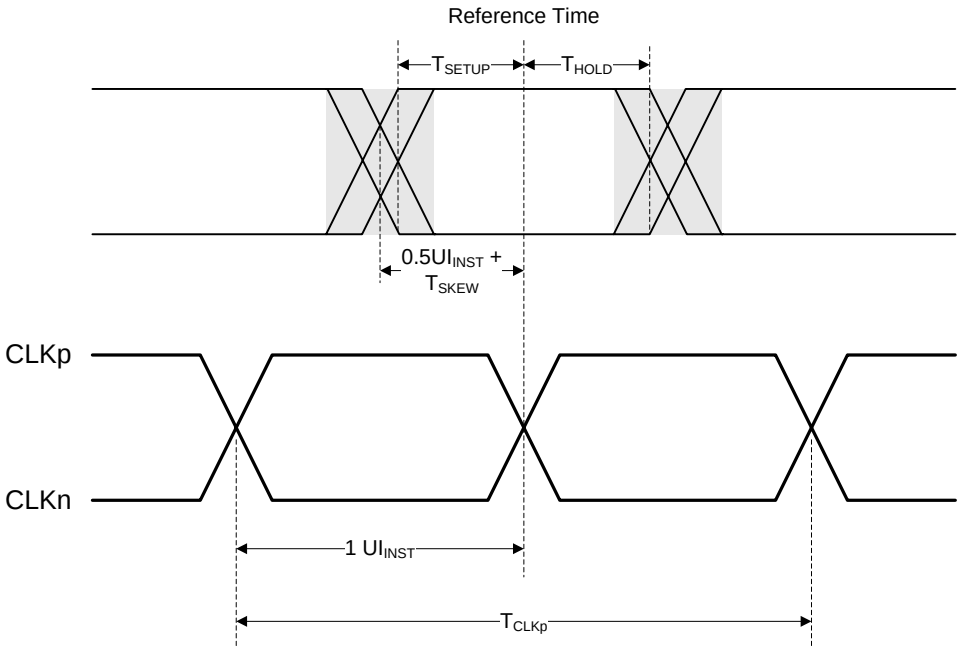


Figure 64 Data to Clock Timing Definitions

10.2.1 Data-Clock Timing Specifications

10.2.1.1 Data Rate ≥ 0.08 Gbps and ≤ 1 Gbps

The Data-Clock timing parameters shown in ***Figure 64*** are specified in ***Table 36***. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX}$] and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

Table 36 Data-Clock Timing Specifications for ≥ 0.08 Gbps and ≤ 1 Gbps

Parameter	Symbol	Min	Max	Unit	Note
HS-TX Timing					
TX Data to Clock Skew	$T_{SKEW[TX]}$	-0.15	0.15	UI_{HS}	1
HS-RX Timing					
RX Data to Clock Setup Time Tolerance	$T_{SETUP[RX]}$	0.15		UI_{HS}	1
RX Data to Clock Hold Time Tolerance	$T_{HOLD[RX]}$	0.15		UI_{HS}	1
Channel Timing					
Channel Data to Clock Skew	$T_{SKEW[TLIS]}$	-0.2	0.2	UI_{HS}	

Note:

1. *All jitter specifications are specified with a 100 ohm differential termination*

10.2.1.2 Data Rate > 1 Gbps and ≤ 1.5 Gbps

The timing budget has been adjusted between the Transmitter, Receiver, and Channel to support a maximum data rate of 1.5 Gbps.

Table 37 Data-Clock Timing Specifications for > 1 Gbps and ≤ 1.5 Gbps

Parameter	Symbol	Min	Max	Unit	Note
HS-TX Timing					
TX Data to Clock Skew	$T_{SKEW[TX]}$	-0.2	0.2	UI_{HS}	1
HS-RX Timing					
RX Data to Clock Setup Time Tolerance	$T_{SETUP[RX]}$	0.2		UI_{HS}	1
RX Data to Clock Hold Time Tolerance	$T_{HOLD[RX]}$	0.2		UI_{HS}	1
Channel Timing					
Channel Data to Clock Skew	$T_{SKEW[TLIS]}$	-0.1	0.1	UI_{HS}	

Note:

1. *All jitter specifications are specified with a 100 ohm differential termination*

10.2.1.3 Data Rate > 1.5 Gbps and ≤ 4.5 Gbps

For higher data rate operation, jitter specifications have been decomposed into Deterministic jitter and Random jitter based on a target BER of 10^{-12}. Meeting the jitter specifications is a recommendation, whereas meeting the Eye diagram specification is a requirement.

Table 38 Data-Clock Timing Specifications for > 1.5 Gbps and ≤ 4.5 Gbps

Parameter	Symbol	Min	Max	Unit	Note
HS-TX Timing					
TX Data to Clock Total Jitter	TJ_{TX}		0.3	UI_{HS}	1
TX Data to Clock Deterministic Jitter	DJ_{TX}		0.2	UI_{HS}	1
TX Data to Clock Random Jitter	RJ_{TX}		0.1	UI_{HS}	1
TX Static Data to Clock Skew	$T_{SKEW[TX]}$ static	-0.2	0.2	UI_{HS}	1
HS-RX Timing					
RX Data to Clock Total Jitter Tolerance	TJ_{RX}	0.50		UI_{HS}	1
RX Data to Clock Deterministic Jitter Tolerance	DJ_{RX}	0.40		UI_{HS}	1
RX Data to Clock Random Jitter Tolerance	RJ_{RX}	0.10		UI_{HS}	1
RX Static Data to Clock Skew Tolerance	$T_{SKEW[RX]}$ static	-0.3	0.3	UI_{HS}	1
Channel Timing					
Channel Static Data to Clock Skew	$T_{SKEW[TLIS]}$ static	-0.1	0.1	UI_{HS}	
Limit for BER					
Target Bit Error Rate	BER		10^{-12}		
Q Factor for BER	Q_{BER}		7.0345		

Note:

1. *All jitter specifications are specified with a 100 ohm differential termination*

10.2.2 Normative Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (sometimes referred to as “Spectrum Spread Clocking”) is a common technique where a low frequency modulation is added to the Transmitter’s clock to reduce the peak emissions.

All Transmitters conformant to D-PHY v2.0 and above shall support SSC as per ***Table 39*** for data rates operating above 2.5 Gbps.

All Receivers conformant to D-PHY v2.0 and above shall support SSC as per ***Table 39*** for data rates operating above 2.5 Gbps.

All Transmitters conformant to D-PHY v2.0 and above shall provide the system integrator with a mechanism to enable/disable SSC transmissions.

SSC can be used in HS Data Transmission Mode. If used during HS Data Transmission Mode, SSC transmission shall be consistent during the entire mode.

SSC should not be used in Escape mode.

SSC shall be implemented within the Transmitter such that a single modulated profile, single modulation rate and a single SSC deviation is common between the clock and all High-speed data lanes.

All SSC parameters are defined for the HS Clock.

Modulation using a triangular profile for the frequency spread should be the baseline. Implementers can provide further emissions reduction using more-complex modulation profiles.

Table 39 Spread Spectrum Clocking Requirements

Parameter	Symbol	Min	Max	Units	Notes
Modulation Rate	$T_{SSC\_MOD\_RATE}$	30	33	kHz	
SSC Deviation	$T_{SSC\_FREQ\_DEV}$	-5000	0	PPM	1, 2
SSC df/dt	$SSC_{df/dt}$	N/A	1250	PPM/µs	3, 4, 5

Note:

1. *The required SSC deviation is also called “Down-Spread”.*
2. *Any implementation with an SSC deviation significantly smaller than 5000 PPM may fail in EMI testing below 1 GHz clock rate (Data Rate < 2 Gbps).*
3. *df/dt limit shall be for clock and all data lanes.*
4. *Measured over a 0.5 µs interval using an alternating 010101010… input pattern at highest data rate. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be a second order low-pass of 40 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.*
5. *Maximum change rate of 1250 PPM/µs is limiting the absolute value of the df/dt.*

10.2.3 Transmitter Eye Diagram Specification

The Eye Diagram Specification shown below is applicable to Transmitters operating at data rates greater than 1.5 Gbps and less than or equal to 4.5 Gbps, and is specified for differential data signals with regard to the differential zero of the forwarded clock. This Transmitter Eye Diagram Specification applies after passing through the reference channel described in TLIS and differential termination of 100 Ohms. A Prorated Eye Diagram is specified for a higher BER, in order to reduce validation time.

The Transmitter Eye Diagram Specification applies to both Data Lanes and Clock Lanes.

The method to measure the Transmitter Eye Diagram of the Clock Lane is defined in the CTS document.

The Clock Lane signal is also limited, as per the HS Clock Timing defined in ***Section 10.1***.

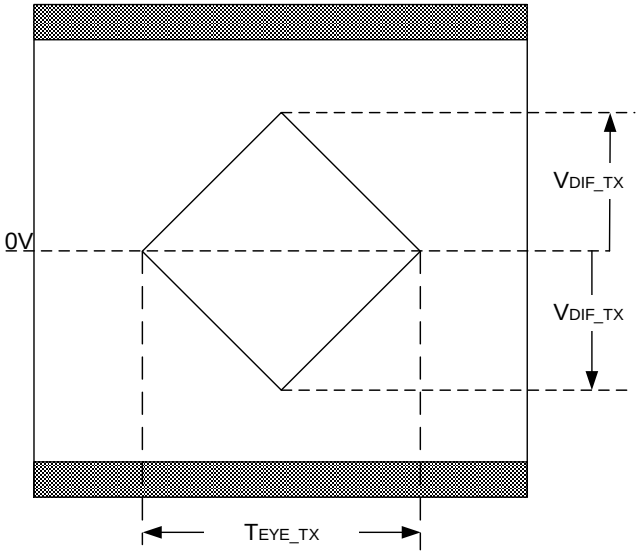


Figure 65 TX Eye Diagram Specification

Table 40 Transmitter Eye Diagram Specification

Bit Error Rate	TEYE_TX	VDIF_TX
10^{-12}	0.5UI	40mV
10^{-6} (Prorated for Validation)	0.53UI	47mV

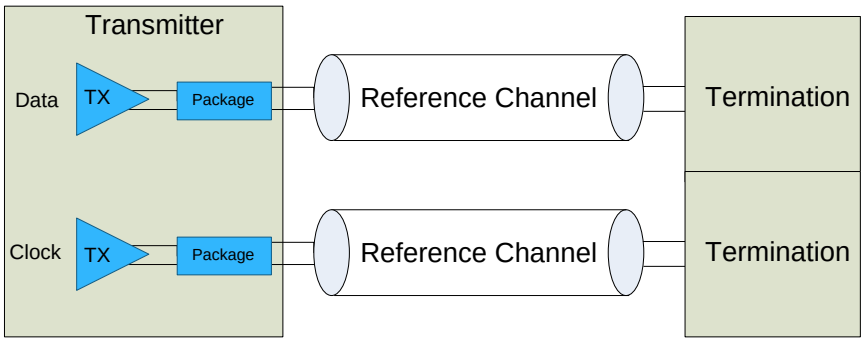


Figure 66 Transmitter Eye Diagram Validation Setup

10.2.4 Receiver Eye Diagram Specification

The Receiver Eye Diagram Specification shown below defines the worst-case Eye that the Receiver shall tolerate while injected at the Rx pads. This Eye Diagram Specification applies to Receivers operating at data rates between 1.5 Gbps and 4.5 Gbps.

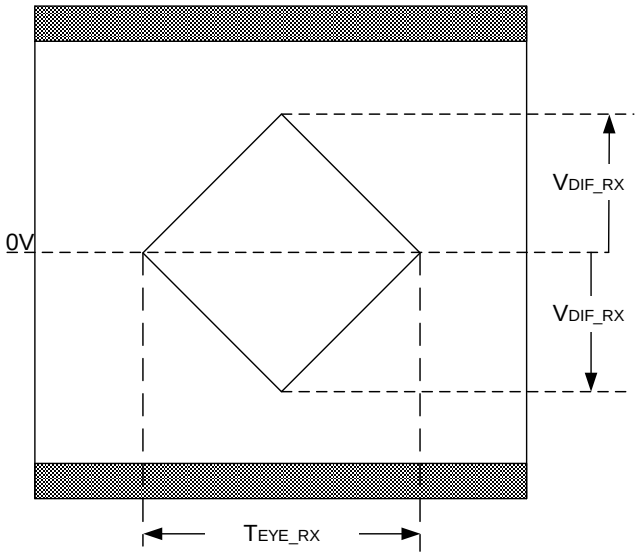


Figure 67 Receiver Eye Diagram Specification

Table 41 Receiver Eye Diagram Specification

Bit Error Rate	TEYE_RX	VDIF_RX
10^{-12}	0.5UI	40mV
10^{-6} (Prorated for Validation)	0.53UI	47mV

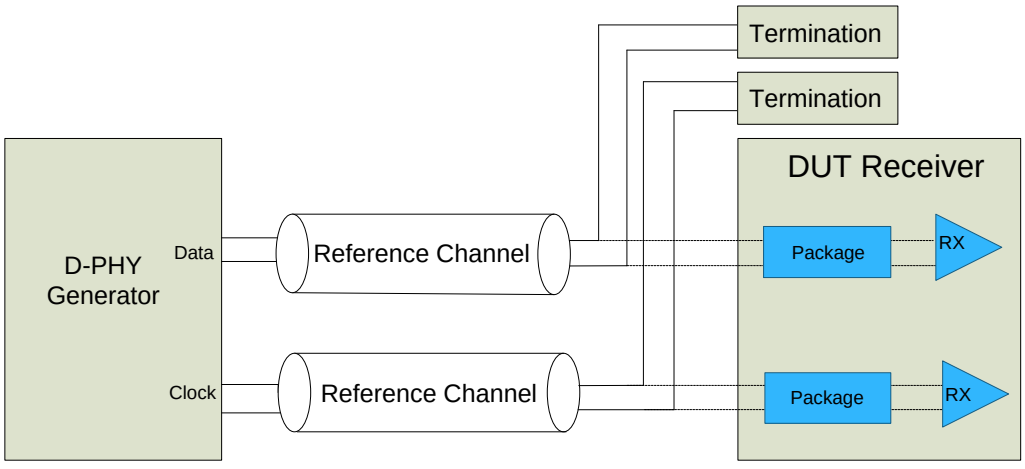


Figure 68 Receiver Eye Diagram Validation Setup

10.3 Reverse High-Speed Data Transmission Timing

This section only applies to Half-Duplex Lane Modules that include Reverse High-Speed Data Transmission functionality.

A Lane enters the Reverse High-Speed Data Transmission mode by means of a Link Turnaround procedure as specified in ***Section 6.5***. Reverse Data Transmission is not source-synchronous; the Clock signal is driven by the Master side while the Data Lane is driven by the Slave side. The Slave Side transmitter shall send one data bit every two periods of the received Clock signal. Therefore, for a given Clock frequency, the Reverse direction data rate is one-fourth the Forward direction data rate. The bit period in this case is defined to be 4*UI_{INST}. UI_{INST} is the value specified for the full-rate forward transmission.

Note that the clock source frequency may change between transmission bursts. However, all Data Lanes shall be in a Low-Power state before changing the clock source frequency.

The conceptual overview of Reverse HS Data Transmission is shown in ***Figure 69***.

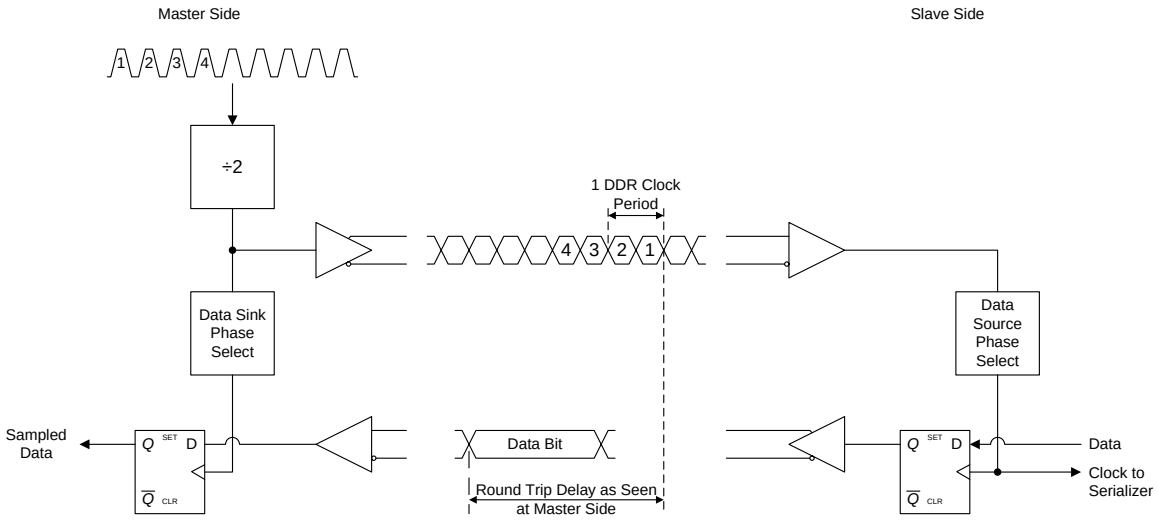


Figure 69 Conceptual View of HS Data Transmission in Reverse Direction

There are four possible phase relationships between clock and data signals in the Reverse direction. The Clock phase used to send data is at the discretion of the Slave side, but once chosen it shall remain fixed throughout that data transmission burst. Signal delays in the interconnect, together with internal signal delays in the Master and Slave Modules, cause a fixed, but unknown, phase relationship in the Master Module between received (Reverse) Data and its own (Forward) Clock. Therefore, the Reverse traffic arriving at the Master side may not be phase aligned with the Forward direction clock.

Synchronization between Clock and Data signals is achieved with the Sync sequence sent by the Slave during the Start of Transmission (SoT). The Master shall include sufficient functionality to correctly sample the received data given the instantaneous UI variations of the Clock sent to the Slave.

Reverse transmission by the Slave side is one-fourth of the Forward direction speed, based on the Forward direction Clock as transmitted via the Clock Lane. This ratio makes it easy to find a suitable phase at the Master Side for Data recovery of Reverse direction traffic.

The known transitions of the received Sync sequence shall be used to select an appropriate phase of the clock signal for data sampling. Thus, there is no need to specify the round trip delay between the source of the clock and the receiver of the data.

The timing of the Reverse transmission as seen at the Slave side is shown in ***Figure 70***.

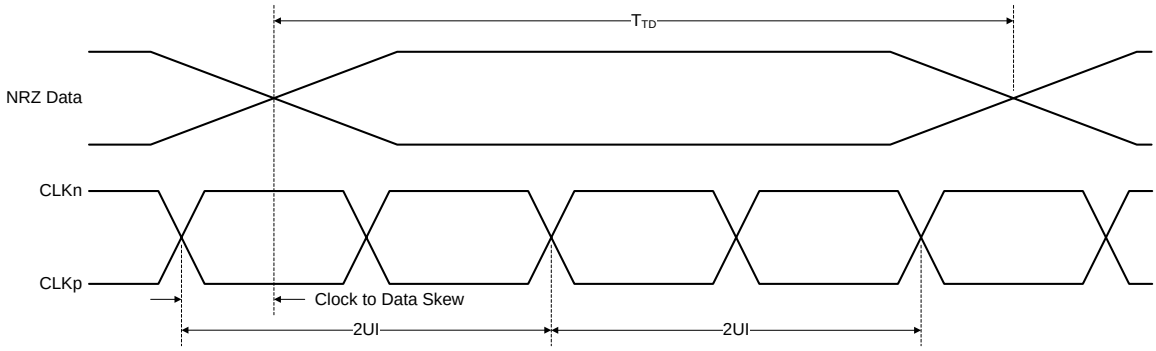


Figure 70 Reverse High-Speed Data Transmission Timing at Slave Side

10.4 Operating Modes: Data Rate and Channel Support Guidance

Table 42 shows the possible configurations of a transmitter, channel, and receiver that can be supported based on the D-PHY v2.1 electrical specification.

Mode 1 is the default configuration targeted to meet the maximum data rate.

Mode 2 is an optional configuration targeted at supporting higher-loss interconnect.

Modes 3 through 10 are optional configurations and are targeted at lowering system-level power consumption. A system design can use these modes based on the transmitter and receiver capabilities.

This section is only a guide for system-level optimization.

Table 42 Operating Modes and Guidance

Modes	Data Rate	Transmitter		Reference Channel	Receiver Termination	Notes
		Swing	De-emphasis			
0	≤ 6.5Gbps	Default	EQ2	Short	80-125 ohms	1
1	≤ 4.5Gbps	Default	EQ2	Short/Standard	80-125 ohms	–
2	≤ 2.5 Gbps	Default	EQ2	Long	80-125 ohms	–
2A	≤ 2.5 Gbps	Default	None	Standard	80-125 ohms	
3	≤ 3.5 Gbps	Half Swing	EQ1	Short	80-125 ohms	–
4	≤ 2.0 Gbps	Half Swing	EQ1	Standard	80-125 ohms	–
5	≤ 1.0 Gbps	Half Swing	EQ1	Long	80-125 ohms	–
6	≤ 1.5 Gbps	Half Swing	EQ1	Short/Standard	Unterminated	–
7	≤ 1.0 Gbps	Half Swing	EQ1	Long	Unterminated	–
8	≤ 1.5 Gbps	Half Swing	None	Short	Unterminated	–
9	≤ 1.0 Gbps	Half Swing	None	Standard	Unterminated	–
10	≤ 0.75 Gbps	Half Swing	None	Long	Unterminated	–

Note:

1. See **Annex *A.12*** *for guidance on 6.5 Gbps data rate.*

11 Regulatory Requirements

All MIPI D-PHY based devices should be designed to meet the applicable regulatory requirements.

12 Built-In HS Test Mode (Informative)

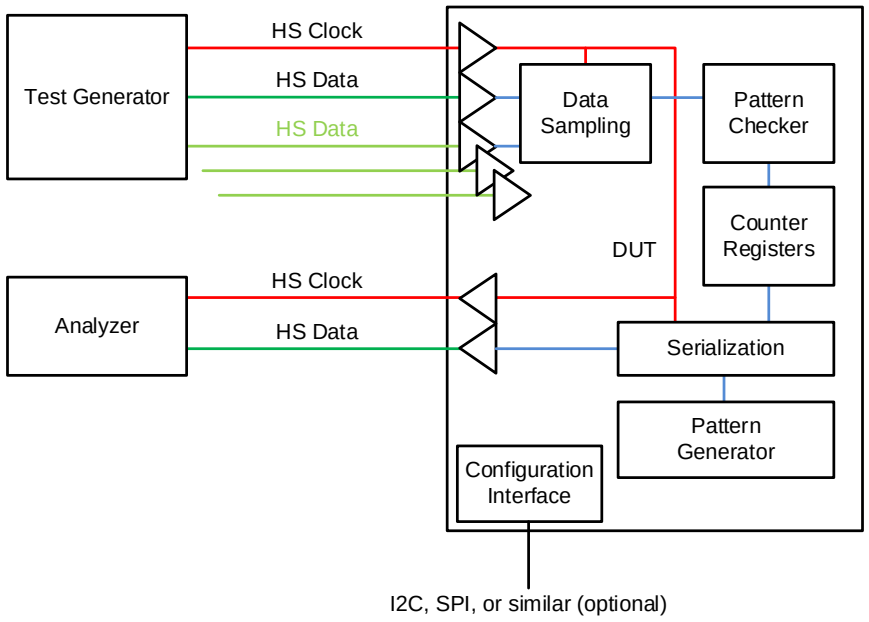


Figure 71 Testing with Pattern Checkers and Generators

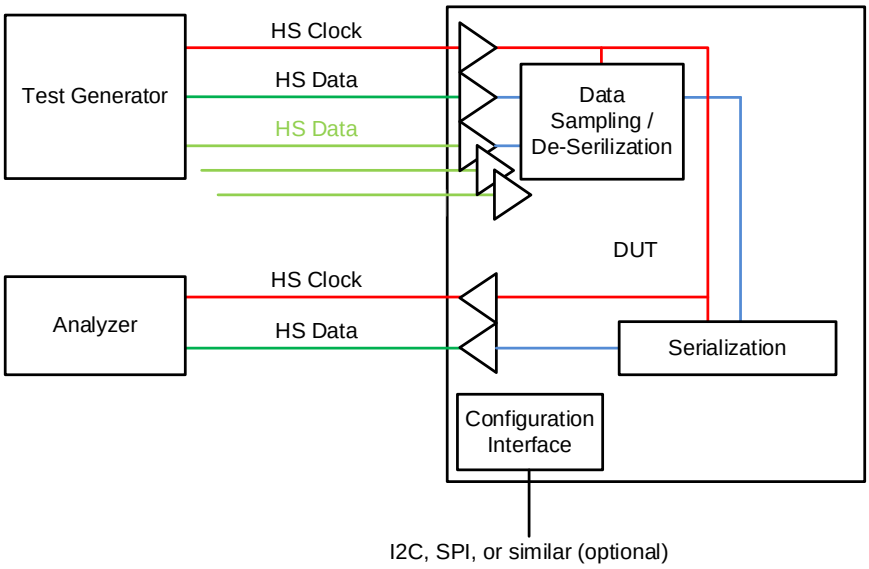


Figure 72 Alternative Testing with Loopback Mode

12.1 Introduction

The standardized built-in test mode simplifies testing of the PHY layer of an Rx and a Tx. It may also be used for production testing, verification, interoperability testing, and self-testing. It requires a minimum set of registers to contain error and bit counters (see ***Figure 71***), or alternatively support loopback testing (see ***Figure 72***). The test mode is a PHY layer mode. As a result, use of the test mode should not require any protocol layers. It focuses on HS testing, because the LP operation and LP to HS transition was not modified by D-PHY Specification revisions above v1.0, and therefore can be tested as they were tested before. This new mode will simplify the HS testing, and allows using the same or even less complicated / expensive equipment for testing new features such as SSC, Jitter, and equalization.

The HS test mode allows testing the tolerance of:

- Jitter
- SSC parameters
- Equalization parameters
- HS amplitude and offset
- Clock to Data timing
- Intra-lane timing, if the device allows multi-lane testing
- Cross talk, if the device allows multi-lane testing

It does not allow testing of:

- LP mode timing and level
- LP-HS timings
- ULPS mode timings and levels
- Protocol specific parameters

12.2 Entering the HS Test Mode

Since the protocol should not be involved in entering the HS test mode, a simple pattern or sequence of LP states is defined to enter the test mode.

The LP Trigger Escape Entry Code sequence from ***Table 8*** (0b01011101) should be used to enter the test mode. If the device allows configuration via an external interface, then the test mode may also be activated by a configuration sequence via the external interface. In this case the vendor should publish the sequence required to activate the test mode.

In HS test mode the Rx of the device should expect HS data. If comparators and (bit- and error-) counters to determine BER are built in, then these registers should be reset and the device should do the Clock-Data alignment as soon as it detects the alignment pattern a HS clock/2 pattern on all tested lanes. For a multi-lane device this feature can be used to determine which lane(s) is/are tested. The Tx side should do the same as the test generator. It should send the initializing sequence for the HS test mode followed by the alignment pattern.

12.3 HS Test Mode

After the alignment pattern the test generator should send a sync word on all tested data lanes (0b00011101) to allow the device to do the symbol synchronization. On the clock lane the clock pattern should be sent continuously. The test pattern is vendor specific and can be one or more of the following

- PRBS (PRBS 9 is preferred, Degree: $x^0+x^5+x^9$) See Errata 01 Item 5
- The compliance pattern (see CTS for definition)
- An application specific pattern.

The PRBS9 is the preferred pattern. If the device supports this then for interoperability can be ensured. The definition of the pattern checkers follows the description of Section 12 of the C-PHY Specification ***[MIPI02]***. For a clarification of the implementation, the following pattern should be expected [15:0] with a 16 bit seed register initialized 0x00FF: See Errata 01 Item 6

`0x00FF, 0x83DF, 0x1732,...`, or binary (LSB first):

```
0b1111111100000000111110111100000101001100111010000111001010010000111001111
0010110101000110110011011000111000100100100011101010110000001000100011000110
0010000100101010100111001000101111011000001010100010011101111100101101010000 1
0010010011011111001001111111011000011001100101001010011000110001111110100 1011
0011100011010001011110011010011010010111011111000110110110101100001011010000
0110110010101010111110111010100101000000001110111010010100101110011100010101
1101011110110011000010010010110111101000011011100001011001
```

See Errata 01 Item 7

If a vendor specific pattern is used, then the device vendor should supply the specification of the test pattern. Comparable results will be obtained in case that this pattern is balanced and the transition density is close to the value for a PRBS9 or the compliance pattern. See Errata 01 Item 8

In case of internal pattern checkers, it is possible for the test generator and the pattern checkers to lose synchronization. In this case the BER will never get back to 0 again, even if the data are recognized properly again. In this case there are two possibilities: See Errata 01 Item 9

- One can be that the pattern checkers do a re-initialization with the default seed and wait for the seed pattern in case of a PRBS as test pattern, or wait for the first word(s) in the test pattern. In this case, the first word(s) should be somehow unique. The detection of a lost synchronization may be done internally, if too many errors occur (threshold vendor specific).
- The second possibility to re-initialize a synchronization loss may be to interrupt the clock. In this case, the re-initialization can be triggered from external by stopping the clock. The device should not exit from HS Test Mode. The de-serialization may be restarted by a sync word followed by the test pattern. An interruption of the clock should reset the PRBS generators, and the device should wait again for the sync pattern. The interruption detection time should set equal to the $T_{Clk\text{-}Miss}$ time (see ***Table 14***).

In case of using loopback (see ***Figure 72***) for test mode, the test pattern should be send back via one or more Tx lanes (defined by the vendor). The loopback data signal should be retimed with the received clock. By this filtering, any jitter on data will be removed, while the clock received by the Rx should be routed through without any retiming.

Note: For PHY interoperability (without testing equipment), it is required that at least one device have integrated pattern generators and checkers (see ***Figure 71***), and that both devices support the same test pattern. In this case, implementing the pattern-generators-and-checker method is recommended as this gives more flexibility then the loopback mode.

The equalization setting should be kept constant since the last HS setting before activating the test mode. Tx testing can be done by using a test generator applying the necessary pattern for Tx testing (see CTS). Triggering the Tx HS test pattern generation requires activating the test mode via an external interface. If the test mode was triggered by a test generator via the Rx side of the device, then the Tx needs to send the -same data as received by Rx (loopback) or the counter values (error checkers).

In case of using pattern checkers and counter register, the vendor should specify how to access these registers. Access to these counters can be implemented either via an external interface such as I2C or SPI, or else the device should send the counter values via its one D-PHY Tx lane. The counters should have enough depth to allow at least 20 seconds of operation without overrun. In case of overflow the counters should start over with 0. The bit/frame counter register can contain a bit counter or a frame counter, in which the vendor needs to specify the factor between counter value and number of received bits. The error counter always should contain the number of errors. To support Tx testing of devices that support the test mode via pattern checkers, the Tx lanes can send the bit/error counters as continuous data stream; or, if the values of the counters are not sent via the link, it can automatically send a test pattern specified by the device vendor.

12.4 Special Case: Multi-Lane Testing

If the device allows using PRBS as test pattern on more than one lane, each lane should use a different seed. Lane 0 should use 0xFF, lane 1 should use 0xFE, and so on, to have different data crossing the link on each lane. This allows cross talk to be tested. If an application-specific pattern is used, these patterns should also be constructed such that they are different from lane to lane. The exact definition of application-specific test patterns is left to the device vendor, and must be documented by the device vendor.

12.5 Exiting from HS Test Mode

After entering the test mode, the device should remain in test mode until directed to leave test mode, for example by an LP11 state applied for at least 500 ms, or by the device being power cycled.

If it is possible to configure the test mode via an external interface, then the same interface can also be used to exit the test mode. In this case, the device vendor must document the exit sequence.

Annex A Logical PHY-Protocol Interface Description (informative)

The PHY Protocol Interface (PPI) is used to make a connection between the PHY Lane Modules and the higher protocol layers of a communication stack. The interface described here is intended to be generic and application independent.

This annex is informative only. Conformance to the D-PHY specification does not depend on any portion of the PPI defined herein. Because of that, this annex avoids normative language and does not use words like “shall” and “should.” Instead, present tense language has been used to describe the PPI, utilizing words like “is” and “does.” The reader may find it helpful to consider this annex to be a description of an example implementation, rather than a specification. The signaling interface described in this annex, The PHY Protocol Interface (PPI) is optional. However, if a module includes the PPI Interface, it shall implement it as described in this annex.

This PPI is optimized for controlling a D-PHY and transmitting and receiving parallel data. The interface described here is defined as an on-chip connection, and does not attempt to minimize signal count or define timing parameters or voltage levels for the PPI signals.

A.1 Signal Description

Table 43 defines the signals used in the PPI. For a PHY with multiple Data Lanes, a set of PPI signals is used for each Lane. Each signal has been assigned into one of six categories: High-Speed transmit signals, High-Speed receive signals, Escape mode transmit signals, Escape mode receive signals, control signals, and error signals. Bi-directional High-Speed Data Lanes with support for bi-directional Escape mode include nearly all of the signals listed in the table. Unidirectional Lanes or Clock Lanes include only a subset of the signals. The direction of each signal is listed as “I” or “O”. Signals with the direction “I” are PHY inputs, driven from the Protocol. Signals with the direction “O” are PHY outputs, driven to the Protocol. For this logical interface, most clocks are described as being generated outside the PHY, although any specific PHY may implement the clock circuit differently.

The “Categories” column in ***Table 43*** indicates for which Lane Module types each signal applies. The category names are described in ***Table 1*** and are summarized here for convenience. Each category is described using a four-letter acronym, defined as <Side, HS-capabilities, Escape-Forward, Escape-Reverse>. The first letter, Side, can be M (Master) or S (Slave). The second letter, High-Speed capabilities, can be F (Forward data), R (Reverse and Forward data), or C (Clock). The third and fourth letters indicate Escape mode capability in the Forward and Reverse directions, respectively. For Data Lanes, the third letter can be A (All) or E (Events – Triggers and ULPS only), while the fourth letter can be A (All, including LPDT), E (Events, triggers and ULPS only), Y (Any but not None: so A or E) or N (None). For a Data Lane, any of the four identification letters can be replaced by an X, to indicate that each of the available options is appropriate. For a Clock Lane, only the first letter can be X, while the other three letters are always CNN.

The signal description includes options for the designer to choose a data path width to simplify the task of timing closure between the D-PHY and high-level protocol logic.

The protocol and D-PHY will select data path widths as described in ***Table 43*** that are most appropriate for the operation. The bus width selection is based on logical binary input as explained in TxDataWidthHS[1:0] and RxDataWidthHS[1:0]. Bus width can be modified based on operational requirements after the completion of the current burst. It is not necessary for the PPI data path width of the transmit function in one IC to match the PPI data path width of the receive function in another IC. The D-PHY has the ability to transmit and receive any integer number of words greater than zero, regardless of the width of the PPI Tx and Rx data paths. A set of data-valid signals accompany each set of data transferred over the PPI to indicate which words contain valid data to transmit or which words contain data that was actually received from the channel.

All timing diagrams in this section refer to a one-byte bus-width case.

1480 **Table 43 PPI Signals**

Symbol	Dir	Categories	Description
High-Speed Transmit Signals			
TxDDRClkHS-I	I	MXXX MCNN	Data Lane High-Speed Transmit DDR Clock. This signal is used to transmit High-Speed data bits over the Lane Interconnect. All Data Lanes use the same TxDDRClkHS-I (in-phase) clock signal.
TxDDRClkHS-Q	I	MCNN	Clock Lane High-Speed Transmit DDR Clock. This signal is used to generate the High-Speed clock signal for the Lane Interconnect. The TxDDRClkHS-Q (quadrature) clock signal is phase shifted from the TxDDRClkHS-I clock signal.
TxWordClkHS	O	MXXX SRXX	High-Speed Transmit Word Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that all transmitting lane modules share one TxWordClkHS signal. The frequency of TxWordClkHS is dependent upon the width of the High-Speed Transmit Data, as follows: • 8-bit width, TxDataHS[7:0], the High-Speed Transmit Word Clock is exactly 1/8 the high-speed data rate. • 16-bit width, TxDataHS[15:0], the High-Speed Transmit Word Clock is exactly 1/16 the high-speed data rate. • 32-bit width, TxDataHS[31:0], the High-Speed Transmit data Clock is exactly 1/32 the high-speed data rate.
TxDataWidthHS[1:0]	I	MXXX SRXX	High-Speed Transmit Data bus Width Select. Selects the bus width of TxDataHS: • TxDataWidthHS[1:0] = 00: 8-bit, TxDataHS[7:0]. • TxDataWidthHS[1:0] = 01: 16-bit, TxDataHS[15:0] • TxDataWidthHS[1:0] = 10: 32-bit, TxDataHS[31:0] • TxDataWidthHS[1:0] = 11: not used, reserved. An implementation may support any data width - one fixed width, or subset of widths or all widths defined above.
TxDataHS[7:0], or TxDataHS[15:0], or TxDataHS[31:0]	I	MXXX SRXX	High-Speed Transmit Data bus width. High-speed data to be transmitted. If the TxWordValidHS signals indicate that more than 8 bits are to be transmitted, then the byte transmission order over the physical interface is TxDataHS[7:0] followed by TxDataHS[15:8] followed by TxDataHS[23:16] followed by TxDataHS[31:24]. Data is captured on rising edges of TxWordClkHS. The following signals are defined for the High-Speed Transmit Data bus based on the width of the transmit data path: • 8-bit width – TxDataHS[7:0] • 16-bit width – TxDataHS[15:0] • 32-bit width – TxDataHS[31:0] An implementation may support any data width - one fixed width, or subset of widths or all widths defined above. The LSB will be transmitted as the first bit and the MSB will be transmitted as the last bit.

Symbol	Dir	Categories	Description
TxWordValidHS[0], or TxWordValidHS[1:0],or TxWordValidHS[3:0]	I	MXXX SRXX	High-Speed Transmit Word Data Valid. When the High-Speed Transmit Data width is greater than 8 bits it is necessary to indicate which 8-bit segments contain valid transmit data to be able to transmit any number of words. The following Transmit Sync Word signals are defined based on the width of the transmit data path: • 8-bit width – TxWordValidHS[0] • 16-bit width – TxWordValidHS[1:0] • 32-bit width – TxWordValidHS[3:0] The following Transmit Word Data Valid signals indicate which bits of the TxDataHS data bus contain valid data to transmit as follows: • TxWordValidHS[0] – TxDataHS[7:0] contains valid data to be transmitted • TxWordValidHS[1] – TxDataHS[15:8] contains valid data to be transmitted • TxWordValidHS[2] – TxDataHS[23:16] contains valid data to be transmitted • TxWordValidHS[3] – TxDataHS[31:24] contains valid data to be transmitted.
TxEqActiveHS	I	MXXX	This is a level sensitive flag indicating the equalization active state. When this flag is high, it indicates the equalization is enabled. When this flag is low, it indicates the equalization is disabled.
TxEqLevelHS	I	MXXX	This is a level sensitive flag indicating the equalization level. When this flag is low (i.e., zero), it indicates a low level of equalization (3.5 dB +/- 1 dB) is active. When this flag is high (i.e., one), it indicates a high level of equalization (7 dB +/- 1 dB) is active.
TxRequestHS	I	MXXX SRXX MCNN	High-Speed Transmit Request and Data Valid. A low-to-high transition on TxRequestHS causes the Lane Module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the Lane Module to initiate an End-of-Transmission sequence. For Clock Lanes, this active high signal causes the Lane Module to begin transmitting a High-Speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on TxDataHS to be transmitted. The Lane Module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low.
TxReadyHS	O	MXXX SRXX	High-Speed Transmit Ready. This active high signal indicates that TxDataHS is accepted by the Lane Module to be serially transmitted. TxReadyHS is valid on rising edges of TxWordClkHS. Optionally, TxReadyHS can be used during deskew calibration to indicate that SoT has ended and data lanes are transmitting deskew burst (clock pattern).

Symbol	Dir	Categories	Description
TxSkewCalHS	I	MXXX	High-Speed Transmit Skew Calibration. This is an optional pin to initiate the periodic deskew burst at the transmitter. A low-to-high transition on TxSkewCalHS causes the PHY to initiate a deskew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop deskew pattern transmission and initiate an end-of-transmission sequence.
High-Speed Receive Signals			
RxWordClkHS	O	MRXX SXXX	High-Speed Receive Word Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock. The frequency of RxWordClkHS is dependent upon the width of the High-Speed Receive Data, as follows: • 8-bit width, RxDataHS[7:0], the High-Speed Receive Word Clock is exactly 1/8 the high-speed received data rate. • 16-bit width, RxDataHS[15:0], the High-Speed Receive Word Clock is exactly 1/16 the high-speed received data rate. • 32-bit width, RxDataHS[31:0], the High-Speed Receive Word Clock is exactly 1/32 the high-speed received data rate.
RxDataWidthHS[1:0]	I	MRXX SXXX	High-Speed Receive Data Width Select. Selects the bus width of RxDataHS: • RxDataWidthHS[1:0] = 00: 8-bit, RxDataHS[7:0] • RxDataWidthHS[1:0] = 01: 16-bit, RxDataHS[15:0] • RxDataWidthHS[1:0] = 10: 32-bit, RxDataHS[31:0] • RxDataWidthHS[1:0] = 11: not used, reserved. An implementation may support any data width - one fixed width, or subset of widths or all widths defined above.
RxDataHS[7:0], or RxDataHS[15:0], or RxDataHS[31:0]	O	MRXX SXXX	High-Speed Receive Data. High-speed data received by the lane module. If the RxValidHS signals indicate that more than 8 bits were received, then the byte reception order over the physical interface is RxDataHS[7:0] followed by RxDataHS[15:8] followed by RxDataHS[23:16] followed by RxDataHS[31:24]. Data is transferred on rising edges of RxWordClkHS. The following signals are defined for the High-Speed Receive Data based on the width of the receive data path: • 8-bit width – RxDataHS[7:0] • 16-bit width – RxDataHS[15:0] • 32-bit width – RxDataHS[31:0] An implementation may support any data width - one fixed width, or subset of widths or all widths defined above. The LSB will be received as the first bit and the MSB will be received as the last bit.

Symbol	Dir	Categories	Description
RxValidHS[0], or RxValidHS[1:0], or RxValidHS[3:0]	O	MRXX SXXX	High-Speed Receive Data Valid. This active high signal indicates that the lane module is driving data to the protocol layer on the RxDataHS output. There is no “RxReadyHS” signal, and the protocol layer is expected to capture RxDataHS on every rising edge of RxWordClkHS where any RxValidHS bit is asserted. There is no provision for the protocol layer to slow down (“throttle”) the receive data. The following High-Speed Receive Data Valid signals are defined based on the width of the receive data path: • 8-bit width – RxValidHS[0] • 16-bit width – RxValidHS[1:0] • 32-bit width – RxValidHS[3:0] The following High-Speed Receive Data Valid signals indicate which bits of the RxDataHS data bus contain valid data as follows: • RxValidHS[0] – RxDataHS[7:0] contains valid data that was received from the channel • RxValidHS[1] – RxDataHS[15:8] contains valid data that was received from the channel • RxValidHS[2] – RxDataHS[23:16] contains valid data that was received from the channel • RxValidHS[3] – RxDataHS[31:24] contains valid data that was received from the channel.
RxActiveHS	O	MRXX SXXX	High-Speed Reception Active. This active high signal indicates that the Lane Module is actively receiving a High-Speed transmission from the Lane interconnect.
RxSyncHS	O	MRXX SXXX	Receiver Synchronization Observed. This active high signal indicates that the Lane Module has seen an appropriate synchronization event. In a typical High-Speed transmission, RxSyncHS is high for one cycle of RxWordClkHS at the beginning of a High-Speed transmission when RxActiveHS is first asserted.
RxClkActiveHS	O	SCNN	Receiver Clock Active. This asynchronous, active high signal indicates that a Clock Lane is receiving a DDR clock signal.
RxDDRClkHS	O	SCNN	Receiver DDR Clock. This is the received DDR clock – it may be used by the protocol if required. This signal is low whenever RxClkActiveHS is low.
RxSkewCalHS	O	SXXX	High-Speed Receive Skew Calibration. This optional active high signal indicates that the high speed deskew burst is being received. RxSkewCalHS is set to the active state when the all-ones sync pattern is received, and is cleared to the inactive state when Dp and Dn transition back to the LP-11 Stop State.

Symbol	Dir	Categories	Description
Escape Mode Transmit Signals			
TxClkEsc	I	MXXX SXXY	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the phase times for Low-Power signals as defined in ***Section 6.6.2***. It is therefore constrained by the normative part of the D-PHY specification. See ***Section 9***. Note that this clock is used to synchronize TurnRequest and is included for any module that supports bi-directional High-Speed operation, even if that module does not support transmit or bi-directional escape mode.
TxRequestEsc	I	MXXX SXXY	Escape mode Transmit Request. This active high signal, asserted together with exactly one of TxLpdtEsc, TxUlpsEsc, or one bit of TxTriggerEsc, is used to request entry into escape mode. Once in escape mode, the Lane stays in escape mode until TxRequestEsc is de-asserted. TxRequestEsc is only asserted by the protocol while TxRequestHS is low.
TxLpdtEsc	I	MXAX SXXA	Escape mode Transmit Low-Power Data. This active high signal is asserted with TxRequestEsc to cause the Lane Module to enter Low-Power data transmission mode. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxUlpsEsc and all bits of TxTriggerEsc are low when TxLpdtEsc is asserted.
TxUlpsExit	I	MXXX SXXY MCNN	Transmit ULP Exit Sequence. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark-1 after TxUlpsExit is asserted. The PHY later drives the Stop state (LP-11) when TxRequestEsc is deasserted. TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.
TxUlpsEsc	I	MXXX SXXY	Escape mode Transmit Ultra-Low Power State. This active high signal is asserted with TxRequestEsc to cause the Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpsEsc is asserted.

Symbol	Dir	Categories	Description
TxTriggerEsc[3:0]	I	MXXX SXXY	Escape mode Transmit Trigger 0-3. One of these active high signals is asserted with TxRequestEsc to cause the associated Trigger to be sent across the Lane interconnect. In the receiving Lane Module, the same bit of RxTriggerEsc is then asserted and remains asserted until the Lane interconnect returns to Stop state, which happens when TxRequestEsc is de-asserted at the transmitter. Only one bit of TxTriggerEsc is asserted at any given time, and only when TxLpdtEsc and TxUlpsEsc are both low. TxTriggerEsc[0] corresponds to Reset-Trigger. TxTriggerEsc[1] corresponds to Entry sequence for HS Test Mode Trigger. TxTriggerEsc[2] corresponds to Unknown-4 Trigger. TxTriggerEsc[3] corresponds to Unknown-5 Trigger.
TxDataEsc[7:0]	I	MXAX SXXA	Escape mode Transmit Data. This is the eight bit escape mode data to be transmitted in Low-Power data transmission mode. The signal connected to TxDataEsc[0] is transmitted first. Data is captured on rising edges of TxClkEsc.
TxValidEsc	I	MXAX SXXA	Escape mode Transmit Data Valid. This active high signal indicates that the protocol is driving valid data on TxDataEsc to be transmitted. The Lane Module accepts the data when TxRequestEsc, TxValidEsc and TxReadyEsc are all active on the same rising TxClkEsc clock edge.
TxReadyEsc	O	MXAX SXXA	Escape mode Transmit Ready. This active high signal indicates that TxDataEsc is accepted by the Lane Module to be serially transmitted. TxReadyEsc is valid on rising edges of TxClkEsc.
Escape Mode Receive Signals			
RxClkEsc	O	MXXY SXXX	Escape mode Receive Clock. This signal is used to transfer received data to the protocol during escape mode. This “clock” is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this “clock” may not be periodic.
RxLpdtEsc	O	MXXA SXAX	Escape Low-Power Data Receive mode. This active high signal is asserted to indicate that the Lane Module is in Low-Power data receive mode. While in this mode, received data bytes are driven onto the RxDataEsc output when RxValidEsc is active. The Lane Module remains in this mode with RxLpdtEsc asserted until a Stop state is detected on the Lane interconnect.
RxUlpsEsc	O	MXXY SXXX	Escape Ultra-Low Power (Receive) mode. This active high signal is asserted to indicate that the Lane Module has entered the Ultra-Low Power State. The Lane Module remains in this mode with RxUlpsEsc asserted until a Stop state is detected on the Lane interconnect.

Symbol	Dir	Categories	Description
RxTriggerEsc[3:0]	O	MXXY SXXX	Escape mode Receive Trigger 0-3. These active high signals indicate that a trigger event has been received. The asserted RxTriggerEsc signal remains active until a Stop state is detected on the Lane interconnect. RxTriggerEsc[0] corresponds to Reset-Trigger. RxTriggerEsc[1] corresponds to Entry sequence for HS Test Mode Trigger. RxTriggerEsc[2] corresponds to Unknown-4 Trigger. RxTriggerEsc[3] corresponds to Unknown-5 Trigger.
RxDataEsc[7:0]	O	MXXA SXAX	Escape mode Receive Data. This is the eight-bit escape mode Low-Power data received by the Lane Module. The signal connected to RxDataEsc[0] was received first. Data is transferred on rising edges of RxClkEsc.
RxValidEsc	O	MXXA SXAX	Escape mode Receive Data Valid. This active high signal indicates that the Lane Module is driving valid data to the protocol on the RxDataEsc output. There is no “RxReadyEsc” signal, and the protocol is expected to capture RxDataEsc on every rising edge of RxClkEsc where RxValidEsc is asserted. There is no provision for the protocol to slow down (“throttle”) the receive data.
Control Signals			
TurnRequest	I	XRXX XFXY	Turn Around Request. This active high signal is used to indicate that the protocol desires to turn the Lane around, allowing the other side to begin transmission. TurnRequest is valid on rising edges of TxClkEsc. TurnRequest is only meaningful for a Lane Module that is currently the transmitter (Direction=0). If the Lane Module is in receive mode (Direction=1), this signal is ignored.
Direction	O	XRXX XFXY	Transmit/Receive Direction. This signal is used to indicate the current direction of the Lane interconnect. When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input).
TurnDisable	I	XRXX XFXY	Disable Turn-around. This signal is used to prevent a (bi-directional) Lane from going into transmit mode – even if it observes a turn-around request on the Lane interconnect. This is useful to prevent a potential “lock-up” situation when a unidirectional Lane Module is connected to a bi-directional Lane Module.
ForceRxmode	I	MRXX MXXY SXXX	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the Lane Module immediately transitions into receive control mode and waits for a Stop state to appear on the Lane interconnect. When used for initialization, this signal should be released, i.e. driven low, only when the Dp & Dn inputs are in Stop state for a time T_{INIT}, or longer.

Symbol	Dir	Categories	Description
ForceTxStopmode	I	MXXX SRXX SXXY	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state.
Stopstate	O	XXXX XCNN	Lane is in Stop state. This active high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface. Also, the protocol may use this signal to indirectly determine if the PHY line levels are in the LP-11 state.
Enable	I	XXXX XCNN	Enable Lane Module. This active high signal forces the Lane Module out of “shutdown”. All line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.
TxUlpsClk	I	MCNN	Transmit Ultra-Low Power State on Clock Lane. This active high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpsClk is de-asserted.
RxUlpsClkNot	O	SCNN	Receive Ultra-Low Power State on Clock Lane. This active low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State. The Lane Module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect.
UlpsActiveNot	O	XXXX XCNN	ULP State (not) Active. This active low signal is asserted to indicate that the Lane is in ULP state. For a transmitter, this signal is asserted some time after TxUlpsEsc and TxRequestEsc (TxUlpsClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TxRequestEsc (TxUlpsClk) inactive to return the Lane to Stop state. For a receiver, this signal indicates that the Lane is in ULP state. At the beginning of ULP state, UlpsActiveNot is asserted together with RxUlpsEsc, or RxUlpsClkNot for a Clock Lane. At the end of the ULP state, this signal becomes inactive to indicate that the Mark-1 state has been observed. Later, after a period of time Twakeup, the RxUlpsEsc (or RxUlpsClkNot) signal is deasserted.

Symbol	Dir	Categories	Description
TxHSIdleClkHS	I	MXXX	HS-Idle State Start. This is an optional signal to initiate the HS-Idle State at the transmitter. A high level on TxHSIdleClkHS directs the PHY to start HS-Idle-Post sub-state when payload transmission on all Date Lanes is completed. A low level on TxHSIdleClkHS directs the PHY to start HS clock and to exit HS-Idle-ClkHS0 sub-state.
TxHSIdleClkReadyHS	O	MXXX	Clock Ready to Exit HS-Idle-ClkHS0 Sub-State. This optional active high signal indicates that the transmitter is ready to exit HS-Idle-ClkHS0 sub-state. A low level on TxHSIdleClkReadyHS indicates that the transmitter is not in HS-Idle State, or not ready to exit HS-Idle-ClkHS0 sub-state. A high level on TxHSIdleClkReadyHS indicates that the transmitter is ready to exit HS-Idle-ClkHS0 sub-state.
Error Signals			
ErrSotHS	O	MRXX SXXX	Start-of-Transmission (SoT) Error. If the High-Speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this active high signal is asserted for one cycle of RxWordClkHS. This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced.
ErrSotSyncHS	O	MRXX SXXX	Start-of-Transmission Synchronization Error. If the High-Speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this active high signal is asserted for one cycle of RxWordClkHS.
ErrEsc	O	MXXY SXXX	Escape Entry Error. If an unrecognized escape entry command is received, this active high signal is asserted and remains asserted until the next change in line state.
ErrSyncEsc	O	MXXA SXAX	Low-Power Data Transmission Synchronization Error. If the number of bits received during a Low-Power data transmission is not a multiple of eight when the transmission ends, this active high signal is asserted and remains asserted until the next change in line state.
ErrControl	O	MXXY SXXX	Control Error. This active high signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains asserted until the next change in line state.
ErrContentionLP0	O	MXXX SXXY	LP0 Contention Error. This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low.
ErrContentionLP1	O	MXXX SXXY	LP1 Contention Error. This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line high.

Table 44 summarizes the signals that are affected by the choice of the transmit data path width.

Table 44 Tx HS PPI Signals, Impact of Data Path Width

	8-bit	16-bit	32-bit
Tx HS Word Clock Rate	1/8 the HS bit rate	1/16 the HS bit rate	1/32 the HS bit rate
Tx HS Data Path	TxDataHS[7:0]	TxDataHS[15:0]	TxDataHS[31:0]
HS Transmit Word Valid	TxWordValidHS[0] → TxDataHS[7:0]	TxWordValidHS[0] → TxDataHS[7:0]; TxWordValidHS[1] → TxDataHS[15:8]	TxWordValidHS[0] → TxDataHS[7:0]; TxWordValidHS[1] → TxDataHS[15:8]; TxWordValidHS[2] → TxDataHS[23:16]; TxWordValidHS[3] → TxDataHS[31:24]

1482 ***Table 45*** summarizes the signals that are affected by the choice of the transmit data path width.

Table 45 Rx HS PPI Signals, Impact of Data Path Width

	8-bit	16-bit	32-bit
Rx HS Word Clock Rate	1/8 the HS bit rate	1/16 the HS bit rate	1/32 the HS bit rate
Rx HS Data Path	RxDataHS[7:0]	RxDataHS[15:0]	RxDataHS[31:0]
HS Receive Word Valid	RxValidHS[0] → RxDataHS[7:0]	RxValidHS[0] → RxDataHS[7:0]; RxValidHS[1] → RxDataHS[15:8]	RxValidHS[0] → RxDataHS[7:0]; RxValidHS[1] → RxDataHS[15:8]; RxValidHS[2] → RxDataHS[23:16]; RxValidHS[3] → RxDataHS[31:24]

A.2 High-Speed Transmit from the Master Side

Figure 73 shows an example of a High-Speed transmission on the Master side. While TxRequestHS is low, the Lane Module ignores the value of TxDataHS. To begin transmission, the protocol drives TxDataHS with the first byte of data and asserts TxRequestHS. This data byte is accepted by the PHY on the first rising edge of TxWordClkHS with TxReadyHS also asserted. At this point, the protocol logic drives the next data byte onto TxDataHS. After every rising clock cycle with TxReadyHS active, the protocol supplies a new valid data byte or ends the transmission. After the last data byte has been transferred to the Lane Module, TxRequestHS is driven low to cause the Lane Module to stop the transmission and enter Stop state. The minimum number of bytes transmitted could be as small as one.

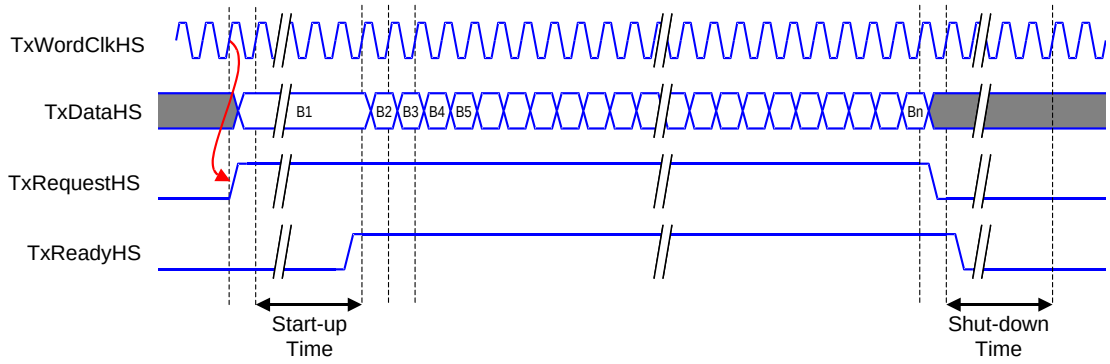


Figure 73 Example High-Speed Transmission from the Master Side (One-Byte Bus Width)

A.3 High-Speed Receive at the Slave Side

Figure 74 shows an example of a High-Speed reception at the Slave side. The RxActiveHS signal indicates that a receive operation is occurring. A normal reception starts with a pulse on RxSyncHS followed by valid receive data on subsequent cycles of RxWordClkHS. Note that the protocol is prepared to receive all of the data. There is no method for the receiving protocol to pause or slow data reception.

If EoT Processing is performed inside the PHY, the RxActiveHS and RxValidHS signals transition low following the last valid data byte, Bn. See ***Figure 74***.

If EoT processing is not performed in the PHY, one or more additional bytes are presented after the last valid data byte. The first of these additional bytes, shown as byte “C” in ***Figure 74***, is all ones or all zeros. Subsequent bytes may or may not be present, and can have any value. For a PHY that does not perform EoT processing, the RxActiveHS and RxValidHS signals transition low simultaneously some time after byte “C” is received. Once these signals have transitioned low, they remain low until the next High-Speed data reception begins.

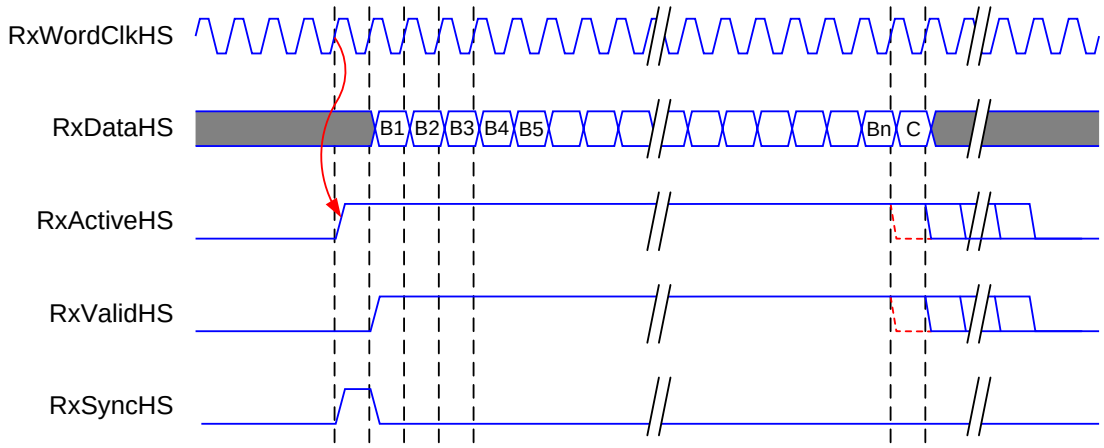


Figure 74 Example High-Speed Receive at the Slave Side (One-Byte Bus Width)

A.4 High-Speed Transmit from the Slave Side

A Slave can only transmit at one-fourth the bandwidth of a Master. Because of this, the TxReadyHS signal is not constant high for a transmitting slave. Otherwise, the transmission is very much like that seen at the PPI interface of a transmitting Master-side Lane Module. ***Figure 75*** shows an example of transmitting from the Slave side.

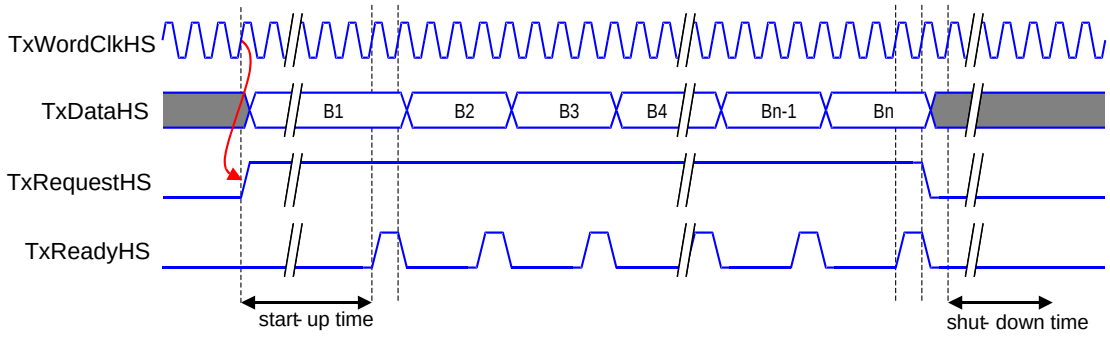


Figure 75 Example High-Speed Transmit from the Slave Side (One-Byte Bus Width)

A.5 High-Speed Receive at the Master Side

Because a Slave is restricted to transmitting at one-fourth the bandwidth of a Master, the RxValidHS signal is only asserted one out of every four cycles of RxWordClkHS during a High-Speed receive operation at the Master side. An example of this is shown in ***Figure 76***. Note that, depending on the bit rate, there may be one or more extra pulses on RxValidHS after the last valid byte, Bn, is received.

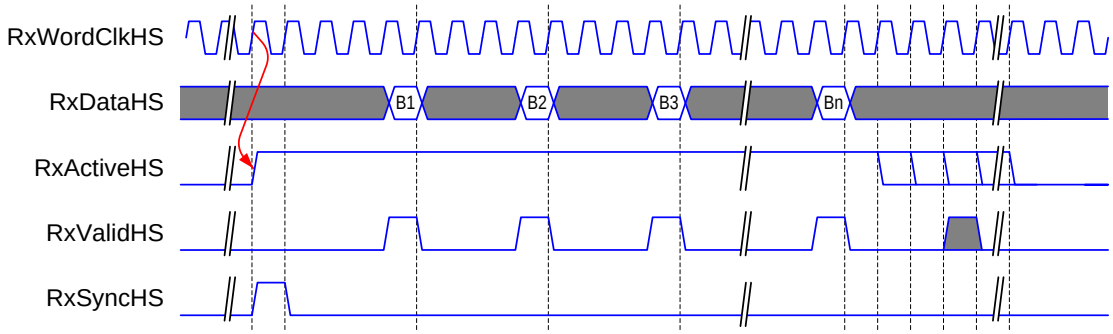


Figure 76 Example High-Speed Receive at the Master Side (One-Byte Bus Width)

A.6 Low-Power Data Transmission

For Low-Power data transmission the TxClkEsc is used instead of TxDDRClkHS-I/Q and TxWordClkHS. Furthermore, while the High-Speed interface signal TxRequestHS serves as both a transmit request and a data valid signal, on the Low-Power interface two separate signals are used. The Protocol directs the Data Lane to enter Low-Power data transmission Escape mode by asserting TxRequestEsc with TxLpdtEsc high. The Low-Power transmit data is transferred on the TxDataEsc lines when TxValidEsc and TxReadyEsc are both active at a rising edge of TxClkEsc. The byte is transmitted in the time after the TxDataEsc is accepted by the Lane Module (TxValidEsc = TxReadyEsc = high) and therefore the TxClkEsc continues running for some minimum time after the last byte is transmitted. The Protocol knows the byte transmission is finished when TxReadyEsc is asserted. After the last byte has been transmitted, the protocol de-asserts TxRequestEsc to end the Low-Power data transmission. This causes TxReadyEsc to return low, after which the TxClkEsc clock is no longer needed. Whenever TxRequestEsc transitions from high-to-low, it always remains in the low state for a minimum of two TxClkEsc clock cycles. ***Figure 77*** shows an example Low-Power data transmission operation.

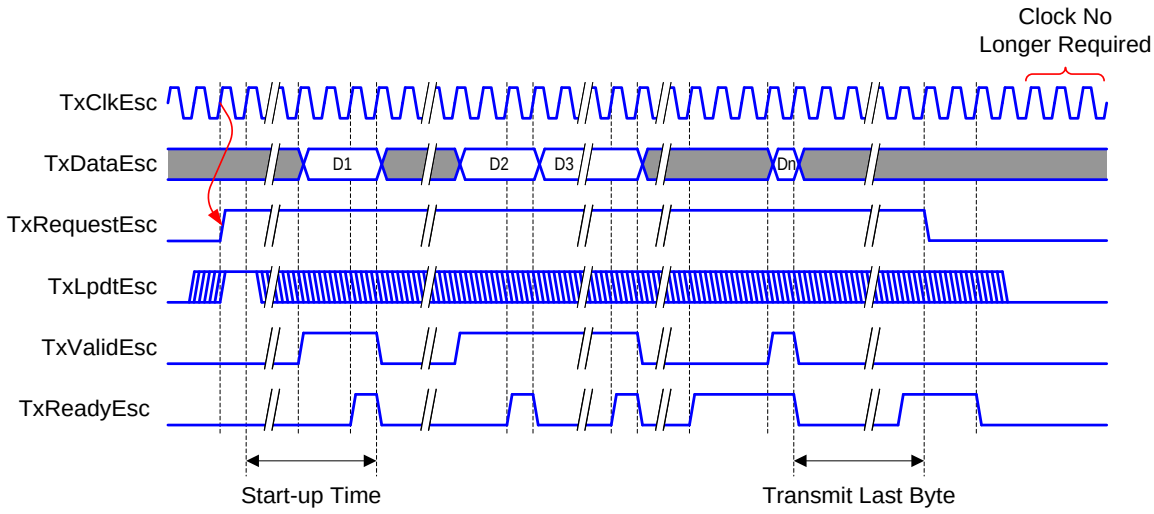


Figure 77 Low-Power Data Transmission

A.7 Low-Power Data Reception

Figure 78 shows an example Low-Power data reception. In this example, a Low-Power escape “clock” is generated from the Lane Interconnect by the logical exclusive-OR of the Dp and Dn lines. This “clock” is used within the Lane Module to capture the transmitted data. In this example, the “clock” is also used to generate RxClkEsc.

The signal RxLpdtEsc is asserted when the escape entry command is detected and stays high until the Lane returns to Stop state, indicating that the transmission has finished. It is important to note that because of the asynchronous nature of Escape mode transmission, the RxClkEsc signal can stop at anytime in either the high or low state. This is most likely to happen just after a byte has been received, but it could happen at other times as well.

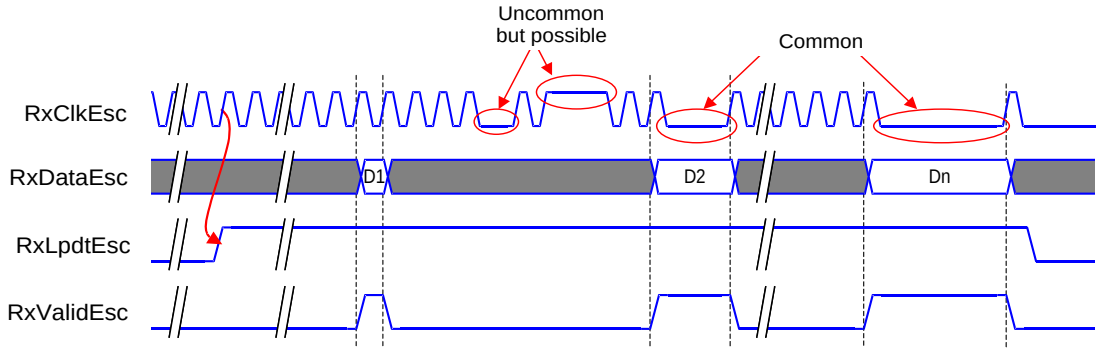


Figure 78 Example Low-Power Data Reception

A.8 Turn-around

If the Master side and Slave side Lane Modules are both bi-directional, it is possible to turn around the Link for High-Speed and/or Escape mode signaling. As explained in ***Section 6.5***, which side is allowed to transmit is determined by passing a “token” back and forth. That is, the side currently transmitting passes the token to the receiving side. If the receiving side acknowledges the turn-around request, as indicated by driving the appropriate line state, the direction is switched.

Figure 79 shows an example of two turn-around events. At the beginning, the local side is the transmitter, as shown by Direction=0. When the protocol on this side wishes to turn the Lane around (i.e. give the token to the other side), it asserts TurnRequest for at least one cycle of TxClkEsc. This initiates the turn-around procedure. The remote side acknowledges the turn-around request by driving the appropriate states on the Lines. When this happens, the local Direction signal changes from transmit (0) to receive (1).

Later in the example of ***Figure 79***, the remote side initiates a turn-around request, passing the token back to the local side. When this happens, the local Direction signal changes back to transmit (0). Note that there is no prescribed way for a receiver to request access to the Link. The current transmitter is in control of the Link direction and decides when to turn the Link around, passing control to the receiver.

If the remote side does not acknowledge the turn-around request, the Direction signal does not change.

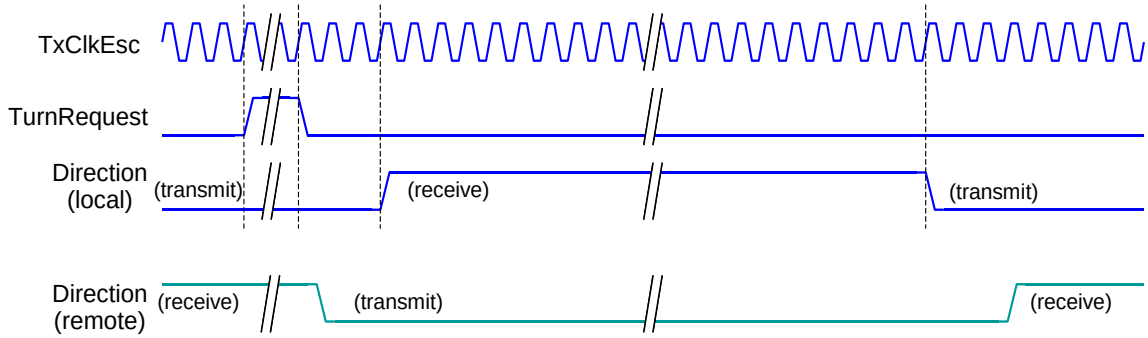


Figure 79 Example Turn-around Actions Transmit-to-Receive and Back to Transmit

A.9 Calibration

Initiation of periodic deskew calibration from the transmitter can be done using the TxSkewCalHS pin on the PPI interface. This is an optional signal pin, and periodic deskew is an optional feature. Receiver deskew can be by-passable using the receiver configuration control. ***Figure 80*** shows the PPI signal outputs as they operate during high-speed data transmission in normal mode.

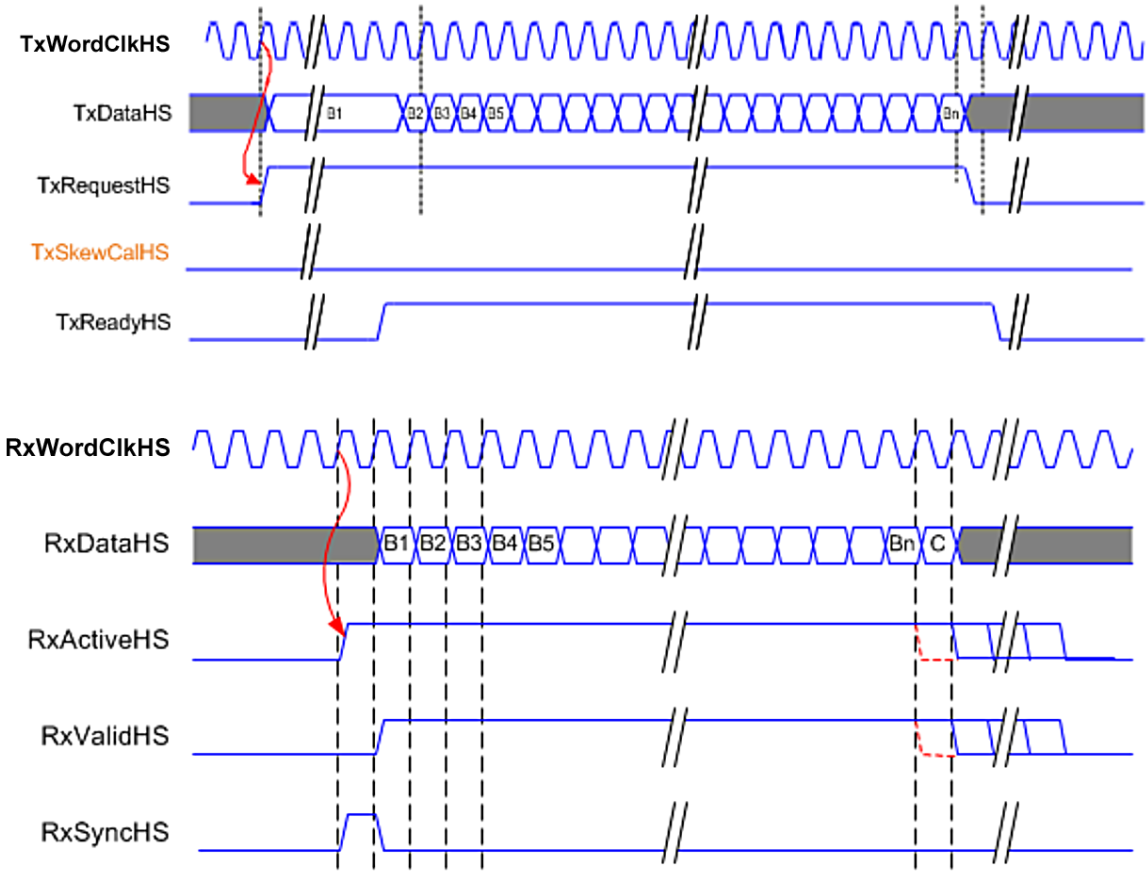


Figure 80 Periodic Skew Calibration - PPI Signal in Normal Mode

Figure 81 shows the PPI signal outputs as they operate during skew calibration in high-speed data transmission. It is possible for the RxWordClkHS to vary in frequency and duty cycle during the deskew operation. If the RxWordClkHS is varied, the period variation from clock period to clock period shall not be reduced by more than 0.5 UI with respect to the nominal period of RxWordClkHS.

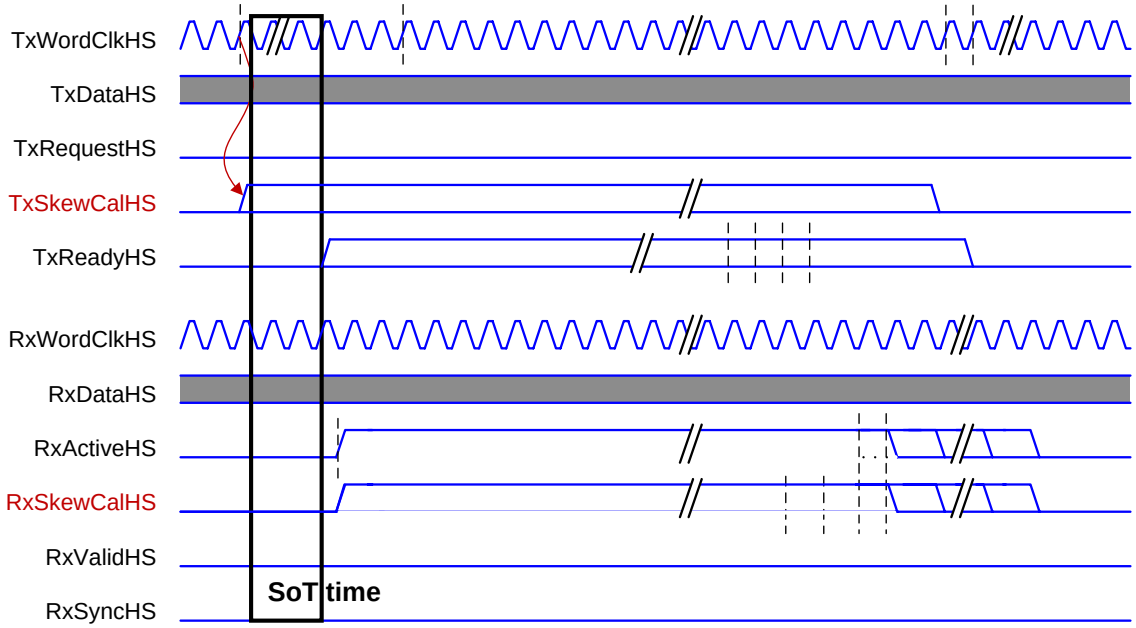


Figure 81 Periodic Skew Calibration - PPI Signal During Skew Calibration

A.10 High Speed Receive in HS-Idle State

Figure 82 illustrates High Speed data reception in the HS-Idle State. RxWordClkHS is derived from the HS clock, and is either at 1 or 0 level during the HS-Idle State. RxActiveHS and RxValidHS are similar to normal operation, and are not de-asserted during the HS-Idle State. HS data reception starts with a pulse on RxSyncHS at the beginning of the HS Date Burst after the HS-Idle State.

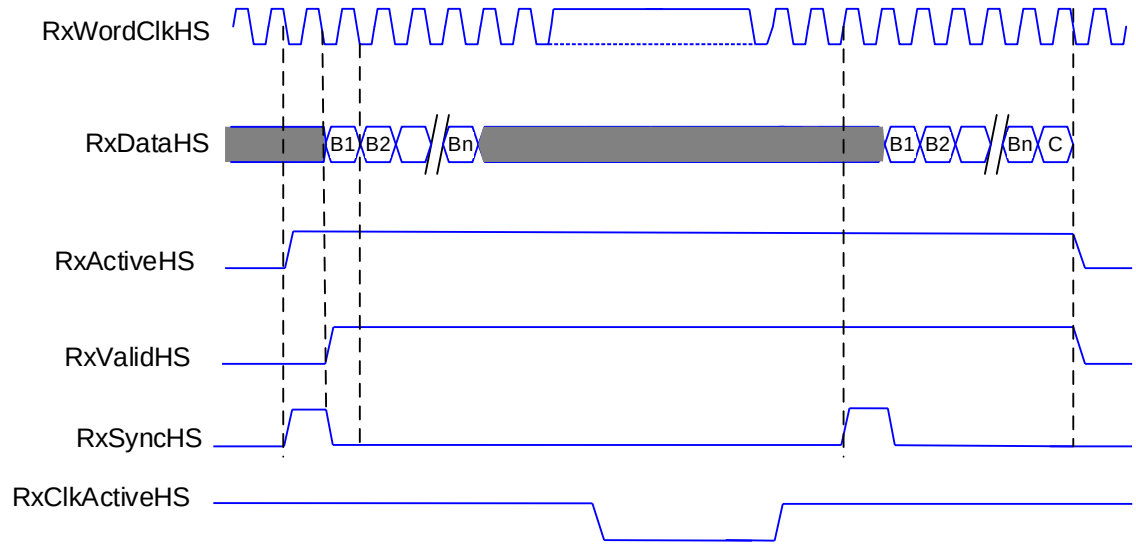


Figure 82 High Speed Reception in HS-Idle Mode

A.11 Optical Link Support

A.11.1 System Setup

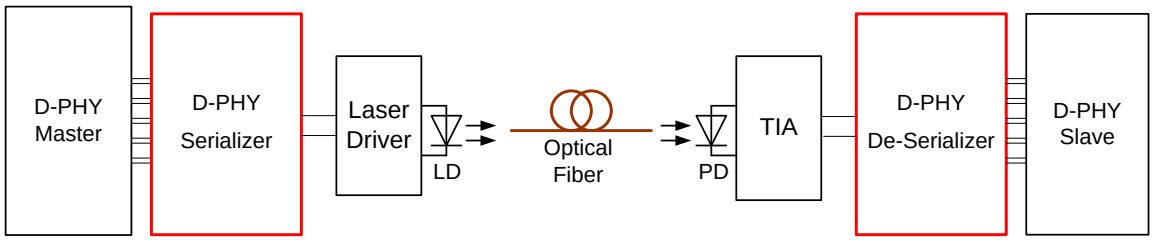


Figure 83 Typical System Setup with Optical Interconnect

Figure 83 shows a typical setup for a D-PHY system using an optical link.

The setup consists of a D-PHY Master providing the master clock and data lanes, and a serializer which multiplexes the data content of N data lanes into a single bit stream with embedded clock. The HS clock provided on the master clock lane is used as a reference for the clock multiplying unit in the serializer. The single bit stream is then converted from an electrical signal to an optical signal by means of a laser driver and a laser diode (LD) connected to it.

The optical signal transmitted through the optical fiber is converted back to an electrical signal by means of a photo diode (PD) and a transimpedance amplifier (TIA). The de-serializer synchronizes to the clock embedded in the serial data stream and de-multiplexes the data content of N data lanes. The output of the de-serializer to the D-PHY Slave is composed of a set of N D-PHY-compliant data lanes and a D-PHY compliant clock lane which replicates the D-PHY signal input to the serializer.

An optical link implemented in this manner provides a transparent interface between a D-PHY Master and a D-PHY Slave.

A.11.2 Serializer and De-Serializer Block Diagrams

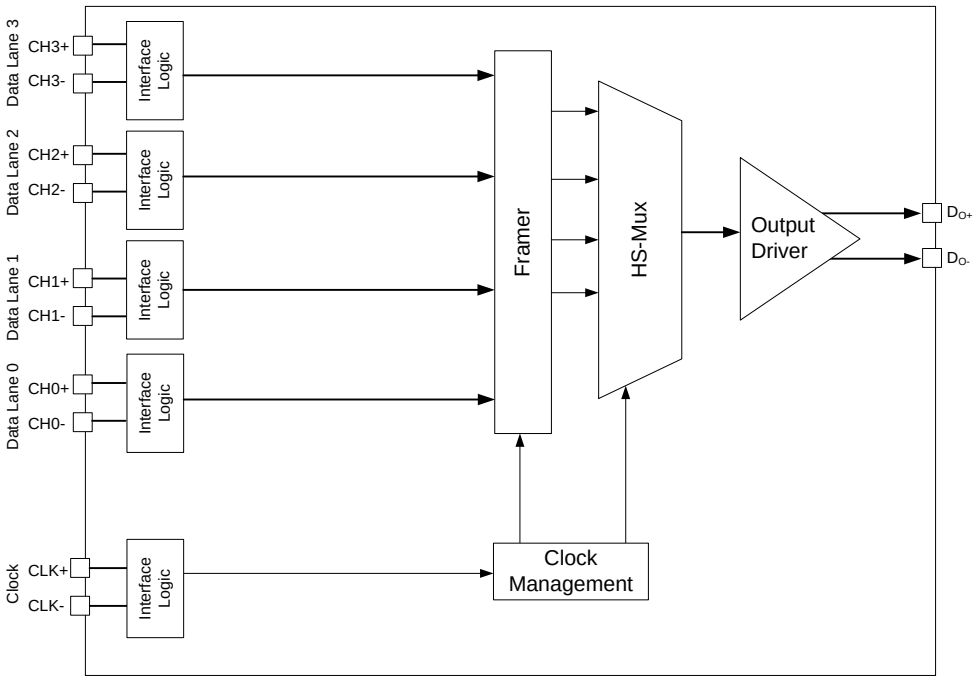


Figure 84 Block Diagram of Typical Serializer for Optical Link

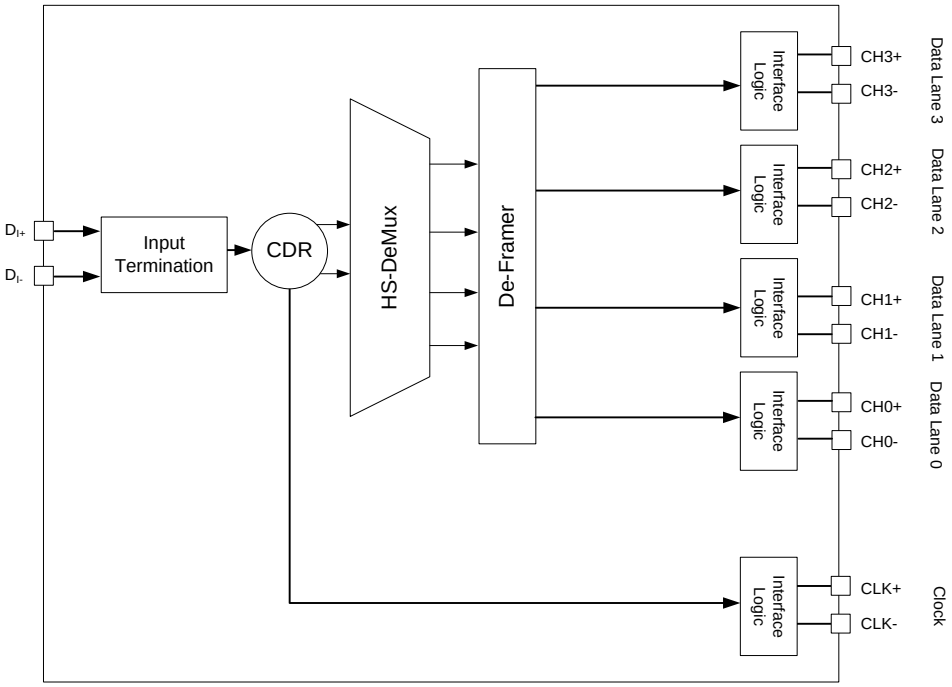


Figure 85 Block Diagram of Typical De-Serializer for Optical Link

Figure 84 and ***Figure 85*** show typical block diagrams for serializers and de-serializers used to implement the optical link.

A.11.3 Timing Constraints

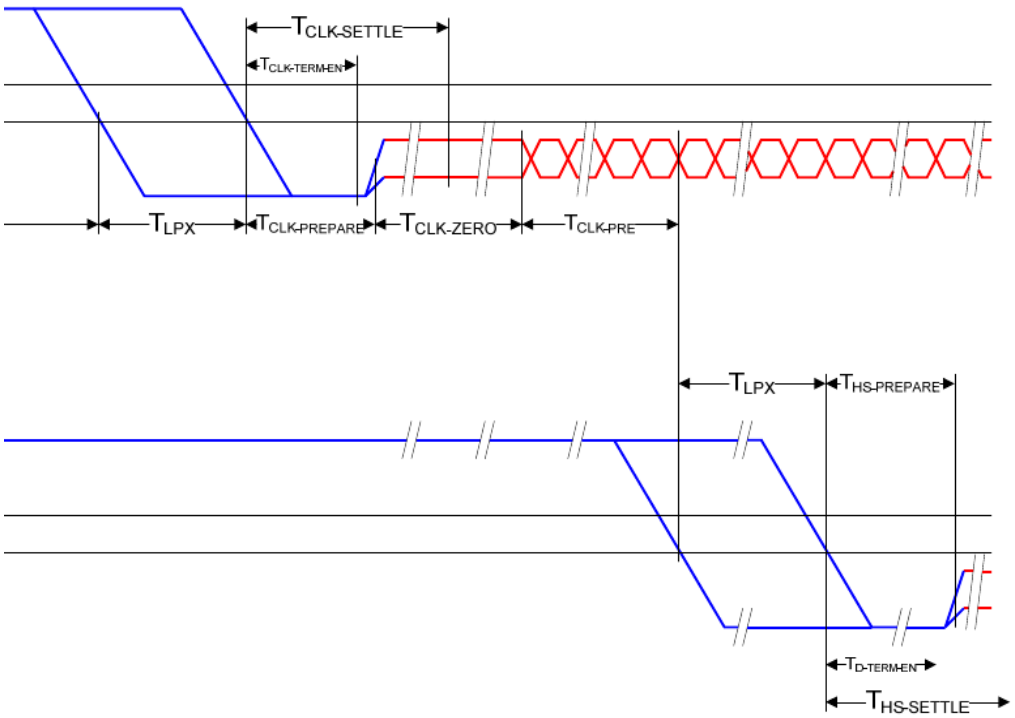


Figure 86 Delay Between Start of HS Clock and HS Data Transmission Without Optical Link

Figure 86 shows that in a purely electrical D-PHY interconnect, there is a timing delay between the start of HS clock transmission and the start of HS data transmission equal to the sum of $T_{CLK-PRE}$ + T_{LPX} + $T_{HS-SETTLE}$. However if an optical link is added as shown in ***Figure 83***, then the serializer's clock multiplying unit (typically a PLL) and the de-serializer's clock and data recovery (CDR) require synchronization times that exceed this timing delay.

Therefore, for an optical D-PHY interconnect an additional wait time $T_{WAIT-OPTICAL}$ shall be inserted before any HS data is transmitted, in order to provide enough timing headroom for the optical link to establish synchronization.

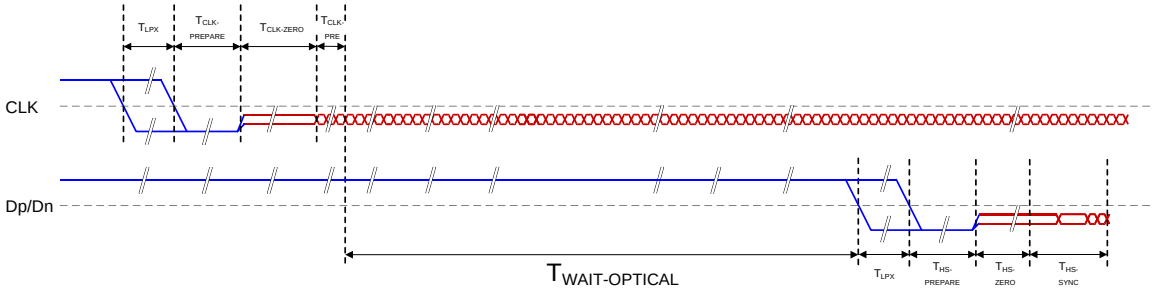


Figure 87 Delay Between Start of HS Clock and HS Data Transmission With Optical Link

Figure 87 illustrates the additional wait time $T_{WAIT-OPTICAL}$ inserted between the end of $T_{CLK-PRE}$ and the beginning of T_{LPX} of the first data lane scheduled to switch from STOP state to HS data mode. The additional wait time $T_{WAIT-OPTICAL}$ ensures that the optical link is fully synchronized by the time the first data lane switches from the STOP state to HS data mode. If the duration of the inserted $T_{WAIT-OPTICAL}$ is too short, then the optical link will not be able to correctly transmit the beginning of the next HS data burst, resulting in loss of state information and of HS data.

A.11.4 System Constraints

A.11.4.1 Bus Turnaround

Due to the optical link's inherently unidirectional nature, bus turnaround (BTA) may not be supported with an optical link.

A.11.4.2 Equalization (De-emphasis), Deskewing, and Spread Spectrum Clocking

Equalization (de-emphasis), deskewing and spread spectrum clocking may be supported by the optical link manufacturer. This must be stated in the corresponding datasheet of the optical link. If these features are included in the optical link, then the electrical inputs of the optical link shall follow the D-PHY specification for a D-PHY RX, and the electrical outputs of the optical link shall follow the specification for a D-PHY TX for these features. System integrators must take care to ensure compliance during implementation.

A.11.4.3 $T_{WAIT-OPTICAL}$

Table 46 specifies $T_{WAIT-OPTICAL}$, the parameter for additional wait time for synchronization of the optical link.

Table 46 Timing with Optical Link

Parameter	Description	Min	Units
$T_{WAIT-OPTICAL}$	Additional wait time for synchronization of the optical link	150,000	UI (lane data bit)

A.12 Higher Data Rate Operation

For certain channel conditions, there is margin to operate D-PHY v2.1 above the specified 4.5 Gbps limit. 6.5 Gbps is possible with a short channel, but the Specification does not detail any parameters beyond 4.5 Gbps. Implementers are left to extend operation to this higher data rate. The Conformance Test requirement is up to a data rate of 4.5 Gbps only for D-PHY v2.1.

Annex B Interconnect Design Guidelines (informative)

This Annex contains design guidelines in order to meet the interconnect requirements as specified in ***Section 8***.

B.1 Practical Distances

The maximum Lane flight time is defined at two nanoseconds. Assuming less than 100ps wiring delay within the RX-TX modules each, the physical distance that can be bridged with external interconnect is around 54cm/√ε. For most practical PCB and flex materials this corresponds to maximum distances around 25-30 cm.

B.2 RF Frequency Bands: Interference

On one side of the Lane there are the RF interference frequencies, which disturb the signals of the Lane. Most likely the dominant interferers are the transmit band frequencies of wireless interconnect standards. On the other side there are the frequencies for which generated EMI by the Lane should be as low as possible because very weak signals in these bands must be received by the radio IC. Some important frequency bands are:

Transmit Bands

- GSM 850 (824-849 MHz)
- GSM 900 (880-915 MHz)
- GSM DCS (1710-1785 MHz)
- GSM PCS (1850-1910 MHz)
- WCDMA (1920-1980 MHz)
- FLASH-OFDM, GSM (450 MHz)

Receive Bands:

- GSM 850 (869-894 MHz)
- GSM 900 (925-960 MHz)
- GSM DCS (1805-1880 MHz)
- GSM PCS (1930-1990 MHz)
- WCDMA (2110-2170 MHz)
- GPS (1574-1577 MHz)

It is important to identify the lowest interference frequency with significant impact, as this sets 'f_{INTMIN}'. For this specification, $f_{INT,MIN}$ is decided to be 450 MHz, because this frequency will most likely be used as the new WCDMA band in the USA in the future.

B.3 Transmission Line Design

In most cases the transmission lines will either be designed as striplines and/or micro-striplines. The coupling between neighboring lines within a pair is small if the distance between them is >2x the dielectric thickness. For the separation of multiple pairs it is highly recommended to interleave the pairs with a ground or supply line in order to reduce coupling.

B.4 Reference Layer

In order to achieve good signal integrity and low EMI it is recommended that either a ground plane or a ground signal is in close proximity of any signal line.

B.5 Printed-Circuit Board

For boards with a large number of conductor layers the dielectric spacing between layers may become so small that it would be hard to meet the characteristic impedance requirements. In those cases a micro-stripline in the top or bottom layers may be a better solution.

B.6 Flex-foils

Either two conductor layers or a reasonable connected cover layer makes it much easier to meet the specifications

B.7 Series Resistance

The DC series resistance of the interconnect should be less than 5 Ohms in order to meet the specifications. It is strongly recommended to keep the resistance in the ground connection below 0.2 Ohm. Furthermore, it is recommended that the DC ground shift be less than 50mV, which may require an even lower value if a large current is flowing through this ground. The lower this ground series resistance value can be made, the better it is for reliability and robustness.

B.8 Connectors

Connectors usually cause some impedance discontinuity. It is important to carefully minimize these discontinuities by design, especially with respect to the through-connection of the reference layer. Although connectors are typically rather small in size, the wrong choice can mess-up signals completely. Please note that the contact resistance of connectors is part of the total series resistance budget and should therefore be sufficiently low.

Annex C 8b9b Line Coding for D-PHY (normative)

Raw data transmission without constraining the data set does not allow in-band control signaling (control symbols inserted into the data stream) during transmission. Line coding conditions the possible bit sequences on the wires and provides reserved codes to include additional control features. Useful additional features may be, for example, idle symbols, specific-event identifiers, sync patterns, and protocol markers.

Comma codes, bit sequences that do not appear anywhere in the data stream (in the absence of bit errors) unless these are intentionally transmitted, provide synchronization features and are very useful to increase robustness.

Furthermore, a line-coding scheme that guarantees a minimum edge density improves the signaling quality and enables skew calibration in the PHY.

Figure 88 shows how the line coding sub-layer fits into the standard hierarchy. The line coding can be considered as a separate sub-layer on top of the basic D-PHY. Optimizations by merging layers are allowed if the resulting solution complies with the PHY specification. These optimization choices are left to implementers.

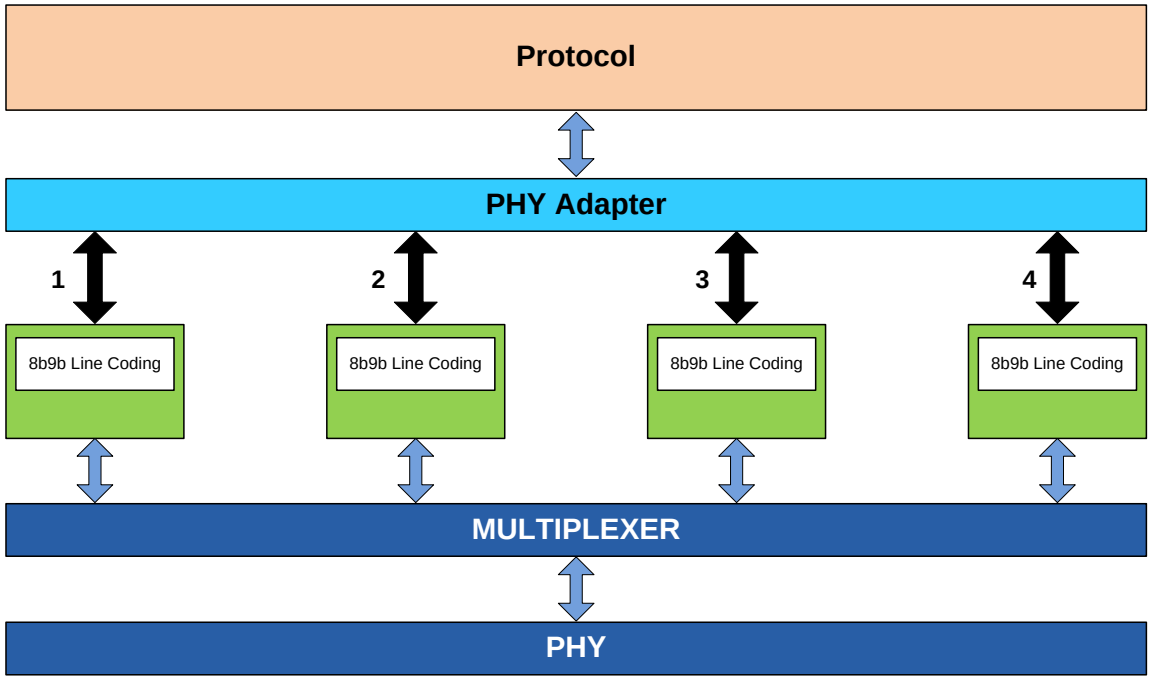


Figure 88 Line Coding Layer Example

Note that the line coding sub-layer is optional. Protocols may exploit only the baseline PHY without line coding. This feature is provided for compatibility with existing protocols. However, in case a protocol decides to use line coding, it shall be implemented as described in this annex.

The PHY-protocol interface above the line coding sub-layer (EPPI) is very similar to the PPI. Some additional signals enable a more functional and flexible control of the PHY with Line Coding. For details of the EPPI see Section C.5.

C.1 Line Coding Features

The 8b9b line coding scheme provides features to both the PHY and protocol layers.

C.1.1 Enabled Features for the Protocol

- Comma code marker for special protocol features
- Word synchronization/resynchronization during transmission bursts
- Automatic idling support; no need for TX to always provide valid data during transmission
- Possibility for future PHY compatible PHY-Protocol Interface (PPI)

C.1.2 Enabled Features for the PHY

- On-the-fly word resynchronization
- Simplification of EoT signaling
- Reduced latency
- Automatic idle symbol insertion and removal in absence of data
- Skew calibration in the RX possible

C.2 Coding Scheme

This section describes the details of the coding scheme.

C.2.1 8b9b Coding Properties

The 8b9b coding has the following properties:

- All code words are nine bits long. Data is encoded byte-wise into 9-bit words, which corresponds to a 12.5% coding overhead.
- Sixteen regular exception codes, i.e. code words that do not appear as regular data words, but require word sync for reliable recognition, are available.
- Six unique exception codes, i.e. code words that do not appear within any sliding window except when that code word is transmitted, are available.
- Guaranteed minimum edge density of at least two polarity transitions per word. Therefore, each word contains at least two ones and two zeros.
- Simple logical functions for encoding and decoding
- Run length is limited to a maximum of seven bits. Data codes have a maximum run length of five bits, unique exception codes have run lengths of six or seven bits.

C.2.2 Data Codes: Basic Code Set

Assume the following notation for the input data word and the coded data word:

- 8-bit data byte: [B_1 B_2 B_3 X_1 X_2 Q_1 Q_2 Q_3]
- 9-bit code word: [B_1 X_1 Y_1 Y_2 B_2 B_3 Y_3 Y_4 X_2]

The 256 data codes are denoted by Dxxx, where xxx is the value of the corresponding 8-bit data byte.

The 8-bit data byte shall be the input for the encoding, and result of the decoding, function. There can be any arbitrary bijective 8b-to-8b logical transformation function between real source data bytes from the protocol and the input data bytes for encoding, as long as the inverse function is present at the receiver side. If such a function is used, it shall be defined in the protocol specification.

The bits {B_1, B_2, B_3, X_1, X_2} appear directly in the code words as can be seen in the code word structure.

{Q_1, Q_2, Q_3} are the remaining three bits in the data byte, which are encoded into {Y_1, Y_2, Y_3, Y_4} using {X_1, X_2}. The decoding of {Y_1, Y_2, Y_3, Y_4} into {Q_1, Q_2, Q_3} does not require {X_1, X_2}.

The relation between Q_i, X_i and Y_i is shown in ***Table 47***.

Table 47 Encoding Table for 8b9b Line Coding of Data Words

8-bit Data Byte								9-bit Code Word, Y bits			
B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	Y_1	Y_2	Y_3	Y_4
x			x	1	1	1	0	0	1	0	0
				0						1	1
				x	0	1	0			0	1
					1	0	0			1	0
x			x	1	1	1	1	1	0	0	0
				0						1	1
				x	0	1	1			0	1
					1	0	1			1	0
x			0	x	0	0	0	1	1	0	1
			1					0	0		
			0	x	0	0	1	1	1	1	0
			1					0	0		

Note:
x = don't care

The logical relation for encoding between $\{Q_1, Q_2, Q_3, X_1, X_2\}$ and $\{Y_1, Y_2, Y_3, Y_4\}$ is given by the following equations:

$$Y_1 = (\sim Q_1 \,\&\, \sim Q_2 \,\&\, \sim X_1) \,|\, (Q_1 \,\&\, Q_3) \,|\, (Q_2 \,\&\, Q_3)$$

$$Y_2 = (\sim Q_1 \,\&\, \sim Q_2 \,\&\, \sim X_1) \,|\, (Q_1 \,\&\, \sim Q_3) \,|\, (Q_2 \,\&\, \sim Q_3)$$

$$Y_3 = (Q_1 \,\&\, \sim Q_2) \,|\, (Q_1 \,\&\, Q_2 \,\&\, \sim X_2) \,|\, (\sim Q_2 \,\&\, Q_3)$$

$$Y_4 = (\sim Q_1 \,\&\, Q_2) \,|\, (Q_1 \,\&\, Q_2 \,\&\, \sim X_2) \,|\, (\sim Q_1 \,\&\, \sim Q_3)$$

The logical relation for decoding between $\{Y_1, Y_2, Y_3, Y_4\}$ and $\{Q_1, Q_2, Q_3\}$ is:

$$Q_1 = (Y_1 \,\hat{}\, Y_2) \,\&\, \sim(\sim Y_3 \,\&\, Y_4)$$

$$Q_2 = (Y_1 \,\hat{}\, Y_2) \,\&\, \sim(Y_3 \,\&\, \sim Y_4)$$

$$Q_3 = (Y_1 \,\&\, \sim Y_2) \,|\, (Y_1 \,\&\, Y_2 \,\&\, Y_3) \,|\, (\sim Y_1 \,\&\, \sim Y_2 \,\&\, Y_3)$$
$$= (Y_1 \,\&\, \sim Y_2) \,|\, (\sim (Y_1 \,\hat{}\, Y_2) \,\&\, Y_3)$$

These logical functions show that the encoding and decoding can be implemented with a few dozen logic gates and therefore do not require additional hardware such as a lookup table or storage of history data.

C.2.3 Comma Codes: Unique Exception Codes

Unique means that these codes are uniquely identifiable in the data stream because these sequences do not occur in any encoding or across word boundaries, assuming no bits are corrupted. The data-encoding scheme described in ***Section C.2.2*** enables a very simple run-length limit based unique exception code mechanism.

There are four code sequences available, called Type A Comma codes, with a run length of six bits, and two code sequences, called Type B Comma codes, with a run length of seven bits. Currently, four Comma codes are sufficient to cover the required features and therefore only Type A Comma codes are used. Type B Comma codes are reserved for future use.

Table 48 Comma Codes

Type	Run Length, bits	Code Name	Comma code	Feature
Type A	6	C600	0 1111 1100	Protocol
		C611	1 0000 0011	EoT
		C610	1 0000 0010	Idle/Sync 1
		C601	0 1111 1101	Idle/Sync 2
Type B	7	C701	1 0000 0001	Reserved 1
		C710	0 1111 1110	Reserved 2

C.2.4 Control Codes: Regular Exception Codes

The normal data set does not use all codes with a maximum run-length of five bits. There are two combinations of the $\{X_i,Y_i\}$ bits that do not appear in any data code word that are available as regular exception codes. Since Comma Codes are defined to have a run-length of six or seven bits, this gives three freely usable bits per code word and results in $2*2^3=16$ different Regular Exception Codes. The syntax of the Regular Exception Code words is given in ***Table 49***, where the bits B_1, B_2 and B_3 can have any binary value.

Table 49 Regular Exception Code Structure

	X_1	Y_1	Y_2			Y_3	Y_4	Y_2	Code Name
B_1	0	1	1	B_2	B_3	0	0	1	C410-C417
B_1	1	0	0	B_2	B_3	1	1	0	C400-C407

These code words are not unique sequences like the Comma codes described in ***Table 48***, but can only be used as exception codes if word sync is already accomplished. These codes are currently reserved and not yet allocated to any function.

C.2.5 Complete Coding Scheme

The complete code table can be found in ***Table 51***.

C.3 Operation with the D-PHY

The line coding impacts the payload of transmission bursts. Section C.3.1 described the generic issues for both HS and LP transmission. Section C.3.2 and Section C.3.3 describe specific details for HS and LP transmission, respectively.

C.3.1 Payload: Data and Control

The payload of a HS or LP transmission burst consists of concatenated serialized 9-bit symbols, representing both data and control information.

C.3.1.1 Idle/Sync Comma Symbols

Idle/Sync Comma code words can be present as symbols within the payload of a transmission burst. These symbols are inserted either on specific request of the protocol, or autonomously when there is a transmission request but there is no valid data available either at the beginning, or anywhere, during transmission. The Idle pattern in the latter case is an alternating C601 and C610 sequence, until there is valid data available to transmit, or transmission has ended. Idle periods may begin with either of the two prescribed Idle symbols. The RX-side PHY shall remove Idle/Sync symbols from the stream and flag these events to the protocol.

C.3.1.2 Protocol Marker Comma Symbol

Comma symbol C600 (Protocol Marker) is allocated for use by protocols on top of the D-PHY. This symbol shall be inserted in the stream on request of the TX-side protocol and flagged by the receiving PHY to the RX-side protocol.

C.3.1.3 EoT Marker

Comma symbol C611 is allocated as the EoT Marker symbol.

C.3.2 Details for HS Transmission

C.3.2.1 SoT

The SoT procedure remains the same as the raw data D-PHY SoT. See Section 6.4.2. The SoT sequence itself is NOT encoded, but can be easily recognized.

The first bit of the first transmitted code symbol of a burst shall be aligned with the rising edge of the DDR clock.

C.3.2.2 HS Transmission Payload

The transmitted burst shall consist of concatenated serialized 9-bit symbols as described in Section C.3.1.

The TX-side PHY can idle by sending the Idle sequences as described in Section C.3.1.1

C.3.2.3 EoT

The TX-side PHY shall insert an EoT marker symbol at the moment the request for HS transmission is withdrawn. The transmitter can pad additional bits after this EoT-Marker symbol before actually switching to LP mode (EoT sequence).

The RX-side PHY shall remove the EoT-Marker symbol and any additional bits appearing after it. Note that with line coding, EoT-processing by backtracking on LP-11 detection to avoid (unreliable) non-payload bits on the PPI is no longer required as the EoT marker symbol notifies the RX-side PHY before the End-of-Transmission.

C.3.3 Details for LP Transmission

C.3.3.1 SoT

The start of LP transmission is identical to basic D-PHY operation.

C.3.3.2 LP Transmission Payload

The transmitted burst shall consist of concatenated serialized 9-bit symbols as described in Section C.3.1.

During LPDT, the TX-side PHY can idle in two ways: either it can send the Idle sequences as described in Section C.3.1.1 and implicitly provide a clock signal to the RX-side PHY, or it can pause the transmission by keeping the Lines at LP-00 (Space) for a certain period of time between bits, which interrupts the clock on the RX side, but minimizes power consumption.

C.3.3.3 EoT

The TX-side PHY shall insert an EoT marker symbol at the moment the request for LP transmission is withdrawn. The TX-side PHY can pad additional (spaced-one-hot) bits after the EoT-Marker symbol before actually ending the transmission by switching via Mark to Stop state (End of LPDT procedure).

The RX-side PHY shall remove the EoT-marker symbol and any additional bits appearing after it.

C.4 Error Signaling

The usage of a line code scheme enables the detection of many signaling errors. These errors include:

- Non-existing code words
- Non-aligned Comma symbols
- EoT detection without detection of EoT-Marker

Detection and flagging of errors is not required, but may help the protocol to recover faster from an error situation.

C.5 Extended PPI

The interface to the protocol shall be extended with functional handles (TX) and flags (RX) to manage the usage of Comma symbols. Whenever necessary, the transmitting PHY can hold the data delivery from the protocol to the TX PHY with the TxReadyHS or TxReadyEsc signal. This is already provided for in the current PPI.

The PPI shall be extended with a TX Valid signal for HS data transmission, TxValidHS. Encoded operation allows for Idling of the Link when there is no new valid data. If the transmitter is ready and the provided data is not valid, an Idle symbol shall be inserted into the stream. Note, contrary to the basic PHY PPI, the Valid signals for a coded PHY can be actively used to manage the data on both TX and RX sides. This arrangement provides more flexibility to the PHY and Protocol layers. For LPDT, this Valid signaling already exists in the PPI. Addition of TxValidHS signal eliminates the constraint in the PPI description for TxRequestHS that the “protocol always provides valid data”.

On the RX side, errors may be flagged to the protocol in case unexpected sequences are observed. Although many different errors are detectable, it is not required that all these errors flags be implemented. The number of error flags implemented depends on the cost/benefit trade-off to be made by the implementer. These error features do not impact compliance of the D-PHY. The signals are mentioned here for informative purposes only.

All control signals shall remain synchronous to the TxWordClk, or RxWordClk. The control signal clock frequency shall be equal to or greater than 1/(n * 9) of the serial bit rate, where n is the data bus width in bytes.

Table 50 lists the additional signals for the PPI on top of the coding sub-layer (EPPI) for an 8-bit interface only.

Table 50 Additional Signals for (Functional) PPI

Symbol	Dir	Categories	Description
TxProMarkerEsc	I	MXAX (SXXA)	Functional handle to insert a Protocol-marker symbol in the serial stream for LPDT. Active HIGH signal
TxProMarkerHS	I	MXXX (SRXX)	Functional handle to insert a Protocol-marker symbol in the serial stream for HS transmission. Active HIGH signal
TxValidHS	I	MXXX (SRXX)	Functional handle for the protocol to hold on providing data to the PHY without ending the HS transmission. In the case of a continued transmission request without Valid data, the PHY coding layer inserts Idle symbols. Active HIGH signal
RxAlignErrorEsc	O	SXAX (MXXA)	Flag to indicate that a Comma code has been observed in the LPDT stream that was not aligned with the assumed word boundary. Active HIGH signal (optional)
RxAlignErrorHS	O	SXXX (MRXX)	Flag to indicate that a Comma code has been observed during HS reception that was not aligned with the assumed word boundary. Active HIGH signal (optional)
RxBadSymbolEsc	O	SXAX (MXXA)	Flag to indicate that a non-existing symbol was received using LPDT. Active HIGH signal (optional)
RxBadSymbolHS	O	SXXX (MRXX)	Flag to indicate that a non-existing symbol was received in HS mode. Active HIGH signal (optional)
RxEoTErrorEsc	O	SXAX (MXXA)	Flag to indicate that at EoT, after LP transmission, a transition to LP-11 has been detected without being preceded by an EoT-marker symbol. Active HIGH signal (optional)
RxEoTErrorHS	O	SXXX (MRXX)	Flag to indicate that at EoT, after HS transmission, a transition to LP-11 has been detected without being preceded by an EoT-marker symbol. Active HIGH signal (optional)
RxIdleEsc	O	SXAX (MXXA)	Indication flag that Idle patterns are observed at the Lines during LPDT. Active HIGH signal (optional)
RxIdleHS	O	SXXX (MRXX)	Indication flag that Idle patterns are observed at the Lines in HS mode. Active HIGH signal (optional)
RxProMarkerEsc	O	SXAX (MXXA)	Functional flag to know that a Protocol-marker symbol occurred in the serial stream using LPDT. This is communicated to the protocol synchronous with the data, exactly at the position where it occurred. Therefore, the interface either shows a flag plus non-valid data or no-flag with valid data. Active HIGH signal
RxProMarkerHS	O	SXXX (MRXX)	Functional flag to know that a Protocol-marker symbol occurred in the serial stream for HS mode. This is communicated to the protocol synchronous with the ByteClk, exactly at the position where it occurred. Therefore, the interface either shows a flag plus non-valid data or no-flag with valid data. Active HIGH signal

C.6 Complete Code Set

1819 ***Table 51*** contains the complete code set.

1820 **Table 51 Code Set (8b9b Line Coding)**

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D000	Data	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0
D001	Data	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0
D002	Data	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0
D003	Data	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0
D004	Data	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0
D005	Data	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0
D006	Data	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	1	0
D007	Data	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0
D008	Data	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1
D009	Data	0	0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	1
D010	Data	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	1	1
D011	Data	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	1	1
D012	Data	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	1
D013	Data	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	0	1
D014	Data	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	1
D015	Data	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	1
D016	Data	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0
D017	Data	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0
D018	Data	0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	0
D019	Data	0	0	0	1	0	0	1	1	0	1	1	0	0	0	0	1	0
D020	Data	0	0	0	1	0	1	0	0	0	1	0	1	0	0	1	0	0
D021	Data	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	0
D022	Data	0	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1	0
D023	Data	0	0	0	1	0	1	1	1	0	1	1	0	0	0	1	1	0
D024	Data	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1
D025	Data	0	0	0	1	1	0	0	1	0	1	0	0	0	0	1	0	1
D026	Data	0	0	0	1	1	0	1	0	0	1	0	1	0	0	0	1	1
D027	Data	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	1
D028	Data	0	0	0	1	1	1	0	0	0	1	0	1	0	0	1	0	1
D029	Data	0	0	0	1	1	1	0	1	0	1	1	0	0	0	1	0	1
D030	Data	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1
D031	Data	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1
D032	Data	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0
D033	Data	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	0	0

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D034	Data	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	0
D035	Data	0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0
D036	Data	0	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	0
D037	Data	0	0	1	0	0	1	0	1	0	0	1	0	0	1	1	0	0
D038	Data	0	0	1	0	0	1	1	0	0	0	0	1	0	1	1	1	0
D039	Data	0	0	1	0	0	1	1	1	0	0	1	0	0	1	1	1	0
D040	Data	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1	1
D041	Data	0	0	1	0	1	0	0	1	0	0	1	1	0	1	1	0	1
D042	Data	0	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1
D043	Data	0	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
D044	Data	0	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1
D045	Data	0	0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	1
D046	Data	0	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	1
D047	Data	0	0	1	0	1	1	1	1	0	0	1	0	0	1	0	0	1
D048	Data	0	0	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0
D049	Data	0	0	1	1	0	0	0	1	0	1	0	0	0	1	1	0	0
D050	Data	0	0	1	1	0	0	1	0	0	1	0	1	0	1	0	1	0
D051	Data	0	0	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
D052	Data	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0
D053	Data	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0
D054	Data	0	0	1	1	0	1	1	0	0	1	0	1	0	1	1	1	0
D055	Data	0	0	1	1	0	1	1	1	0	1	1	0	0	1	1	1	0
D056	Data	0	0	1	1	1	0	0	0	0	1	0	0	0	1	0	1	1
D057	Data	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	1
D058	Data	0	0	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
D059	Data	0	0	1	1	1	0	1	1	0	1	1	0	0	1	0	1	1
D060	Data	0	0	1	1	1	1	0	0	0	1	0	1	0	1	1	0	1
D061	Data	0	0	1	1	1	1	0	1	0	1	1	0	0	1	1	0	1
D062	Data	0	0	1	1	1	1	1	0	0	1	0	1	0	1	0	0	1
D063	Data	0	0	1	1	1	1	1	1	0	1	1	0	0	1	0	0	1
D064	Data	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0
D065	Data	0	1	0	0	0	0	0	1	0	0	1	1	1	0	1	0	0
D066	Data	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0
D067	Data	0	1	0	0	0	0	1	1	0	0	1	0	1	0	0	1	0
D068	Data	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0
D069	Data	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0
D070	Data	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	1	0
D071	Data	0	1	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D072	Data	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	1
D073	Data	0	1	0	0	1	0	0	1	0	0	1	1	1	0	1	0	1
D074	Data	0	1	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1
D075	Data	0	1	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1
D076	Data	0	1	0	0	1	1	0	0	0	0	0	1	1	0	1	0	1
D077	Data	0	1	0	0	1	1	0	1	0	0	1	0	1	0	1	0	1
D078	Data	0	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1
D079	Data	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1
D080	Data	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0
D081	Data	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	0
D082	Data	0	1	0	1	0	0	1	0	0	1	0	1	1	0	0	1	0
D083	Data	0	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1	0
D084	Data	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	0
D085	Data	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	0
D086	Data	0	1	0	1	0	1	1	0	0	1	0	1	1	0	1	1	0
D087	Data	0	1	0	1	0	1	1	1	0	1	1	0	1	0	1	1	0
D088	Data	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1
D089	Data	0	1	0	1	1	0	0	1	0	1	0	0	1	0	1	0	1
D090	Data	0	1	0	1	1	0	1	0	0	1	0	1	1	0	0	1	1
D091	Data	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	1	1
D092	Data	0	1	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1
D093	Data	0	1	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1
D094	Data	0	1	0	1	1	1	1	0	0	1	0	1	1	0	0	0	1
D095	Data	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	0	1
D096	Data	0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	0
D097	Data	0	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0
D098	Data	0	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	0
D099	Data	0	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
D100	Data	0	1	1	0	0	1	0	0	0	0	0	1	1	1	1	0	0
D101	Data	0	1	1	0	0	1	0	1	0	0	1	0	1	1	1	0	0
D102	Data	0	1	1	0	0	1	1	0	0	0	0	1	1	1	1	1	0
D103	Data	0	1	1	0	0	1	1	1	0	0	1	0	1	1	1	1	0
D104	Data	0	1	1	0	1	0	0	0	0	0	1	1	1	1	0	1	1
D105	Data	0	1	1	0	1	0	0	1	0	0	1	1	1	1	1	0	1
D106	Data	0	1	1	0	1	0	1	0	0	0	0	1	1	1	0	1	1
D107	Data	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0	1	1
D108	Data	0	1	1	0	1	1	0	0	0	0	0	1	1	1	1	0	1
D109	Data	0	1	1	0	1	1	0	1	0	0	1	0	1	1	1	0	1

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D110	Data	0	1	1	0	1	1	1	0	0	0	0	1	1	1	0	0	1
D111	Data	0	1	1	0	1	1	1	1	0	0	1	0	1	1	0	0	1
D112	Data	0	1	1	1	0	0	0	0	0	1	0	0	1	1	0	1	0
D113	Data	0	1	1	1	0	0	0	1	0	1	0	0	1	1	1	0	0
D114	Data	0	1	1	1	0	0	1	0	0	1	0	1	1	1	0	1	0
D115	Data	0	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	0
D116	Data	0	1	1	1	0	1	0	0	0	1	0	1	1	1	1	0	0
D117	Data	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	0	0
D118	Data	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	1	0
D119	Data	0	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	0
D120	Data	0	1	1	1	1	0	0	0	0	1	0	0	1	1	0	1	1
D121	Data	0	1	1	1	1	0	0	1	0	1	0	0	1	1	1	0	1
D122	Data	0	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1	1
D123	Data	0	1	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1
D124	Data	0	1	1	1	1	1	0	0	0	1	0	1	1	1	1	0	1
D125	Data	0	1	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1
D126	Data	0	1	1	1	1	1	1	0	0	1	0	1	1	1	0	0	1
D127	Data	0	1	1	1	1	1	1	1	0	1	1	0	1	1	0	0	1
D128	Data	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0
D129	Data	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	0	0
D130	Data	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0
D131	Data	1	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0
D132	Data	1	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0
D133	Data	1	0	0	0	0	1	0	1	1	0	1	0	0	0	1	0	0
D134	Data	1	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	0
D135	Data	1	0	0	0	0	1	1	1	1	0	1	0	0	0	1	1	0
D136	Data	1	0	0	0	1	0	0	0	1	0	1	1	0	0	0	1	1
D137	Data	1	0	0	0	1	0	0	1	1	0	1	1	0	0	1	0	1
D138	Data	1	0	0	0	1	0	1	0	1	0	0	1	0	0	0	1	1
D139	Data	1	0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	1
D140	Data	1	0	0	0	1	1	0	0	1	0	0	1	0	0	1	0	1
D141	Data	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	0	1
D142	Data	1	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1
D143	Data	1	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	1
D144	Data	1	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0
D145	Data	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	0
D146	Data	1	0	0	1	0	0	1	0	1	1	0	1	0	0	0	1	0
D147	Data	1	0	0	1	0	0	1	1	1	1	1	0	0	0	0	1	0

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D148	Data	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1	0	0
D149	Data	1	0	0	1	0	1	0	1	1	1	1	0	0	0	1	0	0
D150	Data	1	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0
D151	Data	1	0	0	1	0	1	1	1	1	1	1	0	0	0	1	1	0
D152	Data	1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	1
D153	Data	1	0	0	1	1	0	0	1	1	1	0	0	0	0	1	0	1
D154	Data	1	0	0	1	1	0	1	0	1	1	0	1	0	0	0	1	1
D155	Data	1	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1
D156	Data	1	0	0	1	1	1	0	0	1	1	0	1	0	0	1	0	1
D157	Data	1	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0	1
D158	Data	1	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1
D159	Data	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1
D160	Data	1	0	1	0	0	0	0	0	1	0	1	1	0	1	0	1	0
D161	Data	1	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0
D162	Data	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0
D163	Data	1	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
D164	Data	1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	0
D165	Data	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0
D166	Data	1	0	1	0	0	1	1	0	1	0	0	1	0	1	1	1	0
D167	Data	1	0	1	0	0	1	1	1	1	0	1	0	0	1	1	1	0
D168	Data	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1	1
D169	Data	1	0	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
D170	Data	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	1
D171	Data	1	0	1	0	1	0	1	1	1	0	1	0	0	1	0	1	1
D172	Data	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1	0	1
D173	Data	1	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
D174	Data	1	0	1	0	1	1	1	0	1	0	0	1	0	1	0	0	1
D175	Data	1	0	1	0	1	1	1	1	1	0	1	0	0	1	0	0	1
D176	Data	1	0	1	1	0	0	0	0	1	1	0	0	0	1	0	1	0
D177	Data	1	0	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0
D178	Data	1	0	1	1	0	0	1	0	1	1	0	1	0	1	0	1	0
D179	Data	1	0	1	1	0	0	1	1	1	1	1	0	0	1	0	1	0
D180	Data	1	0	1	1	0	1	0	0	1	1	0	1	0	1	1	0	0
D181	Data	1	0	1	1	0	1	0	1	1	1	1	0	0	1	1	0	0
D182	Data	1	0	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0
D183	Data	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	1	0
D184	Data	1	0	1	1	1	0	0	0	1	1	0	0	0	1	0	1	1
D185	Data	1	0	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D186	Data	1	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1	1
D187	Data	1	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
D188	Data	1	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1
D189	Data	1	0	1	1	1	1	0	1	1	1	1	0	0	1	1	0	1
D190	Data	1	0	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1
D191	Data	1	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	1
D192	Data	1	1	0	0	0	0	0	0	1	0	1	1	1	0	0	1	0
D193	Data	1	1	0	0	0	0	0	1	1	0	1	1	1	0	1	0	0
D194	Data	1	1	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0
D195	Data	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0
D196	Data	1	1	0	0	0	1	0	0	1	0	0	1	1	0	1	0	0
D197	Data	1	1	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0
D198	Data	1	1	0	0	0	1	1	0	1	0	0	1	1	0	1	1	0
D199	Data	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	1	0
D200	Data	1	1	0	0	1	0	0	0	1	0	1	1	1	0	0	1	1
D201	Data	1	1	0	0	1	0	0	1	1	0	1	1	1	0	1	0	1
D202	Data	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1
D203	Data	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1
D204	Data	1	1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	1
D205	Data	1	1	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1
D206	Data	1	1	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1
D207	Data	1	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	1
D208	Data	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0
D209	Data	1	1	0	1	0	0	0	1	1	1	0	0	1	0	1	0	0
D210	Data	1	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1	0
D211	Data	1	1	0	1	0	0	1	1	1	1	1	0	1	0	0	1	0
D212	Data	1	1	0	1	0	1	0	0	1	1	0	1	1	0	1	0	0
D213	Data	1	1	0	1	0	1	0	1	1	1	1	0	1	0	1	0	0
D214	Data	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1	1	0
D215	Data	1	1	0	1	0	1	1	1	1	1	1	0	1	0	1	1	0
D216	Data	1	1	0	1	1	0	0	0	1	1	0	0	1	0	0	1	1
D217	Data	1	1	0	1	1	0	0	1	1	1	0	0	1	0	1	0	1
D218	Data	1	1	0	1	1	0	1	0	1	1	0	1	1	0	0	1	1
D219	Data	1	1	0	1	1	0	1	1	1	1	1	0	1	0	0	1	1
D220	Data	1	1	0	1	1	1	0	0	1	1	0	1	1	0	1	0	1
D221	Data	1	1	0	1	1	1	0	1	1	1	1	0	1	0	1	0	1
D222	Data	1	1	0	1	1	1	1	0	1	1	0	1	1	0	0	0	1
D223	Data	1	1	0	1	1	1	1	1	1	1	1	0	1	0	0	0	1

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
D224	Data	1	1	1	0	0	0	0	0	1	0	1	1	1	1	0	1	0
D225	Data	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0
D226	Data	1	1	1	0	0	0	1	0	1	0	0	1	1	1	0	1	0
D227	Data	1	1	1	0	0	0	1	1	1	0	1	0	1	1	0	1	0
D228	Data	1	1	1	0	0	1	0	0	1	0	0	1	1	1	1	0	0
D229	Data	1	1	1	0	0	1	0	1	1	0	1	0	1	1	1	0	0
D230	Data	1	1	1	0	0	1	1	0	1	0	0	1	1	1	1	1	0
D231	Data	1	1	1	0	0	1	1	1	1	0	1	0	1	1	1	1	0
D232	Data	1	1	1	0	1	0	0	0	1	0	1	1	1	1	0	1	1
D233	Data	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1	0	1
D234	Data	1	1	1	0	1	0	1	0	1	0	0	1	1	1	0	1	1
D235	Data	1	1	1	0	1	0	1	1	1	0	1	0	1	1	0	1	1
D236	Data	1	1	1	0	1	1	0	0	1	0	0	1	1	1	1	0	1
D237	Data	1	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1
D238	Data	1	1	1	0	1	1	1	0	1	0	0	1	1	1	0	0	1
D239	Data	1	1	1	0	1	1	1	1	1	0	1	0	1	1	0	0	1
D240	Data	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	1	0
D241	Data	1	1	1	1	0	0	0	1	1	1	0	0	1	1	1	0	0
D242	Data	1	1	1	1	0	0	1	0	1	1	0	1	1	1	0	1	0
D243	Data	1	1	1	1	0	0	1	1	1	1	1	0	1	1	0	1	0
D244	Data	1	1	1	1	0	1	0	0	1	1	0	1	1	1	1	0	0
D245	Data	1	1	1	1	0	1	0	1	1	1	1	0	1	1	1	0	0
D246	Data	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	1	0
D247	Data	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0
D248	Data	1	1	1	1	1	0	0	0	1	1	0	0	1	1	0	1	1
D249	Data	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	0	1
D250	Data	1	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1	1
D251	Data	1	1	1	1	1	0	1	1	1	1	1	0	1	1	0	1	1
D252	Data	1	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0	1
D253	Data	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	0	1
D254	Data	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0	1
D255	Data	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1
C400	Rsvd	Does not represent data								0	1	0	0	0	0	1	1	0
C401	Rsvd	Does not represent data								0	1	0	0	0	1	1	1	0
C402	Rsvd	Does not represent data								0	1	0	0	1	0	1	1	0
C403	Rsvd	Does not represent data								0	1	0	0	1	1	1	1	0
C404	Rsvd	Does not represent data								1	1	0	0	0	0	1	1	0
C405	Rsvd	Does not represent data								1	1	0	0	0	1	1	1	0

		8-bit Data Byte								9-bit Symbol								
Name	**Type**	**B_1**	**B_2**	**B_3**	**X_1**	**X_2**	**Q_1**	**Q_2**	**Q_3**	**B_1**	**X_1**	**Y_1**	**Y_2**	**B_2**	**B_3**	**Y_3**	**Y_4**	**X_2**
C406	Rsvd	Does not represent data								1	1	0	0	1	0	1	1	0
C407	Rsvd	Does not represent data								1	1	0	0	1	1	1	1	0
C410	Rsvd	Does not represent data								0	0	1	1	0	0	0	0	1
C411	Rsvd	Does not represent data								0	0	1	1	0	1	0	0	1
C412	Rsvd	Does not represent data								0	0	1	1	1	0	0	0	1
C413	Rsvd	Does not represent data								0	0	1	1	1	1	0	0	1
C414	Rsvd	Does not represent data								1	0	1	1	0	0	0	0	1
C415	Rsvd	Does not represent data								1	0	1	1	0	1	0	0	1
C416	Rsvd	Does not represent data								1	0	1	1	1	0	0	0	1
C417	Rsvd	Does not represent data								1	0	1	1	1	1	0	0	1
C600	Protocol	Does not represent data								0	1	1	1	1	1	1	0	0
C611	EoT	Does not represent data								1	0	0	0	0	0	0	1	1
C601	Idle/Sync1	Does not represent data								0	1	1	1	1	1	1	0	1
C610	Idle/Sync2	Does not represent data								1	0	0	0	0	0	0	1	0
C701	Reserved	Does not represent data								1	0	0	0	0	0	0	0	1
C710	Rsvd	Does not represent data								0	1	1	1	1	1	1	1	0

Note:

Rsvd = Reserved

See Errata 01 Item 10: Insert new Annex D here

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