Arm® Neoverse CMN-700 Coherent Mesh Network

Software Developer Errata Notice

Date of issue: 13-Sep-2023

Non-Confidential

Document version: 13.0

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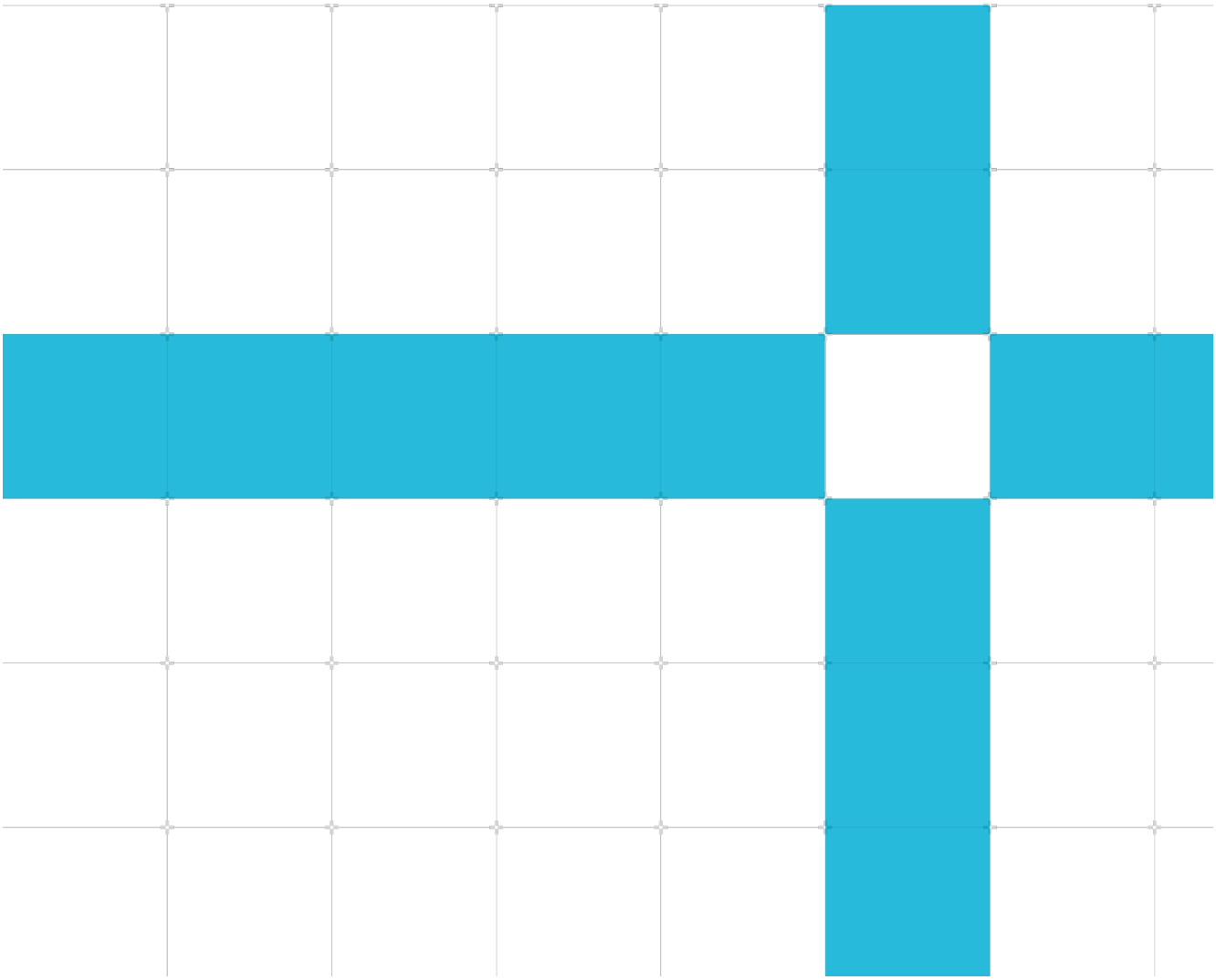
This document contains all known errata since the r0p0 release of the product.



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Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

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Contents

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The **errata summary table** identifies errata that have been fixed in each product revision.

13-Sep-2023: Changes in document version v13.0

ID	Status	Area	Category	Summary
3037722	New	Programmer	Category A	Multi-chip SMP deadlock in the presence of CPU traffic when CCG HA_REQ_PASS_BUFF_DEPTH < RA_NUM_REQS
3033917	New	Programmer	Category B	StashOnce*Sep operations generated by CPU's PRFM PLD/PST L3 instructions targeting remote chip memory can cause a deadlock

23-Aug-2023: Changes in document version v12.0

ID	Status	Area	Category	Summary
3013638	New	Programmer	Category B	Write Stash can cause multi-copy atomicity issue
3013641	New	Programmer	Category B (rare)	Incorrect TagMatch response on partial writes with MTE Match
3015226	New	Programmer	Category C	Debug reads with simultaneous coherent traffic or dynamic power transitions can cause deadlock

09-Aug-2023: Changes in document version v11.0

ID	Status	Area	Category	Summary
3018109	New	Programmer	Category B	QoS QPC can be corrupted in 2xREQ configs

30-Jun-2023: Changes in document version v10.0

ID	Status	Area	Category	Summary
2900369	Updated	Programmer	Category B	CHI or AXI CMN configuration accesses can deadlock when the APB-only configuration access feature is enabled
2909130	Updated	Programmer	Category B	Data Cache Clean operations by VA to the point of Persistence to remote chip memory can cause a deadlock
2951654	New	Programmer	Category B	HN-I Physical Memory ordering can be violated with larger tracker depths

29-Apr-2023: Changes in document version v9.0

ID	Status	Area	Category	Summary
2900369	New	Programmer	Category B	CHI or AXI CMN configuration accesses can deadlock when the APB-only configuration access feature is enabled
2909130	New	Programmer	Category B	Data Cache Clean operations by VA to the point of Persistence to remote chip memory can cause a deadlock

20-Jan-2023: Changes in document version v8.0

ID	Status	Area	Category	Summary
2822447	New	Programmer	Category B	Remote chip DVM Sync operations may be incorrectly suppressed

07-Sep-2022: Changes in document version v7.0

ID	Status	Area	Category	Summary
2473100	Updated	Programmer	Category B	Multi-chip SMP DVM operations can cause hang
2418894	Updated	Programmer	Category C	CCG CCLA PMU events cannot be counted correctly
2732981	New	Programmer	Category C	RAS HN-S, HN-I and SBSX ERRGSR registers do not capture correct device instance information

13-Jul-2022: Changes in document version v6.0

ID	Status	Area	Category	Summary
2473100	New	Programmer	Category B	Multi-chip SMP DVM operations can cause hang

18-Feb-2022: Changes in document version v5.0

ID	Status	Area	Category	Summary
2418894	New	Programmer	Category C	CCG CCLA PMU events cannot be counted correctly

07-Jan-2022: Changes in document version v4.0

No new or updated errata in this document version.

01-Oct-2021: Changes in document version v3.0

No new or updated errata in this document version.

03-May-2021: Changes in document version v2.0

ID	Status	Area	Category	Summary
2128441	New	Programmer	Category B	Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic
2125871	New	Programmer	Category C	HN-I RAS syndrome registers do not capture correct opcode

15-Dec-2020: Changes in document version v1.0

No errata in this document version.

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
3037722	Programmer	Category A	Multi-chip SMP deadlock in the presence of CPU traffic when CCG HA_REQ_PASS_BUFF_DEPTH < RA_NUM_REQS	r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3	Open
2473100	Programmer	Category B	Multi-chip SMP DVM operations can cause hang	r0p0, r1p0, r2p0	r3p0
2128441	Programmer	Category B	Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic	r0p0	r1p0
2900369	Programmer	Category B	CHI or AXI CMN configuration accesses can deadlock when the APB-only configuration access feature is enabled	r1p0, r2p0, r3p0, r3p1	r3p2
3018109	Programmer	Category B	QoS QPC can be corrupted in 2xREQ configs	r3p0, r3p1, r3p2	r3p3
2822447	Programmer	Category B	Remote chip DVM Sync operations may be incorrectly suppressed	r3p0, r3p1, r3p2, r3p3	Open
2909130	Programmer	Category B	Data Cache Clean operations by VA to the point of Persistence to remote chip memory can cause a deadlock	r0p0, r1p0, r2p0, r3p0, r3p1	r3p2
2951654	Programmer	Category B	HN-I Physical Memory ordering can be violated with larger tracker depths	r3p0, r3p1	r3p2
3013638	Programmer	Category B	Write Stash can cause multi-copy atomicity issue	r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3	Open
3033917	Programmer	Category B	StashOnce*Sep operations generated by CPU's PRFM PLD/PST L3 instructions targeting remote chip memory can cause a deadlock	r0p0, r1p0, r2p0, r3p0, r3p1	r3p2
3013641	Programmer	Category B (rare)	Incorrect TagMatch response on partial writes with MTE Match	r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3	Open
2125871	Programmer	Category C	HN-I RAS syndrome registers do not capture correct opcode	r0p0	r1p0

ID	Area	Category	Summary	Found in versions	Fixed in version
3015226	Programmer	Category C	Debug reads with simultaneous coherent traffic or dynamic power transitions can cause deadlock	r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3	Open
2418894	Programmer	Category C	CCG CCLA PMU events cannot be counted correctly	r2p0	r3p0
2732981	Programmer	Category C	RAS HN-S, HN-I and SBSX ERRGSR registers do not capture correct device instance information	r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3	Open

Errata descriptions

Category A

3037722
Multi-chip SMP deadlock in the presence of CPU traffic when CCG HA_REQ_PASS_BUFF_DEPTH < RA_NUM_REQS

Status

Affects: CMN-700
Fault Type: Programmer CAT-A
Fault Status: Present in r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3. Open.

Description

High-bandwidth CPU traffic targeting a remote chip can result in deadlocks.

Configurations Affected

All configurations where a CCG node on one side of the CML_SMP link has a HA_REQ_PASS_BUFF_DEPTH value less than the RA_NUM_REQS value of the CCG node on the other side of the CML_SMP link.

Conditions

High bandwidth CPU traffic targeting the remote chip.

Implications

Deadlocks in the presence of CPU traffic.

Workaround

No workarounds.

Category A (rare)

There are no errata in this category.

Category B

2473100
Multi-chip SMP DVM operations can cause hang

Status

Affects: CMN-700
Fault Type: Programmer CatB
Fault Status: Present in r0p0, r1p0, r2p0. Fixed in r3p0.

Description

DVM operations may hang in the presence of other traffic targeting remote chips in CMN SMP configurations.

Configurations Affected

Any multi-chip SMP CMN configuration.

Conditions

DVM operations and non-DVM op transactions targeting a remote chip in SMP configurations.

Implications

If the conditions are met, DVM operations might not complete, which might cause deadlocks.

Workaround

Disable CML Early DVM completions by writing 1'b0 to por_ccg_ra_aux_ctl.dvm_earlycomp_en

Also, do not change the following register values from the default settings:

- por_ccg_ra_ccprtcl_link0_ctl. lnk0_send_compack: Default is 1'b0
- por_ccg_ha_ccprtcl_link0_ctl. lnk0_send_compack: Default is 1'b0

Note

This might impact cross-chip DVM performance.

2128441
Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r0p0. Fixed in r1p0

Description

High-bandwidth CPU and PCIe traffic targeting a remote chip can result in data corruption or hangs.

Configurations Affected

All configurations that have PCIe RNI instantiated in CCG.

Conditions

High bandwidth CPU and PCIe traffic targeting the remote chip.

Implications

Data corruption and/or an eventual hang in the presence of CPU and PCIe traffic.

Workaround

Program por_ccg_ha_cxprtcl_link0_ctl.lnk0_num_reqcrds to a value of 4'h3 which allocates only 75% of the available credits to link 0.

2900369
CHI or AXI CMN configuration accesses can deadlock when the APB-only configuration access feature is enabled

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r1p0, r2p0, r3p0, r3p1. Fixed in r3p2.

Description

CMN can be configured to only allow APB configuration access. Transactions that target the CMN configuration space via CHI or AXI, return zero data for reads and writes are dropped.

Configurations affected

Any CMN-700 configuration that enables the APB-only configuration mode via the por_abp_only_access configuration register.

Conditions

- APB-only mode enabled via the por_abp_only_access configuration register AND
- CHI transactions targeting the CMN configuration register space within the CMN PERIPHBASE offset range OR
- AXI transactions targeting the CMN configuration register space within the CMN PERIPHBASE offset range

Implications

Deadlocks may occur if the conditions are met, read or write transactions may not complete.

Workaround

Configure the CMN System Address Map to not target HN-D for the CMN configuration address space within the CMN PERIPHBASE offset range.

3018109
QoS QPC can be corrupted in 2xREQ configurations

Status

Affects: CMN-700
Fault Type: Programmer Cat-B
Fault Status: Present in r3p0, r3p1, r3p2. Fixed in: r3p3.

Description

The QoS QPC value can be corrupted in 2xREQ configurations. The QPC value can be overridden to zero depending on the location of the RN-F, RN-I, RN-D, or CCG device within the mesh.

Configurations affected

Configurations with 2xREQ.

Conditions

The following conditions must all be met:

- The RN-F (pass-through mode only), RN-I, RN-D, or CCG issues a transaction request with a non-zero QoS QPC value
- The crosspoint incorrectly overrides the QPC value to zero

Implications

QoS functionality will be impaired due to the zero QPC value, cannot use RN-F pass-through QPC or any RN-I, RN-D, or CCG QoS regulator functionality.

Workarounds

Use the following workarounds to prevent QoS QPC value corruption in 2xREQ configurations:

- Configure to use the RN-F QoS regulators in the MXP instead of the pass-through value from the RN-F. Note that Arm CMN-700 generation CPUs drive at a static 14 QPC value.
- Update the HN-F QoS threshold logic to comprehend the zero values from RN-I, RN-D and CCG.

2822447
Remote chip DVM Sync operations may be incorrectly suppressed

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r3p0, r3p1, r3p2,r3p3. Open.

Description

The CMN-700 DVM Op and Sync optimizations enable filtering Outer-Shareable DVM Ops and suppressing DVM Syncs targeting remote chips in SMP configurations. DVM Syncs can be suppressed if no older DVM Ops were sent to remote chips since the last DVM Sync. DVM Syncs might be incorrectly suppressed even when DVM Ops were sent to the remote chip.

Configurations affected

CMN-700 SMP configurations with the DVM Op and Sync optimization features enabled.

Conditions

The incorrect suppression of DVM Syncs targeting remote chips can occur if all of the following conditions are met:

- Configuration bits por_dn_cfg_ctl.broadcast_dvmop_{outer,inner} != 2'b11 (enables DVM Op Outer-Shareable filtering feature) AND
- Local DVM Syncs issued from a CPU on chip0 AND,
- Incoming remote DVM Syncs issued from remote chip1 AND
- DVM Op(s) issued to remote chip1

Implications

The DVM Sync to remote chip1 may not be issued resulting in DVM coherence issues.

Workaround

Do not enable the DVM Op and Sync optimization features, disabled by default. Do not modify por_dn_cfg_ctl.broadcast_dvmop_{outer,inner}.

2909130
Data Cache Clean operations by VA to the point of Persistence to remote chip memory can cause a deadlock

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r0p0, r1p0, r2p0, r3p0, r3p1. Fixed in r3p2.

Description

Under specific timing conditions, the execution of a Data Cache Clean sequence by VA to the point of Persistence or Point of Deep Persistence instructions that are targeting memory on a remote chip can cause a deadlock.

Configurations affected

Any multi-chip SMP CMN configuration where the CPUs and SOC support the CHI BROADCASTPERSIST attribute.

Conditions

CPU sends a sequence of DC CVAP instructions targeting memory on the remote chip with the same GROUPID:

- DC CGDVADP
- DC CGDVAP
- DC CGVADP
- DC CGVAP
- DC CVADP
- DC CVAP

Implications

A deadlock can occur if the conditions are met, under specific micro-architectural and timing conditions.

Workarounds

1. Set the CPU BROADCASTPERISIST input pin to 1'b0 OR
2. The CMN Persist Response Tracker can be disabled by setting por_ccg_ra_aux_ctl[13] to 1'b0. Note that this may have performance implications.

2951654
HN-I Physical Memory ordering can be violated with larger tracker depths

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r3p0, r3p1. Fixed in r3p2.

Description

HN-I devices support a Physical Memory mode, which implements Arm Normal Memory ordering requirements. Address hazard ordering may not be maintained when HN-I Physical Memory mode is enabled with larger tracker depth settings, which can result in same address transaction re-ordering on the HN-I AXI interface.

Configurations affected

CMN-700 configurations with HN-I, HN-D, HN-P, HN-T, or HN-V with configurations where NUM_RRT_REQS + NUM_AXI_REQS > 128

Conditions

The following conditions must all be met:

- HN-I devices (includes HN-D, HN-P, HN-T, or HN-V) configured with NUM_RRT_REQS + NUM_AXI_REQS > 128
- Physical Memory mode is enabled (por_hni_sam_addrregion<n>_cfg.physical_mem_en=1) for address region n
- 2 transactions in flight to AXI with overlapping addresses

Implications

Data corruption: a younger read might return stale data if following behind an older write to the same address

Workaround

Do not enable Physical Memory mode when using deeper tracker, which results in Device Memory ordering behavior and might have performance implications.

3013638
Write Stash can cause multi-copy atomicity issue

Status

Affects: CMN-700
Fault Type: Programmer Cat-B
Fault Status: Present in r0p0,r1p0, r2p0, r3p0, r3p1, r3p2, r3p3. Open.

Description

CHI and AXI Write Stash operations can incorrectly get early completion before snooping is complete causing multi-copy atomicity issues.

For example, an RN-I or RN-D PCI MSI write issued after a Write Stash can result in the CPU having an older or stale copy of the Write Stash data at the time of the MSI interrupt.

Another example is an RN-I or RN-D write flag issued after completion of the Write Stash, the CPU can observe the flag update before the Write Stash data is updated.

Note that Arm CPUs do not issue Write Stash transactions.

Configurations affected

Any CMN configuration.

Conditions

This erratum occurs when the following conditions are met:

- RN-I or RN-D issues AXI Write Stash transaction with a valid StashNID targeting a CPU cache
- RN-I or RN-D issues another AXI transaction after receiving the completion for the Write Stash, for example PCIE MSI write or write to flag address
- The Stash CPU can observe the results of the second transaction above before the Write Stash data is updated for the first

Implications

If the conditions are met, Write Stash might receive early completion while the Stash CPU still has an old copy causing multi-copy atomicity issues.

Workaround

The workaround is to send the result in Stash to the SLC instead of the CPU cache, by disabling stash snooping using cmn_hns_cfg_ctl.hns_stash_snp_dis for r2p0 and beyond configurations, por_hnf_cfg_ctl.hnf_stash_snp_dis for r1p0 configurations, or por_hnf_aux_ctl.hnf_stash_disable for r0p0 configurations.

3033917
StashOnce*Sep operations generated by CPU's PRFM PLD/PST L3 instructions targeting remote chip memory can cause a deadlock

Status

Affects: CMN-700
Fault Type: Programmer CAT-B
Fault Status: Present in r0p0, r1p0, r2p0, r3p0, r3p1. Fixed in r3p2.

Description

Under specific timing conditions, the execution of a PRFM PLD/PST L3 sequence by VA to the remote chip can cause a deadlock.

Configurations affected

Any multi-chip SMP CMN configuration where the CPUs and SOC support software prefetching, and the software prefetch instructions generate StashOnce*Sep CHI requests to CMN.

Conditions

CPU executes a sequence of PRFM PLD/PST L3 instructions targeting memory on the remote chip, generating StashOnce*Sep requests with the same REQ.StashGroupID.

Implications

A deadlock can occur if the conditions are met, under specific micro-architectural and timing conditions.

Workarounds

Disable the StashOnce*Sep flow on the CML_SMP link by setting por_ccg_ra_aux_ctl.dis_stash_sep_prop = 1'b1.

Category B (rare)

3013641
Incorrect TagMatch response on partial writes with MTE Match

Status

Affects: CMN-700
Fault Type: Programmer Cat-B (rare)
Fault Status: Present in r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3. Open.

Description

Partial Write requests with MTE TagOp Match can cause an incorrect TagMatch response

Configurations affected

Any configuration with HN-F devices that use MTE

Conditions

This erratum occurs when the following conditions are met:

- Non-Arm CPU issues non-allocating WriteUniquePtl with TagOp=Match and Tag=<partial>
- The System Level Cache has dirty data but without MTE Tag
- HN-F incorrectly responds with no TagMatch for the WriteUniquePtl

Implications

If the conditions are met, MTE Write Partial transactions that require TagMatch response can be incorrect. Partial write transactions might not respond with TagMatch.

Workarounds

Use the following workarounds to recieve the correct TagMatch response for partial write transactions:

- CMN-700 r0p0, r1p0, r2p0: No workaround required, Arm CPUs do not issue Write Partial with TagMatch
- CMN-700 r3pX: Set cmn_hns_cfg_ctl.hns_mte_no_sn_match to enable local match for non-Arm CPUs

Category C

2125871
HN-I RAS syndrome registers do not capture correct opcode

Status

Affects: CMN-700
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The OPCODE field in the HN-I por_hni_errmisc RAS Syndrome register does not correctly capture the new REQ opcodes introduced in CHI-E.

Configurations Affected

All CMN-700 configurations that use RAS error logging.

Conditions

A RAS error triggered by a new CHI-E transaction that causes the syndrome to be captured in the por_hni_errmisc register on a transaction processed by HN-I/P/D/V/T.

Implications

A read of the por_hni_errmisc.OPCODE field may return an incorrect opcode. The opcode does not properly reflect an error on a CHI-E opcode that has bit [6] set.

Workaround

RAS handler and software can use the following table indicating which por_hni_errmisc.OPCODE values are affected by aliasing due to this issue. If a RAS error involves opcodes listed as **Yes**, software can indicate that either opcode could have been the actual opcode involved in the error. Note that some cases with opcode[6]=0 are Reserved in the *CHI-E Specification*.

CHI-E REQ Opcodes			
Opcode[5:0]	Opcode[6]=0	Opcode[6]=1	Can Opcode[6]=1 RAS error happen at HN-X?
0x01	ReadShared	MakeReadUnique	**Yes**
0x02	ReadClean	WriteEvictOrEvict	No
0x03	ReadOnce	WriteUniqueZero	**Yes**
0x04	ReadNoSnp	WriteNoSnpZero	No
0x07	ReadUnique	StashOnceSepShared	No
0x08	CleanShared	StashOnceSepUnique	No
0x0C	MakeUnique	ReadPreferUnique	**Yes**
0x10	Reserved	WriteNoSnpFullCleanSh	No
0x11	ReadNoSnpSep	WriteNoSnpFullCleanInv	No
0x12	Reserved	WriteNoSnpFullCleanSh-PerSep	No
0x14	DVMOp	WriteUniqueFullCleanSh	**Yes**
0x16	Reserved (WriteCleanPtl)	WriteUniqueFullCleanSh-PerSep	**Yes**
0x18	WriteUniquePtl	WriteBackFullCleanSh	**Yes**
0x19	WriteUniqueFull	WriteBackFullCleanInv	**Yes**
0x1A	WriteBackPtl	WriteBackFullCleanSh-PerSep	**Yes**
0x1C	WriteNoSnpPtl	WriteCleanFullCleanSh	**Yes**
0x1E	Reserved	WriteCleanFullCleanSh-PerSep	**Yes**
0x20	WriteUniqueFullStash	WriteNoSnpPtlCleanSh	No
0x21	WriteUniquePtlStash	WriteNoSnpPtlCleanInv	No
0x22	StashOnceShared	WriteNoSnpPtlCleanSh-PerSep	No
0x24	ReadOnceCleanInvalid	WriteUniquePtlCleanSh	**Yes**
0x26	ReadNotSharedDirty	WriteUniquePtlCleanSh-PerSep	**Yes**

3015226
Debug reads with simultaneous coherent traffic or dynamic power transitions can cause deadlock

Status

Affects: CMN-700
Fault Type: Programmer Cat-C
Fault Status: r0p0, r1p0, r2p0, r3p0, r3p1, r3p2, r3p3. Open.

Description

HN-F System Level Caches (SLC) and Snoop Filter (SF) Debug Reads with simultaneous coherent traffic or dynamic power retention transitions can cause a deadlock.

Configurations affected

Any configuration.

Conditions

This erratum occurs when one of the following conditions are met:

- Coherent transactions that require HN-F Snoop Filter allocation while performing SLC or SF debug read
- Dynamic retention mode is enabled while performing a SLC or SF debug read

Implications

A deadlock can occur if the conditions are met. Note that expected usage is performing the Debug Reads in the absence of traffic since traffic can change the state of the RAMs.

Workaround

Use the following workarounds to prevent a deadlock:

- Stop CPU (RN-F) and IO (RN-I) coherent traffic before issuing Debug Reads
- Disable Dynamic retention power transitions via cmn_hns_ppu_pwpr.dyn_en = 1'b0 (reset value) for r2p0 and beyond configurations, or por_hnf_ppu_pwpr.dyn_en = 1'b0 (reset value) for r1p0 and r0p0 configurations.

2418894
CCG CCLA PMU events cannot be counted correctly

Status

Affects: CMN-700
Fault Type: Programmer CAT-C
Fault status: Present in r2p0. Fixed in r3p0.

Description

The CCG PMU events cannot be counted correctly for CCG configurations with PCIE_ENABLE parameter set

Configurations affected

CMN configurations that include CCG with PCIE_ENABLE parameter set

Conditions

Programming CMN CCG CCLA PMU events to be counted.

Implications

CCG CCLA PMU events cannot be counted correctly. This may reduce the ability to analyze CXS link efficiency for multi-chip traffic.

The following events will not be counted correctly:

- 8'h21: LA_RX_CXS : number of RX CXS beats
- 8'h22: LA_TX_CXS : number of TX CXS beats
- 8'h23: LA_RX_CXS_AVG_SIZE : average size of RX CXS beats
- 8'h24: LA_TX_CXS_AVG_SIZE : average size of TX CXS beats
- 8'h25: LA_TX_CXS_LCRD_BACKPRESSURE : CXS backpressue due to lack of CXS credits
- 8'h26: LA_LINK_CRDBUF_OCC : CCLA RX RAM buffer occupany
- 8'h27: LA_LINK_CRDBUF_ALLOC: CCLA RX RAM buffer allocation

Workaround

No workaround necessary.

2732981
RAS HN-S, HN-I and SBSX ERRGSR registers do not capture correct device instance information

Status

Affects: CMN-700
Fault Type: Programmer Category C
Fault Status: r0p0, r1p0, r2p0, r3p0, r3p1, r3p2,r3p3. Open.

Description

The CMN Error Group Status Registers (ERRGSR) capture device instance error information for RAS events. The registers indicate the device instance within a device group. The registers are not updated correctly for the HN-S, HN-I and SBSX device groups, so cannot be used to determine the device instances for RAS events.

Configurations Affected

All CMN-700 configurations that use RAS error logging.

Conditions

A RAS event triggered by an HN-S, HN-I or SBSX device.

Implications

Software cannot use the HN-S, HN-I or SBSX ERRGSR registers.

Workaround

The RAS handler must read the individual HN-S, HN-I and SBSX instance RAS logging registers when RAS interrupts occur.