ARM PrimeCell
Multiport Memory Controller (PL176)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p1 of PL176 64-Bit Universal Mem Controller

Proprietary notice

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- The document title
- The documents number
- The page number(s) to which your comments refer
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General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

23 Jan 2006: Changes in Document v2

Page	Status	ID	Cat	Summary
13	New	372514	Cat 3	Memory access failures if tRAS is set smaller than RAS delay

13 Jan 2006: Changes in Document v1

Page	Status	ID	Cat	Summary
9	New	271160	Cat 2	32-bit AHB memory port lockup issue
12	New	282212	Cat 3	Bustest Makefile References GXI tests which do not exist
11	New	254910	Cat 3	Unable to use hardware to disable external clock for DDR SDRAM
10	New	209715	Cat 3	The MPMCDYCS5CASDLY does not configure all bits for CAS delay
14	New	312849	Doc	PL176 TRM incorrectly states Mbit for Mbyte

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0-00LTD0	r0p1-00LTD0
271160	Cat 2	32-bit AHB memory port lockup issue	X	X
209715	Cat 3	The MPMCDYCS5CASDLY does not configure all bits for CAS delay	X	
254910	Cat 3	Unable to use hardware to disable external clock for DDR SDRAM	X	X
282212	Cat 3	Bustest Makefile References GXI tests which do not exist		X
372514	Cat 3	Memory access failures if tRAS is set smaller than RAS delay	X	X
312849	Doc	PL176 TRM incorrectly states Mbit for Mbyte		X

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

271160: 32-bit AHB memory port lockup issue

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Cat 2, Present in: r0p0-00LTD0,r0p1-00LTD0, Open. Updated in this document.

Description

There is an issue with the 32-bit Slave Interface. In Read Cache Enabled mode, when a BYTE wide WRAP4 READ transaction is initiated and the transaction results in an address wrap, the 32 bit slave no longer treats this as a buffered transaction.

Furthermore, a new request is not raised to the memory controller.

This causes that particular 32-bit slave interface to lock up.

This lock up prevents re-arbitration and as a consequence all the AHB's get wait stated indefinitely.

Implications

Lock up of the memory controller preventing any memory accesses to all masters in the system.

Workaround

None

Errata - Category 3

209715: The MPMCDYCS5CASDLY does not configure all bits for CAS delay

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Cat 3, Present in: r0p0-00LTD0, Fixed in r0p1-00LTD0. Unchanged in this document.

Description

The MPMCDYCS5CASDLY[2:0] tie-off inputs only specify the upper 3 bits of the 4-bit MPMCDynamicRasCas1 register. The reset value of bit 0 is '1', so for any tie-off value, the reset value of the CAS latency for chip select 1 will be MPMCDYCS5CASDLY[2:0] + 0.5.

Implications

none

Workaround

This does not cause a functional issue for SDR SyncFlash booting as only DDR devices use the 0.5 value.

During initialisation, the 0.5 value may be programmed by software to the correct value.

254910: Unable to use hardware to disable external clock for DDR SDRAM

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Cat 3, Present in: r0p0-00LTD0,r0p1-00LTD0, Open. Unchanged in this document.

Description

The hardware is unable to disable the external clock to DDR SDRAM when they are put into self refresh mode.

The correct functionality is:

CKE - clock Enable.

CS - Clock Stop (bit1)

SCC - Self Refresh Clock Stop (bit 3)

CKE	CS	SCC	CLOCK-STATUS
1	x	x	RUN
0	1	1	RUN
0	0	1	STOP
0	0	0	STOP
0	1	0	STOP

This is not an issue for SDR SDRAM, and software is able to disable the clock for DDR.

Implications

none

Workaround

None

282212: Bustest Makefile References GXI tests which do not exist

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Cat 3, Present in: r0p1-00LTD0, Open. Unchanged in this document.

Description

The verification/bustest makefile for the PL176 references some gxi tests.

The tests themselves have not been shipped but are only referenced

Page 170, Figure 5.4-1 of the PL176 Design Manual also mentions GXI and does not mention it anywhere else

Implications

None

Workaround

These can just be ignored or removed by deleting them from the makefile

372514: Memory access failures if tRAS is set smaller than RAS delay

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Cat 3, Present in: r0p0-00LTD0,r0p1-00LTD0, Open. New in this document.

Description

If you program the value of MPMCDynamictRAS to be smaller than the RAS delay value in the MPMCDynamicRasCasX register then memory access errors occur.

Most, if not all memory devices, require MPMCDynamictRAS to be larger than RAS in the MPMCDynamicRasCasX register. Therefore this problem will not be encountered for most memory devices.

Implications

The value programmed into the MPMCDynamictRAS register must always be larger than the value programmed in the RAS field of the MPMCDynamicRasCasX register.

Workaround

When programming the memory controller ensure that MPMCDynamictRAS is larger than RAS in the MPMCDynamicRasCasX register.

Errata - Documentation

312849: PL176 TRM incorrectly states Mbit for Mbyte

Status

Affects: product PL176 64-Bit Universal Mem Con.

Fault status: Doc, Present in: r0p1-00LTD0, Open. Unchanged in this document.

Description

Technical Reference Manual ARM DDI 0269A.

Section 2.11, page 2-41 states: "The largest amount of memory that can be allocated to a single chip select is 256Mb."

In section C.4, page C-14, the external pad interface, the note for MPCMADDROUT[27:0] indicates that there is a 256Mb maximum per static memory bank.

Both of these should be MB (MBytes) not Mb (Mbits)

Implications

none

Workaround

none

Errata – Driver Software

There are no Errata in this Category