



SoC Bring-Up Using the Platform Configuration Editor PCE

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1. Overview

This tutorial shows how to use the Platform Configuration Editor (PCE) in Arm DS-5 Development Studio. By the end of this guide, you should be able to connect to an Arm-based System-on-Chip (SoC), use the PCE to detect its underlying system architecture and configure any missing elements of the system. By using the PCE, you will save time and avoid the pitfalls of manually creating debug configuration scripts.

2. Arm SoC Debug and Trace

In order to provide effective debug and trace support for a SoC, a debugger needs a certain amount of information. The debugger needs to know:

- Which devices are present in the SoC (including the type and configuration details of each device, and connection details such as CoreSight base address)
- How these devices relate or connect to each other (their topology)

DS-5 debugger can automatically detect most of this information. However, debugger sometimes fails to detect certain features. The information presented by the SoC may be incomplete or corrupted, or information may be missing because parts of the SoC are powered down, or devices inside the SoC may interfere with topology detection.

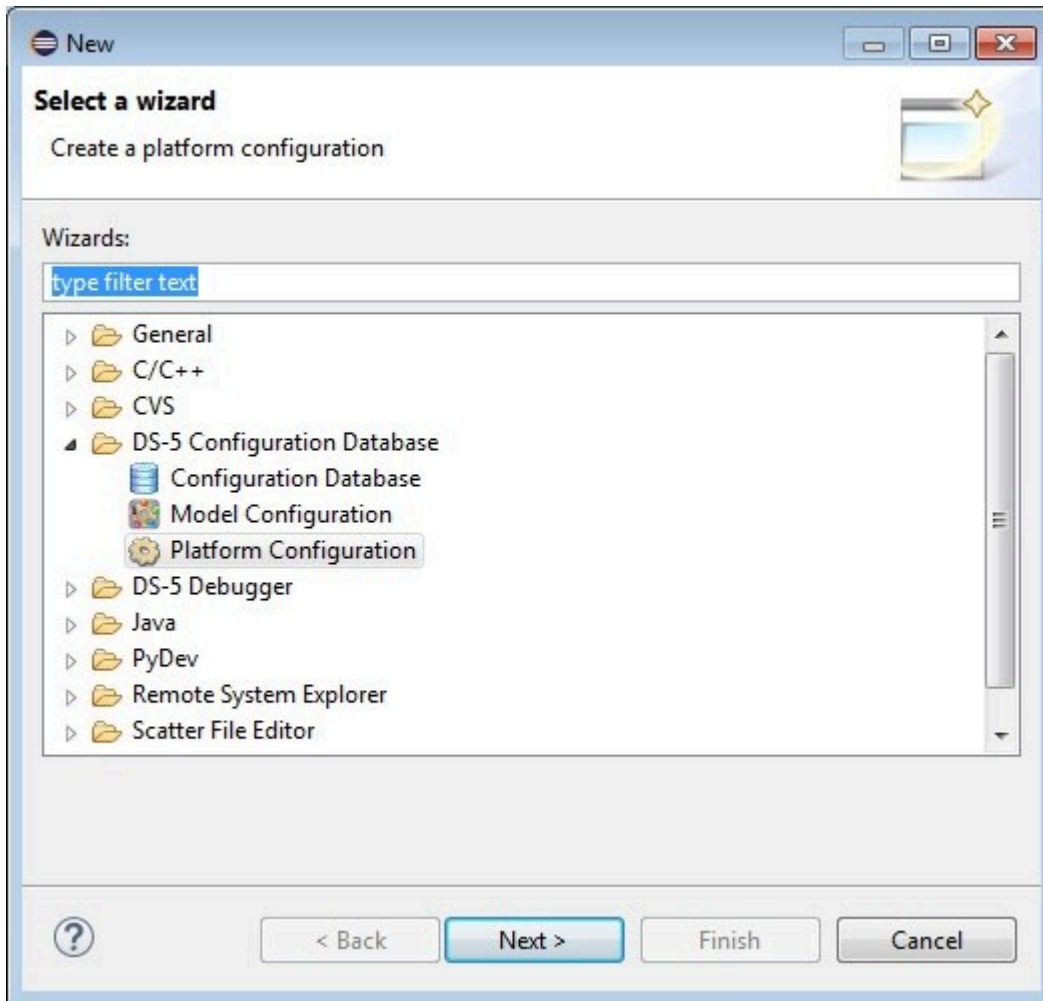
This means that a debugger often has to work with incomplete or incorrect information about a SoC. This can greatly affect the level of debug and trace functionality that the debugger can offer. The debugger could try to make assumptions based on its knowledge of other SoCs, but the flexibility of Arm-based designs means that these assumptions are often limited in their success. Often a CoreSight topology diagram is available, but we have to find some way to get the information in that topology diagram into the debugger.

3. How the PCE is Useful

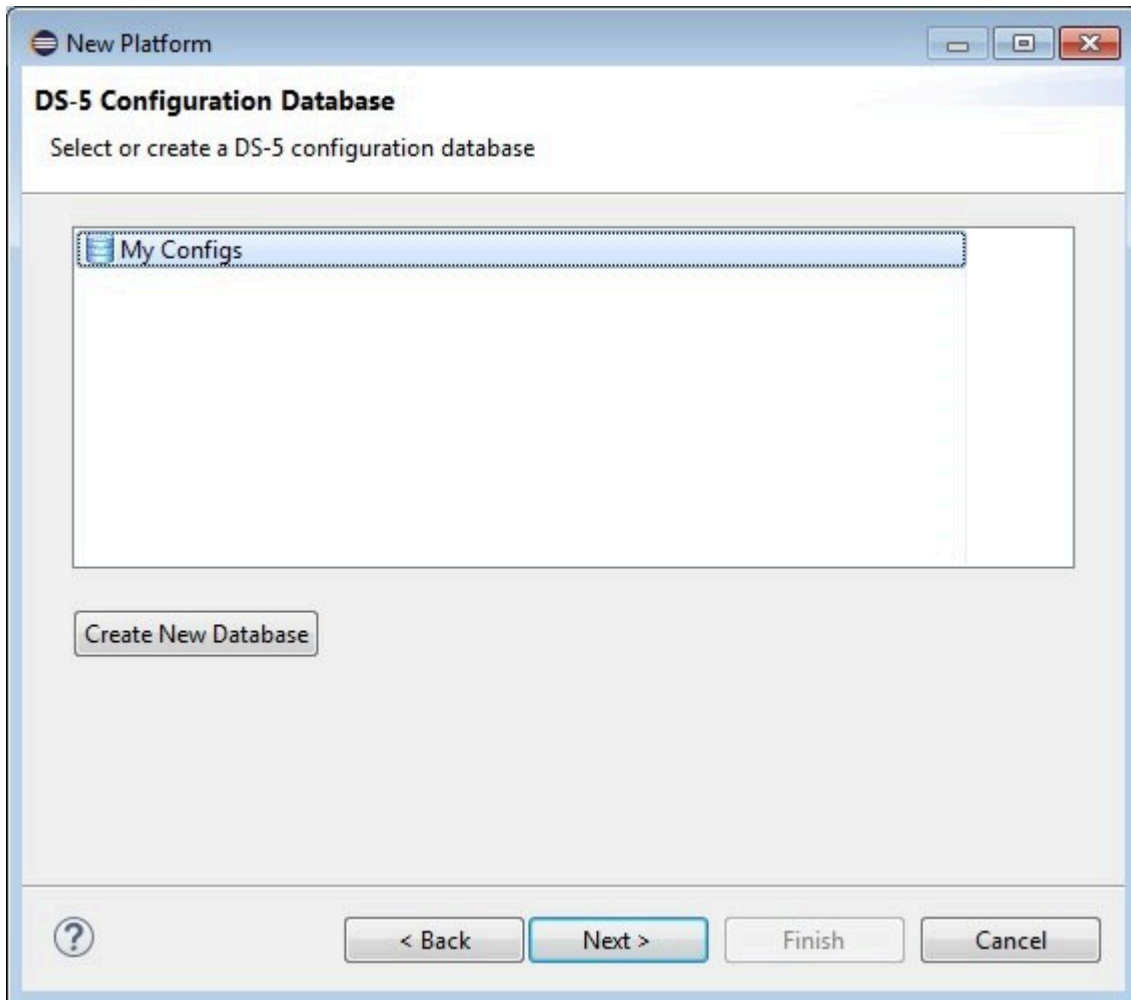
DS-5 contains Platform Configuration Editor (PCE), which provides a simple and flexible way to add platform configuration to DS-5 debugger. In this example, the PCE is used to bring-up a SoC that in the past has caused problems. The SoC contains a mix of Cortex-A and Cortex-M cores, and the device and topology information that it presents is incomplete.

4. SoC Bring-Up in DS-5

The PCE is launched by selecting File > New > Other... from the DS-5 menu and then selecting DS-5 Configuration Database > Platform Configuration:



All DS-5 platform configurations have to be stored in a configuration database. Select a configuration database, or create a new one:



I need to give a manufacturer and platform name:

New Platform

Platform Information

Use this page to enter identification details for the platform.

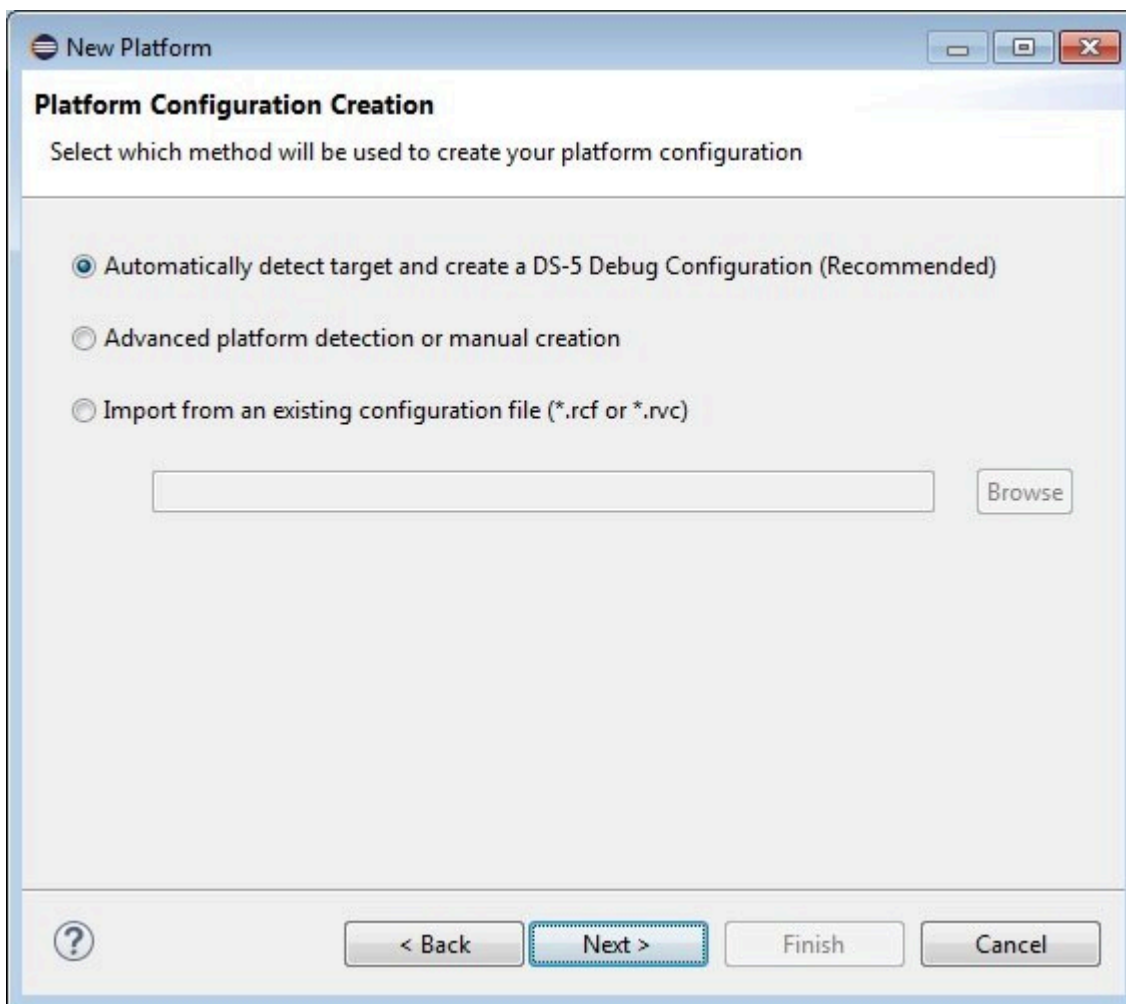
Platform Manufacturer: Imported

Platform Name: ProjectX

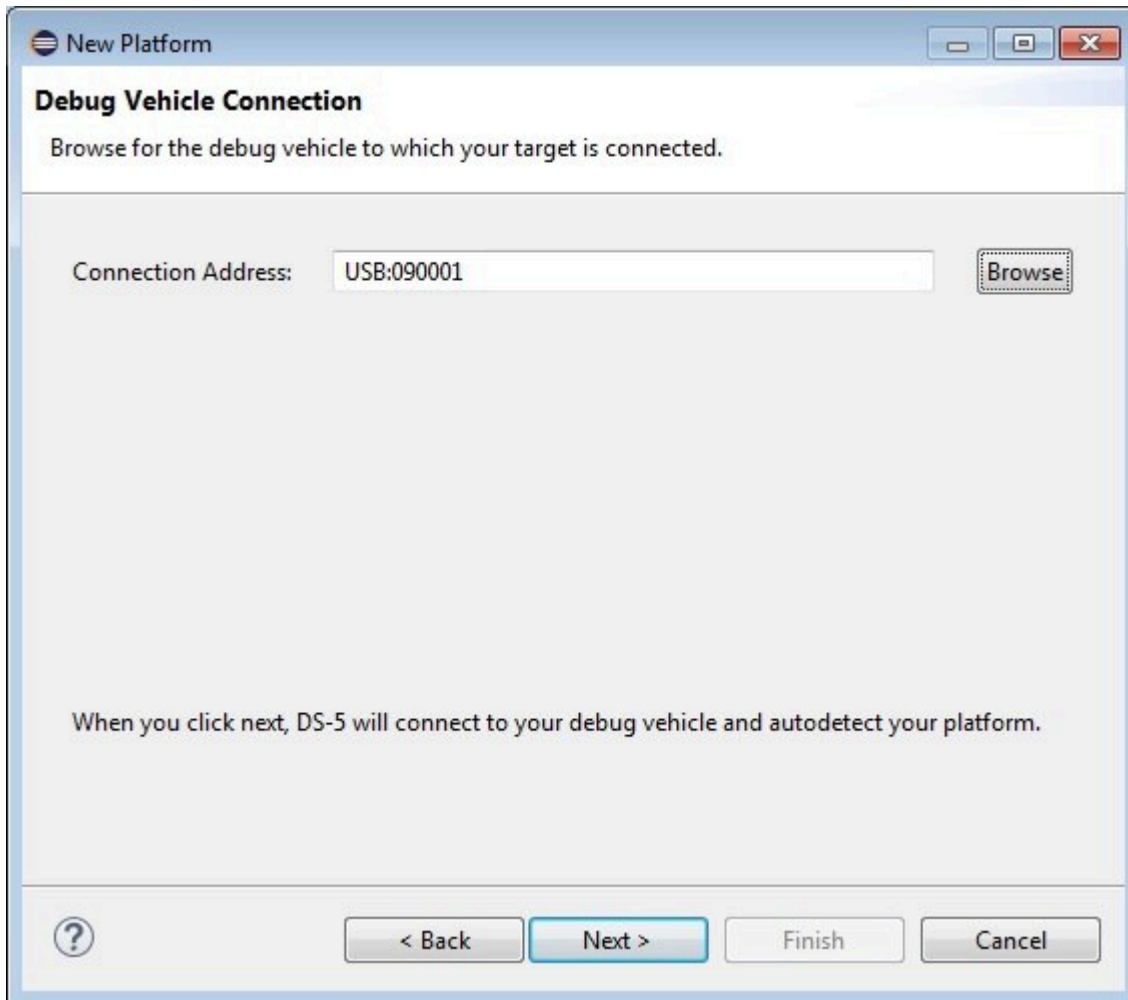
Platform Info URL:

? < Back Next > Finish Cancel

In the next step, there is a choice of workflows. I would like DS-5 to do as much as possible, I don't want to get involved in manual device addition or advanced configuration, and I don't have an existing file to import. So I can just accept the recommended workflow:

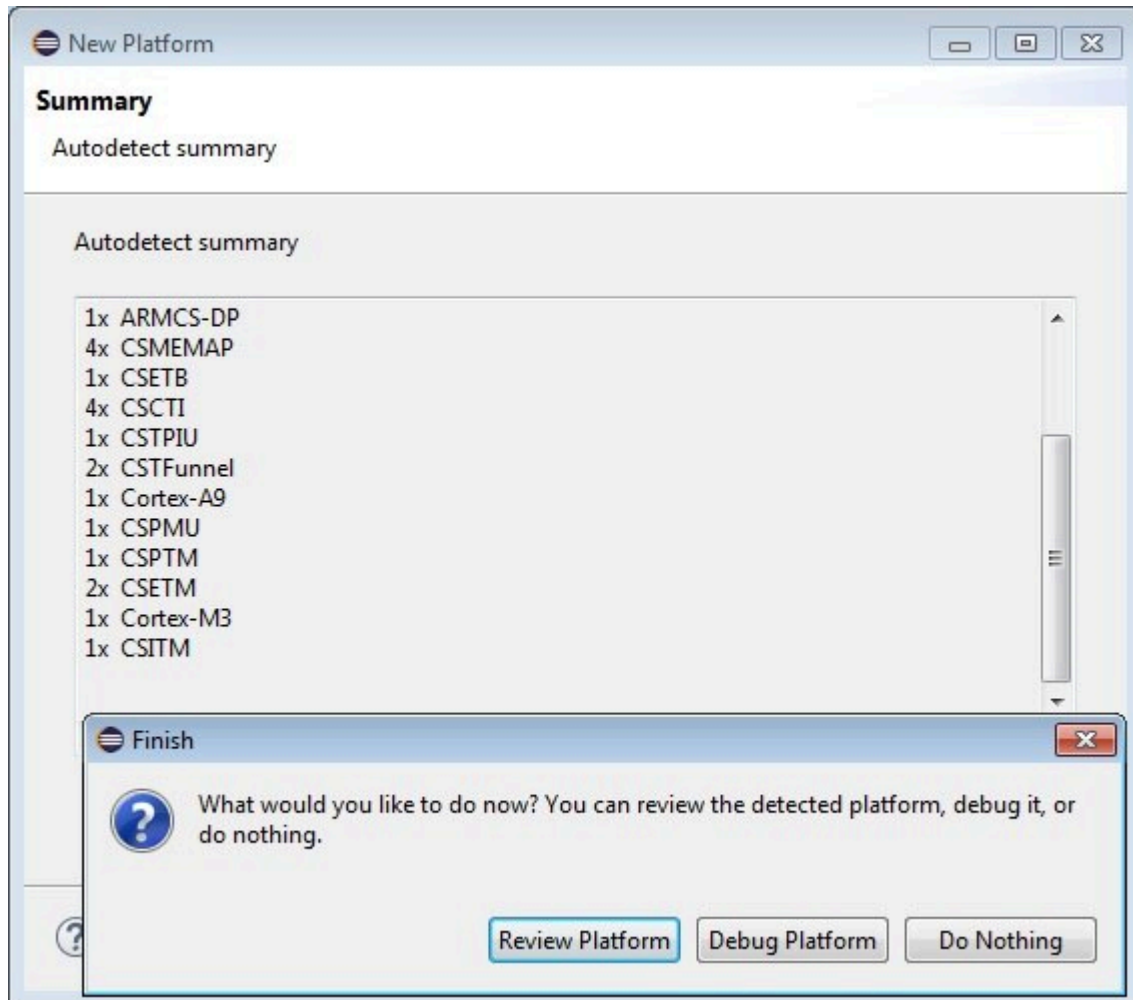


Once I've selected my DSTREAM unit, DS-5 will connect to the SoC and try to read all the information it needs for debug and trace:



After DS-5 has gathered all the information it can from the SoC, I'm presented with a simple summary of the devices that were found in the SoC. I can choose to do nothing now (DS-5 will save the platform configuration it's just generated, and I'll be able to connect and debug later) or I can debug straight away.

There is no need to rebuild the configuration database. That has already been done and represents a simplification over earlier DS-5 releases. The generated platform configuration will be the best that DS-5 can give from the information it could acquire from the SoC, so there may be missing functionality (particularly trace).



From this device summary, I can see a Cortex-A9 and a Cortex-M3. When I try to debug the target, I find that debug works well for both cores, but I only have trace options for the Cortex-A9. I don't have the ability to configure and collect trace for the Cortex-M3, so it looks like DS-5 could not acquire all the information it needed from the SoC. When I review the platform I can see this device summary:

RDDI ID	Device Name	Device Type	Device Family	Device Class	AP Index	Base Address
1	UNKNOWN_6_0	UNKNOWN_6	-	-	-	-
2	UNKNOWN_8_0	UNKNOWN_8	-	-	-	-
3	UNKNOWN_5_0	UNKNOWN_5	-	-	-	-
4	ARMCS-DP_0	ARMCS-DP	CoreSight	DebugPort	-	-
5	CSMEMAP_0	CSMEMAP	CoreSight	AccessPort	0	-
6	CSMEMAP_1	CSMEMAP	CoreSight	AccessPort	1	-
7	CSETB_0	CSETB	CoreSight	TraceSink	1	0x60641000
8	CSCTI_0	CSCTI	CoreSight	Link	1	0x60642000
9	CSTPIU_0	CSTPIU	CoreSight	TraceSink	1	0x60643000
10	CSTFunnel_0	CSTFunnel	CoreSight	Link	1	0x60644000
11	CSTFunnel_1	CSTFunnel	CoreSight	Link	1	0x60645000
12	Cortex-A9_0	Cortex-A9	Cortex	CoreExecutable	1	0x60670000
13	CPMU_0	CPMU	CoreSight	TraceSource	1	0x60671000
14	CSCTI_1	CSCTI	CoreSight	Link	1	0x60672000
15	CSPTM_0	CSPTM	CoreSight	TraceSource	1	0x60673000
16	CSETM_0	CSETM	CoreSight	TraceSource	1	0x607FA000
17	CSCTI_2	CSCTI	CoreSight	Link	1	0x607FB000
18	CSMEMAP_2	CSMEMAP	CoreSight	AccessPort	2	-
19	CSMEMAP_3	CSMEMAP	CoreSight	AccessPort	3	-
20	Cortex-M3_0	Cortex-M3	Cortex	CoreExecutable	3	0xE000ED00
21	CSETM_1	CSETM	CoreSight	TraceSource	3	0xE0041000
22	CSCTI_3	CSCTI	CoreSight	Link	3	0xE0042000
23	CSITM_0	CSITM	CoreSight	TraceSource	3	0xE0000000

The left pane shows my device hierarchy: I have a DAP, which provides access to a number of Access Ports (APs) of various types, which in turn provide access to the devices. Summary device details are shown in the right pane. If I select Component Connections I can view the topology information acquired from the SoC:

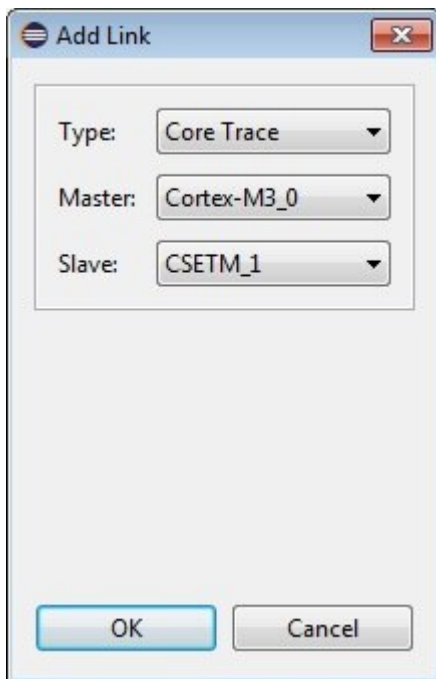
Master	Slave	Link Type	Link Details	Link Origin
CSTFunnel_0 (0x60644000)	CSETB_0 (0x60641000)	ATB	Master Interface = 0, Slave Interface = 0	Detected
CSTFunnel_1 (0x60645000)	CSTPIU_0 (0x60643000)	ATB	Master Interface = 0, Slave Interface = 0	Detected
CSPTM_0 (0x60673000)	CSTFunnel_0 (0x60644000)	ATB	Master Interface = 0, Slave Interface = 3	Detected
CSPTM_0 (0x60673000)	CSTFunnel_1 (0x60645000)	ATB	Master Interface = 0, Slave Interface = 3	Detected
CSETM_0 (0x607FA000)	CSTFunnel_0 (0x60644000)	ATB	Master Interface = 0, Slave Interface = 0	Detected
CSETM_0 (0x607FA000)	CSTFunnel_1 (0x60645000)	ATB	Master Interface = 0, Slave Interface = 0	Detected
Cortex-A9_0 (0x60670000)	CSPTM_0 (0x60673000)	CoreTrace	N/A	Detected
CSCTI_0 (0x60642000)	CSETB_0 (0x60641000)	CTITrigger	Trigger Out = 1	Detected
CSCTI_0 (0x60642000)	CSTPIU_0 (0x60643000)	CTITrigger	Trigger Out = 3	Detected
Cortex-A9_0 (0x60670000)	CSCTI_1 (0x60672000)	CTITrigger	Trigger DBGRESTART = 7	Detected
CSPTM_0 (0x60673000)	CSCTI_1 (0x60672000)	CTITrigger	Trigger In = 6	Detected
CSETM_0 (0x607FA000)	CSCTI_2 (0x607FB000)	CTITrigger	Trigger In = 6	Detected

Here I can see that the topology information acquired from the SoC is incomplete, and may also be corrupted. I can see two cores (Cortex-A9 and Cortex-M3) but three core trace macrocells (a PTM and two ETMs). One of the ETMs seems to be spare. It is connected to the trace funnels (at port 0) but doesn't seem to be connected to either of the cores.

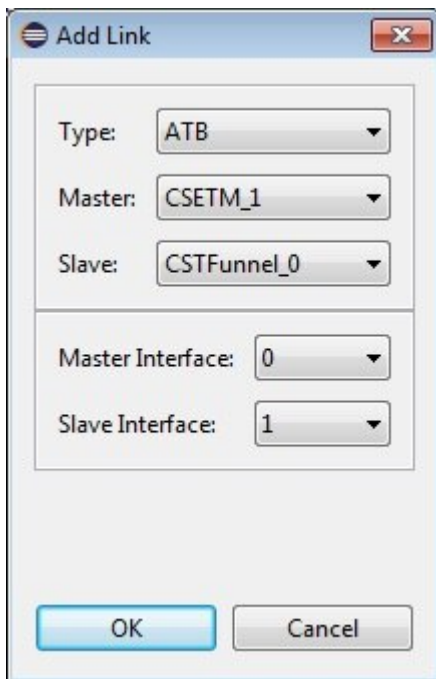
Topology for the Cortex-A9 looks pretty good. It is associated with both a PTM and a CTI, and the PTM is connected to the trace funnels (at port 3), then onwards to the ETB and the TPIU. This topology information was used by DS-5 when it generated the platform configuration, and the trace support that my DS-5 now offers for the Cortex-A9 works just fine. However there's

no topology information for the Cortex-M3, and this is reflected as a lack of functionality in my generated platform configuration.

Adding the link between the Cortex-M3 and its ETM is simple; we should assume that the core and its ETM are on the same AP:



However connecting the ETM to the funnels is more difficult because we have to choose a funnel port. We know that ports 0 and 3 are taken, but that leaves us with a choice of 6 ports. I could use information from a topology diagram if I had one but since I don't have the necessary information my only option is to try each port in turn:



When I save my changes, the platform configuration is automatically rebuilt and I can connect for debug and trace. In this case I'm lucky: port 1 is the first port I tried and it's the correct port, so now I have trace working for the Cortex-M3 as well as for the Cortex-A9. Although I had to enter some information manually I did not have to open the generated platform configuration and do any manual scripting, and this represents a significant improvement.

5. Summary

SoC bring-up in a debugger can be a tricky process that in the past might demand a level of debug expertise and some manual scripting. The PCE bring-up tool in DS-5 contains a number of important features that bring significant benefits to the SoC bring-up process:

- The PCE, with support for automatic detection of platform configuration information from SoC, reduces time and effort needed to bring up a new SoC.
- The PCE does not make assumptions about topology information that cannot be read from the SoC. This makes it easier for the user to spot the missing information, which can then be added.
- Manually adding missing topology information can be done through the main user interface, using simple dialogs. There's no need to hand-edit complex topology files.

6. Troubleshooting

As mentioned earlier, configuring an Arm-based SoC for bring-up can be tricky. Arm provides detailed technical support for our customers, so if you are finding it difficult to bring-up a particular device, don't hesitate to get in touch with us. You can [raise a support case here](#).