ARM CoreSight ™
CoreSight Design Kit for ARM11 (TM090)
Errata Notice

This document contains errata known at the date of issue in releases up to and including r2p0 of Coresight Design Kit for ARM11 (DK11)

Errata for the following components are listed separate errata documents:

TM917 : AHB Trace Macrocell

TM920 : CoreSight ETM11

TM093 : CoreSight Generic Parts

Proprietary notice

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- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Component Revisions

This document reports the errata for all revisions of CoreSight Design Kit for ARM11 (DK11). Each release of DK11 contains several CoreSight sub-components, the revisions of each sub-component for each specific DK11 release are documented in Table 1 below. The errata for these sub-components are listed in separate errata documents.

Component	CoreSight Design Kit for ARM11 Revision				
	r0p0	r0p1	r0p2	r1p0	r2p0
CoreSight Generic Parts	r0p0	r0p1	r0p2	r1p0	r2p0
AHB Trace Macrocell	r0p0	r0p1	r0p2	r0p3	r0p4
CoreSight ETM11	r0p0	r0p1	r0p2	r1p1	r1p1

Table 1 CoreSight Design Kit for ARM11 component revisions.

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

02 Oct 2009: Changes in Document v6

No changes in this document revision

20 Dec 2007: Changes in Document v5

Page	Status	ID	Cat	Summary
10	New	487965	Cat 2	CTI connections do not allow correct synchronised halting of multiple processors

25 Sep 2007: Changes in Document v4

Page	Status	ID	Cat	Summary
13	New	457413	Cat 3	Serial Wire Debug tri-state logic is omitted within example ASIC
14	New	458626	Cat 3	Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH
15	New	458633	Cat 3	Example CoreSight subsystem (CSSYS) does not return error on unused APB

19 Jul 2007: Changes in Document v3

No Errata Changes

1 May 2007: Changes in Document v2

Page	Status	ID	Cat	Summary
9	Updated	396651	Cat 2	CSSYS: example system code incorrect (bad coding)

11 Oct 2006: Changes in Document v1

Page	Status	ID	Cat	Summary
9	New	396651	Cat 2	CSSYS: example system code incorrect (bad coding)
11	New	334758	Cat 3	CS DK11. HTM subsystem: CTI trigger input is unconnected
16	New	338004	Doc	DII 0092 CoreSight DK11 IIM Incorrect paths and filenames

Errata Summary Tables

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r0p1	r0p2	r1p0	r2p0
396651	Cat 2	CSSYS: example system code incorrect (bad coding)	X	X			
487965	Cat 2	CTI connections do not allow correct synchronised halting of multiple processors	X	X	X	X	
334758	Cat 3	CS DK11. HTM subsystem: CTI trigger input is unconnected	X				
457413	Cat 3	Serial Wire Debug tri-state logic is omitted within example ASIC				X	
458626	Cat 3	Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH	X	X	X	X	
458633	Cat 3	Example CoreSight subsystem (CSSYS) does not return error on unused APB	X	X	X	X	
338004	Doc	DII 0092 CoreSight DK11 IIM Incorrect paths and filenames	X				

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

396651: CSSYS: example system code incorrect (bad coding)

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 2, Present in: r0p0,r0p1, Fixed in r0p2.

Description

There are wiring errors in the example CoreSight sub-system RTL (CSSYS.v) supplied within the Integration Kit:

- **PREADYDBGExt** and **PRDATADBGExt** are assigned but never used.
- **PSELDBG** is driven by two signals, once from the output of the APB decoder and once from a signal **PSELDBGExt** which is never driven.

Implications

May cause Design Rule Checking issues as well as synthesis issues.

Workaround

Implementers should modify the example code (CSSYS.v) to remove of references to the **PSELDBGExt** signal.

487965: CTI connections do not allow correct synchronised halting of multiple processors

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 2, Present in: r0p0,r0p1,r0p2,r1p0, Fixed in r2p0.

Description

One of the purposes of including a Cross Trigger Interface (CTI) in a system is to enable synchronised halting of multiple processors in the system, where if one processor enters debug state then all processors enter debug state. The current connections do not permit this to be performed correctly.

The current connections use the DBGACK output from each processor to drive the EDBGRQ input to other processors. When any processor exits debug state, because of the delay introduced by the CTI system, EDBGRQ is not de-asserted sufficiently quickly and any restarted processor will immediately re-enter debug state.

The normal procedure for avoiding this race condition is for the debug tool to disable the CTI network when restarting any processors. However, this means that synchronised halting is not enabled until the debug tool re-enables the CTI network. This delay can range from hundreds to many thousands of cycles, depending on system speeds and debug tool capabilities.

Conditions

Details on the conditions for this erratum and the routines to enable and disable the CTI network are available from ARM in the document titled “Processor Debug Connectivity”, document number PR106-PRDC-009311, which accompanies this errata document.

Implications

If the CTI network is not disabled when restarting the processors then the processors might never restart normal execution.

If the CTI network is disabled when restarting the processors, then synchronised halting is not possible until the debug tool has re-enabled the CTI network. Once the CTI network is re-enabled, if any processor has halted then all connected processors will halt.

Workaround

This is a workaround for system implementers and debug tool vendors need to be aware of these changes.

The erratum can be avoided by modifications to the connections between the processor and CTI. Details of these changes are available from ARM in the document titled “Processor Debug Connectivity”, document number PR106-PRDC-009311, which accompanies this errata document.

Errata - Category 3

334758: CS DK11. HTM subsystem: CTI trigger input is unconnected

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 3, Present in: r0p0, Fixed in r0p1.

Description

The HTM subsystem, cshtmsubsys.v, comprises of an HTM32, HTM64, bus multiplexers and a Cross Trigger Interface (CTI) for each HTM.

The CTI trigger input connection (CTITRIGIN) to each CTI is 8 bits wide. On each CTI within cshtmsubsys.v, bits [6:0] are connected, but bit [7] of the trigger input connection

(CTITRIGIN) on each CTI is unconnected.

Conditions

1. Input 7 of a CTI in cshtmsubsys.v is enabled

The connections present between the HTM and the associated CTI are not affected by this erratum.

Implications

CTI Trigger input bit 7 is unusable in the CTI for the HTM32 and the CTI for the HTM64. If input 7 is enabled then it will result in unpredictable behaviour.

This can cause problems with topology detection routines, for example if this input is stuck at logic 1 then it might result in the routine reporting that everything is connected to this input.

Workaround

Workaround for system implementers:

Modify the HTM sub-system RTL file "cshtmsubsys.v" as follows so that the input is driven. Line 694, change the following:

```
assign CTITRIGINCTI64     = {TRIGGERHTM64, EXTOUTHTM64[1], EXTOUTHTM64[0], 4'b0};
```

to:

```
assign CTITRIGINCTI64     = {1'b0, TRIGGERHTM64, EXTOUTHTM64[1], EXTOUTHTM64[0],
4'b0};
```

Also, line 716, change the following:

```
assign CTITRIGINCTI32     = {TRIGGERHTM32, EXTOUTHTM32[1], EXTOUTHTM32[0], 4'b0};
```

to:

```
assign CTITRIGINCTI32     = {1'b0, TRIGGERHTM32, EXTOUTHTM32[1], EXTOUTHTM32[0],
4'b0};
```

Tools workaround:

If the HTM sub-system (cshtmsubsys) part of the CoreSight DK11 Integration Kit has been implemented, as delivered, then the "Channel to Trigger Enable Register 7" must be permanently disabled for each CTI connected to an HTM. To do this ensure that the register CTIINEN7[3:0], at address offset 0x03C, is set to 4'b0000.

457413: Serial Wire Debug tri-state logic is omitted within example ASIC

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 3, Present in: r1p0, Fixed in r2p0.

Description

Serial Wire Debug (SWD) operates with a clock pin and a bi-directional pin however it is the responsibility of the system integrator to implement tri-state driver logic to convert the uni-directional ports of SWJ-DP.

The Integration Kit provides an example system to demonstrate how to integrate CoreSight features, the top level of an ASIC (ASIC.v) does not follow the recommendations of how to integrate SWJ-DP. No bi-directional pin (**SWDIOTMS**) is shown along with the tri-state logic required for **SWDO** and its enable **SWDOEN**. It currently exports all the signals to the Serial Wire JTAG Interface Master (SWJIM), these signals would not be available to a debug emulator within real implementations.

Implications

The demonstrated integration testbench does not correctly verify the integration of the SWD interface that is required to be implemented within real silicon.

Workaround

none

458626: Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 3, Present in: r0p0,r0p1,r0p2,r1p0, Fixed in r2p0.

Description

The CoreSight Architecture recommends than any unused or unavailable interfaces must respond with **ATVALID** LOW, **AFVALID** LOW, **ATREADY** HIGH and **AFREADY** HIGH where appropriate (other signals may be tied LOW).

Within the Integration Kit, only a limited number of the ATB inputs to the funnel are required. These unused connections have **ATVALIDS**<x> tied LOW and **AFREADYS**<x> tied LOW, where **AFREADYS**<x> should be tied HIGH and <x> is one of the unused interfaces.

Normally a debugger should not enable unused inputs, however, the recommended tie offs ensure safe flush operations if one is enabled.

Conditions

The erratum will only be observed if:

1. The unused ATB input to CSSYS is incorrectly connected with **AFREADYS**<x> tied LOW
2. A debugger enables input port <x>
3. A flush operation is performed

Implications

When the flush request is requested by the trace sink, the Trace Funnel performs a flush of all its enabled ATB inputs. Until all the enabled inputs have returned **AFREADYS** HIGH, normal operation will not be resumed. Under these conditions the Trace Funnel will stop taking trace data from the active ATB inputs and wait on the unconnected inputs because they have not returned **AFREADYS** HIGH.

This does not affect trace operation if unconnected inputs are not enabled or have **AFREADYS** tied HIGH.

Workaround

For debug tools:

- Do not enable unused ATB inputs to the trace funnel.

For system integrators:

- Modify the Integration Kit to tie **AFREADYS**<x> HIGH.

458633: Example CoreSight subsystem (CSSYS) does not return error on unused APB

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Cat 3, Present in: r0p0,r0p1,r0p2,r1p0, Fixed in r2p0.

Description

Where a memory region does not decode to a real slave, the default slave should be used. In the case of APB, this is performed by tieing **PREADY** HIGH, **PSLVERR** HIGH and **PRDATA[31:0]** to 0x00000000.

For the example CoreSight subsystem, CSSYS, if a component with an APB interface is omitted, due to the absence of its `define then this region must select the default slave response. The existing implementation does not return **PSLVERRDBG** HIGH which may cause a debugger to assume that a component is present and that it is simply returning zeros.

Condition

This defect will occur if:

1. A memory mapped CSSYS component is not present. This can correspond to:
   - CSTPIU
   - CSETB
2. The region of memory for that component is accessed.

Implications

A debugger attempting to access an unused region of memory would expect an error response. No error response implies that a component is present. Under the above conditions, a tool may conclude that a component is present where one is not.

A debugger will not be able to determine the component as all reads to the unused region of memory will return zero (0x00000000).

Workaround

It is recommended that system integrators modify the example CoreSight subsystem (CSSYS) to ensure that, when components are absent, the unused regions of memory return error responses.

Errata - Documentation

338004: DII 0092 CoreSight DK11 IIM Incorrect paths and filenames

Status

Affects: product Coresight Design Kit for ARM11 (DK11).

Fault status: Doc, Present in: r0p0, Fixed in r0p1.

Description

Minor defects can be found in DII0092A, CoreSight Design Kit 11 IIM:

1. Page 4-8: Under "Search path", change "/projects/pr106_dart/Libraries..." to "/home/user/Libraries..."
2. Page 9-5: Under "Simulation" and "Logs", change two instances of "etm11cs_intkit" to "cs_dk11_intkit".

Implications

none

Workaround

none