Arm CoreSight basics for Keil tools

arm KEIL

Abstract

Arm CoreSight technology is a set of tools that can be used to debug and trace software that runs on Arm-based devices. Debugging features are used to observe or modify the state of parts of the design, while trace features allow for continuous collection of system information for later off-line analysis. With Arm CoreSight, both are used together at all stages in the design flow.

This application note explains the Arm CoreSight components and how they relate to the debugging experience in Keil tools.

Contents

Introduction

Arm Cortex-M processor-based devices use CoreSight technology which offers powerful debug and trace capabilities.

Debug features include:

- Run Control of the processor allowing you to start and stop programs.
- Single Step one source or assembler line.
- Set breakpoints while the processor is running.
- Read/write memory contents and peripheral registers on-the-fly.
- Program internal and external FLASH memory.

Trace features include:

- Serial Wire Viewer (SWV) provides program counter (PC) sampling, data trace, event trace, and instrumentation trace information.
- Instruction (ETM) Trace streamed directly to your PC enabling debugging of historical sequences, software profiling, and code coverage analysis.

The CoreSight features are available via JTAG and Serial Wire Debug interfaces.
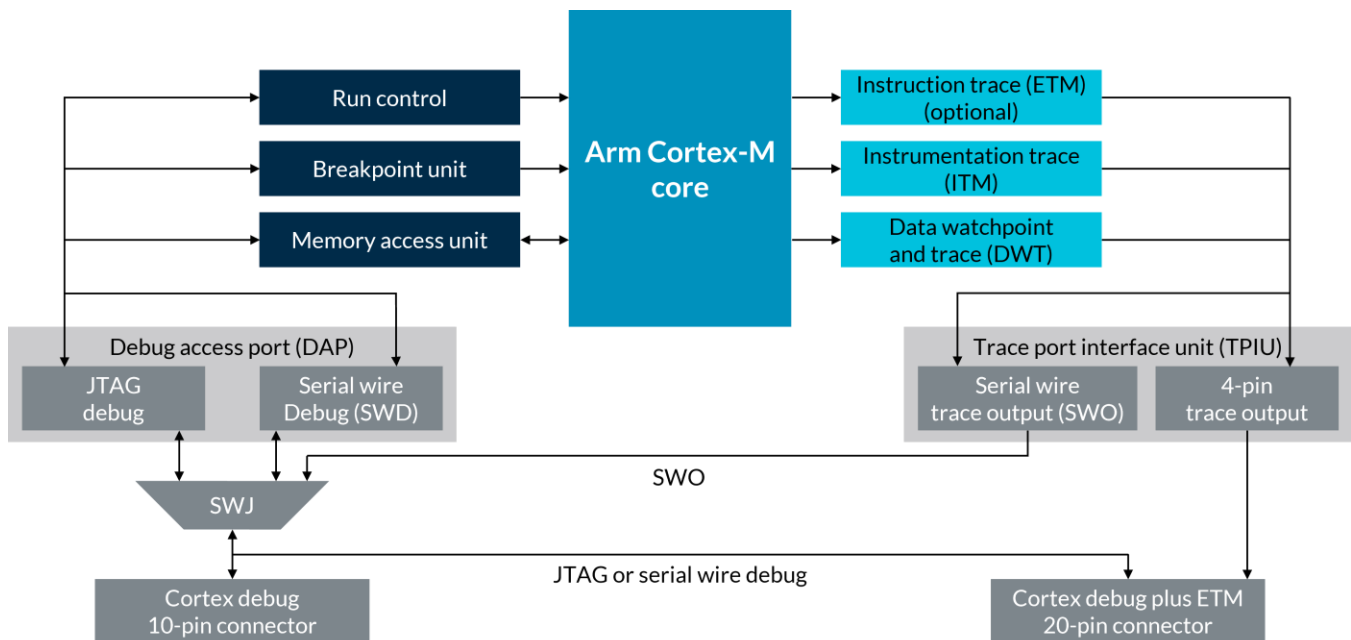
Interfaces

JTAG

JTAG is the industry-standard interface used to download and debug programs on a target processor, as well as many other functions. It offers a convenient and easy way to connect to devices and is available on all ARM processor-based devices. The JTAG interface can be used with Cortex-M based devices to access the CoreSight debug capabilities.

Serial Wire Debug

The Serial Wire Debug (SWD) mode is an alternative to the standard JTAG interface. It uses only two pins to provide the same debug functionality as JTAG with no performance penalty and introduces data trace capabilities with the Serial Wire Viewer (SWV).

The SWD interface pins can be overlaid with JTAG signals, allowing the standard target connectors to be used:

- TCLK - SWCLK (Serial Wire Clock)
- TMS - SWDIO (Serial Wire Data Input/Output)
- TDO - SWO (Serial Wire Output - required for SWV)

JTAG and SWD modes are fully supported by ULINK debug adapters.

Serial Wire Output

The Serial Wire Output pin can be used to provide trace data. For connectors that share JTAG and SWD signals, this pin is shared with the TDO signal.

Trace Output

The 4-pin trace output can be used to provide trace data coming from the Embedded Trace Macrocell (ETM). It is helpful for system development purposes, such as examining timing issues, and for application profiling or performance analysis.

Components

Embedded Trace Macrocell (ETM)

The Embedded Trace Macrocell (ETM) provides high bandwidth instruction trace via four dedicated trace pins accessible on the 20-pin Cortex Debug + ETM connector. This enhanced trace capability records a program's execution instruction-by-instruction which can be used for:

- Debugging historical sequences leading up to events of interest
- Software profiling and algorithm optimization
- Code coverage analysis

Note:

- Instruction trace is only supported by ULINK*pro*.
- ETM is optionally available on Armv7-M and Armv8-M processor-based microcontrollers. It is not available on Armv6-M.

Instruction Trace Macrocell (ITM)

The Instrumentation Trace Macrocell (ITM) has the following features.

- Trace data generation. This includes:
  - printf style debugging using the stimulus port registers which generate instrumentation packets.
  - Global and local timestamp packet generation.
  - Synchronization packet generation.
- Arbitration between trace packets (prioritizing multiple sources and selecting a single source at a time):
  - external Data Watchpoint and Trace (DWT) packets and internally generated packets.

Data Watchpoint and Trace (DWT)

The Data Watchpoint and Trace (DWT) unit receives data transactions and instruction execution information from the processor core. Exception information and core profiling information is also delivered to the DWT from the processor core. Any profiling counter and exception information are passed to the packet generator so it can generate, buffer, and arbitrate packets to be sent to the ITM. The DWT features:

- Watchpoints
- Data tracing
- Program Counter (PC) tracing
- Cycle count matching
- Additional PC sampling:
    - PC sample trace output because of a cycle count event
    - External PC sampling using a PC sample register
- Exception tracing
- Match event tracing
- Performance profiling counters

Serial Wire Viewer (SWV)

Armv7-M and Armv8-M based devices can provide high-speed data trace information in several ways depending on the type of information or analysis you require.

SWV provides real-time data trace information from various sources within a Armv7-M/Armv8-M device. It is transmitted via the SWO pin while your system processor continues to run at full speed. Information is available from the ITM and DWT units, providing:

- PC (Program Counter) sampling
- Event counters that show CPU cycle statistics
- Exception and Interrupt execution with timing statistics
- Trace data - data reads and writes used for timing analysis
- ITM trace information used for simple printf-style debugging

SWV data trace is available via the SWO pin in two output formats:

- UART style (1Mb/s) - supported by ULINK2 and ULINKplus
- Manchester encoded (100Mb/s) - supported by ULINKpro

Note: Data trace via SWV is not available using the JTAG interface. SWV is only available with SWD.
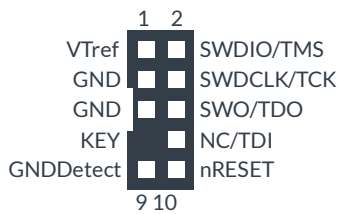
Debugging in µVision

MDK contains the µVision debugger that connects to various debug/trace adapters and allows you to program the Flash memory. It supports traditional features like simple and complex breakpoints, watch windows, and execution control. Using trace, additional features like event/exception viewers, logic analyzer, execution profiler, and code coverage are supported.
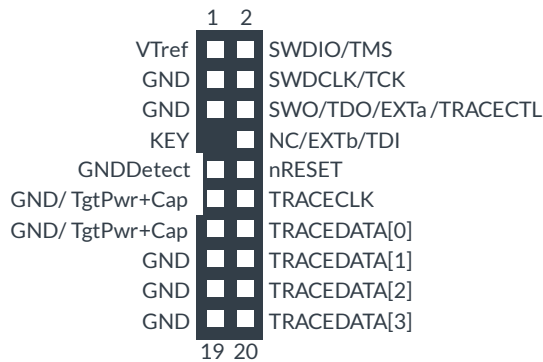
For more information on debugging with µVision, read the chapter "Debugging Applications" in the MDK Getting Started Guide or go to the online documentation.
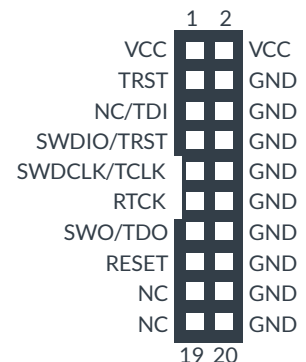
Connectors

There are several target connectors which are used to connect to an Arm target system. They enable debug and trace units such as the ULINK family of debug adapters to physically connect to the target system to program, debug, and gather trace information. Each connector has been defined for particular use cases and has specific benefits.

10-pin Cortex Debug		20-pin Cortex Debug + ETM		20-pin Arm JTAG	
VTref	SWDIO/TMS	VTref	SWDIO/TMS	VCC	VCC
GND	SWDCLK/TCK	GND	SWDCLK/TCK	TRST	GND
GND	SWO/TDO	GND	SWO/TDO/EXTa /TRACECTL	NC/TDI	GND
KEY	NC/TDI	KEY	NC/EXTb/TDI	SWDIO/TRST	GND
GNDDetect	nRESET	GNDDetect	nRESET	SWDCLK/TCLK	GND
		GND/ TgtPwr+Cap	TRACECLK	RTCK	GND
		GND/ TgtPwr+Cap	TRACEDATA[0]	SWO/TDO	GND
		GND	TRACEDATA[1]	RESET	GND
		GND	TRACEDATA[2]	NC	GND
		GND	TRACEDATA[3]	NC	GND

10-pin Cortex Debug Connector

The Cortex Debug Connector provides support for Serial Wire and JTAG interface modes in a very small, low cost 10-pin (0.05") connector. This connector provides access to all SWD, SWV, and JTAG signals available on a Cortex-M based device.

A 10-pin header (Samtec FTSH-105-01) is specified with these dimensions: 0.25" x 0.188" (6.35 mm x 4.78 mm).

20-pin Cortex Debug + ETM Connector

This small 20-pin (0.05") connector provides access to SWD, SWV, JTAG, and ETM (4-bit parallel trace) signals available on an Armv7-M and Armv8-M based device.

A 20-pin header (Samtec FTSH-110-01) is specified with dimensions: 0.50" x 0.188" (12.70 mm x 4.78 mm).

20-Pin Arm Standard JTAG Connector

The Arm standard JTAG connector provides support for Serial Wire and JTAG interface modes in a 20-pin (0.1") connector. It has been used for many years in Arm processor-based systems and can be used to access all SWD, SWV, and JTAG signals available on a Cortex-M based device.

Dimensions of the Arm JTAG connector are 1.29" x 0.722" (33 mm x 18.5 mm).

Appendix - Definitions

It is useful to have a basic understanding of these terms.

1. **DAP** (Debug Access Port): This component is accessed via the JTAG or SWD port. One of the features of the DAP are the memory read and write accesses which provide on-the-fly memory accesses without the need for processor core intervention. μVision uses the DAP to update memory, watch, and peripherals while the processor is running. You can also modify variable values on-the-fly. No CPU cycles are used, the program can be running, and no code stubs are needed. Do not confuse this with CMSIS-DAP which is an Arm on-board debug adapter standard.
2. **ETB** (Embedded Trace Buffer): A small amount of internal RAM used as an ETM trace buffer. This trace does not need a specialized debug adapter such as a ULINKpro. ETB runs as fast as the processor and is especially useful for very fast Cortex-A processors. Not all processors have ETB. See your specific datasheet.
3. **ETM** (Embedded Trace Macrocell): Displays all the executed instructions. The ULINKpro provides ETM. ETM requires a special 20 pin CoreSight connector. ETM also provides Code Coverage and Performance Analysis. ETM is output on the Trace Port or accessible in the ETB (ETB has no Code Coverage or Performance Analysis).
4. **Hardware Breakpoints**: The Cortex-M0+ has 2 breakpoints. The Cortex-M3, M4 and M7 usually have 6. These can be set/unset on-the-fly without stopping the processor. They are no skid: they do not execute the instruction they are set on when a match occurs. The CPU is halted before the instruction is executed.
5. **ITM** (Instrumentation Trace Macrocell): As used by μVision, ITM is thirty-two 32-bit memory addresses (Port 0 through 31) that when written to, will be output on either the SWO or trace port. This is useful for printf type operations (μVision uses port 0 for that). The data can be saved to a file.
6. **JTAG** (Joint Test Action Group): Provides access to the CoreSight debugging module located on the Cortex processor. It uses 4 to 5 pins.
7. **MTB** (Micro Trace Buffer): A portion of the device internal user RAM used for an instruction trace buffer. Only on Cortex-M0+ processors. Cortex-M3/M4 and Cortex-M7 processors provide ETM trace instead.
8. **SWD** (Serial Wire Debug) is a two-pin alternative to JTAG and has about the same capabilities except boundary scan is not possible. SWD is referenced as SW in the μVision Cortex-M Target Driver Setup. The SWJ box must be selected for ULINK debug adapters.
9. **SWO** (Serial Wire Output): SWV frames usually come out this one pin output (shared with JTAG/TDO).
10. **SWV** (Serial Wire Viewer): A trace capability providing display of reads, writes, exceptions, PC samples and printf. SWV must use SWD because the JTAG signal TDO shares the same pin as SWO. The SWV data normally comes out the SWO pin or trace port.
11. **Trace Port**: A 4-bit port that ULINKpro uses to collect ETM frames and optionally SWV (rather than the SWO pin).
12. **Watchpoints**: Both the Cortex-M0, M0+, Cortex-M3, Cortex-M4 and Cortex-M7 can have 2 Watchpoints. These are conditional breakpoints. They stop the program when a specified value is read and/or written to a specified address or variable. There also referred to as Access Breaks in Keil documentation.

Notes:

Not all processors have all features (consult your specific datasheet):

- Cortex-M0/M0+/M23 do not have SWV, ITM or ETM trace. They have DAP read/write.
- Cortex-M3/M4/M7/M33/M55 can have all or most of these features listed implemented.
- MTB may be found on certain Cortex-M0+.
- JTAG and SWD are functionally equivalent. The signals and protocols are not directly compatible.