ARM PrimeCell
Synchronous Static Memory Controller (PL093)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p4 of PL093

Proprietary notice

Document confidentiality status

This document is Non Confidential.

Web address

http://www.arm.com/

Feedback on the product

If you have any comments or suggestions about this product, contact your supplier giving:

- The product name
- A concise explanation of your comments.

Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

INTRODUCTION 5

ERRATA SUMMARY TABLE 7

ERRATA - CATEGORY 1 9

291661: Does not generate nSMBLS correctly For Certain Width Configurations 9

326300: Synchronous Burst Write nSMBURSTWAIT Failure 10

ERRATA - CATEGORY 2 11

150012: Incorrect behaviour with synchronous burst memory devices 11

198809: Register writes update value twice 12

313075: Performance Issue during reads for HSIZE > Memory Size 13

322167: AhbWideRdCounter is Being Incorrectly Decremented 15

323746: Performance Inefficiency When Synchronous Burst Not Started on Burst Boundary 17

328319: Some Processes Are Not Reset In the SsmcPadIf Module 18

331175: Read data loss during page mode reads 19

332124: Incorrect behaviour of SMBAA output 20

332941: Incorrect Assertion of Chip Select for Synchronous Write Transfer 21

338018: Use of EBI interface may cause data loss 22

350401: Byte lane strobe does not get cleared after a write 23

ERRATA - CATEGORY 3 24

There are no Errata in this Category 24

ERRATA - DOCUMENTATION 25

328398: TRM Errors 25

334526: TRM Figure 2-40 incorrectly mentions SMMEMCLK 26

334813: Incorrect Delay Number in TRM 27

341659: Error in Section 3.3.7 in Technical Reference Manual 28

350030: Incorrect halfword transfer comment in TRM 29

350850: Incorrect SMBSRx register bit assignments in TRM 30

ERRATA - SOFTWARE 31

There are no Errata in this category 31

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

07 Sep 2005: Changes in Document v9

Page	Status	ID	Cat	Summary
23	New	350401	Cat 2	Byte lane strobe does not get cleared after a write
30	New	350850	Doc	Incorrect SMBSRx register bit assignments in TRM
29	New	350030	Doc	Incorrect halfword transfer comment in TRM
28	New	341659	Doc	Error in Section 3.3.7 in Technical Reference Manual

17 Jan 2005: Changes in Document v8

Page	Status	ID	Cat	Summary
10	Updated	326300	Cat 1	Synchronous Burst Write nSMBURSTWAIT Failure
22	New	338018	Cat 2	Use of EBI interface may cause data loss
21	Updated	332941	Cat 2	Incorrect Assertion of Chip Select for Synchronous Write Transfer
20	Updated	332124	Cat 2	Incorrect behaviour of SMBAA output
18	Updated	328319	Cat 2	Some Processes Are Not Reset In the SsmcPadIf Module
27	New	334813	Doc	Incorrect Delay Number in TRM
26	New	334526	Doc	TRM Figure 2-40 incorrectly mentions SMMEMCLK

08 Oct 2004: Changes in Document v7

Page	Status	ID	Cat	Summary
9	New	291661	Cat 1	Does not generate nSMBLS correctly For Certain Width Configurations
10	New	326300	Cat 1	Synchronous Burst Write nSMBURSTWAIT Failure
11	New	150012	Cat 2	Burst Write to flash HSIZE != Memsize
12	New	198809	Cat 2	Register writes update value twice
13	New	313075	Cat 2	Performance Issue during reads for HSIZE > Memory Size
15	New	322167	Cat 2	AhbWideRdCounter is Being Incorrectly Decremented
17	New	323746	Cat 2	Performance Inefficiency When Synchronous Burst Not Started on Burst Boundary
19	New	331175	Cat 2	Read data loss during page mode reads
20	New	332124	Cat 2	Incorrect behaviour of SMBAA output
21	New	332941	Cat 2	Incorrect Assertion of Chip Select for Synchronous Write Transfer
25	New	328398	Doc	TRM Errors

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0-00LTD0	r0p1-00LTD0	r0p2-00LTD0	r0p2-00REL0	r0p3-00REL0	r0p4-00REL0
291661	Cat 1	Does not generate nSMBLS correctly For Certain Width Configurations	X	X	X			
326300	Cat 1	Synchronous Burst Write nSMBURSTWAIT Failure			X	X		
150012	Cat 2	Incorrect behaviour with synchronous burst memory devices	X	X	X	X	X	X
198809	Cat 2	Register writes update value twice	X	X	X			
313075	Cat 2	Performance Issue during reads for HSIZE > Memory Size		X	X			
322167	Cat 2	AhbWideRdCounter is Being Incorrectly Decremented			X	X		
323746	Cat 2	Performance Inefficiency When Synchronous Burst Not Started on Burst Boundary			X	X		
328319	Cat 2	Some Processes Are Not Reset In the SsmcPadIf Module				X		
331175	Cat 2	Read data loss during page mode reads			X	X		
332124	Cat 2	Incorrect behaviour of SMBAA output			X	X		
332941	Cat 2	Incorrect Assertion of Chip Select for Synchronous Write Transfer				X		
338018	Cat 2	Use of EBI interface may cause data loss					X	
350401	Cat 2	Byte lane strobe does not get cleared after a write				X	X	X
328398	Doc	TRM Errors			X	X		
334526	Doc	TRM Figure 2-40 incorrectly mentions SMMEMCLK					X	
334813	Doc	Incorrect Delay Number in TRM					X	
341659	Doc	Error in Section 3.3.7 in Technical Reference Manual					X	X
350030	Doc	Incorrect halfword transfer comment in TRM						X
350850	Doc	Incorrect SMBSRx register bit assignments in TRM						X

Errata - Category 1

291661: Does not generate nSMBLS correctly For Certain Width Configurations

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 1, Present in: r0p0-00LTD0,r0p1-00LTD0,r0p2-00LTD0, Fixed in r0p2-00REL0. Updated in this document.

Description

PL093 does not generate nSMBLS correctly for the following scenarios:

1st write where AHB Width < Memory Width, followed by 2nd write where AHB Width >= Memory Width. SSMC does not assert the nSMLBS signals correctly during the second write.

Symptoms

The condition in which the defect occurs is :

Write happening to CS6 with HBURST = INCR4 , HSIZE = WORD,

Followed by a write(with no HTRAN = IDLE cycles in between) to CS6 with HBURST = SINGLE , HSIZE = BYTE to a different location.

The reason for this bug is because of different HSIZE.

Implications

For Reads this should not be a problem as all byte lanes should be selected anyway.

Writes will always be a problem as it can mean that either certain byte lanes are not written to, or certain byte lanes are written to when they should remain unchanged. This means that it cannot be gauranteed that data is being written correctly.

This will be the same for byte or non-byte memories which use just nSMBBLS or nSMBLS and WEN (RBLE setting).

Workaround

none

326300: Synchronous Burst Write nSMBURSTWAIT Failure

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 1, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Updated in this document.

Description

This erratum describes incorrect behaviour of PL093 with respect to synchronous write bursts.

SRAM that is capabale of accepting synchronous write bursts from the PL093, such as synchronous PSRAM, can assert its WAIT signal (connected to nSMBURSTWAIT) to hold-off write accesses. This WAIT can be asserted before the first data beat, and/or during the burst. This assertion of WAIT during a synchronous burst write will cause the PL093 to lose write data, ie, write transfers and data that have been accepted on the AHB side will not be performed to the SRAM.

The PL093 may also lose write data during a synchronous write burst if a BUSY transfer occurs on the AHB bus during the middle of the AHB write burst (An AHB transfer with HTRANS=BUSY). This defect has the same symptoms as described above; data will be accepted on the AHB side but will never be written to memory.

Implications

Write data that appears to have been accepted by the PL093 AHB interface may not be written to memory. This behaviour will occur if the PL093 is writing to synchronous PSRAM (or any memory that asserts a wait signal during synchronous write bursts), in synchronous mode.

Workaround

There are no work arounds for this defect.

Errata - Category 2

150012: Incorrect behaviour with synchronous burst memory devices

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p0-00LTD0,r0p1-00LTD0,r0p2-00LTD0,r0p2-00REL0,r0p3-00REL0,r0p4-00REL0, Open. Updated in this document.

Description

Writes in synchronous burst mode will not be performed as continuous bursts if HSIZE is not equal to the Memory Width.

Symptoms

For example a write of 4 words (32 bit) to 16 bit flash will take 7 (5 setup + 2 data) * 4 cycles = 28 cycles.

The expected time for this access would be 5 (setup) + (2 data)*4 = 13 cycles.

The longer the data transfer the larger the impact that will be seen.

Implications

This is a performance issue rather than a functional issue. System performance (when burst writes are performed on differing HSIZE and memory widths) will be affected

Workaround

If possible, it should be ensured that HSIZE is equal to the Memory Width when interfacing to Micron pseudo-SRAM (or other synchronous burst) devices.

198809: Register writes update value twice

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p0-00LTD0,r0p1-00LTD0,r0p2-00LTD0, Fixed in r0p2-00REL0. Unchanged in this document.

Description

The slave select state machine in the SsmcAhbSlvRegIf block stays in the write state for 2 clock cycles, during which time the HwdataBuf write data value changes in the middle. The target register is updated while the state machine is in the write state, so may change twice depending on the previous register value, the old HWDATA value and the register write HWDATA value.

The target register will be updated in the following manner:

1 - Original register value before write access

2 - Set to the HWDATA value before the write access for one clock cycle

3 - Set to the HWDATA value of the write access

The final register value will always be correct. Register values for a bank with a memory access in progress must not be written to, as this could cause an incorrect value to be used during the memory access.

Implications

The only effect of this defect may be that a register write causes the register value to toggle to an intermediate value for one cycle before changing to the correct target value, which will use a small amount of extra power. As the programmable registers will typically only be written to during system initialisation and will remain unchanged during memory accesses, this will have a tiny effect on the system.

If the previous HWDATA value before the register write matches the target write value, or it matches the register's previous value, then the intermediate register update will not be visible as the value will not change.

Workaround

none

313075: Performance Issue during reads for HSIZE > Memory Size

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p1-00LTD0,r0p2-00LTD0, Fixed in r0p2-00REL0. Updated in this document.

Description

There is a performance issue with respect to HSIZE > MSIZE.

This problems is due to an issue with the loading of BeatCount in the SsmcMemTSM block, when the state machine is in the ST_WAIT_TXRONBUS state. It is likely to occur when AHB width(HSIZE) is greater than Memory Width.

This issue was discovered when the Denalitest3 was run with HSIZE = 2 (32-bits).

For an INCR8 access only the first access was 4x16-bit and the subsequent 6 accesses were each 2x16-bit accesses. The expected behaviour is 3 accesses each 4x16-bit. Likewise the same phenomenon occurs for the INCR16 accesses and for the synchronous INCR8 and INCR16 accesses.

Affected Items:

SsmcMemTSM/SsmcAhbSlvMemIF

Implications

For an INCR8 access only the first access may be 4x16-bit and the subsequent 6 accesses each being 2x16-bit accesses. The expected behaviour is 3 accesses each 4x16-bit. Likewise the same phenomenon occurs for the INCR16 accesses and for the synchronous INCR8 and INCR16 accesses

Workaround

SsmcMemTSM:

Line 2553:

From:

```
else if (BUSYCYC == 1'b0)
```

to:

```
else if ((BUSYCYC == 1'b0) && (HsizeEqMWidth == 1'b1))
```

SsmcAhbSlvMemIf.v

Line 1118:

From:

```
WaitRdCycVer or SlowClkM or SyncEnRead1)
```

to:

```
WaitRdCycVer or SlowClkM or SyncEnRead1 or iHsizeEqMWidth or
```

```
              iAhbNarrow)
```

Line: 1248-1249:

From:

```
                    NextHREADYOUTSMC = (~WaitRdCycVer) & SlowClkM &
                                       (~SyncEnRead1);
```

to:

```
                    NextHREADYOUTSMC = (~WaitRdCycVer) & SlowClkM &
                                       (~SyncEnRead1) &
                                        (iHsizeEqMWidth | iAhbNarrow);
```

Line 1861:

From:

```
         MW1 or READCYC or WaitRdCyc or SlowClkM or SmCSTSM or ErrCond)
```

to:

```
          MW1 or READCYC or SlowClkM or SmCSTSM or ErrCond or
          MemoryRdSt or WaitRdCyc or BUSYCYC)
```

Line 1865:

From:

```
    (SlowClkM == 1'b1) && (iAhbWider == 1'b1) && (READCYC == 1'b1))
```

to:

```
       (SlowClkM == 1'b1) && (iAhbWider == 1'b1) &&
       ((READCYC == 1'b1) || ((BUSYCYC & MemoryRdSt) == 1'b1)))
```

Line 1916:

From:

```
else if ((ErrCond == 1'b1) || (READCYC == 1'b0))
```

to:

```
else if ((ErrCond == 1'b1) ||
            ((READCYC == 1'b0) && ((BUSYCYC & MemoryRdSt) == 1'b0)))
```

322167: AhbWideRdCounter is Being Incorrectly Decremented

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Updated in this document.

Description

A counter in the Ssmc is being decremented incorrectly when nSMBURSTWAIT is used.

Symptoms

The following were seen and thus can also be seen as implications:

A synchronous burst read is incorrectly terminated early. The PL093 corrupts the first read data with data from a read that should have been terminated.

Any burst is separated into two chip selects by deasserting the chip select and reasserting it in the middle of a burst.

This is occurs with synchronous memories when nSMBURSTWAIT is used.

Implications

The PL093 corrupts the first read data with data from a read that should have been terminated.

Workaround

File : SsmcMemTSM.v for verilog and SsmcMemTSM.vhd for vhdl

Region : In ST_BURST_READ state

Note the line ********ISSUE*******

For verilog, the following portion of the code (from line 2531 ....)

```
// Assert WaitRdCyc if WSTBRD1 = "00000" and it is an
// Asynchronous Memories. For Synchronous Memories it can
// be asserted without comparison with WSTBRD1 because,
// WSTBRD1 has no meaning for Synchronous Memories.
if ((SyncEnRead1 == 1'b0) && (WSTBRD1 != 5'b00000))
  NextWaitRdCycVer = 1'b1;
else
  NextWaitRdCycVer = 1'b0;      ********** ISSUE *******
```

Needs to be replaced by

```
// Assert WaitRdCyc if WSTBRD1 = "00000" and it is an
// Asynchronous Memories. For Synchronous Memories it can
// be asserted without comparison with WSTBRD1 because,
```

```
// WSTBRD1 has no meaning for Synchronous Memories.
if ((SyncEnRead1 == 1'b0) && (WSTBRD1 != 5'b00000))
  NextWaitRdCycVer = 1'b1;
else
  NextWaitRdCycVer = (NewBurst | NewBrstOccrd);
```

For VHDL, the following portion of the code(from line 2232)

```
-- Assert WaitRdCyc if WSTBRD1 = "00000" and it is an Asynchronous
-- Memories. For Synchronous Memories it can be asserted without
-- comparison with WSTBRD1 because, WSTBRD1 has no meaning for
-- Synchronous Memories.
if ((SyncEnRead1 = '0') and (WSTBRD1 /= "00000")) then
  NextWaitRdCycVer <= '1';
else
  NextWaitRdCycVer <= '0';    ********** ISSUE **********
end if;
```

Needs to be replaced by

```
-- Assert WaitRdCyc if WSTBRD1 = "00000" and it is an Asynchronous
-- Memories. For Synchronous Memories it can be asserted without
-- comparison with WSTBRD1 because, WSTBRD1 has no meaning for
-- Synchronous Memories.
if ((SyncEnRead1 = '0') and (WSTBRD1 /= "00000")) then
  NextWaitRdCycVer <= '1';
else
  NextWaitRdCycVer <= (NewBurst or NewBrstOccrd);
end if;
```

323746: Performance Inefficiency When Synchronous Burst Not Started on Burst Boundary

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Unchanged in this document.

Description

This issue was found in an INCR8x16 transfer which was broken up into two chip selects, however, any incrementing type burst can result in the burst being broken up into two chip selects.

Implications

There is some performance inefficiency in transfer of data when a synchronous burst read is not started on a burst boundary, that is when the burst read starts on an offset of the burst length.

Workaround

One workaround is to ensure that bursts are issued to start on a burst boundary.

Or modify the RTL as below:

In the file SsmcAhbSlvMemIf.vhd:

Starting from line number 1097, the entire AhbCountComb process block needs to be replaced that in the r0p3 code.

In SsmcAhbSlvMemIf.v, you will need to add:

```
reg [4:0] Temp16;
//Temporary Variable
```

and replace the AhbCountComb process in the r0p2 code with that in the r0p3 code.

Or you can obtain the updated code from Support.

328319: Some Processes Are Not Reset In the SsmcPadIf Module

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00REL0, Fixed in r0p3-00REL0. Updated in this document.

Description

In the process p_SmClkDelPadSeq in SsmcPadIf.v, which is clocked by SMMEMCLKDELAY but is not reset. All of the *Del signals are X until that clock starts.

The last four processes in the PadIf file are not reset either (and probably should be), but they are being clocked on the posedge of SMFBCLK* going from X to 1 at the start of the simulation, as these clocks do not start running properly until the same time as SMMEMCLKDELAY and are inverted versions of it.

Symptoms

When the memory controller is configured for synchronous sram, the memory control signals were found to be undefined for a short time during the first memory access.

These signals include the address, chip enable, write enable, output enable, etc.

The problem is due the fact the value of these signals is dependent on the SMMEMCLKDELAY, which is recommended to be an inverted version of SMCLK.

However, SMCLK does not start until the first memory access even if the controller is configured to have the memory clock be free running. (Bit 0 of SSMCCR is set to '1').

There are a number of signals in SsmcPadIf.v that will not get their initial value until the first edge of SMMEMCLKDELAY. They are nSMWENMCDel, nSMOENMCDel, SMCSMCDel, etc.

Affected Items

SsmcPadIf module

Implications

Some memory control signals were found to be undefined for a short time during the first memory access.

Workaround

None

331175: Read data loss during page mode reads

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Unchanged in this document.

Description

If a HTRANS=BUSY transfer occurs during a page-mode read, incorrect read data may be returned. Data that has been read from the memory will not be transfered on the AHB bus.

Implications

The defect will be seen in the PL093 if it is used in a system with a master capable of performing BUSY transfers, and reading from memory in page-mode bursts. If a BUSY transfer occurs during a page-mode read burst, read data may be lost.

Workaround

There are no work arounds for this defect.

332124: Incorrect behaviour of SMBAA output

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Updated in this document.

Description

Unregistered versions of the BMWrite, BIWriteEn and SyncEnWrite signals have been used in the design. This results in incorrect behaviour on the SMBAA signal during a burst write.

The defect arises when two back to write back transfers occur on the PL093 AHB port, with the first requiring SMBAA to be asstered, and the second not. During the first write to memory, the acceptance of the second write on the AHB port will cause the SMBAA output to be deasstered.

The effect of this will be that all the write data beats will be written to the same memory location, rather than incrementing locations.

The PL093 should use registered versions of BMWrite, BIWriteEn and SyncEnWrite, to avoid the values changing when the second AHB write is accepted.

Implications

This defect will cause SMBAA to be prematurely de-asserted during a burst write, causing data to be written to incorrect memory locations. Rather than writing each data beat to incrementing address locations, all data will be written to the same location.

Note that this will only affect memories which accept burst write transfers and use the SMBAA to increment the write address.

Workaround

There are no workarounds.

332941: Incorrect Assertion of Chip Select for Synchronous Write Transfer

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00REL0, Fixed in r0p3-00REL0. Updated in this document.

Description

Incorrect assertion of Chip Select for synchronous write transfer can occur when the Write Burst

Mode bit (BMWrite) is programmed as '0' in the SSMC control register.

In addition to the above programming, an AHB write access where HSIZE is wider than memory width(for the above programmed memory bank) occurs followed by one more write(either NSEQ/IDLE) to another bank.

Instead of additional chip select assertions for the same bank being seen, only one chip select assertion is seen for the chosen bank and the chip select then changes to another bank.

Implications

For transfers with HSIZE wider than the Memory width, some transfers may not be completed with the chip select being deasserted before completion of the transfer.

Workaround

A workaround is to ensure that when the PL093 is programmed for Synchronous memory, that the PL093 is also programmed to support burst writes.

338018: Use of EBI interface may cause data loss

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p3-00REL0, Fixed in r0p4-00REL0. New in this document.

Description

When the PL093 is used in a system with the PL220 EBI, it is possible that AHB read bursts may be handled incorrectly. If a new AHB read transfer is started at the same time as the external bus is being relinquished by the PL093, the read transfer will be missed. When the PL093 regains the external bus it carries on with the previous AHB transfer rather than starting the new one. This defect is independent of the memory type, synchronous or asynchronous, attached to the PL093.

Implications

The PL093 may return incorrect read data when used in conjunction with the PL220 EBI. If the PL220 EBI is not used, this defect will not occur.

Workaround

There is no workaround.

350401: Byte lane strobe does not get cleared after a write

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Cat 2, Present in: r0p2-00REL0,r0p3-00REL0,r0p4-00REL0, Open. New in this document.

Description

When doing a byte-sized write to a 16-bit memory device, following a halfword write, PL093 asserts two byte-lane strobes (nSMBLS) during the write, thereby corrupting the adjacent byte in memory. This is because during the halfword write, two byte-lane enables (nSMBLS) get activated, which don't get cleared before the byte-sized write.

The proposed fix is in the RTL file SsmcAhbSlvMemIf.v circa line 2375.

The original code is:

```
if ((iWRITECYC == 1'b1) && (iHsizeMemBuf1[1:0] < MW1) && (ErrCond == 1'b0) &&
    ((WaitWrCycMux == 1'b0) || (WaitEnWrFirstCyc == 1'b0)))
  begin
    if (((WaitWrCycVer == 1'b0) && (extracond == 1'b0)) ||
        ((iNewBurst == 1'b1) && (MemoryWrSt == 1'b1)))
```

This should be changed to:

```
if ((iWRITECYC == 1'b1) && (iHsizeMemBuf1[1:0] < MW1) && (ErrCond == 1'b0) &&
    ((WaitWrCycMux == 1'b0) || (WaitEnWrFirstCyc == 1'b0)))
  begin
    if (((WaitWrCycVer == 1'b0) && (extracond == 1'b0)) ||
        (iNewBurst == 1'b1))
```

Implications

When using SRAM or PSRAM static memory, if a 16-bit write to memory is followed by an 8-bit write, incorrect data is written to memory.

Workaround

None

Errata - Category 3

There are no Errata in this Category

Errata - Documentation

328398: TRM Errors

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p2-00LTD0,r0p2-00REL0, Fixed in r0p3-00REL0. Unchanged in this document.

Description

Chapter 2 Page 2-28, Figure 2-14.

There is still data shown as output onto the SMDATAIN bus after chip select signal (SMCS) and output enable (nSMOEN) signals are deasserted. This should not be the case since if the nSMOEN output is deasserted, this will make the memory's output go tristate, so other than the delay for it to go tristate there should not be any data coming into the SMC after the end of the transfer.

Table 3-5 is incorrect in its value of the WSTOEN register at reset. It should be 0x0.

Table 3-6 is incorrect in its value of the WSTWEN register at reset. It should be 0x1.

Figure 2-21 WSTWR timing is incorrect. It should be timed from the sampling of SMADDRVALID being asserted

Implications

None

Workaround

None

334526: TRM Figure 2-40 incorrectly mentions SMMEMCLK

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p3-00REL0, Fixed in r0p4-00REL0. New in this document.

Description

In the TRM, ARM_DDI_0236G, Figure 2-40, replace SMMEMCLK with SMCLK.

Implications

None

Workaround

None

334813: Incorrect Delay Number in TRM

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p3-00REL0, Fixed in r0p4-00REL0. New in this document.

Description

The last sentence on the bottom of Page 2-34 should read:

Figure 2-30 on page 2-35 shows an external synchronous wait applied to a zero wait continuous burst, where the read from location A+18 is delayed by three cycles.

Not two cycles as is incorrectly mentioned .

Implications

None

Workaround

None

341659: Error in Section 3.3.7 in Technical Reference Manual

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p3-00REL0,r0p4-00REL0, Open. New in this document.

Description

Section 3.3.7 states:

"Writing a 1 to this bit clears the write protect error status flag".

This should say:

"Writing a 1 to this bit clears the write timeout error status flag".

Implications

None

Workaround

None

350030: Incorrect halfword transfer comment in TRM

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p4-00REL0, Open. New in this document.

Description

Table 2-7 in the TRM incorrectly shows a halfword transfer as consisting of two transfers on a 32-bit bus. A halfword transfer will complete in one beat on a 32-bit bus.

Implications

none

Workaround

none

350850: Incorrect SMBSRx register bit assignments in TRM

Status

Affects: product PL093 Synch Static Mem Ctrller.

Fault status: Doc, Present in: r0p4-00REL0, Open. New in this document.

Description

In the Technical Reference Manual ARM DDI 0236H Page 3-16, Table 3-10 contains the description for the SMBSRx register bit assignments.

The wording in Table 3-10 under the description of the WaitToutErr bit should be changed from:

“Clears the write protect error status flag”

to:

“Clears the wait timeout error status flag”

Implications

none

Workaround

none

Errata - Software

There are no Errata in this category