Engineering Advice Note

ARM® Cortex®-A53 Reset Mode Clarification

Release Information

The following changes have been made to this Engineering Advice Note.

Document History

Date	Issue	Confidentiality	Change
27/06/2016	**A**	Non-Confidential	First release

Non-Confidential Proprietary Notice

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Confidentiality Status

Product Status

The information in this document is Final, that is for a developed product.

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Contents

Preface

This preface introduces the *ARM® Cortex®-A53 Reset Mode Clarification*.

Intended audience

This document is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the Cortex-A53 processor.

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *ARM® Cortex®-A53 Reset Mode Clarification*.
- The number ARM UAN0017.
- If applicable, the page numbers to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Cortex-A53 reset mode clarification

Technical Reference Manuals (TRMs) for the Cortex®-A57 and Cortex®-A72 processors define the *All cores Warm reset and L2 reset* mode, which is a valid reset mode supported by Cortex-A57 and Cortex-A72.

The All cores Warm reset and L2 reset mode is described in Table 1.

Table 1 All cores Warm reset and L2 reset

Reset combination	Signals	Value	Description
All cores Warm reset and L2 reset	**nCPUPORESET[N:0]**	All = 1	All logic, excluding Debug and ETM (**CLK** and **PCLKDBG**), is held in reset. All breakpoints and watchpoints are retained.
	nCORERESET[N:0]	All = 0	
	nPRESETDBG	1	
	nL2RESET	0	
	nMBISTRESET	1	

However, **nL2RESET** has a different implementation from Cortex-A57 and Cortex-A72. On Cortex-A53, the **nL2RESET** signal can be asserted only when you apply a cold reset (**nCPUPORESET**) to all the CPUs in a cluster. The All cores Warm reset and L2 reset mode is not valid on Cortex-A53 because **nL2RESET** also resets some of the debug logic in the top level of the processor, with details described below.

Note: The Cortex-A53 implementation complies with the ARMv8-A architecture.

The logic that is reset by **nL2RESET** but is not reset by **nCORERESET** is shown in Table 2.

Table 2 Logic and consequences

Logic		**Consequences**
• The *Snoop Control Unit* (SCU) and L2.		-
• All non-debug logic in the governors.		-
• Some of the signals driven to the cores.		-
• Some of the logic routing buses between the cores and the top-level ports, namely:	➢ The *Advanced Trace Bus* (ATB) bus from the ETM.	When reset is asserted, some trace that is up to two 32-bit words can be lost. You can avoid this issue by using the **AFVALIDM** or **AFREADYM** handshake to ensure that all trace data is flushed from the ETM to the system.
	➢ The debug APB bus from the core debug logic.	When **nL2RESET** is asserted, any *Advanced Peripheral Bus* (APB) access to registers in the core power domain behaves as if the core were powered off and returns an error, regardless of whether the APB access is in progress or just started. When the reset is deasserted, such accesses can still work. The registers under debug reset do not lose the values, that is, the debug programming can still be preserved.
	➢ The **TSVALUE** bus to the ETM.	If the ETM generates a timestamp packet while **nL2RESET** is asserted, the generated timestamp has the value 0.
	➢ The **COMMTX**, **COMMRX**, and **DBGNOPWRDWN** outputs.	The pins described above have reset values while **nL2RESET** is asserted. However, these pins return to previous values when they are deasserted.

To do a warm reset with debug active, the only supported reset combination on Cortex-A53 is the *Individual core warm reset with trace and debug active* mode, as described in Table 3.

Table 3 Individual core Warm reset with trace and debug active

Reset combination	Signals	Value	Description
Individual core warm reset with trace and debug active	**nCPUPORESET[CN:0]**	All = 1	Individual core is held in reset.
	nCORERESET[CN:0]	All = 0	
	nPRESETDBG	1	
	nL2RESET	1	
	nMBISTRESET	1	

Recommendation

Cortex-A53 does not support the All cores Warm reset and L2 reset mode. Therefore, ARM recommends that you do not implement this mode on Cortex-A53.

To achieve a similar functionality, use the Cluster Cold reset with debug active mode, and restore the debug programming after the CPU comes out of the reset. In this case, the system must have the ability to keep **nCORERESET** asserted until the debug programming is restored.

References

The following books are referred to in this document, and you can download them directly from the ARM infocenter at http://infocenter.arm.com.

- *ARM® Cortex®-A57 MPCore Processor Technical Reference Manual,* ARM DDI0488H.
- *ARM® Cortex®-A53 MPCore Processor Technical Reference Manual,* ARM DDI 0500G.
- *ARM® Cortex®-A72 MPCore Processor Technical Reference Manual,* ARM 100095_0002_04_en.