



Arm® Neoverse CMN-700 Coherent Mesh Network

Software Developer Errata Notice

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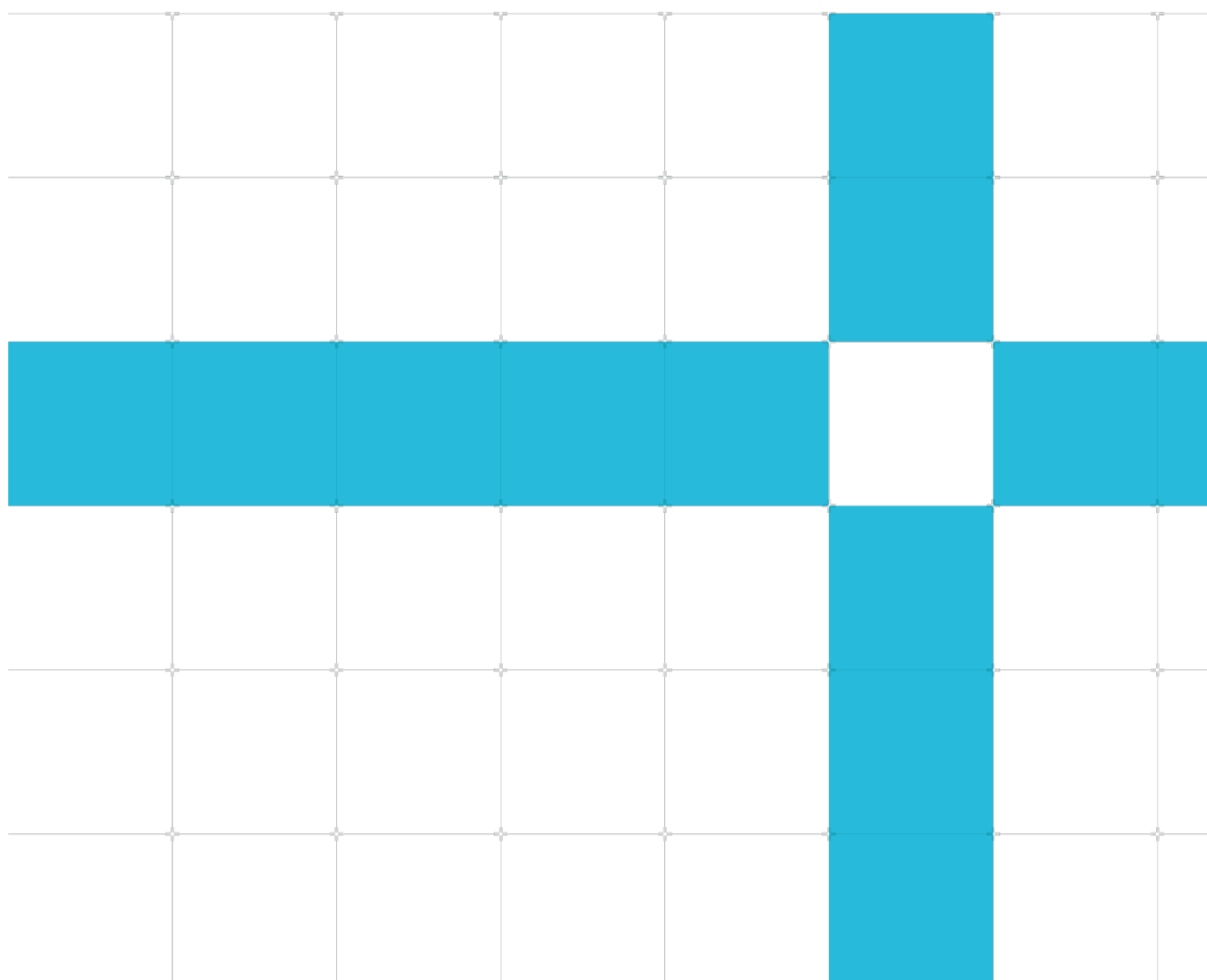
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This document contains all known errata since the r0p0 release of the product.



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Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The [errata summary table](#) identifies errata that have been fixed in each product revision.

13-Jul-2022: Changes in document version v6.0

ID	Status	Area	Category	Summary
2473100	New	Programmer	Category B	Multi-chip SMP DVM operations can cause hang

18-Feb-2022: Changes in document version v5.0

ID	Status	Area	Category	Summary
2418894	New	Programmer	Category C	CCG CCLA PMU events cannot be counted correctly

07-Jan-2022: Changes in document version v4.0

No new or updated errata in this document version.

01-Oct-2021: Changes in document version v3.0

No new or updated errata in this document version.

03-May-2021: Changes in document version v2.0

ID	Status	Area	Category	Summary
2128441	New	Programmer	Category B	Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic
2125871	New	Programmer	Category C	HN-I RAS syndrome registers do not capture correct opcode

15-Dec-2020: Changes in document version v1.0

No errata in this document version.

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
2128441	Programmer	Category B	Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic	r0p0	r1p0
2473100	Programmer	Category B	Multi-chip SMP DVM operations can cause hang	r0p0, r1p0, r2p0	Open
2418894	Programmer	Category C	CCG CCLA PMU events cannot be counted correctly	r2p0	Open
2125871	Programmer	Category C	HN-I RAS syndrome registers do not capture correct opcode	r0p0	r1p0

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

2128441

Multi-chip SMP data corruption or hang in the presence of CPU and PCIe traffic

Status

Affects: CMN-700

Fault Type: Programmer CAT-B

Fault Status: Present in r0p0. Fixed in r1p0

Description

High-bandwidth CPU and PCIe traffic targeting a remote chip can result in data corruption or hangs.

Configurations Affected

All configurations that have PCIe RNI instantiated in CCG.

Conditions

High bandwidth CPU and PCIe traffic targeting the remote chip.

Implications

Data corruption and/or an eventual hang in the presence of CPU and PCIe traffic.

Workaround

Program `por_ccg_ha_cxpctl_link0_ctl.lnk0_num_reqcrds` to a value of 4'h3 which allocates only 75% of the available credits to link 0.

2473100

Multi-chip SMP DVM operations can cause hang

Status

Affects: CMN-700

Fault Type: Programmer CatB

Fault Status: Present in r0p0, r1p0, r2p0. Open.

Description

DVM operations may hang in the presence of other traffic targeting remote chips in CMN SMP configurations.

Configurations Affected

Any multi-chip SMP CMN configuration.

Conditions

DVM operations and non-DVM op transactions targeting a remote chip in SMP configurations.

Implications

If the conditions are met, DVM operations might not complete, which might cause deadlocks.

Workaround

Disable CML Early DVM completions by writing 1'b0 to `por_ccg_ra_aux_ctl.dvm_earlycomp_en`

Also, do not change the following register values from the default settings:

- `por_ccg_ra_ccprctl_link0_ctl.lnk0_send_compack`: Default is 1'b0
- `por_ccg_ha_ccprctl_link0_ctl.lnk0_send_compack`: Default is 1'b0

Note

This might impact cross-chip DVM performance.

Category B (rare)

There are no errata in this category.

Category C

2418894

CCG CCLA PMU events cannot be counted correctly

Status

Affects: CMN-700

Fault Type: Programmer CAT-C

Fault status: Present in r2p0. Open.

Description

The CCG PMU events cannot be counted correctly for CCG configurations with PCIE_ENABLE parameter set

Configurations affected

CMN configurations that include CCG with PCIE_ENABLE parameter set

Conditions

Programming CMN CCG CCLA PMU events to be counted.

Implications

CCG CCLA PMU events cannot be counted correctly. This may reduce the ability to analyze CXS link efficiency for multi-chip traffic.

The following events will not be counted correctly:

- 8'h21: LA_RX_CXS : number of RX CXS beats
- 8'h22: LA_TX_CXS : number of TX CXS beats
- 8'h23: LA_RX_CXS_AVG_SIZE : average size of RX CXS beats
- 8'h24: LA_TX_CXS_AVG_SIZE : average size of TX CXS beats
- 8'h25: LA_TX_CXS_LCRD_BACKPRESSURE : CXS backpressure due to lack of CXS credits
- 8'h26: LA_LINK_CRDBUF_OCC : CCLA RX RAM buffer occupancy
- 8'h27: LA_LINK_CRDBUF_ALLOC: CCLA RX RAM buffer allocation

Workaround

No workaround available.

2125871

HN-I RAS syndrome registers do not capture correct opcode

Status

Affects: CMN-700

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Fixed in r1p0.

Description

The OPCODE field in the HN-I por_hni_errmisc RAS Syndrome register does not correctly capture the new REQ opcodes introduced in CHI-E.

Configurations Affected

All CMN-700 configurations that use RAS error logging.

Conditions

A RAS error triggered by a new CHI-E transaction that causes the syndrome to be captured in the por_hni_errmisc register on a transaction processed by HN-I/P/D/V/T.

Implications

A read of the por_hni_errmisc.OPCODE field may return an incorrect opcode. The opcode does not properly reflect an error on a CHI-E opcode that has bit [6] set.

Workaround

RAS handler and software can use the following table indicating which por_hni_errmisc.OPCODE values are affected by aliasing due to this issue. If a RAS error involves opcodes listed as **Yes**, software can indicate that either opcode could have been the actual opcode involved in the error. Note that some cases with opcode[6]=0 are Reserved in the *CHI-E Specification*.

CHI-E REQ Opcodes			
Opcode[5:0]	Opcode[6]=0	Opcode[6]=1	Can Opcode[6]=1 RAS error happen at HN-X?
0x01	ReadShared	MakeReadUnique	Yes
0x02	ReadClean	WriteEvictOrEvict	No
0x03	ReadOnce	WriteUniqueZero	Yes
0x04	ReadNoSnp	WriteNoSnpZero	No
0x07	ReadUnique	StashOnceSepShared	No
0x08	CleanShared	StashOnceSepUnique	No
0x0C	MakeUnique	ReadPreferUnique	Yes
0x10	Reserved	WriteNoSnpFullCleanSh	No
0x11	ReadNoSnpSep	WriteNoSnpFullCleanInv	No
0x12	Reserved	WriteNoSnpFullCleanSh-PerSep	No
0x14	DVMOp	WriteUniqueFullCleanSh	Yes
0x16	Reserved (WriteCleanPtl)	WriteUniqueFullCleanSh-PerSep	Yes
0x18	WriteUniquePtl	WriteBackFullCleanSh	Yes
0x19	WriteUniqueFull	WriteBackFullCleanInv	Yes
0x1A	WriteBackPtl	WriteBackFullCleanSh-PerSep	Yes
0x1C	WriteNoSnpPtl	WriteCleanFullCleanSh	Yes
0x1E	Reserved	WriteCleanFullCleanSh-PerSep	Yes
0x20	WriteUniqueFullStash	WriteNoSnpPtlCleanSh	No
0x21	WriteUniquePtlStash	WriteNoSnpPtlCleanInv	No
0x22	StashOnceShared	WriteNoSnpPtlCleanSh-PerSep	No
0x24	ReadOnceCleanInvalid	WriteUniquePtlCleanSh	Yes
0x26	ReadNotSharedDirty	WriteUniquePtlCleanSh-PerSep	Yes