Revision 1.0

ARM
LPDDR2 (DMC-342)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p0 of DMC-342 AXI LPDDRII Dyn Mem Ctrl

Proprietary notice

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Feedback on this document

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- The document title
- The documents number
- The page number(s) to which your comments refer
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General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behaviour occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a ‘work-around’ where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behaviour that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behaviour that contravenes the specified behaviour and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behaviour that was not the originally intended behaviour but should not cause any problems in applications.