CoreLink™
Network Interconnect (NIC-301)
Errata Notice

This document contains all errata known at the date of issue in releases from revision r2p0 up to and including revision r2p1

Errata present in prior revisions of the IP are detailed in earlier revisions of the document.

Proprietary notice

Document confidentiality status

This document is Non Confidential.

Web address

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- The product name
- A concise explanation of your comments.

Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

20 Jul 2010: Changes in Document v2.0

Page	Status	ID	Cat	Summary
10	New	738899	Cat 2	Incorrect timing isolation for 1:n & m:1 for modifiable clock boundaries
9	New	736303	Cat 2	Read data corruption possible for 4:1 and 8:1 downsizers

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r2p0-00rel0	r2p1-00rel0
736303	Cat 2	Read data corruption possible for 4:1 and 8:1 downsizers	X	X
738899	Cat 2	Incorrect timing isolation for 1:n & m:1 for modifiable clock boundaries	X	X

Errata - Category 1

No errata in this category.

Errata - Category 2

736303: Read data corruption possible for 4:1 and 8:1 downsizers

Status

Affects: product NIC-301 AMBA 3 Network IC .

Fault status: Cat 2, Present in: r2p0-00rel0, r2p1-00rel0, Open.

Description

In a 4:1 or a 8:1 downsizer read data corruption may occur if all the following conditions are true:

1. Returned read data is being upsized.
2. A downsized beat is being returned to the most significant position of the upsized bus.
3. RREADY is held low
4. Synthesis tool interprets X as a non-zero value

The error is not visible in RTL simulation, it is only visible at gate level and is not detected by normal LEC flows.

Implications

If the above scenario occurs then the returned read data of downsized transactions may be incorrect. For example, for a 128:32 bit downsizer then the upper 32 bits of each beat may be duplicated onto other 32bit locations with each 128 bit beat.

e.g.

0x11111111-22222222-33333333-44444444

may become

0x11111111-11111111-11111111-44444444

The exact nature of the duplication will depend on the synthesis tool.

Workaround

If it is possible to ensure that no AXI read transactions are transmitted across the downsizer that are wider than the outgoing bus then this defect does not apply.

If this cannot be guaranteed then there is no other software work around.

Contact support-fabric@arm.com for a pre-silicon implementation work around.

738899: Incorrect timing isolation for 1:n & m:1 for modifiable clock boundaries

Status

Affects: product NIC-301 AMBA 3 Network IC .

Fault status: Cat 2, Present in: r2p0-00rel0, r2p1-00rel0, Open.

Description

If a clock boundary is programmable then the payload signals on the AR, AW and W channels may be synthesized with underconstrained paths when m:1 synchronisation is programmed by writing 2'b01 to the sync_mode register.

If a clock boundary is programmable then the payload signals on the R and B channels may be synthesized with underconstrained paths when 1:n synchronisation is programmed by writing 2'b10 to the sync_mode register.

The exceptions used in the delivered synthesis scripts assume that the payload crossing the boundary will have a full destination clock period before they are captured at the destination. Therefore if a configuration meets all the following criteria:

1. Has multiple clock domains
2. Has a modifiable clock boundary
3. Is synthesized using the delivered constraints, specifically the exceptions file
4. Synthesized with the destination clock period different to the source clock period

then the payload will incorrectly be assigned a max delay equal to the destination period for sync up or sync down operation.

Implications

If a modifiable clock boundary is programmed for synchronous 1:m or synchronous n:1 operation then the payload for some channels may not be captured correctly when crossing the boundary.

Workaround

Program an m:n clock boundary when a 1:n or m:1 clock boundary is desired.

This is achieved by writing 2'b11 to the sync_mode register of the required register block.

Note that if there are multiple boundary crossings then each boundary crossing will have it's own register block.

Errata - Category 3

No errata in this category.