Arm Cortex-X3 (MP141)

Software Developer Errata Notice

Date of issue: 10-Aug-2022

Non-Confidential

Document version: v9.0

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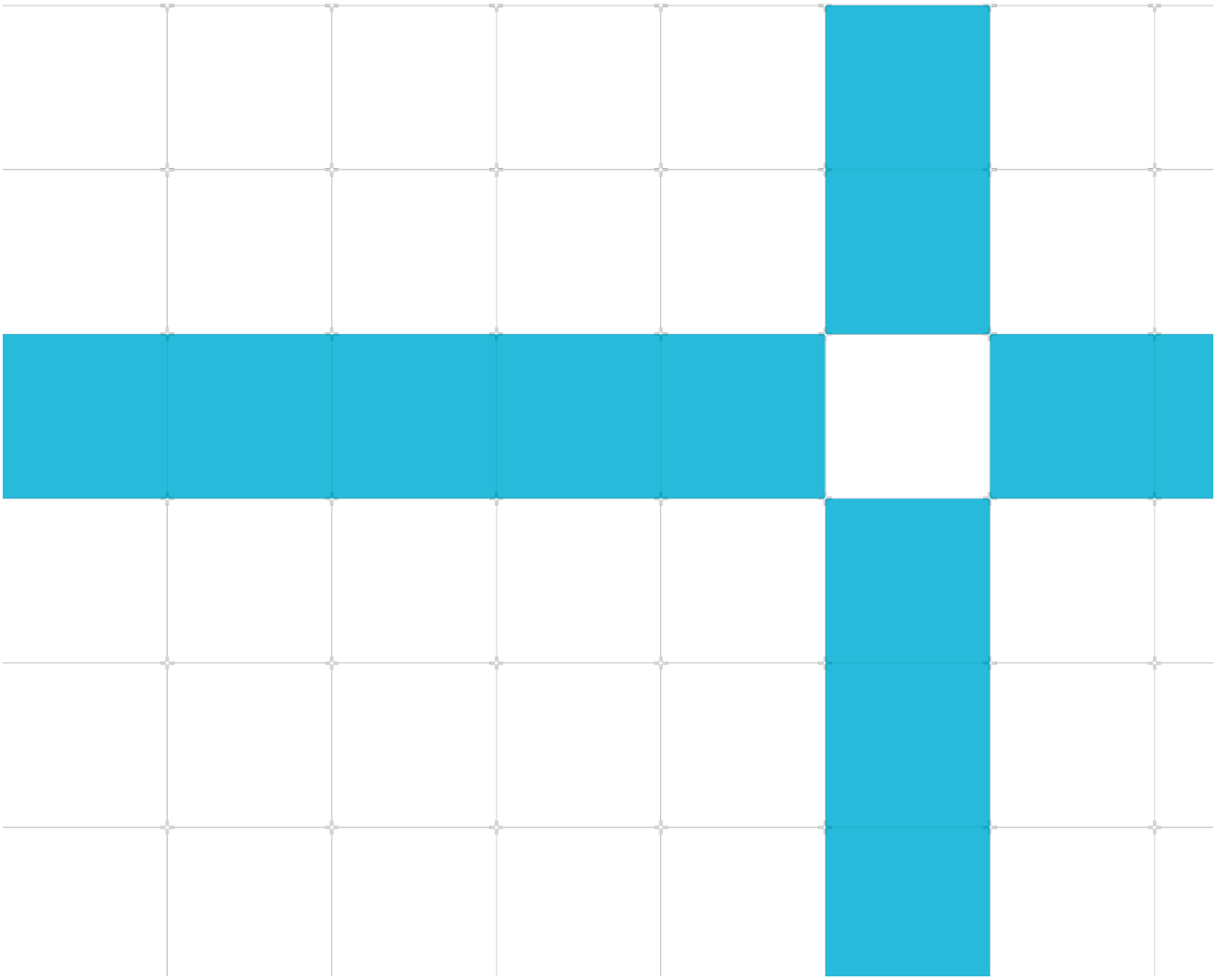
This document contains all known errata since the r0p0 release of the product.



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Contents

r1p0 implementation fixes

Note the following errata might be fixed in some implementations of r1p0. This can be determined by reading the REVIDR_EL1 register where a set bit indicates that the erratum is fixed in this part.

REVIDR_EL1[0]	2641945 L1 hardware prefetcher might cause deadlock

Note that there is no change to the MIDR_EL1 which remains at r1p0. Software will identify this release through the combination of MIDR_EL1 and REVIDR_EL1.

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The **errata summary table** identifies errata that have been fixed in each product revision.

10-Aug-2022: Changes in document version v9.0

ID	Status	Area	Category	Summary
2302506	Updated	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch
2701951	New	Programmer	Category B	The core might fetch stale instruction from memory when both Stage 1 Translation and Instruction Cache are Disabled with Stage 2 forced Write-Back
2652014	New	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect
2676363	New	Programmer	Category C	Execution of STG instructions in close proximity might cause loss of MTE allocation tag data
2693826	New	Programmer	Category C	MTE tag check fail seen on first half of a cache-line crossing load does not get reported
2693832	New	Programmer	Category C	MTE checked load might read an old value of allocation tag by not complying with address dependency ordering
2704518	New	Programmer	Category C	Incorrect value reported for SPE PMU event SAMPLE_FEED
2712633	New	Programmer	Category C	Incorrect read value for Performance Monitors Configuration Register EX field

02-May-2022: Changes in document version v8.0

ID	Status	Area	Category	Summary
2266875	Updated	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits
2302506	Updated	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch
2313909	Updated	Programmer	Category B	Denied power down request might prevent completion of future power down request
2372204	Updated	Programmer	Category B	Translation table walk folding into an L1 prefetch might cause data corruption
2390455	Updated	Programmer	Category B	A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing
2615812	New	Programmer	Category B	Entry into the Full Retention power mode might cause corruption on Itag and BTB RAMs
2641945	New	Programmer	Category B	L1 hardware prefetcher might cause deadlock
2231012	Updated	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands

ID	Status	Area	Category	Summary
2233619	Updated	Programmer	Category C	Lower priority exception might be reported when abort condition is detected at both stages of translation
2252367	Updated	Programmer	Category C	L1 Data poison is not cleared by a store
2275209	Updated	Programmer	Category C	SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions
2277321	Updated	Programmer	Category C	PMU L1D_CACHE_REFILL_OUTER is inaccurate
2299191	Updated	Programmer	Category C	L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop
2302585	Updated	Programmer	Category C	CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1
2307825	Updated	Programmer	Category C	ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk
2312833	Updated	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered
2343688	New	Programmer	Category C	STALL_BACKEND_MEM, Memory stall cycles AMU event count incorrectly
2351560	New	Programmer	Category C	ERXPFGCDN_EL1 register is incorrectly written on Warm reset
2359164	New	Programmer	Category C	Incorrect read value for Performance Monitors Configuration Register
2390828	New	Programmer	Category C	PMU MEM_ACCESS_CHECKED_RD and MEM_ACCESS_CHECKED_WR inaccurate
2391679	New	Programmer	Category C	Software-step not done after exit from Debug state with an illegal value in DSPSR
2409463	New	Programmer	Category C	Incorrect read value for Performance Monitors Control Register
2409683	New	Programmer	Category C	Incorrect sampling of SPE events "tlb_access" for an unaligned SVE load instruction with no active elements
2441604	New	Programmer	Category C	PMU STALL_SLOT_BACKEND and STALL_SLOT_FRONTEND events count incorrectly
2612736	New	Programmer	Category C	Read to dump the instruction cache contents while in Debug state results in deadlock

17-Dec-2021: Changes in document version v7.0

ID	Status	Area	Category	Summary
2302506	New	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch
2372204	New	Programmer	Category B	Translation table walk folding into an L1 prefetch might cause data corruption
2390455	New	Programmer	Category B	A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing

03-Nov-2021: Changes in document version v6.0

ID	Status	Area	Category	Summary
2313909	New	Programmer	Category B	Denied power down request might prevent completion of future power down request
2233619	New	Programmer	Category C	Lower priority exception might be reported when abort condition is detected at both stages of translation
2275209	New	Programmer	Category C	SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions
2299191	New	Programmer	Category C	L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop
2302585	New	Programmer	Category C	CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1
2307825	New	Programmer	Category C	ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk
2312833	New	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered

08-Sep-2021: Changes in document version v5.0

ID	Status	Area	Category	Summary
2266875	New	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits
2232775	New	Programmer	Category C	Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work
2277321	New	Programmer	Category C	PMU L1D_CACHE_REFILL_OUTER is inaccurate

05-Aug-2021: Changes in document version v4.0

ID	Status	Area	Category	Summary
2133701	Updated	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode
2138930	Updated	Programmer	Category B	The CPP instruction will apply to an incorrect EL context
2147714	New	Programmer	Category B	A CFP instruction might not invalidate the correct resources
2156436	Updated	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1
2184829	New	Programmer	Category B	Instruction cache contents might be corrupted when a speculative instruction fetch is initiated for non-cacheable page
2188426	New	Programmer	Category B	Update to MPMM Configuration might not modify MPMM behavior
2214778	New	Programmer	Category B	PDP deadlock due to CMP/CMN + B.AL/B.NV fusion
2222929	New	Programmer	Category B	TRBE might cause a data write to an out-of-range address which is not reserved for TRBE
2073992	Updated	Programmer	Category C	Tag Check Fault might not be reported for some Vector Load instructions with SP as base register
2108450	Updated	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur
2113892	Updated	Programmer	Category C	L2 tag single-bit ECC error might cause deadlock when using the SIP prefetcher

ID	Status	Area	Category	Summary
2115480	Updated	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd
2115856	Updated	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level
2117589	Updated	Programmer	Category C	Hardware prefetcher PMU events count incorrectly
2119356	Updated	Programmer	Category C	L2 data RAM or L2 TQ data RAM might fail to report ECC errors
2141643	Updated	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely
2143137	Updated	Programmer	Category C	Some SVE PMU events count incorrectly
2142812	Updated	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect
2154264	Updated	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect
2159151	Updated	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data
2165452	Updated	Programmer	Category C	PMU_HOVFS event is not always exported when self-hosted trace is disabled
2179550	New	Programmer	Category C	An SError might not be reported for an atomic store that encounters data poison
2189539	New	Programmer	Category C	64 bit source SVE PMULLB/T not considered Cryptography instruction
2227172	New	Programmer	Category C	Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering
2230110	New	Programmer	Category C	Reads of DISR_EL1 incorrectly return 0s while in Debug State
2231012	New	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands
2236039	New	Programmer	Category C	DRPS instruction is not treated as UNDEFINED at EL0 in Debug state
2237091	New	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered
2240363	New	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with vector operands in certain configurations
2240293	New	Programmer	Category C	TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled
2243142	New	Programmer	Category C	L1 MTE Tag poison is not cleared
2243856	New	Programmer	Category C	ELR_ELx[63:48] might hold incorrect value when PE disables address translation
2252367	New	Programmer	Category C	L1 Data poison is not cleared by a store

10-Jun-2021: Changes in document version v3.0

ID	Status	Area	Category	Summary
2156436	New	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1
2143137	New	Programmer	Category C	Some SVE PMU events count incorrectly
2154264	New	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect
2159151	New	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data
2165452	New	Programmer	Category C	PMU_HOVFS event is not always exported when self-hosted trace is disabled
1880119	New	Programmer	Category C	Noncompliance with prioritization of Exception Catch debug events

30-Apr-2021: Changes in document version v2.0

ID	Status	Area	Category	Summary
2070301	New	Programmer	Category B	Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock
2133701	New	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode
2138930	New	Programmer	Category B	The CPP instruction will apply to an incorrect EL context
2073992	New	Programmer	Category C	Tag Check Fault might not be reported for some Vector Load instructions with SP as base register
2108450	New	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur
2113892	New	Programmer	Category C	L2 tag single-bit ECC error might cause deadlock when using the SIP prefetcher
2115480	New	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd
2115856	New	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level
2117121	New	Programmer	Category C	MPAM value associated with instruction fetch might be incorrect
2117589	New	Programmer	Category C	Hardware prefetcher PMU events count incorrectly
2119356	New	Programmer	Category C	L2 data RAM or L2 TQ data RAM might fail to report ECC errors
2141643	New	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely
2142812	New	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect

26-Feb-2021: Changes in document version v1.0

No errata in this document version.

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
2070301	Programmer	Category B	Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock	r0p0, r1p0, r1p1	Open
2133701	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode	r0p0	r1p0
2138930	Programmer	Category B	The CPP instruction will apply to an incorrect EL context	r0p0	r1p0
2147714	Programmer	Category B	A CFP instruction might not invalidate the correct resources	r0p0	r1p0
2156436	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1	r0p0	r1p0
2184829	Programmer	Category B	Instruction cache contents might be corrupted when a speculative instruction fetch is initiated for non-cacheable page	r0p0	r1p0
2188426	Programmer	Category B	Update to MPMM Configuration might not modify MPMM behavior	r0p0	r1p0
2214778	Programmer	Category B	PDP deadlock due to CMP/CMN + B.AL/B.NV fusion	r0p0	r1p0
2222929	Programmer	Category B	TRBE might cause a data write to an out-of-range address which is not reserved for TRBE	r0p0	r1p0
2266875	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits	r0p0, r1p0	r1p1
2302506	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch	r0p0, r1p0, r1p1	Open
2313909	Programmer	Category B	Denied power down request might prevent completion of future power down request	r0p0, r1p0	r1p1
2372204	Programmer	Category B	Translation table walk folding into an L1 prefetch might cause data corruption	r0p0, r1p0	r1p1

ID	Area	Category	Summary	Found in versions	Fixed in version
2390455	Programmer	Category B	A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing	r0p0, r1p0	r1p1
2615812	Programmer	Category B	Entry into the Full Retention power mode might cause corruption on Itag and BTB RAMs	r0p0, r1p0, r1p1	Open
2641945	Programmer	Category B	L1 hardware prefetcher might cause deadlock	r0p0, r1p0	r1p1
2701951	Programmer	Category B	The core might fetch stale instruction from memory when both Stage 1 Translation and Instruction Cache are Disabled with Stage 2 forced Write-Back	r0p0, r1p0, r1p1	Open
1880119	Programmer	Category C	Noncompliance with prioritization of Exception Catch debug events	r0p0, r1p0, r1p1	Open
2073992	Programmer	Category C	Tag Check Fault might not be reported for some Vector Load instructions with SP as base register	r0p0	r1p0
2108450	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur	r0p0	r1p0
2113892	Programmer	Category C	L2 tag single-bit ECC error might cause deadlock when using the SIP prefetcher	r0p0	r1p0
2115480	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd	r0p0	r1p0
2115856	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level	r0p0	r1p0
2117121	Programmer	Category C	MPAM value associated with instruction fetch might be incorrect	r0p0, r1p0, r1p1	Open
2117589	Programmer	Category C	Hardware prefetcher PMU events count incorrectly	r0p0	r1p0
2119356	Programmer	Category C	L2 data RAM or L2 TQ data RAM might fail to report ECC errors	r0p0	r1p0
2141643	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely	r0p0	r1p0

ID	Area	Category	Summary	Found in versions	Fixed in version
2142812	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect	r0p0	r1p0
2143137	Programmer	Category C	Some SVE PMU events count incorrectly	r0p0	r1p0
2154264	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect	r0p0	r1p0
2159151	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data	r0p0	r1p0
2165452	Programmer	Category C	PMU_HOVFS event is not always exported when self-hosted trace is disabled	r0p0	r1p0
2179550	Programmer	Category C	An SError might not be reported for an atomic store that encounters data poison	r0p0	r1p0
2189539	Programmer	Category C	64 bit source SVE PMULLB/T not considered Cryptography instruction	r0p0	r1p0
2227172	Programmer	Category C	Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering	r0p0	r1p0
2230110	Programmer	Category C	Reads of DISR_EL1 incorrectly return 0s while in Debug State	r0p0	r1p0
2231012	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands	r0p0, r1p0	r1p1
2232775	Programmer	Category C	Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work	r0p0	r1p0
2233619	Programmer	Category C	Lower priority exception might be reported when abort condition is detected at both stages of translation	r0p0, r1p0	r1p1
2236039	Programmer	Category C	DRPS instruction is not treated as UNDEFINED at EL0 in Debug state	r0p0	r1p0
2237091	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered	r0p0	r1p0

ID	Area	Category	Summary	Found in versions	Fixed in version
2240293	Programmer	Category C	TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled	r0p0	r1p0
2240363	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with vector operands in certain configurations	r0p0	r1p0
2243142	Programmer	Category C	L1 MTE Tag poison is not cleared	r0p0	r1p0
2243856	Programmer	Category C	ELR_ELx[63:48] might hold incorrect value when PE disables address translation	r0p0	r1p0
2252367	Programmer	Category C	L1 Data poison is not cleared by a store	r0p0, r1p0	r1p1
2275209	Programmer	Category C	SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions	r0p0, r1p0	r1p1
2277321	Programmer	Category C	PMU L1D_CACHE_REFILL_OUTER is inaccurate	r0p0, r1p0	r1p1
2299191	Programmer	Category C	L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop	r0p0, r1p0	r1p1
2302585	Programmer	Category C	CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1	r0p0, r1p0	r1p1
2307825	Programmer	Category C	ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk	r0p0, r1p0	r1p1
2312833	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered	r0p0, r1p0	r1p1
2343688	Programmer	Category C	STALL_BACKEND_MEM, Memory stall cycles AMU event count incorrectly	r0p0, r1p0	r1p1
2351560	Programmer	Category C	ERXPFGCDN_EL1 register is incorrectly written on Warm reset	r0p0, r1p0	r1p1
2359164	Programmer	Category C	Incorrect read value for Performance Monitors Configuration Register	r0p0, r1p0	r1p1
2390828	Programmer	Category C	PMU MEM_ACCESS_CHECKED_RD and MEM_ACCESS_CHECKED_WR inaccurate	r0p0, r1p0	r1p1

ID	Area	Category	Summary	Found in versions	Fixed in version
2391679	Programmer	Category C	Software-step not done after exit from Debug state with an illegal value in DSPSR	r0p0, r1p0, r1p1	Open
2409463	Programmer	Category C	Incorrect read value for Performance Monitors Control Register	r0p0, r1p0	r1p1
2409683	Programmer	Category C	Incorrect sampling of SPE events "tlb_access" for an unaligned SVE load instruction with no active elements	r0p0, r1p0	r1p1
2441604	Programmer	Category C	PMU STALL_SLOT_BACKEND and STALL_SLOT_FRONTEND events count incorrectly	r0p0, r1p0	r1p1
2612736	Programmer	Category C	Read to dump the instruction cache contents while in Debug state results in deadlock	r0p0, r1p0, r1p1	Open
2652014	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect	r0p0, r1p0, r1p1	Open
2676363	Programmer	Category C	Execution of STG instructions in close proximity might cause loss of MTE allocation tag data	r0p0, r1p0, r1p1	Open
2693826	Programmer	Category C	MTE tag check fail seen on first half of a cache-line crossing load does not get reported	r0p0, r1p0, r1p1	Open
2693832	Programmer	Category C	MTE checked load might read an old value of allocation tag by not complying with address dependency ordering	r0p0, r1p0, r1p1	Open
2704518	Programmer	Category C	Incorrect value reported for SPE PMU event SAMPLE_FEED	r0p0, r1p0, r1p1	Open
2712633	Programmer	Category C	Incorrect read value for Performance Monitors Configuration Register EX field	r0p0, r1p0, r1p1	Open

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

2070301
Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0, r1p1. Open.

Description

If the data prefetcher is disabled (by an MSR to CPUECTLR register) while a prefetch TLB miss is outstanding, the processor might deadlock on the next context switch.

Configurations Affected

All configurations are affected.

Conditions

- MSR write to CPUECTLR register that disables the data prefetcher.
- A TLB miss from the prefetch TLB is outstanding.

Implications

If the above conditions are met, a deadlock might occur on the next context switch.

Workaround

- Workaround option 1:
  If the following code surrounds the MSR, it will prevent the erratum from happening:
  - CPP
  - DSB
  - ISB
  - MSR CPUECTLR - disabling the prefetcher
  - ISB

- Workaround option 2:
  Place the data prefetcher in the most conservative mode instead of disabling it. This will greatly reduce prefetches but not eliminate them. This is accomplished by writing the following bits to the

value indicated:
- ECTLR2[14:11], PF_MODE= 4'b1001

2133701
Trace data might get overwritten in TRBE FILL mode

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Trace Buffer memory size is defined using base pointer and limit pointer in the Trace Buffer Extension (TRBE) programming model. In trace buffer fill mode, TRBE is expected to generate an interrupt and stop the collection of trace after reaching the limit pointer. Due to this erratum, under some microarchitecture conditions, TRBE might roll back to the base pointer after generating an interrupt and continue to write at the base pointer, and up to three cache lines after the base pointer before the collection stops.

Configurations Affected

This erratum affects all configurations.

Conditions

1. ETE and TRBE are enabled.
2. ETE is in a trace allowed region.
3. TRBLIMITR_EL1[2:1] is programmed to 2'b00.

Implications

Due to this erratum, trace data present at the base pointer location and up to three cache lines after the base pointer might get overwritten. The current write pointer also increments by same number of cache line locations.

Workaround

Software can program 256 bytes of ignore packets starting from the base pointer and offset the write pointer TRBPTR_EL1 by 256 bytes before enabling TBE. That ensures oldest trace is not corrupted.

2138930
The CPP instruction will apply to an incorrect EL context

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The CPP instruction will not operate on the desired EL as encoded in the instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A CPP instruction is executed.

Implications

The CPP instruction will cause the hardware prefetcher to invalidate the hardware prefetcher state associated with an EL other than the EL encoded in the instruction.

Workaround

Set CPUACTLR5_EL1[44] which will cause the CPP instruction to invalidate hardware prefetcher state trained from any EL.

2147714
A CFP instruction might not invalidate the correct resources

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Executing a CFP instruction under certain conditions might not invalidate resources specified by the instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A CFP instruction is executed.
2. The Exception level specified in the instruction is EL0.
3. HCR_EL2.TGE==1 and HCR_EL2.E2H==1.

Implications

If the previous conditions are met, then the CFP instruction might not invalidate branch predictor resources associated with EL0 context managed by EL2.

Workaround

This erratum can be avoided by setting CPUACTLR_EL1[22]=1. Setting CPUACTLR_EL1[22] will cause the CFP instruction to invalidate all branch predictor resources regardless of context.

Using this workaround might cause the PE to encounter another erratum. Please refer to erratum ID 2243856 "ELR_ELx[63:48] might hold incorrect value when PE disables address translation" for more details.

2156436
Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The Trace Buffer Extension (TRBE) can be used by software to store trace packets from Embedded Trace Extension (ETE) unit to memory. The TRBE unit interfaces with the MMU for translating a virtual address to a physical address. Once a physical address is available, the TRBE unit sends trace packets to the L2 unit to be stored to the memory. The TRBE unit requests a new translation to the MMU when a virtual address crosses the 4K page boundary. Due to this erratum, if a pending translation request from Exception level EL0 or EL1 is serviced after the PE switches context to Exception level EL2, then translation with an incorrect ASID might be provided to the TRBE unit. This can lead to a write to a page with the incorrect ASID.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The TRBE is enabled.
2. Owning Exception level is EL1.
3. TRBLIMITR_EL1.nVM is set to 0, such that the trace buffer pointer addresses are virtual addresses in the EL1&0 translation regime using the current ASID from TTBRx_EL1. This means that the page is marked nG (non-global page).
4. The TRBE unit requests a memory translation request.
5. Before the above memory translation request completes, a context switch occurs from EL0 or EL1, to EL2.

Implications

If the above conditions are met, under certain microarchitectural conditions, incorrect physical address and page attributes from a different ASID might be provided to the TRBE unit. The TRBE might then write to memory using incorrect page attributes from another ASID, leading to a write that is not expected.

Workaround

The software should use global pages (nG=0) for the pages that are used by the TRBE to store data when owning Exception level is EL1.

2184829
Instruction cache contents might be corrupted when a speculative instruction fetch is initiated for non-cacheable page

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When the CPU initiates a speculative instruction fetch from a memory location with a non-cacheable memory, the response might be incorrectly written into the instruction cache. This written data might corrupt the instructions associated with an unrelated address. When the CPU fetches the instruction from this corrupted instruction cache line, the CPU might execute incorrect instructions.

Configurations Affected

The erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The CPU initiates a speculative instruction fetch from a memory location with a non-cacheable Normal memory or a Device memory. This memory location is not marked as execute-never.
2. An older branch instruction in the program order is newly identified in the front-end pipeline. This branch flushes the frontend pipeline.

Implications

When the above conditions are met with certain rare timing events, the instruction cache line associated with a different address might be modified by the response for the memory location with a non-cacheable memory. If the CPU reads instruction from this address, then the CPU might execute incorrect instructions stored in the instruction cache.

Workaround

Setting CPUACTLR_EL1[14] disables regional clock gating for the instruction fetch unit. This workaround might cause additional power in the clock tree for the instruction fetch unit. This workaround has no performance impact.

2188426
Update to MPMM Configuration might not modify MPMM behavior

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Attempts to modify the MPMM state (MPMM enable or MPMM gear) by completing an SPR write or Utility bus write to an MPMM-related configuration register will not change the internal MPMM state. A second write of the same data is required to affect the change.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under either of the the following conditions:

1. An MSR write occurs to the MPMM control registers.
2. A Utility bus write occurs to the MPMM control registers.

Implications

The first MPMM control register write with a new value will not affect the behavior of the MPMM logic.

Workaround

MSR or Utility bus writes to the MPMM control registers should be repeated twice with the same written data value in order for the write to affect the logic.

2214778
PDP deadlock due to CMP/CMN + B.AL/B.NV fusion

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When Performance Defined Power (PDP) is enabled, a Compare (CMP) or Compare negative (CMN) instruction followed by a conditional branch of form B.AL or B.NV might cause a deadlock.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PDP configuration is enabled.
2. Execution of CMP/CMN, followed by B.AL/B.NV.

Implications

If above conditions are met, then a deadlock might result, requiring a reset of the processor.

Workaround

This erratum can be avoided by setting CPUACTLR5_EL1[17] to 1 and applying following patch. These instructions are not expected to be present in the code often, so any performance impact should be minimal. The code sequence should be applied early in the boot sequence prior to any of the possible errata conditions being met.

```
    LDR x0,=0x0
    MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
    LDR x0,=0x005400000E
    MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
    LDR x0,=0x00FF00001E
    MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
    LDR x0,=0x800000000003FF
    MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0
    ISB
```

2222929
TRBE might cause a data write to an out-of-range address which is not reserved for TRBE

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Trace buffer memory size is defined using base pointer and limit pointer in Trace Buffer Extension (TRBE) programming model. TRBE is expected to wrap to base pointer without crossing the limit pointer. Because of this erratum, under some conditions, TRBE might generate a write to the next virtually addressed page following the last page of TRBE address space.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Embedded Trace Extension (ETE) and TRBE are enabled.
2. ETE is in trace allowed region.
3. TRBE current pointer is at last page of Trace buffer.
4. TRBE requests translation for the last page.
5. LS indicates to TRBE that it is unable to service the translation request.

Implications

When previous conditions are met under rare microarchitectural conditions, TRBE might incorrectly generate a data write to the next virtually addressed page following the last page of Trace Buffer. This can lead to data corruption if that page is currently used by another application and result in loss of trace up to 64 bytes.

Workaround

The software can mark as not valid the next page following the last TRBE page, meaning the errant access will generate a Translation Fault buffer management event. This will prevent the data corruption but will not prevent the loss of trace data.

2266875
A CFP instruction might execute with incorrect upper ASID or VMID bits

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The upper 8 bits of ASID or VMID might be incorrect for a CFP instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A CFP is executed with EL0 target execution context and {HCR_EL2.TGE, HCR_EL2.E2H} is {1,1} and TCR_EL2.AS=0.
2. A CFP is executed at EL2 or EL3 and the target execution context is EL0 or EL1 and VTCR_EL2.VS=0.

Implications

If either of the previous conditions are met, then the CFP instruction might not invalidate branch predictor resources associated with EL0 or EL1 contexts.

Workaround

This erratum can be avoided by setting CPUACTLR_EL1[22]=1. Setting CPUACTLR_EL1[22] will cause the CFP instruction to invalidate all branch predictor resources regardless of context.

2302506
Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0, and r1p1 Open.

Description

A Processing Element (PE) executing a PLDW or PRFM PST instruction that lies on a mispredicted branch path might cause a second PE executing a store exclusive to the same cache line address to fail continuously.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. One PE is executing store exclusive.
2. A second PE has branches that are consistently mispredicted.
3. The second PE instruction stream contains a PLDW or PRFM PST instruction on the mispredicted path that accesses the same cache line address as the store exclusive executed by the first PE.
4. PLDW/PRFM PST causes an invalidation of the first PE's caches and a loss of the exclusive monitor.

Implications

If the above conditions are met, the store exclusive instruction might continuously fail.

Workaround

Set CPUACTLR2_EL1[0] to 1 to force PLDW/PFRM ST to behave like PLD/PRFM LD and not cause invalidations to other PE caches. There might be a small performance degradation to this workaround for certain workloads that share data.

2313909
Denied power down request might prevent completion of future power down request

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

If a Processing Element (PE) initiates a power down request that is ultimately denied due to an external event, a future power down request might fail to complete.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE initiates a power down request (ON to OFF state transition) by setting CORE_PWRDN_EN and executing a WFI instruction.
2. PE completes the hardware flush of its caches.
3. An event, such as an external interrupt, causes an abort of the power down request.
4. PE returns to the ON state without performing a hardware reset.

Implications

If the above conditions are met, the PE might fail complete a subsequent power down request resulting in a deadlock.

Workaround

This erratum can be avoided by setting CPUACTLR2_EL1[36] to 1 before the power-down sequence that includes setting the CORE_PWRDN_EN bit, and executing a WFI. This bit should be cleared on exiting WFI by any mechanism other than reset.

2372204
Translation table walk folding into an L1 prefetch might cause data corruption

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

A translation table walk that matches an existing L1 prefetch with a read request outstanding on CHI might fold into the prefetch, which might lead to data corruption for a future instruction fetch.

Configurations Affected

This erratum affects all configurations

Conditions

1. In specific microarchitectural situations, the PE merges a translation table walk request with an older hardware or software prefetch L2 cache miss request.

Implications

If the previous conditions are met, an unrelated instruction fetch might observe incorrect data.

Workaround

Disable folding of demand requests into older prefetches with L2 miss requests outstanding by setting CPUACTLR2_EL1[40] to 1.

2390455
A continuous stream of incoming DVM syncs may cause TRBE to prevent the core from forward progressing

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

A continuous stream of incoming *Distributed Virtual Memory* (DVM) syncs might cause the *Trace Buffer Extension* (TRBE) to prevent the core from forward progressing, while executing a WFx.

Configurations Affected

This erratum affects all configurations.

Conditions

The erratum occurs if all the following conditions are met:

- The *Processing Element* (PE) executes a WFE or WFI instruction.
- TRBE is in use and needs to write trace data to its buffer.
- A continuous stream of DVM sync operations is received from other PEs.

Implications

When all of the above conditions are met, the PE might be prevented from entering WFE or WFI, and the pending WFE or WFI operation cannot be interrupted.

Workaround

There is no workaround.

2615812
Entry into the Full Retention power mode might cause corruption on Itag and BTB RAMs

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

If a core enters in Full Retention power mode, then the *Chip Enable* (CE) pin of Itag RAM or BTB RAM might be set. Physical RAMs don't support such states, so it leads to corruption when the core comes back to normal power mode and tries to reuse the RAM content.

Configurations Affected

This erratum affects all configurations.
This erratum affects implementations where RAM contents might be corrupted if the CE pin is asserted during retention.

Conditions

The erratum occurs if all the following conditions apply:

- The *Processing Element* (PE) enters the FULL_RET power state.
- The Itag or BTB RAMs are placed into a low-power mode during the PE FULL_RET power state.
- The PE power state transitions back to ON without going through the OFF power state.

Implications

If the conditions are met, the RAM contents of the itag and BTB RAMs might be corrupted. As a result, the PE might:

- Fetch and execute incorrect opcodes as a result of itag corruption.
- Predict incorrect targets from corrupted BTB RAMs.

Workaround

This erratum can be avoided by the firmware on power-on by disabling use of the Full Retention power mode in the core (setting IMP_CPUPWRCTLR_EL1.WFI_RET_CTRL to 0b000 and IMP_CPUPWRCTRL_EL1.WFE_RET_CTRL to 0b000).

2641945
L1 hardware prefetcher might cause deadlock

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

Clock gating logic in the L2 cache might cause internal interface signals to remain asserted, leading to unexpected operation of one of the L1 data cache hardware prefetchers.

Configurations Affected

This erratum affects all configurations

Conditions

Hardware prefetching is enabled.

Implications

If the previous condition is met, unexpected operation, including deadlock, might occur.

Workaround

Disable the affected L1 data cache prefetcher by setting CPUACTLR6_EL1[41] to 'b1. Doing so will incur a performance penalty of ~1%.

Contact Arm for an alternate workaround that impacts power.

2701951
The core might fetch stale instruction from memory when both Stage 1 Translation and Instruction Cache are Disabled with Stage 2 forced Write-Back

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

If a core is fetching instructions from memory while stage 1 translation is disabled and instruction cache is disabled, the core ignores Stage 2 forced Write-Back indication programmed by HCR_EL2.FWB and makes a Non-cacheable, Normal memory request. This may cause the core to fetch stale data from memory subsystem.

Configurations Affected

This erratum might affect system configurations that do not use Arm interconnect IP.

Conditions

The erratum occurs if all the following conditions apply:

- The *Processing Element* (PE) is using EL1 translation regime.
- Stage 2 translation is enabled (HCR_EL2.VM=1).
- Stage 1 translation is disabled (SCTLR_EL1.M=0).
- Instruction cache is enabled from EL2 (HCR_EL2.ID=0).
- Instruction cache is disabled from EL1 (SCTLR_EL1.I=0).

Implications

If the conditions are satisfied, the core makes all instruction fetch requests as Non-cacheable, Normal memory regardless of stage 2 translation output even if Stage 2 Forced Write-back is enabled. This might cause the core to fetch stale data from memory because Non-cacheable memory access does not probe any of cache hierarchy (e.g., Level-2 cache). If the bypassed cache hierarchy contains data modified by other initiators, stale data might be fetched from memory.

Workaround

For Hypervisor, initiating appropriate cache maintenance operations as if the core does not support stage 2 Forced Write-back feature. The cache maintenance operation should be initiated when new memory is allocated to a guest OS. This operation writeback the modified data in intermediate caches to point of coherency.

Category B (rare)

There are no errata in this category.

Category C

1880119
Noncompliance with prioritization of Exception Catch debug events

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, r1p1. Open.

Description

ARMv8.2 architecture requires that Debug state entry due to an Exception Catch debug event (generated on exception entry) occur before any asynchronous exception is taken at the first instruction in the exception handler. An asynchronous exception might be taken as a higher priority exception than Exception Catch and the Exception Catch might be missed altogether.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Debug Halting is allowed.
2. EDECCR bits are configured to catch exception entry to ELx.
3. A first exception is taken resulting in entry to ELx.
4. A second, asynchronous exception becomes visible at the same time as exception entry to ELx.
5. The second, asynchronous exception targets an Exception level ELy that is higher than ELx.

Implications

If the above conditions are met, the core might recognize the second exception and not enter Debug state as a result of Exception Catch on the first exception. When the handler for the second exception completes, software might return to execute the first exception handler, and assuming the core does not halt for any other reason, the first exception handler will be executed and entry to Debug state via Exception Catch will not occur.

Workaround

When setting Exception Catch on exceptions taken to an Exception level ELx, the debugger should do either or both of the following:

1. Ensure that Exception Catch is also set for exceptions taken to all higher Exception Levels, so that the second (asynchronous) exception generates an Exception Catch debug event.
2. Set Exception Catch for an Exception Return to ELx, so that when the second (asynchronous) exception handler completes, the exception return to ELx generates an Exception Catch debug event.

Additionally, when a debugger detects that the core has halted on an Exception Catch to an Exception level ELy, where y > x, it should check the ELR_ELy and SPSR_ELy values to determine whether the exception was taken on an ELx exception vector address, meaning an Exception Catch on entry to ELx has been missed.

2073992
Tag Check Fault might not be reported for some Vector Load instructions with SP as base register

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Memory access generated by some Vector Load instructions with Stack Pointer (SP) as base register are incorrectly treated as Tag Unchecked access instead of Tag Checked access.

Configurations Affected

This erratum affects all configurations where the **BROADCASTMTE** pin is HIGH.

Conditions

1. MTE is enabled
2. One of the following instruction with SP as base register generates a memory access to a page that is marked MTE tagged:
    - Post-indexed variants of SIMD LD1 (single or multiple structure)
    - Post-indexed variants of SIMD LD1R
    - Post-indexed variants of SIMD LD2 (single or multiple structure)
    - Post-indexed variants of SIMD LD2R
    - Post-indexed variants of SIMD LD3 (single or multiple structure)
    - Post-indexed variants of SIMD LD3R
    - Post-indexed variants of SIMD LD4 (single or multiple structure)
    - Post-indexed variants of SIMD LD4R

Implications

If the above conditions are met, the Processing Element (PE) might not report a Tag Check Fault as the memory access is incorrectly treated as Tag Unchecked access.

Workaround

There is no workaround for this erratum.

2108450
Speculative access to a recently unmapped physical address previously containing page tables might occur

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

If the memory containing page tables is unmapped or the cacheable attribute is changed while there are pending hardware prefetches to that table, the read requests might illegally occur after a `DSB` instruction.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under the following conditions:

- A table walk occurs.
- The hardware prefetcher generates a cacheable request to adjacent cache lines, allocating the L2 cache.
- The physical address containing the page tables is unmapped or the cacheable attribute is changed.

Implications

If the above conditions are met, an illegal read might occur in a short window of time after the `DSB` instruction. Arm believes this will not cause incorrect execution in any practical system.

Workaround

No workaround is required.

2113892
L2 tag single-bit ECC error might cause deadlock when using the SIP prefetcher

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

A single-bit ECC error in the L2 tag RAM that affects a SIP hardware prefetcher request might cause the PE to deadlock.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under the following conditions:

1. The L2 cache detects a single-bit ECC error in the L2 tag RAM.
2. The SIP hardware prefetcher issues a request to the L2 cache.

Implications

If the above conditions are met and in rare timing circumstances, the PE might encounter data corruption or a deadlock.

Workaround

In most situations, a workaround is not necessary due to the rarity of the required conditions.

To rule out this erratum as a cause for incorrect system behavior, the following workaround can be used: Force the L2 tag into inline ECC correction mode by setting CPUACTLR2_EL1[46] to 1. This setting incurs a small performance penalty due to an increase in L2 latency of one cycle.

2115480
L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When the PE receives a SnpPreferUnique or SnpPreferUniqueFwd snoop from the interconnect, it might not correctly count the L1 data cache and L2 cache invalidations that result.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE receives SnpPreferUnique or SnpPreferUniqueFwd from the coherent interconnect.
2. PE invalidates the L1 data cache and L2 cache.

Implications

If the above conditions are met, the L1D_CACHE_INVAL event will fail to increment and the L2D_CACHE_INVAL event might fail to increment. The relative infrequency of the necessary conditions means that the L1D_CACHE_INVAL and L2D_CACHE_INVAL events are still meaningful.

Workaround

There is no workaround.

2115856
Data abort on SVE first fault load might be routed to incorrect Exception level

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Under certain conditions, data abort on SVE first fault load might be routed to incorrect Exception level.

Configurations Affected

All configurations are affected.

Conditions

All of the following conditions must be met:

1. First active lane of SVE first fault load crosses a page boundary.
2. Translation table walk for the second page generates an external abort.
3. Memory tagging is enabled and access to bytes on the first page generates a tag check fail.
4. SCR_EL3.EA or HCR_EL2.TEA bits are set.

Implications

If the above conditions are met, data abort will not get routed to the correct Exception level. If this scenario occurred at EL0/EL1/EL2 and SCR_EL3.EA bit is set, data abort will not get routed to EL3. Likewise if this scenario occurred at EL0/EL1 and HCR_EL2.TEA bit is set and SCR_EL3.EA bit is not set, data abort will not get routed to EL2. The potential impact of this erratum to a practical system is considered to be very minor, given the precondition of an unrecoverable error.

Workaround

There is no workaround for this erratum.

2117121
MPAM value associated with instruction fetch might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, r1p1. Open.

Description

Under some scenarios, the MPAM value associated with an instruction fetch request might be incorrect when context changes.

Configurations Affected

This erratum affects all configurations.

Conditions

1. An Instruction fetch request is attempted before a context switch but is not completed until after a context switch.

Implications

The MPAM value associated with the instruction fetch request might be incorrect.

Workaround

There is no workaround.

2117589
Hardware prefetcher PMU events count incorrectly

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The following PMU events do not count correctly:

- 0x191, Number of cycles in which the hardware prefetcher is in the more aggressive mode.
- 0x192, Number of cycles in which the hardware prefetcher is in the less aggressive mode.
- 0x193, Number of cycles in which the hardware prefetcher is in the most conservative mode.

Configurations Affected

This erratum affects all configurations.

Conditions

One of the PMU event counters is configured to count any of the following events:

- 0x191
- 0x192
- 0x193

Implications

The counter values for these events will not be correct and therefore cannot be used.

Workaround

There is no workaround.

2119356
L2 data RAM or L2 TQ data RAM might fail to report ECC errors

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When the L2 cache is configured for specific ECC granule sizes, it might fail to report a detected single-bit ECC error in the L2 data RAM or L2 TQ data RAM.

Configurations Affected

This erratum affects all configurations.

Conditions

1. L2 cache detects a single-bit ECC error in the L2 data RAM or in the L2 TQ data RAM, in a protection granule that is already marked as poisoned due to a deferred error from another agent.

Implications

If the above condition is met, then the PE might fail to report the single-bit ECC error in the RAS error log registers. This might cause a small loss in diagnostic capability.

Workaround

There is no workaround.

2141643
A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Executing an A64 WFI or WFE instruction while in Debug state results in suspension of execution, and execution cannot be resumed by the normal WFI or WFE wake-up events while in Debug state.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The Processing Element (PE) is in Debug state and in AArch64 Execution state.
2. A WFI or WFE instruction is executed from EDITR.

Implications

If the above conditions are met, the PE will suspend execution.

This is not thought to be a serious erratum, because an attempt to execute a WFI or WFE instruction while in Debug state is not expected.

For WFI executed in Debug state, execution can only resume by any of the following:

- A Cold or Warm reset
- A Restart request trigger event from the Cross Trigger Interface (CTI) causing exit from Debug state, followed by a WFI wake-up event

For WFE executed in Debug state, execution can only resume by any of the following:

- A Cold or Warm reset
- A Restart request trigger event from the CTI causing exit from Debug state, followed by a WFE wake-up event
- An external event that sets the Event Register. Examples include executing an SEV instruction on another PE in the system or an event triggered by the Generic Timer.

Workaround

A workaround is unnecessary, because an attempt to execute a WFI or WFE instruction while in Debug state is not expected.

2142812
PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 does not count correctly, and MEM_ACC_CHECKED 0x4024 might not count correctly.

Configurations Affected

This erratum affects all configurations.

Conditions

1. One of the PMU event counters is configured to count event 0x4026 or 0x4024.
2. MTE is enabled.
3. SCTLR_ELx.ATA=1
4. A store instruction is executed that generates a memory-write access that is Tag Checked.

Implications

The counter values for these events will not be correct and therefore cannot be used reliably.

Workaround

There is no workaround.

2143137
Some SVE PMU events count incorrectly

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The following Performance Monitoring Unit (PMU) events do not count correctly:

- 0x8074, SVE_PRED_SPEC, SVE predicated operations speculatively executed
- 0x8075, SVE_PRED_EMPTY_SPEC, SVE predicated operations with no active predicates, operations speculatively executed
- 0x8076, SVE_PRED_FULL_SPEC, SVE predicated operations with all active predicates, operations speculatively executed
- 0x8077, SVE_PRED_PARTIAL_SPEC, SVE predicated operations with partially active predicates, operations speculatively executed

Configurations Affected

This erratum affects all configurations.

Conditions

One of the PMU event counters is configured to count any of the following events:

- 0x8074
- 0x8075
- 0x8076
- 0x8077

Implications

Load and store operations due to SVE instructions are not counted by any of these events. The counter values for these events will only reflect predicated SVE data processing operations. For example, this means that the ratios of each of the 0x8075-0x8077 event values to the 0x8074 event value will not be as expected because load and store operations are not included. However, the types of predicate used by data processing operations will still be usefully indicated.

Workaround

This erratum has no workaround.

2154264
FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

An SVE first fault contiguous load instruction that encounters a Tag Check fail when accessing the first active element and a watchpoint match on one of the non-first active elements can generate a Data abort exception with incorrect value in FAR_ELx.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging and watchpoints are enabled.
2. An SVE first fault contiguous load instruction accesses memory and generates a Data Abort exception due to Tag Check fail on the first active element.
3. There is a watchpoint match on one of the non-first active elements.

Implications

If the above conditions are met, a Data Abort exception will be generated with an incorrect value in FAR_ELx. ESR_ELx will indicate Synchronous Tag Check Fault. The FAR_ELx value could be anything between the start address of the access up to twice the access size.

Workaround

This erratum has no workaround.

2159151
Direct access of L2 data RAMs using RAMINDEX returns incomplete data

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

A direct access to the L2 data RAM using the RAMINDEX function returns incomplete data in the DDATA2 register.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under the following condition:

1. Direct access to internal memory targeting L2 data RAM is executed.

Implications

A direct access to the L2 data RAM will result in zeros on DDATA2_EL3[19:16]. These bits should contain ECC[15:12] corresponding to Data[127:64], but instead contain zeros.

Workaround

There is no workaround.

2165452
PMU_HOVFS event is not always exported when self-hosted trace is disabled

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

PMU_HOVFS is a PMU event that can be exported to the ETM. Exporting this event is disabled if TRFCR_EL2.E2TRE == 0b0, but this setting only applies when self-hosted trace is enabled. Due to this erratum, the event is never exported when TRFCR_EL2.E2TRE == 0b0, including when self-hosted trace is disabled.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The ETM is configured to use PMU_HOVFS as an external input event.
2. Self-hosted trace is disabled and TRFCR_EL2.E2TRE == 0b0.

Implications

Overflows of PMU counters reserved by EL2 might not be visible.

Workaround

To use the PMU_HOVFS as an external input event when self-hosted trace is disabled, ensure TRFCR_EL2.E2TRE is set to 1 (0b1).

2179550
An SError might not be reported for an atomic store that encounters data poison

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Under certain conditions, an atomic store that encounters data poison might not report an SError.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. An atomic store that is unaligned to its data size but within a 16-byte boundary accesses memory.
2. The atomic store accesses multiple L1 data banks such that not all banks have data poison.

Implications

If the above conditions are met, an SError might not be reported although poisoned data is consumed. Note that the data remains poisoned in the L1 and will be reported on the next access.

Workaround

This erratum has no workaround.

2189539
64 bit source SVE PMULLB/T not considered Cryptography instruction

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

64 bit source element variants of SVE PMULLB and PMULLT are incorrectly classified as non-cryptography instructions. When the **CRYPTODISABLE** pin is asserted, 64 bit source SVE PMULLB or SVE PMULLT instructions are executed rather than taking the expected undefined instruction exception. In addition to this, when the CRYPTODISABLE pin is deasserted, PMU counts for CRYPTO_SPEC (PMU event 0x77) do not include 64 bit source SVE PMULLB and PMULLT in their counts.

Configurations Affected

This erratum affects all configurations.

Conditions

Cryptodisable

1. **CRYPTODISABLE** pin is high.
2. 64 bit source SVE PMULLB or SVE PMULLT is executed.

PMU Counts

1. **CRYPTODISABLE** pin is low.
2. PMU Enabled to count PMU EVENT 0x77 (CRYPTO_SPEC).
3. 64 bit source SVE PMULLB or SVE PMULLT is executed.

Implications

If the above conditions are met, then the instructions will be executed instead of taking the undefined exception that is required by Arm architecture.
In addition, the PMU counter for the CRYPTO_SPEC event (PMU EVENT 0x77) will not increment for 64 bit source SVE PMULLB PMULLT instructions.

Workaround

There is no workaround.

2227172
Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Writes to contiguous bytes might be combined into one streaming write of 64 bytes. If such writes are performed to memory mapped Non-shareable and write-back, then two streaming writes to the same physical address might be performed in the wrong order.

Configurations Affected

This erratum affects all configurations.

Conditions

Write stream operations to memory mapped Non-shareable and write-back, or shareable can allocate the L2 cache without issuing a request on the CHI interface. This creates the possibility of two concurrent pending WriteNoSnpFull transactions of the same cache line on CHI, without the proper sequencing to guarantee the order they are performed.

Implications

If the above conditions are met, then the combined writes might be performed in the wrong order as determined by the sequential execution model.

Workaround

This erratum can be avoided by mapping all write-back memory as Inner or Outer Shareable.

2230110
Reads of DISR_EL1 incorrectly return 0s while in Debug State

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When the Processing Element (PE) is in Debug State, reads of DISR_EL1 from EL1 or EL2 with SCR_EL3.EA=0x1 will incorrectly return 0s.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The PE is executing in Debug State at EL1 or EL2, with SCR_EL3.EA=0x1.
2. The PE executes an MRS to DISR_EL1.

Implications

If the above conditions are met, then the read of DISR_EL1 will incorrectly return 0s.

Workaround

No workaround is expected to be required.

2231012
Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

Under certain circumstances, the SPE events E[17] "Partial predicate" and E[18] "Empty predicate" might not be captured as required.

Configurations Affected

This erratum affects all configurations.

Conditions:

1. SPE samples an SVE instruction with no vector operands.

Implications

If the above conditions are met, then the SPE events E[17] "Partial predicate" and E[18] "Empty predicate" might not be captured for the given instruction.

Workaround

There is no workaround.

2232775
Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Valid access to ICV_BPR1_EL1 from Secure EL1 when ICV_CTLR_EL1.CBPR is set to 1 should modify ICV_BPR0_EL1 on writes and return the value from ICV_BPR0_EL1 on reads. Instead, reads of ICV_BPR1_EL1 return ICV_BPR0_EL1 plus one, saturated to 0b111. Writes to ICV_BPR1_EL1 are ignored.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The PE is in Secure state in the EL1 exception level.
2. ICV_CTLR_EL1.CBPR is set to 1.
3. A valid read or write access to ICV_BPR1_EL1 occurs.

Implications

If the above conditions are met, then an incorrect value might be returned on read or a valid write might be ignored potentially, affecting the priority of interrupts in the CPU.

Workaround

This erratum has no workaround.

2233619
Lower priority exception might be reported when abort condition is detected at both stages of translation

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

When a permission fault or unsupported atomic fault is detected in the second stage of translation during stage 1 translation table walk, and there is a higher priority alignment fault due to SCTLR_EL1.C bit not being set, then Data Abort might be generated reflecting the lower priority fault.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs when all the following conditions apply:

1. The core executes an atomic, load/store exclusive, or load-acquire/store-release instruction.
2. SCTLR_EL1.C bit is not set and access is not aligned to size of data element.
3. A permission fault or unsupported atomic fault is detected in the second stage of translation during stage 1 translation table walk.

Implications

If the previous conditions are met, a Data Abort exception will be generated and incorrectly routed to EL2 with Data Fault Status Code (DFSC) of permission fault or unsupported atomic fault, when it should have been routed to EL1 with DFSC of alignment fault.

Workaround

This erratum has no workaround.

2236039
DRPS instruction is not treated as UNDEFINED at EL0 in Debug state

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

In Debug state, DRPS is not treated as an UNDEFINED instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The Processing Element (PE) is in Debug state.
2. PE is executing at EL0.
3. PE executes DRPS instruction.

Implications

If the above conditions are met, then the PE will incorrectly execute DRPS as NOP instead of treating it as an UNDEFINFED instruction.

Workaround

There is no workaround.

2237091
ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When an L1D tag double bit error is encountered, a Data Abort exception might be reported with an incorrect fault type of Synchronous Tag Check Fault in the ESR_ELx register under unusual micro architectural conditions.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging is enabled.
2. A precise checked access due to a load instruction encounters L1D tag double bit error.

Implications

If the previous conditions are met, a Data Abort exception will be generated with an incorrect Data Fault Status Code (DFSC) of Synchronous Tag Check Fault in the ESR_ELx register when it should have been Synchronous External Abort.
If this scenario occurred at EL0/EL1/EL2 and SCR_EL3.EA bit is set, then Data Abort will not get routed to EL3.
Likewise if this scenario occurred at EL0/EL1 and HCR_EL2.TEA bit is set, then Data Abort will not get routed to EL2. A fatal RAS error will still be reported.

Workaround

This erratum has no workaround.

2240293
TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Under certain conditions, Trace Buffer Extension (TRBE) might use incorrect Cacheability attributes for TRBE data when address translation is disabled.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. TRBE is enabled with TRBLIMITR_EL1.nVM == 1.
2. TRBMAR_EL1.Attr is programmed to use Cacheable attributes.
3. MDCR_EL2.E2TB = 2'b00 (EL2 owning)
4. HCR_EL2.CD=1 and HCR_EL2.VM=1
5. PE is executing at EL=1 or EL=0.
6. TRBE writes data to memory.

Implications

When the above conditions are met, PE might incorrectly use Non-Cacheable attribute instead of Cacheable attribute from TRBMAR_EL1.Attr[3:0] for TRBE data. Trace data might be lost if the memory location used by TRBE is present in cache when this write happens.

Workaround

This erratum has no workaround.

2240363
Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with vector operands in certain configurations

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

Under certain circumstances, SPE events E[17] "Partial predicate" and E[18] "Empty predicate" might not be captured as required.

Configurations Affected

This erratum affects configurations with VEC_2X128=0.

Conditions:

1. Vector unit in the core is configured with 4 VX pipes.
2. SPE samples an SVE instruction with vector operands.

Implications

If the above conditions are met, then SPE event E[17] "Partial predicate" and E[18] "Partial predicate" might not be reliably captured for the given instruction.

Workaround

There is no workaround.

2243142
L1 MTE Tag poison is not cleared

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

The MTE Tag poison is not cleared by an STG or DC G[Z]VA instruction.

Configurations Affected

This erratum affects all configurations with the **BROADCASTMTE** pin asserted.

Conditions

This erratum occurs under the following conditions:

1. A Processing Element (PE) accesses a line that encounters poison on the MTE Tag.
2. The PE executes an STG or DC G[Z]VA to the same 16-byte address.

Implications

If the above conditions are met, then the MTE Tag poison does not get cleared in the L1 Tag.

Workaround

There is no workaround.

2243856
ELR_ELx[63:48] might hold incorrect value when PE disables address translation

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r1p0.

Description

When the CPU executes an exception return in order to switch context and the new context satisfies certain rare conditions, the top 16 bits of ELR_ELx might track an incorrect value.

Configurations Affected

The erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. CPUACTLR_EL1[22] is set to 1.
2. The PE executes an ERET, ERETAA or ERETAB instruction to switch to a new context.
3. Either stage 1 or stage 2 translation was enabled when ERET is executed. After ERET, both stage 1 and stage 2 translations are turned off.
4. ELR_ELx[63:48] specified by ERET is neither 0x0000 (all zero) nor 0xffff (all one).

Implications

When the above conditions are met, the PE takes instruction abort (address size fault) or asynchronous exception after ERET without executing the instruction in the context specified by ERET. After the exception is taken, ELR_ELx specified by ERET should hold the same value because no instruction is executed. However, PE might modify ELR_ELx[63:48] to zero.

ERET with non-zero ELR_ELx[63:48] causes an address size fault during address translation disabled because the CPU supports less than 256TB physical address space. Arm also assumes the new context is controlled by privileged software (for example, Hypervisor) because translation is turned off. Therefore, software can hit this erratum only when the system software uses this malicious address in the ELR_ELx register.

Workaround

This erratum has no workaround.

2252367
L1 Data poison is not cleared by a store

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

The L1 Data poison is not cleared by a store under certain conditions.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. A Processing Element (PE) executes a store that does not write a full word to a location that has data marked as poison.
2. The PE executes another store that writes to all bytes that contain data poison before the previous store is globally observable.

Implications

If the above conditions are met, then the poison bit in the L1 Data cache does not get cleared.

Workaround

This erratum can be avoided by inserting a DMB before and after a word-aligned store that is intended to clear the poison bit.

2275209
SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The SPE, PMU events for full/partial/empty/not full predicate capture the cases where an instruction reads a full, not full, partial, or empty value for governing predicate according to the size of the instruction. Under certain circumstances, the event might be incorrectly captured.

Configurations Affected

This erratum affects all configurations.

Conditions

- PMU is configured to sample events for SVE_PRED_EMPTY_SPEC (0x8075), SVE_PRED_FULL_SPEC (0x8076), SVE_PRED_NOT_FULL_SPEC (0x8079), or SVE_PRED_PARTIAL_SPEC (0x8077).
- One of these SVE conversion instructions is executed: SCVTF, UCVTF, FCTVZU, FCVTZS, FCVT, FCVTX, FCVTXNT, or FCVTNT.
- Governing predicate used by instruction has a different value than All-Active or All-Empty.

or

- SPE samples one of these SVE conversion instructions: SCVTF, UCVTF, FCTVZU, FCVTZS, FCVT, FCVTX, FCVTXNT, or FCVTNT.
- Governing predicate used by instruction has a different value than All-Active or All-Empty.

Implications

If the previous conditions are met, the following events might be incorrectly captured:

- SPE event E[17] "Partial predicate"
- SPE event E[18] "Empty predicate"
- PMU event SVE_PRED_EMPTY_SPEC (0x8075)
- PMU event SVE_PRED_FULL_SPEC (0x8076)
- PMU event SVE_PRED_NOT_FULL_SPEC (0x8079)
- PMU event SVE_PRED_PARTIAL_SPEC (0x8077)

Workaround

This erratum has no workaround.

2277321
PMU L1D_CACHE_REFILL_OUTER is inaccurate

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

The L1D_CACHE_REFILL_OUTER PMU event 0x45 is inaccurate due to ignoring refills generated from a system cache. The L1D_CACHE_REFILL PMU event 0x3 should be the sum of PMU events L1D_CACHE_REFILL_INNER 0x44 and L1D_CACHE_REFILL_OUTER 0x45, however, due to the inaccuracy of L1D_CACHE_REFILL_OUTER 0x45 it is possible that this might not be the case.

Note: L1D_CACHE_REFILL PMU event 0x3 does accurately count all L1D cache refills, including refills from a system cache.

Configurations Affected

This erratum affects all configurations which implement a system cache.

Conditions

This erratum occurs under the following conditions:

1. The L2 inner cache is allocated with data transferred from a system cache.

Implications

When the previous condition is met, the L1D_CACHE_REFILL_OUTER PMU event 0x45 does not increment properly.

Workaround

The correct value of L1D_CACHE_REFILL_OUTER PMU event 0x45 can be calculated by subtracting the value of L1D_CACHE_REFILL_INNER PMU event 0x44 from L1D_CACHE_REFILL PMU event 0x3.

2299191
L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

A double-bit ECC error in a cache line containing Memory Tagging Extensions (MTE) tags might result in the L1 and L2 caches becoming out-of-sync with respect to MTE tag validity. This can lead to a situation in which the L1 evicts dirty MTE tags to the L2 as part of a fill/evict sequence or a snoop. If this eviction satisfies an external forwarding snoop, the RN-F might fail to provide legal responses which might lead to a deadlock.

Configurations Affected

This erratum affects all configurations using the Memory Tagging Extensions.

Conditions

When using MTE, under specific microarchitectural and timing conditions, an L2 double-bit ECC error in the L2 tag RAMs might allow the L1 data cache to later evict a cache line with dirty MTE tags.
The erratum occurs if the eviction satisfies an external snoop of one of these types:

- SnpUniqueFwd
- SnpCleanFwd
- SnpSharedFwd
- SnpNotSharedDirtyFwd
- SnpPreferUniqueFwd

Implications

If the previous conditions are met, the PE might provide an SnpRespDataFwded response to the HN-F, but fail to provide a CompData response to the original requester, leading to a system deadlock.

Workaround

This erratum has no workaround.

2302585
CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

In some contexts when CSSELR_EL1.InD == 0x1, CSSELR_EL1.TnD is defined to be RES0.
In other contexts when CSSELR_EL1.InD == 0x0, CSSELR_EL1.TnD is defined to be R/W.
When a bit is RES0 in some contexts and R/W in other contexts, then it cannot be implemented as RAZ/WI for RES0 contexts.
In affected products, CSSELR_EL1.TnD is incorrectly treated as RAZ/WI instead of the correct R/W behavior when CSSELR_EL1.InD == 0x1.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The PE is executing with CSSELR_EL1.InD == 0x1.
2. The PE attempts to read or write CSSELR_EL1.TnD.

Implications

Reads of CSSELR_EL1.TnD will return 0x0 and writes will be ignored.

Workaround

This erratum is not expected to require a workaround.

2307825
ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

When a data double bit error or external abort is encountered during a translation table walk, a synchronous exception is reported with the ISV bit set in the ESR_ELx register.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following condition:

1. A data double bit error or external abort is encountered during a translation table walk, and a synchronous exception is reported.

Implications

If the previous condition is met, the ESR_ELx.ISV bit will be set. The ESR[23:14] bits are set with the correct syndrome for the instruction making the access. That is SAS, SSE, SRT, SF, and AR are all set according to the instruction.

Workaround

This erratum has no workaround.

2312833
ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

When a data double bit error or external abort is encountered on one half of an unaligned load, a Data Abort exception might be reported with an incorrect fault type of Synchronous Tag Check Fault in the ESR_ELx register. This occurs under unusual micro-architectural conditions.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging is enabled.
2. A precise checked access due to an unaligned load instruction encounters a data double bit error or external abort.

Implications

If the previous conditions are met, a Data Abort exception will be generated with an incorrect Data Fault Status Code (DFSC) of Synchronous Tag Check Fault in the ESR_ELx register, when it should have been Synchronous External Abort.

If this scenario occurred at EL0/EL1/EL2, and the SCR_EL3.EA bit is set, then the Data Abort will not get routed to EL3.

Likewise, if this scenario occurred at EL0/EL1, and the HCR_EL2.TEA bit is set, then the Data Abort will not get routed to EL2. A RAS error will still be reported.

Workaround

This erratum has no workaround.

2343688
STALL_BACKEND_MEM, Memory stall cycles AMU event count incorrectly

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The following *Activity Monitor Unit* (AMU) event does not count correctly:

- 0x4005, STALL_BACKEND_MEM. The counter counts cycles in which the PE is unable to dispatch instructions from the frontend to the backend of the PE. It is due to a backend stall caused by a miss in the last level of cache within the PE clock domain. This event is counted by AMEVCNTR03.

Configurations Affected

This erratum affects all configurations.

Conditions

- AMU is enabled

Implications

The counter values for the event will not be correct and therefore cannot be used reliably.

Workaround

This erratum has no workaround.

2351560
ERXPFGCDN_EL1 register is incorrectly written on Warm reset

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The ERXPFGCDN_EL1 register is written a reset value of 0 at both cold and Warm reset, when it should only be reset at Cold reset.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs when a Warm reset occurs.

Implications

If the previous condition is met, the value of ERXPFGCDN_EL1 will not be preserved across a Warm reset.

Workaround

This erratum has no workaround.

2359164
Incorrect read value for Performance Monitors Configuration Register

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0. Fixed in r1p1.

Description

The Performance Monitors Configuration Register (PMCFGR) returns an incorrect read value for the CCD field.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Debugger reads the PMCFGR register.

Implications

The PMCFGR.CCD field incorrectly reports the value 0x1 indicating that Cycle counter has prescale, instead of the expected value of 0x0, since the field is RAZ if AArch32 isn't supported.

Workaround

There is no workaround.

2390828 PMU MEM_ACCESS_CHECKED_RD and MEM_ACCESS_CHECKED_WR inaccurate

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The MEM_ACCESS_CHECKED_RD and MEM_ACCESS_CHECKED_WR PMU events increment incorrectly when accessing a tagged page, but is inactive due to SVE predication.

Configurations Affected

This erratum affects configurations with BROADCASTMTE=1.

Conditions

This erratum occurs if the following conditions apply:

1. a load or store access crosses a page-boundary
2. one unaligned half accesses a page that is MTE tagged, but is inactive due to SVE predication
3. the other unaligned half accesses a page that is not MTE tagged

Implications

If the previous conditions are met, the PMU event might increment inaccurately.

Workaround

This erratum has no workaround.

2391679
Software-step not done after exit from Debug state with an illegal value in DSPSR

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open

Description

On exit from Debug state, PSTATE.SS is set according to DSPSR.SS and DSPSR.M.
If DSPSR.M encodes an illegal value, then PSTATE.SS should be set according to the current Exception level. When the erratum occurs, the PE always writes PSTATE.SS to 0.

Configurations Affected

This erratum affects all configurations.

Conditions

- Software-step is enabled in current Exception level
- DSPSR.M encodes an illegal value, like:
  - M[4] set
  - M is a higher Exception level than current Exception level
  - M targets EL2 or EL1, when they are not available
- DSPSR.D is not set
- DSPSR.SS is set

Implications

If the previous conditions are met, then, on exit from Debug state the PE will directly take a Software-step Exception, without stepping an instruction as expected from DSPSR.SS=1.

Workaround

This erratum has no workaround.

2409463
Incorrect read value for Performance Monitors Control Register

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The Performance Monitors Control Register (PMCR_EL0) and the External Performance Monitor Control Register (PMCR) might return an incorrect read value for the X field.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Software writes a nonzero value to the PMCR_EL0.X, or debugger writes a nonzero value to the PMCR.X
2. Software reads the PMCR_EL0 register, or debugger reads the PMCR register

Implications

The PMCR_EL1.X or PMCR.X field incorrectly reports the value 0x1, indicating exporting of events in an IMPLEMENTATION DEFINED PMU event export bus is enabled. The expected value is 0x0, as the implementation does not include a PMU event export bus.

Workaround

This erratum has no workaround.

2409683
Incorrect sampling of SPE events "tlb_access" for an unaligned SVE load instruction with no active elements

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

Under certain circumstances, the SPE events E[4] "TLB Access" might not be captured as required.

Configurations Affected

This erratum affects all configurations.

Conditions

SPE samples an unaligned SVE load instruction with no active elements.

Implications

If the previous conditions are met, then the SPE events E[4] "TLB Access" might not be consistent with the PMU event 0x0025 (L1D_TLB). Note that PMU event 0x0025 (L1D_TLB) is accurate.

Workaround

This erratum has no workaround.

2441604
PMU STALL_SLOT_BACKEND and STALL_SLOT_FRONTEND events count incorrectly

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, and r1p0. Fixed in r1p1.

Description

The following Performance Monitoring Unit (PMU) events do not count correctly:

- 0x3D, STALL_SLOT_BACKEND, no operation sent for execution on a slot due to the backend
- 0x3E, STALL_SLOT_FRONTEND, no operation sent for execution on a slot due to the frontend

Configurations Affected

This erratum affects all configurations.

Conditions

One of the PMU event counters is configured to count any of the following events:

- 0x3D, STALL_SLOT_BACKEND
- 0x3E, STALL_SLOT_FRONTEND

Implications

When operations are stalled in the processing element's dispatch pipeline slot, some of those slot stalls are counted as frontend stalls when they should have been counted as backend stalls, rendering PMU events 0x3D (STALL_SLOT_BACKEND) and 0x3E (STALL_SLOT_FRONTEND) inaccurate. The PMU event 0x3F (STALL_SLOT) does still accurately reflect its intended count of "No operation sent for execution on a slot".

Workaround

This erratum has no workaround.

2612736
Read to dump the instruction cache contents while in Debug state results in deadlock

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

In Debug state, an access to read the instruction cache data contents using SYS_IMP_RAMINDEX will not complete and will deadlock any ITR transactions that follow.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs if all the following conditions apply:

1. The PE enters Debug state.
2. User sets SYS_IMP_RAMINDEX RAM_ID field to 0x1 in order to select the read of instruction cache contents, and performs the read.

Implications

The instruction cache read deadlocks, and the debugger might lose control.

Workaround

This erratum can be avoided by the debugger if the instruction cache is not read when the core is in Debug state.

2652014
FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

A *Scalable Vector Extension* (SVE) first fault contiguous load instruction that encounters a Tag Check fail when accessing the first active element and a watchpoint match on one of the non-first active elements can generate a Data abort exception with incorrect value in FAR_ELx.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging and watchpoints are enabled.
2. An SVE first fault contiguous load instruction accesses memory and generates a Data Abort exception due to Tag Check fail on the first active element.
3. There is a watchpoint match on one of the non-first active elements.

Implications

If the above conditions are met, a Data Abort exception will be generated with an incorrect value in FAR_ELx. ESR_ELx will indicate Synchronous Tag Check Fault.

Workaround

This erratum has no workaround.

2676363
Execution of STG instructions in close proximity might cause loss of MTE allocation tag data

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

Under certain rare micro-architectural conditions, two or more STG instructions that access the same cacheline but different 32-bytes might not write the *Memory Tagging Extension* (MTE) allocation tag to memory in the presence of an ECC error to the same cache index.

Configurations Affected

This erratum affects all configurations where the BROADCASTMTE pin is HIGH.

Conditions

1. Memory tagging is enabled.
2. Two or more STG instructions are executed in close proximity to the same cache line.
3. The STG instructions access different 32-bytes locations.
4. An L2 fill for a different cacheline but to the same index has a single bit data error that could have otherwise caused a capacity evict of the cacheline accessed by the STG instructions

Implications

If the above conditions are met, then under specific micro-architectural conditions, the MTE allocation tag might not be written to memory, resulting in a silent corruption of the MTE tag.

Workaround

If desired, this erratum can be avoided by setting CPUACTLR5_EL1[13] to 1.

Note: setting CPUACTLR5_EL1[13] to 1 is expected to result in a small performance degradation for workloads that use MTE (approximately 1.6% when using MTE imprecise mode, 0.9% for MTE precise mode).

2693826
MTE tag check fail seen on first half of a cache-line crossing load does not get reported

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

Under some unusual microarchitectural conditions, tag check fail seen on first half of a cache-line crossing load does not get reported.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging is enabled
2. Cache-line crossing load is executed that fails tag check on first half of the access
3. Unusual microarchitectural conditions occur

Implications

If the above conditions are met, precise checked loads that see tag mismatch will not report an exception and imprecise checked loads will not update the TFSR register.

Workaround

This erratum has no workaround.

2693832
MTE checked load might read an old value of allocation tag by not complying with address dependency ordering

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

Under some unusual micro-architectural conditions, checked load might read an old value of allocation tag by not complying with address dependency ordering.

Configurations Affected

All configurations are affected.

Conditions

The erratum occurs when all the following apply:

1. Initially, memory location M has allocation tag A.
2. *Processing Element* x (PEx) stores to M using allocation tag A.
3. PEy changes the allocation tag of M from A to B.
4. PEx makes a checked load from M using allocation tag A, with a dependency such that it should observe allocation tag B.

Implications

If the above conditions are met, PEx may not observe the new allocation tag for the memory location and may fail to report a tag check fail.

Workaround

This erratum has no workaround.

2704518
Incorrect value reported for SPE PMU event SAMPLE_FEED

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1, Open.

Description

Under certain conditions when a CMP instruction is followed by a Branch, the SAMPLE_FEED PMU event 0x4001 is not reported.

Configurations Affected

This erratum affects all configurations.

Conditions

1. *Statistical Profiling Extension* (SPE) sampling is enabled.
2. SPE samples a CMP instruction, which is followed immediately by a BR instruction.

Implications

If the above conditions are met, then the SAMPLE_FEED event may not be incremented.

For most expected use cases, the inaccuracy is not expected to be significant.

Workaround

There is no workaround.

2712633
Incorrect read value for Performance Monitors Configuration Register EX field

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0, r1p0, and r1p1. Open.

Description

The Performance Monitors Configuration Register (PMCFGR) might return an incorrect read value for the EX field.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs when the software reads the PMCFGR register.

Implications

The PMCFGR.EX field incorrectly reports the value 0x1, indicating exporting of events in an IMPLEMENTATION DEFINED PMU event export bus is enabled. The expected value is 0x0, as the implementation does not include a PMU event export bus.

Workaround

This erratum has no workaround.