SoC Designer™ Plus

Version 8.5

Fast Models System Creator
Cycle Models Reference

ARM DUI 0985F

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Release Information

The following changes have been made to this document:

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Product Status

The information in this document is final, that is for a developed product.

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Contents

1 Introduction

This is the Cycle Model reference for the SoC Designer™ Plus Fast Models System Creator. Supported Cycle Models are listed, along with restrictions on their use and other notes. If a Cycle Model is listed as supporting:

- **Fast Models but not Swap & Play™** — You can include the Cycle Model in a Fast Models component, but the Fast Models system cannot be used with Swap & Play.

- **Save/Restore but not Swap & Play** — You can use the Cycle Model in a Fast Models system with Swap & Play, provided the Cycle Model is not included in the Fast Models component; i.e. it remains a cycle-accurate model.

For more information on using Fast Models with SoC Designer Plus, refer to the *Fast Models System Creator User Guide*.

2 Supported Cycle Models from ARM IP Exchange

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AMBA® Network Interconnect (NIC-301)	√	√	√	The Remapping features is not supported for Fast Models and Swap & Play.
BP147 PrimeCell® Infrastructure AMBA 3 TrustZone™ Protection Controller		√		The ID registers are not present in the Fast Model.
CoreLink™ ADB-400 AMBA® Domain Bridge		√	√	
CoreLink CCI-400 Cache Coherent Interconnect (PL420)				
CoreLink CCI-500 Cache Coherent Interconnect (PL422)				
CoreLink CCI-550 Cache Coherent Interconnect (PL423)				
CoreLink CCN-502 Cache Coherent Network (PL502)	√	√	√	
CoreLink CCN-504 Cache Coherent Network (PL510)	√	√	√	

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
CoreLink DMC-400 Dynamic Memory Controller	√	√	√	
CoreLink GIC-400 Generic Interrupt Controller	√	√	√	
CoreLink GIC-500 Generic Interrupt Controller (PL600)				
CoreLink MMU-400 System Memory Management Unit (PL470)	√			
CoreLink NIC-400 Network Interconnect	√	√	√	The Remapping features is not supported for Fast Models and Swap & Play.
Cortex®-A32 Processor				
Cortex-A35 Processor				
Cortex-A53 Processor	√	√	√	
Cortex-A57 Processor	√	√	√	
Cortex-A7 MPCore Processor	√	√	√	
Cortex-A9 MPCore Processor	√	√	√	
Cortex-A9 Processor		√	√	
Cortex-A15 MPCore Processor	√	√	√	
Cortex-A72 Processor	√	√	√	
Cortex-A73 Processor				
Cortex-M3 Processor		√		
Cortex-M4 Processor		√		
Cortex-M7 Processor				
Cortex-R4 Processor		√		
Cortex-R5 Processor				

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
Cortex-R7 Processor	√	√	√	Refer to the *Cortex-R7 Cycle Model User Guide*, Section 1.1.4 for restrictions and workarounds.
Cortex-R8 Processor	√	√	√	
L220 Cache Controller		√		Registers are memory mapped into the address space of the main transaction slave port. The peripheral port can not be used to access memory mapped registers.
PL011 PrimeCell® UART	√	√	√	File I/O is not supported. A socket connection to a telnet session is used for all I/O.
PL022 PrimeCell Synchronous Serial Port (SSP)		√		Supported as a slave device only. DMA is not implemented.
PL061 PrimeCell General Purpose Input/Output (GPIO)		√		
PL080 PrimeCell DMA Controller		√		
PL190 PrimeCell Vectored Interrupt Controller	√			
PL192 PrimeCell Vectored Interrupt Controller		√		
PL301 PrimeCell High-Performance Matrix (HPM)		√	√	Memory maps and remap are not supported. Programming via the AXI or APB port is not supported. Registers are not implemented.

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
PL310 Cache Controller		√	√	Internal interrupt state (and its corresponding registers) is not restored with Swap & Play. The PL310 can be directly connected only to a Cortex-A9. Connecting to other types of cores (such as the Cortex-R8) requires custom components.
PrimeCell CCI-400 Interconnect (PL420)	√	√	√	

3 Supported Cycle Models for AMBA Miscellaneous Bridges

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AHB to AHB Asynchronous Bridge CM_Bridge_Ahb_Ahb_Async_32 CM_Bridge_Ahb_Ahb_Async_64	√	√	√	
AHB-Lite to AHB Bridge CM_Bridge_AhbLite_Ahb_SS_32 CM_Bridge_AhbLite_Ahb_SS_64 CM_Bridge_AhbLite_AhbLite_SS_32 CM_Bridge_AhbLite_AhbLite_SS_64	√	√	√	

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AHB-Lite to AXI Bridge CM_Bridge_AhbLite_Axi_SS_32 CM_Bridge_AhbLite_Axi_SS_64 CM_Bridge_AhbLite_Axi_SS_128 CM_Bridge_AhbLite_Axi_MS_32 CM_Bridge_AhbLite_Axi_MS_64 CM_Bridge_AhbLite_Axi_MS_128	√	√	√	
AHB-Lite to AHB Synchronous Bridge CM_Bridge_AhbLite_Ahb_Sync_SS_32 CM_Bridge_AhbLite_Ahb_Sync_SS_64 CM_Bridge_AhbLite_AhbLite_Sync_SS_32 CM_Bridge_AhbLite_AhbLite_Sync_SS_64	√	√	√	FM Support for the slave-side interface
AXI to AHB-Lite Bridge CM_Bridge_Axi_AhbLite_SS_32 CM_Bridge_Axi_AhbLite_SS_64 CM_Bridge_Axi_AhbLite_SS_128 CM_Bridge_Axi_AhbLite_MS_32 CM_Bridge_Axi_AhbLite_MS_64 CM_Bridge_Axi_AhbLite_MS_128	√	√	√	
AXI to APB Bridge CM_Bridge_Axi_Apb	√	√	√	

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AXI to AXI Asynchronous Bridge CM_Bridge_Axi_Axi_ASync_32 CM_Bridge_Axi_Axi_ASync_64 CM_Bridge_Axi_Axi_ASync_128	√	√	√	
AXI to AXI Synchronous Bridge CM_Bridge_Axi_Axi_Sync_32 CM_Bridge_Axi_Axi_Sync_64 CM_Bridge_Axi_Axi_Sync_128	√	√	√	
AXI Register Slice CM_Regslice_Axi_Axi_Forward_32 CM_Regslice_Axi_Axi_Forward_64 CM_Regslice_Axi_Axi_Forward_128 CM_Regslice_Axi_Axi_Reverse_32 CM_Regslice_Axi_Axi_Reverse_64 CM_Regslice_Axi_Axi_Reverse_128	√	√	√	
AHB Resizer CM_Resize_Ahb_SS_64_32	√	√	√	

Cycle Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AXI Resizer CM_Resize_Axi_32_64 CM_Resize_Axi_32_128 CM_Resize_Axi_64_128 CM_Resize_Axi_128_64 CM_Resize_Axi_128_32 CM_Resize_Axi_64_32	√	√	√	
APB System Controller CM_Sysctrl_Apb	√	√	√	
APB Timer CM_Timer_APB	√	√	√	
PIF/AMBA Bridge CM_Pif_Axi family CM_Axi_Pif family CM_Pif_Ahblite family CM_Ahblite_Pif family	√	√	√	

4 Supported Cycle Models from the SoC Designer Plus Protocol Bundle

Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
Aggregator/Deaggregator Components	√	√	√	When connecting an Aggregator/Deaggregator component in a Fast Models system to a component in a Cycle Accurate system (crossing the FM/CA boundary), single bit wires must be used. For more information about blending Cycle Accurate models and Fast Models, refer to the *Fast Models System Creator User Guide*.
AHBv2LiteToAHBv2SS	√	√	√	
AHBv2_LiteMem AHBv2_LiteMem[1-8]	√			
AHBv2_Mem AHBv2_Mem[1-8]	√	√		
AHBv2Mux_Lite		√		
AHBv2ToAHBv2LiteMS		√		
AHBv2ToAHBv2LiteSS	√	√		
AHBv2ToAPB		√		
APBMerger	√	√	√	
AXI4_Mem	√	√	√	
AXI4_Stub	√			The MxScript file loaded into the stub is not saved or restored. When opening a system in preparation for loading a checkpoint file, you must specify the MxScript file in the “Select Application Files” dialog.
AXI4ToAXIv2	√	√	√	
AXI4ToAXI4	√	√	√	

Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
AXIv2_Mem	√	√	√	
AXIv2_Slave	√	√	√	
AXIv2_Stub	√	√	√	The MxScript file loaded into the stub is not saved or restored. When opening a system in preparation for loading a checkpoint file, you must specify the MxScript file in the “Select Application Files” dialog.
AXIv2ToAXI4	√	√	√	
CarbonSemihost CarbonSemihost2		√	√	Semihosting is handled internally by Fast Models processors, so no external component is needed. You can include the CarbonSemihost components in the Fast Models to simplify the resulting system. Parameters from the CarbonSemihost instances are ignored. For Swap & Play, only the default file handles (stdin, stdout, stderr) are restored. No other files can be open.
CarbonMemoryMapped CounterModule	√	√	√	
CDIV		√	√	
CHIToAXI4		√	√	
CHI_to_CHI*	√	√	√	
intVector	√	√	√	
MxAHBv2		√		
MxAHBv2_Lite		√		
MxAXI4	√	√	√	

Model	Save/Restore Support	Fast Models Support	Swap & Play Support	Notes
MxAXIv2	√	√	√	
MxMem1 MxMem2 MxMem3 MxMem4		√	√	
MxSigDriver	√			