# Release notes for System Registers for Arm A-profile Architecture

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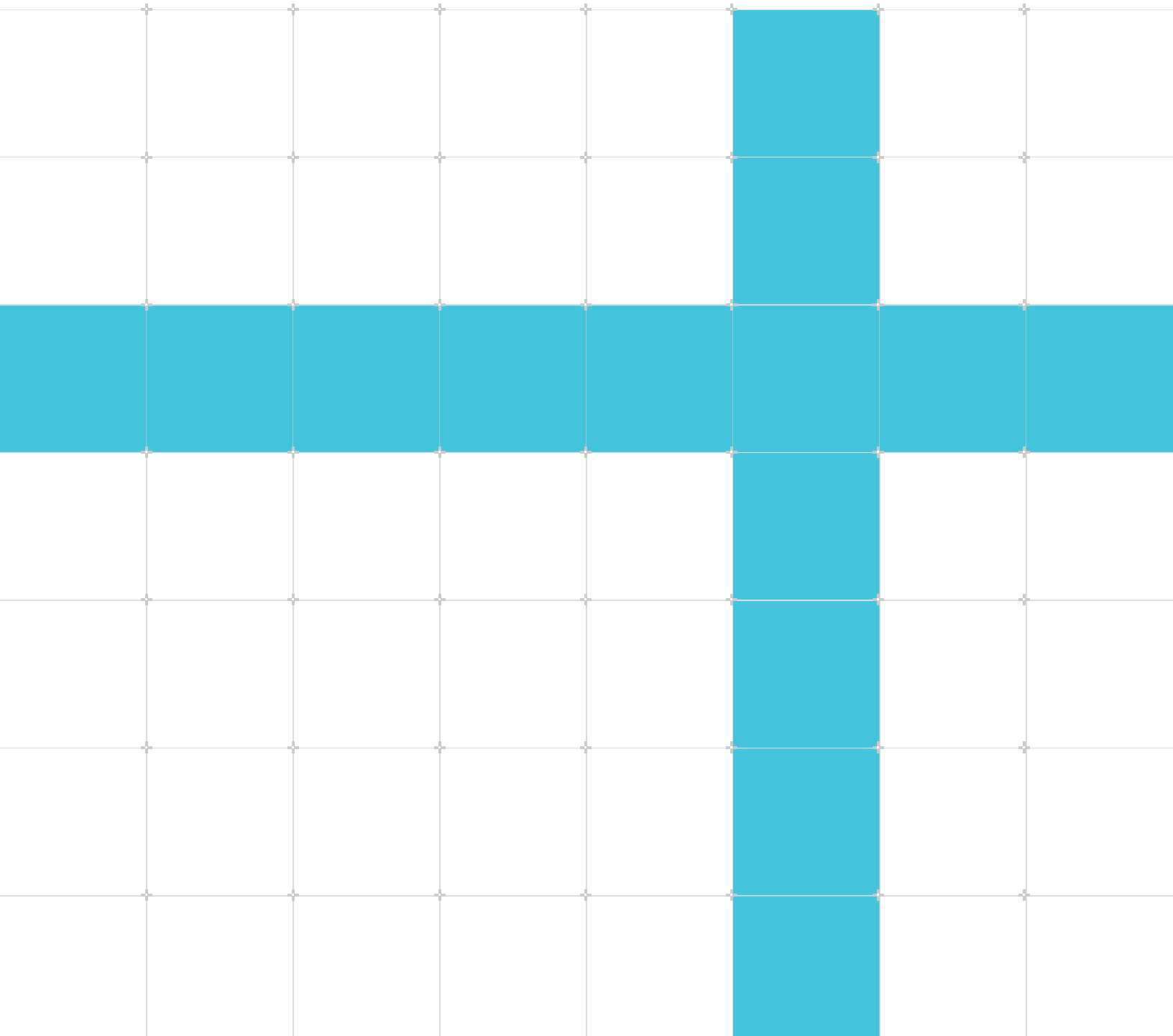

# Release notes for System Registers for Arm A-profile Architecture



## Release information

### Document history

| Issue | Date | Confidentiality | Change |
|---|---|---|---|
| 2023_09-01 | 29 September 2023 | Non-Confidential | 2023-09 release |

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Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

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# Contents

# 1. Release notes for System Registers for Arm A-profile Architecture (2023-09)

29 September 2023

## Product Status

The information in this release covers multiple versions of the architecture. The content relating to different versions is given different quality ratings.

The information relating to the 2023 Extensions of the A-profile Architecture and FEAT_D128 of the 2022 Extensions is at Alpha quality. Alpha quality means that most major features of the specification are described in this release, but some features and details might be missing.

The information relating to the remainder of the 2022 Extensions of the A-profile Architecture and the rest of the Architecture is at Beta quality. Beta quality means that all major features of the specification are described, but some details might be missing.

## Change history

This release contains the following changes:

- This release introduces the 2023 Extensions of the A-profile Architecture.
- References to the value of HCR_EL2.{NV2, NV1, NV} are updated to refer to the Effective value of HCR_EL2.{NV2, NV1, NV}.
- References to the value of HCR_EL2.{E2H, TGE} are updated to refer to the Effective value of HCR_EL2.{E2H, TGE}.
- EDDFR.ExtTrcBuf is clarified to state that non-zero values require EDDFR.TraceBuffer to be defined and match ID_AA64DFR0_EL1.
- TLBI accessibility pseudocode is updated to correctly handle reserved Security states.
- The TRCAUTHSTATUS.SNID and TRCAUTHSTATUS.NSNID descriptions are extended to describe implementations when FEAT_RME does not implement Secure state.
- The meaning of field value `0b0010` in ID_AA64MMFR2_EL1.VARange is clarified.
- Added access conditions for registers in the CNTBaseN, CNTEL0BaseN, or CNTCTLBase frames, when FEAT_RME is implemented.
- The description of HCR_EL2.ATA is corrected to reflect new effective value and register behavior.
- TLBI RPALOS and TLBI RPAOS fields are updated to include FEAT_D128 Address extension.
- The reset behaviour of MECIDR_EL2.MECIDWidthm1 is corrected.
- PAR_EL1 fields when D128 is implemented are clarified.
- Bits in TCR_EL2 and TCR2_EL2 are corrected to describe permitted caching in a TLB.
- PMBSR_EL1.TopLevel and TRBSR_EL1.TopLevel fields are added to the registers.
- The EDPRSR.SPD field is corrected to remove the incorrect Core power domain statement.

- HDFGxTR2_EL1.nSPMEV* fields are corrected to show that if event counter n is not implemented, reads of SPMEV* registers are not undefined.
- The register format of ERR<n>STATUS when RAS System Architecture v2 is implemented is corrected to be conditional on ERR<n>FR instead of ERR<q>FR.
- The field description of ICV_CTLR_EL1.PRIbits is clarified to refer to virtual priority bits.
- Reserved, **RES0** fields in EDPFR are relaxed to be Reserved, **UNKNOWN**.
- Accessibility pseudocode in PMEVCNTSVR<n>_EL1 is updated with behaviors when unimplemented counters are accessed.
- ISR and ISR_EL1 descriptions are updated to account for RME.
- CNTKCTL_EL1 accessibility pseudocode is updated so as not to be required to update fields specific to CNTKCTL_EL2.
- DISR_EL1 is updated to include fields WU, WnRV and WnR.
- PMCR_EL0.DP described behavior when FEAT_SPE_DPFZS is not implemented is corrected.
- The SPMACCESSR_ELx registers are updated to ignore SPMACCESSR_EL1 when executing at EL2 with HCR_EL2.E2H set to 1.
- PFAR_EL1 and PFAR EL2 accessibility pseudocode is updated to include the SCR_EL3.PFAREn trap.
- The accessibility pseudocode of DISR_EL1 and DISR is updated to account for the modified behavior of HCR_EL2.VSE, which allows a hypervisor to inject a virtual SError exception into a guest under different conditions.
- Clarification of behavior of PMSELR_EL0.SEL when the value indicates an unimplemented counter.
- ERR<n>FR field descriptions are updated to remove a compatibility break between RAS System Architecture v1.1 and RAS System Architecture v2. The field descriptions of RCWMASK_EL1.Mask and RCWSMASK_EL1.Software_Mask are clarified to state the impact of FEAT_MEC.
- The accessibility pseudocode for PMZR_EL0 is clarified by using the new ZeroPMUCounters(X[t,64]) function. New pseudocode function ZeroPMUCounters() defined to represent the action of write to PMZR_EL0 register. New functions {{GetPMUWriteMask()}} and {{GetPMUReadMask()}} are introduced, to return a mask of the PMU counters that are writable or readable at the current Exception level.
- The RNDR and RNDRRS register definitions are relaxed to remove the implicit coupling of RNDR to RNDRRS.
- In ICC_CTLR, ICC_DIR, ICC_PMR, ICC_RPR, ICV_CTLR, ICV_DIR, ICC_PMR, and ICC_RPR, the accessibility pseudocode is updated to include the ICC_SRE.SRE trap.
- ID_AA64ZFR0_EL1.B16B16 and ID_AA64SMR0_EL1.{B16B16,F16F16} are updated such that the features identified by these fields are dependent on FEAT_SVE2 and FEAT_SME2 instead of FEAT_SVE2p1 and FEAT_SME2p1.
- External registers EDDFR, EDPFR and EDWAR are updated from two 32-bit registers to a single 64-bit register.
- PMU.PMCGCR0 is updated to 64-bit wide when FEAT_PMUv3_EXT64 is implemented.

- SPSR_EL3 corrected to refer to SPSR_EL1.
- EC values are added to field conditions in PMBSR_EL1 and TRBSR_EL1.
- The condition for unsupported architected activity monitor events in AMEVCNTVOFF0_EL2 accessibility is clarified.
- The description of AMDEVARCH.ARCHID is updated to include the value for the 64-bit AMU external interface.
- The accessibility pseudocode for CNTPS_TVAL_EL1 is corrected.
- In ESR_EL1, ESR_EL2, and ESR_EL3, the effect of FEAT_FPACCOMBINE on the reporting of a PAC Fail exception is corrected.
- The descriptions of MPIDR_EL1.MT and MPIDR.MT are updated to clarify that these fields do not mean multithreading is implemented.
- Clarified the descriptions in CNTHCTL_EL2 to remove redundant conditions on HCR_EL2.E2H.
- Accessibility conditions on EDSCR.SDD == 1 have been updated to use functions EL3SDDUndef() and EL3SDDUndefPriority().
- PMCR_EL0.DP is updated to indicate the behavior when FEAT_PMUv3p9 is or is not implemented.
- The relaxations for generating and reporting watchpoints, introduced by FEAT_SME, will be retrospectively permitted for SVE from Armv8.2-A.

## Known issues

All issues identified in the below list will be fixed in a future release.

- The behavior of DBGBCR<n>_EL1.MASK, if it is a reserved value, will be clarified to state that it is **CONSTRAINED UNPREDICTABLE**.
- Accessibility for RAS registers will be relaxed to remove traps when there is a minimal RASv2 implementation.
- HCRX_EL2 behavior when EL2 is not implemented or SCR_EL3.HXEn is 0, and the interaction of the value of HCRX_EL2.MSCEn will be clarified.
- Mappings for corresponding SET and CLR registers will be updated to show that they map to one another.
- The relaxations for setting FAR on SVE instructions are relaxed to replace the dependency on FEAT_Debugv8p9.
- The values in TCR_EL2.IPS and PS fields that apply to FEAT_D128 will be clarified.

## Potential upcoming changes

Arm is constantly exploring ways to make the architecture presentation precise and clear. Towards this, the following changes are expected in future releases:

- Accessibility of unimplemented registers will be improved.
- Accessibility for memory mapped accesses to registers will be improved.
- Accessibility when there is a width mismatch between the accessor and the register will be improved.

- Configurability details will be captured more formally to define features, acceptable feature choices, and mapping of features to ID registers.