ARM CoreSight ™
CoreSight Design Kit for ARM9E/EJ-S (TM085)
Errata Notice

This document contains all errata known at the date of issue for revision r2p0 of Coresight Design Kit for ARM9E (DK9)

Errata for the following CoresSight Design Kit sub-components are listed in separate errata documents:

TM917 : AHB Trace Macrocell

TM910 : CoreSight ETM9

TM093 : CoreSight Generic Parts

Proprietary notice

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- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Component Revisions

This document reports the errata for all revisions of CoreSight Design Kit for ARM9 (DK9). Each release of DK9 contains several CoreSight sub-components, the revisions of each sub-component for each specific DK9 release are documented in Table 1 below. The errata for these sub-components are listed in separate errata documents.

	CoreSight Design Kit for ARM9 Revision		
Component	r0p0	r1p0	r2p0
AHB Trace Macrocell	r0p1	r0p3	r0p4
CoreSight ETM9	r0p0	r0p1	r0p1
CoreSight Generic Parts	r0p1	r1p0	r2p0

Table 1 CoreSight Design Kit for ARM9 sub-component revisions.

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

02 Oct 2009: Changes in Document v4

No changes in this document revision

20 Dec 2007: Changes in Document v3

Page	Status	ID	Cat	Summary
10	New	488014	Cat 2	CTI connections do not allow correct synchronised halting of multiple processors

25 Sep 2007: Changes in Document v2

Page	Status	ID	Cat	Summary
9	Updated	356613	Cat 2	CSSYS for CS DK9. Example system code incorrect (bad coding)
11	New	439113	Cat 3	HTM Comparison failure
12	New	457319	Cat 3	Example CoreSight subsystem (CSSYS) does not return error on unused APB
13	New	457325	Cat 3	Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH

11 Oct 2006: Changes in Document v1

Page	Status	ID	Cat	Summary
9	New	356613	Cat 2	CSSYS for CS DK9. Example system code incorrect (bad coding)

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r1p0	r2p0
356613	Cat 2	CSSYS for CS DK9. Example system code incorrect (bad coding)	X		
488014	Cat 2	CTI connections do not allow correct synchronised halting of multiple processors	X	X	
439113	Cat 3	HTM Comparison failure	X		
457319	Cat 3	Example CoreSight subsystem (CSSYS) does not return error on unused APB	X		
457325	Cat 3	Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH	X		

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

356613: CSSYS for CS DK9. Example system code incorrect (bad coding)

Status

Affects: product Coresight Design Kit for ARM9E (DK9).

Fault status: Cat 2, Present in: r0p0, Fixed in r1p0.

Description

There are wiring errors in the example CoreSight sub-system RTL (CSSYS.v) supplied within the Integration Kit:

- **PREADYDBGExt** and **PRDATADBGExt** are assigned but never used.
- **PSELDBG** is driven by two signals, once from the output of the APB decoder and once from a signal **PSELDBGExt** which is never driven.

Implications

May cause Design Rule Checking issues as well as synthesis issues.

Workaround

Implementers should modify the example code (CSSYS.v) to remove of references to the **PSELDBGExt** signal.

488014: CTI connections do not allow correct synchronised halting of multiple processors

Status

Affects: product Coresight Design Kit for ARM9E (DK9).

Fault status: Cat 2, Present in: r0p0,r1p0, Fixed in r2p0.

Description

One of the purposes of including a Cross Trigger Interface (CTI) in a system is to enable synchronised halting of multiple processors in the system, where if one processor enters debug state then all processors enter debug state. The current connections do not permit this to be performed correctly.

The current connections use the DBGACK output from each processor to drive the EDBGRQ input to other processors. When any processor exits debug state, because of the delay introduced by the CTI system, EDBGRQ is not de-asserted sufficiently quickly and any restarted processor will immediately re-enter debug state.

The normal procedure for avoiding this race condition is for the debug tool to disable the CTI network when restarting any processors. However, this means that synchronised halting is not enabled until the debug tool re-enables the CTI network. This delay can range from hundreds to many thousands of cycles, depending on system speeds and debug tool capabilities.

Conditions

Details on the conditions for this erratum and the routines to enable and disable the CTI network are available from ARM in the document titled “Processor Debug Connectivity”, document number PR106-PRDC-009311, which accompanies this errata document.

Implications

If the CTI network is not disabled when restarting the processors then the processors might never restart normal execution.

If the CTI network is disabled when restarting the processors, then synchronised halting is not possible until the debug tool has re-enabled the CTI network. Once the CTI network is re-enabled, if any processor has halted then all connected processors will halt.

Workaround

This is a workaround for system implementers and debug tool vendors need to be aware of these changes.

The erratum can be avoided by modifications to the connections between the processor and CTI. Details of these changes are available from ARM in the document titled “Processor Debug Connectivity”, document number PR106-PRDC-009311, which accompanies this errata document.

Errata - Category 3

439113: HTM Comparison failure

Status

Affects: product Coresight Design Kit for ARM9E (DK9).

Fault status: Cat 3, Present in: r0p0, Fixed in r1p0.

Description

If during the atbTrace.s test, conditions arise to cause an overflow of the HTM's FIFO, the post processing scripts that analyse the HTM trace might incorrectly report a failure.

Conditions

If the following items occur then the atbTrace.s test may report a failure

1. The HTM is enabled,
2. The FIFO within the HTM overflows
3. The comparison script (HTMCompare) cannot correctly interpret the trace data

Implications

This does not affect the integration testing of the HTM which is performed without the need to decompress trace data.

Workaround

none

457319: Example CoreSight subsystem (CSSYS) does not return error on unused APB

Status

Affects: product Coresight Design Kit for ARM9E (DK9).

Fault status: Cat 3, Present in: r0p0, Fixed in r1p0.

Description

Where a memory region does not decode to a real slave, the default slave should be used. In the case of APB, this is performed by tieing **PREADY** HIGH, **PSLVERR** HIGH and **PRDATA[31:0]** to 0x00000000.

For the example CoreSight subsystem, CSSYS, if a component with an APB interface is omitted, due to the absence of its `define then this region must select the default slave response. The existing implementation does not return **PSLVERRDBG** HIGH which may cause a debugger to assume that a component is present and that it is simply returning zeros.

Condition

This defect will occur if:

1. A memory mapped CSSYS component is not present. This can correspond to:
   - CSTPIU
   - CSETB
2. The region of memory for that component is accessed.

Implications

A debugger attempting to access an unused region of memory would expect an error response. No error response implies that a component is present. Under the above conditions, a tool may conclude that a component is present where one is not.

A debugger will not be able to determine the component as all reads to the unused region of memory will return zero (0x00000000).

Workaround

It is recommended that system integrators modify the example CoreSight subsystem (CSSYS) to ensure that, when components are absent, the unused regions of memory return error responses.

457325: Flush fails on unused ATB slave interfaces if AFREADYS is not tied HIGH

Status

Affects: product Coresight Design Kit for ARM9E (DK9).

Fault status: Cat 3, Present in: r0p0, Fixed in r1p0.

Description

The CoreSight Architecture recommends than any unused or unavailable interfaces must respond with **ATVALID** LOW, **AFVALID** LOW, **ATREADY** HIGH and **AFREADY** HIGH where appropriate (other signals may be tied LOW).

Within the Integration Kit, only a limited number of the ATB inputs to the funnel are required. These unused connections have **ATVALIDS**<x> tied LOW and **AFREADYS**<x> tied LOW, where **AFREADYS**<x> should be tied HIGH and <x> is one of the unused interfaces.

Normally a debugger should not enable unused inputs, however, the recommended tie offs ensure safe flush operations if one is enabled.

Conditions

The erratum will only be observed if:

1. The unused ATB input to CSSYS is incorrectly connected with **AFREADYS**<x> tied LOW
2. A debugger enables input port <x>
3. A flush operation is performed

Implications

When the flush request is requested by the trace sink, the Trace Funnel performs a flush of all its enabled ATB inputs. Until all the enabled inputs have returned **AFREADYS** HIGH, normal operation will not be resumed. Under these conditions the Trace Funnel will stop taking trace data from the active ATB inputs and wait on the unconnected inputs because they have not returned **AFREADYS** HIGH.

This does not affect trace operation if unconnected inputs are not enabled or have **AFREADYS** tied HIGH.

Workaround

For debug tools:

- Do not enable unused ATB inputs to the trace funnel.

For system integrators:

- Modify the Integration Kit to tie **AFREADYS**<x> HIGH.

Errata - Documentation

There are no Errata in this Category