Arm® CoreLink™ CMN-600AE Coherent Mesh Network

Software Developer Errata Notice

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Non-Confidential

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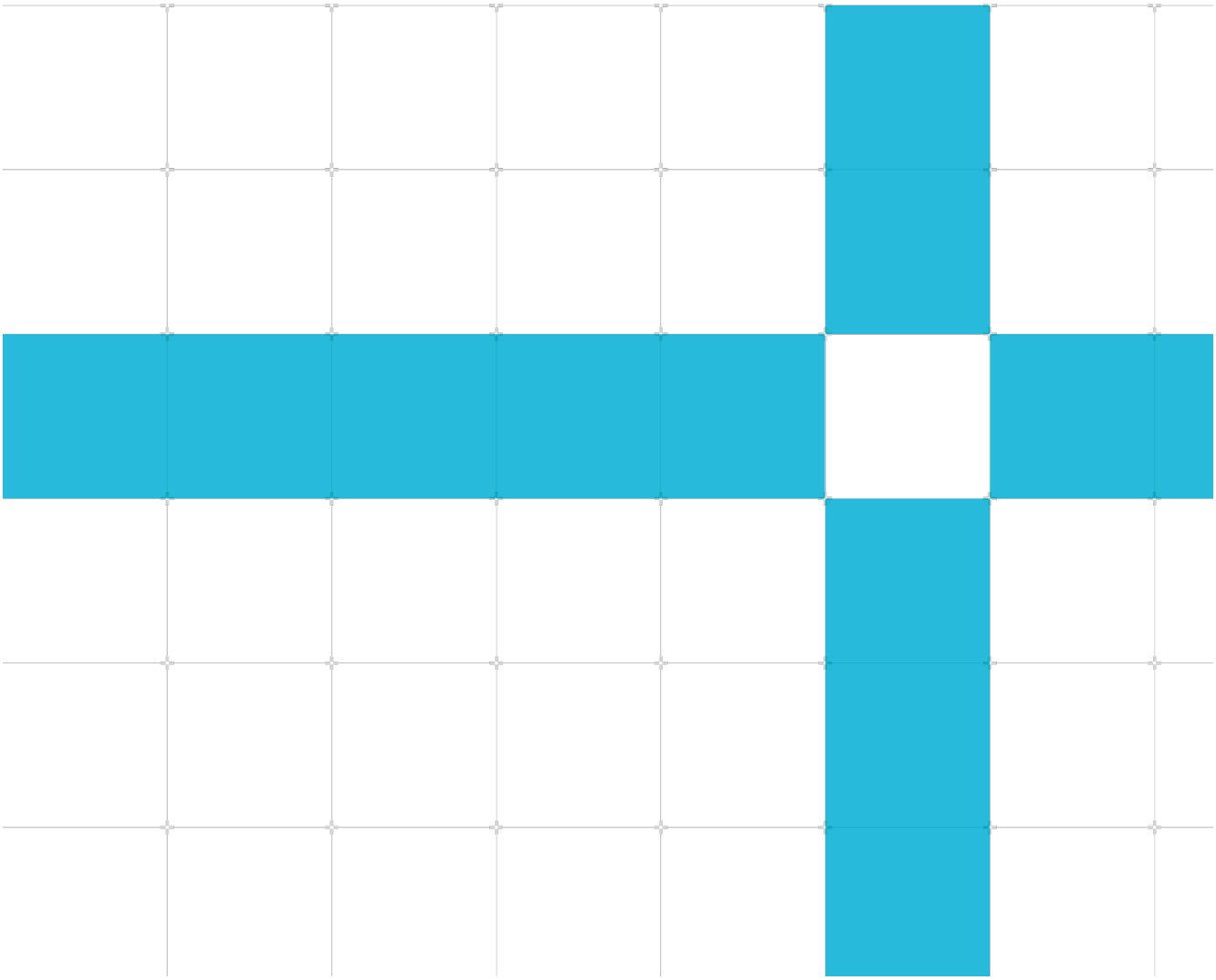
This document contains all known errata since the r0p0 release of the product.



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Contents

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The **errata summary table** identifies errata that have been fixed in each product revision.

07-Oct-2022: Changes in document version v8.0

ID	Status	Area	Category	Summary
2741288	New	Programmer	Category C	RAS HN-I and SBSX ERRGSR registers do not capture correct device instance information

21-Jan-2022: Changes in document version v7.0

ID	Status	Area	Category	Summary
2419818	New	Programmer	Category B	Accesses from RNs to RNI/RND/CXRH MPU registers permitted when APB Access Override is disabled

21-Sep-2021: Changes in document version v6.0

No new or updated errata in this document version.

26-Apr-2021: Changes in document version v5.0

ID	Status	Area	Category	Summary
2134907	New	Programmer	Category B	PCIe write ordering might not be maintained for writes that target a remote chip

16-Sep-2020: Changes in document version v4.0

ID	Status	Area	Category	Summary
1935203	New	Programmer	Category B	SECC error on ABF operation can cause coherency failures for other memory addresses

30-Apr-2020: Changes in document version v3.0

No new or updated errata in this document version.

20-Nov-2019: Changes in document version v2.0

No new or updated errata in this document version.

13-Jun-2019: Changes in document version v1.0

No errata in this document version.

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
2134907	Programmer	Category B	PCIe write ordering might not be maintained for writes that target a remote chip	r0p0, r1p0	Open
2419818	Programmer	Category B	Accesses from RNs to RNI/RND/CXRH MPU registers permitted when APB Access Override is disabled	r0p0, r1p0	Open
1935203	Programmer	Category B	SECC error on ABF operation can cause coherency failures for other memory addresses	r0p0, r1p0	Open
2741288	Programmer	Category C	RAS HN-I and SBSX ERRGSR registers do not capture correct device instance information	r0p0, r1p0	Open

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

2134907
PCIe write ordering might not be maintained for writes that target a remote chip

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0. Open.

Description

Two same-**AxID** writes from a PCIe Root Complex (RC) that target a remote chip might be reordered, resulting in a PCIe Ordered Write Observation (OWO) violation.

Configurations Affected

Any multi-chip CML configuration where a CXG is the target for PCIe write traffic.

Conditions

Both of the following conditions must be met for the erratum to exist:

- PCIe write traffic must target CXG (cross-chip traffic).
- RN SAM target type must be programmed to CXRA.

Implications

PCIe ordering violation which might result in data corruption.

Workaround

Set the RN SAM memory region target type to HN-I for the memory region that is targeted by PCIe writes to CXG. This setting has the following effects:

- All writes (WriteNoSnp/WriteUniq/WriteUniqStash) are changed to Non-cacheable WriteNoSnp.
- All reads (RDONCE/ROMI/ROCI) are changed to Non-cacheable ReadNoSnp.
- Reads and writes will still look up the SF and SLC on remote HN-F but will not allocate a line in SLC on a miss.
- Performance implications:
  - Ordered PCIe writes targeting CXG have lower bandwidth since OWO ordering is maintained.
  - Allocating PCIe reads and writes will not allocate in remote SLC.

2419818
Accesses from RNs to RNI/RND/CXRH MPU registers permitted when APB Access Override is disabled

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0, r1p0 versions. Open.

Description

Per specification, when APB Access Override is disabled (FMU Control Register por_fmu_por_fmu_ctl, bit[3] = 0), read and write accesses from the RNs to the MPU, FDC and FMU configuration registers are not permitted. RN* reads should return all zeros with no error indication and writes should be silently dropped.

This erratum permits RNs to have unrestricted access to RN-I, RN-D and CXRH MPU registers.

Configurations affected

All configurations.

Conditions

APB Access Override is disabled (FMU Control Register por_fmu_por_fmu_ctl, bit[3] = 0).

Implications

Non-secure software running on RNs could illegally access RN-I, RN-D and CXRH MPU registers.

Workaround

Disallow RN* read and write access to the RN-I, RN-D and CXRH MPU configuration address regions. This is done by programming MPUs in XP (for RN-Fs), RN-I, RN-D and CXRH.

1935203
SECC error on ABF operation can cause coherency failures for other memory addresses

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0 and r1p0 versions. Open.

Description

CMN-600AE supports Address Based Flush (ABF) where upper and lower system addresses can be programmed and then request hardware-based engine to flush out that address range from all System Level Caches (SLC). This ABF state machine works in the presence of other memory requests.

Single-bit ECC errors on the ABF accesses can corrupt the CMN Snoop Filter state, and result in coherency failures for other unrelated memory addresses.

Configurations Affected

Any configuration of CMN-600AE where ABF is used.

Conditions

This bug appears when the following three conditions occur:

- SLC address from flush set/way is outside ABF programmed range AND
- SLC Tag read has single bit ECC error AND
- There is independent request in pipeline N cycles ahead of ABF request (where N is SLC_TAG_RAM_LATENCY)
  In this case, ABF request corrupts SF vector for independent request that's ahead of ABF causing coherency failure.

Implications

The ABF flush sequence can cause coherency fails for unrelated memory addresses during the sequence.

WorkAround

Use the CMN power management features to flush the SLC, flushes the full SLC contents vs. the upper/lower range.

Category B (rare)

There are no errata in this category.

Category C

2741288
RAS HN-I and SBSX ERRGSR registers do not capture correct device instance information

Status

Affects: CMN-600AE
Fault Type: Programmer Category C
Fault Status: r0p0, r1p0. Open.

Description

The CMN Error Group Status Registers (ERRGSR) capture device instance error information for RAS events. The registers indicate the device instance within a device group. The registers are not updated correctly for the HN-I and SBSX device groups, so cannot be used to determine the device instances for RAS events.

Configurations Affected

All CMN-600AE configurations that use RAS error logging.

Conditions

A RAS event triggered by an HN-I or SBSX device.

Implications

Software cannot use the HN-I or SBSX ERRGSR registers.

Workaround

The RAS handler must read the individual HN-I and SBSX instance RAS logging registers when RAS interrupts occur.