ARM 7500

Product Overview

Document Number: ARM DVI 0002B

Issued: September 1995

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ARM7500 Product Overview

Change Log

Issue	Date	By	Change
A	Sep 94		Created
B	Oct 95	AP	Updated to conform to the house style.

Introduction

ARM7500 is a highly integrated, high performance, low power RISC based single chip computer centred around a cached ARM7 processor macrocell. The device is aimed at low cost consumer multimedia applications such as set top boxes and games consoles, but can also be used readily in navigation, EPOS, security and instrumentation products.

ARM7500 contains all the functionality required to create a complete computing system with the minimum of external components. It has memory and I/O control on-chip, to enable the direct connection of external memory and I/O peripheral devices. A sophisticated video controller allows the ARM7500 to directly drive an LCD or CRT display. The chip also includes two sound interfaces.

Features

ARM7500 has the following features:

- highly integrated multimedia microcontroller with **minimum cost/high performance** design goals
- ARM7 RISC cpu (30 Dhrystone (2.1) MIPS @ 33MHz), including 4K-byte combined i/d Cache, memory management unit and write buffer
- direct connection of ROM and DRAM
- memory configured as two 16 Mbyte ROM banks and four 64Mbyte DRAM banks
- 16-bit or 32-bit memory widths programmable for each bank
- 288 Mbyte address space
- 3 channel DMA controller (Video, cursor and sound) with 63.6 Mbytes/sec peak transfer rate
- I/O controller supports an AT-style PC bus and PCMCIA execute-in-place
- 2 serial keyboard/mouse ports.
- 4 ADC channels for joystick connection
- sound system with CD quality 32-bit serial and 8 channel analogue stereo sound
- video controller with up to 120MHz pixel clock
- resolution better than SVGA/XGA
- 16 Million colours from a 256 entry palette
- red, green and blue 8-bit linear DACs for direct CRT drive
- 16 level grey scaler for LCD displays
- two power management modes, SUSPEND and STOP (<50µA typ)
- typical power consumption for normal operation at 32 MHz is 680mW driving at a SVGA CRT, 430 mW driving an LCD (0.25 VGA)
- available in 240 pin PQFP package

Applications

The wide range of features incorporated into ARM7500 make it an extremely flexible device. It can be programmed, according to the required application, to optimise for high performance or low power, or a combination of both.

Portable computing, instruments and test equipment

Power management circuitry coupled with the power efficient characteristics of the ARM processor macrocell makes the ARM7500 particularly suitable for low power portable applications. 32-bit and 16-bit wide memory systems are supported, so a high performance 32-bit system or a lower cost 16-bit based system can be designed.

The ARM7500 will drive monochrome (single or dual panel) and colour LCDs.

Multimedia, graphic display systems and games consoles

The combination of the ARM macrocell processing power and the peripheral macrocells make the ARM7500 particularly suited to any application requiring high quality video, sound and general data I/O.

The four on-chip A to D converters allow the connection of analogue joysticks. The serial ports allow keyboard and mouse connection.

Example Of a Set-Top Application

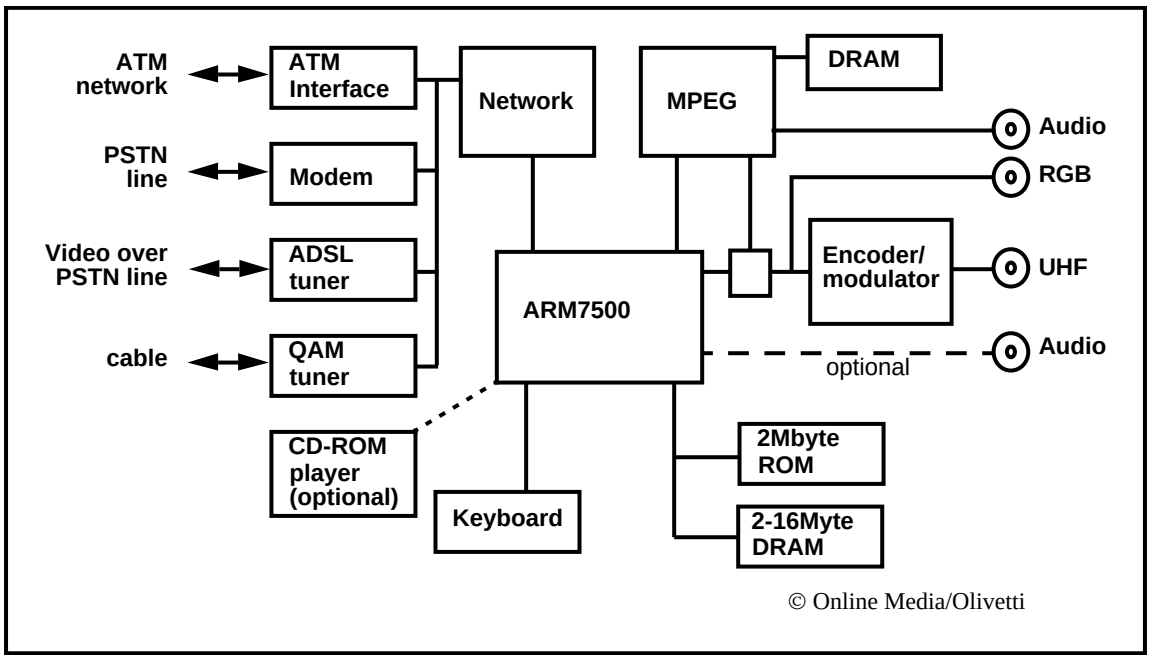


Figure 1: Set-top application example

ARM7500 Overview

ARM7500 is based around the ARM710C microprocessor macrocell. It includes a separate video and sound subsystem with a range of memory and I/O control features which together implement the majority of the functionality of a complete RISC based computing system. The ARM7500 block diagram is shown in *Figure 2: ARM7500 block diagram*.

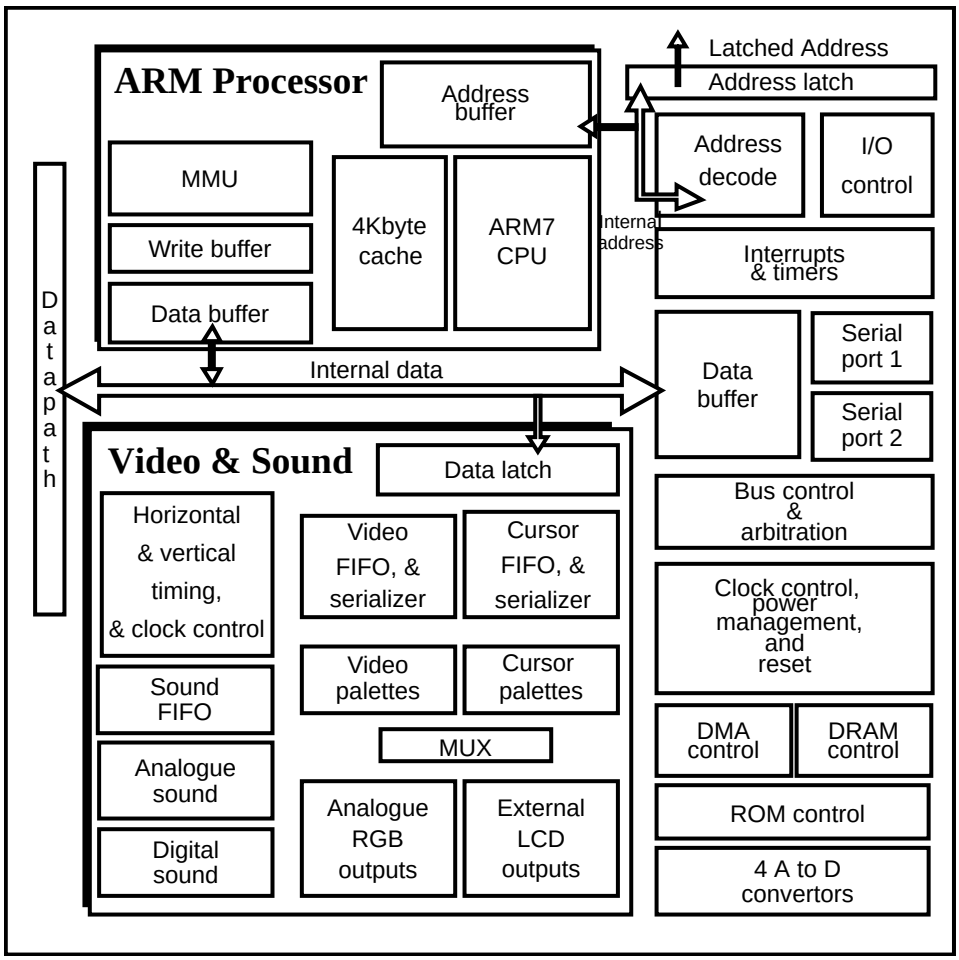


Figure 2: ARM7500 block diagram

The pinout diagram is shown on page 9.

ARM processor macrocell

The ARM710C is a 32-bit RISC microprocessor macrocell. It incorporates an ARM7 processor core, 4Kbyte cache, a write buffer, and a Memory Management Unit (MMU). It is fully static with very low power consumption.

The mixed data and instruction cache together with the write buffer substantially raise the average execution speed and reduce the average amount of memory bandwidth required by the processor. This allows the ARM7500 bus structure to support Direct Memory Access (DMA) channels with minimal performance loss.

The MMU supports a conventional two-level page-table structure and a number of extensions which make it ideal for embedded control, Unix and Object Oriented systems.

The instruction set comprises ten basic instruction types:

- Two instructions make use of the on-chip arithmetic logic unit, barrel shifter and multiplier to perform high-speed operations on the data in a bank of 31 registers, each 32 bits wide.
- Three classes of instruction control data transfer between memory and the registers, one optimized for flexibility of addressing, another for rapid context switching and the third for swapping data.
- Two instructions control the flow and privilege level of execution.
- Three types are dedicated to the control of external coprocessors which allow the functionality of the instruction set to be extended in an open and uniform way. However, the facility to add an external co-processor is not available on the ARM7500 so software emulation of the co-processor functions would be necessary.

The ARM instruction set is a good target for compilers of many different high-level languages. Where required for critical code segments, assembly code programming is also straightforward, unlike some RISC processors which depend on sophisticated compiler technology to manage complicated instruction interdependencies.

The memory interface has been designed to allow the performance potential to be realised without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals permit the ARM7500 to exploit the paged mode access offered by industry standard DRAMs.

Video and Sound macrocell

Video features

The video and sound macrocell gives the ARM7500 the flexibility to drive high specification CRT or low power LCD displays.

The video and sound macrocell can generate a display at any pixel rate up to 120MHz. To obviate the need for many crystals on the PCB, the video macrocell is designed to drive a Voltage Controlled Oscillator (VCO) to provide the master frequency. A large number of frequencies are possible with this approach. The 32MHz reference frequency generated within ARM7500 can be used to yield a number of common VCO frequencies.

The ARM7500 has a 28-bit wide, 256-entry palette. This is constructed out of three 8-bit wide look-up-tables (LUTs), each with 256 entries, named Red, Green, and Blue, and one 4-bit wide LUT with 16 entries, named Ext. The Red, Green and Blue LUTs each drive their respective DACs, whereas the Ext LUT is normally configured to drive an output port. These bits may be used outside the chip for a variety of purposes such as supremacy, fading, hi-resolution and LCD driving.

ARM7500 has a hardware cursor 32 pixels wide and any number of pixels high. Its 2 bits per pixel allow 4 colours (transparent plus three other colours from a selection of $2^{24)}$. It can display the hardware cursor in LCD mode.

ARM7500 can drive a:

- single panel Liquid Crystal Display at 1, 2, 4, 8, 16 or 32 bits per pixel
- dual panel LCD at 1, 2 or 4 bits per pixel.

Grey-scaling is provided at up to 16 shades.

ARM7500 is also capable of driving single panel colour LCDs with no grey scaling in its normal (video) mode.

Sound Features

The video and sound macrocell has two sound systems built into it. These are an 8-bit analogue stereo system, and a 32-bit serial sound interface suitable for driving external CD DACs.

Analogue stereo mode can work with 1, 2, 4 or 8 stereo channels. The 8-bit sound data is fed through a DAC to produce the sound signal. The DAC transfer characteristic consists of 16 linear segments (chords). Each chord has 16 steps, and the step size in one chord is twice that of the preceding chord. This gives an approximation to the μ225 law.

The serial sound interface offers a far superior 32-bit stereo sound (two 1- bit channels) from a three pin serial interface. The serial sound output can be used with any DAC with a serial sound input.

Clock control and power management

The clocking strategy for ARM7500 has been designed for maximum flexibility, and includes separate clock inputs for the CPU core clock, the Memory system clock and the I/O system clock in addition to the video clock inputs. Each of the three clock inputs has a selectable divide-by-two prescaler to generate a 50/50 mark-space ratio if required.

There are two levels of power management included. In SUSPEND mode, the clock to the CPU is stopped, but the display continues to work normally, until an interrupt is received. In STOP mode, all clocks are stopped. Two asynchronous wake up event pins are provided to terminate stop mode. Circuitry is included on chip to stop the oscillator and restart it cleanly when required.

Memory system

The memory system interface control logic is designed to be completely asynchronous in operation to the I/O control logic. This means the clock to the memory controller can be increased in frequency to allow fast memory to be used. The converse is also true, the clock can be slowed down for slow memory. This implementation allows the system designer to use what ever memory is available without having to alter any interface timing, ensuring maximum system flexibility.

ARM7500 can control a 32-bit or 16-bit wide memory system. The width of each bank of ROM or DRAM is selectable by programming appropriate register bits.

A DRAM controller is included which can directly drive up to 4 banks of DRAM. Four NRAS strobes individually select one of the four banks, and four NCAS strobes provide individual byte selection. The DRAM address multiplexing option provided will allow a wide variety of DRAM sizes from 256K to beyond 16MB to be used. Up to 256 page mode transfers may occur in one sequential burst.

When configured for operation with a 16-bit DRAM system, the DRAM controller will convert the access into two DRAM cycles to access the two halves of the 32-bit word. Byte transfers will only take one DRAM access cycle, even in 16-bit mode.

A programmable register allows one of four DRAM refresh rates to be selected. In addition, a register is provided to enable direct software control of the NCAS and NRAS lines for setting DRAM into a self refresh state.

A ROM controller supports two 16Mbyte banks of ROM with individually programmable read cycle timings. Support is provided for burst mode reads. Each ROM bank can be programmed to operate in 16-bit wide mode.

DMA

Three fully programmable DMA channels are included, for video, cursor and sound data. The DMA controller includes additional support for video DMA to enable the video macrocell to drive dual panel LCDs. The DMA controller is fast enough to acquire data at the same rate as the DRAM interface.

I/O control

The I/O bus of ARM7500 is 16 bits wide but for some types of access, can be expanded to 32 bits by the use of external transceivers. The input clock I_OCLK provides a reference for the subsystem which is nominally 32MHz.

There are three distinct I/O cycle types:

- Simple I/O with fixed 8MHz timings
- Module I/O with variable length 8MHz timings
- PC bus style I/O with fixed 16MHz timings and support for 32-bit data

Simple I/O

The Simple I/O type of access is 16-bit only and has 4 different cycle speeds selectable by address. When writing, the upper halfword of the ARM data bus is written out on the I/O bus. When reading, the I/O bus data is read back onto the lower halfword of the ARM data bus.

During these accesses, a chip select is asserted with an appropriate read or write strobe based on the 8MHz clock.

Module I/O

The Module I/O type of access is again16-bit only. Its speed is controlled by a handshake mechanism with the external hardware. The signals NIORQ (output) and NIOGT (input) are used for this handshaking. When writing, the upper halfword of the ARM data bus is written out on the I/O bus. When reading, the I/O bus data is read back onto the lower halfword of the ARM data bus.

During these accesses, a chip select is asserted but read and write strobes are not used.

PC bus style I/O

The PC bus style I/O type of access routes the lower halfword of the ARM bus through the device providing a direct 16-bit interface. Signals are generated to support the addition of external latches/drivers to extend the I/O data by 16 bits. The upper halfword of the ARM data bus is routed through these external devices if present.

There are 5 different address areas generating 5 different chip selects using the same type of access. There are 4 fixed cycle types based on the 16MHz clock, although the largest area only supports two of these cycle types. Any access may be held up by external circuitry removing the READY signal before the end of the cycle.

During these accesses, the relevant chip select is asserted as well as read or write strobes as appropriate.

Two special inputs are provided to allow external circuitry to route the full 32 bits through the 16-bit I/O bus using multiplexing. This allows, for example, the execution of code from a 16 bit PCMCIA card with suitable external controller. On a read I/O, if this latching signal is used, the data read back onto the ARM data bus comes from the I/O bus instead of the external extension latches.

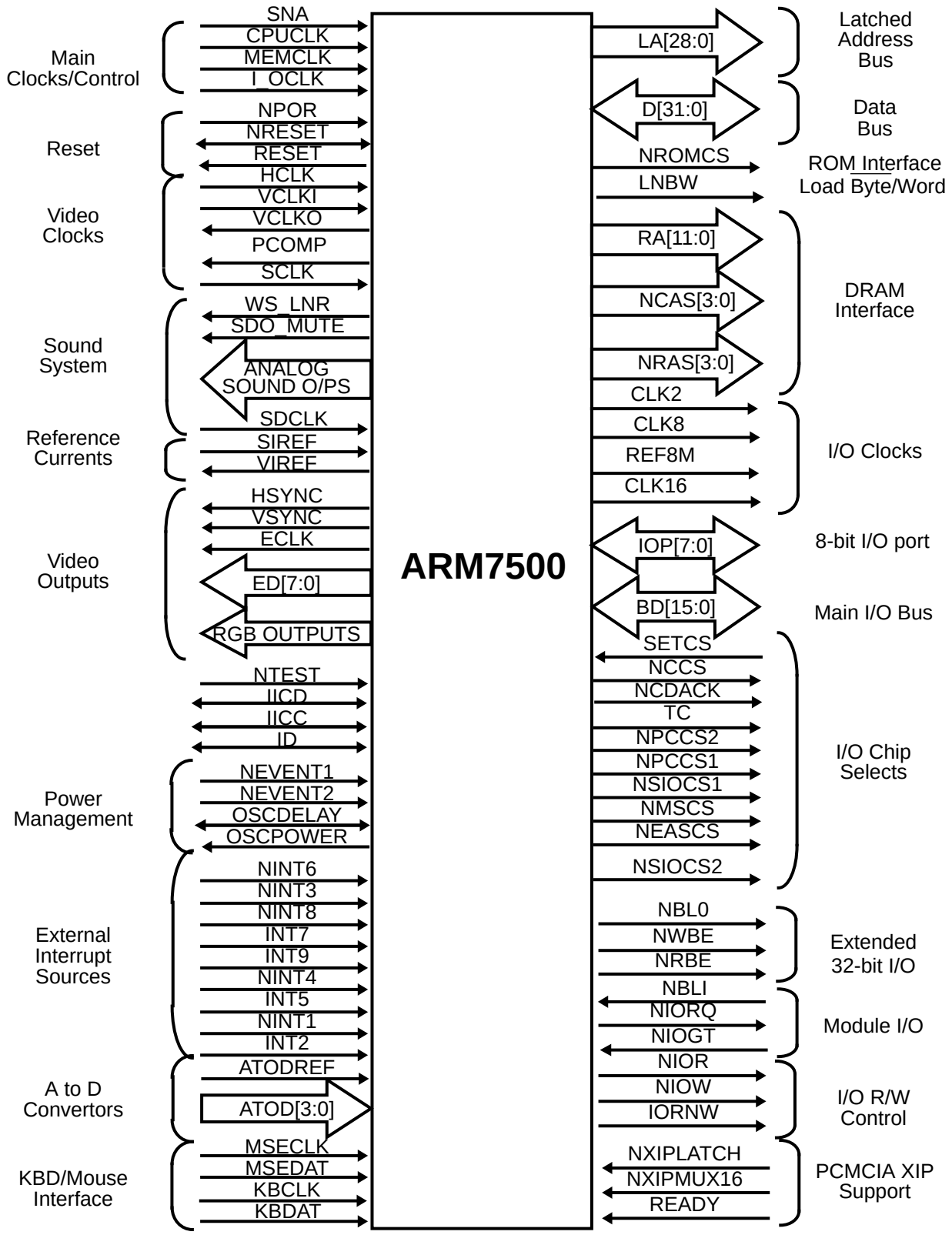
Other features

ARM7500 includes four slope integration A to D converter channels and two serial keyboard/mouse ports. There are 8 general purpose open drain I/O lines which can be used as inputs or outputs and as interrupt sources if required. An interrupt handler processes a variety of internal and external interrupt sources to generate the IRQ and FIQ interrupts for the ARM710C.

Tools and Support

ARM7500 is supported by a C compiler/assembler/utilities set of software tools. A software emmulator for cpu/instruction set emulation is also available.

There are also a number of third party operating systems available.


ARM7500
Main Clocks/Control
SNA
CPUCLK
MEMCLK
I_OCLK
Reset
NPOR
NRESET
RESET
Video Clocks
HCLK
VCLKI
VCLKO
PCOMP
SCLK
Sound System
WS_LNR
SDO_MUTE
ANALOG SOUND O/PS
Reference Currents
SDCLK
SIREF
VIREF
Video Outputs
HSYNC
VSYNC
ECLK
ED[7:0]
RGB OUTPUTS
NTEST
IICD
IICC
ID
Power Management
NEVENT1
NEVENT2
OSCDELAY
OSCPOWER
External Interrupt Sources
NINT6
NINT3
NINT8
INT7
INT9
NINT4
INT5
NINT1
INT2
A to D Convertors
ATODREF
ATOD[3:0]
KBD/Mouse Interface
MSECLK
MSEDAT
KBCLK
KBDAT
LA[28:0]
Latched Address Bus
D[31:0]
Data Bus
NROMCS
LNBW
ROM Interface
Load Byte/Word
RA[11:0]
NCAS[3:0]
NRAS[3:0]
DRAM Interface
CLK2
CLK8
REF8M
CLK16
I/O Clocks
IOP[7:0]
8-bit I/O port
BD[15:0]
Main I/O Bus
SETCS
NCCS
NCDACK
TC
NPCCS2
NPCCS1
NSIOCS1
NMSCS
NEASCS
NSIOCS2
I/O Chip Selects
NBL0
NWBE
NRBE
Extended 32-bit I/O
NBLI
NIORQ
NIOGT
Module I/O
NIOR
NIOW
IORNW
I/O R/W Control
NXIPLATCH
NXIPMUX16
READY
PCMCIA XIP Support