Arm® Musca-A Test Chip and Board

Technical Overview

arm

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Technical Overview

Release Information

Document History

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0000-00	31 January 2018	Non-Confidential	First issue
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The information in this document is Final, that is for a developed product.

Web Address

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Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Conformity

The *Waste Electrical and Electronic Equipment* (WEEE) marking, that is, the crossed out wheelie-bin figure, indicates that this product must not be disposed of with general waste within the European Union. To prevent possible harm to the environment from uncontrolled waste disposal, the user is required to recycle the product responsibly to promote reuse of material resources. To comply with EU law, you must dispose of the product in one of the following ways:

- Return it to the distributer where it was purchased. The distributer is required to arrange free collection when requested.
- Recycle it using local WEEE recycling facilities. These facilities are now very common and might provide free collection.
- If purchased directly from Arm, Arm provides free collection. Please e-mail *weee@arm.com* for instructions.

The CE Declaration of Conformity for this product is available on request.

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling this product.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across any sensitive equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

Contents
Arm® Musca-A Test Chip and Board Technical Overview

Preface

This preface introduces the *Arm® Musca-A Test Chip and Board Technical Overview*.

It contains the following:

About this book

This book gives an overview of the Musca-A test chip and all board variants.

Intended audience

This book is written for experienced hardware and software developers to enable low-power, secure IoT endpoint development using the Musca-A test chip and board.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter introduces the Musca-A test chip and Musca-A board.

Chapter 2 Hardware and software
This chapter gives an overview of the Musca-A board and test chip hardware and software.

Appendix A Specifications
This appendix contains electrical specifications of the Musca-A board.

Appendix B Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

`<and>`
Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

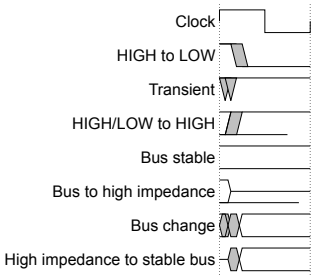

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n
: At the start or end of a signal name, n denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications
- *Arm® Musca-A Test Chip and Board Technical Reference Manual* (101107).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Overview* (101123).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Reference Manual* (DDI 0574B).
- *Arm® CoreLink™ SIE-200 System IP for Embedded Technical Reference Manual* (DDI 0571).
- *Arm® Cortex®-M System Design Kit Technical Reference Manual* (DDI 0479).
- *Arm® Cortex®-M33 Processor Technical Reference Manual* (100230).
- *PrimeCell UART (PL011) Technical Reference Manual* (DDI 0183).
- *Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual* (DDI 0224).
- *CoreSight™ Components Technical Reference Manual* (DDI 0314).
- *Arm® DS-5 Arm DSTREAM User Guide.* (DUI 0481).
- *Arm® DS-5 Using the Debug Hardware Configuration Utilities* (DUI 0498).

The following books are only available to licensees or require registration with Arm.
- *Arm® CryptoCell-312 Technical Reference Manual* (100774).
- *Arm® v7-M Architecture Reference Manual* (DDI 0403).

Other publications

None.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm Musca-A Test Chip and Board Technical Overview*.
- The number 101195_0000_02_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

Arm tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter introduces the Musca-A test chip and Musca-A board.

It contains the following sections:

1.1 Precautions

This section describes precautions that ensure safety and prevent damage to your Musca-A board.

This section contains the following subsections:

1.1.1 Ensuring safety

The DAPLink 5V USB connector supplies power to the Musca-A board.

——— Warning ———

Do not use the Musca-A board near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.

———————————

1.1.2 Operating temperature

The Musca-A board has been tested in the temperature range 0°C-30°C.

1.1.3 Preventing damage

The Musca-A board is intended for use within a laboratory or engineering development environment.

——— Caution ———

To avoid damage to the Musca-A board, observe the following precautions:

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not fit an Arduino Shield while the Musca-A board is powered up.

———————————

1.2 About the Musca-A board

The Musca-A board is a development system that demonstrates the foundation of single-chip secure *Internet of Things* (IoT) endpoints.

The Musca-A board provides access to the Musca-A test chip which implements the Arm CoreLink SSE-200 Subsystem for Embedded product. The Musca-A test chip, and the SSE-200, enable design and development of a low-power, secure IoT endpoint.

The Musca-A test chip features two Cortex-M33 processors, a memory system, and sensor interfaces.

The Musca-A board enables development and evaluation of custom software on the Musca-A test chip. The board and test chip provide the following main features:

- CoreLink SSE-200 Subsystem for Embedded that includes, but is not limited to, the following:
  - CPU0 element: One Cortex-M33 processor. No FPU, no DSP, no coprocessor.
  - CPU1 element: One Cortex-M33 processor. FPU, DSP, no coprocessor.
  - Two 2KB caches, one for each processor.
  - 4 × 32KB SRAM: CPU0 96KB + CPU1 32KB *Tightly Coupled Memory* (TCM).
  - 2MB system memory SRAM.
  - Arm CryptoCell-312 (partial functionality).
- On-board DAPLink that provides the following access:
  - *Serial Wire Debug* (SWD).
  - *USB Mass Storage Device* (USBMSD).
  - UART. The UART on the Musca-A test chip does not support hardware flow control.
  - Remote reset.
- On-board:
  - 3-axis orientation and motion sensor (gyro sensor).
  - Temperature sensor/ADC/DAC.
  - *Quad Serial Peripheral Interface* (QSPI) 8MB boot flash.

  ———— **Note** ————

  Normal Musca-A test chip boot operation is from external QSPI 8MB boot flash memory. Only the lowest 256KB of QSPI memory is directly accessible. More memory is accessible through indirect addressing.

  ————————————

- P-JTAG processor debug and SWD header.
- User RGB LED, status LEDs, user reset, and ON/OFF push buttons.
- Board is powered from USB 5V power or li-ion rechargeable battery backup (battery not supplied), selectable by a slider switch.

The Musca-A board provides headers for Arduino Shield expansion to support development of custom designs. The Shield interface provides:

- 16 3V3 GPIO.
- UART, no hardware flow control.
- SPI (master only).
- I^2C.
- I^2S.
- 3-channel PWM.
- 6-channel analog interface.

1.3 Location of components

The following figure shows the physical layout of the Musca-A board.

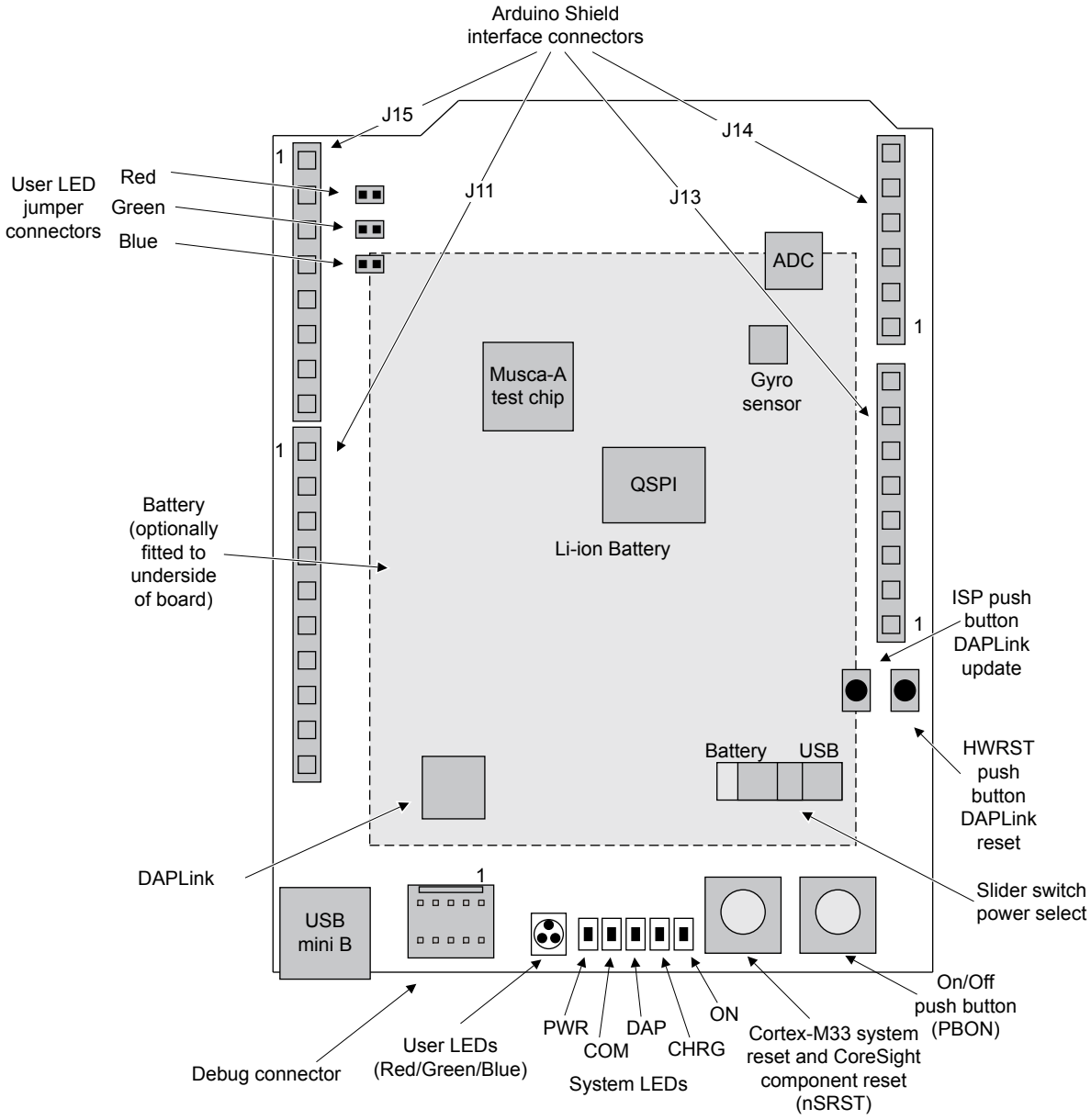

Figure 1-1 Layout of the Musca-A board

1.4 Part numbers and ordering information

The following table contains part numbers for ordering different Musca-A board variants.

Table 1-1 Musca-A board variants

Board variant	Board	Arm part number (MSI number)	Board HBI Number	Comment
varA	MUSCA-A1 TESTCHIP Board	V2M-MUSCA-0345A	HBI-0326A	-
varB	MUSCA-A2 TESTCHIP Board	V2M-MUSCA-0345B	HBI-0326B	Musc-A1 test chip updated to Musca-A2 for hardened security testing.
varC	MUSCA-A2 TESTCHIP Board (HP)	V2M-MUSCA-0345C	HBI-0326C	Musc-A1 test chip updated to Musca-A2 for hardened security testing. More power available to Arduino Shield.

Chapter 2
Hardware and software

This chapter gives an overview of the Musca-A board and test chip hardware and software.

It contains the following sections:

2.1 Board hardware

The hardware infrastructure of the Musca-A board provides access to the Musca-A test chip and supports Shield expansion.

Overview of Musca-A board hardware

The user peripheral interfaces connect directly between the Musca-A test chip and the peripheral device, or between the test chip and the Shield header.

The DAPLink controller functions:

- As a DAPLink to provide the following over USB:
  - *Serial Wire Debug* (SWD).
  - UART. The UART on the Musca-A test chip does not support hardware flow control.
  - *USB Mass Storage Device* (USBMSD for user QSPI code or DAPLink firmware update).
  - Remote reset.
- As a system controller to control the following:
  - Power supplies.
  - Resets.
  - SCC pre-loading.

The following figure shows the hardware infrastructure of the Musca-A board.

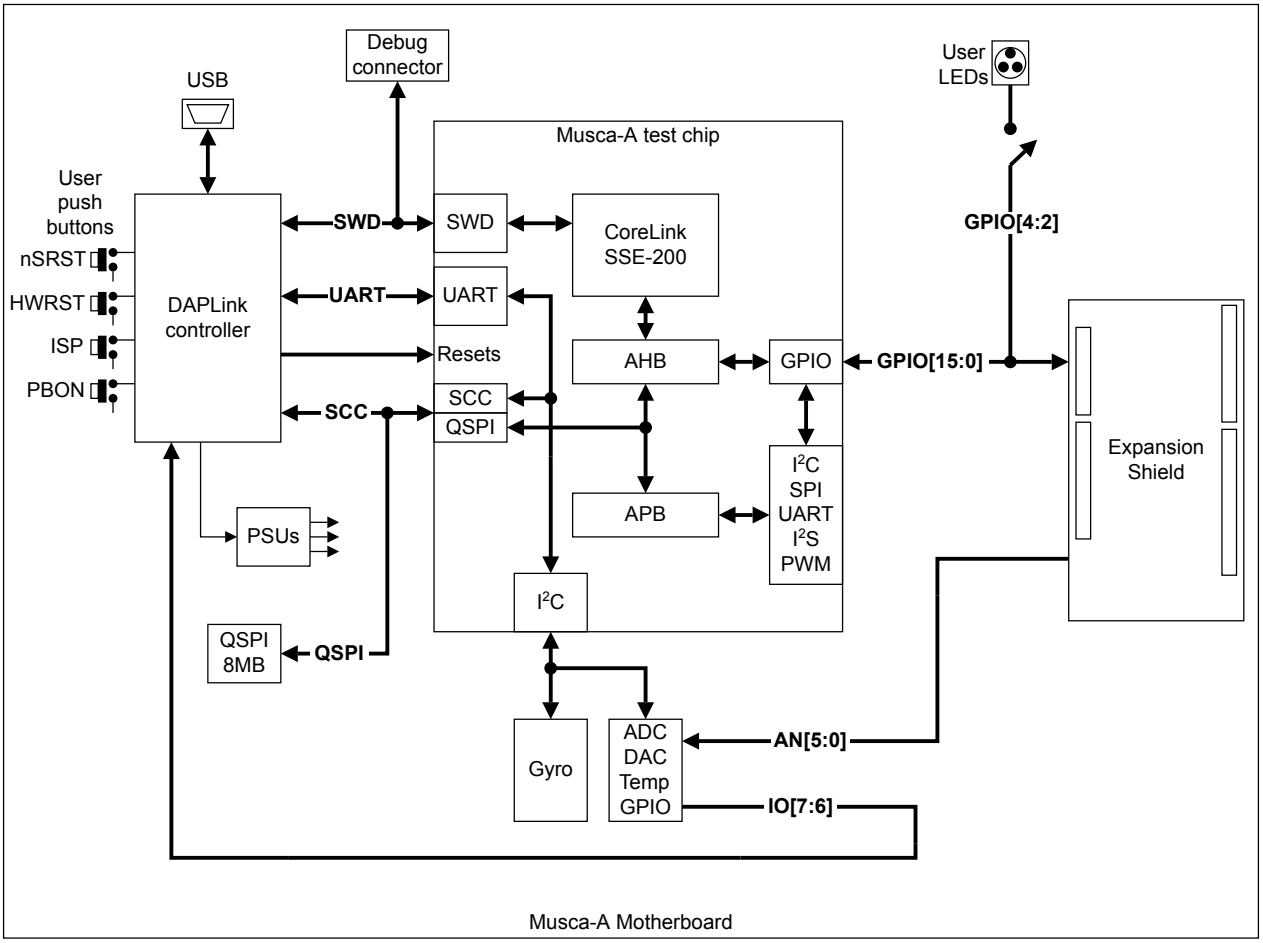

Figure 2-1 Hardware infrastructure of the Musca-A board

Musca-A board components

The Musca-A board contains the following components:

- Musca-A test chip, incorporating CoreLink SSE-200 subsystem:
- Arduino Shield expansion to enable custom designs:
  - UART. The UART on the Musca-A test chip does not support hardware flow control.
  - I^2S.
  - SPI (master only).
  - I^2C.
  - PWM.
  - 6-channel analog input from on-board combined ADC/DAC.
  - 16 3V3 GPIO.
- On-board DAPLink that enables the following functionality over USB:
  - *Serial Wire Debug* (SWD).
  - *USB Mass Storage Device* (USBMSD).
  - UART. The UART on the Musca-A test chip does not support hardware flow control.
  - Remote reset.
- On-board gyro sensor:
  - MMA7660FC 3-axis orientation and motion detection sensor.
  - I2C interface to Musca-A test chip.
- On-board combined ADC/DAC/temperature sensor:
  - AD5593.
  - 6-channel 3V3 ADC/DAC/GPIO output to Arduino Shield.
  - ADC output to DAPLink controller.
  - Temperature indicator.
- 8MB On-board QSPI boot flash:
  - Both Secure and Non-secure access.
  - Normal Musca-A test chip boot operation is from external QSPI 8MB boot flash memory. Only the lowest 256KB of QSPI memory is directly accessible. More memory is accessible through indirect addressing.
- Debug connector that provides access to:
  - P-JTAG processor debug.
  - *Serial Wire Debug* (SWD).
- User push-button:
  - PBON On/Off push-button.
  - nSRST: Cortex-M33 system reset and CoreSight component reset.
  - ISP: Updates DAPLink firmware.
  - HWRST: Resets DAPLink.
- RGB LED. Jumper connectors provide optional connections between:
  - Red LED and connection between Arduino header and Musca-A test chip GPIO[2] pin, optional PWM0.
  - Green LED and connection between Arduino header and Musca-A test chip GPIO[3] pin, optional PWM1.
  - Blue LED and connection between Arduino header and Musca-A test chip GPIO[4] pin, optional PWM2.

    Note

    The SCC registers select the functions of pins GPIO[4:2].

- Status LEDs.
- 5V USB or battery power, selectable by slider switch:
  - DAPLink 5V USB connector.
  - CLN 523450, Lithium Ion, 3.7V, 950mAh (not supplied).

2.2 Architecture of the Musca-A test chip

The Musca-A test chip features Cortex-M33 processors, a memory system, integrated connectivity, and sensor interfaces.

Overview of Musca-A test chip

The Musca-A test chip consists of the SSE-200 subsystem with external memory, interfaces, clock generator, and *Serial Configuration Control* (SCC) registers for setting default powerup values.

See the following documentation for more information on the SSE-200 subsystem:

- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Overview*.
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Reference Manual*.

See the *Arm® Musca-A Test Chip and Board Technical Reference Manual* for more information on the Musca-A test chip.

The following figure shows a high-level view of the architecture of the Musca-A test chip.

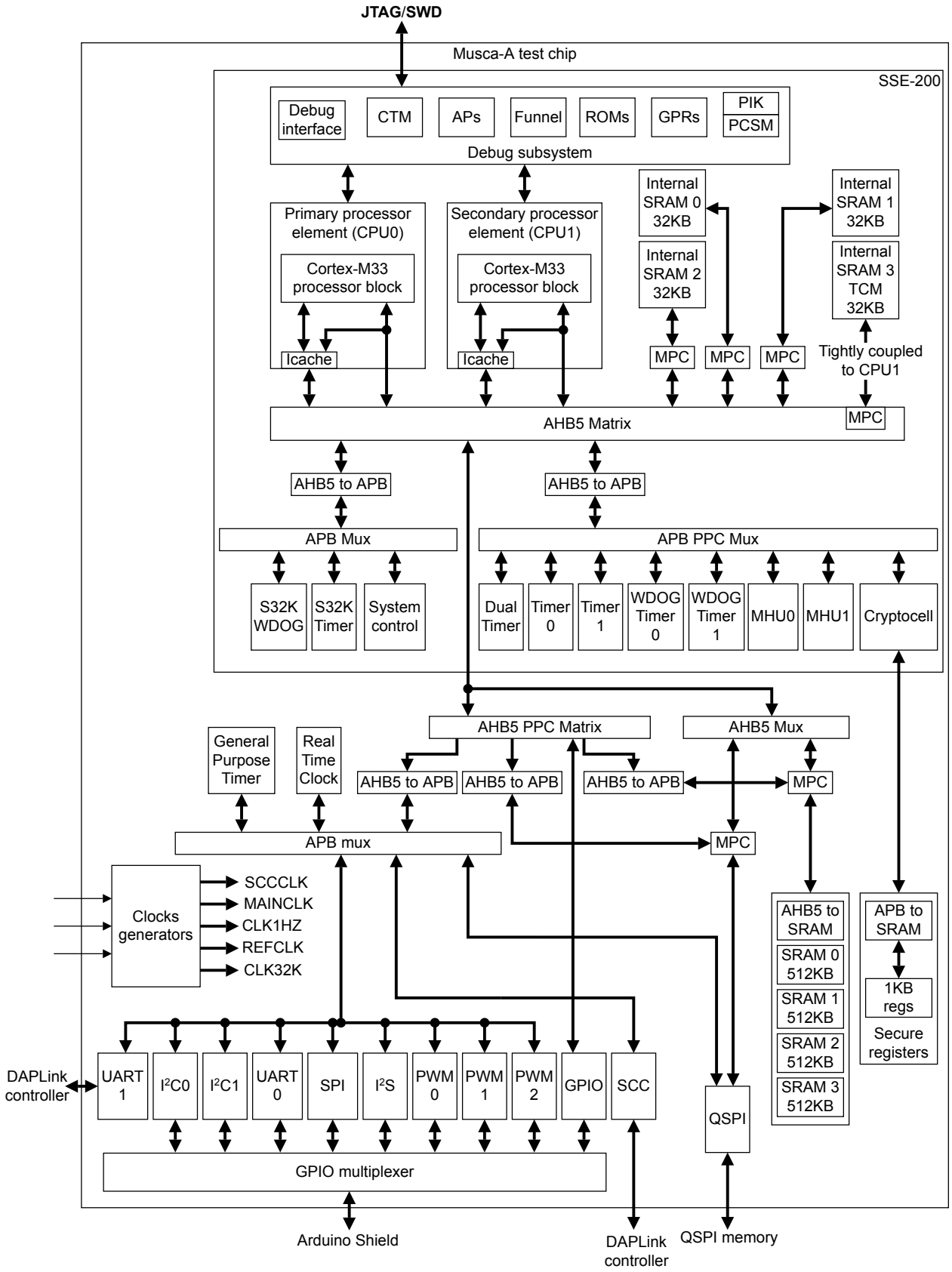

Figure 2-2 Architecture of the Musca-A test chip

Major components and systems of the Musca-A test chip

SSE-200 subsystem

- Two processors:
  - CPU0 element: Cortex-M33 No FPU, no DSP, no coprocessor, 50MHz maximum. Used as main processor.
  - CPU1 element: Cortex-M33 with FPU and DSP, no coprocessor, 170MHz maximum.
- Memory system:
  - One 2KB cache for each Cortex-M33 processor.
  - System 96KB SRAM and 32KB Tightly Coupled Memory (TCM) tight coupled to CPU1. Organized as 4 × 32KB.
- CoreSight component and *Serial Wire Debug* (SWD).
- CryptoCell-312 (partial functionality).
- Secure AMBA® interconnect:
  - AHB5 Bus matrix.
  - AHB5 TrustZone® Memory Protection Controller (MPC).
  - AHB5 TrustZone Peripheral Protection Controller (PPC).
  - AHB5 Exclusive Access Monitor (EAM).
  - AHB5 Access Control Gates. (ACG).
  - AHB5 to APB bridges.
  - Expansion AHB5 master and slave buses - two each.
- Security components:
  - *Implementation-defined Attribution Unit* (IDAU).
  - Secure and Non-secure configurable peripherals and memory access.
  - Secure boot.
- Secure APB peripherals:
  - One general-purpose timer with configurable security in the **S32KCLK** domain.
  - Two general-purpose timers, Timer0 and Timer1, in the **SYSCLK** domain.
  - One Cortex-M System Design Kit (CMSDK) dual timer with configurable security.
  - One secure watchdog in the **S32KCLK** domain.
  - Two secure watchdogs in the **SYSCLK** domain.

Musca-A test chip outside the SSE-200 subsystem

- 2MB Code SRAM: 4 × 512KB independently power-enabled.
- 1KB Security Registers emulating One-Time Programming (OTP).
- One Real Time Clock (RTC) in the Always ON domain.
- One 32-bit general-purpose timer running on 32.768kHz with programmable interrupts.
- 16 external (GPIO) interrupts.
- 16 GPIO.
- Three-channel I^2S:
  - Two master transmitters.
  - One master receiver.
- Three independent *Pulse Width Modulation* (PWM) outputs.
- Two UARTs, UART0 user, UART1 debug. The UART on the Musca-A test chip does not support hardware flow control.
- Two I^2C:
  - I^2C0. Can be used as Master (default) or slave.
  - I^2C1. Master only to on-board interfaces.
- One SPI, master only.
- One alternate function I/O multiplexer (all function DIOS).
- One QSPI for external flash control with *Execute in Place* (XIP) capability.
- Off-chip QSPI flash boot.
- External powerup reset.
- Three system clock sources:
  - External **REFCLK**, 32.768kHz.
  - External **FASTCLK**, 32MHz.
  - On-chip PLL. Input 32.768kHz. Output up to 200MHz to Cortex-M33 processors.
  - Debug:
    - One JTAG/SWD port.
- One Serial Configuration Controller (SCC) with dual access port:
  - SCC serial during reset.
  - APB after reset.

2.3 Software, firmware, board, and tools setup

Arm supplies software and firmware for the Musca-A board.

Software and firmware

You can access software and firmware at the Arm Community pages which are accessible from *https://www.arm.com/musca*.

Setting up a project

To power the board, connect the USB port to your computer and press the PBON user push button. The DAPLink interface appears in the Windows device manager as an Mbed composite device part of which is the Mbed serial port (UART). The following figure shows an example configuration which shows the Mbed composite device and the Mbed serial port.

Note

Other components of the Mbed composite device are not visible in the Windows device manager. See *2.1 Board hardware* on page 2-16 for the other components of the Mbed composite device.

The UART on the Musca-A test chip does not support hardware flow control.

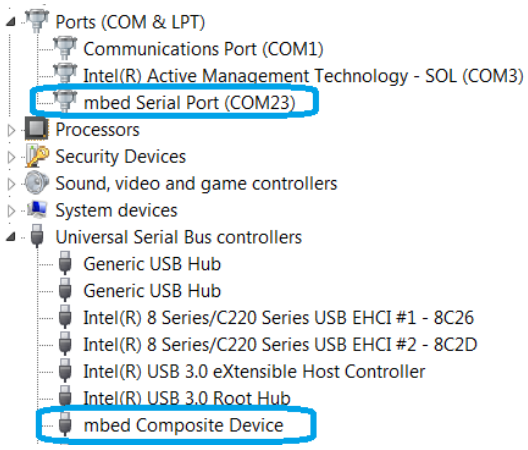

Figure 2-3 DAPLink interface

Updating DAPLink firmware

To update the DAPLink firmware, you can use the DAPLink drag and drop update method:

1. Press and hold the ISP button while powering up the board using the USB lead.
2. Delete file `firmware.bin` that appears in the `CRP DISABLD USB` drive.
3. Copy `DAPLink_QSPI_XTAL_v1.2.bin`, or a later version, to the `CRP DISABLD drive`.
   - From a Windows system, you can simply Drag and Drop the file.
   - On Linux/Mac OS, use the following command:

     ```
     dd if={new_firmware.bin} of=/Volumes/CRP\ DISABLD/firmware.bin conv=notrunc
     ```

4. Power cycle the board using the USB lead. Do not press the ISP button during the power cycle.

Updating QSPI software image

To update the QSPI image, perform the following steps:

1. Power up the board by connecting the USB lead and pressing the PBON push button.
2. Drop a `.bin` format QSPI software image onto the `MBED` drive, for example `blinky.bin`.
3. Power cycle the board or press the nSRST button to reset the system and boot from the new QSPI software image.

Note

The file `blinky.bin` is available at the Arm Community pages which are accessible from *https://www.arm.com/musca*.

DAPLink UART setting

The default DAPLink UART setting is:

- 115,200 baud (8N1).

Appendix A
Specifications

This appendix contains electrical specifications of the Musca-A board.

It contains the following section:

A.1 Electrical specifications

See the *Arm® Musca-A Test Chip and Board Technical Reference Manual* for information on the Musca-A board power supply rails and maximum current loads.

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- *B.1 Revisions* on page Appx-B-27.

B.1 Revisions

The following table lists the technical changes between released issues of this book.

Table B-1 Issue 101195_0000_00

Change	Location	Affects
No changes, first release.	-	-

Table B-2 Differences between issue 101195_0000_00 and issue 101195_0000_01

Change	Location	Affects
SPI available as master interface only.	*1.2 About the Musca-A board* on page 1-12. *2.1 Board hardware* on page 2-16. *2.2 Architecture of the Musca-A test chip* on page 2-18.	All board versions
UARTs do not support hardware flow control.	*1.2 About the Musca-A board* on page 1-12. *2.1 Board hardware* on page 2-16. *2.2 Architecture of the Musca-A test chip* on page 2-18. *2.3 Software, firmware, board, and tools setup* on page 2-22.	All board versions
Added part numbers and board variant ordering information.	*1.4 Part numbers and ordering information* on page 1-14	All board versions
Added information on how to update DAPLink firmware from a Linux/Mac OS.	*2.3 Software, firmware, board, and tools setup* on page 2-22	All board versions

Table B-3 Differences between issue 101195_0000_01 and issue 101195_0000_02

Change	Location	Affects
Updated CE Conformance Notice.	*Conformance Notices* on page 3.	All board versions