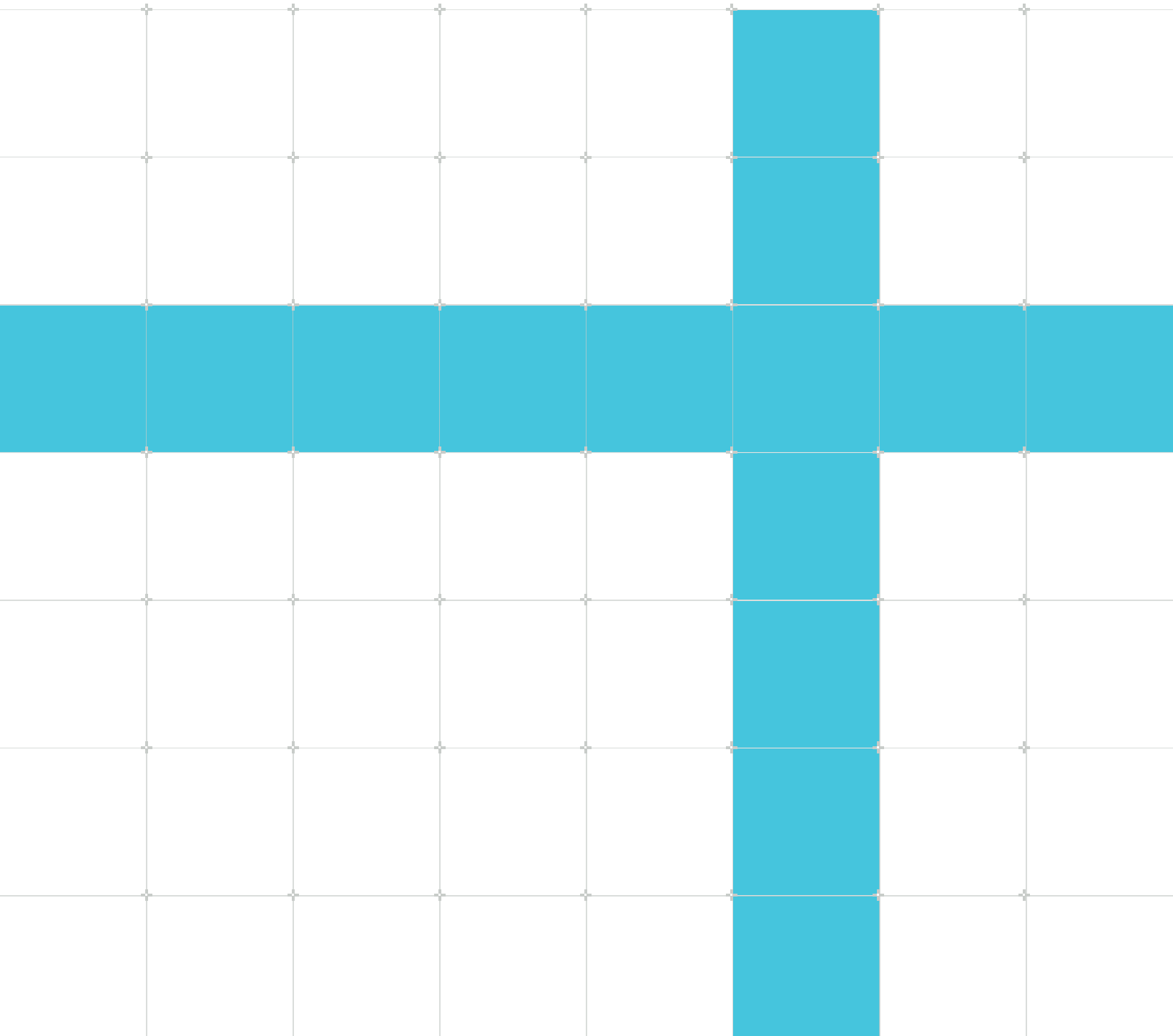
Release Note for Downloads Arm Development Studio Morello Edition

2022.0M0

Non-Confidential

Issue 01
109386_2022-0M0_01_en



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Release information

Document history

Issue	Date	Confidentiality	Change
2022_0M0-01	18 January 2022	Non-Confidential	2022.0M0 release

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(LES-PRE-20349|version 21.0)

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Contents

1. Release Note for Downloads Arm Development Studio Morello Edition 2022.0M0

The release notes contain:

- A highlight of the tools included in the suite
- What's included in Morello Edition
- How to get started with Development Studio
- How to provide feedback and get support
- Known limitations in this release

What's included in Development Studio Morello Edition?

Arm Development Studio for Morello combines the professional Arm development environment with extended capabilities to aid the Arm Morello program with architecture exploration and software design.

Arm Development Studio IDE

Arm Development Studio IDE is a professional software development solution for bare-metal embedded systems. It covers stages in development from boot code, to kernel and driver porting for bare-metal debugging. The Morello Fixed Virtual Platform (FVP) and compiler are provided independently, and can be imported to be used in the IDE. Please refer to the Morello program resources page to gain access to the installations binaries.

Arm Debugger

Arm Debugger is a graphical debugger supporting software development on Arm processor-based targets and Fixed Virtual Platforms (FVP).

This release of the Debugger adds debug and trace support for the Morello System Development Platform (SDP), in addition to the existing debug and trace support for Morello FVP. The SDP is a development platform for hardware prototyping, software development, system validation, and performance profiling or tuning. It includes the Morello SoC running an open-source software stack, and an embedded debug probe.

Arm Streamline

Arm Streamline is a system-wide performance analysis tool to analyze Linux, Android, and bare-metal embedded systems. Streamline's visualization tools make it easy to find performance bottlenecks in CPU, GPU, and other Arm IP.

Examples

Bare-metal examples for Morello are provided. These may be compiled with the LLVM Compiler and then run/debugged on the Morello FVP.

A tutorial also shows how to connect to the Cortex-M7s in the Morello FVP, and debug the System Control Processor (SCP) and Manageability Control Processor (MCP) firmware that runs on them.

Supported Host Platforms

The list of supported host platforms is available online, in the Hardware and host platform requirements section of the Getting Started Guide.

This release adds support for Ubuntu 20.04 LTS as a host platform.

Getting Started

For an in-depth introduction to Development Studio, system requirements and installation instructions, please consult the online Getting started page. A copy of the Getting started guide is also included in your installation of Development Studio and accessible from within the IDE.

You can find tutorials, documentation and videos on the Development Studio Morello Edition welcome page.

Feedback & Support

You can raise queries and support issues relating to Development Studio on the Arm Community website.

Noteworthy Issues and Limitations

The following issues and limitations apply to this release:

- To collect a history of program execution ("trace") from the Morello System Development Platform (SDP), the DTSL options in the Debug Configuration must be configured appropriately. To collect trace from the Rainier cores, use CSTMC_3/ETF or CSTMC_2/ETR (using, for example, system memory address `0x10000000`). For DSTREAM-ST/-PT, off-chip trace (via the TPIU) is also possible. For DSTREAM-ST, use port width 4. For DSTREAM-PT, use port width 32. To collect trace from the Cortex-M7 cores, use CSTMC_2/ETR (using, for example, system memory address `0x10000000`) or off-chip trace (via the TPIU) with DSTREAM-ST/-PT as above.
- Software breakpoints may not work reliably on the Morello System Development Platform (SDP) unless the Error Correction Code (ECC) capability is enabled for the Registered Memory Modules (RDIMMs). To enable the ECC capability for correct DDR read/write, the DDR memory space being used (e.g. `0x80000000 - 0xFFFFFFFF`) must be zeroed before enabling the ECC bits. This is done in the Trusted Firmware (TF-A) code by:
  - https://github.com/ARM-software/arm-trusted-firmware/blob/master/plat/arm/board/morello/morello_bl2_setup.c#L23
  - https://github.com/ARM-software/arm-trusted-firmware/blob/master/plat/arm/board/morello/morello_bl31_setup.c#L179

As an alternative, hardware breakpoints may be used instead of software breakpoints.