ARM PrimeCell®
Micro-DMA Controller (PL230)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p0 of MicroDMA Controller -Perpetual

Proprietary notice

Document confidentiality status

This document is Non Confidential.

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Feedback on this document

If you have any comments on about this document, please send email to errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments.

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible.

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

05 May 2009: Changes in Document v3

Page	Status	ID	Cat	Summary
10	New	603116	Cat 3	Incorrect OVL warning "PL230_W01: paddr[1:0] is non-zero"
11	New	696269	Doc	The chnl_prot_ctrl bits of the dma_cfg APB register must not change when the master_enable bit is set

12 Mar 2007: Changes in Document v2

No changes in this document revision

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0-00rel0	r0p0-02rel0
696269	Doc	The chnl_prot_ctrl bits of the dma_cfg APB register must not change when the master_enable bit is set	X	X
603116	Cat 3	Incorrect OVL warning "PL230_W01: paddr[1:0] is non-zero"		X

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

There are no Errata in this Category

Errata - Category 3

603116: Incorrect OVL warning "PL230_W01: paddr[1:0] is non-zero"

Status

Affects: product MicroDMA Controller -Perpetual.

Fault status: Cat 3, Present in: r0p0-02rel0, Open.

Description

When PL230 is simulated, with OVL assertions, enabled the following assertion can be triggered by valid input stimulus:

PL230_W01: paddr[1:0] is non-zero. Only word aligned accesses supported

When the APB interface input **psel** is not asserted it is legal to drive any value on the inputs **paddr[1:0]**. The defect may cause the OVL warning to be generated when **psel** is not asserted.

Implications

When PL230 is simulated with OVL assertions enabled incorrect warnings may be given about the APB interface address not indicating a word aligned access.

Workaround

Compile PL230 without the OVL assertions. OVL assertions are enabled when the Verilog `define macros ASSERT_ON and OVL_ASSERT_ON are defined in the scope of the PL230 instance or on the simulator command line.

Errata - Documentation

696269: The chnl_prot_ctrl bits of the dma_cfg APB register must not change when the master_enable bit is set

Status

Affects: product MicroDMA Controller -Perpetual.

Fault status: Doc, Present in: r0p0-00rel0,r0p0-02rel0, Open.

Description

Section 3.2.2 "DMA configuration" of the "PrimeCell® µDMA Controller (PL230) Technical Reference Manual" (ARM DDI 0417A) should also state the following:

The chnl_prot_ctrl bits must not be changed when the master_enable bit is set because this may cause a protocol error on the AHB master interface. As the dma_cfg register is write-only the user must read the status of the master enable bit from the dma_status register.

Implications

none

Workaround

none

Errata – Driver Software

There are no Errata in this Category