

Arm® CoreLink™ DMC-620 Dynamic Memory Controller

Revision: r1p0

Technical Reference Manual



Arm CoreLink DMC-620 Dynamic Memory Controller

Technical Reference Manual

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Release information

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Product status

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Web address

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Preface

This preface introduces the *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual*.

It contains the following:

- [About this book](#) on page 7.
- [Feedback](#) on page 10.

About this book

This book is for the Arm® CoreLink™ DMC-620 Dynamic Memory Controller.

Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

rm Identifies the major revision of the product, for example, r1.

pn Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced hardware engineers who want to integrate the delivered ARM *System on Chip* (SoC) product in a SoC design.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter describes the DMC-620.

Chapter 2 Functional description

This chapter describes how the DMC-620 operates.

Chapter 3 Programmers model

This chapter describes the programmers model of the DMC-620.

Appendix A Signal descriptions

This appendix describes the DMC-620 signals.

Appendix B Revisions

This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the [Arm® Glossary](#) for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

monospace *italic*

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

monospace **bold**

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments.
For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

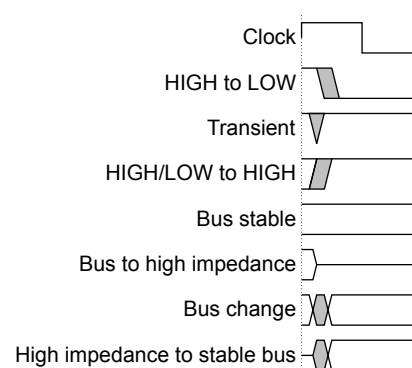


Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.
Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

- *Arm® AMBA® APB Protocol Specification* (Arm IHI 0024).
- *AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces* (Arm IHI 0068).
- *Principles of Arm® Memory Maps White Paper* (Arm DEN 0001).
- *Arm®v8.2 RAS Architecture Extension Specification*.

The following confidential books are only available to licensees:

- *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Configuration and Integration Manual* (Arm 100569).
- *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Design Manual* (Arm 100567).
- *Arm® CoreLink™ CCN-504 Cache Coherent Network Technical Reference Manual* (Arm 100017).
- *Arm® AMBA® 5 CHI Architecture Specification* (Arm IHI 0050).

Other publications

- *JEDEC STANDARD DDR3 SDRAM Specification*, JESD79-3D, <http://www.jedec.org>.
- *JEDEC STANDARD DDR3L SDRAM Specification*, JESD79-3-1A, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 SDRAM Specification*, JESD79-4, <http://www.jedec.org>.
- *JEDEC STANDARD DDR3 RDIMM Specification*, JESD82-29, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 SDRAM Registered DIMM Design Specification*, JESD21-C MODULE4.20.28, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 RCD Specification*, JESD82-31, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 DB Specification*, JESD82-32, <http://www.jedec.org>.
- *JEDEC STANDARD NVDIMM-N Byte Addressable Energy Backed Interface Design Specification*, JESD245, <http://www.jedec.org>.
- *DDR PHY Interface DFI 3.1 Specification*, <http://ddr-phy.org/>.
- *DDR PHY Interface DFI 4.0 Specification*, <http://ddr-phy.org/>.

Note

See the *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Release Note* for the actual versions of the specifications that Arm used when designing the device.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title *Arm CoreLink DMC-620 Dynamic Memory Controller Technical Reference Manual*.
- The number 100568_0100_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

————— **Note** —————

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Chapter 1

Introduction

This chapter describes the DMC-620.

It contains the following sections:

- *1.1 About the product* on page 1-12.
- *1.2 DMC-620 compliance* on page 1-13.
- *1.3 Features* on page 1-14.
- *1.4 Interfaces* on page 1-15.
- *1.5 Configurable options* on page 1-16.
- *1.6 Test features* on page 1-17.
- *1.7 Product documentation and design flow* on page 1-18.
- *1.8 Product revisions* on page 1-20.

1.1 About the product

About the product is a high-level overview of the DMC-620.

The DMC-620 is an Arm AMBA 5 CHI SoC peripheral, developed, tested, and licensed by Arm. It is a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol.

It supports the following memory devices:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

The following figure shows an example system:

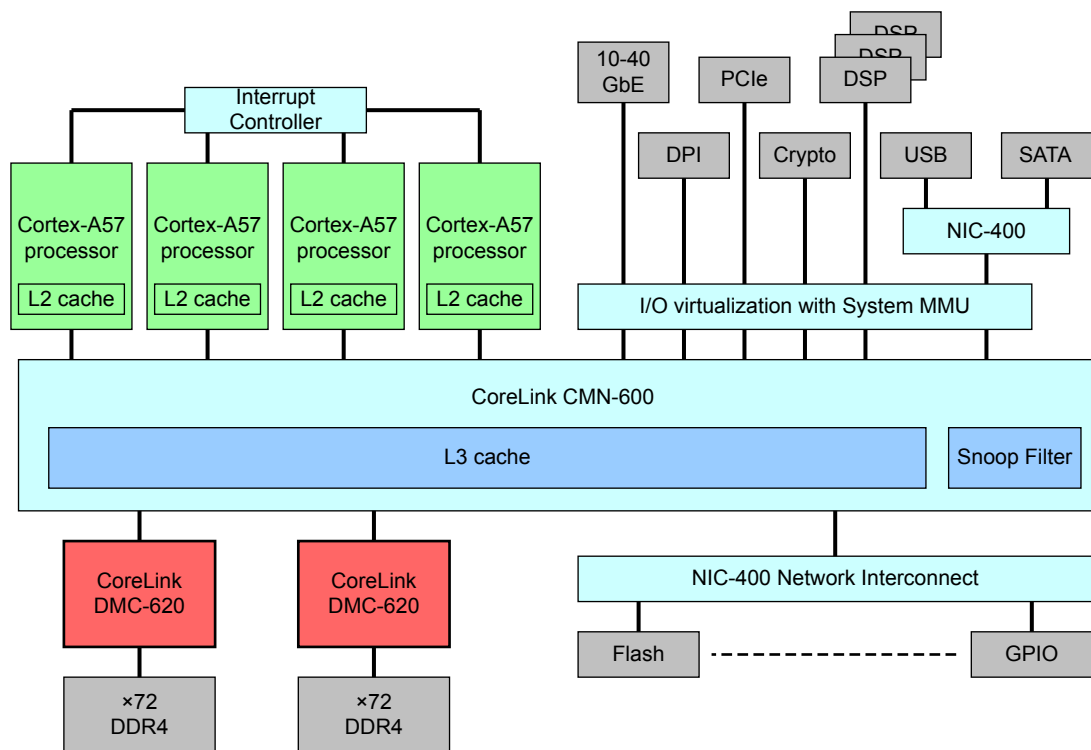


Figure 1-1 Example system

The DMC-620 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface, and to a processor through the programmers APB3 interface to program the DMC-620. It connects to the SDRAM devices through its memory interface block and the *DDR PHY Interface* (DFI).

1.2 DMC-620 compliance

The DMC-620 is compatible with the following protocol specifications and standards:

- AMBA 5 CHI-A/CHI-B/CHI-C protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR4 Data Buffer Specification.
- DDR4 RCD02 Specification.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- JEDEC JESD245 NVDIMM-N Byte Addressable Energy Backed Interface Specification.
- DFI 3.1.
- DFI 4.0.

1.3 Features

The DMC-620 supports DDR3 and DDR4 SDRAMs. It also supports error checking, reliability, availability, and serviceability features. In addition, *Quality of Service* (QoS) features and Arm TrustZone® architecture security extensions are built in throughout the controller.

The DMC-620 has the following features:

- Profiling signals that enable performance profiling to be performed in the system.
- TrustZone architecture security extensions.
- Buffering to optimize read and write turnaround, and to maximize bandwidth.
- A *System Interface* (SI) that provides:
 - A CHI interface to connect to a CoreLink *Cache Coherent Network* (CCN) or a CoreLink *Coherent Mesh Network* (CMN).
 - An AMBA5 CHI interface supporting the CHI-A, CHI-B, and CHI-C architecture.
 - An APB interface for configuration and initialization.
 - An external performance event interface for connecting to CoreSight™ on-chip debug and trace technology.
 - A 128-bit or 256-bit CHI interface.
- A *Memory Interface* (MI) that provides:
 - A DFI 3.1 and 4.0 interface to a PHY that supports DDR3, DDR3L, and DDR4.
 - Support for 1:2 DFI frequency ratio mode.
 - Support for either a 32-bit wide data SDRAM interface or a 64-bit wide data SDRAM interface.
- Low-power operation through programmable SDRAM power modes.
- ARMv8.2 compatible *Reliability, Availability, Serviceability* (RAS):
 - *Single Error Correcting, Double Error Detecting* (SECEDED) *Error-Correcting Code* (ECC) for off-chip DRAM.
 - Symbol-based ECC, to correct memory chip and data-lane failures.
 - SECEDED ECC for on-chip RAM protection.
 - Supports ARMv8.2 end-to-end RAS protection, data poisoning, and deferment.
 - Hardware *Read-Modify-Write* (RMW) for systems supporting sparse writes.
 - *Command-Address* (CA) parity checks for DDR3 and DDR4 link faults.
 - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling and automated recovery.
- *Power Control Logic* (PCL) that generates powerdown requests to the SDRAM, and manages power enables for the PHY logic.
- 3DS support for 8H, 4H, and 2H devices.
- DDR4 *Registered Dual In-line Memory Module* (RDIMM) and *Load-Reduced Dual In-line Memory Module* (LRDIMM) support.
- Flexible *Dual In-line Memory Module* (DIMM) topology support:
 - Signal multiplexing that allows a single board layout to support different RDIMM device types (3DS or planer), and a different number of devices.
 - Support for RDIMM Encoded or Direct CS.
- Core to DMC Prefetch Hint direct path allowing the core to directly initiate a DMC prefetch.
- Configurable out-of-order request queue depth and symbol ECC logic.

1.4 Interfaces

This section lists the interfaces in the DMC-620.

The DMC-620 has the following external interfaces:

- A System interface to provide read and write access to or from a master that supports either the CHI-A, CHI-B, or CHI-C protocol.
- An APB3 programmers interface to program and control the DMC-620.
- A DFI-compatible PHY interface to transfer data to and from the external memory.
- A Profile and Debug interface.
- A Low-power clock control interface that uses the Q-Channel protocol. See [Q-Channel interface on page 2-26](#).
- An Abort interface that is a four-phase request and acknowledge handshake. The Abort interface can be used to recover from a livelock when DRAM or PHY fails.
- User I/O ports.
- A set of interrupts that are used to report operational events and detected faults.

1.5 Configurable options

The DMC-620 has the following configurable options:

Table 1-1 Configurable options

Option	Parameter	Default	Default value	Description
CHI-A, CHI-B, or CHI-C	DMC_CHIB, DMC_CHIC	CHIC	1	Configures an AMBA 5 CHI Protocol Specification CHI Issue A, CHI Issue B, or CHI Issue C. ————— Note ————— For CHI-C, both parameters CHI-B and CHI-C must be 1. —————
128-bit or 256-bit CHI-B interface	DMC_SYS_DATA_WIDTH	128	256	Valid in CHI-B only. Configures a 128-bit or 256-bit CHI interface.
Include Symbol ECC	DMC_SYM_ECC	Yes	1	Includes logic for Symbol ECC. Symbol ECC is only supported with a x64 DRAM interface.
Queue depth	DMC_QUEUE_DEPTH	128	128	Can select a depth of 64 or 128.

————— **Note** —————

- If Symbol ECC is excluded from the configuration, you must ensure the `err0ctlr_ecc` field is never set to 2.
 - If the DMC is configured for a CHI-A interconnect, you must ensure the `err0ctlr_cpi` and `err0ctlr_cdi` fields are set to ignore the CHI-B *Data Byte Parity* (DBP) and poison bits.
-

1.6 Test features

The DMC-620 provides the following test features:

- Integration test logic for integration testing.
- A debug and profile interface to enable you to monitor transaction events.

1.7 Product documentation and design flow

This section describes the DMC-620 books and how they relate to the design flow.

Documentation

The DMC-620 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) summarizes the functionality of the DMC, and describes its signals.

The TRM is a non-confidential book available to the public.

Design Manual

The *Design Manual* (DM) describes the functionality and the effects of functional options on the behavior of the DMC. It is required at all stages of the design flow. The choices that are made in the design flow mean that some behavior that is described in the DM is not relevant. If you are programming the DMC, then contact:

- The implementer to determine what integration, if any, was performed before implementing the DMC.
- The integrator to determine the pin configuration of the device that you are using.

The DM is a confidential book that is only available to licensees.

Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes how to integrate the DMC into a SoC. The CIM includes a description of the signals that the integrator must tie off to connect the DMC into an SoC design or to other IP.

The CIM describes:

- How to synthesize the *Register Transfer Level* (RTL).
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The Arm product deliverables include reference scripts and information about using them to implement your design. Contact your EDA vendor for EDA tool support.

The CIM is a confidential book that is only available to licensees.

Design flow

The DMC-620 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer synthesizes the RTL to produce a hard macrocell. This stage includes integrating RAMs into the design.

Integration

The integrator connects the implemented design into a SoC. This stage includes connecting it to a memory system.

Programming

The system programmer develops the software that is required to initialize the DMC, and tests the required application software.

Each process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the DMC.

The operation of the final device depends on:

Configuration inputs

The integrator configures some features of the DMC by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software programming

The programmer configures the DMC by programming particular values into registers. This stage affects the behavior of the DMC.

Note

This manual refers to implementation-defined features. Reference to a feature that is included means that the appropriate signal configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

1.8 Product revisions

This section describes the differences in functionality between product revisions of the DMC-620.

r0p0

First release.

r0p0-r1p0

The functional changes are:

- Incorrect VREF DQ training behavior fixed.
- CHI-C support added.

Chapter 2

Functional description

This chapter describes how the DMC-620 operates.

It contains the following sections:

- [2.1 About the functions](#) on page 2-22.
- [2.2 Clocking and resets](#) on page 2-24.
- [2.3 Interfaces](#) on page 2-25.
- [2.4 Constraints and limitations of use](#) on page 2-28.

2.1 About the functions

This section gives a brief description of all the functions of the DMC-620.

The following figure shows a block diagram of the functions of the DMC-620. The colors show the different categories of functions:

- Blue indicates the blocks that are associated with data flow. The System interface is an example.
- Green indicates the blocks that are associated with programming. The Programming interface is an example.
- Orange indicates the blocks that are associated with the quality and efficiency of the communication to external memory. The QoS engine is an example.

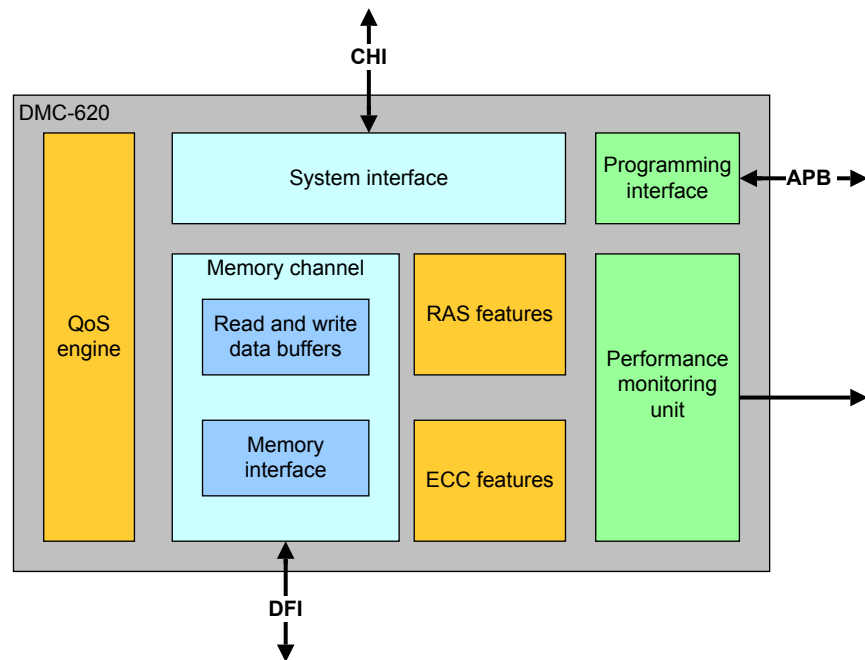


Figure 2-1 DMC functional block diagram

System Interface

The DMC-620 interfaces to the rest of the SoC through the System interface. This interface connects to a CHI *Slave Node* (SN-F) interface. For any attempted accesses that the system makes outside of the programmed address range, the System interface responds with a *Non-data Error* (NDERR) response. Depending on how you program the DMC-620, it converts the system access information to the correct rank, bank, column, and row access of the external SDRAM. The System interface supports TrustZone features to regulate Secure and Non-secure accesses to both Secure and Non-secure regions of memory.

The DMC monitors queue occupancies and dictates whether system requests of any given QoS are accepted. Prefetched and Dynamic P-Credit requests are allocated based on a threshold setting, which is derived from register settings.

Note

There is no support for exclusive access in the DMC because the CoreLink CCN-5xx and CMN-6xx products support exclusive access requests in the *Home Node* (HN-F).

Memory channel

Through this interface, the DMC-620 conducts data transactions with the SDRAM and regulates the power consumption of the SDRAM. The DMC-620 uses the ECC information that it receives from the SDRAM to maximize the reliability from these devices.

Programming interface

Through this interface, a master in the system programs the DMC-620. You can define the Secure and Non-secure regions of external memory. You can also define how the DMC-620 addresses the external memory from the address that the system provides on its System interface. You can also make direct accesses to the SDRAM, for example to initialize it.

QoS engine

The DMC-620 provides controls to enable you to adjust its arbitration scheme for your system to maximize the availability of your external memory devices. It provides buffers to reorder system transaction requests. It uses an advanced scheduling algorithm to ensure that traffic going to one memory bank causes minimal disruption to traffic going to a different memory bank. It also schedules transaction requests according to the availability of the destination memory bank. For system access requests to different available memory banks, the DMC-620 arbitrates these requests using the QoS priority initially, and then the temporal priority. The memory access requests all compete for control of the external SDRAM bus and SDRAM bank.

RAS

RAS features include support for the following:

- V8.2 RAS Extension compliant.
- Supports end-to-end RAS protection, data poisoning, and deferment.
- SECDED ECC and symbol-based ECC for external DRAM. The symbol-based ECC performs quad-symbol correct and multi-symbol detect.
- SECDED ECC of on-chip SRAM buffers within the DMC-620.
- An automated retry of failed read transactions.
- Write-back of corrected errors.
- To improve containment of faults, the DMC-620 supports:
 - Link error protection for the memory interface, including automated hardware recovery for system memory access, training, and other hardware operations.
 - Programmable data scrubbing. The DMC-620 periodically detects and corrects data errors in the memory autonomously.

2.2 Clocking and resets

The DMC-620 normally operates as one synchronous clock domain between the interconnect and the external DDR interface. However, the Programming interface can operate asynchronously to this.

This section shows the clock and reset signals that the DMC-620 requires.

Clocks

The DMC-620 has three clock inputs:

clk

clk is the main DMC clock that runs at SDRAM clock frequency. It must run synchronous to, and at the same frequency, as the CHI interconnect. If the CHI interconnect is not running at SDRAM clock frequency, then an asynchronous bridge such as the CCN *Device Source Synchronous Bridge* (DSSB) must be used.

clkdiv2

This clock runs the DFI interface and connects to both the DMC and the PHY. It must be edge synchronous to **clk**, and run at half the **clk** frequency.

pclk

pclk can run asynchronously to **clk** and **clkdiv2**.

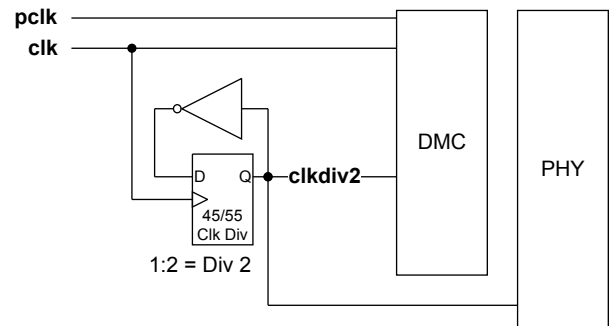


Figure 2-2 SoC hierarchy

Reset

Resets must be applied for a minimum duration of 16 clock cycles for each clock domain.

There are two reset inputs. **RESETn** resets both **clk** and the **clkdiv2** registers and **PRESETn** resets the **pclk** registers. The **pclk** domain must be out of reset before the **clk** and **clkdiv2** domains.

Note

- To assert any DMC-620 reset signal, you must set it LOW.
- To perform a DMC-620 reset, you must assert both reset signals.

2.3 Interfaces

This section describes the interfaces of the DMC-620, as the following figure shows.

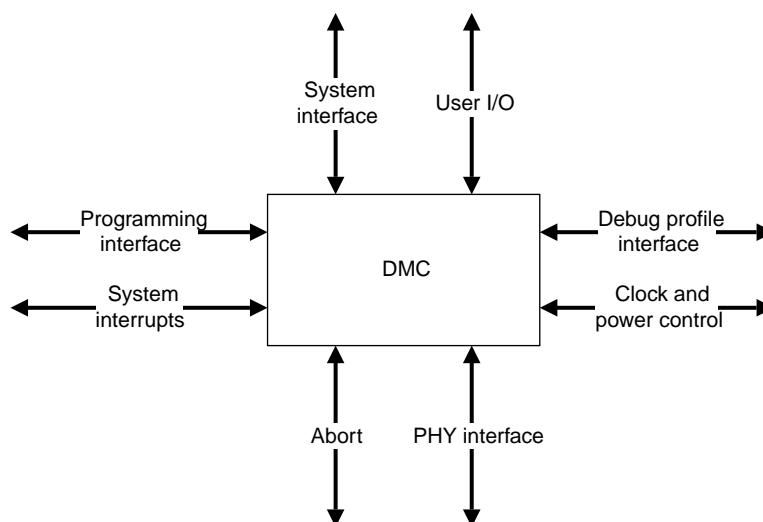


Figure 2-3 Interfaces of the DMC-620

This section contains the following subsections:

- [2.3.1 System interface on page 2-25.](#)
- [2.3.2 Programming interface on page 2-25.](#)
- [2.3.3 PHY interface on page 2-25.](#)
- [2.3.4 Low-power clock control interface on page 2-26.](#)
- [2.3.5 Abort interface on page 2-26.](#)

2.3.1 System interface

This section describes the function of the System interface.

The System interface provides protocol conversion between CHI and internal read/write requests. Because CHI is packet-based, and a slave node only supports read and write semantics, this translation is straightforward at a transaction level because no transformation function is performed.

2.3.2 Programming interface

This section describes the APB3 interface, which is used for programming the DMC-620.

The AMBA APB3 slave interface allows software to configure the controller and to initialize the memory devices. The APB3 programming interface also provides a means of performing architectural state transitions in addition to querying certain debug and profile information. The APB3 interface is a memory-mapped register interface.

2.3.3 PHY interface

The PHY interface provides command scheduling and arbitration, including the generation of any required SDRAM prepare commands, for example, **ACTIVATE** and **PRECHARGE**.

The PHY interface is compatible with the DDR standards for DDR4 and DDR3 (including DDR3L). It provides:

- Command scheduling and arbitration.
- Automated **AUTOREFRESH** command generation.
- SDRAM interface link protection including automated retries for failed commands to ensure the correct ordering of those retried commands to SDRAM.

- Automated SDRAM and PHY logic power control.
- Profile and debug information.
- Support for 1:2 frequency ratio mode.

2.3.4 Low-power clock control interface

This section describes the clock requirements for the DMC-620.

The DMC-620 provides a Low-power control interface using the Q-Channel protocol. The Low-power control interface is used to place the DMC into its low-power state, where the clock can be removed. The system can use the APB interface to put the DMC into its low-power state, and take it out of its low-power state.

Q-Channel interface

The DMC has a Q-Channel interface that allows an external power controller to place the DMC into a low-power state.

It is a standard Q-Channel interface as defined in the *AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces* using the following signals:

- **qactive**.
- **qreqn**.
- **qacceptn**.
- **qdeny**.

When the DMC receives a request, it puts the DRAM into self_refresh before asserting **qacceptn** to accept the request that indicates the **clk** can be stopped.

The DMC denies requests to power down using the Q-Channel when geardown_mode is enabled. In this case, low-power mode can still be entered using the APB interface.

There is a separate Q-Channel interface for the **pclk** using the following signals:

- **qactive_apb**.
- **qreqn_apb**.
- **qacceptn_apb**.
- **qdeny_apb**.

The DMC never denies a request to power down the APB clock although it might be delayed based on APB activity.

————— **Note** —————

These two interfaces are interrelated and a change on one can cause **qactive** on the other to be asserted. If this occurs, then the powerup request must be responded to in a timely fashion to allow the request to be serviced.

See the *AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces*.

2.3.5 Abort interface

When a fault is detected on the DFI interface, it causes repeated retries of commands on the memory interface. The Abort interface is a 4-phase request and acknowledge handshake. The DMC can use this interface to recover from a livelock that is caused by a DRAM failure or a PHY failure.

The following diagram shows the request, acknowledge handshake:

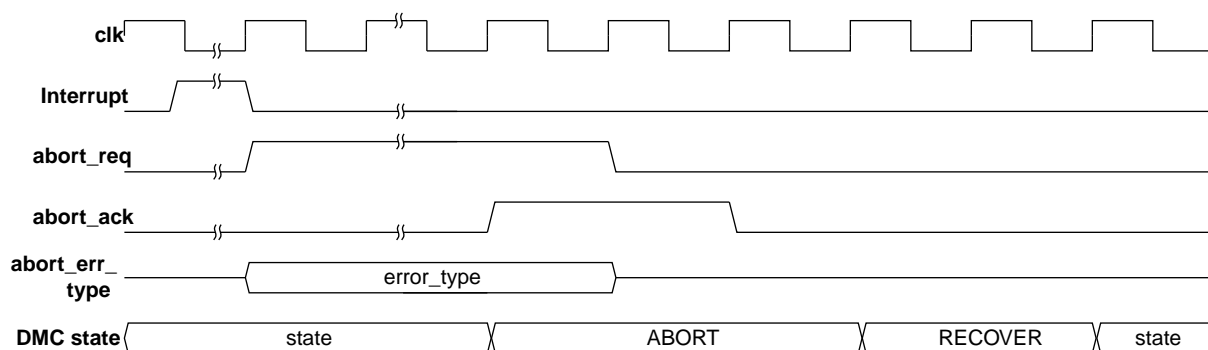


Figure 2-4 Abort interface timing diagram

The system can issue an abort at any time, which puts the DMC into the ABORT architectural state. Software must then restore the memory state. All current system transactions are retried after software restores the memory state and puts the DMC back into the READY state.

The Abort interface has the payload signal **abort_err_type** as an input to the DMC, which the DMC outputs as **dfi_disconnect_error** on the DFI interface during an abort sequence. Any PHY training that is in progress gets aborted and the DMC indicates to the PHY the error type through **dfi_disconnect_error**.

2.4 Constraints and limitations of use

The constraints and limitations of the DMC-620 depend on the SDRAMs used, and the interoperability within the PHYs. Which in turn, depends on the *DDR Physical Interface* (DFI) parameters.

The SDRAMs supported by the DMC-620 are:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

Note

These devices are described in the JEDEC specifications that are global standards for the microelectronics industry.

The DIMMs supported by the DMC-620 are:

- DDR3 UDIMM.
- DDR4 UDIMM.
- DDR4 RDIMM.
- DDR4 LRDIMM.
- DDR4 3DS. DIMMs utilizing 3DS parts are supported.

The JEDEC specification implies the following constraints and must be met:

1. $t_{xp} < t_{xsr}$ - Exiting power down timing must be less than self-refresh exit.
2. $t_{mrw_cs} < t_{mrw}$ - The delay after a Mode Register Write command and before any other command is issued to a different rank. This delay must be less than the delay applied after a Mode Register Write command and before any other command is issued to the same rank.

Chapter 3

Programmers model

This chapter describes the programmers model of the DMC-620.

It contains the following sections:

- [3.1 About this programmers model on page 3-30.](#)
- [3.2 Register descriptions on page 3-31.](#)
- [3.3 Register summary on page 3-32.](#)

3.1 About this programmers model

The following information applies to the dmc620 registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
 - Do not modify undefined register bits.
 - Ignore undefined register bits on reads.
 - All register bits are reset to the reset value specified in the [3.3 Register summary on page 3-32](#)
- Access type is described as follows:

RW Read and write.

RO Read only.

WO Write only.

3.2 Register descriptions

This section describes the dmc620 registers.

[3.3 Register summary on page 3-32](#) provides cross references to individual registers.

3.3 Register summary

The following table shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000	memc_status	RO	0x00000000	32	3.3.1 memc_status on page 3-51
0x004	memc_config	RO	0x00000000	32	3.3.2 memc_config on page 3-51
0x008	memc_cmd	WO	0x00000000	32	3.3.3 memc_cmd on page 3-52
0x010	address_control_next	RW	0x00030202	32	3.3.4 address_control_next on page 3-52
0x014	decode_control_next	RW	0x001A3000	32	3.3.5 decode_control_next on page 3-52
0x018	format_control	RW	0x1200113	32	3.3.6 format_control on page 3-53
0x01C	address_map_next	RW	0x00000000	32	3.3.7 address_map_next on page 3-53
0x020	low_power_control_next	RW	0x00000020	32	3.3.8 low_power_control_next on page 3-53
0x028	turnaround_control_next	RW	0x0F0F0F0F	32	3.3.9 turnaround_control_next on page 3-53
0x02C	hit_turnaround_control_next	RW	0x08909FBF	32	3.3.10 hit_turnaround_control_next on page 3-54
0x030	qos_class_control_next	RW	0x0000FC8	32	3.3.11 qos_class_control_next on page 3-54
0x034	escalation_control_next	RW	0x00080F03	32	3.3.12 escalation_control_next on page 3-54
0x038	qv_control_31_00_next	RW	0x76543210	32	3.3.13 qv_control_31_00_next on page 3-55
0x03C	qv_control_63_32_next	RW	0xFEDCBA98	32	3.3.14 qv_control_63_32_next on page 3-55
0x040	rt_control_31_00_next	RW	0x00000000	32	3.3.15 rt_control_31_00_next on page 3-55
0x044	rt_control_63_32_next	RW	0x00000000	32	3.3.16 rt_control_63_32_next on page 3-56
0x048	timeout_control_next	RW	0x00000001	32	3.3.17 timeout_control_next on page 3-56
0x04C	credit_control_next	RW	0x00000F03	32	3.3.18 credit_control_next on page 3-56
0x050	write_priority_control_31_00_next	RW	0x00000000	32	3.3.19 write_priority_control_31_00_next on page 3-56
0x054	write_priority_control_63_32_next	RW	0x00000000	32	3.3.20 write_priority_control_63_32_next on page 3-57
0x058	queue_threshold_control_31_00_next	RW	0x00000008	32	3.3.21 queue_threshold_control_31_00_next on page 3-57
0x05C	queue_threshold_control_63_32_next	RW	0x00000000	32	3.3.22 queue_threshold_control_63_32_next on page 3-57
0x060	address_shutter_31_00_next	RW	0x00000000	32	3.3.23 address_shutter_31_00_next on page 3-58
0x064	address_shutter_63_32_next	RW	0x00000000	32	3.3.24 address_shutter_63_32_next on page 3-58
0x068	address_shutter_95_64_next	RW	0x00000000	32	3.3.25 address_shutter_95_64_next on page 3-58
0x06C	address_shutter_127_96_next	RW	0x00000000	32	3.3.26 address_shutter_127_96_next on page 3-59
0x070	address_shutter_159_128_next	RW	0x00000000	32	3.3.27 address_shutter_159_128_next on page 3-59
0x074	address_shutter_191_160_next	RW	0x00000000	32	3.3.28 address_shutter_191_160_next on page 3-59

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x078	memory_address_max_31_00_next	RW	0x00000010	32	3.3.29 memory_address_max_31_00_next on page 3-59
0x07C	memory_address_max_47_32_next	RW	0x00000000	32	3.3.30 memory_address_max_47_32_next on page 3-60
0x080	access_address_min0_31_00_next	RW	0x00000000	32	3.3.31 access_address_min0_31_00_next on page 3-60
0x084	access_address_min0_47_32_next	RW	0x00000000	32	3.3.32 access_address_min0_47_32_next on page 3-60
0x088	access_address_max0_31_00_next	RW	0x00000000	32	3.3.33 access_address_max0_31_00_next on page 3-61
0x08C	access_address_max0_47_32_next	RW	0x00000000	32	3.3.34 access_address_max0_47_32_next on page 3-61
0x090	access_address_min1_31_00_next	RW	0x00000000	32	3.3.35 access_address_min1_31_00_next on page 3-61
0x094	access_address_min1_47_32_next	RW	0x00000000	32	3.3.36 access_address_min1_47_32_next on page 3-62
0x098	access_address_max1_31_00_next	RW	0x00000000	32	3.3.37 access_address_max1_31_00_next on page 3-62
0x09C	access_address_max1_47_32_next	RW	0x00000000	32	3.3.38 access_address_max1_47_32_next on page 3-62
0x0A0	access_address_min2_31_00_next	RW	0x00000000	32	3.3.39 access_address_min2_31_00_next on page 3-62
0x0A4	access_address_min2_47_32_next	RW	0x00000000	32	3.3.40 access_address_min2_47_32_next on page 3-63
0x0A8	access_address_max2_31_00_next	RW	0x00000000	32	3.3.41 access_address_max2_31_00_next on page 3-63
0x0AC	access_address_max2_47_32_next	RW	0x00000000	32	3.3.42 access_address_max2_47_32_next on page 3-63
0x0B0	access_address_min3_31_00_next	RW	0x00000000	32	3.3.43 access_address_min3_31_00_next on page 3-64
0x0B4	access_address_min3_47_32_next	RW	0x00000000	32	3.3.44 access_address_min3_47_32_next on page 3-64
0x0B8	access_address_max3_31_00_next	RW	0x00000000	32	3.3.45 access_address_max3_31_00_next on page 3-64
0x0BC	access_address_max3_47_32_next	RW	0x00000000	32	3.3.46 access_address_max3_47_32_next on page 3-65
0x0C0	access_address_min4_31_00_next	RW	0x00000000	32	3.3.47 access_address_min4_31_00_next on page 3-65
0x0C4	access_address_min4_47_32_next	RW	0x00000000	32	3.3.48 access_address_min4_47_32_next on page 3-65
0x0C8	access_address_max4_31_00_next	RW	0x00000000	32	3.3.49 access_address_max4_31_00_next on page 3-65

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0CC	access_address_max4_47_32_next	RW	0x00000000	32	3.3.50 access_address_max4_47_32_next on page 3-66
0x0D0	access_address_min5_31_00_next	RW	0x00000000	32	3.3.51 access_address_min5_31_00_next on page 3-66
0x0D4	access_address_min5_47_32_next	RW	0x00000000	32	3.3.52 access_address_min5_47_32_next on page 3-66
0x0D8	access_address_max5_31_00_next	RW	0x00000000	32	3.3.53 access_address_max5_31_00_next on page 3-67
0x0DC	access_address_max5_47_32_next	RW	0x00000000	32	3.3.54 access_address_max5_47_32_next on page 3-67
0x0E0	access_address_min6_31_00_next	RW	0x00000000	32	3.3.55 access_address_min6_31_00_next on page 3-67
0x0E4	access_address_min6_47_32_next	RW	0x00000000	32	3.3.56 access_address_min6_47_32_next on page 3-68
0x0E8	access_address_max6_31_00_next	RW	0x00000000	32	3.3.57 access_address_max6_31_00_next on page 3-68
0x0EC	access_address_max6_47_32_next	RW	0x00000000	32	3.3.58 access_address_max6_47_32_next on page 3-68
0x0F0	access_address_min7_31_00_next	RW	0x00000000	32	3.3.59 access_address_min7_31_00_next on page 3-68
0x0F4	access_address_min7_47_32_next	RW	0x00000000	32	3.3.60 access_address_min7_47_32_next on page 3-69
0x0F8	access_address_max7_31_00_next	RW	0x00000000	32	3.3.61 access_address_max7_31_00_next on page 3-69
0x0FC	access_address_max7_47_32_next	RW	0x00000000	32	3.3.62 access_address_max7_47_32_next on page 3-69
0x100	channel_status	RO	0x00000003	32	3.3.63 channel_status on page 3-70
0x104	channel_status_63_32	RO	0x00000000	32	3.3.64 channel_status_63_32 on page 3-70
0x108	direct_addr	RW	0x00000000	32	3.3.65 direct_addr on page 3-70
0x10C	direct_cmd	WO	0x00000000	32	3.3.66 direct_cmd on page 3-71
0x110	dci_replay_type_next	RW	0x00000002	32	3.3.67 dci_replay_type_next on page 3-71
0x114	direct_control_next	RW	0x0003FFFF	32	3.3.68 direct_control_next on page 3-71
0x118	dci_strb	RW	0x0000000F	32	3.3.69 dci_strb on page 3-72
0x11C	dci_data	RW	0x00000000	32	3.3.70 dci_data on page 3-72
0x120	refresh_control_next	RW	0x00000000	32	3.3.71 refresh_control_next on page 3-72
0x128	memory_type_next	RW	0x00000101	32	3.3.72 memory_type_next on page 3-73
0x130	feature_config	RW	0x000018E0	32	3.3.73 feature_config on page 3-73
0x138	nibble_failed_031_000	RW	0x00000000	32	3.3.74 nibble_failed_031_000 on page 3-73
0x13C	nibble_failed_063_032	RW	0x00000000	32	3.3.75 nibble_failed_063_032 on page 3-73

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x140	nibble_failed_095_064	RW	0x00000000	32	3.3.76 nibble_failed_095_064 on page 3-74
0x144	nibble_failed_127_096	RW	0x00000000	32	3.3.77 nibble_failed_127_096 on page 3-74
0x148	queue_allocate_control_031_000	RW	0xFFFFFFFF	32	3.3.78 queue_allocate_control_031_000 on page 3-74
0x14C	queue_allocate_control_063_032	RW	0xFFFFFFFF	32	3.3.79 queue_allocate_control_063_032 on page 3-75
0x150	queue_allocate_control_095_064	RW	0xFFFFFFFF	32	3.3.80 queue_allocate_control_095_064 on page 3-75
0x154	queue_allocate_control_127_096	RW	0xFFFFFFFF	32	3.3.81 queue_allocate_control_127_096 on page 3-75
0x16C	link_err_count	RW	0x00000000	32	3.3.82 link_err_count on page 3-76
0x170	scrub_control0_next	RW	0x0FFFFFF0	32	3.3.83 scrub_control0_next on page 3-76
0x174	scrub_address_min0_next	RW	0x00000000	32	3.3.84 scrub_address_min0_next on page 3-76
0x178	scrub_address_max0_next	RW	0x00000000	32	3.3.85 scrub_address_max0_next on page 3-77
0x17C	scrub_address_current0	RO	0x00000000	32	3.3.86 scrub_address_current0 on page 3-77
0x180	scrub_control1_next	RW	0x0FFFFFF0	32	3.3.87 scrub_control1_next on page 3-77
0x184	scrub_address_min1_next	RW	0x00000000	32	3.3.88 scrub_address_min1_next on page 3-77
0x188	scrub_address_max1_next	RW	0x00000000	32	3.3.89 scrub_address_max1_next on page 3-78
0x18C	scrub_address_current1	RO	0x00000000	32	3.3.90 scrub_address_current1 on page 3-78
0x1A0	cs_remap_control_31_00_next	RW	0x00020001	32	3.3.91 cs_remap_control_31_00_next on page 3-78
0x1A4	cs_remap_control_63_32_next	RW	0x00080004	32	3.3.92 cs_remap_control_63_32_next on page 3-79
0x1A8	cs_remap_control_95_64_next	RW	0x00200010	32	3.3.93 cs_remap_control_95_64_next on page 3-79
0x1AC	cs_remap_control_127_96_next	RW	0x00800040	32	3.3.94 cs_remap_control_127_96_next on page 3-79
0x1B0	cid_remap_control_31_00_next	RW	0x20001000	32	3.3.95 cid_remap_control_31_00_next on page 3-80
0x1B4	cid_remap_control_63_32_next	RW	0x00004000	32	3.3.96 cid_remap_control_63_32_next on page 3-80
0x1C0	cke_remap_control_next	RW	0x76543210	32	3.3.97 cke_remap_control_next on page 3-80
0x1C4	rst_remap_control_next	RW	0x76543210	32	3.3.98 rst_remap_control_next on page 3-80
0x1C8	ck_remap_control_next	RW	0x76543210	32	3.3.99 ck_remap_control_next on page 3-81
0x1D0	power_group_control_31_00_next	RW	0x00020001	32	3.3.100 power_group_control_31_00_next on page 3-81
0x1D4	power_group_control_63_32_next	RW	0x00080004	32	3.3.101 power_group_control_63_32_next on page 3-81
0x1D8	power_group_control_95_64_next	RW	0x00200010	32	3.3.102 power_group_control_95_64_next on page 3-82
0x1DC	power_group_control_127_96_next	RW	0x00800040	32	3.3.103 power_group_control_127_96_next on page 3-82
0x1E0	phy_rdwrdata_cs_mask_31_00	RW	0xF7FBDFDE	32	3.3.104 phy_rdwrdata_cs_mask_31_00 on page 3-82
0x1E4	phy_rdwrdata_cs_mask_63_32	RW	0xF7FBDFEF	32	3.3.105 phy_rdwrdata_cs_mask_63_32 on page 3-83
0x1E8	phy_request_cs_remap	RW	0x76543210	32	3.3.106 phy_request_cs_remap on page 3-83
0x1F0	feature_control_next	RW	0x0AA00000	32	3.3.107 feature_control_next on page 3-83

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1F4	<code>mux_control_next</code>	RW	0x00000000	32	3.3.108 mux_control_next on page 3-84
0x1F8	<code>rank_remap_control_next</code>	RW	0x76543210	32	3.3.109 rank_remap_control_next on page 3-84
0x200	<code>t_refi_next</code>	RW	0x00090100	32	3.3.110 t_refi_next on page 3-84
0x204	<code>t_rfc_next</code>	RW	0x00008C23	32	3.3.111 t_rfc_next on page 3-84
0x208	<code>t_mrr_next</code>	RW	0x00000002	32	3.3.112 t_mrr_next on page 3-85
0x20C	<code>t_mrwl_next</code>	RW	0x0000000C	32	3.3.113 t_mrwl_next on page 3-85
0x210	<code>refresh_enable_next</code>	RW	0x00000001	32	3.3.114 refresh_enable_next on page 3-85
0x218	<code>t_rcd_next</code>	RW	0x00000005	32	3.3.115 t_rcd_next on page 3-86
0x21C	<code>t_ras_next</code>	RW	0x0000000E	32	3.3.116 t_ras_next on page 3-86
0x220	<code>t_rp_next</code>	RW	0x00000005	32	3.3.117 t_rp_next on page 3-86
0x224	<code>t_rpall_next</code>	RW	0x00000005	32	3.3.118 t_rpall_next on page 3-87
0x228	<code>t_rrd_next</code>	RW	0x04000404	32	3.3.119 t_rrd_next on page 3-87
0x22C	<code>t_act_window_next</code>	RW	0x03561414	32	3.3.120 t_act_window_next on page 3-87
0x234	<code>t_rtr_next</code>	RW	0x10060404	32	3.3.121 t_rtr_next on page 3-88
0x238	<code>t_rtw_next</code>	RW	0x00060606	32	3.3.122 t_rtw_next on page 3-88
0x23C	<code>t_rtp_next</code>	RW	0x00000004	32	3.3.123 t_rtp_next on page 3-88
0x244	<code>t_wr_next</code>	RW	0x00000005	32	3.3.124 t_wr_next on page 3-89
0x248	<code>t_wtr_next</code>	RW	0x00040505	32	3.3.125 t_wtr_next on page 3-89
0x24C	<code>t_wtw_next</code>	RW	0x10060404	32	3.3.126 t_wtw_next on page 3-89
0x250	<code>t_clock_control_next</code>	RW	0x00000505	32	3.3.127 t_clock_control_next on page 3-90
0x254	<code>t_xmpd_next</code>	RW	0x000003FF	32	3.3.128 t_xmpd_next on page 3-90
0x258	<code>t_ep_next</code>	RW	0x00000002	32	3.3.129 t_ep_next on page 3-90
0x25C	<code>t_xp_next</code>	RW	0x00060002	32	3.3.130 t_xp_next on page 3-91
0x260	<code>t_esr_next</code>	RW	0x0000000E	32	3.3.131 t_esr_next on page 3-91
0x264	<code>t_xsr_next</code>	RW	0x05120100	32	3.3.132 t_xsr_next on page 3-91
0x268	<code>t_esrck_next</code>	RW	0x00000005	32	3.3.133 t_esrck_next on page 3-92
0x26C	<code>t_ckxsr_next</code>	RW	0x00000001	32	3.3.134 t_ckxsr_next on page 3-92
0x270	<code>t_cmd_next</code>	RW	0x00000000	32	3.3.135 t_cmd_next on page 3-92
0x274	<code>t_parity_next</code>	RW	0x00000900	32	3.3.136 t_parity_next on page 3-93
0x278	<code>t_zqcs_next</code>	RW	0x00000040	32	3.3.137 t_zqcs_next on page 3-93
0x27C	<code>t_rw_odt_clr_next</code>	RW	0x00000000	32	3.3.138 t_rw_odt_clr_next on page 3-93
0x300	<code>t_rddata_en_next</code>	RW	0x00000001	32	3.3.139 t_rddata_en_next on page 3-94
0x304	<code>t_phyrdlat_next</code>	RW	0x00000000	32	3.3.140 t_phyrdlat_next on page 3-94
0x308	<code>t_phywrlat_next</code>	RW	0x00000001	32	3.3.141 t_phywrlat_next on page 3-94
0x310	<code>rdlwl_control_next</code>	RW	0x00001080	32	3.3.142 rdlwl_control_next on page 3-95

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x314	rdlvl_mrs_next	RW	0x00000004	32	3.3.143 rdlvl_mrs_next on page 3-95
0x318	t_rdlvl_en_next	RW	0x00000000	32	3.3.144 t_rdlvl_en_next on page 3-95
0x31C	t_rdlvl_rr_next	RW	0x00000000	32	3.3.145 t_rdlvl_rr_next on page 3-96
0x320	wrlvl_control_next	RW	0x00101000	32	3.3.146 wrlvl_control_next on page 3-96
0x324	wrlvl_mrs_next	RW	0x00000086	32	3.3.147 wrlvl_mrs_next on page 3-96
0x328	t_wrlvl_en_next	RW	0x00000000	32	3.3.148 t_wrlvl_en_next on page 3-97
0x32C	t_wrlvl_ww_next	RW	0x00000000	32	3.3.149 t_wrlvl_ww_next on page 3-97
0x334	training_wrlvl_slice_status	RO	0x00000000	32	3.3.150 training_wrlvl_slice_status on page 3-97
0x338	training_rdlvl_slice_status	RO	0x00000000	32	3.3.151 training_rdlvl_slice_status on page 3-98
0x33C	training_rdlvl_gate_slice_status	RO	0x00000000	32	3.3.152 training_rdlvl_gate_slice_status on page 3-98
0x340	training_wdqlvl_slice_status	RO	0x00000000	32	3.3.153 training_wdqlvl_slice_status on page 3-98
0x344	training_wdqlvl_slice_result	RO	0x00000000	32	3.3.154 training_wdqlvl_slice_result on page 3-98
0x348	phy_power_control_next	RW	0x00000000	32	3.3.155 phy_power_control_next on page 3-99
0x34C	t_lpresp_next	RW	0x00000000	32	3.3.156 t_lpresp_next on page 3-99
0x350	phy_update_control_next	RW	0x2FE00000	32	3.3.157 phy_update_control_next on page 3-99
0x354	t_odth_next	RW	0x00000006	32	3.3.158 t_odth_next on page 3-100
0x358	odt_timing_next	RW	0x06000600	32	3.3.159 odt_timing_next on page 3-100
0x360	odt_wr_control_31_00_next	RW	0x08040201	32	3.3.160 odt_wr_control_31_00_next on page 3-100
0x364	odt_wr_control_63_32_next	RW	0x80402010	32	3.3.161 odt_wr_control_63_32_next on page 3-101
0x368	odt_rd_control_31_00_next	RW	0x00000000	32	3.3.162 odt_rd_control_31_00_next on page 3-101
0x36C	odt_rd_control_63_32_next	RW	0x00000000	32	3.3.163 odt_rd_control_63_32_next on page 3-101
0x370	temperature_readout	RO	0x00000000	32	3.3.164 temperature_readout on page 3-101
0x378	training_status	RO	0x00000000	32	3.3.165 training_status on page 3-102
0x37C	training_status_63_32	RO	0x00000000	32	3.3.166 training_status_63_32 on page 3-102
0x380	dq_map_control_15_00_next	RW	0x00000000	32	3.3.167 dq_map_control_15_00_next on page 3-102
0x384	dq_map_control_31_16_next	RW	0x00000000	32	3.3.168 dq_map_control_31_16_next on page 3-103
0x388	dq_map_control_47_32_next	RW	0x00000000	32	3.3.169 dq_map_control_47_32_next on page 3-103
0x38C	dq_map_control_63_48_next	RW	0x00000000	32	3.3.170 dq_map_control_63_48_next on page 3-103
0x390	dq_map_control_71_64_next	RW	0x00000000	32	3.3.171 dq_map_control_71_64_next on page 3-104
0x398	rank_status	RO	0x00000000	32	3.3.172 rank_status on page 3-104
0x39C	mode_change_status	RO	0x00000000	32	3.3.173 mode_change_status on page 3-104
0x3B0	odt_cp_control_31_00_next	RW	0x08040201	32	3.3.174 odt_cp_control_31_00_next on page 3-105
0x3B4	odt_cp_control_63_32_next	RW	0x80402010	32	3.3.175 odt_cp_control_63_32_next on page 3-105
0x400	user_status	RO	0x00000000	32	3.3.176 user_status on page 3-105
0x408	user_config0_next	RW	0x00000000	32	3.3.177 user_config0_next on page 3-106

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x40C	user_config1_next	RW	0x00000000	32	3.3.178 user_config1_next on page 3-106
0x410	user_config2	RW	0x00000000	32	3.3.179 user_config2 on page 3-106
0x414	user_config3	RW	0x00000000	32	3.3.180 user_config3 on page 3-107
0x500	interrupt_control	RW	0x00000000	32	3.3.181 interrupt_control on page 3-107
0x508	interrupt_clr	WO	0x00000000	32	3.3.182 interrupt_clr on page 3-107
0x510	interrupt_status	RO	0x00000000	32	3.3.183 interrupt_status on page 3-107
0x538	failed_access_int_info_31_00	RO	0x00000000	32	3.3.184 failed_access_int_info_31_00 on page 3-108
0x53C	failed_access_int_info_63_32	RO	0x00000000	32	3.3.185 failed_access_int_info_63_32 on page 3-108
0x540	failed_prog_int_info_31_00	RO	0x00000000	32	3.3.186 failed_prog_int_info_31_00 on page 3-108
0x544	failed_prog_int_info_63_32	RO	0x00000000	32	3.3.187 failed_prog_int_info_63_32 on page 3-109
0x548	link_err_int_info_31_00	RO	0x00000000	32	3.3.188 link_err_int_info_31_00 on page 3-109
0x54C	link_err_int_info_63_32	RO	0x00000000	32	3.3.189 link_err_int_info_63_32 on page 3-109
0x550	arch_fsm_int_info_31_00	RO	0x00000000	32	3.3.190 arch_fsm_int_info_31_00 on page 3-110
0x554	arch_fsm_int_info_63_32	RO	0x00000000	32	3.3.191 arch_fsm_int_info_63_32 on page 3-110
0x610	t_db_train_resp_next	RW	0x00000000	32	3.3.192 t_db_train_resp_next on page 3-110
0x614	t_lvl_disconnect_next	RW	0x0000000F	32	3.3.193 t_lvl_disconnect_next on page 3-111
0x620	wdqlvl_control_next	RW	0x00000094	32	3.3.194 wdqlvl_control_next on page 3-111
0x624	wdqlvl_vrefdq_train_mrs_next	RW	0x00000000	32	3.3.195 wdqlvl_vrefdq_train_mrs_next on page 3-111
0x628	wdqlvl_address_31_00_next	RW	0x00000000	32	3.3.196 wdqlvl_address_31_00_next on page 3-112
0x62C	wdqlvl_address_63_32_next	RW	0x00000000	32	3.3.197 wdqlvl_address_63_32_next on page 3-112
0x630	t_wdqlvl_en_next	RW	0x00000000	32	3.3.198 t_wdqlvl_en_next on page 3-112
0x634	t_wdqlvl_ww_next	RW	0x00000000	32	3.3.199 t_wdqlvl_ww_next on page 3-113
0x638	t_wdqlvl_rw_next	RW	0x00000000	32	3.3.200 t_wdqlvl_rw_next on page 3-113
0x63C	training_wdqlvl_slice_resp	RO	0x00000000	32	3.3.201 training_wdqlvl_slice_resp on page 3-113
0x640	training_rdlvl_slice_resp	RO	0x00000000	32	3.3.202 training_rdlvl_slice_resp on page 3-114
0x654	phymstr_control_next	RW	0x00000000	32	3.3.203 phymstr_control_next on page 3-114
0x700	err0fr	RO	0x000009AA	32	3.3.204 err0fr on page 3-114
0x708	err0ctrl0	RW	0x00000010	32	3.3.205 err0ctrl0 on page 3-115
0x70C	err0ctrl1	RW	0x000000C0	32	3.3.206 err0ctrl1 on page 3-115
0x710	err0status	RO	0x00000000	32	3.3.207 err0status on page 3-115
0x740	err1fr	RO	0x000009AA	32	3.3.208 err1fr on page 3-116
0x748	err1ctrl	RO	0x00000000	32	3.3.209 err1ctrl on page 3-116
0x750	err1status	RW	0x00000000	32	3.3.210 err1status on page 3-116
0x758	err1addr0	RW	0x00000000	32	3.3.211 err1addr0 on page 3-116
0x75C	err1addr1	RW	0x00000000	32	3.3.212 err1addr1 on page 3-117

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x760	err1misc0	RW	0x00000000	32	3.3.213 err1misc0 on page 3-117
0x764	err1misc1	RW	0x00000000	32	3.3.214 err1misc1 on page 3-117
0x768	err1misc2	RW	0x00000000	32	3.3.215 err1misc2 on page 3-118
0x76C	err1misc3	RW	0x00000000	32	3.3.216 err1misc3 on page 3-118
0x770	err1misc4	RW	0x00000000	32	3.3.217 err1misc4 on page 3-118
0x774	err1misc5	RW	0x00000000	32	3.3.218 err1misc5 on page 3-119
0x780	err2fr	RO	0x000009AA	32	3.3.219 err2fr on page 3-119
0x788	err2ctrl	RO	0x00000000	32	3.3.220 err2ctrl on page 3-119
0x790	err2status	RW	0x00000000	32	3.3.221 err2status on page 3-120
0x798	err2addr0	RW	0x00000000	32	3.3.222 err2addr0 on page 3-120
0x79C	err2addr1	RW	0x00000000	32	3.3.223 err2addr1 on page 3-120
0x7A0	err2misc0	RW	0x00000000	32	3.3.224 err2misc0 on page 3-121
0x7A4	err2misc1	RW	0x00000000	32	3.3.225 err2misc1 on page 3-121
0x7A8	err2misc2	RW	0x00000000	32	3.3.226 err2misc2 on page 3-121
0x7AC	err2misc3	RW	0x00000000	32	3.3.227 err2misc3 on page 3-121
0x7B0	err2misc4	RW	0x00000000	32	3.3.228 err2misc4 on page 3-122
0x7B4	err2misc5	RW	0x00000000	32	3.3.229 err2misc5 on page 3-122
0x7C0	err3fr	RO	0x000009AA	32	3.3.230 err3fr on page 3-122
0x7C8	err3ctrl	RO	0x00000000	32	3.3.231 err3ctrl on page 3-123
0x7D0	err3status	RW	0x00000000	32	3.3.232 err3status on page 3-123
0x7D8	err3addr0	RW	0x00000000	32	3.3.233 err3addr0 on page 3-123
0x7DC	err3addr1	RW	0x00000000	32	3.3.234 err3addr1 on page 3-124
0x7E0	err3misc0	RO	0x00000000	32	3.3.235 err3misc0 on page 3-124
0x7E4	err3misc1	RO	0x00000000	32	3.3.236 err3misc1 on page 3-124
0x800	err4fr	RO	0x000009AA	32	3.3.237 err4fr on page 3-125
0x808	err4ctrl	RO	0x00000000	32	3.3.238 err4ctrl on page 3-125
0x810	err4status	RW	0x00000000	32	3.3.239 err4status on page 3-125
0x818	err4addr0	RW	0x00000000	32	3.3.240 err4addr0 on page 3-126
0x81C	err4addr1	RW	0x00000000	32	3.3.241 err4addr1 on page 3-126
0x820	err4misc0	RW	0x00000000	32	3.3.242 err4misc0 on page 3-126
0x824	err4misc1	RW	0x00000000	32	3.3.243 err4misc1 on page 3-127
0x828	err4misc2	RW	0x00000000	32	3.3.244 err4misc2 on page 3-127
0x840	err5fr	RO	0x000009AA	32	3.3.245 err5fr on page 3-127
0x848	err5ctrl	RO	0x00000000	32	3.3.246 err5ctrl on page 3-128
0x850	err5status	RW	0x00000000	32	3.3.247 err5status on page 3-128

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x858	err5addr0	RW	0x00000000	32	3.3.248 err5addr0 on page 3-128
0x85C	err5addr1	RW	0x00000000	32	3.3.249 err5addr1 on page 3-129
0x860	err5misc0	RW	0x00000000	32	3.3.250 err5misc0 on page 3-129
0x864	err5misc1	RW	0x00000000	32	3.3.251 err5misc1 on page 3-129
0x868	err5misc2	RW	0x00000000	32	3.3.252 err5misc2 on page 3-129
0x880	err6fr	RO	0x000009AA	32	3.3.253 err6fr on page 3-130
0x888	err6ctlr	RO	0x00000000	32	3.3.254 err6ctlr on page 3-130
0x890	err6status	RW	0x00000000	32	3.3.255 err6status on page 3-130
0x898	err6addr0	RW	0x00000000	32	3.3.256 err6addr0 on page 3-131
0x89C	err6addr1	RW	0x00000000	32	3.3.257 err6addr1 on page 3-131
0x8A0	err6misc0	RW	0x00000000	32	3.3.258 err6misc0 on page 3-131
0x8A4	err6misc1	RW	0x00000000	32	3.3.259 err6misc1 on page 3-132
0x920	errgsr	RW	0x00000000	32	3.3.260 errgsr on page 3-132
0xA00	pmu_snapshot_req	WO	0x00000000	32	3.3.261 pmu_snapshot_req on page 3-132
0xA04	pmu_snapshot_ack	RO	0x00000000	32	3.3.262 pmu_snapshot_ack on page 3-133
0xA08	pmu_overflow_status_clkdiv2	RW	0x00000000	32	3.3.263 pmu_overflow_status_clkdiv2 on page 3-133
0xA0C	pmu_overflow_status_clk	RW	0x00000000	32	3.3.264 pmu_overflow_status_clk on page 3-133
0xA10	pmu_clkdiv2_counter_0_mask_31_00	RW	0x00000000	32	3.3.265 pmu_clkdiv2_counter_0_mask_31_00 on page 3-133
0xA14	pmu_clkdiv2_counter_0_mask_63_32	RW	0x00000000	32	3.3.266 pmu_clkdiv2_counter_0_mask_63_32 on page 3-134
0xA18	pmu_clkdiv2_counter_0_match_31_00	RW	0x00000000	32	3.3.267 pmu_clkdiv2_counter_0_match_31_00 on page 3-134
0xA1C	pmu_clkdiv2_counter_0_match_63_32	RW	0x00000000	32	3.3.268 pmu_clkdiv2_counter_0_match_63_32 on page 3-134
0xA20	pmu_clkdiv2_counter_0_control	RW	0x00000000	32	3.3.269 pmu_clkdiv2_counter_0_control on page 3-135
0xA28	pmu_clkdiv2_counter_0_snapshot_value_31_00	RO	0x00000000	32	3.3.270 pmu_clkdiv2_counter_0_snapshot_value_31_00 on page 3-135
0xA30	pmu_clkdiv2_counter_0_value_31_00	RW	0x00000000	32	3.3.271 pmu_clkdiv2_counter_0_value_31_00 on page 3-135
0xA38	pmu_clkdiv2_counter_1_mask_31_00	RW	0x00000000	32	3.3.272 pmu_clkdiv2_counter_1_mask_31_00 on page 3-136
0xA3C	pmu_clkdiv2_counter_1_mask_63_32	RW	0x00000000	32	3.3.273 pmu_clkdiv2_counter_1_mask_63_32 on page 3-136
0xA40	pmu_clkdiv2_counter_1_match_31_00	RW	0x00000000	32	3.3.274 pmu_clkdiv2_counter_1_match_31_00 on page 3-136
0xA44	pmu_clkdiv2_counter_1_match_63_32	RW	0x00000000	32	3.3.275 pmu_clkdiv2_counter_1_match_63_32 on page 3-136

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0xA48	pmu_clkdiv2_counter_1_control	RW	0x00000000	32	3.3.276 <i>pmu_clkdiv2_counter_1_control</i> on page 3-137
0xA50	pmu_clkdiv2_counter_1_snapshot_value_31_00	RO	0x00000000	32	3.3.277 <i>pmu_clkdiv2_counter_1_snapshot_value_31_00</i> on page 3-137
0xA58	pmu_clkdiv2_counter_1_value_31_00	RW	0x00000000	32	3.3.278 <i>pmu_clkdiv2_counter_1_value_31_00</i> on page 3-137
0xA60	pmu_clkdiv2_counter_2_mask_31_00	RW	0x00000000	32	3.3.279 <i>pmu_clkdiv2_counter_2_mask_31_00</i> on page 3-138
0xA64	pmu_clkdiv2_counter_2_mask_63_32	RW	0x00000000	32	3.3.280 <i>pmu_clkdiv2_counter_2_mask_63_32</i> on page 3-138
0xA68	pmu_clkdiv2_counter_2_match_31_00	RW	0x00000000	32	3.3.281 <i>pmu_clkdiv2_counter_2_match_31_00</i> on page 3-138
0xA6C	pmu_clkdiv2_counter_2_match_63_32	RW	0x00000000	32	3.3.282 <i>pmu_clkdiv2_counter_2_match_63_32</i> on page 3-139
0xA70	pmu_clkdiv2_counter_2_control	RW	0x00000000	32	3.3.283 <i>pmu_clkdiv2_counter_2_control</i> on page 3-139
0xA78	pmu_clkdiv2_counter_2_snapshot_value_31_00	RO	0x00000000	32	3.3.284 <i>pmu_clkdiv2_counter_2_snapshot_value_31_00</i> on page 3-139
0xA80	pmu_clkdiv2_counter_2_value_31_00	RW	0x00000000	32	3.3.285 <i>pmu_clkdiv2_counter_2_value_31_00</i> on page 3-139
0xA88	pmu_clkdiv2_counter_3_mask_31_00	RW	0x00000000	32	3.3.286 <i>pmu_clkdiv2_counter_3_mask_31_00</i> on page 3-140
0xA8C	pmu_clkdiv2_counter_3_mask_63_32	RW	0x00000000	32	3.3.287 <i>pmu_clkdiv2_counter_3_mask_63_32</i> on page 3-140
0xA90	pmu_clkdiv2_counter_3_match_31_00	RW	0x00000000	32	3.3.288 <i>pmu_clkdiv2_counter_3_match_31_00</i> on page 3-140
0xA94	pmu_clkdiv2_counter_3_match_63_32	RW	0x00000000	32	3.3.289 <i>pmu_clkdiv2_counter_3_match_63_32</i> on page 3-141
0xA98	pmu_clkdiv2_counter_3_control	RW	0x00000000	32	3.3.290 <i>pmu_clkdiv2_counter_3_control</i> on page 3-141
0xAA0	pmu_clkdiv2_counter_3_snapshot_value_31_00	RO	0x00000000	32	3.3.291 <i>pmu_clkdiv2_counter_3_snapshot_value_31_00</i> on page 3-141
0xAA8	pmu_clkdiv2_counter_3_value_31_00	RW	0x00000000	32	3.3.292 <i>pmu_clkdiv2_counter_3_value_31_00</i> on page 3-142
0xAB0	pmu_clkdiv2_counter_4_mask_31_00	RW	0x00000000	32	3.3.293 <i>pmu_clkdiv2_counter_4_mask_31_00</i> on page 3-142
0xAB4	pmu_clkdiv2_counter_4_mask_63_32	RW	0x00000000	32	3.3.294 <i>pmu_clkdiv2_counter_4_mask_63_32</i> on page 3-142
0xAB8	pmu_clkdiv2_counter_4_match_31_00	RW	0x00000000	32	3.3.295 <i>pmu_clkdiv2_counter_4_match_31_00</i> on page 3-142
0xABC	pmu_clkdiv2_counter_4_match_63_32	RW	0x00000000	32	3.3.296 <i>pmu_clkdiv2_counter_4_match_63_32</i> on page 3-143
0xAC0	pmu_clkdiv2_counter_4_control	RW	0x00000000	32	3.3.297 <i>pmu_clkdiv2_counter_4_control</i> on page 3-143

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0xAC8	pmu_clkdiv2_counter_4_snapshot_value_31_00	RO	0x00000000	32	3.3.298 <i>pmu_clkdiv2_counter_4_snapshot_value_31_00</i> on page 3-143
0xAD0	pmu_clkdiv2_counter_4_value_31_00	RW	0x00000000	32	3.3.299 <i>pmu_clkdiv2_counter_4_value_31_00</i> on page 3-144
0xAD8	pmu_clkdiv2_counter_5_mask_31_00	RW	0x00000000	32	3.3.300 <i>pmu_clkdiv2_counter_5_mask_31_00</i> on page 3-144
0xADC	pmu_clkdiv2_counter_5_mask_63_32	RW	0x00000000	32	3.3.301 <i>pmu_clkdiv2_counter_5_mask_63_32</i> on page 3-144
0xAE0	pmu_clkdiv2_counter_5_match_31_00	RW	0x00000000	32	3.3.302 <i>pmu_clkdiv2_counter_5_match_31_00</i> on page 3-145
0xAE4	pmu_clkdiv2_counter_5_match_63_32	RW	0x00000000	32	3.3.303 <i>pmu_clkdiv2_counter_5_match_63_32</i> on page 3-145
0xAE8	pmu_clkdiv2_counter_5_control	RW	0x00000000	32	3.3.304 <i>pmu_clkdiv2_counter_5_control</i> on page 3-145
0xAF0	pmu_clkdiv2_counter_5_snapshot_value_31_00	RO	0x00000000	32	3.3.305 <i>pmu_clkdiv2_counter_5_snapshot_value_31_00</i> on page 3-145
0xAF8	pmu_clkdiv2_counter_5_value_31_00	RW	0x00000000	32	3.3.306 <i>pmu_clkdiv2_counter_5_value_31_00</i> on page 3-146
0xB00	pmu_clkdiv2_counter_6_mask_31_00	RW	0x00000000	32	3.3.307 <i>pmu_clkdiv2_counter_6_mask_31_00</i> on page 3-146
0xB04	pmu_clkdiv2_counter_6_mask_63_32	RW	0x00000000	32	3.3.308 <i>pmu_clkdiv2_counter_6_mask_63_32</i> on page 3-146
0xB08	pmu_clkdiv2_counter_6_match_31_00	RW	0x00000000	32	3.3.309 <i>pmu_clkdiv2_counter_6_match_31_00</i> on page 3-147
0xB0C	pmu_clkdiv2_counter_6_match_63_32	RW	0x00000000	32	3.3.310 <i>pmu_clkdiv2_counter_6_match_63_32</i> on page 3-147
0xB10	pmu_clkdiv2_counter_6_control	RW	0x00000000	32	3.3.311 <i>pmu_clkdiv2_counter_6_control</i> on page 3-147
0xB18	pmu_clkdiv2_counter_6_snapshot_value_31_00	RO	0x00000000	32	3.3.312 <i>pmu_clkdiv2_counter_6_snapshot_value_31_00</i> on page 3-148
0xB20	pmu_clkdiv2_counter_6_value_31_00	RW	0x00000000	32	3.3.313 <i>pmu_clkdiv2_counter_6_value_31_00</i> on page 3-148
0xB28	pmu_clkdiv2_counter_7_mask_31_00	RW	0x00000000	32	3.3.314 <i>pmu_clkdiv2_counter_7_mask_31_00</i> on page 3-148
0xB2C	pmu_clkdiv2_counter_7_mask_63_32	RW	0x00000000	32	3.3.315 <i>pmu_clkdiv2_counter_7_mask_63_32</i> on page 3-148
0xB30	pmu_clkdiv2_counter_7_match_31_00	RW	0x00000000	32	3.3.316 <i>pmu_clkdiv2_counter_7_match_31_00</i> on page 3-149
0xB34	pmu_clkdiv2_counter_7_match_63_32	RW	0x00000000	32	3.3.317 <i>pmu_clkdiv2_counter_7_match_63_32</i> on page 3-149
0xB38	pmu_clkdiv2_counter_7_control	RW	0x00000000	32	3.3.318 <i>pmu_clkdiv2_counter_7_control</i> on page 3-149
0xB40	pmu_clkdiv2_counter_7_snapshot_value_31_00	RO	0x00000000	32	3.3.319 <i>pmu_clkdiv2_counter_7_snapshot_value_31_00</i> on page 3-150

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0xB48	pmu_clkdiv2_counter_7_value_31_00	RW	0x00000000	32	3.3.320 pmu_clkdiv2_counter_7_value_31_00 on page 3-150
0xB50	pmu_clk_counter_0_mask_31_00	RW	0x00000000	32	3.3.321 pmu_clk_counter_0_mask_31_00 on page 3-150
0xB54	pmu_clk_counter_0_mask_63_32	RW	0x00000000	32	3.3.322 pmu_clk_counter_0_mask_63_32 on page 3-151
0xB58	pmu_clk_counter_0_match_31_00	RW	0x00000000	32	3.3.323 pmu_clk_counter_0_match_31_00 on page 3-151
0xB5C	pmu_clk_counter_0_match_63_32	RW	0x00000000	32	3.3.324 pmu_clk_counter_0_match_63_32 on page 3-151
0xB60	pmu_clk_counter_0_control	RW	0x00000000	32	3.3.325 pmu_clk_counter_0_control on page 3-151
0xB68	pmu_clk_counter_0_snapshot_value_31_00	RO	0x00000000	32	3.3.326 pmu_clk_counter_0_snapshot_value_31_00 on page 3-152
0xB70	pmu_clk_counter_0_value_31_00	RW	0x00000000	32	3.3.327 pmu_clk_counter_0_value_31_00 on page 3-152
0xB78	pmu_clk_counter_1_mask_31_00	RW	0x00000000	32	3.3.328 pmu_clk_counter_1_mask_31_00 on page 3-152
0xB7C	pmu_clk_counter_1_mask_63_32	RW	0x00000000	32	3.3.329 pmu_clk_counter_1_mask_63_32 on page 3-153
0xB80	pmu_clk_counter_1_match_31_00	RW	0x00000000	32	3.3.330 pmu_clk_counter_1_match_31_00 on page 3-153
0xB84	pmu_clk_counter_1_match_63_32	RW	0x00000000	32	3.3.331 pmu_clk_counter_1_match_63_32 on page 3-153
0xB88	pmu_clk_counter_1_control	RW	0x00000000	32	3.3.332 pmu_clk_counter_1_control on page 3-154
0xB90	pmu_clk_counter_1_snapshot_value_31_00	RO	0x00000000	32	3.3.333 pmu_clk_counter_1_snapshot_value_31_00 on page 3-154
0xB98	pmu_clk_counter_1_value_31_00	RW	0x00000000	32	3.3.334 pmu_clk_counter_1_value_31_00 on page 3-154
0xE00	integ_cfg	RW	0x00000000	32	3.3.335 integ_cfg on page 3-154
0xE08	integ_outputs	WO	0x00000000	32	3.3.336 integ_outputs on page 3-155
0x1010	address_control_now	RO	0x00030202	32	3.3.337 address_control_now on page 3-155
0x1014	decode_control_now	RO	0x001A3000	32	3.3.338 decode_control_now on page 3-155
0x101C	address_map_now	RO	0x00000000	32	3.3.339 address_map_now on page 3-156
0x1020	low_power_control_now	RO	0x00000020	32	3.3.340 low_power_control_now on page 3-156
0x1028	turnaround_control_now	RO	0x0F0F0F0F	32	3.3.341 turnaround_control_now on page 3-156

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x102 C	hit_turnaround_control_now	RO	0x08909FBF	32	3.3.342 hit_turnaround_control_now on page 3-157
0x103 0	qos_class_control_now	RO	0x00000FC8	32	3.3.343 qos_class_control_now on page 3-157
0x103 4	escalation_control_now	RO	0x00080F03	32	3.3.344 escalation_control_now on page 3-157
0x103 8	qv_control_31_00_now	RO	0x76543210	32	3.3.345 qv_control_31_00_now on page 3-158
0x103 C	qv_control_63_32_now	RO	0xFEDCBA98	32	3.3.346 qv_control_63_32_now on page 3-158
0x104 0	rt_control_31_00_now	RO	0x00000000	32	3.3.347 rt_control_31_00_now on page 3-158
0x104 4	rt_control_63_32_now	RO	0x00000000	32	3.3.348 rt_control_63_32_now on page 3-159
0x104 8	timeout_control_now	RO	0x00000001	32	3.3.349 timeout_control_now on page 3-159
0x104 C	credit_control_now	RO	0x00000F03	32	3.3.350 credit_control_now on page 3-159
0x105 0	write_priority_control_31_00_now	RO	0x00000000	32	3.3.351 write_priority_control_31_00_now on page 3-160
0x105 4	write_priority_control_63_32_now	RO	0x00000000	32	3.3.352 write_priority_control_63_32_now on page 3-160
0x105 8	queue_threshold_control_31_00_now	RO	0x00000008	32	3.3.353 queue_threshold_control_31_00_now on page 3-160
0x105 C	queue_threshold_control_63_32_now	RO	0x00000000	32	3.3.354 queue_threshold_control_63_32_now on page 3-161
0x106 0	address_shutter_31_00_now	RO	0x00000000	32	3.3.355 address_shutter_31_00_now on page 3-161
0x106 4	address_shutter_63_32_now	RO	0x00000000	32	3.3.356 address_shutter_63_32_now on page 3-161
0x106 8	address_shutter_95_64_now	RO	0x00000000	32	3.3.357 address_shutter_95_64_now on page 3-162
0x106 C	address_shutter_127_96_now	RO	0x00000000	32	3.3.358 address_shutter_127_96_now on page 3-162
0x107 0	address_shutter_159_128_now	RO	0x00000000	32	3.3.359 address_shutter_159_128_now on page 3-162
0x107 4	address_shutter_191_160_now	RO	0x00000000	32	3.3.360 address_shutter_191_160_now on page 3-163
0x107 8	memory_address_max_31_00_now	RO	0x00000010	32	3.3.361 memory_address_max_31_00_now on page 3-163
0x107 C	memory_address_max_47_32_now	RO	0x00000000	32	3.3.362 memory_address_max_47_32_now on page 3-163

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1080	access_address_min0_31_00_now	RO	0x00000000	32	3.3.363 access_address_min0_31_00_now on page 3-164
0x1084	access_address_min0_47_32_now	RO	0x00000000	32	3.3.364 access_address_min0_47_32_now on page 3-164
0x1088	access_address_max0_31_00_now	RO	0x00000000	32	3.3.365 access_address_max0_31_00_now on page 3-164
0x108C	access_address_max0_47_32_now	RO	0x00000000	32	3.3.366 access_address_max0_47_32_now on page 3-165
0x1090	access_address_min1_31_00_now	RO	0x00000000	32	3.3.367 access_address_min1_31_00_now on page 3-165
0x1094	access_address_min1_47_32_now	RO	0x00000000	32	3.3.368 access_address_min1_47_32_now on page 3-165
0x1098	access_address_max1_31_00_now	RO	0x00000000	32	3.3.369 access_address_max1_31_00_now on page 3-166
0x109C	access_address_max1_47_32_now	RO	0x00000000	32	3.3.370 access_address_max1_47_32_now on page 3-166
0x10A0	access_address_min2_31_00_now	RO	0x00000000	32	3.3.371 access_address_min2_31_00_now on page 3-166
0x10A4	access_address_min2_47_32_now	RO	0x00000000	32	3.3.372 access_address_min2_47_32_now on page 3-167
0x10A8	access_address_max2_31_00_now	RO	0x00000000	32	3.3.373 access_address_max2_31_00_now on page 3-167
0x10AC	access_address_max2_47_32_now	RO	0x00000000	32	3.3.374 access_address_max2_47_32_now on page 3-167
0x10B0	access_address_min3_31_00_now	RO	0x00000000	32	3.3.375 access_address_min3_31_00_now on page 3-168
0x10B4	access_address_min3_47_32_now	RO	0x00000000	32	3.3.376 access_address_min3_47_32_now on page 3-168
0x10B8	access_address_max3_31_00_now	RO	0x00000000	32	3.3.377 access_address_max3_31_00_now on page 3-168
0x10BC	access_address_max3_47_32_now	RO	0x00000000	32	3.3.378 access_address_max3_47_32_now on page 3-169
0x10C0	access_address_min4_31_00_now	RO	0x00000000	32	3.3.379 access_address_min4_31_00_now on page 3-169
0x10C4	access_address_min4_47_32_now	RO	0x00000000	32	3.3.380 access_address_min4_47_32_now on page 3-169
0x10C8	access_address_max4_31_00_now	RO	0x00000000	32	3.3.381 access_address_max4_31_00_now on page 3-170
0x10CC	access_address_max4_47_32_now	RO	0x00000000	32	3.3.382 access_address_max4_47_32_now on page 3-170
0x10D0	access_address_min5_31_00_now	RO	0x00000000	32	3.3.383 access_address_min5_31_00_now on page 3-170

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x10D4	access_address_min5_47_32_now	RO	0x00000000	32	3.3.384 access_address_min5_47_32_now on page 3-171
0x10D8	access_address_max5_31_00_now	RO	0x00000000	32	3.3.385 access_address_max5_31_00_now on page 3-171
0x10DC	access_address_max5_47_32_now	RO	0x00000000	32	3.3.386 access_address_max5_47_32_now on page 3-171
0x10E0	access_address_min6_31_00_now	RO	0x00000000	32	3.3.387 access_address_min6_31_00_now on page 3-172
0x10E4	access_address_min6_47_32_now	RO	0x00000000	32	3.3.388 access_address_min6_47_32_now on page 3-172
0x10E8	access_address_max6_31_00_now	RO	0x00000000	32	3.3.389 access_address_max6_31_00_now on page 3-172
0x10EC	access_address_max6_47_32_now	RO	0x00000000	32	3.3.390 access_address_max6_47_32_now on page 3-173
0x10F0	access_address_min7_31_00_now	RO	0x00000000	32	3.3.391 access_address_min7_31_00_now on page 3-173
0x10F4	access_address_min7_47_32_now	RO	0x00000000	32	3.3.392 access_address_min7_47_32_now on page 3-173
0x10F8	access_address_max7_31_00_now	RO	0x00000000	32	3.3.393 access_address_max7_31_00_now on page 3-174
0x10FC	access_address_max7_47_32_now	RO	0x00000000	32	3.3.394 access_address_max7_47_32_now on page 3-174
0x1110	dc_i_replay_type_now	RO	0x00000002	32	3.3.395 dc_i_replay_type_now on page 3-174
0x1114	direct_control_now	RO	0x0003FFFF	32	3.3.396 direct_control_now on page 3-175
0x1120	refresh_control_now	RO	0x00000000	32	3.3.397 refresh_control_now on page 3-175
0x1128	memory_type_now	RO	0x00000101	32	3.3.398 memory_type_now on page 3-175
0x1170	scrub_control0_now	RO	0x0FFFFFF0	32	3.3.399 scrub_control0_now on page 3-175
0x1174	scrub_address_min0_now	RO	0x00000000	32	3.3.400 scrub_address_min0_now on page 3-176
0x1178	scrub_address_max0_now	RO	0x00000000	32	3.3.401 scrub_address_max0_now on page 3-176
0x1180	scrub_control1_now	RO	0x0FFFFFF0	32	3.3.402 scrub_control1_now on page 3-176
0x1184	scrub_address_min1_now	RO	0x00000000	32	3.3.403 scrub_address_min1_now on page 3-177
0x1188	scrub_address_max1_now	RO	0x00000000	32	3.3.404 scrub_address_max1_now on page 3-177

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x11A0	cs_remap_control_31_00_now	RO	0x00020001	32	3.3.405 cs_remap_control_31_00_now on page 3-177
0x11A4	cs_remap_control_63_32_now	RO	0x00080004	32	3.3.406 cs_remap_control_63_32_now on page 3-178
0x11A8	cs_remap_control_95_64_now	RO	0x00200010	32	3.3.407 cs_remap_control_95_64_now on page 3-178
0x11AC	cs_remap_control_127_96_now	RO	0x00800040	32	3.3.408 cs_remap_control_127_96_now on page 3-178
0x11B0	cid_remap_control_31_00_now	RO	0x20001000	32	3.3.409 cid_remap_control_31_00_now on page 3-179
0x11B4	cid_remap_control_63_32_now	RO	0x00004000	32	3.3.410 cid_remap_control_63_32_now on page 3-179
0x11C0	cke_remap_control_now	RO	0x76543210	32	3.3.411 cke_remap_control_now on page 3-179
0x11C4	rst_remap_control_now	RO	0x76543210	32	3.3.412 rst_remap_control_now on page 3-179
0x11C8	ck_remap_control_now	RO	0x76543210	32	3.3.413 ck_remap_control_now on page 3-180
0x11D0	power_group_control_31_00_now	RO	0x00020001	32	3.3.414 power_group_control_31_00_now on page 3-180
0x11D4	power_group_control_63_32_now	RO	0x00080004	32	3.3.415 power_group_control_63_32_now on page 3-180
0x11D8	power_group_control_95_64_now	RO	0x00200010	32	3.3.416 power_group_control_95_64_now on page 3-181
0x11DC	power_group_control_127_96_now	RO	0x00800040	32	3.3.417 power_group_control_127_96_now on page 3-181
0x11F0	feature_control_now	RO	0x0AA00000	32	3.3.418 feature_control_now on page 3-181
0x11F4	mux_control_now	RO	0x00000000	32	3.3.419 mux_control_now on page 3-182
0x11F8	rank_remap_control_now	RO	0x76543210	32	3.3.420 rank_remap_control_now on page 3-182
0x1200	t_refi_now	RO	0x00090100	32	3.3.421 t_refi_now on page 3-182
0x1204	t_rfc_now	RO	0x00008C23	32	3.3.422 t_rfc_now on page 3-183
0x1208	t_mrr_now	RO	0x00000002	32	3.3.423 t_mrr_now on page 3-183
0x120C	t_mrwnow	RO	0x0000000C	32	3.3.424 t_mrwnow on page 3-183
0x1210	refresh_enable_now	RO	0x00000001	32	3.3.425 refresh_enable_now on page 3-184

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1218	t_rcd_now	RO	0x00000005	32	3.3.426 t_rcd_now on page 3-184
0x121C	t_ras_now	RO	0x0000000E	32	3.3.427 t_ras_now on page 3-184
0x1220	t_rp_now	RO	0x00000005	32	3.3.428 t_rp_now on page 3-185
0x1224	t_rpall_now	RO	0x00000005	32	3.3.429 t_rpall_now on page 3-185
0x1228	t_rrd_now	RO	0x04000404	32	3.3.430 t_rrd_now on page 3-185
0x122C	t_act_window_now	RO	0x03561414	32	3.3.431 t_act_window_now on page 3-186
0x1234	t_rtr_now	RO	0x10060404	32	3.3.432 t_rtr_now on page 3-186
0x1238	t_rtw_now	RO	0x00060606	32	3.3.433 t_rtw_now on page 3-186
0x123C	t_rtp_now	RO	0x00000004	32	3.3.434 t_rtp_now on page 3-187
0x1244	t_wr_now	RO	0x00000005	32	3.3.435 t_wr_now on page 3-187
0x1248	t_wtr_now	RO	0x00040505	32	3.3.436 t_wtr_now on page 3-187
0x124C	t_wtw_now	RO	0x10060404	32	3.3.437 t_wtw_now on page 3-188
0x1250	t_clock_control_now	RO	0x00000505	32	3.3.438 t_clock_control_now on page 3-188
0x1254	t_xmpd_now	RO	0x000003FF	32	3.3.439 t_xmpd_now on page 3-188
0x1258	t_ep_now	RO	0x00000002	32	3.3.440 t_ep_now on page 3-189
0x125C	t_xp_now	RO	0x00060002	32	3.3.441 t_xp_now on page 3-189
0x1260	t_esr_now	RO	0x0000000E	32	3.3.442 t_esr_now on page 3-189
0x1264	t_xsr_now	RO	0x05120100	32	3.3.443 t_xsr_now on page 3-190
0x1268	t_esrck_now	RO	0x00000005	32	3.3.444 t_esrck_now on page 3-190
0x126C	t_ckxsr_now	RO	0x00000001	32	3.3.445 t_ckxsr_now on page 3-190
0x1270	t_cmd_now	RO	0x00000000	32	3.3.446 t_cmd_now on page 3-191

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x127 4	t_parity_now	RO	0x00000900	32	3.3.447 <i>t_parity_now</i> on page 3-191
0x127 8	t_zqcs_now	RO	0x00000040	32	3.3.448 <i>t_zqcs_now</i> on page 3-191
0x127 C	t_rw_odt_clr_now	RO	0x00000000	32	3.3.449 <i>t_rw_odt_clr_now</i> on page 3-192
0x130 0	t_rddata_en_now	RO	0x00000001	32	3.3.450 <i>t_rddata_en_now</i> on page 3-192
0x130 4	t_phyrdlat_now	RO	0x00000000	32	3.3.451 <i>t_phyrdlat_now</i> on page 3-192
0x130 8	t_phywrlat_now	RO	0x00000001	32	3.3.452 <i>t_phywrlat_now</i> on page 3-193
0x131 0	rdlvl_control_now	RO	0x00001080	32	3.3.453 <i>rdlvl_control_now</i> on page 3-193
0x131 4	rdlvl_mrs_now	RO	0x00000004	32	3.3.454 <i>rdlvl_mrs_now</i> on page 3-193
0x131 8	t_rdlvl_en_now	RO	0x00000000	32	3.3.455 <i>t_rdlvl_en_now</i> on page 3-194
0x131 C	t_rdlvl_rr_now	RO	0x00000000	32	3.3.456 <i>t_rdlvl_rr_now</i> on page 3-194
0x132 0	wrlvl_control_now	RO	0x00101000	32	3.3.457 <i>wrlvl_control_now</i> on page 3-194
0x132 4	wrlvl_mrs_now	RO	0x00000086	32	3.3.458 <i>wrlvl_mrs_now</i> on page 3-195
0x132 8	t_wrlvl_en_now	RO	0x00000000	32	3.3.459 <i>t_wrlvl_en_now</i> on page 3-195
0x132 C	t_wrlvl_ww_now	RO	0x00000000	32	3.3.460 <i>t_wrlvl_ww_now</i> on page 3-195
0x134 8	phy_power_control_now	RO	0x00000000	32	3.3.461 <i>phy_power_control_now</i> on page 3-196
0x134 C	t_lpresp_now	RO	0x00000000	32	3.3.462 <i>t_lpresp_now</i> on page 3-196
0x135 0	phy_update_control_now	RO	0x2FE00000	32	3.3.463 <i>phy_update_control_now</i> on page 3-196
0x135 4	t_odth_now	RO	0x00000006	32	3.3.464 <i>t_odth_now</i> on page 3-197
0x135 8	odt_timing_now	RO	0x06000600	32	3.3.465 <i>odt_timing_now</i> on page 3-197
0x136 0	odt_wr_control_31_00_now	RO	0x08040201	32	3.3.466 <i>odt_wr_control_31_00_now</i> on page 3-197
0x136 4	odt_wr_control_63_32_now	RO	0x80402010	32	3.3.467 <i>odt_wr_control_63_32_now</i> on page 3-198

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1368	odt_rd_control_31_00_now	RO	0x00000000	32	3.3.468 odt_rd_control_31_00_now on page 3-198
0x136C	odt_rd_control_63_32_now	RO	0x00000000	32	3.3.469 odt_rd_control_63_32_now on page 3-198
0x1380	dq_map_control_15_00_now	RO	0x00000000	32	3.3.470 dq_map_control_15_00_now on page 3-199
0x1384	dq_map_control_31_16_now	RO	0x00000000	32	3.3.471 dq_map_control_31_16_now on page 3-199
0x1388	dq_map_control_47_32_now	RO	0x00000000	32	3.3.472 dq_map_control_47_32_now on page 3-199
0x138C	dq_map_control_63_48_now	RO	0x00000000	32	3.3.473 dq_map_control_63_48_now on page 3-200
0x1390	dq_map_control_71_64_now	RO	0x00000000	32	3.3.474 dq_map_control_71_64_now on page 3-200
0x13B0	odt_cp_control_31_00_now	RO	0x08040201	32	3.3.475 odt_cp_control_31_00_now on page 3-200
0x13B4	odt_cp_control_63_32_now	RO	0x80402010	32	3.3.476 odt_cp_control_63_32_now on page 3-201
0x1408	user_config0_now	RO	0x00000000	32	3.3.477 user_config0_now on page 3-201
0x140C	user_config1_now	RO	0x00000000	32	3.3.478 user_config1_now on page 3-201
0x1610	t_db_train_resp_now	RO	0x00000000	32	3.3.479 t_db_train_resp_now on page 3-202
0x1614	t_lvl_disconnect_now	RO	0x0000000F	32	3.3.480 t_lvl_disconnect_now on page 3-202
0x1620	wdqlvl_control_now	RO	0x00000094	32	3.3.481 wdqlvl_control_now on page 3-202
0x1624	wdqlvl_vrefdq_train_mrs_now	RO	0x00000000	32	3.3.482 wdqlvl_vrefdq_train_mrs_now on page 3-203
0x1628	wdqlvl_address_31_00_now	RO	0x00000000	32	3.3.483 wdqlvl_address_31_00_now on page 3-203
0x162C	wdqlvl_address_63_32_now	RO	0x00000000	32	3.3.484 wdqlvl_address_63_32_now on page 3-203
0x1630	t_wdqlvl_en_now	RO	0x00000000	32	3.3.485 t_wdqlvl_en_now on page 3-204
0x1634	t_wdqlvl_ww_now	RO	0x00000000	32	3.3.486 t_wdqlvl_ww_now on page 3-204
0x1638	t_wdqlvl_rw_now	RO	0x00000000	32	3.3.487 t_wdqlvl_rw_now on page 3-204
0x1654	phymstr_control_now	RO	0x00000000	32	3.3.488 phymstr_control_now on page 3-205

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1FD0	periph_id_4	RO	0x00000014	32	3.3.489 periph_id_4 on page 3-205
0x1FE0	periph_id_0	RO	0x00000054	32	3.3.490 periph_id_0 on page 3-205
0x1FE4	periph_id_1	RO	0x000000B4	32	3.3.491 periph_id_1 on page 3-206
0x1FE8	periph_id_2	RO	0x0000000B	32	3.3.492 periph_id_2 on page 3-206
0x1FEC	periph_id_3	RO	0x00000000	32	3.3.493 periph_id_3 on page 3-206
0x1FF0	component_id_0	RO	0x0000000D	32	3.3.494 component_id_0 on page 3-206
0x1FF4	component_id_1	RO	0x000000F0	32	3.3.495 component_id_1 on page 3-207
0x1FF8	component_id_2	RO	0x00000005	32	3.3.496 component_id_2 on page 3-207
0x1FFC	component_id_3	RO	0x000000B1	32	3.3.497 component_id_3 on page 3-207

3.3.1 memc_status

Holds the architectural status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x000
Type	Read-only
Reset	0x00000000
Width	32

3.3.2 memc_config

Holds the configuration data for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc_config register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x004
---------------	-------

Type	Read-only
Reset	0x00000000
Width	32

3.3.3 memc_cmd

Used to change the architectural state of the DMC, or execute queued manager operations. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The memc_cmd register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x008
Type	Write-only
Reset	0x00000000
Width	32

3.3.4 address_control_next

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x010
Type	Read-write
Reset	0x00030202
Width	32

3.3.5 decode_control_next

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, ie. row_order != bank_order != rank_order. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The decode_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x014
Type	Read-write
Reset	0x001A3000

Width 32

3.3.6 format_control

Configures the memory burst access parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The format_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x018
Type	Read-write
Reset	0x12000113
Width	32

3.3.7 address_map_next

Configures the system address mapping options. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_map_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x01C
Type	Read-write
Reset	0x00000000
Width	32

3.3.8 low_power_control_next

Configures the low-power features of the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The low_power_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x020
Type	Read-write
Reset	0x00000020
Width	32

3.3.9 turnaround_control_next

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The turnaround_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x028
Type	Read-write
Reset	0x0F0F0F0F
Width	32

3.3.10 hit_turnaround_control_next

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The hit_turnaround_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x02C
Type	Read-write
Reset	0x08909FBF
Width	32

3.3.11 qos_class_control_next

Configures the priority class for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qos_class_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x030
Type	Read-write
Reset	0x00000FC8
Width	32

3.3.12 escalation_control_next

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The escalation_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x034
Type	Read-write
Reset	0x00080F03
Width	32

3.3.13 qv_control_31_00_next

Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qv_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x038
Type	Read-write
Reset	0x76543210
Width	32

3.3.14 qv_control_63_32_next

Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qv_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x03C
Type	Read-write
Reset	0xFEDCBA98
Width	32

3.3.15 rt_control_31_00_next

Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rt_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x040
Type	Read-write
Reset	0x00000000

Width 32

3.3.16 **rt_control_63_32_next**

Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rt_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x044
Type	Read-write
Reset	0x00000000
Width	32

3.3.17 **timeout_control_next**

Configures the prescaler applied to timeout values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The timeout_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x048
Type	Read-write
Reset	0x00000001
Width	32

3.3.18 **credit_control_next**

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The credit_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x04C
Type	Read-write
Reset	0x00000F03
Width	32

3.3.19 **write_priority_control_31_00_next**

Configures the priority settings for write requests within the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The write_priority_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x050
Type	Read-write
Reset	0x00000000
Width	32

3.3.20 write_priority_control_63_32_next

Configures the priority settings for write requests within the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The write_priority_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x054
Type	Read-write
Reset	0x00000000
Width	32

3.3.21 queue_threshold_control_31_00_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue_threshold_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x058
Type	Read-write
Reset	0x00000008
Width	32

3.3.22 queue_threshold_control_63_32_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue_threshold_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x05C
Type	Read-write
Reset	0x00000000
Width	32

3.3.23 address_shutter_31_00_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x060
Type	Read-write
Reset	0x00000000
Width	32

3.3.24 address_shutter_63_32_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x064
Type	Read-write
Reset	0x00000000
Width	32

3.3.25 address_shutter_95_64_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_95_64_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x068
Type	Read-write
Reset	0x00000000

Width 32

3.3.26 address_shutter_127_96_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_127_96_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x06C
Type	Read-write
Reset	0x00000000
Width	32

3.3.27 address_shutter_159_128_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_159_128_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x070
Type	Read-write
Reset	0x00000000
Width	32

3.3.28 address_shutter_191_160_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_191_160_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x074
Type	Read-write
Reset	0x00000000
Width	32

3.3.29 memory_address_max_31_00_next

Configures the address space control for the DMC default region. Applies post address translation.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory_address_max_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x078
Type	Read-write
Reset	0x00000010
Width	32

3.3.30 memory_address_max_47_32_next

Configures the address space control for the DMC default region. Applies post address translation.

Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory_address_max_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x07C
Type	Read-write
Reset	0x00000000
Width	32

3.3.31 access_address_min0_31_00_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min0_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x080
Type	Read-write
Reset	0x00000000
Width	32

3.3.32 access_address_min0_47_32_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min0_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x084
Type	Read-write
Reset	0x00000000
Width	32

3.3.33 access_address_max0_31_00_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max0_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x088
Type	Read-write
Reset	0x00000000
Width	32

3.3.34 access_address_max0_47_32_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max0_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x08C
Type	Read-write
Reset	0x00000000
Width	32

3.3.35 access_address_min1_31_00_next

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min1_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x090
Type	Read-write
Reset	0x00000000

Width 32

3.3.36 **access_address_min1_47_32_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min1_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x094
Type	Read-write
Reset	0x00000000
Width	32

3.3.37 **access_address_max1_31_00_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max1_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x098
Type	Read-write
Reset	0x00000000
Width	32

3.3.38 **access_address_max1_47_32_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max1_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x09C
Type	Read-write
Reset	0x00000000
Width	32

3.3.39 **access_address_min2_31_00_next**

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min2_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0A0
Type	Read-write
Reset	0x00000000
Width	32

3.3.40 access_address_min2_47_32_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min2_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0A4
Type	Read-write
Reset	0x00000000
Width	32

3.3.41 access_address_max2_31_00_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max2_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0A8
Type	Read-write
Reset	0x00000000
Width	32

3.3.42 access_address_max2_47_32_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max2_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0AC
Type	Read-write
Reset	0x00000000
Width	32

3.3.43 access_address_min3_31_00_next

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min3_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0B0
Type	Read-write
Reset	0x00000000
Width	32

3.3.44 access_address_min3_47_32_next

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min3_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0B4
Type	Read-write
Reset	0x00000000
Width	32

3.3.45 access_address_max3_31_00_next

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max3_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0B8
Type	Read-write
Reset	0x00000000

Width 32

3.3.46 **access_address_max3_47_32_next**

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max3_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0BC
Type	Read-write
Reset	0x00000000
Width	32

3.3.47 **access_address_min4_31_00_next**

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min4_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0C0
Type	Read-write
Reset	0x00000000
Width	32

3.3.48 **access_address_min4_47_32_next**

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min4_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0C4
Type	Read-write
Reset	0x00000000
Width	32

3.3.49 **access_address_max4_31_00_next**

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max4_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0C8
Type	Read-write
Reset	0x00000000
Width	32

3.3.50 access_address_max4_47_32_next

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max4_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0CC
Type	Read-write
Reset	0x00000000
Width	32

3.3.51 access_address_min5_31_00_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min5_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0D0
Type	Read-write
Reset	0x00000000
Width	32

3.3.52 access_address_min5_47_32_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min5_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0D4
Type	Read-write
Reset	0x00000000
Width	32

3.3.53 access_address_max5_31_00_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max5_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0D8
Type	Read-write
Reset	0x00000000
Width	32

3.3.54 access_address_max5_47_32_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max5_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0DC
Type	Read-write
Reset	0x00000000
Width	32

3.3.55 access_address_min6_31_00_next

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min6_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0E0
Type	Read-write
Reset	0x00000000

Width 32

3.3.56 **access_address_min6_47_32_next**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min6_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0E4
Type	Read-write
Reset	0x00000000
Width	32

3.3.57 **access_address_max6_31_00_next**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max6_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0E8
Type	Read-write
Reset	0x00000000
Width	32

3.3.58 **access_address_max6_47_32_next**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max6_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0EC
Type	Read-write
Reset	0x00000000
Width	32

3.3.59 **access_address_min7_31_00_next**

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min7_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0F0
Type	Read-write
Reset	0x00000000
Width	32

3.3.60 access_address_min7_47_32_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min7_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0F4
Type	Read-write
Reset	0x00000000
Width	32

3.3.61 access_address_max7_31_00_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max7_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0F8
Type	Read-write
Reset	0x00000000
Width	32

3.3.62 access_address_max7_47_32_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max7_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x0FC
Type	Read-write
Reset	0x00000000
Width	32

3.3.63 channel_status

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x100
Type	Read-only
Reset	0x00000003
Width	32

3.3.64 channel_status_63_32

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel_status_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x104
Type	Read-only
Reset	0x00000000
Width	32

3.3.65 direct_addr

Sets the direct command address field for direct commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The direct_addr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x108
Type	Read-write
Reset	0x00000000

Width 32

3.3.66 **direct_cmd**

Generates direct commands from the manager. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG, PAUSED or READY states.

The direct_cmd register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10C
Type Write-only
Reset 0x00000000
Width 32

3.3.67 **dci_replay_type_next**

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dci_replay_type_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x110
Type Read-write
Reset 0x00000002
Width 32

3.3.68 **direct_control_next**

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The direct_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x114
Type Read-write
Reset 0x0003FFFF
Width 32

3.3.69 dci_strb

Configures the write data strobe values used during direct_cmd WRITE operations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The dci_strb register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x118
Type	Read-write
Reset	0x0000000F
Width	32

3.3.70 dci_data

Reading from this register location returns read data received a result of a READ command. Writing to this register location sets the data to be used for direct_cmd WRITE commands. You must read or write once for each 32-bit data word of a DRAM burst. Access restrictions: RW Can be read from when in CONFIG, PAUSED or READY states. Can be written to when in CONFIG, PAUSED or READY states.

The dci_data register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11C
Type	Read-write
Reset	0x00000000
Width	32

3.3.71 refresh_control_next

Configures the type of refresh commands issued by the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The refresh_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x120
Type	Read-write
Reset	0x00000000
Width	32

3.3.72 memory_type_next

Configures the DMC for the attached memory type. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory_type_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x128
Type	Read-write
Reset	0x00000101
Width	32

3.3.73 feature_config

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The feature_config register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x130
Type	Read-write
Reset	0x000018E0
Width	32

3.3.74 nibble_failed_031_000

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_031_000 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x138
Type	Read-write
Reset	0x00000000
Width	32

3.3.75 nibble_failed_063_032

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_063_032 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x13C
Type	Read-write
Reset	0x00000000
Width	32

3.3.76 nibble_failed_095_064

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_095_064 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x140
Type	Read-write
Reset	0x00000000
Width	32

3.3.77 nibble_failed_127_096

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_127_096 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x144
Type	Read-write
Reset	0x00000000
Width	32

3.3.78 queue_allocate_control_031_000

Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_031_000 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x148
Type	Read-write
Reset	0xFFFFFFFF
Width	32

3.3.79 queue_allocate_control_063_032

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_063_032 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x14C
Type	Read-write
Reset	0xFFFFFFFF
Width	32

3.3.80 queue_allocate_control_095_064

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_095_064 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x150
Type	Read-write
Reset	0xFFFFFFFF
Width	32

3.3.81 queue_allocate_control_127_096

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_127_096 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x154
Type	Read-write

Reset	0xFFFFFFFF
Width	32

3.3.82 link_err_count

Counter register for link errors. The counter increments on detection of a new link error (dfi_alert_n or dfi_err). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The link_err_count register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x16C
Type	Read-write
Reset	0x00000000
Width	32

3.3.83 scrub_control0_next

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_control0_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x170
Type	Read-write
Reset	0x0FFFFFF0
Width	32

3.3.84 scrub_address_min0_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_min0_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x174
Type	Read-write
Reset	0x00000000
Width	32

3.3.85 scrub_address_max0_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_max0_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x178
Type	Read-write
Reset	0x00000000
Width	32

3.3.86 scrub_address_current0

Current scrub address for scrub 0. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub_address_current0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x17C
Type	Read-only
Reset	0x00000000
Width	32

3.3.87 scrub_control1_next

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_control1_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x180
Type	Read-write
Reset	0x0FFFFFF0
Width	32

3.3.88 scrub_address_min1_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_min1_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x184
Type	Read-write
Reset	0x00000000
Width	32

3.3.89 scrub_address_max1_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_max1_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x188
Type	Read-write
Reset	0x00000000
Width	32

3.3.90 scrub_address_current1

Current scrub address for scrub 1. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub_address_current1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x18C
Type	Read-only
Reset	0x00000000
Width	32

3.3.91 cs_remap_control_31_00_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1A0
Type	Read-write
Reset	0x00020001
Width	32

3.3.92 cs_remap_control_63_32_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1A4
Type	Read-write
Reset	0x00080004
Width	32

3.3.93 cs_remap_control_95_64_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_95_64_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1A8
Type	Read-write
Reset	0x00200010
Width	32

3.3.94 cs_remap_control_127_96_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_127_96_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1AC
Type	Read-write
Reset	0x00800040
Width	32

3.3.95 cid_remap_control_31_00_next

Control register for dfi_CID remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid_remap_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1B0
Type	Read-write
Reset	0x20001000
Width	32

3.3.96 cid_remap_control_63_32_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid_remap_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1B4
Type	Read-write
Reset	0x00004000
Width	32

3.3.97 cke_remap_control_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cke_remap_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1C0
Type	Read-write
Reset	0x76543210
Width	32

3.3.98 rst_remap_control_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rst_remap_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1C4
Type	Read-write
Reset	0x76543210
Width	32

3.3.99 ck_remap_control_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The ck_remap_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1C8
Type	Read-write
Reset	0x76543210
Width	32

3.3.100 power_group_control_31_00_next

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke_remap_control register should belong to the same power-group Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1D0
Type	Read-write
Reset	0x00020001
Width	32

3.3.101 power_group_control_63_32_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1D4
Type	Read-write
Reset	0x00080004
Width	32

3.3.102 power_group_control_95_64_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_95_64_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1D8
Type	Read-write
Reset	0x00200010
Width	32

3.3.103 power_group_control_127_96_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_127_96_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1DC
Type	Read-write
Reset	0x00800040
Width	32

3.3.104 phy_rdwrdata_cs_mask_31_00

Maps a logical rank to the physical rank phy_rd/wrdata_cs output pins. Using this register it is possible to map a logical rank to multiple phy_rdwrdata_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_rdwrdata_cs_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1E0
Type	Read-write
Reset	0xF7FBDFE

Width 32

3.3.105 phy_rdwrdata_cs_mask_63_32

Maps a logical rank to the physical rank phy_rd/wrdata_cs output pins. Using this register it is possible to map a logical rank to multiple phy_rdwrdata_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_rdwrdata_cs_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1E4
Type	Read-write
Reset	0x7FBDFEF
Width	32

3.3.106 phy_request_cs_remap

Maps PHY training request from a physical chip select to DMC internal logical chip select. Requests which are mapped using this register are dfi_rdlvl_cs, dfi_rdlvl_gate_cs, dfi_wrlvl_cs, dfi_phylvl_req_cs_n and dfi_phymstr_cs_state. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_request_cs_remap register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1E8
Type	Read-write
Reset	0x76543210
Width	32

3.3.107 feature_control_next

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The feature_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1F0
Type	Read-write
Reset	0x0AA00000
Width	32

3.3.108 mux_control_next

Control muxing options for the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The mux_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1F4
Type	Read-write
Reset	0x00000000
Width	32

3.3.109 rank_remap_control_next

Control register for rank remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rank_remap_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1F8
Type	Read-write
Reset	0x76543210
Width	32

3.3.110 t_refi_next

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_refi_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x200
Type	Read-write
Reset	0x00090100
Width	32

3.3.111 t_rfc_next

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rfc_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x204
Type	Read-write
Reset	0x00008C23
Width	32

3.3.112 t_mrr_next

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_mrr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x208
Type	Read-write
Reset	0x00000002
Width	32

3.3.113 t_mrw_next

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_mrw_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x20C
Type	Read-write
Reset	0x0000000C
Width	32

3.3.114 refresh_enable_next

Configures refresh counters . Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The refresh_enable_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x210
Type	Read-write
Reset	0x00000001
Width	32

3.3.115 t_rcd_next

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rcd_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x218
Type	Read-write
Reset	0x00000005
Width	32

3.3.116 t_ras_next

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ras_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x21C
Type	Read-write
Reset	0x0000000E
Width	32

3.3.117 t_rp_next

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rp_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x220
Type	Read-write
Reset	0x00000005
Width	32

3.3.118 t_rpall_next

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rpall_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x224
Type	Read-write
Reset	0x00000005
Width	32

3.3.119 t_rrd_next

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rrd_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x228
Type	Read-write
Reset	0x04000404
Width	32

3.3.120 t_act_window_next

Configures the tFAW and tMAWi timing parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_act_window_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x22C
Type	Read-write
Reset	0x03561414
Width	32

3.3.121 t_rtr_next

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), different chip-selects (t_rtr_cs), and same chip, different logical rank(t_rtr_dlr). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x234
Type	Read-write
Reset	0x10060404
Width	32

3.3.122 t_rtw_next

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_rtw_l), and other chip-selects (t_rtw_cs). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtw_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x238
Type	Read-write
Reset	0x00060606
Width	32

3.3.123 t_rtp_next

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtp_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x23C
Type	Read-write
Reset	0x00000004
Width	32

3.3.124 t_wr_next

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITES, to the same bank. Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: $t_wr(dmc) = CWL + 4 + tWR(\text{from dram data sheet})$. CWL should account for write CRC if enabled. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x244
Type	Read-write
Reset	0x00000005
Width	32

3.3.125 t_wtr_next

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs). Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: $t_wtr(dmc) = CWL + WBL/2 + tWR(\text{DRAM})$. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wtr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x248
Type	Read-write
Reset	0x00040505
Width	32

3.3.126 t_wtw_next

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes, same chip, different logical rank(t_wtw_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wtw_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x24C
Type	Read-write
Reset	0x10060404
Width	32

3.3.127 t_clock_control_next

Configures the enter DRAM clock disable timing parameter. This parameter is applied between stopping the clock when idle, or when in a power-down state, and any subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_clock_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x250
Type	Read-write
Reset	0x00000505
Width	32

3.3.128 t_xmpd_next

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xmpd_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x254
Type	Read-write
Reset	0x000003FF
Width	32

3.3.129 t_ep_next

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ep_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x258
Type	Read-write
Reset	0x00000002
Width	32

3.3.130 t_xp_next

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t_xpdll must be greater than or equal to tRCD and tCKE, and t_xp must be greater than or equal to tMPX_S. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xp_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x25C
Type	Read-write
Reset	0x00060002
Width	32

3.3.131 t_esr_next

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_esr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x260
Type	Read-write
Reset	0x0000000E
Width	32

3.3.132 t_xsr_next

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xsr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x264
Type	Read-write
Reset	0x05120100
Width	32

3.3.133 t_esrck_next

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_esrck_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x268
Type	Read-write
Reset	0x00000005
Width	32

3.3.134 t_ckxsr_next

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ckxsr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x26C
Type	Read-write
Reset	0x00000001
Width	32

3.3.135 t_cmd_next

Configures command signaling timing. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_cmd_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x270
Type	Read-write

Reset 0x00000000
Width 32

3.3.136 t_parity_next

Parity latencies t_parinlat and t_completion. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_parity_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x274
Type Read-write
Reset 0x00000900
Width 32

3.3.137 t_zqcs_next

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_zqcs_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x278
Type Read-write
Reset 0x00000040
Width 32

3.3.138 t_rw_odt_clr_next

This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as tpoll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to t_odt_off_rd/wr(max setting) + DODTLoff(from DDR4 spec) Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rw_odt_clr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x27C
Type Read-write

Reset 0x00000000
Width 32

3.3.139 t_rddata_en_next

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rddata_en_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x300
Type Read-write
Reset 0x00000001
Width 32

3.3.140 t_phyrdlat_next

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_phyrdlat_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x304
Type Read-write
Reset 0x00000000
Width 32

3.3.141 t_phywrlat_next

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrddata_en, dfi_wrddata_cs and dfi_wrddata signals. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_phywrlat_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x308
Type Read-write
Reset 0x00000001
Width 32

3.3.142 rdlvl_control_next

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x310
Type	Read-write
Reset	0x00001080
Width	32

3.3.143 rdlvl_mrs_next

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl_mrs_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x314
Type	Read-write
Reset	0x00000004
Width	32

3.3.144 t_rdlvl_en_next

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rdlvl_en_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x318
Type	Read-write
Reset	0x00000000
Width	32

3.3.145 t_rdlvl_rr_next

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rdlvl_rr_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x31C
Type	Read-write
Reset	0x00000000
Width	32

3.3.146 wrlvl_control_next

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x320
Type	Read-write
Reset	0x00101000
Width	32

3.3.147 wrlvl_mrs_next

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl_mrs_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x324
Type	Read-write
Reset	0x00000086
Width	32

3.3.148 t_wrlvl_en_next

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wrlvl_en_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x328
Type	Read-write
Reset	0x00000000
Width	32

3.3.149 t_wrlvl_ww_next

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wrlvl_ww_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x32C
Type	Read-write
Reset	0x00000000
Width	32

3.3.150 training_wrlvl_slice_status

Shows slice information relating to the wrlvl training request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_wrlvl_slice_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x334
Type	Read-only
Reset	0x00000000
Width	32

3.3.151 training_rdlvl_slice_status

Shows slice information relating to the rdlvl training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_slice_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x338
Type	Read-only
Reset	0x00000000
Width	32

3.3.152 training_rdlvl_gate_slice_status

Shows slice information relating to the rdlvl gate training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_gate_slice_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x33C
Type	Read-only
Reset	0x00000000
Width	32

3.3.153 training_wdqlvl_slice_status

Shows slice information relating to the WrDQ training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x340
Type	Read-only
Reset	0x00000000
Width	32

3.3.154 training_wdqlvl_slice_result

Shows per slice result from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_result register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x344
Type	Read-only
Reset	0x00000000
Width	32

3.3.155 phy_power_control_next

Configures the low-power requests made to the PHY for the different channel states. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_power_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x348
Type	Read-write
Reset	0x00000000
Width	32

3.3.156 t_lpresp_next

Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_lpresp_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x34C
Type	Read-write
Reset	0x00000000
Width	32

3.3.157 phy_update_control_next

Configures the update mechanism to use in response to PHY training requests. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_update_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x350
Type	Read-write
Reset	0x2FE00000
Width	32

3.3.158 t_odth_next

Configures the ODT8 timing parameter as timed from Write command registered with ODT high
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_odth_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x354
Type	Read-write
Reset	0x00000006
Width	32

3.3.159 odt_timing_next

Configures the ODT on and off timing. Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The odt_timing_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x358
Type	Read-write
Reset	0x06000600
Width	32

3.3.160 odt_wr_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions:
RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_wr_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x360
Type	Read-write
Reset	0x08040201
Width	32

3.3.161 odt_wr_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_wr_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x364
Type	Read-write
Reset	0x80402010
Width	32

3.3.162 odt_rd_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_rd_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x368
Type	Read-write
Reset	0x00000000
Width	32

3.3.163 odt_rd_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_rd_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x36C
Type	Read-write
Reset	0x00000000
Width	32

3.3.164 temperature_readout

Holds the status of the temperature information. Reading the register returns the current temperature from the most recent automated temperature poll. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The temperature_readout register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x370
Type	Read-only
Reset	0x00000000
Width	32

3.3.165 training_status

Shows information relating to the training request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x378
Type	Read-only
Reset	0x00000000
Width	32

3.3.166 training_status_63_32

Shows information relating to the update request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_status_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x37C
Type	Read-only
Reset	0x00000000
Width	32

3.3.167 dq_map_control_15_00_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_15_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x380
Type	Read-write
Reset	0x00000000
Width	32

3.3.168 dq_map_control_31_16_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_31_16_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x384
Type	Read-write
Reset	0x00000000
Width	32

3.3.169 dq_map_control_47_32_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_47_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x388
Type	Read-write
Reset	0x00000000
Width	32

3.3.170 dq_map_control_63_48_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_63_48_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x38C
Type	Read-write
Reset	0x00000000
Width	32

3.3.171 dq_map_control_71_64_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_71_64_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x390
Type	Read-write
Reset	0x00000000
Width	32

3.3.172 rank_status

Shows the current status of geardown, MPD and CAL. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The rank_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x398
Type	Read-only
Reset	0x00000000
Width	32

3.3.173 mode_change_status

Shows the current status of the sequence that is currently being processed. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The mode_change_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x39C
Type	Read-only
Reset	0x00000000
Width	32

3.3.174 odt_cp_control_31_00_next

Determines which of the 8 dfi_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_cp_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x3B0
Type	Read-write
Reset	0x08040201
Width	32

3.3.175 odt_cp_control_63_32_next

Determines which of the 8 dfi_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_cp_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x3B4
Type	Read-write
Reset	0x80402010
Width	32

3.3.176 user_status

Shows the value of the input user_status signals. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The user_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x400
Type	Read-only
Reset	0x00000000
Width	32

3.3.177 user_config0_next

Drives the output user_config0 signal. Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The user_config0_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x408
Type	Read-write
Reset	0x00000000
Width	32

3.3.178 user_config1_next

Drives the output user_config1 signal. Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The user_config1_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x40C
Type	Read-write
Reset	0x00000000
Width	32

3.3.179 user_config2

Drives the output user_config2 signal. Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The user_config2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x410
Type	Read-write
Reset	0x00000000
Width	32

3.3.180 user_config3

Drives the output user_config3 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user_config3 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x414
Type	Read-write
Reset	0x00000000
Width	32

3.3.181 interrupt_control

Configures interrupt behavior. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The interrupt_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x500
Type	Read-write
Reset	0x00000000
Width	32

3.3.182 interrupt_clr

Clear register for interrupts. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The interrupt_clr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x508
Type	Write-only
Reset	0x00000000
Width	32

3.3.183 interrupt_status

Status register for interrupts (pre-mask). Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The interrupt_status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x510
Type	Read-only
Reset	0x00000000
Width	32

3.3.184 failed_access_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_access_int_info_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x538
Type	Read-only
Reset	0x00000000
Width	32

3.3.185 failed_access_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_access_int_info_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x53C
Type	Read-only
Reset	0x00000000
Width	32

3.3.186 failed_prog_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_prog_int_info_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x540
Type	Read-only
Reset	0x00000000
Width	32

3.3.187 failed_prog_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_prog_int_info_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x544
Type	Read-only
Reset	0x00000000
Width	32

3.3.188 link_err_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link_err_int_info_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x548
Type	Read-only
Reset	0x00000000
Width	32

3.3.189 link_err_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link_err_int_info_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x54C
Type	Read-only
Reset	0x00000000
Width	32

3.3.190 arch_fsm_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch_fsm_int_info_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x550
Type	Read-only
Reset	0x00000000
Width	32

3.3.191 arch_fsm_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch_fsm_int_info_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x554
Type	Read-only
Reset	0x00000000
Width	32

3.3.192 t_db_train_resp_next

Configures the t_db_train_resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi_db_train_resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi_rddata_valid) to define the delay between DFI read command and when the response is valid on the dfi_rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_db_train_resp_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x610
Type	Read-write
Reset	0x00000000
Width	32

3.3.193 t_lvl_disconnect_next

Configures the t_lvl_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t*lvl_disconnect and t*lvl_disconnect_error timing parameters from the PHY Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_lvl_disconnect_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x614
Type	Read-write
Reset	0x0000000F
Width	32

3.3.194 wdqlvl_control_next

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x620
Type	Read-write
Reset	0x00000094
Width	32

3.3.195 wdqlvl_vrefdq_train_mrs_next

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the wdqlvl_control register. You enable this function with the wdqlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_vrefdq_train_mrs_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x624
Type	Read-write
Reset	0x00000000
Width	32

3.3.196 wdqlvl_address_31_00_next

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_address_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x628
Type	Read-write
Reset	0x00000000
Width	32

3.3.197 wdqlvl_address_63_32_next

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_address_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x62C
Type	Read-write
Reset	0x00000000
Width	32

3.3.198 t_wdqlvl_en_next

Configures the t_wdqlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wdqlvl_en, the delay between asserting dfi_wdqlvl_en and the first training command, the delay between de-asserting dfi_wdqlvl_en and de-asserting ODT, and de-asserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_en_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x630
Type	Read-write
Reset	0x00000000
Width	32

3.3.199 t_wdqlvl_ww_next

Configures the t_wdqlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wdqlvl_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_ww_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x634
Type	Read-write
Reset	0x00000000
Width	32

3.3.200 t_wdqlvl_rw_next

Configures the t_wdqlvl_rw timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_rw_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x638
Type	Read-write
Reset	0x00000000
Width	32

3.3.201 training_wdqlvl_slice_resp

Shows per slice response from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_resp register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x63C
Type	Read-only
Reset	0x00000000
Width	32

3.3.202 training_rdlvl_slice_resp

Shows per slice response from the PHY in response to the rdlvl training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_slice_resp register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x640
Type	Read-only
Reset	0x00000000
Width	32

3.3.203 phymstr_control_next

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phymstr_control_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x654
Type	Read-write
Reset	0x00000000
Width	32

3.3.204 err0fr

This record defines features which are common to all RAS error records in this section. Each field defines which of the architecturally-defined common features are implemented and, of the implemented features, which are software programmable. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x700
Type	Read-only
Reset	0x000009AA
Width	32

3.3.205 err0ctrl0

This register is the global control register for the DMC RAS functions. This register control features such as ECC type and enable, error reporting and interrupt enable, error deferment, etc. The setting of a Global control record bit affects all records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctrl0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x708
Type	Read-write
Reset	0x00000010
Width	32

3.3.206 err0ctrl1

This register is the global control register for the DMC RAS functions. The registers in this record affect all DMC RAS records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctrl1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x70C
Type	Read-write
Reset	0x000000C0
Width	32

3.3.207 err0status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x710
Type	Read-only
Reset	0x00000000
Width	32

3.3.208 err1fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x740
Type	Read-only
Reset	0x000009AA
Width	32

3.3.209 err1ctrl

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTRL. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1ctrl register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x748
Type	Read-only
Reset	0x00000000
Width	32

3.3.210 err1status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x750
Type	Read-write
Reset	0x00000000
Width	32

3.3.211 err1addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. If an error has an associated physical address, this must be written to the

address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x758
Type	Read-write
Reset	0x00000000
Width	32

3.3.212 err1addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank}. If an error has an associated physical address, this must be written to the address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x75C
Type	Read-write
Reset	0x00000000
Width	32

3.3.213 err1misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x760
Type	Read-write
Reset	0x00000000
Width	32

3.3.214 err1misc1

This register gives the bank, logical rank, and failed nibble location of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x764
Type	Read-write
Reset	0x00000000
Width	32

3.3.215 err1misc2

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x768
Type	Read-write
Reset	0x00000000
Width	32

3.3.216 err1misc3

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc3 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x76C
Type	Read-write
Reset	0x00000000
Width	32

3.3.217 err1misc4

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc4 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x770
Type	Read-write
Reset	0x00000000
Width	32

3.3.218 err1misc5

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc5 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x774
Type	Read-write
Reset	0x00000000
Width	32

3.3.219 err2fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x780
Type	Read-only
Reset	0x000009AA
Width	32

3.3.220 err2ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2ctlr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x788
Type	Read-only

Reset 0x00000000
Width 32

3.3.221 err2status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x790
Type Read-write
Reset 0x00000000
Width 32

3.3.222 err2addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x798
Type Read-write
Reset 0x00000000
Width 32

3.3.223 err2addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank} Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x79C
Type Read-write
Reset 0x00000000
Width 32

3.3.224 err2misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7A0
Type	Read-write
Reset	0x00000000
Width	32

3.3.225 err2misc1

This register gives the bank and logical rank of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7A4
Type	Read-write
Reset	0x00000000
Width	32

3.3.226 err2misc2

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The err2misc2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7A8
Type	Read-write
Reset	0x00000000
Width	32

3.3.227 err2misc3

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The err2misc3 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7AC
Type	Read-write
Reset	0x00000000
Width	32

3.3.228 err2misc4

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The err2misc4 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7B0
Type	Read-write
Reset	0x00000000
Width	32

3.3.229 err2misc5

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The err2misc5 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7B4
Type	Read-write
Reset	0x00000000
Width	32

3.3.230 err3fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7C0
Type	Read-only
Reset	0x000009AA
Width	32

3.3.231 err3ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3ctlr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7C8
Type	Read-only
Reset	0x00000000
Width	32

3.3.232 err3status

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7D0
Type	Read-write
Reset	0x000000
Width	32

3.3.233 err3addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x7D8
Type	Read-write
Reset	0x00000000

Width 32

3.3.234 err3addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank} Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x7DC
Type Read-write
Reset 0x00000000
Width 32

3.3.235 err3misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last created. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x7E0
Type Read-only
Reset 0x00000000
Width 32

3.3.236 err3misc1

This register gives the bank and logical rank of the first error detected since last created. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x7E4
Type Read-only
Reset 0x00000000
Width 32

3.3.237 err4fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x800
Type	Read-only
Reset	0x000009AA
Width	32

3.3.238 err4ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4ctlr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x808
Type	Read-only
Reset	0x00000000
Width	32

3.3.239 err4status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x810
Type	Read-write
Reset	0x000000
Width	32

3.3.240 err4addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x818
Type	Read-write
Reset	0x00000000
Width	32

3.3.241 err4addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x81C
Type	Read-write
Reset	0x00000000
Width	32

3.3.242 err4misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x820
Type	Read-write
Reset	0x00000000
Width	32

3.3.243 err4misc1

This register gives the bank and logical rank, and DBID of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x824
Type	Read-write
Reset	0x00000000
Width	32

3.3.244 err4misc2

Ram Correctable Error Counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x828
Type	Read-write
Reset	0x00000000
Width	32

3.3.245 err5fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x840
Type	Read-only
Reset	0x000009AA
Width	32

3.3.246 err5ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5ctlr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x848
Type	Read-only
Reset	0x00000000
Width	32

3.3.247 err5status

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x850
Type	Read-write
Reset	0x000000
Width	32

3.3.248 err5addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x858
Type	Read-write
Reset	0x00000000
Width	32

3.3.249 err5addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank} Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x85C
Type	Read-write
Reset	0x00000000
Width	32

3.3.250 err5misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x860
Type	Read-write
Reset	0x00000000
Width	32

3.3.251 err5misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x864
Type	Read-write
Reset	0x00000000
Width	32

3.3.252 err5misc2

RAM Uncorrectable error counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x868
Type	Read-write
Reset	0x00000000
Width	32

3.3.253 err6fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6fr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x880
Type	Read-only
Reset	0x000009AA
Width	32

3.3.254 err6ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6ctlr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x888
Type	Read-only
Reset	0x00000000
Width	32

3.3.255 err6status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6status register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x890
Type	Read-write
Reset	0x000000
Width	32

3.3.256 err6addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x898
Type	Read-write
Reset	0x00000000
Width	32

3.3.257 err6addr1

Contains the physical CID and Rank broken out in the following way {[31:6] = Reserved, [5:3] = CID, [2:0] = Rank} Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x89C
Type	Read-write
Reset	0x00000000
Width	32

3.3.258 err6misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x8A0
Type	Read-write

Reset	0x00000000
Width	32

3.3.259 err6misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x8A4
Type	Read-write
Reset	0x00000000
Width	32

3.3.260 errgsr

This register shows the status of all the DMC error records. When a CFH, FH, or ER interrupt occurs software may check this register to tell which error record(s) caused the interrupt. Each field in this register is a copy of each individual records ERRnSTATUS.V bit. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The errgsr register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x920
Type	Read-write
Reset	0x00000000
Width	32

3.3.261 pmu_snapshot_req

Generates PMU snapshot request Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The pmu_snapshot_req register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA00
Type	Write-only
Reset	0x00000000
Width	32

3.3.262 pmu_snapshot_ack

Indicates PMU snapshot acknowledge Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_snapshot_ack register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA04
Type	Read-only
Reset	0x00000000
Width	32

3.3.263 pmu_overflow_status_clkdiv2

Indicates which clkdiv2 counters have overflowed Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_overflow_status_clkdiv2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA08
Type	Read-write
Reset	0x00000000
Width	32

3.3.264 pmu_overflow_status_clk

Indicates which clk domain counters have overflowed Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_overflow_status_clk register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA0C
Type	Read-write
Reset	0x00000000
Width	32

3.3.265 pmu_clkdiv2_counter_0_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA10
Type	Read-write
Reset	0x00000000
Width	32

3.3.266 pmu_clkdiv2_counter_0_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA14
Type	Read-write
Reset	0x00000000
Width	32

3.3.267 pmu_clkdiv2_counter_0_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA18
Type	Read-write
Reset	0x00000000
Width	32

3.3.268 pmu_clkdiv2_counter_0_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA1C
Type	Read-write
Reset	0x00000000
Width	32

3.3.269 pmu_clkdiv2_counter_0_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA20
Type	Read-write
Reset	0x00000000
Width	32

3.3.270 pmu_clkdiv2_counter_0_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_0_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA28
Type	Read-only
Reset	0x00000000
Width	32

3.3.271 pmu_clkdiv2_counter_0_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA30
Type	Read-write
Reset	0x00000000
Width	32

3.3.272 pmu_clkdiv2_counter_1_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA38
Type	Read-write
Reset	0x00000000
Width	32

3.3.273 pmu_clkdiv2_counter_1_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA3C
Type	Read-write
Reset	0x00000000
Width	32

3.3.274 pmu_clkdiv2_counter_1_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA40
Type	Read-write
Reset	0x00000000
Width	32

3.3.275 pmu_clkdiv2_counter_1_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA44
Type	Read-write
Reset	0x00000000
Width	32

3.3.276 pmu_clkdiv2_counter_1_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA48
Type	Read-write
Reset	0x00000000
Width	32

3.3.277 pmu_clkdiv2_counter_1_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_1_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA50
Type	Read-only
Reset	0x00000000
Width	32

3.3.278 pmu_clkdiv2_counter_1_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA58
Type	Read-write
Reset	0x00000000
Width	32

3.3.279 pmu_clkdiv2_counter_2_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA60
Type	Read-write
Reset	0x00000000
Width	32

3.3.280 pmu_clkdiv2_counter_2_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA64
Type	Read-write
Reset	0x00000000
Width	32

3.3.281 pmu_clkdiv2_counter_2_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA68
Type	Read-write
Reset	0x00000000
Width	32

3.3.282 pmu_clkdiv2_counter_2_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA6C
Type	Read-write
Reset	0x00000000
Width	32

3.3.283 pmu_clkdiv2_counter_2_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA70
Type	Read-write
Reset	0x00000000
Width	32

3.3.284 pmu_clkdiv2_counter_2_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_2_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA78
Type	Read-only
Reset	0x00000000
Width	32

3.3.285 pmu_clkdiv2_counter_2_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA80
Type	Read-write
Reset	0x00000000
Width	32

3.3.286 pmu_clkdiv2_counter_3_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA88
Type	Read-write
Reset	0x00000000
Width	32

3.3.287 pmu_clkdiv2_counter_3_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA8C
Type	Read-write
Reset	0x00000000
Width	32

3.3.288 pmu_clkdiv2_counter_3_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA90
Type	Read-write
Reset	0x00000000
Width	32

3.3.289 pmu_clkdiv2_counter_3_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA94
Type	Read-write
Reset	0x00000000
Width	32

3.3.290 pmu_clkdiv2_counter_3_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xA98
Type	Read-write
Reset	0x00000000
Width	32

3.3.291 pmu_clkdiv2_counter_3_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_3_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAA0
Type	Read-only
Reset	0x00000000
Width	32

3.3.292 pmu_clkdiv2_counter_3_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAA8
Type	Read-write
Reset	0x00000000
Width	32

3.3.293 pmu_clkdiv2_counter_4_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAB0
Type	Read-write
Reset	0x00000000
Width	32

3.3.294 pmu_clkdiv2_counter_4_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAB4
Type	Read-write
Reset	0x00000000
Width	32

3.3.295 pmu_clkdiv2_counter_4_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAB8
Type	Read-write
Reset	0x00000000
Width	32

3.3.296 pmu_clkdiv2_counter_4_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xABC
Type	Read-write
Reset	0x00000000
Width	32

3.3.297 pmu_clkdiv2_counter_4_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAC0
Type	Read-write
Reset	0x00000000
Width	32

3.3.298 pmu_clkdiv2_counter_4_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_4_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAC8
Type	Read-only
Reset	0x00000000
Width	32

3.3.299 pmu_clkdiv2_counter_4_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAD0
Type	Read-write
Reset	0x00000000
Width	32

3.3.300 pmu_clkdiv2_counter_5_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAD8
Type	Read-write
Reset	0x00000000
Width	32

3.3.301 pmu_clkdiv2_counter_5_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xADC
Type	Read-write
Reset	0x00000000
Width	32

3.3.302 pmu_clkdiv2_counter_5_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAE0
Type	Read-write
Reset	0x00000000
Width	32

3.3.303 pmu_clkdiv2_counter_5_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAE4
Type	Read-write
Reset	0x00000000
Width	32

3.3.304 pmu_clkdiv2_counter_5_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAE8
Type	Read-write
Reset	0x00000000
Width	32

3.3.305 pmu_clkdiv2_counter_5_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states.
Cannot be changed.

The pmu_clkdiv2_counter_5_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAF0
Type	Read-only
Reset	0x00000000
Width	32

3.3.306 pmu_clkdiv2_counter_5_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xAF8
Type	Read-write
Reset	0x00000000
Width	32

3.3.307 pmu_clkdiv2_counter_6_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB00
Type	Read-write
Reset	0x00000000
Width	32

3.3.308 pmu_clkdiv2_counter_6_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB04
Type	Read-write
Reset	0x00000000
Width	32

3.3.309 pmu_clkdiv2_counter_6_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB08
Type	Read-write
Reset	0x00000000
Width	32

3.3.310 pmu_clkdiv2_counter_6_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB0C
Type	Read-write
Reset	0x00000000
Width	32

3.3.311 pmu_clkdiv2_counter_6_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB10
Type	Read-write
Reset	0x00000000
Width	32

3.3.312 pmu_clkdiv2_counter_6_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_6_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB18
Type	Read-only
Reset	0x00000000
Width	32

3.3.313 pmu_clkdiv2_counter_6_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB20
Type	Read-write
Reset	0x00000000
Width	32

3.3.314 pmu_clkdiv2_counter_7_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB28
Type	Read-write
Reset	0x00000000
Width	32

3.3.315 pmu_clkdiv2_counter_7_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB2C
Type	Read-write
Reset	0x00000000
Width	32

3.3.316 pmu_clkdiv2_counter_7_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB30
Type	Read-write
Reset	0x00000000
Width	32

3.3.317 pmu_clkdiv2_counter_7_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB34
Type	Read-write
Reset	0x00000000
Width	32

3.3.318 pmu_clkdiv2_counter_7_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB38
Type	Read-write
Reset	0x00000000
Width	32

3.3.319 pmu_clkdiv2_counter_7_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_7_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB40
Type	Read-only
Reset	0x00000000
Width	32

3.3.320 pmu_clkdiv2_counter_7_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB48
Type	Read-write
Reset	0x00000000
Width	32

3.3.321 pmu_clk_counter_0_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB50
Type	Read-write
Reset	0x00000000
Width	32

3.3.322 pmu_clk_counter_0_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB54
Type	Read-write
Reset	0x00000000
Width	32

3.3.323 pmu_clk_counter_0_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB58
Type	Read-write
Reset	0x00000000
Width	32

3.3.324 pmu_clk_counter_0_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB5C
Type	Read-write
Reset	0x00000000
Width	32

3.3.325 pmu_clk_counter_0_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB60
Type	Read-write
Reset	0x00000000
Width	32

3.3.326 pmu_clk_counter_0_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clk_counter_0_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB68
Type	Read-only
Reset	0x00000000
Width	32

3.3.327 pmu_clk_counter_0_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB70
Type	Read-write
Reset	0x00000000
Width	32

3.3.328 pmu_clk_counter_1_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_mask_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB78
Type	Read-write
Reset	0x00000000
Width	32

3.3.329 pmu_clk_counter_1_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_mask_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB7C
Type	Read-write
Reset	0x00000000
Width	32

3.3.330 pmu_clk_counter_1_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_match_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB80
Type	Read-write
Reset	0x00000000
Width	32

3.3.331 pmu_clk_counter_1_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_match_63_32 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB84
Type	Read-write
Reset	0x00000000
Width	32

3.3.332 pmu_clk_counter_1_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_control register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB88
Type	Read-write
Reset	0x00000000
Width	32

3.3.333 pmu_clk_counter_1_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clk_counter_1_snapshot_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB90
Type	Read-only
Reset	0x00000000
Width	32

3.3.334 pmu_clk_counter_1_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_value_31_00 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xB98
Type	Read-write
Reset	0x00000000
Width	32

3.3.335 integ_cfg

Integration test register to enable integration test mode. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The integ_cfg register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xE00
Type	Read-write
Reset	0x00000000
Width	32

3.3.336 integ_outputs

Drives the value of outputs when in integration test mode. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG or LOW-POWER states.

The integ_outputs register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0xE08
Type	Write-only
Reset	0x00000000
Width	32

3.3.337 address_control_now

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1010
Type	Read-only
Reset	0x00030202
Width	32

3.3.338 decode_control_now

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, ie. row_order != bank_order != rank_order. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The decode_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1014
Type	Read-only
Reset	0x001A3000
Width	32

3.3.339 address_map_now

Configures the system address mapping options. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address_map_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x101C
Type	Read-only
Reset	0x00000000
Width	32

3.3.340 low_power_control_now

Configures the low-power features of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The low_power_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1020
Type	Read-only
Reset	0x00000020
Width	32

3.3.341 turnaround_control_now

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The turnaround_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1028
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Type	Read-only
Reset	0x0F0F0F0F
Width	32

3.3.342 hit_turnaround_control_now

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The hit_turnaround_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x102C
Type	Read-only
Reset	0x08909FBF
Width	32

3.3.343 qos_class_control_now

Configures the priority class for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qos_class_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1030
Type	Read-only
Reset	0x00000FC8
Width	32

3.3.344 escalation_control_now

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The escalation_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1034
Type	Read-only
Reset	0x00080F03
Width	32

3.3.345 qv_control_31_00_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1038
Type	Read-only
Reset	0x76543210
Width	32

3.3.346 qv_control_63_32_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x103C
Type	Read-only
Reset	0xFEDCBA98
Width	32

3.3.347 rt_control_31_00_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1040
Type	Read-only
Reset	0x00000000
Width	32

3.3.348 rt_control_63_32_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1044
Type	Read-only
Reset	0x00000000
Width	32

3.3.349 timeout_control_now

Configures the prescaler applied to timeout values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The timeout_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1048
Type	Read-only
Reset	0x00000001
Width	32

3.3.350 credit_control_now

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The credit_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x104C
Type	Read-only
Reset	0x00000F03
Width	32

3.3.351 write_priority_control_31_00_now

Configures the priority settings for write requests within the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write_priority_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1050
Type	Read-only
Reset	0x00000000
Width	32

3.3.352 write_priority_control_63_32_now

Configures the priority settings for write requests within the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write_priority_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1054
Type	Read-only
Reset	0x00000000
Width	32

3.3.353 queue_threshold_control_31_00_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue_threshold_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1058
Type	Read-only
Reset	0x00000008
Width	32

3.3.354 queue_threshold_control_63_32_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue_threshold_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x105C
Type	Read-only
Reset	0x00000000
Width	32

3.3.355 address_shutter_31_00_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1060
Type	Read-only
Reset	0x00000000
Width	32

3.3.356 address_shutter_63_32_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1064
Type	Read-only
Reset	0x00000000
Width	32

3.3.357 address_shutter_95_64_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_95_64_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1068
Type	Read-only
Reset	0x00000000
Width	32

3.3.358 address_shutter_127_96_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_127_96_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x106C
Type	Read-only
Reset	0x00000000
Width	32

3.3.359 address_shutter_159_128_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_159_128_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1070
Type	Read-only
Reset	0x00000000
Width	32

3.3.360 address_shutter_191_160_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_191_160_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1074
Type	Read-only
Reset	0x00000000
Width	32

3.3.361 memory_address_max_31_00_now

Configures the address space control for the DMC default region. Applies post address translation.
Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory_address_max_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1078
Type	Read-only
Reset	0x00000010
Width	32

3.3.362 memory_address_max_47_32_now

Configures the address space control for the DMC default region. Applies post address translation.
Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory_address_max_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x107C
Type	Read-only
Reset	0x00000000
Width	32

3.3.363 access_address_min0_31_00_now

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min0_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1080
Type	Read-only
Reset	0x00000000
Width	32

3.3.364 access_address_min0_47_32_now

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min0_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1084
Type	Read-only
Reset	0x00000000
Width	32

3.3.365 access_address_max0_31_00_now

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max0_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1088
Type	Read-only
Reset	0x00000000
Width	32

3.3.366 access_address_max0_47_32_now

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max0_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x108C
Type	Read-only
Reset	0x00000000
Width	32

3.3.367 access_address_min1_31_00_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min1_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1090
Type	Read-only
Reset	0x00000000
Width	32

3.3.368 access_address_min1_47_32_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min1_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1094
Type	Read-only
Reset	0x00000000
Width	32

3.3.369 access_address_max1_31_00_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max1_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1098
Type	Read-only
Reset	0x00000000
Width	32

3.3.370 access_address_max1_47_32_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max1_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x109C
Type	Read-only
Reset	0x00000000
Width	32

3.3.371 access_address_min2_31_00_now

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min2_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10A0
Type	Read-only
Reset	0x00000000
Width	32

3.3.372 access_address_min2_47_32_now

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min2_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10A4
Type	Read-only
Reset	0x00000000
Width	32

3.3.373 access_address_max2_31_00_now

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max2_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10A8
Type	Read-only
Reset	0x00000000
Width	32

3.3.374 access_address_max2_47_32_now

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max2_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10AC
Type	Read-only
Reset	0x00000000
Width	32

3.3.375 access_address_min3_31_00_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min3_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10B0
Type	Read-only
Reset	0x00000000
Width	32

3.3.376 access_address_min3_47_32_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min3_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10B4
Type	Read-only
Reset	0x00000000
Width	32

3.3.377 access_address_max3_31_00_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max3_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10B8
Type	Read-only
Reset	0x00000000
Width	32

3.3.378 access_address_max3_47_32_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max3_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10BC
Type	Read-only
Reset	0x00000000
Width	32

3.3.379 access_address_min4_31_00_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min4_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10C0
Type	Read-only
Reset	0x00000000
Width	32

3.3.380 access_address_min4_47_32_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min4_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10C4
Type	Read-only
Reset	0x00000000
Width	32

3.3.381 access_address_max4_31_00_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max4_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10C8
Type	Read-only
Reset	0x00000000
Width	32

3.3.382 access_address_max4_47_32_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max4_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10CC
Type	Read-only
Reset	0x00000000
Width	32

3.3.383 access_address_min5_31_00_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min5_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10D0
Type	Read-only
Reset	0x00000000
Width	32

3.3.384 access_address_min5_47_32_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min5_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10D4
Type	Read-only
Reset	0x00000000
Width	32

3.3.385 access_address_max5_31_00_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max5_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10D8
Type	Read-only
Reset	0x00000000
Width	32

3.3.386 access_address_max5_47_32_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max5_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10DC
Type	Read-only
Reset	0x00000000
Width	32

3.3.387 access_address_min6_31_00_now

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min6_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10E0
Type	Read-only
Reset	0x00000000
Width	32

3.3.388 access_address_min6_47_32_now

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min6_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10E4
Type	Read-only
Reset	0x00000000
Width	32

3.3.389 access_address_max6_31_00_now

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max6_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10E8
Type	Read-only
Reset	0x00000000
Width	32

3.3.390 access_address_max6_47_32_now

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max6_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10EC
Type	Read-only
Reset	0x00000000
Width	32

3.3.391 access_address_min7_31_00_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min7_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10F0
Type	Read-only
Reset	0x00000000
Width	32

3.3.392 access_address_min7_47_32_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min7_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10F4
Type	Read-only
Reset	0x00000000
Width	32

3.3.393 access_address_max7_31_00_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max7_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10F8
Type	Read-only
Reset	0x00000000
Width	32

3.3.394 access_address_max7_47_32_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max7_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x10FC
Type	Read-only
Reset	0x00000000
Width	32

3.3.395 dci_replay_type_now

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The dci_replay_type_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1110
Type	Read-only
Reset	0x00000002
Width	32

3.3.396 direct_control_now

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The direct_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1114
Type	Read-only
Reset	0x0003FFFF
Width	32

3.3.397 refresh_control_now

Configures the type of refresh commands issued by the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or PAUSED states.

The refresh_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1120
Type	Read-only
Reset	0x00000000
Width	32

3.3.398 memory_type_now

Configures the DMC for the attached memory type. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The memory_type_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1128
Type	Read-only
Reset	0x00000101
Width	32

3.3.399 scrub_control0_now

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub_control0_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1170
Type	Read-only
Reset	0x0FFFFFF00
Width	32

3.3.400 scrub_address_min0_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_min0_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1174
Type	Read-only
Reset	0x00000000
Width	32

3.3.401 scrub_address_max0_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_max0_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1178
Type	Read-only
Reset	0x00000000
Width	32

3.3.402 scrub_control1_now

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub_control1_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1180
Type	Read-only
Reset	0x0FFFFFF00
Width	32

3.3.403 scrub_address_min1_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_min1_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1184
Type	Read-only
Reset	0x00000000
Width	32

3.3.404 scrub_address_max1_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_max1_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1188
Type	Read-only
Reset	0x00000000
Width	32

3.3.405 cs_remap_control_31_00_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11A0
Type	Read-only

Reset 0x00020001
Width 32

3.3.406 cs_remap_control_63_32_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x11A4
Type Read-only
Reset 0x00080004
Width 32

3.3.407 cs_remap_control_95_64_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_95_64_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x11A8
Type Read-only
Reset 0x00200010
Width 32

3.3.408 cs_remap_control_127_96_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_127_96_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x11AC
Type Read-only
Reset 0x00800040
Width 32

3.3.409 cid_remap_control_31_00_now

Control register for dfi_CID remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid_remap_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11B0
Type	Read-only
Reset	0x20001000
Width	32

3.3.410 cid_remap_control_63_32_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid_remap_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11B4
Type	Read-only
Reset	0x00004000
Width	32

3.3.411 cke_remap_control_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cke_remap_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11C0
Type	Read-only
Reset	0x76543210
Width	32

3.3.412 rst_remap_control_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rst_remap_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11C4
Type	Read-only
Reset	0x76543210
Width	32

3.3.413 ck_remap_control_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The ck_remap_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11C8
Type	Read-only
Reset	0x76543210
Width	32

3.3.414 power_group_control_31_00_now

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke_remap_control register should belong to the same power-group Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11D0
Type	Read-only
Reset	0x00020001
Width	32

3.3.415 power_group_control_63_32_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11D4
Type	Read-only
Reset	0x00080004
Width	32

3.3.416 power_group_control_95_64_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_95_64_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11D8
Type	Read-only
Reset	0x00200010
Width	32

3.3.417 power_group_control_127_96_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_127_96_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11DC
Type	Read-only
Reset	0x00800040
Width	32

3.3.418 feature_control_now

Control register for DMC features. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The feature_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x11F0
Type	Read-only
Reset	0x0AA00000

Width 32

3.3.419 mux_control_now

Control muxing options for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The mux_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x11F4
Type Read-only
Reset 0x00000000
Width 32

3.3.420 rank_remap_control_now

Control register for rank remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rank_remap_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x11F8
Type Read-only
Reset 0x76543210
Width 32

3.3.421 t_refi_now

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_refi_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1200
Type Read-only
Reset 0x00090100
Width 32

3.3.422 t_rfc_now

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rfc_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1204
Type	Read-only
Reset	0x00008C23
Width	32

3.3.423 t_mrr_now

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_mrr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1208
Type	Read-only
Reset	0x00000002
Width	32

3.3.424 t_mrwnow

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_mrwnow register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x120C
Type	Read-only
Reset	0x0000000C

Width 32

3.3.425 refresh_enable_now

Configures refresh counters . Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The refresh_enable_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1210
Type Read-only
Reset 0x00000001
Width 32

3.3.426 t_rcd_now

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rcd_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1218
Type Read-only
Reset 0x00000005
Width 32

3.3.427 t_ras_now

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ras_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x121C
Type Read-only
Reset 0x0000000E
Width 32

3.3.428 t_rp_now

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rp_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1220
Type	Read-only
Reset	0x00000005
Width	32

3.3.429 t_rpall_now

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rpall_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1224
Type	Read-only
Reset	0x00000005
Width	32

3.3.430 t_rrd_now

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rrd_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1228
Type	Read-only
Reset	0x04000404
Width	32

3.3.431 t_act_window_now

Configures the tFAW and tMAWi timing parameters. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER, or PAUSED states.

The t_act_window_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x122C
Type	Read-only
Reset	0x03561414
Width	32

3.3.432 t_rtr_now

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), different chip-selects (t_rtr_cs), and same chip, different logical rank(t_rtr_dlr). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1234
Type	Read-only
Reset	0x10060404
Width	32

3.3.433 t_rtw_now

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_rtw_l), and other chip-selects (t_rtw_cs). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtw_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1238
Type	Read-only
Reset	0x00060606
Width	32

3.3.434 t_rtp_now

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtp_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x123C
Type	Read-only
Reset	0x00000004
Width	32

3.3.435 t_wr_now

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITES, to the same bank. Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: $t_wr(dmc) = CWL + 4 + tWR(\text{from dram data sheet})$. CWL should account for write CRC if enabled. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1244
Type	Read-only
Reset	0x00000005
Width	32

3.3.436 t_wtr_now

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs). Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: $t_wtr(dmc) = CWL + WBL/2 + tWR(\text{DRAM})$. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wtr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1248
Type	Read-only
Reset	0x00040505
Width	32

3.3.437 t_wtw_now

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes, same chip, different logical rank(t_wtw_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wtw_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x124C
Type	Read-only
Reset	0x10060404
Width	32

3.3.438 t_clock_control_now

Configures the enter DRAM clock disable timing parameter. This parameter is applied between stopping the clock when idle, or when in a power-down state, and any subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_clock_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1250
Type	Read-only
Reset	0x00000505
Width	32

3.3.439 t_xmpd_now

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xmpd_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1254
Type	Read-only
Reset	0x000003FF
Width	32

3.3.440 t_ep_now

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ep_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1258
Type	Read-only
Reset	0x00000002
Width	32

3.3.441 t_xp_now

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t_xpdll must be greater than or equal to tRCD and tCKE, and t_xp must be greater than or equal to tMPX_S. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xp_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x125C
Type	Read-only
Reset	0x00060002
Width	32

3.3.442 t_esr_now

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_esr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1260
Type	Read-only
Reset	0x0000000E
Width	32

3.3.443 t_xsr_now

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xsr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1264
Type	Read-only
Reset	0x05120100
Width	32

3.3.444 t_esrck_now

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_esrck_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1268
Type	Read-only
Reset	0x00000005
Width	32

3.3.445 t_ckxsr_now

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ckxsr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x126C
Type	Read-only
Reset	0x00000001
Width	32

3.3.446 t_cmd_now

Configures command signaling timing. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_cmd_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1270
Type	Read-only
Reset	0x00000000
Width	32

3.3.447 t_parity_now

Parity latencies t_parinlat and t_completion. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_parity_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1274
Type	Read-only
Reset	0x00000900
Width	32

3.3.448 t_zqcs_now

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_zqcs_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1278
Type	Read-only
Reset	0x00000040

Width 32**3.3.449 t_rw_odt_clr_now**

This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as tpoll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to t_odt_off_rd/wr(max setting) + DODTLoff(from DDR4 spec) Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rw_odt_clr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x127C
Type	Read-only
Reset	0x00000000
Width	32

3.3.450 t_rddata_en_now

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rddata_en_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1300
Type	Read-only
Reset	0x00000001
Width	32

3.3.451 t_phyrdlat_now

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_phyrdlat_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1304
---------------	--------

Type	Read-only
Reset	0x00000000
Width	32

3.3.452 t_phywrlat_now

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en, dfi_wrdata_cs and dfi_wrdata signals. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_phywrlat_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1308
Type	Read-only
Reset	0x00000001
Width	32

3.3.453 rdlvl_control_now

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1310
Type	Read-only
Reset	0x00001080
Width	32

3.3.454 rdlvl_mrs_now

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl_mrs_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1314
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Type	Read-only
Reset	0x00000004
Width	32

3.3.455 t_rdlvl_en_now

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rdlvl_en_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1318
Type	Read-only
Reset	0x00000000
Width	32

3.3.456 t_rdlvl_rr_now

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rdlvl_rr_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x131C
Type	Read-only
Reset	0x00000000
Width	32

3.3.457 wrlvl_control_now

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wrlvl_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1320
Type	Read-only
Reset	0x00101000
Width	32

3.3.458 wrlvl_mrs_now

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wrlvl_mrs_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1324
Type	Read-only
Reset	0x00000086
Width	32

3.3.459 t_wrlvl_en_now

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wrlvl_en_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1328
Type	Read-only
Reset	0x00000000
Width	32

3.3.460 t_wrlvl_ww_now

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wrlvl_ww_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x132C
Type	Read-only
Reset	0x00000000
Width	32

3.3.461 phy_power_control_now

Configures the low-power requests made to the PHY for the different channel states. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phy_power_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1348
Type	Read-only
Reset	0x00000000
Width	32

3.3.462 t_lpresp_now

Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_lpresp_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x134C
Type	Read-only
Reset	0x00000000
Width	32

3.3.463 phy_update_control_now

Configures the update mechanism to use in response to PHY training requests. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phy_update_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1350
Type	Read-only
Reset	0x2FE00000
Width	32

3.3.464 t_odth_now

Configures the ODT8 timing parameter as timed from Write command registered with ODT high
Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_odth_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1354
Type	Read-only
Reset	0x00000006
Width	32

3.3.465 odt_timing_now

Configures the ODT on and off timing. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_timing_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1358
Type	Read-only
Reset	0x06000600
Width	32

3.3.466 odt_wr_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_wr_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1360
Type	Read-only
Reset	0x08040201

Width 32

3.3.467 odt_wr_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_wr_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1364
Type	Read-only
Reset	0x80402010
Width	32

3.3.468 odt_rd_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_rd_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1368
Type	Read-only
Reset	0x00000000
Width	32

3.3.469 odt_rd_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_rd_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x136C
Type	Read-only
Reset	0x00000000
Width	32

3.3.470 dq_map_control_15_00_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_15_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1380
Type	Read-only
Reset	0x00000000
Width	32

3.3.471 dq_map_control_31_16_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_31_16_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1384
Type	Read-only
Reset	0x00000000
Width	32

3.3.472 dq_map_control_47_32_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_47_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1388
Type	Read-only

Reset 0x00000000
Width 32

3.3.473 dq_map_control_63_48_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_63_48_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x138C
Type Read-only
Reset 0x00000000
Width 32

3.3.474 dq_map_control_71_64_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_71_64_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1390
Type Read-only
Reset 0x00000000
Width 32

3.3.475 odt_cp_control_31_00_now

Determines which of the 8 dfi_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_cp_control_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x13B0

Type	Read-only
Reset	0x08040201
Width	32

3.3.476 odt_cp_control_63_32_now

Determines which of the 8 dfi_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_cp_control_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x13B4
Type	Read-only
Reset	0x80402010
Width	32

3.3.477 user_config0_now

Drives the output user_config0 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user_config0_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1408
Type	Read-only
Reset	0x00000000
Width	32

3.3.478 user_config1_now

Drives the output user_config1 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user_config1_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x140C
Type	Read-only
Reset	0x00000000
Width	32

3.3.479 t_db_train_resp_now

Configures the t_db_train_resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi_db_train_resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi_rddata_valid) to define the delay between DFI read command and when the response is valid on the dfi_rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_db_train_resp_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1610
Type	Read-only
Reset	0x00000000
Width	32

3.3.480 t_lvl_disconnect_now

Configures the t_lvl_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t*lvl_disconnect and t*lvl_disconnect_error timing parameters from the PHY Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_lvl_disconnect_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1614
Type	Read-only
Reset	0x0000000F
Width	32

3.3.481 wdqlvl_control_now

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1620
Type	Read-only

Reset	0x00000094
Width	32

3.3.482 wdqlvl_vrefdq_train_mrs_now

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the wdqlvl_control register. You enable this function with the wdqlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_vrefdq_train_mrs_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1624
Type	Read-only
Reset	0x00000000
Width	32

3.3.483 wdqlvl_address_31_00_now

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_address_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1628
Type	Read-only
Reset	0x00000000
Width	32

3.3.484 wdqlvl_address_63_32_now

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_address_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x162C
Type	Read-only
Reset	0x00000000

Width 32

3.3.485 t_wdqlvl_en_now

Configures the t_wdqlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wdqlvl_en, the delay between asserting dfi_wdqlvl_en and the first training command, the delay between de-asserting dfi_wdqlvl_en and de-asserting ODT, and de-asserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_en_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1630
Type	Read-only
Reset	0x00000000
Width	32

3.3.486 t_wdqlvl_ww_now

Configures the t_wdqlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wdqlvl_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_ww_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1634
Type	Read-only
Reset	0x00000000
Width	32

3.3.487 t_wdqlvl_rw_now

Configures the t_wdqlvl_rw timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_rw_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1638
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Type	Read-only
Reset	0x00000000
Width	32

3.3.488 **phymstr_control_now**

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phymstr_control_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1654
Type	Read-only
Reset	0x00000000
Width	32

3.3.489 **periph_id_4**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_4 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FD0
Type	Read-only
Reset	0x00000014
Width	32

3.3.490 **periph_id_0**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FE0
Type	Read-only
Reset	0x00000054
Width	32

3.3.491 **periph_id_1**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FE4
Type	Read-only
Reset	0x000000B4
Width	32

3.3.492 **periph_id_2**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FE8
Type	Read-only
Reset	0x0000000B
Width	32

3.3.493 **periph_id_3**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_3 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FEC
Type	Read-only
Reset	0x00000000
Width	32

3.3.494 **component_id_0**

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_0 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FF0
Type	Read-only
Reset	0x0000000D
Width	32

3.3.495 component_id_1

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_1 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FF4
Type	Read-only
Reset	0x000000F0
Width	32

3.3.496 component_id_2

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_2 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FF8
Type	Read-only
Reset	0x00000005
Width	32

3.3.497 component_id_3

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_3 register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1FFC
Type	Read-only
Reset	0x000000B1
Width	32

Appendix A

Signal descriptions

This appendix describes the DMC-620 signals.

It contains the following section:

- [A.1 Signals list on page Appx-A-210.](#)

A.1 Signals list

DMC signals list that excludes bus interface signals. The bus interface signals are defined by their own bus protocol standard.

The following table shows the Primary clock and reset signals bus list of the DMC.

Table A-1 DMC Primary clock and reset signals list

Name	Width	Description
clk		Primary DMC clock
resetn		Primary DMC reset

The following table shows the Divided Primary DMC clock. Edge Synchronous, half the frequency of clk bus list of the DMC.

Table A-2 DMC Divided Primary DMC clock. Edge Synchronous, half the frequency of clk list

Name	Width	Description
clkdiv2		Primary DMC clock. Edge Synchronous, half the frequency of clk
resetn		Primary DMC reset

The following table shows the APB clock and reset signals bus list of the DMC.

Table A-3 DMC APB clock and reset signals list

Name	Width	Description
pclk		APB clock
presetn		APB reset

The following table shows the APB Interface bus list of the DMC.

Table A-4 DMC APB Interface list

Name	Width	Description
paddr	32	APB address
psel		APB select
penable		APB enable
pwrite		APB write
pwwdata	32	APB write data
pready		APB ready
prdata	32	APB read data
pslverr		APB error signal

The following table shows the DFI Interface bus list of the DMC.

Table A-5 DMC DFI Interface list

Name	Width	Description
dfi_address_p0	18	Address to DDR3 PHY
dfi_address_p1	18	Address to DDR3 PHY
dfi_bank_p0	3	Bank Address to PHY
dfi_bank_p1	3	Bank Address to PHY
dfi_ras_n_p0	1	Row address strobe to PHY
dfi_ras_n_p1	1	Row address strobe to PHY
dfi_cas_n_p0	1	Column address strobe to PHY
dfi_cas_n_p1	1	Column address strobe to PHY
dfi_we_n_p0	1	Write enable to PHY
dfi_we_n_p1	1	Write enable to PHY
dfi_cs_p0	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_cs_p1	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_act_n_p0	1	Activate to PHY
dfi_act_n_p1	1	Activate to PHY
dfi_bg_p0	2	Bank group address to PHY
dfi_bg_p1	2	Bank group address to PHY
dfi_cid_p0	3	Chip ID to PHY
dfi_cid_p1	3	Chip ID to PHY
dfi_cke_p0	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_cke_p1	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_odt_p0	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_odt_p1	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_reset_n_p0	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_reset_n_p1	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_parity_in_p0	1	Command parity to PHY
dfi_parity_in_p1	1	Command parity to PHY
dfi_wrdata_en_p0	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_en_p1	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_p0	(DFI_DATA_BITS/2)	Write data to PHY
dfi_wrdata_p1	(DFI_DATA_BITS/2)	Write data to PHY
dfi_wrdata_cs_p0	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_cs_p1	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_mask_p0	(DFI_DATA_BYTES/2)	Write data mask PHY
dfi_wrdata_mask_p1	(DFI_DATA_BYTES/2)	Write data mask PHY
dfi_rddata_en_p0	(DFI_DATA_SLICES)	Enable for read data

Table A-5 DMC DFI Interface list (continued)

Name	Width	Description
dfi_rddata_en_p1	(DFI_DATA_SLICES)	Enable for read data
dfi_rddata_p0	(DFI_DATA_BITS/2)	Read data input from PHY
dfi_rddata_p1	(DFI_DATA_BITS/2)	Read data input from PHY
dfi_rddata_dbi_p0	(DFI_DATA_SLICES*2)	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.
dfi_rddata_dbi_p1	(DFI_DATA_SLICES*2)	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.
dfi_rddata_valid_p0	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_valid_p1	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_cs_p0	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_rddata_cs_p1	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_ctrlupd_req	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_ctrlupd_ack	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phyupd_req	1	DFI PHY-initiated update request
dfi_phyupd_ack	1	DFI PHY-initiated update acknowledge
dfi_phyupd_type	2	DFI PHY-initiated update type
dfi_data_byte_disable	(DFI_DATA_BYTES/2)	This signal is part of DFI 4.0, see DFI specification for details.
dfi_dram_clk_disable	MEMORY_CHIP_SELECTS	DRAM clock disable to PHY
dfi_init_start	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_init_complete	1	Indicates PHY initialization complete
dfi_alert_n_p0	1	This signal is part of DFI 4.0, see JEDEC specification for details.
dfi_alert_n_p1	1	This signal is part of DFI 4.0, see JEDEC specification for details.
dfi_frequency	5	This signal is part of DFI 4.0, see DFI specification for details.
dfi_geardown_en	1	This signal is part of DFI 4.0 Geardown Interface.
dfi_err	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_err_info	4	This signal is part of DFI 4.0, see DFI specification for details.
dfi_disconnect_error	1	Provides Disconnect type if a disconnect occurs on training, update, or PHY-master interface. This signal is part of DFI 4.0 Disconnect Interface.
dfi_phymstr_req	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_cs_state	MEMORY_CHIP_SELECTS	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_state_sel	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_type	2	This signal is part of DFI 4.0, see DFI specification for details.

Table A-5 DMC DFI Interface list (continued)

Name	Width	Description
dfi_phymstr_ack	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phylvl_req_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see DFI specification for details.
dfi_phylvl_ack_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see DFI specification for details.
dfi_rdlvl_req	DFI_DATA_SLICES	DFI read data eye training request
dfi_rdlvl_cs	MEMORY_CHIP_SELECTS	DFI read data eye training request target chip-select
dfi_rdlvl_en	DFI_DATA_SLICES	DFI read data eye training enable
dfi_rdlvl_resp	(DFI_DATA_SLICES*2)	DFI read data eye training response
dfi_rdlvl_done	DFI_DATA_SLICES	DFI Read data eye training done
dfi_rdlvl_gate_req	DFI_DATA_SLICES	DFI read gate training request
dfi_rdlvl_gate_cs	MEMORY_CHIP_SELECTS	DFI read gate training request target chip-select
dfi_rdlvl_gate_en	DFI_DATA_SLICES	DFI read gate training enable
dfi_wrlvl_req	DFI_DATA_SLICES	DFI write leveling training request
dfi_wrlvl_cs	MEMORY_CHIP_SELECTS	DFI write leveling training request target chip-select
dfi_wrlvl_en	DFI_DATA_SLICES	DFI write leveling training enable
dfi_wrlvl_strobe_p0	DFI_DATA_SLICES	DFI write leveling training strobe
dfi_wrlvl_strobe_p1	DFI_DATA_SLICES	DFI write leveling training strobe
dfi_wrlvl_resp	DFI_DATA_SLICES	DFI write leveling training response
dfi_wdqlvl_req	DFI_DATA_SLICES	DFI Write-DQ leveling training request
dfi_wdqlvl_cs	MEMORY_CHIP_SELECTS	DFI Write-DQ leveling training request target chip-select
dfi_wdqlvl_en	DFI_DATA_SLICES	DFI Write-DQ leveling training enable
dfi_wdqlvl_result	DFI_DATA_SLICES	DFI Write-DQ leveling training result
dfi_wdqlvl_done	DFI_DATA_SLICES	DFI Write-DQ leveling training done
dfi_wdqlvl_resp	(DFI_DATA_SLICES*2)	DFI Write-DQ leveling training response
dfi_lvl_pattern	4	This signal is part of DFI 4.0, see DFI specification for details.
dfi_lvl_periodic	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_db_train_en	DFI_DATA_SLICES	Enable for DB-DRAM Training. This signal is part of DFI 4.0 DB-DRAM Training.
dfi_db_train_resp_w0	(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)	Response data for DB-DRAM Training. This signal is part of DFI 4.0.
dfi_db_train_resp_w1	(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)	Response data for DB-DRAM Training. This signal is part of DFI 4.0.
dfi_lp_ctrl_req	1	DFI command low-power request
dfi_lp_data_req	1	DFI data low-power request
dfi_lp_wakeup	4	DFI command low-power PHY wakeup allowance
dfi_lp_ack	1	DFI command low-power acknowledge

The following table shows the Q-Channel Interface for DMC bus list of the DMC.

Table A-6 DMC Q-Channel Interface for DMC list

Name	Width	Description
qreqn	1	Request from the external clock controller to prepare to stop the clock
qacceptn	1	Positive acknowledgement after receiving QREQn assertion indicating that the DMC has completed preparation to stop the clocks and that the external clock controller can stop the clock
qdeny	1	Negative acknowledgement after receiving QREQn assertion indicating that the DMC has refused the request from the external clock controller to prepare to stop the clock
qactive	1	Indication that the DMC is active

The following table shows the Q-Channel Interface for APB interface bus list of the DMC.

Table A-7 DMC Q-Channel Interface for APB interface list

Name	Width	Description
qreqn_apb	1	Request from the external clock controller to prepare to stop the clock
qacceptn_apb	1	Positive acknowledgement after receiving QREQn assertion indicating that the APB interface has completed preparation to stop the clocks and that the external clock controller can stop the clock
qdeny_apb	1	Negative acknowledgement after receiving QREQn assertion indicating that the APB interface has refused the request from the external clock controller to prepare to stop the clock
qactive_apb	1	Indication that the APB interface is active

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-8 DMC Clock Frequency Change Interface list

Name	Width	Description
cc_frequency	5	Used to indicate new frequency as part of frequency change protocol
cc_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
cc_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-9 DMC Clock Frequency Change Interface list

Name	Width	Description
dfi_frequency	5	Used to indicate new frequency as part of frequency change protocol
dfi_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
dfi_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Abort Interface bus list of the DMC.

Table A-10 DMC Abort Interface list

Name	Width	Description
abort_req	1	An input to abort retries in the face of DFI link errors.
abort_err_type	1	Abort Error Type as a payload to abort_req.
abort_ack	1	An output to acknowledge that the DMC has completed outstanding transactions as a result of an abort.

The following table shows the Memory BIST interface bus list of the DMC.

Table A-11 DMC Memory BIST interface list

Name	Width	Description
mbistresetsn	1	MBIST reset. Active low.
mbistreq	1	MBIST request
mbistack	1	MBIST acknowledge
mbistwriteen	1	MBIST write enable
mbistreaden	1	MBIST read enable
mbistaddr	MAX_TID_BITS	MBIST address
mbistarray	4	MBIST array selection
mbistcfg	1	MBIST Configuration
mbistindata	154	MBIST write data
mbistoutdata	154	MBIST read data

The following table shows the DFT interface bus list of the DMC.

Table A-12 DMC DFT interface list

Name	Width	Description
DFTCLKCGEN	1	DFT clock gate override
DFTRSTDISABLE	2	DFT reset synchronizer disable
DFTRAMHOLD	1	DFT on-chip RAM hold
DFTMCPHOLD	1	DFT multicycle path hold

The following table shows the user-defined inputs bus list of the DMC.

Table A-13 DMC user-defined inputs list

Name	Width	Description
user_status	32	User-defined inputs

The following table shows the user-defined outputs bus list of the DMC.

Table A-14 DMC user-defined outputs list

Name	Width	Description
user_config0	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

Table A-15 DMC user-defined outputs list

Name	Width	Description
user_config1	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

Table A-16 DMC user-defined outputs list

Name	Width	Description
user_config2	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

Table A-17 DMC user-defined outputs list

Name	Width	Description
user_config3	32	User-defined outputs

The following table shows the Direct command event trigger inputs bus list of the DMC.

Table A-18 DMC Direct command event trigger inputs list

Name	Width	Description
direct_cmd_event_in	4	Direct command event trigger inputs

The following table shows the Direct command event triggered outputs bus list of the DMC.

Table A-19 DMC Direct command event triggered outputs list

Name	Width	Description
direct_cmd_event_out	4	Direct command event triggered outputs

The following table shows the memory_type bus list of the DMC.

Table A-20 DMC memory_type list

Name	Width	Description
memory_type	3	An external output of the value of the memory_type register bitfield.

The following table shows the Tie-off value to set the value of CMOD in the periph_id_3 bitfield bus list of the DMC.

Table A-21 DMC Tie-off value to set the value of CMOD in the periph_id_3 bitfield list

Name	Width	Description
user_periph_id_3	8	Tie-off value to set the value of CMOD in the periph_id_3 bitfield

The following table shows the Tie-off value for reset of register bitfield t_rddata_en_diff bus list of the DMC.

Table A-22 DMC Tie-off value for reset of register bitfield t_rddata_en_diff list

Name	Width	Description
t_rddata_en_diff_tie_off	6	Tie-off value for reset of register bitfield t_rddata_en_diff

The following table shows the Tie-off value for reset of register bitfield t_phyrdcslat bus list of the DMC.

Table A-23 DMC Tie-off value for reset of register bitfield t_phyrdcslat list

Name	Width	Description
t_phyrdcslat_tie_off	5	Tie-off value for reset of register bitfield t_phyrdcslat

The following table shows the Tie-off value for reset of register bitfield t_phyrdlat bus list of the DMC.

Table A-24 DMC Tie-off value for reset of register bitfield t_phyrdlat list

Name	Width	Description
t_phyrdlat_tie_off	7	Tie-off value for reset of register bitfield t_phyrdlat

The following table shows the Tie-off value for reset of register bitfield t_phywrlat_diff bus list of the DMC.

Table A-25 DMC Tie-off value for reset of register bitfield t_phywrlat_diff list

Name	Width	Description
t_phywrlat_diff_tie_off	5	Tie-off value for reset of register bitfield t_phywrlat_diff

The following table shows the Tie-off value for reset of register bitfield t_phywrcslat bus list of the DMC.

Table A-26 DMC Tie-off value for reset of register bitfield t_phywrcslat list

Name	Width	Description
t_phywrcslat_tie_off	5	Tie-off value for reset of register bitfield t_phywrcslat

The following table shows the Tie-off value for reset of register bitfield t_phywrdata bus list of the DMC.

Table A-27 DMC Tie-off value for reset of register bitfield t_phywrdata list

Name	Width	Description
t_phywrdata_tie_off	1	Tie-off value for reset of register bitfield t_phywrdata

The following table shows the Tie-off value for reset of register bitfield refresh_dur_rdlvl bus list of the DMC.

Table A-28 DMC Tie-off value for reset of register bitfield refresh_dur_rdlvl list

Name	Width	Description
refresh_dur_rdlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_rdlvl

The following table shows the Tie-off value for reset of register bitfield t_rdlvl_en bus list of the DMC.

Table A-29 DMC Tie-off value for reset of register bitfield t_rdlvl_en list

Name	Width	Description
t_rdlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_rdlvl_en

The following table shows the Tie-off value for reset of register bitfield t_rdlvl_rr bus list of the DMC.

Table A-30 DMC Tie-off value for reset of register bitfield t_rdlvl_rr list

Name	Width	Description
t_rdlvl_rr_tie_off	10	Tie-off value for reset of register bitfield t_rdlvl_rr

The following table shows the Tie-off value for reset of register bitfield refresh_dur_wrlvl bus list of the DMC.

Table A-31 DMC Tie-off value for reset of register bitfield refresh_dur_wrlvl list

Name	Width	Description
refresh_dur_wrlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl

The following table shows the Tie-off value for reset of register bitfield t_wrlvl_en bus list of the DMC.

Table A-32 DMC Tie-off value for reset of register bitfield t_wrlvl_en list

Name	Width	Description
t_wrlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_wrlvl_en

The following table shows the Tie-off value for reset of register bitfield t_wrlvl_ww bus list of the DMC.

Table A-33 DMC Tie-off value for reset of register bitfield t_wrlvl_ww list

Name	Width	Description
t_wrlvl_ww_tie_off	10	Tie-off value for reset of register bitfield t_wrlvl_ww

The following table shows the Tie-off value for reset of register bitfield refresh_dur_wrlvl bus list of the DMC.

Table A-34 DMC Tie-off value for reset of register bitfield refresh_dur_wrlvl list

Name	Width	Description
refresh_dur_wdqlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_ww bus list of the DMC.

Table A-35 DMC Tie-off value for reset of register bitfield t_wdqlvl_ww list

Name	Width	Description
t_wdqlvl_ww_tie_off	10	Tie-off value for reset of register bitfield t_wdqlvl_ww

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_rw bus list of the DMC.

Table A-36 DMC Tie-off value for reset of register bitfield t_wdqlvl_rw list

Name	Width	Description
t_wdqlvl_rw_tie_off	10	Tie-off value for reset of register bitfield t_wdqlvl_rw

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_en bus list of the DMC.

Table A-37 DMC Tie-off value for reset of register bitfield t_wdqlvl_en list

Name	Width	Description
t_wdqlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_wdqlvl_en

The following table shows the Tie-off value for reset of register bitfield refresh_dur_phymstr bus list of the DMC.

Table A-38 DMC Tie-off value for reset of register bitfield refresh_dur_phymstr list

Name	Width	Description
refresh_dur_phymstr_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_phymstr

The following table shows the Tie-off value for reset of register bitfield t_db_train_resp bus list of the DMC.

Table A-39 DMC Tie-off value for reset of register bitfield t_db_train_resp list

Name	Width	Description
t_db_train_resp_tie_off	7	Tie-off value for reset of register bitfield t_db_train_resp

The following table shows the Tie-off value for reset of register bitfield t_lpresp bus list of the DMC.

Table A-40 DMC Tie-off value for reset of register bitfield t_lpresp list

Name	Width	Description
t_lpresp_tie_off	6	Tie-off value for reset of register bitfield t_lpresp

The following table shows the Tie-off value for reset of register bitfield user_config0 bus list of the DMC.

Table A-41 DMC Tie-off value for reset of register bitfield user_config0 list

Name	Width	Description
user_config0_tie_off	32	Tie-off value for reset of register bitfield user_config0

The following table shows the Tie-off value for reset of register bitfield user_config1 bus list of the DMC.

Table A-42 DMC Tie-off value for reset of register bitfield user_config1 list

Name	Width	Description
user_config1_tie_off	32	Tie-off value for reset of register bitfield user_config1

The following table shows the Tie-off value for reset of register bitfield user_config2 bus list of the DMC.

Table A-43 DMC Tie-off value for reset of register bitfield user_config2 list

Name	Width	Description
user_config2_tie_off	32	Tie-off value for reset of register bitfield user_config2

The following table shows the Tie-off value for reset of register bitfield user_config3 bus list of the DMC.

Table A-44 DMC Tie-off value for reset of register bitfield user_config3 list

Name	Width	Description
user_config3_tie_off	32	Tie-off value for reset of register bitfield user_config3

The following table shows the Tie-off value to set the physical node ID of the DMC bus list of the DMC.

Table A-45 DMC Tie-off value to set the physical node ID of the DMC list

Name	Width	Description
system_id	CHI_RSP_FLIT_SRCID_WIDTH	Tie-off value to set the physical node ID of the DMC

The following table shows the Tie off value to specify the concatenated physical node IDs of up to SYSTEM_REQUESTORS Home Nodes that are permitted to access the DMC. SYSTEM_REQUESTORS is 8 when configured as DMC_CHIB==0, and is 32 when configured as DMC_CHIB==1. Bus list of the DMC.

Table A-46 DMC Tie off value to specify the concatenated physical node IDs list

Name	Width	Description
home_node_id	(CHI_REQ_FLIT_SRCID_WIDTH*SYSTEM_REQUESTORS)	Tie off value to specify the concatenated physical node IDs of the requestors that are permitted to access the DMC

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring bus list of the DMC.

Table A-47 DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring list

Name	Width	Description
dfi_rdlvl_periodic	1	Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring bus list of the DMC.

Table A-48 DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring list

Name	Width	Description
dfi_rdlvl_gate_periodic	1	Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring bus list of the DMC.

Table A-49 DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring list

Name	Width	Description
dfi_wrlvl_periodic	1	Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring bus list of the DMC.

Table A-50 DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring list

Name	Width	Description
dfi_wdqlvl_periodic	1	Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring

The following table shows the interrupt signal list of the DMC.

Table A-51 DMC interrupts list

Name	Width	Description
er_int	1	The DMC has detected an uncorrectable error or previously poisoned data that cannot be deferred
cfh_int	1	The number of correctable errors detected by the DMC has overflowed an error counter
fh_int	1	The DMC has detected a new (non-poisoned) data failure that cannot be corrected, but might be able to be deferred
failed_access_int	1	The DMC has detected a system request that has failed a permissions check
failed_prog_int	1	The DMC has detected a programming request that is not permitted
link_err_int	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun
temperature_event_int	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor
arch_fsm_int	1	The DMC has detected a change in the architectural state
scrub_engine0_complete_int	1	The DMC scrub engine 0 has completed a scrub
scrub_engine1_complete_int	1	The DMC scrub engine 1 has completed a scrub
scrub_engine_behind_schedule_int	1	A DMC scrub engine is behind schedule
phy_request_int	1	The DMC has detected a PHY request
combined_int	1	A combined interrupt that is the logical OR of the other interrupts
failed_access_owflow	1	The DMC has detected a system request that has failed a permissions check and a previously detected assertion was not cleared
failed_prog_owflow	1	The DMC has detected a programming request that is not permitted and a previously detected assertion was not cleared
link_err_owflow	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun and a previously detected assertion was not cleared
temperature_event_owflow	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor and a previously detected assertion was not cleared

Table A-51 DMC interrupts list (continued)

Name	Width	Description
arch_fsm_oflow	1	The DMC has detected a change in the architectural state and a previously detected assertion was not cleared
scrub_engine0_complete_oflow	1	The DMC scrub engine 0 has completed a scrub and a previously detected assertion was not cleared
scrub_engine1_complete_oflow	1	The DMC scrub engine 1 has completed a scrub and a previously detected assertion was not cleared
scrub_engine_behind_schedule_oflow	1	A DMC scrub engine is behind schedule and a previously detected assertion was not cleared
phy_request_oflow	1	The DMC has detected a PHY request and a previously detected assertion was not cleared
combined_oflow	1	A combined interrupt that is the logical OR of the other interrupt overflows.
pmu_counter_oflow	1	An interrupt that indicates at least one PMU counter has overflowed

Appendix B

Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- [B.1 Revisions on page Appx-B-224](#).

B.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue 0000-00

Change	Location	Affects
First release	-	All revisions.

Table B-2 Differences between issue 0000-00 and issue 0000-01

Change	Location	Affects
No technical changes.	-	All revisions.

Table B-3 Differences between issue 0000-01 and issue 0000-02

Change	Location	Affects
No technical changes.	-	All revisions.

Table B-4 Differences between issue 0000-02 and issue 0100-00

Change	Location	Affects
Updated Configurable options.	1.5 Configurable options on page 1-16	r1p0.
Product revisions have been updated for r1p0.	1.8 Product revisions on page 1-20	r1p0.
References to CHI-C support have been added.	<ul style="list-style-type: none"> 1.2 DMC-620 compliance on page 1-13 1.3 Features on page 1-14 1.4 Interfaces on page 1-15 	r1p0.