ARM Embedded Trace Macrocell CoreSight™ ETM™-A5

Product Revision r0

Software Developers Errata Notice

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- the document title
- the document number, ARM-EPM-027734
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Release Information

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text in Chapter 2. Fixed errata are not shown as updated unless the erratum text has changed. The summary table in section 2.2 identifies errata that have been fixed in each product revision.

04 Oct 2012: Changes in Document v1

Page	Status	ID	Cat	Rare	Summary of Erratum
7	New	732696	CatB		Timestamp may be incomplete after reprogramming
8	New	744829	CatB		ETM can generate corrupt trace when timestamping is enabled
9	New	771119	CatC		ETMSR[1] might be set when ETM is not empty

Contents

Chapter 1.
Introduction

This chapter introduces the errata notice for the ARM CoreSight ETM-A5 Embedded Trace Macrocell

1.1. Scope of this document

This document describes errata categorized by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

This document describes errata that may impact anyone who is developing software that will run on implementations of this ARM product.

1.2. Categorization of errata

Errata recorded in this document are split into the following levels of severity:

Table 1 Categorization of errata

Errata Type	Definition
Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A(rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B(rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Chapter 2.
Errata Descriptions

2.1. Product Revision Status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

2.2. Revisions Affected

Table 2 below lists the product revisions affected by each erratum. A cell marked with **X** indicates that the erratum affects the revision shown at the top of that column.

This document includes errata that affect revision r0 only.

Refer to the reference material supplied with your product to identify the revision of the IP.

Table 2 Revisions Affected

ID	Cat	Rare	Summary of Erratum	r0p0	r0p1	r0p2
744829	CatB		ETM can generate corrupt trace when timestamping is enabled	X	X	X
732696	CatB		Timestamp may be incomplete after reprogramming	X		
771119	CatC		ETMSR[1] might be set when ETM is not empty	X	X	X

2.3. Category A

There are no errata in this category

2.4. Category A (Rare)

There are no errata in this category

2.5. Category B

732696: Timestamp may be incomplete after reprogramming

Category B
Products Affected: CoreSight ETM-A5.
Present in: r0p0

Description

ETM-A5 can be configured to insert timestamp packets in the trace stream.

The ETMv3.5 architecture requires that a full timestamp packet is inserted at a convenient point after the programming bit is cleared.

As a result of this erratum a partial rather than full timestamp packet may be output when programming bit is cleared for the second or subsequent times after the ETM-A5 is reset. This will mean that it will not be possible to determine the upper bits of the timestamp packet until the next full timestamp packet is output.

Conditions

The following sequence must occur:

1) The ETM is enabled with the Timestamping enable bit, Register 0x0 (Main Control Register) bit [28], set.
2) The ETM is disabled by setting the Programming bit, Register 0x0 (Main Control Register) bit [10].
3) The ETM-A5 is re-enabled by clearing the Programming bit, with the Timestamping enable bit set.

Implications

If a partial timestamp is output following the clearing of the programming bit, it will not be possible to determine the upper bits of the timestamp packet until the next full timestamp packet is output.

Trace is not corrupted.

Workaround

These workarounds are for users or tool vendors.

To mitigate the impact of the erratum, increase the synchronisation frequency. This will mean that synchronisation points resulting in the generation of a full timestamp packet will occur more frequently.

To prevent this erratum from occurring, reset the ETM following a trace session before reprogramming.

744829: ETM can generate corrupt trace when timestamping is enabled

Category B

Products Affected: CoreSight ETM-A5.

Present in: r0p0, r0p1, r0p2

Description

The ETM-A5 macrocell can generate corrupt trace when timestamping is enabled, caused by a conflict between prioritizing timestamp packets and alignment synchronization (A-sync) packets. On rare occasions, this can occur when trace restarts after a gap in the trace.

The correct behaviour is to output a timestamp packet, followed by an A-sync packet, followed by an I-sync packet. Because of this erratum, the ETM outputs a timestamp packet, followed by up to 6 bytes of corrupt data, followed by an I-sync packet.

The quantity of corrupt data depends upon the size of the timestamp packet as shown in the following table:

Timestamp packet size	Number of corrupt bytes
2	6
3	6
4	6
5	6
6	5
7	4
8	3
9	2
10	1

In all cases, the final byte of corrupt data has the value 0x80.

Conditions

All of the following conditions must occur:

- The ETM is enabled with the Timestamping enable bit set (bit [28] of register 0x0, ETMCR - Main Control Register)
- There is a gap in the trace, either because trace is being filtered or because the ETM internal trace buffer overflows
- A timestamp is output on the same cycle as trace restarts after the gap

Timestamps are output for a number of reasons, such a periodic synchronization, external synchronization requests, and timestamp events.

Implications

The trace cannot be analysed until the next A-Sync packet is output. This erratum also causes another synchronization request to occur, meaning another A-Sync packet will appear soon after the corrupt data. This should minimise the amount of trace data which is corrupted.

Workaround

If Timestamping is enabled there is no workaround to prevent the erratum. However, it is possible to determine if the erratum has occurred when analysing the trace stream because the last corrupt byte is 0x80, this byte is a known distance from the timestamp packet, and this byte is always followed by an I-Sync packet. When analysing the trace stream, if the last byte of the possibly corrupt data after a timestamp is not 0x80, or the byte after the last byte of possibly corrupt data is not an I-Sync header, then the erratum has not occurred.

2.6. Category B (Rare)

There are no errata in this category

2.7. Category C

771119: ETMSR[1] might be set when ETM is not empty

Category C

Products Affected: CoreSight ETM-A5.

Present in: r0p0, r0p1, r0p2

Description

The ETM-A5 macrocell includes a status register bit (ETMSR[1]) which indicates the state of the trace unit following a request to disable the ETM functions, made by writing to the programming bit in the control register (ETMCR[10]). One function of the programming bit is to disable the trace port and to empty the FIFO. Due to this erratum, this does not occur correctly if the ATB interface is operated at a lower clock frequency than the ETM using the clock-enable signal ATCLKEN.

Configurations Affected

To be affected by this erratum, all of the following must apply:

- The ETM-A5 macrocell must be used in a system where the ATB clock, ATCLK, is synchronous to the ETM-A5 clock CLK
- The ATCLK frequency is lower than the ETM-A5 clock frequency and the ATCLKEN signal is used to synchronise the trace interface to the ETM-A5 clock domain

Conditions

1) The programming bit in ETMCR is set using the APB interface
2) The associated programming bit is read from the ETMSR as 1

Implications

The following data items can be observed on the ATB interface after the ETMSR programming bit indicates that the ETM is empty:

- An item of trace data which had left the FIFO before ETMCR[10] was set but was stalled on the ATB interface
- A trigger event generated in the cycle in which the FIFO became empty

In both these cases the pending data or trigger is correctly written out to the ATB interface.

Workaround

There is no workaround for this erratum.