

Application Note **102**

ETM Multiplexing Modes

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Application Note 102 ETM Multiplexing Modes

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Release information

The following changes have been made to this Application Note.

Change history

Date	Issue	Change
September 2002	A	First release

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1 Introduction

Trace documentation introduces the concept of multiplexing. This document describes the different multiplexing options that are available, providing an illustration and a brief overview of each. For simplicity, only four trace packet lines are used in these diagrams

NOTE: The term *Multiplexing* is NOT used here to describe sharing of pins such as GPIO with trace output, these descriptions assume that, if shared, the pins are currently used to provide trace data.

1.1 Table of supported configurations

The following configurations are supported:

Configuration	MultiTrace 1.0	Third party TPAs
Normal mode	Yes	Yes
MultiTrace Multiplexing	Yes	Contact vendor
ETM Multiplexing	Yes (using downloadable patch)	Contact vendor
Demultiplexed mode	No	Contact vendor
Half-rate clocking	Yes	Contact vendor

2 Description of Supported Configurations

The following sections provide a brief overview of each of the configurations listed in the previous table.

2.1 Normal mode – no multiplexing

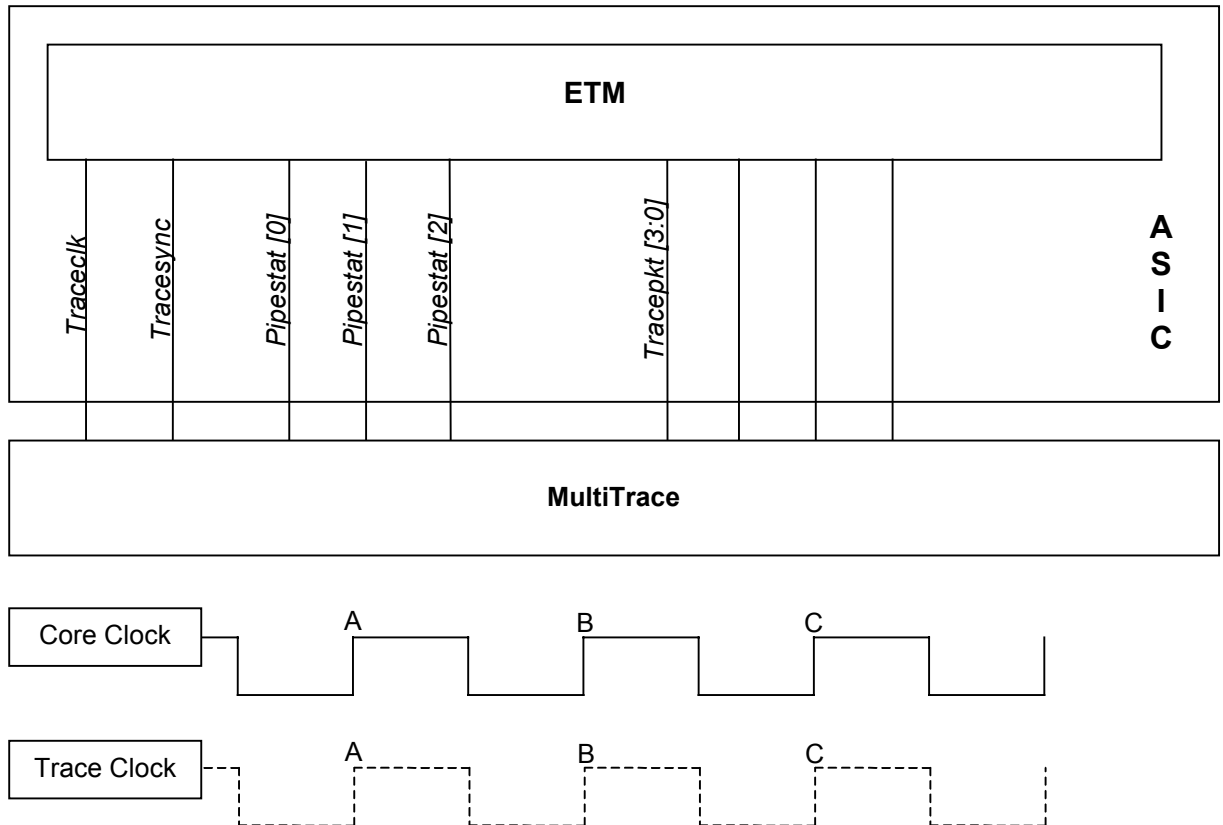


Figure 2-1 Normal mode – No Multiplexing

Standard tracing configuration. Trace clock driven directly by the core clock. Trace information is sampled on the rising edge of each clock cycle (A, B & C).

2.2 MultiTrace multiplexing

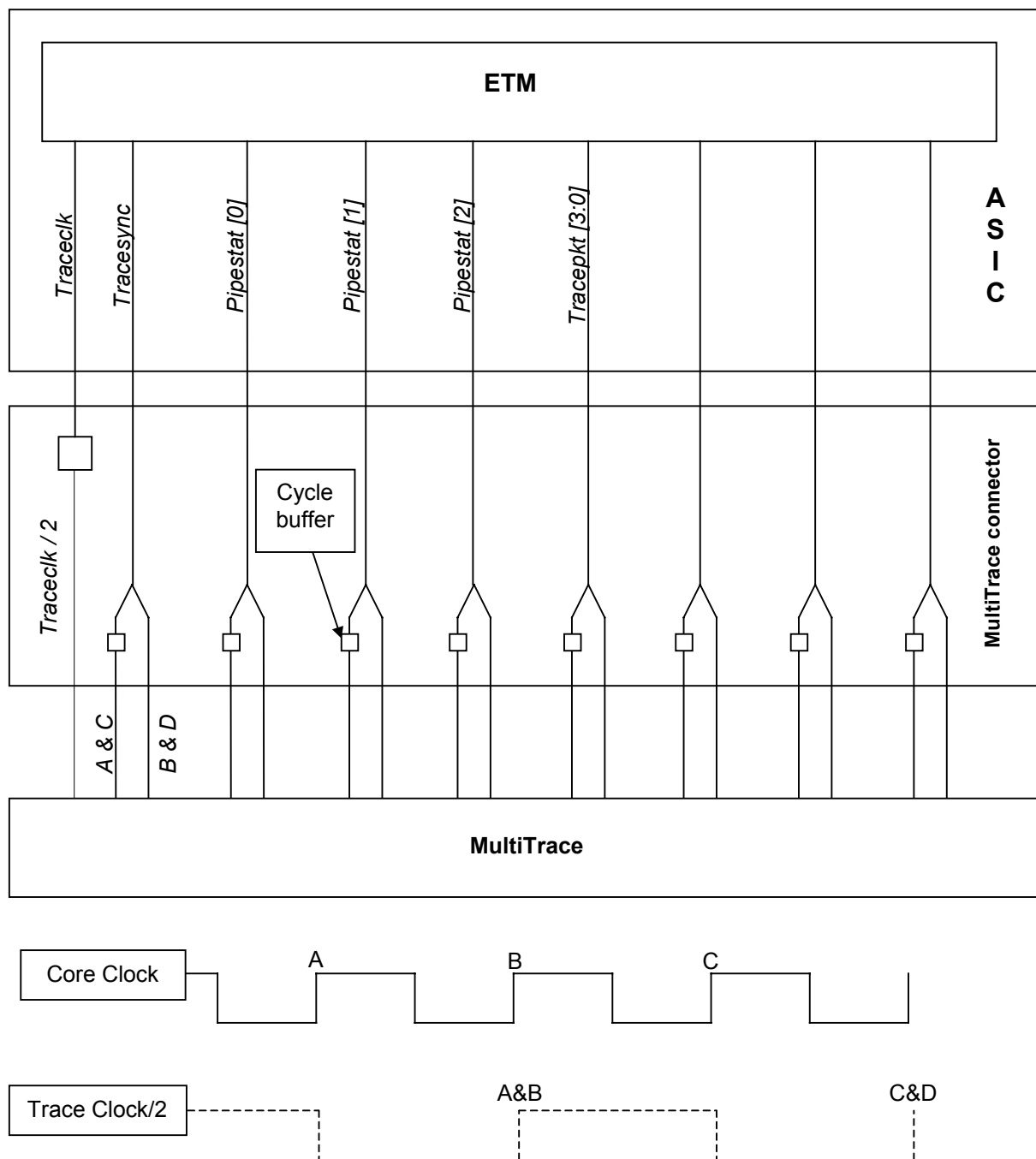


Figure 2.2 MultiTrace Multiplexing.

The MultiTrace MICTOR connector houses circuitry which divides the signals from the ETM. Data collected at point A is held in a buffer here. At point B the next set of data arrives at the MultiTrace connector. All data is now transferred to the MultiTrace unit. Therefore twice as much data is sent, but only half as often.

This allows the core to be clocked at higher speeds (and effectively double the data to be transferred as each transfer uses 1 'line' of MultiTrace memory).

It has the drawback that timestamps are less accurate. Both events A & B will have the same timestamp.

With 4-bit width tracing MultiTrace can also perform 4-way multiplexing using *traceclk/4*.

2.3 ETM multiplexing

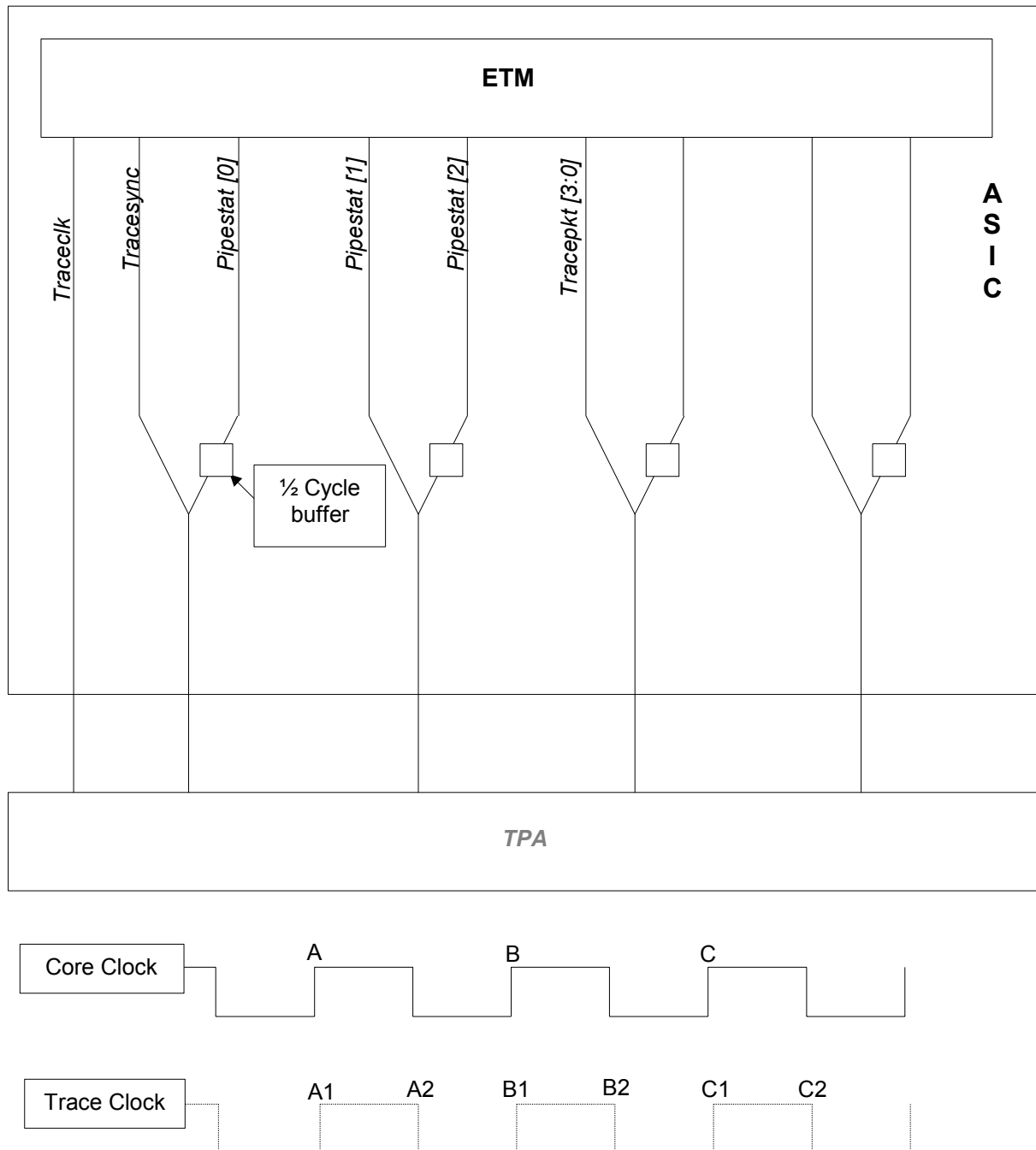


Figure 2.3 ETM Multiplexing.

The aim here is to reduce the number of pins required for transferring data out from the ETM. To achieve this half of the required signals are delayed for half a cycle. The first half are transmitted on the rising clock edge, then the remainder is transferred on the falling clock edge

This of course requires the TPA to be capable of receiving data at very high speeds on both clock edges.

This mode of multiplexing is supported by patched versions of MultiTrace

2.4 Demultiplexed mode (MultiTrace multiplexing onboard the ASIC)

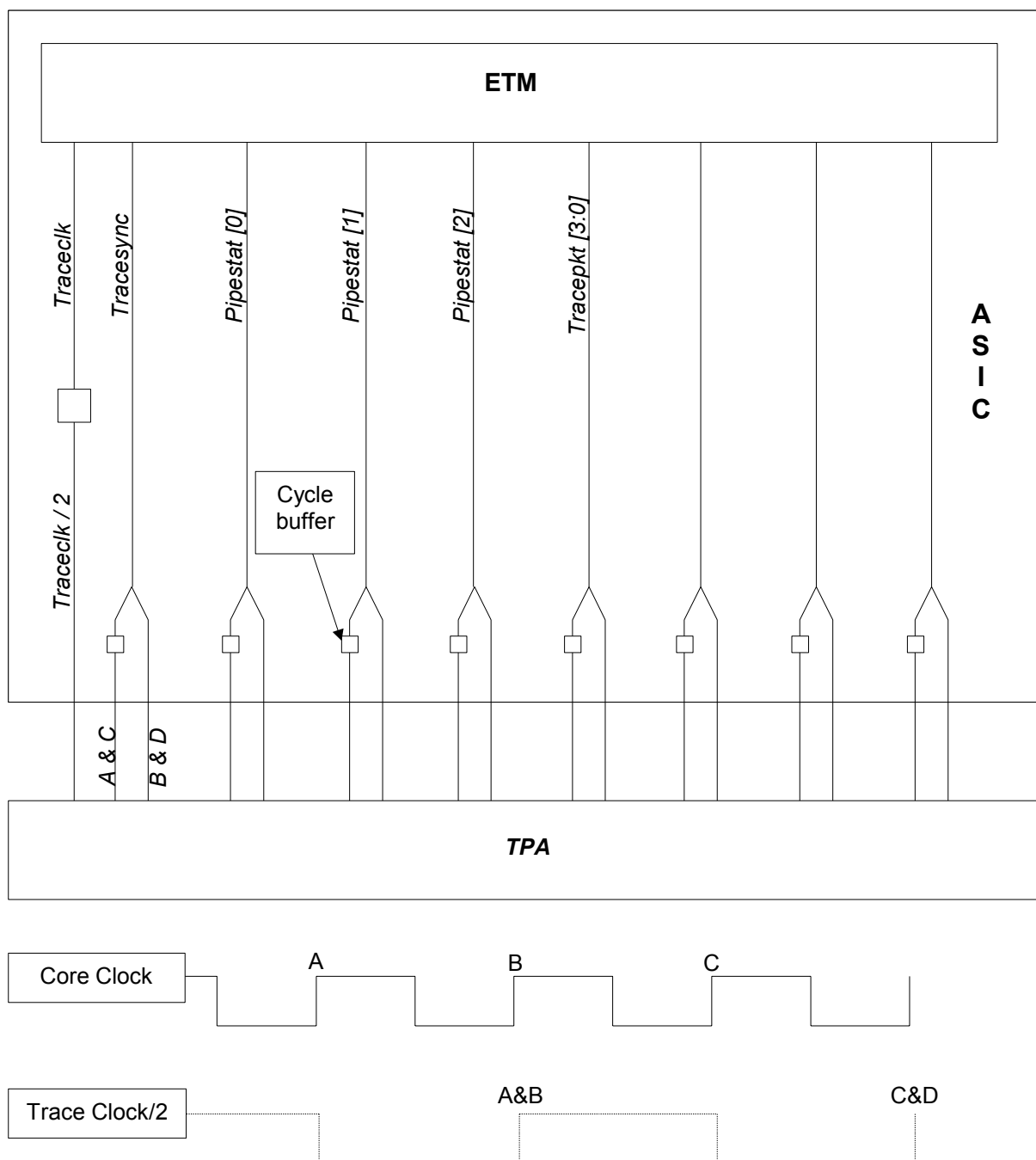


Figure 2.4 Demultiplexed mode.

This is essentially MultiTrace multiplexing performed onboard the ASIC.

MultiTrace does not support demultiplexed trace capture.

Physical limitations of the MICTOR connector mean that for 8 or 16-bit width output a second connector is required.

2.5 Half-rate clocking

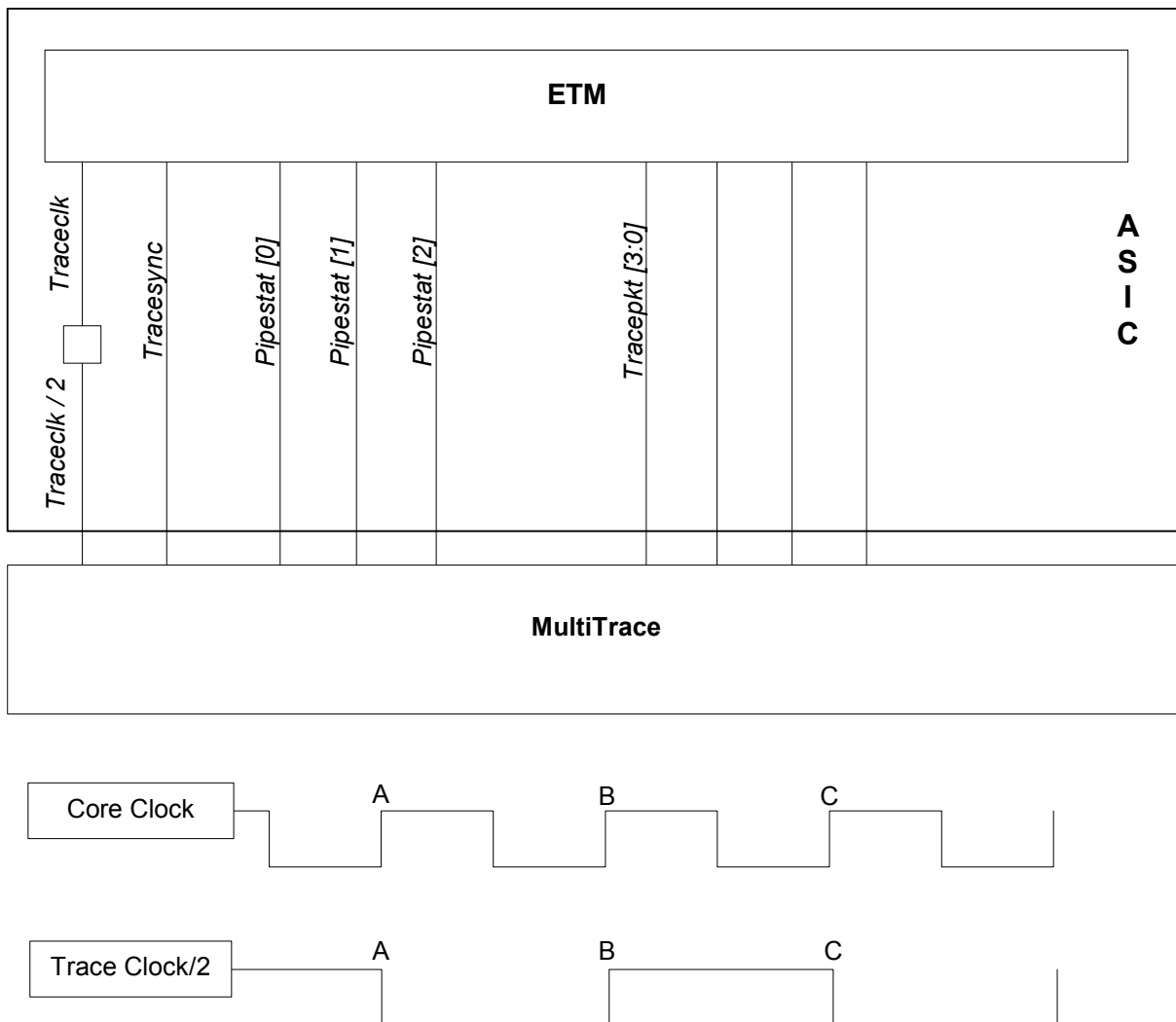


Figure 2.5 Half-rate clocking

This is not actually multiplexing, but is a feature that is worth mentioning here.

Data is transferred at the same rate as standard tracing configuration. Here the trace clock signal is halved and trace data appears on the rising and falling edge of 'traceclock/2'. This removes the overhead of a high frequency pad to output the full-rate trace clock. The high frequency signal is not needed. A signal of half the frequency will suffice.

MultiTrace supports this functionality.

This feature can also be seen in operation as part of demultiplexing.