

PrimeCell® AMBA 3 AXI TrustZone Memory Adapter (BP141) Cycle Model

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User Guide



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Preface

A Cycle Model component is a library developed from ARM intellectual property (IP) that is generated through Cycle Model Studio™. The Cycle Model then can be used within a virtual platform tool, for example, SoC Designer.

About This Guide

This guide provides all the information needed to configure and use the Cycle Model in SoC Designer.

Audience

This guide is intended for experienced hardware and software developers who create components for use with SoC Designer. You should be familiar with the following products and technology:

- SoC Designer
- Hardware design verification
- Verilog or SystemVerilog programming language

Conventions

This guide uses the following conventions:

Convention	Description	Example
<code>courier</code>	Commands, functions, variables, routines, and code examples that are set apart from ordinary text.	<code>sparseMem_t SparseMemCreateNew();</code>
<i>italic</i>	New or unusual words or phrases appearing for the first time.	<i>Transactors</i> provide the entry and exit points for data ...
bold	Action that the user performs.	Click Close to close the dialog.
<text>	Values that you fill in, or that the system automatically supplies.	<platform>/ represents the name of various platforms.
[text]	Square brackets [] indicate optional text.	\$CARBON_HOME/bin/modelstudio [<filename>]
[text1 text2]	The vertical bar indicates “OR,” meaning that you can supply text1 or text 2.	\$CARBON_HOME/bin/modelstudio [<name>.symtab.db <name>.ccfg]

Also note the following references:

- References to C code implicitly apply to C++ as well.
- File names ending in .cc, .cpp, or .cxx indicate a C++ source file.

Further reading

This section lists related publications. The following publications provide information that relate directly to SoC Designer:

- *SoC Designer Installation Guide*
- *SoC Designer User Guide*
- *SoC Designer Standard Component Library Reference Manual*

The following publications provide reference information about ARM® products:

- *AMBA 3 AHB-Lite Overview*
- *AMBA Specification (Rev 2.0)*
- *AMBA AHB Transaction Level Modeling Specification*
- *Architecture Reference Manual*

See <http://infocenter.arm.com/help/index.jsp> for access to ARM documentation.

The following publications provide additional information on simulation:

- IEEE 1666™ SystemC Language Reference Manual, (IEEE Standards Association)
- SPIRIT User Guide, Revision 1.2, SPIRIT Consortium.

Glossary

AMBA	<i>Advanced Microcontroller Bus Architecture</i> . The ARM open standard on-chip bus specification that describes a strategy for the interconnection and management of functional blocks that make up a System-on-Chip (SoC).
AHB	<i>Advanced High-performance Bus</i> . A bus protocol with a fixed pipeline between address/control and data phases. It only supports a subset of the functionality provided by the AMBA AXI protocol.
APB	<i>Advanced Peripheral Bus</i> . A simpler bus protocol than AXI and AHB. It is designed for use with ancillary or general-purpose peripherals such as timers, interrupt controllers, UARTs, and I/O ports.
AXI	<i>Advanced eXtensible Interface</i> . A bus protocol that is targeted at high performance, high clock frequency system designs and includes a number of features that make it very suitable for high speed sub-micron interconnect.
Cycle Model	A software object created by the Cycle Model Studio (or <i>Cycle Model Compiler</i>) from an RTL design. The Cycle Model contains a cycle- and register-accurate model of the hardware design.
Cycle Model Studio	Graphical tool for generating, validating, and executing hardware-accurate software models. It creates a Cycle Model, and it also takes a Cycle Model as input and generates a component that can be used in SoC Designer, Platform Architect, or Accellera SystemC for simulation.
CASI	<i>ESL API Simulation Interface</i> , is based on the SystemC communication library and manages the interconnection of components and communication between components.
CADI	<i>ESL API Debug Interface</i> , enables reading and writing memory and register values and also provides the interface to external debuggers.
CAPI	<i>ESL API Profiling Interface</i> , enables collecting historical data from a component and displaying the results in various formats.
Component	Building blocks used to create simulated systems. Components are connected together with unidirectional transaction-level or signal-level connections.
ESL	<i>Electronic System Level</i> . A type of design and verification methodology that models the behavior of an entire system using a high-level language such as C or C++.
HDL	<i>Hardware Description Language</i> . A language for formal description of electronic circuits, for example, Verilog.
RTL	<i>Register Transfer Level</i> . A high-level hardware description language (HDL) for defining digital circuits.
SoC Designer	High-performance, cycle accurate simulation framework which is targeted at System-on-a-Chip hardware and software debug as well as architectural exploration.
SystemC	SystemC is a single, unified design and verification language that enables verification at the system level, independent of any detailed hardware and software implementation, as well as enabling co-verification with RTL design.
Transactor	<i>Transaction adaptors</i> . You add transactors to your component to connect your component directly to transaction level interface ports for your particular platform.

Chapter 1

Using the Cycle Model in SoC Designer

This chapter describes the functionality of the Cycle Model component, and how to use it in SoC Designer. It contains the following sections:

- [TZMA BP141 Cycle Model Functionality](#)
- [Adding and Configuring the SoC Designer Component](#)
- [Available Component ESL Ports](#)
- [Setting Component Parameters](#)
- [Debug Features](#)
- [Available Profiling Data](#)

1.1 TZMA BP141 Cycle Model Functionality

The PrimeCell TrustZone Memory Adapter (TZMA) is an AMBA compliant System-on-Chip peripheral. The TZMA enables a single physical memory cell of up to 2MB to be shared between a secure and a non-secure partition. The size of the partitions is controlled by the configurations of the BP141 and by a single input to the BP141 component.

The BP141 routes transactions according to:

1. the memory regions that they are attempting to access.
2. their security mode.

This section provides a summary of the functionality of the Cycle Model compared to that of the hardware. For details of the functionality of the hardware that the Cycle Model simulates, refer to the ARM PrimeCell Infrastructure AMBA 3 AXI TrustZone Memory Adapter (BP141) Technical Overview.

- [Fully Functional Features](#)
- [Unsupported Hardware Features](#)
- [Features Additional to the Hardware](#)

1.1.1 Fully Functional Features

The following features of the TZMA BP141 hardware implementation are fully implemented in the BP141 TZMA Cycle Model.

- it is compatible with the AXI internal memory interface BP140
- it has a configuration input that can be driven from the TrustZone Protection Controller (TZPC) or tied off as required
- supports a single active read and a single active write transaction
- there is no low-power interface
- it does not provide exclusive access monitoring
- it can be configured with the following:
 - data width of 32 or 64 bits
 - ID width of 1 to 32 bits
 - addressable memory size of up to 2MB

1.1.2 Unsupported Hardware Features

The following features of the TZMA BP141 hardware are not implemented in the BP141 TZMA Cycle Model:

- SCAN control related signals are not supported in the Cycle Model: SCANENABLE, SCANINPCLK, and SCANOUTPCLK.

1.1.3 Features Additional to the Hardware

The following features that are implemented in the TZMA BP141 Cycle Model to enhance usability do not exist in the TrustZone Memory Adapter (BP141) hardware:

- The Data width, ID width, and TZMEMSIZE can be adjusted by changing the value of the component parameters.

1.2 Adding and Configuring the SoC Designer Component

The following topics briefly describe how to use the component. See the *SoC Designer User Guide* (ARM DUI 0956) for more information.

- [SoC Designer Component Files](#)
- [Adding the Cycle Model to the Component Library](#)
- [Adding the Component to the SoC Designer Canvas](#)

1.2.1 SoC Designer Component Files

The component files are the final output from the Cycle Model Studio compile and are the input to SoC Designer Plus. There are two versions of the component; an optimized release version for normal operation, and a debug version.

On Linux the debug version of the component is compiled without optimizations and includes debug symbols for use with gdb. The release version is compiled without debug information and is optimized for performance.

On Windows the debug version of the component is compiled referencing the debug runtime libraries, so it can be linked with the debug version of SoC Designer Plus. The release version is compiled referencing the release runtime library. Both release and debug versions generate debug symbols for use with the Visual C++ debugger on Windows.

The provided component files are listed below:

Table 1-1 SoC Designer Component Files

Platform	File	Description
Linux	maxlib.lib<component_name>.conf	SoC Designer configuration file
	lib<component_name>.mx.so	SoC Designer component runtime file
	lib<component_name>.mx_DBG.so	SoC Designer component debug file
Windows	maxlib.lib<component_name>.win-dows.conf	SoC Designer configuration file
	lib<component_name>.mx.dll	SoC Designer component runtime file
	lib<component_name>.mx_DBG.dll	SoC Designer component debug file

Additionally, this User Guide PDF file is provided with the component.

1.2.2 Adding the Cycle Model to the Component Library

The compiled Cycle Model component is provided as a configuration file (.conf). To make the component available in the Component Window in SoC Designer Canvas, perform the following steps:

1. Launch SoC Designer Canvas.
2. From the File menu, select **Preferences**.
3. Click on **Component Library** in the list on the left.
4. Under the Additional Component Configuration Files window, click **Add**.
5. Browse to the location where the SoC Designer Cycle Model is located and select the component configuration file:
 - maxlib.lib<component_name>.conf (for Linux)
 - maxlib.lib<component_name>.windows.conf (for Windows)
6. Click **OK**.
7. To save the preferences permanently, click the **OK & Save** button.

The component is now available from the SoC Designer Component Window.

1.2.3 Adding the Component to the SoC Designer Canvas

Locate the component in the Component Window and drag it out to the Canvas.

1.3 Available Component ESL Ports

Table 1-2 describes the ESL ports that are exposed in SoC Designer Plus. See the *ARM PrimeCell AMBA 3 AXI TrustZone Memory Adapter (BP141) Technical Overview* for more information.

Table 1-2 ESL Component Ports

ESL Port	Description	Direction	Type
axi_s axi_m	AXI slave and master ports.	slave master	AXI
ARESETn	Input reset. Reset port for receiving reset signal.	Input	Signal slave
clk-in	Input clock. This component can be connected to the clock master. If it is unconnected, it is implicitly connected to the system master clock.	Input	Clock slave
R0SIZE	Input that sets the size (in 4KB units) of the secure region.	Input	Signal slave

All pins that are not listed in this table have been either tied or disconnected for performance reasons.

1.3.1 AXI Transaction Slave/Master Interfaces

The axi_s port and the axi_m port are AXI transaction ports. The axi_m port is normally connected to a memory component. The data width of both ports is set by a component parameter. The ID width is set by a second parameter. See [Setting Component Parameters](#) for more information about these parameters.

1.4 Setting Component Parameters

You can change the settings of all the component parameters in SoC Designer Canvas, and of some of the parameters in SoC Designer Simulator. To modify the Cycle Model parameters:

1. In the Canvas, right-click on the Cycle Model and select **Edit Parameters....** You can also double-click the component. The Edit Parameters dialog box appears.
2. In the Parameters window, double-click the **Value** field of the parameter that you want to modify.
3. If it is a text field, type a new value in the Value field. If a menu choice is offered, select the desired option. The parameters are described in Table 1-3.

Table 1-3 Component Parameters

Name	Description	Allowed Values	Default Value	Runtime ¹
Align Waveforms	When set to true, waveforms dumped from the component are aligned with the SoC Designer simulation time. The reset sequence, however, is not included in the dumped data. When set to false, the reset sequence is dumped to the waveform data, however, the component time is not aligned with the SoC Designer time.	true, false	true	No
ARESETn	Specifies the value used for the ARESETn input if it is left disconnected.	0,1	1	Yes
axi_s Enable Debug Messages axi_m Enable Debug Messages	Whether debug messages are logged for the axi_s and axi_m ports.	true, false	false	Yes
Carbon DB Path	Sets the directory path to the database file.	Not Used	empty	No
Data width	Sets the width of the data paths for axi_s and axi_m.	32,64	64	No
Dump Waveforms	Whether SoC Designer dumps waveforms for this component.	true, false	false	Yes
Enable Debug Messages	Enable or disable the capture of debug messages.	true, false	false	Yes
ID width	Sets the width of the ID signals within the axi_s and axi_m ports.	1-32	4	No
R0SIZE	The value that is used for the R0SIZE input if it is left disconnected. ²	0x0-0x200	0x0	Yes
TZMEMSIZE	The size of total addressable memory measured in 4KB units. ³	0x0-0x200	0x200	No
Waveform File ⁴	Name of the waveform file.	string	arm_cm_BP141.vcd	No

Table 1-3 Component Parameters (continued)

Name	Description	Allowed Values	Default Value	Runtime ¹
Waveform Format	Sets the format of the waveform file.	VCD, FSDB	VCD	No
Waveform Timescale	Sets the timescale to be used in the waveform.	Many values in drop-down	1 ns	No

1. Yes means the parameter can be dynamically changed during simulation, No means it can be changed only when building the system, Reset means it can be changed during simulation, but its new value will be taken into account only at the next reset.
2. The R0SIZE parameter, as well as the R0SIZE input represent an address measured in 4KB units, thus 0x200 represents an address of 2MB.
3. The TZMEMSIZE parameter, represent a value measured in 4KB units, thus 0x200 represents a memory size of 2MB.
4. When enabled, SoC Designer writes accumulated waveforms to the waveform file in the following situations: when the waveform buffer fills, when validation is paused and when validation finishes, and at the end of each validation run.

1.5 Debug Features

The TZMA BP141 Cycle Model contains no special debug features or internal registers.

1.6 Available Profiling Data

The TZMA BP141 Cycle Model has no profiling capabilities.