ARM ETM
CoreSight™ ETM9™ r0 (TM910)
Errata Notice

This document contains all errata known at the date of issue in CoreSight ETM9 r0 releases up to and including revision r0p1 of CoreSight ETM9

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General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- a unique defect tracking identifier
- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1	Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.
Category 2	Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.
Category 3	Behavior that was not the originally intended behavior but should not cause any problems in applications.
Implementation	Errata that are of particular interest to those implementing the product and that have no software implications.

Change Control

24 May 2007: Changes in Document v5

Page	Status	ID	Cat	Summary
31	New	435286	Cat 3	Address Comparators might behave incorrectly while processor is halted in debug
33	New	436732	Cat 3	CPRT View Data filtering is inaccurate under rare conditions
35	New	439043	Imp	PCLKEN input to ETM9CSSingle might cause timing closure failures

27 Mar 2007: Changes in Document revision 4.0

Page	Status	ID	Cat	Summary
14	Updated	388999	Cat 2	ETM FIFO might not empty when setting the programming bit
15	New	401255	Cat 2	Address Comparator might not match on non-word-aligned instruction address
16	New	401320	Cat 2	AFREADYM signal might not be asserted
18	New	401323	Cat 2	Accesses to ATCLK registers can cause APB interface to lockup
20	New	408625	Cat 2	A-Sync packet might not be output when trace is enabled
22	New	425210	Cat 2	Trigger might not occur
29	New	417671	Cat 3	PCLKENDBG not used on writes to Claim Tag registers
27	New	409114	Cat 3	ETMJTAGPORT behaves incorrectly when simultaneous JTAG and APB transactions occur
30	New	425217	Cat 3	Multiple trigger requests might occur

22 May 2006: Changes in Document revision 3.0

Page	Status	ID	Cat	Summary
11	Updated	354112	Cat 2	ATCLK registers might return incorrect value
13	New	388738	Cat 2	Toggling of NIDEN and DBGEN might cause incorrect trace
14	New	388999	Cat 2	ETM FIFO might not empty when setting the programming bit
25	New	389003	Cat 3	Lock Access can be modified when PADDRDBG31 is HIGH
26	New	389487	Cat 3	Even numbered Single Address Comparators incorrectly match when a data abort occurs

22 Aug 2005: Changes in Document revision 2.0

Page	Status	ID	Cat	Summary
24	New	350998	Cat 3	Writes to counter value register might cause counter event to fire immediately
11	New	354112	Cat 2	ATCLK registers might return incorrect value
12	New	356598	Cat 2	Register reads via ETM JTAG Port might return incorrect values

08 Feb 2005: Changes in Document revision 1.0

No Errata in this document revision

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus X indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r0p1
354112	Cat 2	ATCLK registers might return incorrect value	X	
356598	Cat 2	Register reads via ETM JTAG Port might return incorrect values	X	
388738	Cat 2	Toggling of NIDEN and DBGEN might cause incorrect trace	X	
388999	Cat 2	ETM FIFO might not empty when setting the programming bit	X	
401255	Cat 2	Address Comparator might not match on non-word-aligned instruction address	X	
401320	Cat 2	AFREADYM signal might not be asserted	X	
401323	Cat 2	Accesses to ATCLK registers can cause APB interface to lockup	X	
408625	Cat 2	A-Sync packet might not be output when trace is enabled	X	
425210	Cat 2	Trigger might not occur	X	
350998	Cat 3	Writes to counter value register might cause counter event to fire immediately	X	
389003	Cat 3	Lock Access can be modified when PADDRDBG31 is HIGH	X	
389487	Cat 3	Even numbered Single Address Comparators incorrectly match when a data abort occurs	X	
409114	Cat 3	ETMJTAGPORT behaves incorrectly when simultaneous JTAG and APB transactions occur	X	
417671	Cat 3	PCLKENDBG not used on writes to Claim Tag registers	X	
425217	Cat 3	Multiple trigger requests might occur	X	
435286	Cat 3	Address Comparators might behave incorrectly while processor is halted in debug	X	
436732	Cat 3	CPRT View Data filtering is inaccurate under rare conditions	X	
439043	Imp	PCLKEN input to ETM9CSSingle might cause timing closure failures	X	

All errata affect the CoreSight ETM9 when connected to any processor based upon the ARM9EJ-S or ARM9E-S unless otherwise stated.

Errata - Category 1

There are no Errata in this Category.

Errata - Category 2

354112: ATCLK registers might return incorrect value

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 2, Present in: r0p0, Fixed in r0p1.

Description

The readable registers in the CoreSight ETM9 programmer's model which are clocked using ATCLK might return 32'h00000000 instead of the correct value. The affected registers are:

- CoreSight Trace ID, register 0x080 (offset 0x200)
- ITTRIGGERACK, register 0x3B9 (offset 0xEE4)
- ITATBCTR2, register 0x3BC (offset 0xEF0)

When any two of the above registers are read in close succession, the second register read might return 32'h00000000.

Conditions

1. One of the aforementioned registers is read via the Debug APB interface
2. A second register on the aforementioned list is read via the Debug APB interface

Implications

The read data from the second register is incorrect.

Workaround

This is a workaround for tool vendors.

The CoreSight ETM9 is implemented in 2 types of system, based on the method of accessing the ETM registers:

1. The ETM is accessed via the ETM JTAG Port. The erratum does not occur in these systems since the ATCLK registers are not accessible via the ETM JTAG Port.
2. The ETM is accessed via the Debug-APB interface, controlled by a Debug Access Port (DAP). In these systems, ATCLK is always equal to or faster than PCLKDBG and this workaround must be applied.

When reading any of the aforementioned registers, four register reads must be made from a register in the PCLKDBG domain prior to reading the ATCLK domain register. This ensures the read data for the ATCLK register is ready to be passed out over the APB interface.

It is recommended that the PCLKDBG domain register read is the Component ID0 (register 0x3FC, offset 0xFF0). The four reads will each return a data value of 0x0000000D, which must be ignored.

356598: Register reads via ETM JTAG Port might return incorrect values

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 2, Present in: r0p0, Fixed in r0p1.

Description

This erratum only affects CoreSight ETM9 when used with the ETM JTAG Port, as connected in ETM9CSSingle. If the ETM JTAG Port is not used, this erratum does not occur.

When reading a register via the ETM JTAG Port, 2 shifts of 40 bits must take place in the Shift-DR state of the JTAG TAP state machine. The first 40 bits indicate a read of a register is required and the second 40 bits are used to scan out the result of the read. Between the shifts of 40 bits, the JTAG State machine must go through the Update-DR state and return to Shift-DR. Whilst returning to Shift-DR, if the JTAG state machine does not pass through Run-Test/Idle, the read data returned in the second 40 bit shift will be incorrect.

Conditions

1. The CoreSight ETM9 is used with the ETM JTAG Port
2. A register read is performed where the JTAG TAP state machine does not pass through Run-Test/Idle between the read command being scanned in and the read data being scanned out.

Implications

The data returned when reading ETM registers via JTAG is incorrect.

Workaround

This workaround is for tool vendors.

When reading ETM registers, the JTAG TAP state machine must pass through the Run-Test/Idle state when transitioning from Update-DR to Shift-DR. This increases the number of TCK cycles taken to move between Update-DR and Shift-DR by one cycle.

388738: Toggling of NIDEN and DBGEN might cause incorrect trace

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 2, Present in: r0p0, Fixed in r0p1.

Description

Two inputs signals, NIDEN and DBGEN, are provided on CoreSight ETM9 as global control signals to allow the CoreSight ETM9 to operate.

If both of these signals are LOW, then the CoreSight ETM9 should stop tracing and output all trace currently in the FIFO. If either of the signals is subsequently driven HIGH, the CoreSight ETM9 should restart tracing at the following instruction boundary.

If this erratum occurs, the ETM FIFO does not empty when these signals are driven LOW. When one of the signals is driven HIGH, the data remaining in the FIFO is output, but the ETM might not restart tracing correctly and might output incorrect trace. Packet boundary synchronisation is maintained.

Conditions

The following operations must occur in the sequence defined:

1. The CoreSight ETM9 is enabled and generating trace
2. NIDEN and DBGEN are driven LOW
3. NIDEN or DBGEN is driven HIGH

Implications

The trace data is incorrect until the next I-Sync packet or indirect branch packet.

It is not expected that the signals NIDEN and DBGEN will be dynamically changed during tracing since the normal usage model for these signals is to permanently disable tracing on a device. If these signals are not dynamically changed during tracing, this erratum does not occur.

Workaround

There is no workaround for this erratum.

Trace synchronisation can be regained at the next indirect branch packet or I-Sync packet.

388999: ETM FIFO might not empty when setting the programming bit

Status

Affects: product CoreSight ETM9.

Fault status: Cat 2, Present in: r0p0, Fixed in r0p1.

Description

When setting the programming bit (bit [10] of the ETM Control register, 0x000), the CoreSight ETM9 stops tracing and empties its internal trace data FIFO. When the FIFO is empty, bit [1] of the ETM Status register (0x004) is set to 1'b1 to indicate the ETM has reached a stable state. This erratum might cause bit [1] of the ETM Status register to never be set to 1'b1.

Conditions

The conditions below must occur in order.

1. The CoreSight ETM9 is enabled and TraceEnable is active
2. The ARM9 processor executes an indirect branch instruction
3. The programming bit in the CoreSight ETM9 is set
4. The ARM9 processor executes the instruction at the destination of the indirect branch

This erratum does not occur if the processor is halted before the ETM programming bit is set.

Implications

The ETM Architecture specification describes the process by which programming the ETM registers must be performed. Part of this process describes what to perform when setting the programming bit and includes instructions to read the ETM Status register until bit [1] is set. If this erratum occurs, the programming process cannot complete because bit [1] of the ETM Status register is never set.

Workaround

This is a workaround for tools vendors.

When setting the programming bit, the ETM Status register must be read until bit [1] is set. If this does not occur within a reasonable number of iterations (it is recommended that you use a minimum of 200 iterations), perform the following steps:

1. Save the value of the TraceEnable Event register (register 0x008, offset 0x020)
2. Write 0x0000406F to the TraceEnable Event register, to disable trace generation
3. Clear the programming bit
4. Set the programming bit
5. Read the ETM Status register until bit [1] is set

If bit [1] of the ETM Status Register still does not return set, double the iteration limit and try again. Repeat the above steps until the status register reads as set.

401255: Address Comparator might not match on non-word-aligned instruction address

Status

Affects: product CoreSight ETM9.

Fault status: Cat 2, Present in: r0p0, Fixed in r0p1.

Description

If a Single Address Comparator is set to match on an instruction address which is not word aligned but is half-word aligned, the behavior of the comparator is Unpredictable.

Conditions

1. A Single Address Comparator is programmed for instruction address comparisons
2. The Single Address Comparator value register has bits [1:0] equal to b10
3. An instruction is executed at the programmed address

Implications

The behavior of the comparator is Unpredictable when the instruction is executed, for example when executing Thumb code. The comparator might match or it might not match.

The behavior of any resources which are dependent on this comparator is Unpredictable. For example, if the ETM trigger is set to fire on the affected comparator, the trigger might or might not occur when the desired instruction is executed.

The operation of address range comparators is not affected by this erratum.

Workaround

This is a workaround for tools vendors and users.

If a Single Address Comparator is required to be programmed for an instruction address comparison with bit [1] of the address set, use an Address Range Comparator instead.

For example, if a comparison is required for address 0x00001002, configure an Address Range Comparator for the range: 0x00001002 to 0x00001004.

You should be aware than an Address Range Comparator configured in this way will continue to match until the next instruction is executed, whereas a Single Address Comparators would only match for one cycle. This might cause problems depending on what the comparator is being used to control. It should also be noted that Address Range Comparators cannot be used to control the TraceEnable Start/Stop block.

401320: AFREADYM signal might not be asserted

Status

Affects: product CoreSight ETM9.

Fault status: Cat 2, Present in: r0p0, Fixed in r0p1.

Description

On the AMBA Trace Port (ATB) of the CoreSight ETM9, two signals are provided to implement a trace data flushing mechanism. AFVALIDM is an input signal which requests a flush of all trace currently stored in the CoreSight ETM9. AFREADYM is an output signal which indicates when all stored data has been output by the CoreSight ETM9 and is asserted in response to an assertion of AFVALIDM. This flushing mechanism allows trace capture devices to dynamically request all stored data to be output.

On CoreSight ETM9 the AFREADYM signal might not be asserted under certain conditions, causing the ETM to never acknowledge the flush request.

Two sets of conditions can cause this erratum to occur, described below in Conditions 1 and Conditions 2.

Conditions 1

The following conditions must occur in the following order for this erratum to occur:

1. The ETM PWRDOWN bit (bit [0] of the ETM Control Register 0x000) is cleared
2. The ETM PWRDOWN bit is set
3. AFVALIDM is asserted

This erratum does not occur when the CoreSight ETM9 is used in the ETM9CSSingle configuration.

Conditions 2

The following conditions must occur in the following order for this erratum to occur:

1. The ETM PWRDOWN bit (bit [0] of the ETM Control Register 0x000) is cleared
2. The ETM is programmed and tracing is enabled
3. Both the NIDEN and DBGEN input signals are driven LOW while trace data is still in the ETM’s FIFO
4. AFVALIDM is asserted

This erratum does not occur when the CoreSight ETM9 is used in the ETM9CSSingle configuration.

Implications

Trace capture devices will usually use the flush mechanism to request all data from the system before stopping trace capture. When this erratum occurs these trace capture devices will never receive a flush completion acknowledgement via AFREADYM and therefore might never stop capturing trace. For example, if the trace capture device is the CoreSight TPIU or CoreSight ETB then trace decompression tools might continue polling the TPIU or ETB waiting for trace capture to stop and it never stops, thereby causing an infinite loop until the device is reset, or a timeout in the tools is triggered.

Workaround

This is a workaround for tools vendors.

If a trace capture device is configured to issue a flush before trace capture stops then the following tasks must be performed:

- If the CoreSight ETM9 is connected to a trace funnel, then the CoreSight ETM9 should be configured to be the lowest priority ATB source. This ensures that the ETM flushed last. This might impact the number of FIFO overflows observed in a bandwidth limited system.
- The tools should monitor the status of the flush operation. When using a CoreSight TPIU or CoreSight ETB this can be done using the Formatter and Flush Status Register. If a flush is observed to continue for a long period of time (for example, 100ms or more) then trace capture should be disabled immediately without waiting for the flush to complete.

This might result in some of the trace which was present in the CoreSight ETM9 to not be captured by the trace capture device.

Trace tools can avoid this erratum by configuring the trace capture devices to never request a flush when the CoreSight ETM9 is connected to the trace capture device. This might result in some of the trace which was present in all trace sources to not be captured by the trace capture device.

Trace tools can avoid Conditions 1 if this erratum by ensuring the ETM is never powered down once it has been powered up. This is done by keeping bit [0] of the ETM Control Register clear.

System implementors can avoid Conditions 2 of this erratum by ensuring NIDEN and DBGEN are not changed dynamically.

401323: Accesses to ATCLK registers can cause APB interface to lockup

Status

Affects: product CoreSight ETM9.

Fault status: Cat 2, Present in: r0p0, Fixed in r0p1.

Description

The CoreSight ETM9 performs internal clock gating to decrease power consumption. Many of the internal registers are clock gated when any of the following conditions exist:

1. The ETMPWRDOWN (bit [0] of the ETM Control register, 0x000) is HIGH
2. The input signals NIDEN and DBGEN are both LOW

When the internal registers are clock gated, accesses to the programmer's model registers in the ATCLK domain cause the output signal PREADYDBG to remain LOW, thereby causing the APB interface to lock up and preventing further accesses to the ETM and other devices on the same APB bus until the ETM is reset.

Conditions

1. The ETMPWRDOWN (bit [0] of the ETM Control register, 0x000) is HIGH, OR the input signals NIDEN and DBGEN are both LOW
2. One of the following registers is accessed:
   a. CoreSight Trace ID register (register 0x080, offset 0x200)
   b. Integration Register ITATBCTR0 (register 0x3BE, offset 0xEF8)
   c. Integration Register ITATBCTR1 (register 0x3BD, offset 0xEF4)
   d. Integration Register ITATBCTR2 (register 0x3BC, offset 0xEF0)
   e. Integration Register ITATBDATA0 (register 0x3BB, offset 0xEEC)
   f. Integration Register ITTRIGGERREQ (register 0x3BA, offset 0xEE8)
   g. Integration Register ITTRIGGERACK (register 0x3B9, offset 0xEE4)

These registers cannot be accessed via JTAG when the ETM9CS is used in the ETM9CSSingle configuration. As such this erratum cannot occur if the only supported access mechanism is via JTAG to ETM9CSSingle.

Implications

When this erratum occurs, the PREADYDBG output from the CoreSight ETM9 is driven low until PRESETDBGn is asserted LOW. This means the APB bus is locked up and no further accesses can be made to the CoreSight ETM9 or any other peripherals on the same APB bus.

This erratum does not affect JTAG accesses to the CoreSight ETM9 when using the ETM JTAG PORT in ETM9CSSingle, since the ATCLK registers cannot be accessed in this configuration.

This erratum is highly unlikely to occur, since debug tools must always power up the ETM before accessing the affected registers. If NIDEN and DBGEN are both LOW, tools must inspect the Authentication Status register (register 0x3EE, offset 0xFB8) to determine if non-invasive debug is enabled before accessing the affected registers. The only other likely reason to access these registers is by faulty software, for example where a corrupted pointer causes the ETM registers to be accessed by accident.

Workaround

This is a workaround for tools vendors.

Tools should ensure that the proper mechanisms are used to detect if the ETM is powered up and non-invasive debug is enabled before accessing the affected registers. The ETMPWRDOWN bit (bit [0] of the ETM Control register, register 0x000) must be LOW and the Authentication Status register (register 0x3EE, offset 0xFB8) must indicate non-invasive debug is enabled.

If NIDEN or DBGEN can be dynamically changed in the system, then the workaround might not guarantee avoidance of this erratum.

There is no workaround when faulty software accidentally accesses the ETM.

408625: A-Sync packet might not be output when trace is enabled

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 2, Present in: r0p0, Fixed in r0p1.

Description

An alignment synchronisation (A-Sync) packet is required every time the ETM programming bit is cleared, to ensure trace decompression tools can determine the packet boundary of the trace protocol. A-Sync packets are also output periodically in the trace stream.

When the ETM programming bit is cleared, this erratum might cause an A-Sync packet to be missing from the trace output.

Conditions

1. ATCLKEN is used to clock gate ATCLK
2. The PWRDOWN bit in the ETM control register is cleared
3. The programming bit in the ETM control register is cleared within 3 ATCLK cycles of the PWRDOWN bit

If ATCLKEN is always b1, this erratum does not occur.

If ATCLK is equal to or faster than PCLK, this erratum does not occur because there is a guaranteed minimum of 3 PCLK cycles between the two programming accesses in Conditions 2 and 3. This is likely in most systems.

In normal systems, at least 10 of the ETM registers must be accessed between Conditions 2 and 3 to correctly enable trace. If this minimum set of registers is programmed then there is a guaranteed minimum of 30 PCLK cycles between Conditions 2 and 3, thereby eliminating the possibility of this erratum occurring to systems where ATCLK is at least 10 times slower than PCLK. This is very unlikely.

In summary, this erratum is very unlikely to occur.

Implications

In ETMs not subject to this erratum, trace decompression tools perform the following sequence in order to synchronise with the instruction trace:

1. Search from the beginning of the captured trace until an A-Sync packet is found
2. Search from the A-Sync packet until an I-Sync packet is found
3. Start instruction trace decompression

In addition, a data synchronisation packet must be found before data trace decompression can begin. This aspect is not discussed further.

If the trace capture device has not wrapped around (that is, no part of the trace stream has been overwritten), then the trace stream should start as follows when this erratum does not occur:

1. A-Sync packet
2. Non-periodic I-Sync packet
3. Other trace packets

When this erratum occurs, the A-Sync packet is missing.

If this erratum occurs, packet boundary alignment might not be possible when tracing is enabled. This is important if trace is stored in a circular buffer, because trace synchronisation might not be possible.

Workaround

This is a workaround for tools vendors:

The trace decompressor can work around the erratum in the following way:

- If it is known that the trace capture device has not wrapped around, then the decompressor can omit the search for an A-Sync packet. The trace will begin on a packet boundary, and an A-Sync is not required.
- If it is known that the trace capture device has wrapped around, then this erratum has no implications and the normal decompression sequence must be followed.

Since this erratum is very unlikely to occur, this workaround does not need to be implemented.

This is a workaround for system implementors:

Ensure ATCLKEN is tied to b1. If ATCLK needs to be slowed down, this must be performed externally to the ETM.

Since this erratum is very unlikely to occur, this workaround does not need to be implemented.

425210: Trigger might not occur

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 2, Present in: r0p0, Fixed in r0p1.

Description

If an A-Sync packet is generated at the same time as a trigger occurs, the Trigger packet might not appear in the trace stream.

Additionally, the TRIGOUT signal from the ETM9CS might not be asserted.

Conditions

The following conditions must occur in the same clock cycle:

1. An A-Sync packet is generated
2. A Trigger occurs

A-Sync packets are generated periodically in the trace stream and the period is dependent on the value of the Synchronization Frequency Register (register 0x078), which can take a value of between 60 and 4096.

Implications

The Trigger packet does not occur in the trace stream.

If using an ETM9CSSingle, the trigger condition might not occur on the trace port. This means the trace capture and analysis tools might not stop capturing trace which means that the desired trace might be overwritten in the trace capture device.

If using the CoreSight ETM9 in a CoreSight system the TRIGOUT signal is not asserted. This means that the trigger condition might not occur on the trace port or be embedded in the trace stream by a Trace Port Interface Unit. This means trace capture and analysis tools might not stop capturing trace which means that the desired trace might be overwritten in the trace capture device. Additionally, any cross triggering in the system which is configured to trigger on the ETM's TRIGOUT signal might not trigger.

It should be noted that this erratum is unlikely to occur. This is because A-Sync packets are usually generated quite rarely, depending on the Synchronization Frequency. For example, the default value of the Synchronization Frequency Register is 1024, which means that an A-Sync packet is generated every 1024 bytes of trace. Since the ETM can generate up to 4 bytes of trace per cycle, this would imply a 1 in 256 chance of the erratum occurring in a single trace run. However, since the trace output is bursty, with an average of around 2 bytes per cycle for full data trace, the erratum is likely to occur significantly less than once in 256 separate trace runs with the default Synchronization Frequency Register value (1024).

Workaround

The probability of this erratum occurring can be reduced by increasing the value of the Synchronization Frequency Register.

There is no workaround for this erratum when using ETM9CSSingle.

If using CoreSight ETM9 in a CoreSight system, then an External Output (EXTOUT) from the ETM could be used to trigger the cross-trigger infrastructure and the trace sink, such as a TPIU or ETB. It should be noted that the normal trigger generation in the ETM only generates one trigger event, whereas using the EXTOUT might cause multiple trigger events if used in this way. The ETM’s sequencer could be used in conjunction with the EXTOUT to avoid this.

Errata - Category 3

350998: Writes to counter value register might cause counter event to fire immediately

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

If the counter reload value register (register 0x50 or 0x51) is written with a value of zero and the counter value register (register 0x5c or 0x5d) is written with a value greater than zero, the counter should decrement on the counter enable event and then fire the 'counter at zero' event once the counter reaches zero. This erratum causes the 'counter at zero' event to fire immediately after the programming bit is cleared.

Conditions

1. Counter reload value register (0x50 or 0x51) programmed with zero
2. Counter value register (0x5c or 0x5d) programmed with a non-zero value

Implications

The counter behaves unexpectedly.

Workaround

There is no workaround for this erratum and tools vendors are advised to avoid programming the counters in this manner.

This is outside the normal usage model of the counter. The counter value register (0x5c or 0x5d) should only be written to restore the value of the counter if the state of the ETM is saved to memory and restored later. Under these conditions the counter value register is always less than or equal to the value of the counter reload value register and the erratum does not occur.

389003: Lock Access can be modified when PADDRDBG31 is HIGH

Status

Affects: product CoreSight ETM9.

Fault status: Cat 3, Present in: r0p0, Fixed in r0p1.

Description

When PADDRDBG31 is HIGH, the CoreSight ETM9 should consider all programming accesses to have been initiated by an external debugger. When PADDRDBG31 is LOW, the CoreSight ETM9 should consider all programming accesses to have been initiated by software running on the system.

The lock access mechanism consists of the Lock Access Register (register 0x3EC) and the Lock Status Register (register 0x3ED). The lock access mechanism should indicate that no lock access mechanism exists if programming accesses are initiated from an external debugger ie when PADDRDBG31 is HIGH. Writes to the Lock Access Register should be ignored by the ETM when PADDRDBG31 is HIGH.

Due to this erratum on CoreSight ETM9, when PADDRDBG31 is HIGH, the Lock Status Register correctly indicates that no lock access mechanism is present on accesses from an external debugger. However, the Lock Access Register can be used to mistakenly allow accesses by software running on the system.

Conditions

1. PADDRDBG31 is HIGH
2. Debugger software does not check the Lock Status Register before writing to the Lock Access Register

Implications

If an external debugger writes the lock access key, 0xC5ACCE55, to the Lock Access Register, the software lock is unlocked and software running on the system can write to the ETM registers. Additionally, if an external debugger was to write any value apart from 0xC5ACCE55 to the Lock Access Register, the software lock is locked, preventing any software running on the system from writing to the ETM registers.

Since an external debugger should read the Lock Status Register to determine if the lock mechanism is present before writing to the Lock Access Register, it is expected that no external debugger will write to the Lock Access Register thereby never causing this erratum to have any adverse effects.

Workaround

It is possible for target resident software to be given access to the ETM registers when the debugger might expect them to be locked out.

If an external debugger writes the lock access key, 0xC5ACCE55, to the Lock Access Register, the software lock is unlocked and software running on the system can write to the ETM registers. Additionally, if an external debugger was to write any value apart from 0xC5ACCE55 to the Lock Access Register, the software lock is locked, preventing any software running on the system from writing to the ETM registers.

Since an external debugger should read the Lock Status Register to determine if the lock mechanism is present before writing to the Lock Access Register, it is expected that no external debugger will write to the Lock Access Register thereby never causing this erratum to have any adverse effects.

389487: Even numbered Single Address Comparators incorrectly match when a data abort occurs

Status

Affects: product CoreSight ETM9.

Fault status: Cat 3, Present in: r0p0, Fixed in r0p1.

Description

When a Single Address Comparator is configured to match on data addresses with the Exact Match bit set, the comparator should not match if a data abort occurs. In CoreSight ETM9, the even numbered Single Address Comparators 2, 4, 6 and 8 will match regardless of whether a data abort occurs.

Conditions

1. One of the even numbered address comparators is configured to match a data address
2. The Exact Match bit (bit [7] of the Address Comparator Access Type Register) is set
3. A data transfer occurs which matches the address in the Address Comparator Value register
4. The data transfer is aborted

Address Range comparators are unaffected by this erratum.

Implications

Any resource in the CoreSight ETM9 which is programmed to be sensitive to the affected comparators will fire unexpectedly if this erratum occurs.

Workaround

This is a workaround for users and for tools vendors.

Single Address Comparators 1, 3, 5 and 7 are unaffected by this erratum. When programming comparators for Data Address matching with the Exact Match bit set, you must only use comparators 1, 3, 5 or 7 for these purposes. All comparators can be used when programming for other conditions.

409114: ETMJTAGPORT behaves incorrectly when simultaneous JTAG and APB transactions occur

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

The ETMJTAGPORT, as used in ETM9CSSingle, supports accesses originating from a JTAG port or from a system-driven APB port. The system-driven APB port will typically be driven by target resident software. In most situations, only one of these access mechanisms will be used at any one time.

For this erratum to occur, an access from the system-driven APB port must occur at the same time as the JTAG port is in use. When this erratum occurs, Unpredictable behavior might occur on the APB input port to the CoreSight ETM9.

Conditions 1

The following conditions must occur in order:

1. Scan chain 6 is selected in the ETMJTAGPORT
2. INTEST is selected as the JTAG instruction in the ETMJTAGPORT
3. A software access is initiated over the system-driven APB input port to the ETMJTAGPORT
4. Scan chain 6 is deselected, or a JTAG instruction which is not INTEST is selected in the ETMJTAGPORT

The software access in stage 3 above is delayed because the PREADY output from the ETMJTAGPORT is driven LOW. After stage 4 above, the ETMJTAGPORT allows the software access to be transmitted to the CoreSight ETM9 and subsequently allows the software access to complete.

This erratum can only occur if the ETM9CSSingle configuration is used.

Conditions 2

The following conditions must occur in order:

1. Scan chain 6 is selected in the ETMJTAGPORT
2. A software access is initiated over the system-driven APB input port to the ETMJTAGPORT
3. PCLK cycle after the software access is initiated, INTEST is selected as the JTAG instruction in the ETMJTAGPORT

The software access in stage 2 above is delayed because the PREADY output from the ETMJTAGPORT is driven LOW.

This erratum can only occur if the ETM9CSSingle configuration is used.

Implications

System-driven accesses to the ETM using the APB port might cause Unpredictable behavior if performed during a debugger-driven JTAG access. This behavior might include:

- The software access in Conditions 1 above completes incorrectly. If the transaction was a write, the register might not be updated.
- If the transaction was a read, the read data returned might be incorrect.
- The APB protocol on the input to the CoreSight ETM9 might be violated, causing subsequent accesses to the ETM to behave incorrectly. This might involve PREADYDBG from the CoreSight ETM9 being held LOW, causing a deadlock on the APB interface, preventing any further APB operations to the ETM or any other components on same the APB bus.
- Future JTAG driven accesses might have no effect, in that write accesses do not update the ETM and read accesses return Unpredictable values.

In normal circumstances, only one access mechanism is used at any one time. Therefore this erratum is very unlikely to occur.

Workaround

This is a workaround for tools vendors.

To prevent this errata occurring, only one of the access mechanisms must be used at any one time, either JTAG or software accesses. If this is the case, this erratum does not occur.

417671: PCLKENDBG not used on writes to Claim Tag registers

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

The clock enable PCLKENDBG for the APB interface is not used on writes to the Claim Tag registers. This causes multiple writes to the Claim Tag registers.

Conditions

1. PCLKENDBG is used to slow down PCLKDBG
2. A write to the Claim Tag Set or Claim Tag Clear register is performed

Implications

This does not cause any functional problems with the operation of the ETM. The write data bus PWDATADBG must be stable for the whole duration of the APB transaction, which means that the same value is written multiple times.

This erratum might cause static timing analysis failures during implementation.

If ETM9CSSingle is implemented and the system-driven APB interface is not used, this erratum cannot occur.

Workaround

This is a workaround for system implementors.

If a slow APB clock is required, PCLKDBG must be gated externally to the ETM to provide the required clock frequency. PCLKENDBG must be tied HIGH.

425217: Multiple trigger requests might occur

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

The TRIGOUT signal from the ETM9CS might be asserted multiple times for one trigger event.

Conditions

This erratum does not happen in an ETM9CSSingle system.

The following conditions must occur:

1. The TRIGSBYPASS input signal is tied LOW
2. A Trigger occurs
3. The ATB transaction which contains the Trigger packet is stalled by the CoreSight system for at least 5 cycles

The ATB transaction might be stalled because the trace port cannot output the data quickly enough. For example, if a trace port size of 4 bits is used, the ATB transaction might be delayed for up to 8 cycles. Other trace sources in the system might also affect the available bandwidth on the ATB interface.

Implications

The TRIGOUT signal is asserted multiple times.

This might cause the CoreSight trace sink to indicate multiple triggers in the trace stream or on the trace port.

If the TRIGOUT signal is used in a cross trigger system then multiple trigger events might be signaled to other devices which are connected to the cross trigger system and configured to receive the trigger indication.

This does not affect the ETM's trace stream.

In most trace capture devices, this erratum should not be a problem.

Workaround

A workaround for tools vendors is to only use the first trigger in the trace stream when multiple triggers are present.

Due to the low impact, there is no need to workaround this erratum.

435286: Address Comparators might behave incorrectly while processor is halted in debug

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

When the Address Comparator has been program to match on instruction addresses it might cause the Comparator to behave incorrectly soon after the processor is halted in debug.

During an Instruction Address comparison an extra comparison is performed on entrance to debug state. An Unpredictable address will be used to resolve the comparison and therefore an Unpredictable behaviour might occur.

A Single Address Comparator might incorrectly match.

A Range Address Comparator might incorrectly match or might incorrectly stop matching.

Conditions

Single Address Comparator

- The Comparator is programmed for instruction address comparison
- Processor enters debug state
- Erroneous comparison does match

Range Address Comparators condition 1

- The comparator is programmed for instruction address comparison
- The comparator is programmed so that the last instruction before entering debug state matches
- Processor enters debug state.
- Erroneous comparison does not match

Range Address Comparators condition 2

- The comparator is programmed for Instruction Address Comparison
- The comparator is programmed so that the last instruction before entering debug state does not match
- Processor enters debug state.
- Erroneous comparison does match

Implications

The behavior of the comparator is Unpredictable when the processor is halted in debug. Any resource in the CoreSight ETM9 which is programmed to be sensitive to the affected comparators will fire unexpectedly if this erratum occurs.

The behavior of any resources which are dependent on this comparator is Unpredictable. For example, if the ETM trigger is set to fire on the affected comparator, the trigger might or might not occur.

Workaround

There is no workaround for this erratum.

436732: CPRT View Data filtering is inaccurate under rare conditions

Status

Affects:	product CoreSight ETM9.
Fault status:	Cat 3, Present in: r0p0, Fixed in r0p1.

Description

If CPRT data transfers are to be traced only when ViewData is active, then if ViewData is active but the instruction immediately preceding a CPRT is programmed to be in a ViewData exclude region, then the data transfer associated with the CPRT access itself will erroneously also be excluded. Also if the instruction preceding a CPRT is programmed to be in a ViewData include region, but the CPRT is in a ViewData exclude region, then the CPRT access will erroneously also be included.

Conditions

Both the Monitor CPRT (bit [1]) and Filter CPRT (bit [19]) are set in the ETM Control Register, so that CPRTs are traced only when ViewData is active.

There are two scenarios:

1. The ETM is programmed so that the instruction preceding a CPRT is excluded from the trace but the CPRT transfer itself should be included in the trace. An example of how this condition could be programmed is as follows:

- A Single Address Comparator is programmed with the address of the instruction preceding a CPRT.
- ViewData Control 1 Register is programmed for Exclude control of the Single Address Comparator programmed as above.
- The ViewData Event Register is programmed so that ViewData is active.

2. The ETM is programmed so that the instruction preceding a CPRT is included from the trace but the CPRT transfer itself should be excluded from the trace. An example of how this condition could be programmed is as follows:

- A Single Address Comparator is programmed with the address of the instruction preceding a CPRT.
- ViewData Control 1 Register is programmed for Include control of the Single Address Comparator programmed as above.
- ViewData Control 3 Register is programmed for Mixed mode.
- The ViewData Event Register is programmed so that ViewData is active.

Implications

The data item associated with a CPRT instruction will either be missing from the trace when it should be present, or will be present in the trace when it should be missing.

Workaround

To avoid unexpectedly missing CPRT transfers, do not use Single Address Comparators to exclude instructions from View Data, instead use Address Range Comparators.

Errata – Implementation

439043: PCLKEN input to ETM9CSSingle might cause timing closure failures

Status

Affects: product CoreSight ETM9.

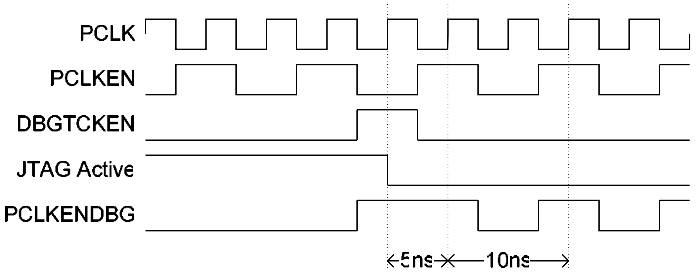
Fault status: Imp, Present in: r0p0, Fixed in r0p1.

Description

This erratum only affects CoreSight ETM9 when used in the ETM9CSSingle configuration.

The ETMJTAGPORT in ETM9CSSingle generates PCLKENDBG as an APB clock-enable for the CoreSight ETM9. PCLKENDBG is driven from either PCLKEN (the system APB clock enable) or DBGTCKEN from the JTAG synchronising logic in ETM9CSSingle. When the ETMJTAGPORT switches from JTAG to system APB or from system APB to JTAG, the PCLKENDBG input to the CoreSight ETM9 might cause consecutive PCLKENDBG pulses to be closer than synthesis constraints allow.

For example, consider if PCLK is driven at 200MHz and PCLKEN is used to produce an effective system APB clock speed of 100MHz. The time between 2 rising PCLK edges where PCLKEN is high is 10ns. If the ETMJTAGPORT switches while PCLKEN is low, then the time between 2 rising PCLK edges where PCLKENDBG is high might be 5ns. This might violate timing constraints. The timing diagram below shows how PCLKENDBG might behave



Conditions

- The CoreSight ETM9 is used in the ETM9CSSingle configuration
- The system APB uses PCLKEN to give an effective APB speed which is slower than PCLK
- The ETMJTAGPORT is used to program the ETM

Implications

Timing constraints might be violated. This might result in failure to achieve timing closure. This is not expected to cause significant functional problems because the signals which are sampled using PCLK and PCLKENDBG in the CoreSight ETM9 will not be changing around the switching point under normal circumstances.

Workaround

These are 2 workarounds for system implementors.

1. PCLKEN should be tied HIGH. If a slower APB speed is required, PCLK should be gated before being driven into ETM9CSSingle.
2. An external synchroniser should be used to generate DBGTCKEN and DBGTCKEN must be coincident with PCLKEN. JTAGSBYPASS to ETM9CSSingle is tied HIGH. Please contact ARM Ltd for more details.