ARM CoreSight ™
AHB Trace Macrocell (TM917)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p3 of AHB Trace Macrocell

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General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

14 Jun 2007: Changes in Document v4

Page	Status	ID	Cat	Summary
8	New	440270	Cat 1	ASYNC packet generation suppressed by HREADY high
16	New	440271	Cat 3	TraceOff packet might duplicate at the end of a trace session

1 May 2007: Changes in Document v3

Page	Status	ID	Cat	Summary
10	Updated	356153	Cat 2	AHB Reset connected to a data pin
11	Updated	402788	Cat 2	Invalid trace data may be output after a HTM FIFO flush
13	Updated	403712	Cat 2	Writes to HTM by external debuggers unexpectedly fail when sync bypass is enabled
14	Updated	365238	Cat 3	Setting of ITCR causes ATB violation and ATB transaction to be lost

20 Oct 2006: Changes in Document v2

Page	Status	ID	Cat	Summary
10	New	356153	Cat 2	AHB Reset connected to a data pin
11	New	402788	Cat 2	Invalid trace data may be output after a HTM FIFO flush
13	New	403712	Cat 2	Writes to HTM by external debuggers unexpectedly fail when sync bypass is enabled
14	New	365238	Cat 3	Setting of ITCR causes ATB violation and ATB transaction to be lost

21 Mar 2005: Changes in Document v1

Page	Status	ID	Cat	Summary
9	New	335891	Cat 2	Incorrect HTRANS detection with HTMHCTRLSEL of 0xE and 0xF
17	New	332112	Doc	DDI0328A HTM TRM Reset value error: Table 3-2 HTMDEVID reset value is 0x00000917. Should be 0x00000000.

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r0p1	r0p2	r0p3
332112	Doc	DDI0328A HTM TRM : HTMDEVID register reset value error	X			
440270	Cat 1	ASYNC packet generation suppressed by HREADY high	X	X	X	
335891	Cat 2	Incorrect HTRANS detection with HTMHCTRLSEL of 0xE and 0xF	X			
356153	Cat 2	AHB Reset connected to a data pin	X	X		
402788	Cat 2	Invalid trace data may be output after a HTM FIFO flush	X	X		
403712	Cat 2	Writes to HTM by external debuggers unexpectedly fail when sync bypass is enabled	X	X		
365238	Cat 3	Setting of ITCR causes ATB violation and ATB transaction to be lost	X	X		
440271	Cat 3	TraceOff packet might duplicate at the end of a trace session	X	X	X	

Errata - Category 1

440270: ASYNC packet generation suppressed by HREADY high

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 1, Present in: r0p0,r0p1,r0p2, Fixed in r0p3. New in this document.

Description

The HTM uses a TraceOff packet to indicate the ending of trace, or stopping of trace capturing if the trace start/stop control inside the HTM is used. It has a value of 0x28, as documented in the chapter 4 of HTM TRM. The TraceOff packet is output by the HTM at the end of each trace session, when the PROG bit in the HTMCONTROL register is set.

If the PROG bit is set while the internal pipelined **HREADY** signal in the AHB being traced is high, the TraceOff packet can be output twice. This is caused by the TraceOff packet generation which can be triggered by two separated mechanisms: setting of PROG bit, and turning off of the Trace Enabling block. These two sources are offset by 1 clock cycle. The second mechanism only triggers when the pipelined **HREADY** signal is high. So the duplicated TraceOff packet scenario depends on the AHB state.

Conditions

- Pipelined **HREADY** is high when PROG bit is switched from 0 to 1.

Implications

For systems with no wait states or wait states of only one cycle, the ASYNC packet will always be suppressed. As a result external trace decompression software cannot decompress the trace.

For systems with transfers with two or more wait states the ASYNC packet could be delayed, causing the beginning of the trace to be lost. Depending on the wait state pattern on the bus being traced, the regular ASYNC packet during the trace can also be delayed and can cause a problem to trace decompression if ASYNC is not output for a long time.

Workaround

There is no work around for the erratum.

Errata - Category 2

335891: Incorrect HTRANS detection with HTMHCTRLSEL of 0xE and 0xF

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 2, Present in: r0p0, Fixed in r0p1. Unchanged in this document.

Description

The HTM Control comparators do not operate correctly on data-phase signals, HTMCTRLSEL selector values 0xE and 0xF. For example, when configured to match on HRESP[1:0] indicating an error response (selector 0xF), the comparator will not deterministically fire when HRESP does indicate an error response. The reason for this is because the comparator output is qualified by a registered version of HTRANS, which might or might not be valid when the data-phase of the transaction completes.

Conditions

A HTMCTRLSEL0-7 register (0x200-0x21C) has bits [3:0] set to 0xE or 0xF

Implications

HTM generated trace may not be output as expected due to an incorrect matching of the comparator. This does not affect the ability to decompress the trace data.

Workaround

Workaround for tools:

For reliable comparator matching, the setting of HTMHCTRLSEL to 0xE and 0xF should be avoided.

356153: AHB Reset connected to a data pin

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 2, Present in: r0p0,r0p1, Fixed in r0p2. Unchanged in this document.

Description

The AHB reset pin, HRESETn is used as a data input to an internal register. The HRESETn signal is also used as a true reset within the HTM block, and therefore should be constrained as a reset signal.

Implications

Usage of a special pin (reset) as a data signal can result in synthesis timing issues due to the differing requirements for data and reset signals.

Workaround

None.

402788: Invalid trace data may be output after a HTM FIFO flush

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 2, Present in: r0p0,r0p1, Fixed in r0p2. Unchanged in this document.

Description

When the AFVALIDM input is asserted ATB packets stored in the HTM buffer will be flushed. However, if the AFVALIDM input is asserted at the same time that ATB packets are being presented and accepted on the ATB interface, then in some cases a FIFO underrun will occur in the buffer of the HTM. This will cause invalid ATB packets to be output on the ATB interface.

This does not affect flushing the HTM buffer by setting the PROG bit.

Conditions

Cycles of ATCLK:

1. Cycle N: AFVALIDM is not asserted.
2. Cycle N+1: A flush is started by asserting AFVALIDM.
3. Cycle N+2: One or more ATB packets are presented on the ATB interface independently of the flush operation and are accepted immediately (ATVALIDM and ATREADYM are both asserted)
4. Cycle N+3: No new ATB packets arrive in the FIFO buffer.

FIFO underrun takes place in cycle N+4. The Valid ATB packets in the FIFO buffer will be output, followed by invalid ATB packets.

The condition at cycle N+2 could be met by one of the following circumstances prior to cycle N+2:

1. ATB packets were generated recently and are entering the HTM buffer (ATVALIDM becomes asserted in cycle N+2).
2. ATB packets were generated some time ago but are not being accepted on the ATB interface because ATREADYM is not asserted (ATREADYM becomes asserted in cycle N+2). Both of the above circumstances occurring at the same time.

If trace is disabled sufficient cycles before the flush and AFREADYM is asserted this erratum will not occur.

Implications

Trace data will not be valid and not decompressible by tools. The invalid ATB packets could include reserved packet encodings and could cause synchronization in the packets stream to be lost until the next A-sync packet.

Workaround

Work around for implementers:

1. Tie AFVALIDM input of the HTM to 1'b0 (effectively stopping any flush request being received by the HTM) AND

2. Disconnect the AFREADY output of the HTM and tie the signal to 1'b1 (HTM is effectively given the response that it is always flushed)

It should be noted that this implementation prevents the workaround for the erratum 365238 from being possible.

Work arounds for tools:

- Flush the HTM buffer using the PROG bit instead of using AFVALIDM.

or

- Disable trace before asserting AFVALIDM. For instance using the HTMTRACEDISABLE input. In the case of HTMTRACEDISABLE it must be asserted at least 7 cycles of HCLK before AFVALIDM assuming that AFREADYM is asserted.

403712: Writes to HTM by external debuggers unexpectedly fail when sync bypass is enabled

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 2, Present in: r0p0,r0p1, Fixed in r0p2. Unchanged in this document.

Description

The HTM is locked when the register HTMLOCK_STATUS register 0x3 (bit [0] indicates lockpresent and bit [1] that it is locked). The lock can be set either out of reset or following a write to HTMLOCK_ACCESS of a value other than 0xC5ACCE55. In this state writes cannot be made to HTM registers unless the input **PADDRDBG31** is HIGH (which presents a memory model where there is no lock access mechanism). However, when the conditions below are met, writes which should not be blocked are still prevented by the lock mechanism.

Conditions

1. The HTM is locked (HTMLOCK_STATUS, at offset 0xFB4, bit 1 is HIGH) (only detectable when **PADDRDBG31** is LOW)
2. **SYNCBYPASS** is tied to 1'b1.
3. A write transfer where **PADDRDBG31** is asserted.

The writes to HTM registers in the AHB clock domain will fail when they should succeed.

Implications

The **PADDRDBG31** input can only be asserted by debug tools to access the HTM registers regardless of the HTM lock status. Under the above conditions writes to the HTM registers might fail (write operation ignored) when they should be expected to succeed.

Workaround

Workaround for implementers:

- **SYNCBYPASS** should not be set even when **HCLK** and **PCLKDBG** are synchronous.

Workaround for tools:

- Although when discovering the address location of the HTM it is presented at an address location were bit [31] is set (0x8000_0000 offset), it is still possible to access the HTM through the APB-AP in the DAP with bit [31] clear (effectively shifting the memory access into the 0x0000_0000 to 0x7FFF_FFFF region). When accessing the HTM through this address location, the lock access mechanism can be accessed and disabled (performing a write to HTMLOCK_ACCESS of 0xC5ACCE55).

Errata - Category 3

365238: Setting of ITCR causes ATB violation and ATB transaction to be lost

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 3, Present in: r0p0,r0p1, Fixed in r0p2. Unchanged in this document.

Description

Setting the HTM Test Control register (ITCR) after a trace session might cause a violation of the ATB protocol if trace was still being output when the ITCR is set. Enabling the integration mode (ITCR bit [0] is HIGH) forces ATVALID to be LOW, overriding the former signal value. If this happens during an ATB transaction, it will violate the ATB protocol, as ATVALID is specified as staying HIGH until the ready response (ATREADY HIGH) has been sent by the trace sink.

As this pre-emptively stops data leaving the HTM, there might be additional trace still held inside the HTM FIFO.

Conditions

1. Trace session is performed with the HTM generating trace data.
2. Trace data remains in the HTM.
3. The ITCR register (0xF00 bit [0]) is set.

Implications

- A violation of the ATB protocol can occur when setting ITCR which might result in connected ATB devices (e.g. replicator, bridge) to go into an invalid state.
- ATB transactions might be lost.
- The output trace stream could be incomplete if the HTM is taken into Integration Mode after a trace session.

Workaround

A tool workaround for this issue can be achieved if the trace sink (e.g. ETB or TPIU)connected to the HTM supports flushing and offers information about the flush progress status.

The steps to follow are:

1. Configure the trace sink to stop on flush completion: this is not compulsory, but since the objective is to take the HTM and the trace infrastructure into Integration Mode, it is advisable to stop any normal tracing once the HTM has been flushed.
2. Set the HTM Programming bit to 1.
3. Start a manual flush on the trace sink.
4. Poll the status register of the trace sink until the flush is complete and the trace sink has stopped.
5. Set the HTM Integration Mode Control Register to 1.

Note that Integration Mode isn't typically used after the device has been programmed, but normally at power-up only, when the device has been reset.

440271: TraceOff packet might duplicate at the end of a trace session

Status

Affects: product AHB Trace Macrocell.

Fault status: Cat 3, Present in: r0p0,r0p1,r0p2, Fixed in r0p3. New in this document.

Description

The HTM uses a TraceOff packet to indicate the ending of trace, or stopping of trace capturing if the trace start/stop control inside the HTM is used. It has a value of 0x28, as documented in the chapter 4 of HTM TRM. The TraceOff packet is output by the HTM at the end of each trace session, when the PROG bit in the HTMCONTROL register is set.

If the PROG bit is set while the internal pipelined **HREADY** signal in the AHB being traced is high, the TraceOff packet can be output twice. This is caused by the TraceOff packet generation which can be triggered by two separated mechanisms: setting of PROG bit, and turning off of the Trace Enabling block. These two sources are offset by 1 clock cycle. The second mechanism only triggers when the pipelined **HREADY** signal is high. So the duplicated TraceOff packet scenario depends on the AHB state.

Conditions

- Pipelined **HREADY** is high when PROG bit is switched from 0 to 1.

Implications

The result trace may result in an extra TraceOff packet at the end of a trace session. However, this does not affect the decoding of trace information.

Workaround

Trace decompression software can ignore the extra TraceOff packet.

Errata - Documentation

332112: DDI0328A HTM TRM : HTMDEVID register reset value error

Status

Affects: product AHB Trace Macrocell.

Fault status: Doc, Present in: r0p0, Fixed in r0p1. Unchanged in this document.

Description

On page 3-6 of the AHB Trace Macrocell r0p0 TRM, table 3-2 defines HTMDEVID reset value as 0x00000917. This should instead be a value of 0x00000000.

Implications

If the HTMDEVID register is read after reset has occured the value will be different from that documented in Table 3-2.

Workaround

Use Reset value according to this erratum.