ARM®

PrimeCell® Infrastructure AMBA™ 3 AXI™ to AMBA 3 APB™ Bridge (BP135) Revision: r0p0
Technical Overview

This technical overview describes the functionality of the AXI to APB bridge in the following sections:

1 Preliminary material

1.1 Release information

Changes to this document are listed in Table 1.

Table 1 Change history

Date	Issue	Change
29 November 2004	A	First issue for r0p0

1.2 Proprietary notice

1.3 Confidentiality status

1.4 Product status

The information in this document is for a final product, that is a developed product.

1.5 Web address

http://www.arm.com

2 About the AXI to APB bridge

You can use the AXI to APB bridge, `AxiToApb`, to connect between AXI and APB domains. Figure 1 shows a block diagram of an AXI to APB bridge used in a simple configuration with two APB slaves.

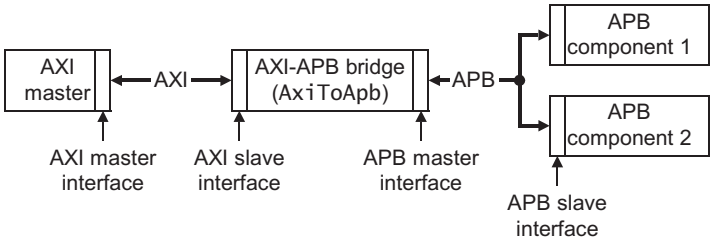

Figure 1 AXI to APB bridge block diagram

The component has the following features:

- 32-bit AXI slave and APB master interfaces.
- Supports up to 16 connected APB peripherals
- TrustZone support:
  - one **TZDECPROT** input signal for each decoded APB peripheral implemented as two 8-bit buses
  - DECERR response given for non-secure access to secure region and transfer not performed on APB.
- Translates all incoming AXI transfers irrespective of size.
- Supports single active transfer only.
- Supports the **PREADY** signal which translates to wait states on AXI.
- Supports the **PCLKEN** signal for differing clock speeds between AXI and APB.
- The **PSLVERR** signal translates to SLVERR response on AXI, an error on any transfer within a burst results in SLVERR as the AXI write response.
- Unused **PSEL** outputs are indicated by **PSELEN[15:0]** tie-offs on input pins. A DECERR response is given for an attempted access to any unused region.
- The HDL code is supplied as Verilog.

3 Functional description

The bridge provides an interface between the high-speed AXI domain and the low-power APB domain. It appears as a slave on AXI but as a master on APB that can access up to sixteen slave peripherals.

Read and write transfers on the AXI bus are converted into corresponding transfers on the APB. Because the APB is not pipelined, wait states are added during transfers to and from the APB when the AXI must wait for the APB protocol.

A multiplexor is implemented inside the bridge. It is responsible for selecting the following output of each APB slave to the bridge:

- read data, **PRDATAx**[1]
- transfer done, **PREADYx**
- transfer response, **PSLVERRx**.

3.1 Interface attributes

The AXI slave interface attributes for the AXI to APB bridge are provided in Table 2.

Table 2 Slave interface attributes

Attribute	Description	Value
Combined acceptance capability	The maximum number of active transactions that a slave can accept. This must be specified if read and write address storage is combined.	1
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	1
Read data reorder depth	The number of active read transactions for which a slave may transmit data. This is counted from the earliest transaction.	1

1. The letter **x** in the signal name denotes a number from 0-15.

4 Physical data

This section describes:

- *AC characteristics*
- *Gate count*.

4.1 AC characteristics

The AXI to APB bridge adheres to the following timing guidelines. The figures refer to the percentage of clock cycle allowed for each function.:

- AXI inputs must be valid for 40% prior to the rising edge of the clock
- AXI outputs must be valid for 20% after the rising edge of the clock
- APB inputs must be valid for 70% prior to the rising edge of the clock
- APB outputs must be valid for 20% after the rising edge of the clock.

Timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

4.2 Gate count

The estimated total gate counts with respect to the library described in *AC characteristics* is 3220.

Note

The gate count estimate does not include scan logic.

5 Signal descriptions

Figure 2 shows the component signal connections. The bridge uses:

- AMBA AXI signals as described in the *AMBA AXI Protocol Specification*.
- AMBA APB signals as described in the *AMBA APB Protocol Specification*.

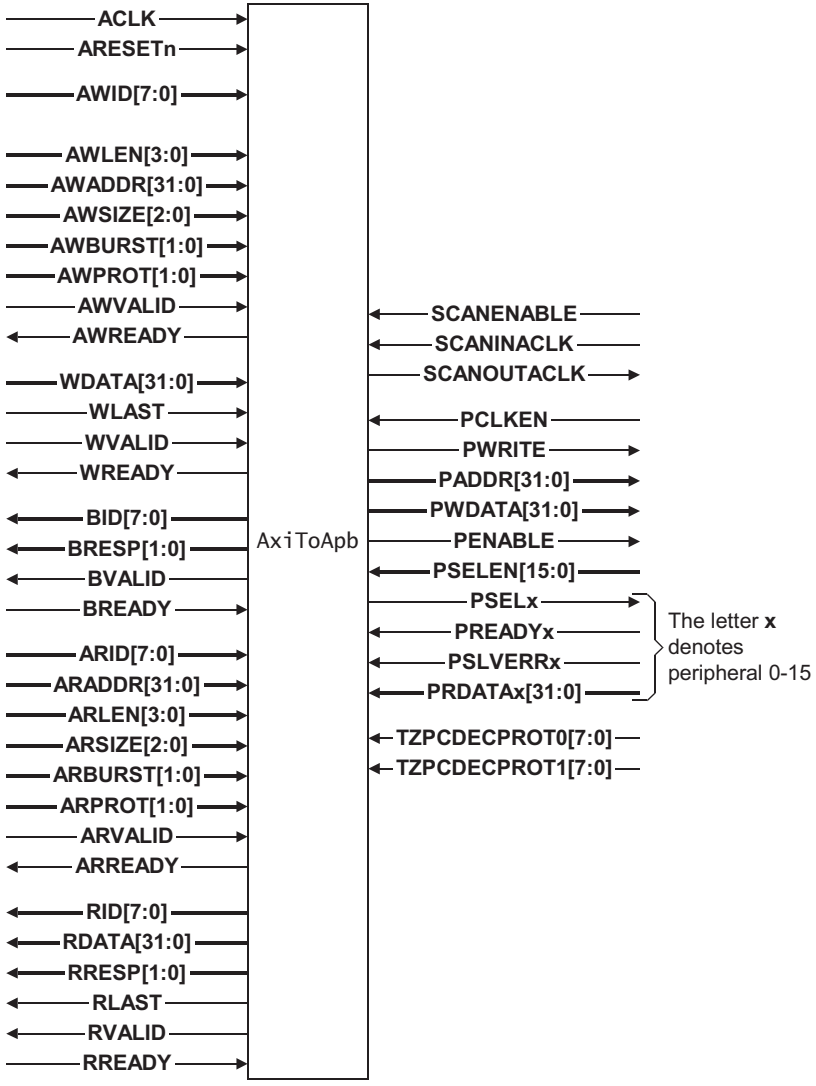

Figure 2 AXI to APB bridge signal connections

Table 3 lists signals that are present on the bridge but are not described in the relevant specification.

Table 3 Non-standard signals

Name	Type	Source/ destination	Description
SCANENABLE	Input	Scan logic	Scan mode enable
SCANINACLK	Input	Scan logic	Scan chain input
SCANOUTACLK	Output	Scan logic	Scan chain output
PCLKEN	Input	Clock source	APB clock enable that enables the APB device to run at an integer fraction of **ACLK**. **PCLKEN** remains asserted for **ACLK**. This signal corresponds to the rising edge of **PCLK**.
PSELEN[15:0]	Input	Tie-offs	Tie-offs for presence of APB slave slot: HIGH indicates APB slave device exists in that slot LOW indicates absence of APB device in that slot.
TZPCDECPROT0[7:0]	Input	*TrustZone Protection Controller* (TZPC)	TrustZone protection control information for APB peripherals 0-7: LOW indicates that all AXI access to that APB peripheral must be protected (secure) HIGH indicates that all AXI access to that APB peripheral can be secure or non-secure.
TZPCDECPROT1[7:0]	Input	TZPC	TrustZone protection control information for APB peripherals 8-15: LOW indicates that all AXI access to that APB peripheral must be protected (secure) HIGH indicates that all AXI access to that APB peripheral can be secure or non-secure.

