



ARM CoreSight™
PTM-A9 (TM950)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r1p0 of CoreSight PTM-A9

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General suggestion for additions and improvements are also welcome.

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Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

- | | |
|------------|---|
| Category 1 | Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable. |
| Category 2 | Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications. |
| Category 3 | Behavior that was not the originally intended behavior but should not cause any problems in applications. |

Change Control

25 Sep 2009: Changes in Document v3

Page	Status	ID	Cat	Summary
11	New	711668	Cat 3	Configuration Extension register has wrong value
10	Updated	568015	Cat 3	Timestamp not inserted if requested when trace disabled
12	New	720107	Cat 3	Periodic Synchronisation can be delayed, causing overflow
14	New	720403	Cat 3	Timestamp packet does not always indicate clock change

15 Dec 2008: Changes in Document v2

Page	Status	ID	Cat	Summary
10	New	568015	Cat 3	Timestamp not inserted if requested when trace disabled

15 April 2008: Initial Document v1

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r1p0
568015	Cat 3	Timestamp not inserted if requested when trace disabled	X	
711668	Cat 3	Configuration Extension register has wrong value	X	X
720107	Cat 3	Periodic Synchronisation can be delayed, causing overflow	X	X
720403	Cat 3	Timestamp packet does not always indicate clock change	X	X

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

There are no Errata in this Category

Errata - Category 3

568015: Timestamp not inserted if requested when trace disabled

Status

Affects: product CoreSight PTM-A9.

Fault status: Cat 3, Present in: r0p0, Fixed in r1p0.

Description

The PTM can be configured to insert timestamp packets at intervals in the trace stream. The PFT Architecture requires that one more timestamp packet should be inserted for the first request after trace is disabled, for example when the programming bit is set. As a result of this erratum, timestamps which are requested when TraceEnable is low will be delayed until trace enable becomes high again.

Conditions

1. The PTM is enabled
2. Timestamping is enabled
3. TraceEnable goes high, then low.
4. An event which causes the insertion of a timestamp occurs after TraceEnable goes low.

Implications

If timestamps are requested less frequently than TraceEnable stays high, fewer timestamps will be inserted in the trace stream than expected. If cycle accuracy is disabled, this will impact the ability to correlate trace streams.

Timestamps will only be missing whilst TraceEnable is low. If trace is enabled again, timestamps will be inserted correctly.

There is no corruption of the trace stream.

Workaround

There is no workaround for this erratum.

Increasing the frequency at which timestamps are requested may reduce the impact of this erratum.

711668: Configuration Extension register has wrong value**Status**

Affects: product CoreSight PTM-A9.

Fault status: Cat 3, Present in: r0p0, r1p0, Open.

Description

The PTM implements several read only registers which provide a mechanism for tools using the PTM to determine which features are present in a specific implementation. The Configuration Code Extension register (0x7A, address 0x1E8) has an incorrect value in both r0p0 and r1p0 releases of 0x000008EA. The correct values are specified in the TRM and are as follows:

r0p0 should be 0x00C018EA

r1p0 should be 0x00C019A2

Conditions

1. The Configuration Code Extension register is read

Implications

This erratum has no impact on the generation of trace, or the configurations which can be enabled. Tools which read this register in order to determine the capabilities of the PTM will detect fewer features than are actually present. The missing bits indicate

[23] Return stack implemented.

[22] Timestamping Implemented.

[12] reserved, for compatibility with Etm Arch.

[10:3] are incorrect in r1p0, and should indicate 52 external inputs.

Workaround

This workaround is for tools using the PTM-A9. Rather than relying on the Configuration Code extension register, the peripheral ID registers (at offsets 0xFE0 to 0xFEC) can be used to determine the version of the PTM-A9, and the features which are implemented.

Return stack is implemented in r0p0 and r1p0.

Timestamping is implemented in r0p0 and r1p0.

The extended external input bus is 52 bits for r1p0, 28 bits for r0p0.

720107: Periodic Synchronisation can be delayed, causing overflow

Status

Affects: product CoreSight PTM-A9.

Fault status: Cat 3, Present in: r0p0,r1p0, Open.

Description

The PTM is required to insert synchronisation information into the trace stream at intervals in order to allow a partial trace dump to be decompressed. The synchronisation period is either determined external to the PTM or by a counter which by default requests synchronisation every 1024 bytes of trace.

It is not important for the protocol that the synchronisation is inserted precisely at a regular interval, so allowance is made to delay synchronisation if the PTM is required to generate other trace packets, or if there is not sufficient space in the FIFO. So as to guarantee that regardless of the conditions, some synchronisation packets are always inserted a 'forced overflow' mechanism will shut off trace if a new synchronisation request occurs before the previous request was satisfied. This forced overflow mechanism is minimally intrusive to the trace stream, but ensures that synchronisation is inserted after no more than 2x the requested interval.

Due to this erratum, some specific sequences of instructions can result in the PTM not being able to insert any synchronisation into the trace stream whilst that instruction sequence continues. Typically, there will just be a short delay which may not be noticed and the synchronisation is inserted once the particular pattern of waypoints changed. It is possible that overflows will be generated in the trace regardless of the utilisation of the FIFO in the PTM. In this scenario, typically only a single byte of trace (up to 5 waypoints) would be lost.

The scenario does not correspond to sustained high rates of trace generation which could genuinely cause the FIFO to become full.

Scenarios where this erratum is triggered are rare, and are probably limited to code iterating around a loop many times. The loop would contain several branches and be dependant on memory accesses completing.

Conditions

1. Tracing is enabled
2. Branch broadcasting is disabled
3. Cycle accuracy is disabled
4. The processor executes tight loops of repeating code, lasting longer than the configured synchronisation period.

Implications

The impact of this erratum is to reduce the frequency of periodic synchronisation and potentially cause trace overflows where some trace is lost. In the case of an overflow, trace following the overflow can be correctly decompressed. The erratum will be more noticeable if the periodic synchronisation requests are more frequent.

Workaround

The most appropriate workaround will depend on the use-case for the trace:

1. If the trace buffer is large enough, consider increasing the synchronisation period by setting the ETMSYNCFR to a higher value.
2. If it is required that no trace is lost (and periodic synchronisation does not have to be guaranteed), set bit[0] of ETMAUXCR to disable the forced overflow function. Synchronisation will then be inserted at the earliest opportunity, dependant on the executed instruction stream.

720403: Timestamp packet does not always indicate clock change

Status

Affects: product CoreSight PTM-A9.

Fault status: Cat 3, Present in: r0p0, r1p0, Open.

Description

The PFT architecture states that when the clock frequency of the processor changes (as indicated by a single-cycle pulse on the CLKCHANGE input pin) a timestamp packet must be output which indicates this change (using the R bit in the timestamp header).

The R bit in the timestamp packet is a hint to tools that a discontinuity has been introduced into the timestamp stream, and the ratio of processor clock to timestamp clock must be determined again for the purpose of interpolating between timestamps using cycle counts.

As a result of this erratum, the R bit might not be set in the timestamp packet. The CLKCHANGE pin does correctly cause the insertion of a timestamp packet.

Note that if the timestamp clock and processor clock are the same, it is recommended that CLKCHANGE be tied low. This pin is intended to support future systems where a single timestamp source is shared across multiple sub-systems having different clock domains.

Conditions

1. The PTM is enabled
2. Tracing is active
3. Timestamping is enabled
4. Processor clock and timestamp generation are implemented in different clock domains
5. CLKCHANGE input pin is driven high

Implications

Timestamp packets are still inserted with the correct timestamp value.

This erratum will impact the accuracy of interpolation between timestamps.

There is no corruption of the trace stream.

Workaround

No workaround is required for this erratum.

Errata - Documentation