PrimeCell® Infrastructure AMBA™ 3 AXI File Reader Master (BP144)

Revision: r0p0

Technical Overview

ARM®

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Release Information

The following changes have been made to this book.

Change History

Date	Issue	Change
17 December 2004	A	First issue for r0p0

Proprietary Notice

Confidentiality Status

Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

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Chapter 1
Technical Overview

This technical overview describes the functionality of the AXI *File Reader Master* (FRM) in the following sections:

- *About the AXI FRM* on page 1-2
- *Functional description* on page 1-3
- *Signal descriptions* on page 1-5.

1.1 About the AXI FRM

You can use the AXI FRM, `FileRdMasterAxi`, to simulate AXI systems quickly and efficiently by generating explicit AXI bus transfers that are described in a stimulus file. It enables you to specify the requested timings of all master-generated signals.

The FRM supports a special command that enables the independent AXI channels to be synchronized at a point described in the stimulus file. It can also repeatedly read from an address until the data returned meets certain criteria.

The FRM is a behavioral component and is not intended to be synthesized.

The `FileRdMasterAxi` has the following features:

- It converts a human-readable stimulus file that describes transactions into AXI transfers.
- It comprises:
  - Perl pre-processor script
  - Verilog virtual component.
- It supports a subset of the AXI XVC vector format, see the *PrimeCell Infrastructure AMBA 3 AXI File Reader Master Design Manual*.
- It supports requested master generated timings.
- It supports a behavioral Quit command.
- It checks slave-generated data and responses.
- It has a configurable data bus width of 32 or 64 bits.

1.2 Functional description

Figure 1-1 shows the AXI FRM data flow.

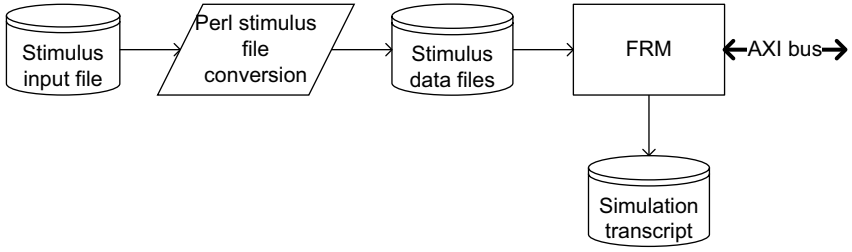

Figure 1-1 FRM data flow

The stimulus input file is text-based. It enables you to define the AXI transactions for simulation. The filename of the stimulus data file is specified using a Verilog parameter at the point of instantiation within the HDL code.

The input stimulus file is converted to seven HDL hexadecimal format stimulus data files by the Perl pre-processor script:

- one for each AXI write channel:
  - write address
  - write data
  - write response.
- one for each AXI read channel:
  - read address
  - read data.
- one set of simulation comment vectors for each AXI address channel:
  - write address
  - read address.

The pre-processor script also checks the stimulus input file for syntax, functional errors and AXI protocol errors. The checks and errors are further described in the *PrimeCell Infrastructure AMBA 3 AXI File Reader Master Design Manual*.

The stimulus data files are input to the FRM. This initiates the defined transactions on the relevant AXI channels. The transactions are monitored by the FRM and compared with expected results from the stimulus data files. This comparison is output in the form of a human-readable transcript file.

1.2.1 Master interface attributes

Table 1-1 lists the FRM interface attributes.

Table 1-1 Master interface attributes

Attribute	Description	Value
Read ID capability	The maximum number of different **ARID** values that a master can generate for all active read transactions at any one time.	1
Read ID width	The number of bits in the **ARID** bus.	0
Read issuing capability	The maximum number of active read transactions that a master can generate.	Stimulus-dependent
Write ID capability	The maximum number of different **AWID** values that a master can generate for all active write transactions at any one time	1
Write ID width	The number of bits in the **AWID** and **WID** buses.	0
Write issuing capability	The maximum number of active write transactions that a master can generate.	Stimulus-dependent

1.3 Signal descriptions

The AXI FRM uses standard AMBA AXI signals as described in the *AMBA AXI Protocol Specification* except for the following:

- **AWID** is not used and is not present on the write address channel interface
- **WID** is not used and is not present on the write data channel interface
- **BID** is not used and is not present on the write response channel interface
- **ARID** is not used and is not present on the read address channel interface
- **RID** is not used and is not present on the read data channel interface
- **RLAST** is not used but is present on the read data channel interface.

The AXI FRM signals are shown in:

- *Global and low-power interface signals*
- *Write channel signals*
- *Read channel signals* on page 1-6.

Note

The upper value of some bus widths is provided as a name to indicate that the number of signal lines in the bus is derived from user-defined generics or parameters. These are described in the *PrimeCell Infrastructure AMBA 3 AXI File Reader Master Design Manual*.

1.3.1 Global and low-power interface signals

Figure 1-2 shows the AXI global and low-power interface signal connections.

Figure 1-2 Global and low-power interface signal connections

1.3.2 Write channel signals

Figure 1-3 on page 1-6 shows the AXI write address, write data, and write response channel signal connections

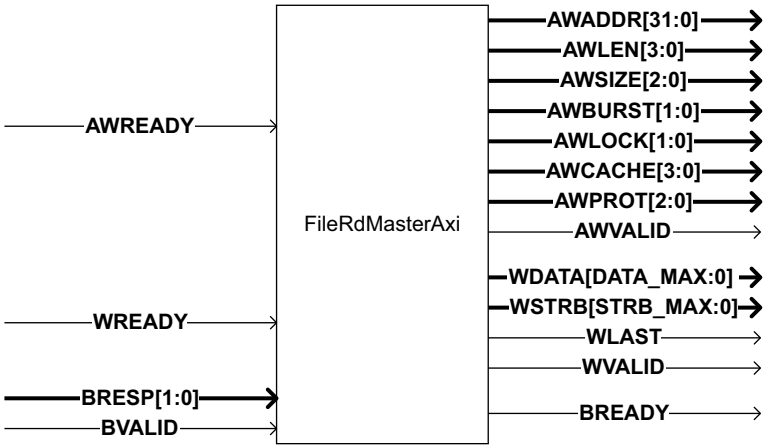

Figure 1-3 Write channel signal connections

1.3.3 Read channel signals

Figure 1-4 shows the AXI read address and read data channel signal connections.

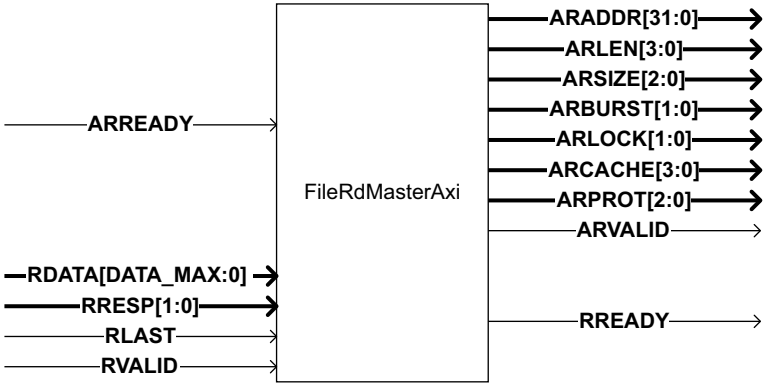

Figure 1-4 Read channel signal connections