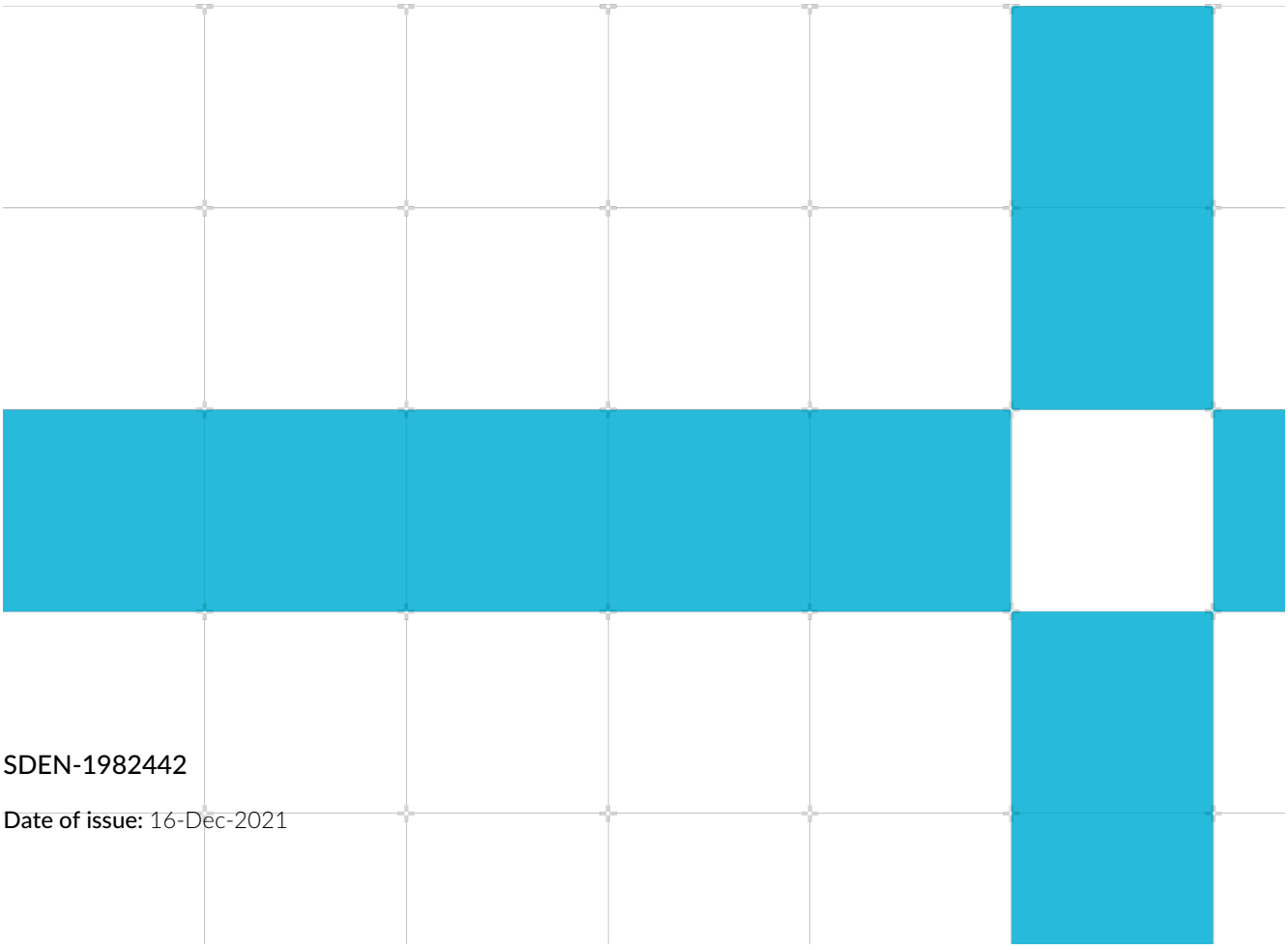
Arm Neoverse N2 (MP128)

Software Developer Errata Notice

This document contains all known errata since the r0p0 release of the product.



SDEN-1982442

Date of issue: 16-Dec-2021

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(LES-PRE-20349)

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Contents

r0p0 implementation fixes

Note the following errata might be fixed in some implementations of r0p0. This can be determined by reading the REVIDR_EL1 register where a set bit indicates that the erratum is fixed in this part.

REVIDR_EL1[0]	2001293 Fault info captured in FAR and ESR registers for LDP 64-bit variant could be incorrect

Note that there is no change to the MIDR_EL1 which remains at r0p0. Software will identify this release through the combination of MIDR_EL1 and REVIDR_EL1.

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The **errata summary table** identifies errata that have been fixed in each product revision.

16-Dec-2021: Changes in document version v9.0

ID	Status	Area	Category	Summary
2001293	Updated	Programmer	Category A	Fault info captured in FAR and ESR registers for LDP 64-bit variant could be incorrect
2002655	Updated	Programmer	Category B	Embedded Trace of WFI or WFE instructions might corrupt PE architectural state
2009478	Updated	Programmer	Category B	RAS errors during core power down might cause a deadlock
2017090	Updated	Programmer	Category B	TRBE and SPE writes to MTE tagged pages might not report external aborts
2025414	Updated	Programmer	Category B	Streaming STG and STG2 performance lower than expected with TCF=NONE
2036776	Updated	Programmer	Category B	Reads of ERRIDR_EL1.NUM return an incorrect value
2048466	Updated	Programmer	Category B	Utility Bus register accesses to reserved addresses of PE might hang
2067956	Updated	Programmer	Category B	Loss of MTE tag coherency with L2 cache tag ECC errors
2067961	Updated	Programmer	Category B	The trace data is not flushed completely during a TSB instruction executed in prohibited region
2138956	Updated	Programmer	Category B	Executing a WFI or WFE instruction after a STREX instruction might result in a deadlock under specific conditions
2138958	Updated	Programmer	Category B	Execution of ST2G instructions in close proximity might cause loss of MTE allocation tag data
2139208	Updated	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode
2180384	Updated	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1
2189731	Updated	Programmer	Category B	The CPP instruction will apply to an incorrect EL context
2242400	Updated	Programmer	Category B	PDP deadlock due to CMP/CMN + B.AL/B.NV fusion
2242415	Updated	Programmer	Category B	A CFP instruction might not invalidate the correct resources
2253138	Updated	Programmer	Category B	TRBE might cause a data write to an out-of-range address which is not reserved for TRBE
2280757	Updated	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits
2326639	Updated	Programmer	Category B	Denied power down request might prevent completion of future power down request

ID	Status	Area	Category	Summary
2376738	New	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch
2388448	New	Programmer	Category B	A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing
2388450	New	Programmer	Category B	Translation table walk folding into an L1 prefetch might cause data corruption
2340933	New	Programmer	Category B (rare)	AMBA CHI TXREQ starvation due to unfair PCrdGrant assignment
2002685	Updated	Programmer	Category C	DRPS might not execute correctly in Debug state with SCTLR_ELx.IESB set in the current EL
2009482	Updated	Programmer	Category C	Execution of STG instructions in close proximity might incorrectly write MTE Allocation Tag to memory more than once
2025410	Updated	Programmer	Category C	DSB might not guarantee completion of direct reads of L2 cache memories
2033429	Updated	Programmer	Category C	Corrupted register state results from executing specific form of SEL instruction followed by SVE AESMC or AESIMC instruction
2048467	Updated	Programmer	Category C	CPU might fetch incorrect instruction from a page programmed as non-cacheable in stage-1 translation and as device memory in stage-2 translation
2052733	Updated	Programmer	Category C	ER1PFGCTL.MV is improperly implemented as Read/Write
2067959	Updated	Programmer	Category C	External aborts for streaming writes to MTE tagged pages may report multiple errors
2067960	Updated	Programmer	Category C	Trace data lost during collection stop in TRBE
2067962	Updated	Programmer	Category C	L3D_CACHE_ALLOC PMU inaccurate when using WriteEvictOrEvict transactions
2072986	Updated	Programmer	Category C	An execution of MSR instruction might not update the destination register correctly when an external debugger initiates APB write operation to update debug registers
2138952	Updated	Programmer	Category C	External APB write to a register located at offset 0x084 might incorrectly issue a write to External Debug Instruction Transfer Register
2138954	Updated	Programmer	Category C	Incorrect Fault Status code reported for predicated SVE op
2138955	Updated	Programmer	Category C	Tag check fail might not be reported for an unaligned predicated SVE store
2138959	Updated	Programmer	Category C	OSECCR_EL1/EDECCR is incorrectly included in the Warm Reset domain
2138960	Updated	Programmer	Category C	Extra A-sync packet might get written to Trace Buffer in Trace prohibited region
2139204	Updated	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur
2139205	Updated	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd

ID	Status	Area	Category	Summary
2139207	Updated	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level
2149120	Updated	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely
2153906	Updated	Programmer	Category C	Collision bit in PMBSR is reported incorrectly when there are multiple errors on SPE writes
2189737	Updated	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect
2189738	Updated	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data
2189739	Updated	Programmer	Category C	PMU_HOVFS event not always exported when self-hosted trace is disabled
2218242	Updated	Programmer	Category C	Some SVE PMU events count incorrectly
2218243	Updated	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect
2240288	Updated	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands
2242397	Updated	Programmer	Category C	Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering
2242404	Updated	Programmer	Category C	64 bit source SVE PMULLB/T not considered Cryptography instruction
2242416	Updated	Programmer	Category C	An SError might not be reported for an atomic store that encounters data poison
2253154	Updated	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered
2276004	New	Programmer	Category C	Incorrect Fault Status Code reported on a SPE buffer translation fault
2280302	Updated	Programmer	Category C	Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work
2280397	New	Programmer	Category C	PMU L1D_CACHE_REFILL_OUTER is inaccurate
2307062	Updated	Programmer	Category C	Reads of DISR_EL1 incorrectly return 0s while in Debug State
2307063	Updated	Programmer	Category C	DRPS instruction is not treated as UNDEFINED at EL0 in Debug state
2307064	Updated	Programmer	Category C	ELR_ELx[63:48] might hold incorrect value when PE disables address translation
2307065	Updated	Programmer	Category C	TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled
2307066	Updated	Programmer	Category C	L1 MTE Tag poison is not cleared
2341660	New	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered
2341661	New	Programmer	Category C	ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk

ID	Status	Area	Category	Summary
2341669	New	Programmer	Category C	SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions
2341671	New	Programmer	Category C	Lower priority exception might be reported when abort condition is detected at both stages of translation
2346744	New	Programmer	Category C	CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1
2346745	New	Programmer	Category C	L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop
2393116	New	Programmer	Category C	L1 Data poison is not cleared by a store

08-Oct-2021: Changes in document version v8.0

ID	Status	Area	Category	Summary
2009478	Updated	Programmer	Category B	RAS errors during core power down might cause a deadlock
2242415	Updated	Programmer	Category B	A CFP instruction might not invalidate the correct resources
2280757	New	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits
2326639	New	Programmer	Category B	Denied power down request might prevent completion of future power down request
2149120	Updated	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely
2240288	New	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands
2280302	New	Programmer	Category C	Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work
2307062	New	Programmer	Category C	Reads of DISR_EL1 incorrectly return 0s while in Debug State
2307063	New	Programmer	Category C	DRPS instruction is not treated as UNDEFINED at EL0 in Debug state
2307064	New	Programmer	Category C	ELR_ELx[63:48] might hold incorrect value when PE disables address translation
2307065	New	Programmer	Category C	TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled
2307066	New	Programmer	Category C	L1 MTE Tag poison is not cleared

16-Jul-2021: Changes in document version v7.0

ID	Status	Area	Category	Summary
2180384	New	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1
2242400	New	Programmer	Category B	PDP deadlock due to CMP/CMN + B.AL/B.NV fusion
2242415	New	Programmer	Category B	A CFP instruction might not invalidate the correct resources
2253138	New	Programmer	Category B	TRBE might cause a data write to an out-of-range address which is not reserved for TRBE
2242397	New	Programmer	Category C	Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering
2242404	New	Programmer	Category C	64 bit source SVE PMULLB/T not considered Cryptography instruction
2242416	New	Programmer	Category C	An SError might not be reported for an atomic store that encounters data poison
2253154	New	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered

08-Jun-2021: Changes in document version v6.0

ID	Status	Area	Category	Summary
2002655	Updated	Programmer	Category B	Embedded Trace of WFI or WFE instructions might corrupt PE architectural state
2189731	New	Programmer	Category B	The CPP instruction will apply to an incorrect EL context
2149120	New	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely
2153906	New	Programmer	Category C	Collision bit in PMBSR is reported incorrectly when there are multiple errors on SPE writes
2189737	New	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect
2189738	New	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data
2189739	New	Programmer	Category C	PMU_HOVFS event not always exported when self-hosted trace is disabled
2218242	New	Programmer	Category C	Some SVE PMU events count incorrectly
2218243	New	Programmer	Category C	FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect

14-Apr-2021: Changes in document version v5.0

ID	Status	Area	Category	Summary
2138953	New	Programmer	Category B	Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock
2138956	New	Programmer	Category B	Executing a WFI or WFE instruction after a STREX instruction might result in a deadlock under specific conditions
2138958	New	Programmer	Category B	Execution of ST2G instructions in close proximity might cause loss of MTE allocation tag data
2139208	New	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode
2138952	New	Programmer	Category C	External APB write to a register located at offset 0x084 might incorrectly issue a write to External Debug Instruction Transfer Register
2138954	New	Programmer	Category C	Incorrect Fault Status code reported for predicated SVE op
2138955	New	Programmer	Category C	Tag check fail might not be reported for an unaligned predicated SVE store
2138959	New	Programmer	Category C	OSECCR_EL1/EDECCR is incorrectly included in the Warm Reset domain
2138960	New	Programmer	Category C	Extra A-sync packet might get written to Trace Buffer in Trace prohibited region
2139204	New	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur
2139205	New	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd
2139206	New	Programmer	Category C	MPAM value associated with instruction fetch might be incorrect
2139207	New	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level

02-Feb-2021: Changes in document version v4.0

ID	Status	Area	Category	Summary
2036776	New	Programmer	Category B	Reads of ERRIDR_EL1.NUM return an incorrect value
2048466	New	Programmer	Category B	Utility Bus register accesses to reserved addresses of PE might hang
2067956	New	Programmer	Category B	Loss of MTE tag coherency with L2 cache tag ECC errors
2067961	New	Programmer	Category B	The trace data is not flushed completely during a TSB instruction executed in prohibited region
2048467	New	Programmer	Category C	CPU might fetch incorrect instruction from a page programmed as non-cacheable in stage-1 translation and as device memory in stage-2 translation
2052733	New	Programmer	Category C	ER1PFGCTL.MV is improperly implemented as Read/Write
2067959	New	Programmer	Category C	External aborts for streaming writes to MTE tagged pages may report multiple errors
2067960	New	Programmer	Category C	Trace data lost during collection stop in TRBE
2067962	New	Programmer	Category C	L3D_CACHE_ALLOC PMU inaccurate when using WriteEvictOrEvict transactions
2072986	New	Programmer	Category C	An execution of MSR instruction might not update the destination register correctly when an external debugger initiates APB write operation to update debug registers

08-Dec-2020: Changes in document version v3.0

ID	Status	Area	Category	Summary
2009478	New	Programmer	Category B	RAS errors during core power down might cause a deadlock
2017090	New	Programmer	Category B	TRBE and SPE writes to MTE tagged pages might not report external aborts
2025414	New	Programmer	Category B	Streaming STG and STG2 performance lower than expected with TCF=NONE
2025410	New	Programmer	Category C	DSB might not guarantee completion of direct reads of L2 cache memories
2033429	New	Programmer	Category C	Corrupted register state results from executing specific form of SEL instruction followed by SVE AESMC or AESIMC instruction

06-Nov-2020: Changes in document version v2.0

ID	Status	Area	Category	Summary
2001293	New	Programmer	Category A	Fault info captured in FAR and ESR registers for LDP 64-bit variant could be incorrect
2002655	New	Programmer	Category B	Embedded Trace of WFI or WFE instructions might corrupt PE architectural state
2002685	New	Programmer	Category C	DRPS might not execute correctly in Debug state with SCTLR_ELx.IESB set in the current EL
2009482	New	Programmer	Category C	Execution of STG instructions in close proximity might incorrectly write MTE Allocation Tag to memory more than once

16-Oct-2020: Changes in document version v1.0

ID	Status	Area	Category	Summary
1982438	New	Programmer	Category C	Noncompliance with prioritization of Exception Catch debug events
1982439	New	Programmer	Category C	The core might report incorrect fetch address to FAR_ELx when the core is fetching an instruction from a virtual address associated with page table entry which has been modified
1982440	New	Programmer	Category C	IDATAn_EL3 might represent incorrect value after direct memory access to internal memory for Instruction TLB

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
2001293	Programmer	Category A	Fault info captured in FAR and ESR registers for LDP 64-bit variant could be incorrect	r0p0	r0p1
2002655	Programmer	Category B	Embedded Trace of WFI or WFE instructions might corrupt PE architectural state	r0p0	r0p1
2009478	Programmer	Category B	RAS errors during core power down might cause a deadlock	r0p0	r0p1
2017090	Programmer	Category B	TRBE and SPE writes to MTE tagged pages might not report external aborts	r0p0	r0p1
2025414	Programmer	Category B	Streaming STG and STG2 performance lower than expected with TCF=NONE	r0p0	r0p1
2036776	Programmer	Category B	Reads of ERRIDR_EL1.NUM return an incorrect value	r0p0	r0p1
2048466	Programmer	Category B	Utility Bus register accesses to reserved addresses of PE might hang	r0p0	r0p1
2067956	Programmer	Category B	Loss of MTE tag coherency with L2 cache tag ECC errors	r0p0	r0p1
2067961	Programmer	Category B	The trace data is not flushed completely during a TSB instruction executed in prohibited region	r0p0	r0p1
2138953	Programmer	Category B	Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock	r0p0	Open
2138956	Programmer	Category B	Executing a WFI or WFE instruction after a STREX instruction might result in a deadlock under specific conditions	r0p0	r0p1
2138958	Programmer	Category B	Execution of ST2G instructions in close proximity might cause loss of MTE allocation tag data	r0p0	r0p1
2139208	Programmer	Category B	Trace data might get overwritten in TRBE FILL mode	r0p0	r0p1
2180384	Programmer	Category B	Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1	r0p0	r0p1
2189731	Programmer	Category B	The CPP instruction will apply to an incorrect EL context	r0p0	r0p1
2242400	Programmer	Category B	PDP deadlock due to CMP/CMN + B.AL/B.NV fusion	r0p0	r0p1
2242415	Programmer	Category B	A CFP instruction might not invalidate the correct resources	r0p0	r0p1
2253138	Programmer	Category B	TRBE might cause a data write to an out-of-range address which is not reserved for TRBE	r0p0	r0p1
2280757	Programmer	Category B	A CFP instruction might execute with incorrect upper ASID or VMID bits	r0p0	r0p1

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2326639	Programmer	Category B	Denied power down request might prevent completion of future power down request	r0p0	r0p1
2376738	Programmer	Category B	Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch	r0p0	r0p1
2388448	Programmer	Category B	A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing	r0p0	r0p1
2388450	Programmer	Category B	Translation table walk folding into an L1 prefetch might cause data corruption	r0p0	r0p1
2340933	Programmer	Category B (rare)	AMBA CHI TXREQ starvation due to unfair PCrdGrant assignment	r0p0	r0p1
1982438	Programmer	Category C	Noncompliance with prioritization of Exception Catch debug events	r0p0	Open
1982439	Programmer	Category C	The core might report incorrect fetch address to FAR_ELx when the core is fetching an instruction from a virtual address associated with page table entry which has been modified	r0p0	Open
1982440	Programmer	Category C	IDATAn_EL3 might represent incorrect value after direct memory access to internal memory for Instruction TLB	r0p0	Open
2002685	Programmer	Category C	DRPS might not execute correctly in Debug state with SCTLR_ELx.IESB set in the current EL	r0p0	r0p1
2009482	Programmer	Category C	Execution of STG instructions in close proximity might incorrectly write MTE Allocation Tag to memory more than once	r0p0	r0p1
2025410	Programmer	Category C	DSB might not guarantee completion of direct reads of L2 cache memories	r0p0	r0p1
2033429	Programmer	Category C	Corrupted register state results from executing specific form of SEL instruction followed by SVE AESMC or AESIMC instruction	r0p0	r0p1
2048467	Programmer	Category C	CPU might fetch incorrect instruction from a page programmed as non-cacheable in stage-1 translation and as device memory in stage-2 translation	r0p0	r0p1
2052733	Programmer	Category C	ER1PFGCTL.MV is improperly implemented as Read/Write	r0p0	r0p1
2067959	Programmer	Category C	External aborts for streaming writes to MTE tagged pages may report multiple errors	r0p0	r0p1
2067960	Programmer	Category C	Trace data lost during collection stop in TRBE	r0p0	r0p1
2067962	Programmer	Category C	L3D_CACHE_ALLOC PMU inaccurate when using WriteEvictOrEvict transactions	r0p0	r0p1
2072986	Programmer	Category C	An execution of MSR instruction might not update the destination register correctly when an external debugger initiates APB write operation to update debug registers	r0p0	r0p1

ID	Area	Category	Summary	Found in versions	Fixed in version
2138952	Programmer	Category C	External APB write to a register located at offset 0x084 might incorrectly issue a write to External Debug Instruction Transfer Register	r0p0	r0p1
2138954	Programmer	Category C	Incorrect Fault Status code reported for predicated SVE op	r0p0	r0p1
2138955	Programmer	Category C	Tag check fail might not be reported for an unaligned predicated SVE store	r0p0	r0p1
2138959	Programmer	Category C	OSECCR_EL1/EDECCR is incorrectly included in the Warm Reset domain	r0p0	r0p1
2138960	Programmer	Category C	Extra A-sync packet might get written to Trace Buffer in Trace prohibited region	r0p0	r0p1
2139204	Programmer	Category C	Speculative access to a recently unmapped physical address previously containing page tables might occur	r0p0	r0p1
2139205	Programmer	Category C	L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd	r0p0	r0p1
2139206	Programmer	Category C	MPAM value associated with instruction fetch might be incorrect	r0p0	Open
2139207	Programmer	Category C	Data abort on SVE first fault load might be routed to incorrect Exception level	r0p0	r0p1
2149120	Programmer	Category C	A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely	r0p0	r0p1
2153906	Programmer	Category C	Collision bit in PMBSR is reported incorrectly when there are multiple errors on SPE writes	r0p0	r0p1
2189737	Programmer	Category C	PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect	r0p0	r0p1
2189738	Programmer	Category C	Direct access of L2 data RAMs using RAMINDEX returns incomplete data	r0p0	r0p1
2189739	Programmer	Category C	PMU_HOVFS event not always exported when self-hosted trace is disabled	r0p0	r0p1
2218242	Programmer	Category C	Some SVE PMU events count incorrectly	r0p0	r0p1
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2240288	Programmer	Category C	Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands	r0p0	r0p1
2242397	Programmer	Category C	Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering	r0p0	r0p1

ID	Area	Category	Summary	Found in versions	Fixed in version
2242404	Programmer	Category C	64 bit source SVE PMULLB/T not considered Cryptography instruction	r0p0	r0p1
2242416	Programmer	Category C	An SError might not be reported for an atomic store that encounters data poison	r0p0	r0p1
2253154	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered	r0p0	r0p1
2276004	Programmer	Category C	Incorrect Fault Status Code reported on a SPE buffer translation fault	r0p0	r0p1
2280302	Programmer	Category C	Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work	r0p0	r0p1
2280397	Programmer	Category C	PMU L1D_CACHE_REFILL_OUTER is inaccurate	r0p0	r0p1
2307062	Programmer	Category C	Reads of DISR_EL1 incorrectly return 0s while in Debug State	r0p0	r0p1
2307063	Programmer	Category C	DRPS instruction is not treated as UNDEFINED at EL0 in Debug state	r0p0	r0p1
2307064	Programmer	Category C	ELR_ELx[63:48] might hold incorrect value when PE disables address translation	r0p0	r0p1
2307065	Programmer	Category C	TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled	r0p0	r0p1
2307066	Programmer	Category C	L1 MTE Tag poison is not cleared	r0p0	r0p1
2341660	Programmer	Category C	ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered	r0p0	r0p1
2341661	Programmer	Category C	ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk	r0p0	r0p1
2341669	Programmer	Category C	SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions	r0p0	r0p1
2341671	Programmer	Category C	Lower priority exception might be reported when abort condition is detected at both stages of translation	r0p0	r0p1
2346744	Programmer	Category C	CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1	r0p0	r0p1
2346745	Programmer	Category C	L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop	r0p0	r0p1
2393116	Programmer	Category C	L1 Data poison is not cleared by a store	r0p0	r0p1

Errata descriptions

Category A

2001293
Fault info captured in FAR and ESR registers for LDP 64-bit variant might be incorrect

Status

Fault Type: Programmer Category A
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain conditions, the FAR (Fault Address Register) and ESR (Exception Syndrome Register) could have incorrect values when the LDP (Load Pair) 64-bit variant generates an abort.

Configurations affected

All configurations are affected.

Conditions

All of the following conditions must be met:

1. The LDP 64-bit variant crosses a page boundary.
2. Data read from lower bytes on the first page results in a synchronous abort due to an internal ECC error, external abort, or MTE tag check fail.
3. Data read from upper bytes on the second page results in alignment fault, MMU fault, or watchpoint exception.

Implications

If the above conditions are met the contents of the FAR and ESR registers could have incorrect values.

Workaround

This erratum can be avoided by setting CPUACTLR5_EL1[10] to 1. Setting CPUACTLR5_EL1[10] to 1 would have a significant performance (approximately 20%) impact on streaming workloads that use LDP 64-bit variant. Performance impact on non streaming workloads would be much smaller (approximately 1%).

Category A (rare)

There are no errata in this category.

Category B

2002655
Embedded Trace of WFI or WFE instructions might corrupt PE architectural state

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Executing a **WFI** or **WFE** instruction with Embedded Trace enabled might corrupt AArch32 PSTATE.ITSTATE, AArch64 PSTATE.BTYPE, or trace information intended for Embedded Trace, resulting in architecture violations.

Configurations Affected

This erratum affects all configurations.

Conditions

The erratum occurs under the following conditions:

1. Embedded Trace is enabled.
2. A **WFI** or **WFE** instruction is executed.

Implications

Under certain internal timing conditions exacerbated by a high frequency of branch instructions and/or AArch32 IT instructions, the PE might corrupt PSTATE.ITSTATE, PSTATE.BTYPE, or trace information. Corruption of any of these values might lead to any of the following architecture violations:

- Applying conditionality erroneously to AArch32 instructions (wrong condition code applied, or condition code applied when it should not be, or failing to apply a condition code when it should be).
- Applying erroneous BTYPE information to AArch64 instructions in guarded pages (wrong BTYPE value resulting in erroneous Branch Target Exceptions or failing to report a Branch Target Exception).
- Reporting erroneous trace information to Embedded Trace.

Workaround

This erratum can be worked around by using the instruction patching mechanism. This can be done through the following write sequence to several IMPLEMENTATION DEFINED registers. The code sequence should be applied early in the boot sequence prior to any of the possible errata conditions being met. There is no performance or power impact associated with this workaround.

```
LDR x0,=0x6
MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
LDR x0,=0xF3A08002
MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
LDR x0,=0xFFF0F7FE
MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
LDR x0,=0x40000001003ff
MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0

LDR x0,=0x7
MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
LDR x0,=0xBF200000
MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
LDR x0,=0xFFEF0000
MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
LDR x0,=0x40000001003f3
MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0

ISB
```

2009478
RAS errors during core power down might cause a deadlock

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

If a Reliability, Availability, and Serviceability (RAS) error occurs when a core is being powered down, then the power down sequence is designed to be aborted so that the error can be handled by software. As explained in this erratum, the power down sequence might complete despite the error occurring, or it might cause a deadlock.

Configurations affected

All configurations are affected.

Conditions

1. The ERXCTLR_EL1.ED bit is set for any of the core error records, and at least one of the CI, DUI, CFI, FI, or UI bits is set.
2. Software running on the core sets the CPUPWRCTLR.CORE_PWRDN_EN bit and executes a **WFI** instruction.
3. The core Power Policy Unit (PPU) requests that the core transitions from the ON power mode to either the OFF or OFF_EMU power mode.
4. During the L1 or L2 cache clean and invalidate done by the power transition, a RAS error occurs that causes any of the **nCOREFAULTIRQ**, **nCOREERRIRQ**, **nCOMPLEXFAULTIRQ**, or **nCOMPLEXERRIRQ** pins to be asserted.

Implications

The PPU will see the power down request being denied because of the RAS error, however the core will not wake up from the **WFI** instruction and therefore software is not able to handle the error. If the PPU requests the core to power down again, either because it is set to dynamic mode, or because the component programming the PPU requests the power down again, then the second power down might either:

- Complete and power off the core, despite the fact that the error has not been handled.
- Deadlock, preventing the power down from completing.

There is still substantial benefit being gained from the ECC logic. There might be a negligible increase in overall system failure rate because of this erratum.

Workaround

The ERXCTLR_EL1.ED bit should be cleared for all the core error records before software sets the CPUPWRCTLR.CORE_PWRDN_EN bit to request a power down. This will cause any error detected during the power down to be ignored. In systems that are particularly concerned about errors during this time, software can clean and invalidate the L1 and L2 caches before clearing the ERXCTLR_EL1.ED bit. This will minimise, but not eliminate, the probability of detecting an error during the powerdown, but at the expense of a longer time to execute the power down sequence.

2017090
TRBE and SPE writes to MTE tagged pages might not report external aborts

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Memory writes due to the Trace Buffer Extension (TRBE) or Statistical Profiling Extension (SPE) to memory pages that are Tagged via the Memory Tagging Extension and present in the PE caches might fail to report external aborts.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

1. PE enables the TRBE or SPE features.
2. TRBE or SPE issues a write to a memory page that is marked MTE Tagged.
3. Interconnect returns a completion response with an error indication - Poison, DErr, or NDErr.

Implications

If the above conditions are met, the PE might fail to record the external abort in TRBSR_EL1.EA (TRBE) or PMBSR_EL1 (SPE).

Workaround

If the external abort conditions are non-transient, a read of the TBRE or SPE memory buffers will observe the same external abort condition as the write and take a data abort. If the external abort conditions are transient, memory pages used for TBRE and SPE can be marked as Untagged.

2025414
Streaming STG and STG2 performance lower than expected with TCF=NONE

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When writing MTE allocation tags, STG and STG2 instructions might encounter lower than expected performance when SCTLR_ELx.TCF is set to NONE.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE executes a series of STG or STG2 instruction with SCTLR_ELx.TCF set to NONE.

Implications

If the above conditions are met, the measured bandwidth might be one half of what is expected.

Workaround

Disable store issue prefetching by setting CPUECLTR_EL1[8] to 1. Note that doing so might incur a performance penalty of 0 to 0.3%.

2036776
Reads of ERRIDR_EL1.NUM return an incorrect value

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Reads of ERRIDR_EL1.NUM may incorrectly return a value of 0x1. The correct value is 0x2.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The PE reads ERRIDR_EL1.

Implications

If the above conditions are met, the value read for ERRIDR_EL1.NUM may incorrectly report as 0x1.

Workaround

Software should ignore the value in ERRIDE_EL1.NUM, and always consider ERRIDR_EL1.NUM to be 0x2.

2048466
Utility Bus register accesses to reserved addresses of PE might hang

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Utility Bus register accesses to some reserved regions of the PE might be ignored and result in a hang.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under the following condition:

- Utility Bus Read/Write to a reserved region in PE is executed.

Implications

The Utility Bus register access to DSU might not complete, resulting in a hang.

Workaround

Utility Bus reserved regions of page size in the PE should not be mapped by an MMU onto system memory. Also, these regions should not be made accessible by lower ELs than host.

When using an external debugger, accesses to Utility Bus reserved addresses should be avoided.

2067956
Loss of MTE tag coherency with L2 cache tag ECC errors

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Dirty MTE tags contained in the L1 cache might be lost when performing streaming writes in imprecise MTE checking mode and specific timing conditions occur that coincide with an L2 tag single-bit ECC error.

Configurations Affected

This erratum affects all configurations of Matterhorn and the 512kB L2 configuration of Perseus when using imprecise MTE checking mode.

Conditions

1. PE issues streaming write to L2 cache.
2. Specific timing conditions and an L2 tag single-bit ECC error cause an L1 eviction to provide updated MTE tags from the L1 cache to the same address as the streaming write while older MTE tags are being read from the L2 cache.

Implications

If the above conditions are met, in rare timing conditions the updated MTE tags from the L1 cache might be lost and the streaming write might fail its MTE tag check.

Workaround

Set CPUACTLR_EL1[46] to force L2 tag ECC inline correction mode. This mode incurs a 1-cycle latency penalty and thus degrades CPU performance by less than 1%.

2067961
The trace data is not flushed completely during a TSB instruction executed in prohibited region

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When Embedded Trace Extension (ETE) is in trace prohibited region, and a TSB instruction is executed, any trace data associated with the instructions before the TSB must be observable in memory. Because of this erratum, four bytes of trace data are not pushed to the memory before completing the TSB instruction and those bytes might get lost or might get written to memory in next context.

Configurations Affected

This erratum affects all configurations.

Conditions

1. ETE is enabled.
2. ETE is in trace prohibited region.
3. TRBE is enabled.
4. TSB instruction is executed.

Implications

Four bytes of trace data before TSB instruction might get lost or might get written to memory in next context.

Workaround

To avoid this erratum, software can execute two sequential TSB instructions in any code where one TSB instruction is expected to be required.

2138953
Disabling of data prefetcher with outstanding prefetch TLB miss might cause a deadlock

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Open.

Description

If the data prefetcher is disabled (by an MSR to CPUECTLR register) while a prefetch TLB miss is outstanding, the processor might deadlock on the next context switch.

Configurations Affected

All configurations are affected.

Conditions

- MSR write to CPUECTLR register that disables the data prefetcher.
- A TLB miss from the prefetch TLB is outstanding.

Implications

If the above conditions are met, a deadlock might occur on the next context switch.

Workaround

- Workaround option 1:
  If the following code surrounds the MSR, it will prevent the erratum from happening:
  - cpp
  - dsb
  - isb
  - MSR CPUECTLR - disabling the prefetcher
  - isb

- Workaround option 2:
  Place the data prefetcher in the most conservative mode instead of disabling it. This will greatly reduce prefetches but not eliminate them. This is accomplished by writing the following bits to the value indicated:
  - ectlr2[14:11], PF_MODE= 4'b1001

2138956
Executing a WFI or WFE instruction after a STREX instruction might result in a deadlock under specific conditions

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain micro-architectural conditions, executing a WFI or WFE instruction after a STREX that has encountered an external abort might result in a deadlock.

Configurations Affected

This erratum affects all configurations where the BROADCASTMTE pin is HIGH.

Conditions

1. Memory tagging is enabled.
2. A STREX instruction executed in MTE precise mode encounters an external abort or poisoned MTE tag.
3. A WFI or WFE instruction is executed.

Implications

If the above conditions are met, then, under specific micro-architectural conditions, the core might deadlock.

Workaround

This erratum can be avoided by inserting a sequence of 16 DMB ST instructions prior to WFI or WFE. Performance impact is expected to be negligible in real systems. This sequence can be implemented through execution of the following code at EL3 as soon as possible after boot:

```
LDR x0,=0x3
 MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
 LDR x0,=0xF3A08002
 MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
 LDR x0,=0xFFF0F7FE
 MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
 LDR x0,=0x10002001003FF
 MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0

LDR x0,=0x4
 MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
```

```
LDR x0,=0xBF200000
MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
LDR x0,=0xFFEF0000
MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
LDR x0,=0x10002001003F3
MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0

ISB
```

2138958
Execution of ST2G instructions in close proximity might cause loss of MTE allocation tag data

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain micro-architectural conditions, an ST2G instruction that crosses a 32-byte boundary might not write part of the MTE allocation tag to memory.

Configurations Affected

This erratum affects all configurations where the BROADCASTMTE pin is HIGH.

Conditions

1. Memory tagging is enabled.
2. Two or more ST2G instructions are executed in close proximity to the same cache line such that they miss in the L1 cache.
3. One of the ST2G instructions crosses a 32-byte boundary.

Implications

If the above conditions are met, then under specific micro-architectural conditions, the ST2G that crosses the 32-byte boundary might not write part of the MTE allocation tag to memory.

Workaround

This erratum can be avoided by setting CPUACTLR5_EL1[13] to 1. Setting CPUACTLR5_EL1[13] to 1 is expected to result in a small performance degradation for workloads that use MTE (approximately 1.6% when using MTE imprecise mode, 0.9% for MTE precise mode).

2139208
Trace data might get overwritten in TRBE FILL mode

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Trace Buffer memory size is defined using base pointer and limit pointer in the Trace Buffer Extension (TRBE) programming model. In trace buffer fill mode, TRBE is expected to generate an interrupt and stop the collection of trace after reaching the limit pointer. Due to this erratum, under some microarchitecture conditions, TRBE might roll back to the base pointer after generating an interrupt and continue to write at the base pointer, and up to three cache lines after the base pointer before the collection stops.

Configurations Affected

This erratum affects all configurations.

Conditions

1. ETE and TRBE are enabled.
2. ETE is in a trace allowed region.
3. TRBLIMITR_EL1[2:1] is programmed to 2'b00.

Implications

Due to this erratum, trace data present at the base pointer location and up to three cache lines after the base pointer might get overwritten. The current write pointer also increments by same number of cache line locations.

Workaround

Software can program 256 bytes of ignore packets starting from the base pointer and offset the write pointer TRBPTR_EL1 by 256 bytes before enabling TBE. That ensures oldest trace is not corrupted.

2180384
Enabling TRBE might cause a data write to a page with the wrong ASID when owning Exception level is EL1

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The Trace Buffer Extension (TRBE) can be used by software to store trace packets from Embedded Trace Extension (ETE) unit to memory. The TRBE unit interfaces with the MMU for translating a virtual address to a physical address. Once a physical address is available, the TRBE unit sends trace packets to the L2 unit to be stored to the memory. The TRBE unit requests a new translation to the MMU when a virtual address crosses the 4K page boundary. Due to this erratum, if a pending translation request from Exception level EL0 or EL1 is serviced after the PE switches context to Exception level EL2, then translation with an incorrect ASID might be provided to the TRBE unit. This can lead to a write to a page with the incorrect ASID.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The TRBE is enabled.
2. Owning Exception level is EL1.
3. TRBLIMITR_EL1.nVM is set to 0, such that the trace buffer pointer addresses are virtual addresses in the EL1&0 translation regime using the current ASID from TTBRx_EL1. This means that the page is marked nG (non-global page).
4. The TRBE unit requests a memory translation request.
5. Before the above memory translation request completes, a context switch occurs from EL0 or EL1, to EL2.

Implications

If the above conditions are met, under certain microarchitectural conditions, incorrect physical address and page attributes from a different ASID might be provided to the TRBE unit. The TRBE might then write to memory using incorrect page attributes from another ASID, leading to a write that is not expected.

Workaround

The software should use global pages (nG=0) for the pages that are used by the TRBE to store data when owning Exception level is EL1.

2189731
The CPP instruction will apply to an incorrect EL context

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The **CPP** instruction will not operate on the desired EL as encoded in the instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following condition:

1. A **CPP** instruction is executed.

Implications

The **CPP** instruction will cause the hardware prefetcher to invalidate the hardware prefetcher state associated with an EL other than the EL that is encoded in the instruction.

Workaround

Set CPUACTLR5_EL1[44] which will cause the **CPP** instruction to invalidate the hardware prefetcher state trained from any EL.

2242400
PDP deadlock due to CMP/CMN + B.AL/B.NV fusion

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When Performance Defined Power (PDP) is enabled, a Compare (CMP) or Compare negative (CMN) instruction followed by a conditional branch of form B.AL or B.NV might cause a deadlock.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PDP configuration is enabled.
2. Execution of CMP/CMN, followed by B.AL/B.NV.

Implications

If above conditions are met, then a deadlock might result, requiring a reset of the processor.

Workaround

This erratum can be avoided by setting CPUACTLR5_EL1[17] to 1 and applying following patch. These instructions are not expected to be present in the code often, so any performance impact should be minimal. The code sequence should be applied early in the boot sequence prior to any of the possible errata conditions being met.

```
LDR x0,=0x2
MSR S3_6_c15_c8_0,x0 ; MSR CPUPSELR_EL3, X0
LDR x0,=0x10F600E000
MSR S3_6_c15_c8_2,x0 ; MSR CPUPOR_EL3, X0
LDR x0,=0x10FF80E000
MSR S3_6_c15_c8_3,x0 ; MSR CPUPMR_EL3, X0
LDR x0,=0x80000000003FF
MSR S3_6_c15_c8_1,x0 ; MSR CPUPCR_EL3, X0
ISB
```

2242415
A CFP instruction might not invalidate the correct resources

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Executing a CFP instruction under certain conditions might not invalidate resources specified by the instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A CFP instruction is executed.
2. The Exception level specified in the instruction is EL0.
3. HCR_EL2.TGE==1 and HCR_EL2.E2H==1.

Implications

If the previous conditions are met, then the CFP instruction might not invalidate branch predictor resources associated with EL0 context managed by EL2.

Workaround

This erratum can be avoided by setting CPUACTLR_EL1[22]=1. Setting CPUACTLR_EL1[22] will cause the CFP instruction to invalidate all branch predictor resources regardless of context.

Using this workaround might cause the PE to encounter another erratum. Please refer to erratum ID 2243871 "ELR_ELx[63:48] might hold incorrect value when PE disables address translation" for more details.

2253138
TRBE might cause a data write to an out-of-range address which is not reserved for TRBE

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Trace buffer memory size is defined using base pointer and limit pointer in Trace Buffer Extension (TRBE) programming model. TRBE is expected to wrap to base pointer without crossing the limit pointer. Because of this erratum, under some conditions, TRBE might generate a write to the next virtually addressed page following the last page of TRBE address space.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Embedded Trace Extension (ETE) and TRBE are enabled.
2. ETE is in trace allowed region.
3. TRBE current pointer is at last page of Trace buffer.
4. TRBE requests translation for the last page.
5. LS indicates to TRBE that it is unable to service the translation request.

Implications

When previous conditions are met under rare microarchitectural conditions, TRBE might incorrectly generate a data write to the next virtually addressed page following the last page of Trace Buffer. This can lead to data corruption if that page is currently used by another application and result in loss of trace up to 64 bytes.

Workaround

The software can mark as not valid the next page following the last TRBE page, meaning the errant access will generate a Translation Fault buffer management event. This will prevent the data corruption but will not prevent the loss of trace data.

2280757
A CFP instruction might execute with incorrect upper ASID or VMID bits

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The upper 8 bits of ASID or VMID might be incorrect for a CFP instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A CFP is executed with EL0 target execution context and {HCR_EL2.TGE, HCR_EL2.E2H} is {1,1} and TCR_EL2.AS=0.
2. A CFP is executed at EL2 or EL3 and the target execution context is EL0 or EL1 and VTCR_EL2.VS=0.

Implications

If either of the previous conditions are met, then the CFP instruction might not invalidate branch predictor resources associated with EL0 or EL1 contexts.

Workaround

This erratum can be avoided by setting CPUACTLR_EL1[22]=1. Setting CPUACTLR_EL1[22] will cause the CFP instruction to invalidate all branch predictor resources regardless of context.

2326639
Denied power down request might prevent completion of future power down request

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

If a Processing Element (PE) initiates a power down request that is ultimately denied due to an external event, a future power down request might fail to complete.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE initiates a power down request (ON to OFF state transition) by setting CORE_PWRDN_EN and executing a WFI instruction.
2. PE completes the hardware flush of its caches.
3. An event, such as an external interrupt, causes an abort of the power down request.
4. PE returns to the ON state without performing a hardware reset.

Implications

If the above conditions are met, the PE might fail complete a subsequent power down request resulting in a deadlock.

Workaround

This erratum can be avoided by setting CPUACTLR2_EL1[36] to 1 before the power-down sequence that includes setting the CORE_PWRDN_EN bit and executing a WFI. This bit should be cleared on exiting WFI by any mechanism other than reset.

2376738
Continuous failing STREX because of another PE executing prefetch for store behind consistently mispredicted branch

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A PE executing a PLDW or PRFM PST instruction that lies on a mispredicted branch path might cause a second PE executing a store exclusive to the same cache line address to fail continuously.

Configurations Affected

This erratum affects all configurations.

Conditions

1. One PE is executing store exclusive.
2. A second PE has branches that are consistently mispredicted.
3. The second PE instruction stream contains a PLDW or PRFM PST instruction on the mispredicted path that accesses the same cache line address as the store exclusive executed by the first PE.
4. PLDW/PRFM PST causes an invalidation of the first PE's caches and a loss of the exclusive monitor.

Implications

If the above conditions are met, the store exclusive instruction might continuously fail.

Workaround

Set CPUACTLR2_EL1[0] to 1 to force PLDW/PFRM ST to behave like PLD/PRFM LD and not cause invalidations to other PE caches. There might be a small performance degradation to this workaround for certain workloads that share data.

2388448
A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A continuous stream of incoming DVM syncs may cause TRBE to prevent the CPU from forward progressing, while executing a WFx.

Configurations Affected

This erratum affects all configurations.

Conditions

The erratum occurs if all the following conditions are met:

- The PE executes a WFE or WFI instruction
- TRBE is in use and needs to write trace data to its buffer
- a continuous stream of DVM sync operations is received from other PEs

Implications

When the above conditions are met, the PE might be prevented from entering WFE or WFI, and the pending WFE or WFI operation cannot be interrupted.

Workaround

There is no workaround.

2388450
Translation table walk folding into an L1 prefetch might cause data corruption

Status

Fault Type: Programmer Category B
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A translation table walk that matches an existing L1 prefetch with a read request outstanding on CHI might fold into the prefetch, which might lead to data corruption for a future instruction fetch.

Configurations Affected

This erratum affects all configurations

Conditions

1. In specific microarchitectural situations, the PE merges a translation table walk request with an older hardware or software prefetch L2 cache miss request.

Implications

If the previous conditions are met, an unrelated instruction fetch might observe incorrect data.

Workaround

Disable folding of demand requests into older prefetches with L2 miss requests outstanding by setting CPUACTLR2_EL1[40] to 1.

Category B (rare)

2340933
AMBA CHI TXREQ starvation due to unfair PCrdGrant assignment

Status

Fault Type: Programmer Category B rare
Fault Status: Present in r0p0. Fixed in r0p1.

Description

AMBA CHI protocol credit grants might not be distributed in a fair manner inside the *Processing Element* (PE), leading to a livelock condition.

Configurations Affected

This erratum affects all configurations.

Conditions

Under specific micro-architectural conditions and the presence of protocol retries on the AMBA CHI interface, the PE might fail to assign protocol credits in a fair manner across L2 cache banks.

Implications

If the above conditions are met, a retried CHI request might never consume a protocol credit provided by a PCrdGrant response and will therefore not be re-issued to the interconnect, potentially leading to a deadlock of the PE.

Based on multiple generations of hardware with the same functionality, Arm has no evidence that systems operating in standard configurations are susceptible to this erratum.

Workaround

If a workaround is required, set CPUACTLR5_EL1[61] to 1.

Category C

1982438
Noncompliance with prioritization of Exception Catch debug events

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open.

Description

ARMv8.2 architecture requires that Debug state entry due to an Exception Catch debug event (generated on exception entry) occur before any asynchronous exception is taken at the first instruction in the exception handler. An asynchronous exception might be taken as a higher priority exception than Exception Catch and the Exception Catch might be missed altogether.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Debug Halting is allowed.
2. EDECCR bits are configured to catch exception entry to ELx.
3. A first exception is taken resulting in entry to ELx.
4. A second, asynchronous exception becomes visible at the same time as exception entry to ELx.
5. The second, asynchronous exception targets an Exception level ELy that is higher than ELx.

Implications

If the above conditions are met, the core might recognize the second exception and not enter Debug state as a result of Exception Catch on the first exception. When the handler for the second exception completes, software might return to execute the first exception handler, and assuming the core does not halt for any other reason, the first exception handler will be executed and entry to Debug state via Exception Catch will not occur.

Workaround

When setting Exception Catch on exceptions taken to an Exception level ELx, the debugger should do either or both of the following:

1. Ensure that Exception Catch is also set for exceptions taken to all higher Exception Levels, so that the second (asynchronous) exception generates an Exception Catch debug event.
2. Set Exception Catch for an Exception Return to ELx, so that when the second (asynchronous) exception handler completes, the exception return to ELx generates an Exception Catch debug event.

Additionally, when a debugger detects that the core has halted on an Exception Catch to an Exception level ELy, where y > x, it should check the ELR_ELy and SPSR_ELy values to determine whether the exception was taken on an ELx exception vector address, meaning an Exception Catch on entry to ELx has been missed.

1982439
The core might report incorrect fetch address to FAR_ELx when the core is fetching an instruction from a virtual address associated with a page table entry which has been modified

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open.

Description

When a core fetches an instruction from a virtual address that is associated with a page table entry which has been modified and the fetched block is affected by parity error, the core might report an incorrect address within the same 32B block onto the Fault Address Register (FAR).

Configurations Affected

All configurations are affected.

Conditions

1. The core fetches instructions from an aligned 32B virtual address block.
2. A page table entry associated with the above 32B aligned block is updated. The new translation would cause an instruction abort.
3. TLB holds the old translation since the synchronization process, for example, TLB Invalidate (TLBI) followed by Data Synchronization Barrier (DSB), was not completed.
4. Some of the fetched instructions are affected by parity error in I-cache data RAM.
5. Context synchronization events were not processed between the last executed instruction and the above instruction.

Implications

When the above conditions are satisfied, a core might report an incorrect fetch address to FAR_ELx. The address reported in FAR_ELx points at an earlier location in the same aligned 32B block. FAR_ELx[63:5] still points correct virtual address.

Workaround

There is no workaround.

1982440
IDATAn_EL3 might represent incorrect value after direct memory access to internal memory for Instruction TLB

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open.

Description

After implementation-defined RAMINDEX register is programmed to initiate direct memory access to internal memory for Instruction TLB, implementation-defined IDATAn_EL3 value represents unpredictable value.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Implementation-defined RAMINDEX register is programmed to initiate direct memory access to internal memory for Instruction TLB.

Implications

If the above conditions are met, IDATAn_EL3 register might represent incorrect value for Translation regime, VMID, ASID, and VA[48:21].

Workaround

There is no workaround.

2002685
DRPS might not execute correctly in Debug state with SCTLR_ELx.IESB set in the current EL

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

In Debug state with SCTLR_ELx.IESB set to 1, the **DRPS** (debug only) instruction does not execute properly. Only partial functionality of the **DRPS** instruction is performed.

Configurations Affected

This erratum affects all configurations.

Conditions

The erratum occurs under the following conditions:

1. Core is in Debug state.
2. SCTLR_ELx.IESB is set to 1 for the current exception level.
3. The **DRPS** instruction is executed.

Implications

If the above conditions are met, **DRPS** does not complete as intended, which might lead to an incorrect operation or result. Register data or memory will not be corrupted. There are also no security or privilege violations.

Workaround

The erratum can be avoided by clearing SCTLR_ELx.IESB, followed by insertion of an **ISB** and **ESB** instruction in code before the **DRPS** instruction.

2009482
Execution of STG instructions in close proximity might incorrectly write MTE Allocation Tag to memory more than once

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain micro-architectural conditions, an STG instruction might write MTE Allocation Tag to memory more than once.

Configurations Affected

This erratum affects all configurations where the **BROADCASTMTE** pin is HIGH.

Conditions

1. Memory tagging is enabled.
2. Two or more STG instructions that write both Allocation Tag and Data are executed in close proximity.
3. Above STG instructions access the same cache line address but different 32 bytes in memory.

Implications

If the above conditions are met, then under specific micro-architectural conditions Allocation Tag for the entire cache line may be written to memory twice. This is not expected to be an issue as Allocation Tags are written by only one software agent at a time. The value of Allocation Tag will not change between these two writes since there will not be another write to Allocation Tag from another PE.

Workaround

There is no workaround.

2025410
DSB might not guarantee completion of direct reads of L2 cache memories

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Direct reads of internal memories are implemented using a SYS #6, C15, C0, #0, <Xt> instruction executed in EL3. In response to this instruction, the PE reads an internal memory and places the contents in implementation defined DDATAx registers. A DSB is intended to guarantee completion of the memory access. If the targeted RAMs are the L2 tag, L2 victim, or L2 data RAM, a DSB might not provide this guarantee.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE executes a SYS #6, C15, C0, #0, <Xt> instruction, where Xt specifies the L2 tag, L2 data, or L2 victim RAMs.
2. PE executes a DSB.
3. PE reads the DDATAx registers.

Implications

If the above conditions are met, along with specific microarchitectural conditions, the DDATAx registers may not be updated when the DSB completes.

Workaround

When performing direct memory accesses to L2 cache memories do the following:

1. Set CPUACTLR2_EL1[46].
2. Perform the direct memory accesses.
3. Clear CPUACTLR2_EL1[46].

Note that setting CPUACTLR2_EL1[46] incurs a 1-2% performance penalty. Thus, CPUACTLR2_EL1[46] should not be set by default.

2033429
Corrupted register state results from executing specific form of SEL instruction followed by SVE AESMC or AESIMC instruction

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain conditions, execution of two SVE instructions, either SEL(vectors) followed by AESMC or SEL(vectors) followed by AESIMC, might result in corruption of a destination vector register.

Configurations affected

This erratum affects configurations with CRYPTO==TRUE.

Conditions

The following SVE instruction sequence is required:

1. PE executes SEL <Zd>.B, <Pg>, <Zn>.B, <Zm>.B
2. PE executes either AESMC <Zd>.B, <Zd>.B or AESIMC <Zd>.B, <Zd>.B

Implications

The sequence of instructions described in the conditions above are not expected to occur in real code, because they do not perform useful computation. As such, no impact is expected to real systems.

Workaround

Because the code sequences for this erratum are not expected to occur in real code, no workaround is required.

2048467
CPU might fetch incorrect instruction from a page programmed as non-cacheable in stage-1 translation and as device memory in stage-2 translation

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When an instruction fetch is initiated for a page programmed as non-cacheable normal memory in stage-1 translation and as device memory in stage-2 translation, the instruction memory might incorrectly return 0. This might cause an unexpected UNDEFINED exception.

Configurations Affected

The erratum affects configurations with COHERENT_ICACHE=0.

Conditions

This erratum occurs under the following conditions:

1. A CPU fetch instruction from a page satisfies the following:
    - Stage-1 translation of this page is programmed as non-cacheable normal memory.
    - Stage-2 translation of this page is programmed as device memory.

Implications

If the above conditions are met, the CPU might read 0 from the instruction memory. This instruction might cause an unexpected UNDEFINED exception. Instruction fetches to device memory are not architecturally predictable in any case, and device memory is expected to be marked as execute never, so this erratum is not expected to cause any problems to real-world software.

Workaround

This erratum has no workaround.

2052733
ER1PFGCTL.MV is improperly implemented as Read/Write

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

ER1PFGCTL.MV is improperly implemented as Read/Write. The Architecture requires it to be Read-As-One/Write-Ignore because all injected errors set ER1STATUS.MV=0x1.

Configurations affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The PE executes a write to ER1PFGCTL.
2. The PE executes a read from ER1PFGCTL.

Implications

Software cannot use ER1PFGCTL.MV to determine how to control the MV bit for an injected error. All injected errors will set ER1STATUS.MV=0x1.

Workaround

No workaround is expected to be required.

2067959
External aborts for streaming writes to MTE tagged pages may report multiple errors

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

If a streaming write to a memory page with Memory Tagging Extension (MTE) tagging enabled receives an External abort, it may report multiple SError aborts.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

1. The Processing Element (PE) generates a write of a full cache line to a memory page that is marked MTE Tagged.
2. A transaction issued on the CHI interconnect on behalf of the streaming write receives an External abort from the interconnect

Implications

If the above conditions are met, the PE might report multiple SError aborts. External aborts received from the interconnect represent error conditions in the system, such as accesses to unmapped devices and uncorrectable ECC errors. These conditions are more severe than the possibility of the PE reporting multiple SError aborts.

Workaround

There is no workaround.

2067960
Trace data lost during collection stop in TRBE

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When a collection stop event occurs in the Trace Buffer Extension (TRBE), trace collection from the Embedded Trace Extension (ETE) is stopped and the data in the TRBE buffers are flushed to memory. When this occurs under certain micro-architectural timing conditions, 64 bytes of trace data might get lost and replaced with Ignore bytes. This does not result in a current pointer mismatch.

Configurations affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. ETE and TRBE are enabled.
2. ETE is in a trace-allowed region.
3. A collection stop event occurs in TRBE.

Implications

When the above conditions are met, 64 bytes of trace data might get lost and replaced with Ignore bytes while getting written to memory.

Workaround

The erratum has no workaround.

2067962
L3D_CACHE_ALLOC PMU inaccurate when using WriteEvictOrEvict transactions

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When the L2 cache issues a WriteEvictOrEvict transaction for a L2 copyback, the L3D_CACHE_ALLOC PMU event is not counted, even though it might cause an L3 cache allocation.

Configurations Affected

This erratum affects all configurations that enable WriteEvictOrEvict transactions through CPUECLTR_EL1[45]=1.

Conditions

1. CPUECTLR_EL1[45] is set to 1 (default value).
2. PE is configured to count PMU event 0x29 L3D_CACHE_ALLOCATE.
3. L2 victimizes a cache line in the UC or SC state and generates a WriteEvictOrEvict transaction.

Implications

If the above conditions are met, the PE fails to inclement the PMU count.

Workaround

The DSU L3 cache PMU feature can be used to count L3 allocations across all PEs in the cluster.

2072986
An execution of MSR instruction might not update the destination register correctly when an external debugger initiates an APB write operation to update debug registers

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When an MSR instruction and an APB write operation are processed on the same cycle, the MSR instruction might not update the destination register correctly.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. A CPU executes an MSR instruction to update any of following SPR registers:
   a. DBGBCR<n>_EL1
   b. DBGBVR<n>_EL1
   c. DBGWCR<n>_EL1
   d. DBGWVR<n>_EL1
   e. OSECCR_EL1
2. An external debugger initiates an APB write operation for any of following registers:
   a. DBGBCR<n>
   b. DBGBVR<n>
   c. DBGBXVR<n>
   d. DBGWCR<n>
   e. DBGWVR<n>
   f. DBGWXVR<n>
   g. EDECCR
   h. EDITR
3. The SPR registers (for example, OSLSR_EL1.OSLK and EDSCR.TDA) and external pins are programmed to allow the following behavior:
   a. The execution of an **MSR** instruction in condition 1 to update its destination register without neither a system trap nor a debug halt
   b. The APB write operation in condition 2 to update its destination register without error
4. The **MSR** instruction execution in condition 1 and APB write operation in condition 2 happen in

same cycle.
5. The MSR write and the APB write are to two different registers. The architecture specifies that it is the software or debugger's responsibility to ensure writes to the same register are updated as expected.

Implications

If the above conditions are met, an execution of the MSR instruction might not update the destination register correctly. The destination register might contain one of following values after execution:

1. The execution of the MSR instruction is ignored. The destination register of the MSR instruction holds an old value.
2. The execution of the MSR instruction writes an incorrect value to its destination register.

A external debugger and system software are expected to be coordinated to prevent conflict in these registers.

Workaround

No workaround is required for this erratum.

2138952
External APB write to a register located at offset 0x084 might incorrectly issue a write to External Debug Instruction Transfer Register

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The core might incorrectly issue a write to External Debug Instruction Transfer Register (EDITR) when an external APB write to another register that is located at offset 0x084 is performed in the Debug state. The following debug components share the offset alias with the EDITR register:

- ETE - TRCVIIECTLR - ViewInst Include/Exclude Control Register
- Reserved locations

The following debug component shares the offset alias with the EDITR register when the PE is configured with 20-PMUs:

- PMU - PMEVCNTR16[63:32] - Event Counter 16

Configurations Affected

This erratum affects all configurations.

Conditions

1. The core is in debug state.
2. The External Debug Status and Control Register (EDSCR) cumulative error flag field is 0b0.
3. Memory access mode is disabled, in example, EDSCR.MA = 0b0.
4. The OS Lock is unlocked.
5. External APB write is performed to a memory mapped register at offset 0x084 other than the EDITR.

Implications

If the above conditions are met, then the core might issue a write to the EDITR and try to execute the instruction pointed to by the ITR. As a result of the execution, the following might happen:

- CPU state and/or memory might get corrupted.
- The CPU might generate an UNDEFINED exception.
- The EDSCR.ITE bit will be set to 0.

Workaround

Before programming any register at this offset when the PE is in Debug state, the debugger should either:

- Set the EDSCR.ERR bit by executing some Undefined instruction (e.g. writing zero to EDITR); or
- Set the OS Lock and then unlock it afterwards.

2138954
Incorrect Fault Status code reported for predicated SVE op

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

An SVE predicated store to a page with MTE tagging enabled that encounters a poisoned MTE Tag with no active elements and also has a tag check fail for a different MTE Tag might report a Synchronous External Abort instead of a Synchronous Tag Check Fault.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under the following conditions:

1. A PE executes an SVE predicated store to a page that is marked MTE Tagged.
2. The store accesses more than one Tag granule, such that there are no active elements corresponding to one of the granules accessed that also has a poisoned MTE tag.
3. The memory access results in a Tag check fail.

Implications

If the above conditions are met, the PE might report a Synchronous External Abort instead of Synchronous Tag Check Fault.

Workaround

This erratum has no workaround.

2138955
Tag check fail might not be reported for an unaligned predicated SVE store

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

An SVE predicated store to a page with MTE tagging enabled might not report a fault when it encounters a tag check fail.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted

Conditions

This erratum occurs under the following conditions:

1. A PE executes an SVE predicated store to a page that is marked MTE Tagged.
2. The store access crosses a cache line boundary.
3. Both cache line accesses encounter a tag check fault.
4. Before the fault is reported, the first cache line is snooped out and another PE modifies the tag.
5. The tag check passes for the first cache line access when the line is fetched again.

Implications

If the above conditions are met, the PE might not report a Synchronous Tag Check Fault. This erratum is reported as a Programmer Category C since most of the time, a tag check fault would be correctly detected.

Workaround

This erratum has no workaround.

2138959
OSECCR_EL1/EDECCR is incorrectly included in the Warm Reset domain

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

OSECCR_EL1/EDECCR is incorrectly included in the Warm Reset domain. If a Warm Reset occurs, then the value in this register will be lost.

Configurations Affected

This erratum affects all configurations.

Conditions

1. Warm Reset is asserted.

Implications

If the above conditions are met, then the value in OSECCR_EL1/EDECCR will be lost.

Workaround

A debugger should enable a Reset Catch debug event by setting CTIDEVCTL.RCE to 1. This causes the PE to generate a Reset Catch debug event on a Warm reset, allowing the debugger to reprogram the EDECCR.

2138960
Extra A-sync packet might get written to Trace Buffer in Trace prohibited region

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

An external trace analyzer can request that an A-sync packet is injected into the trace stream, which the Embedded Trace Extension (ETE) will insert when the next P0 Element is traced. Due to this erratum, this A-sync packet might incorrectly get generated and written to trace buffer memory via TRBE under the conditions mentioned below.

Configurations Affected

This erratum affects all configurations.

Conditions

The erratum occurs under the following conditions:

1. TRBE is enabled.
2. ETE is in trace prohibited region.
3. A **TSB** instruction is executed and completed.
4. TRBE is disabled.
5. A synchronization request is received on the ATB interface.
6. TRBE is enabled.

Implications

If the above conditions occur, an A-sync packet might go to TRBE and when a new **TSB** instruction is executed, this packet might get written to memory. Under normal usage Arm expects that this unexpected trace will have no impact.

Workaround

There is no workaround.

2139204
Speculative access to a recently unmapped physical address previously containing page tables might occur

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

If the memory containing page tables is unmapped or cacheable attribute is changed while there are pending hardware prefetches to that table, the read requests might illegally occur after a DSB instruction.

Configurations Affected

All configurations are affected.

Conditions

- A table walk occurs.
- The hardware prefetcher generates a cacheable request to adjacent cache lines, allocating the L2 cache.
- The physical address containing the page tables is unmapped or cacheable attribute is changed.

Implications

If the above conditions are met, an illegal read might occur in a short window of time after the DSB instruction. Arm does not believe this will cause incorrect execution in any practical system.

Workaround

No workaround is required.

2139205
L1D_CACHE_INVAL and L2D_CACHE_INVAL PMU events fail to increment for SnpPreferUnique and SnpPreferUniqueFwd

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When the PE receives a SnpPreferUnique or SnpPreferUniqueFwd snoop from the interconnect, it might not correctly count the L1 data cache and L2 cache invalidations that result.

Configurations Affected

This erratum affects all configurations.

Conditions

1. PE receives SnpPreferUnique or SnpPreferUniqueFwd from the coherent interconnect.
2. PE invalidates the L1 data cache and L2 cache.

Implications

If the above conditions are met, the L1D_CACHE_INVAL event will fail to increment and the L2D_CACHE_INVAL event might fail to increment. The relative infrequency of the necessary conditions means that the L1D_CACHE_INVAL and L2D_CACHE_INVAL events are still meaningful.

Workaround

There is no workaround.

2139206
MPAM value associated with instruction fetch might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open.

Description

Under some scenarios, the MPAM value associated with an instruction fetch request might be incorrect when context changes.

Configurations Affected

This erratum affects all configurations.

Conditions

1. An Instruction fetch request is attempted before a context switch but is not completed until after a context switch.

Implications

The MPAM value associated with the instruction fetch request might be incorrect.

Workaround

There is no workaround.

2139207
Data abort on SVE first fault load might be routed to incorrect Exception level

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain conditions, data abort on SVE first fault load might be routed to incorrect Exception level.

Configurations Affected

All configurations are affected.

Conditions

All of the following conditions must be met:

1. First active lane of SVE first fault load crosses a page boundary.
2. Translation table walk for the second page generates an external abort.
3. Memory tagging is enabled and access to bytes on the first page generates a tag check fail.
4. SCR_EL3.EA or HCR_EL2.TEA bits are set.

Implications

If the above conditions are met, data abort will not get routed to the correct Exception level. If this scenario occurred at EL0/EL1/EL2 and SCR_EL3.EA bit is set, data abort will not get routed to EL3. Likewise if this scenario occurred at EL0/EL1 and HCR_EL2.TEA bit is set and SCR_EL3.EA bit is not set, data abort will not get routed to EL2. The potential impact of this erratum to a practical system is considered to be very minor, given the precondition of an unrecoverable error.

Workaround

There is no workaround for this erratum.

2149120
A64 WFI or A64 WFE executed in Debug state suspends execution indefinitely

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Executing an A64 WFI or WFE instruction while in Debug state results in suspension of execution, and execution cannot be resumed by the normal WFI or WFE wake-up events while in Debug state.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The Processing Element (PE) is in Debug state and in AArch64 Execution state.
2. A WFI or WFE instruction is executed from EDITR.

Implications

If the above conditions are met, the PE will suspend execution.

This is not thought to be a serious erratum, because an attempt to execute a WFI or WFE instruction while in Debug state is not expected.

For WFI executed in Debug state, execution can only resume by any of the following:

- A Cold or Warm reset
- A Restart request trigger event from the Cross Trigger Interface (CTI) causing exit from Debug state, followed by a WFI wake-up event

For WFE executed in Debug state, execution can only resume by any of the following:

- A Cold or Warm reset
- A Restart request trigger event from the CTI causing exit from Debug state, followed by a WFE wake-up event
- An external event that sets the Event Register. Examples include executing an SEV instruction on another PE in the system or an event triggered by the Generic Timer.

Workaround

A workaround is unnecessary, because an attempt to execute a WFI or WFE instruction while in Debug state is not expected.

2153906
Collision bit in PMBSR is reported incorrectly when there are multiple errors on SPE writes

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Collision information captured by PMBSR_EL1.COLL might be lost under certain circumstances, when the buffer management interrupt is raised.

Configurations Affected

This erratum affects all configurations.

Conditions

1. A sampling collision event is detected.
2. Subsequent SPE write results in 2 SEI errors.

Implications

If the above conditions are met, the collision indicator in PMBSR_EL1 is incorrectly set to 0, following the 2nd SEI error. PMBSR_EL1 does capture and set the "Data Loss" (DL) indicator and all the other PMBSR_EL1 fields correctly.

Workaround

There is no workaround for this erratum.

2189737
PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 counts incorrectly and MEM_ACC_CHECKED 0x4024 might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The PMU Event MEM_ACCESS_CHECKED_WR, 0x4026 does not count correctly, and MEM_ACC_CHECKED 0x4024 might not count correctly.

Configurations Affected

This erratum affects all configurations.

Conditions

1. One of the PMU event counters is configured to count event 0x4026 or 0x4024.
2. MTE is enabled.
3. SCTLR_ELx.ATA=1.
4. A store instruction is executed that generates a memory-write access that is Tag Checked.

Implications

The counter values for these events will not be correct and therefore cannot be used reliably.

Workaround

There is no workaround.

2189738
Direct access of L2 data RAMs using RAMINDEX returns incomplete data

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A direct access to the L2 data RAM using the RAMINDEX function returns incomplete data in the DDATA2 register.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following condition:

1. Direct access to internal memory targeting L2 data RAM is executed.

Implications

A direct access to the L2 data RAM will result in zeros on DDATA2_EL3[19:16]. These bits should contain ECC[15:12] corresponding to Data[127:64], but instead contains zeros.

Workaround

There is no workaround.

2189739
PMU_HOVFS event not always exported when self-hosted trace is disabled

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

PMU_HOVFS is a PMU event that can be exported to the ETM.
This event should be exported if self-hosted trace is disabled, or, if self-hosted trace is enabled and TRFCR_EL2.E2TRE == 0b1.
This event is not exported if self-hosted trace is enabled and TRFCR_EL2.E2TRE == 0b0.
Due to this erratum, when self-hosted trace is disabled, the event is never exported if TRFCR_EL2.E2TRE == 0b0.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The ETM is configured to use PMU_HOVFS as an external input event.
2. Self-hosted trace is disabled and TRFCR_EL2.E2TRE == 0b0.

Implications

Overflows of PMU counters reserved by EL2 might not be visible.

Workaround

To use the PMU_HOVFS as an external input event when self-hosted trace is disabled, ensure TRFCR_EL2.E2TRE is set to 0b1.

2218242
Some SVE PMU events count incorrectly

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The following Performance Monitoring Unit (PMU) events do not count correctly:

- 0x8074, SVE_PRED_SPEC, SVE predicated Operations speculatively executed
- 0x8075, SVE_PRED_EMPTY_SPEC, SVE predicated operations with no active predicates, Operations speculatively executed
- 0x8076, SVE_PRED_FULL_SPEC, SVE predicated operations with all active predicates, Operations speculatively executed
- 0x8077, SVE_PRED_PARTIAL_SPEC, SVE predicated operations with partially active predicates, Operations speculatively executed

Configurations Affected

This erratum affects all configurations.

Conditions

One of the PMU event counters is configured to count any of the following events:

- 0x8074
- 0x8075
- 0x8076
- 0x8077

Implications

Load and store operations due to SVE instructions are not counted by any of these events. The counter values for these events will only reflect predicated SVE data processing operations. For example, this means that the ratios of each of the 0x8075-0x8077 event values to the 0x8074 event value will not be as expected because load and store operations are not included. However, the types of predicate used by data processing operations will still be usefully indicated.

Workaround

There is no workaround.

2218243
FAR_ELx contents for a Data Abort exception on SVE first fault contiguous load instruction due to Tag Check fail might be incorrect

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A SVE first fault contiguous load instruction that encounters both a Tag Check fail when accessing the first active element and a watchpoint match on one of the non-first active elements can generate a Data abort exception with an incorrect value in FAR_ELx.

Configurations Affected

All configurations are affected.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging and watchpoints are enabled.
2. A SVE first fault contiguous load instruction accesses memory and generates a Data Abort exception due to a Tag Check fail on the first active element.
3. There is a watchpoint match on one of the non-first active elements.

Implications

If the above conditions are met, a Data Abort exception will be generated with an incorrect value in FAR_ELx. ESR_ELx will indicate Synchronous Tag Check Fault. The FAR_ELx value could be anything between the start address of the access and up to twice the access size.

Workaround

This erratum has no workaround.

2240288
Incorrect sampling of SPE events "Partial predicate" and "Empty predicate" for SVE instruction with no vector operands

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain circumstances, the SPE events E[17] "Partial predicate" and E[18] "Empty predicate" might not be captured as required.

Configurations Affected

This erratum affects all configurations.

Conditions:

1. SPE samples an SVE instruction with no vector operands.

Implications

If the above conditions are met, then the SPE events E[17] "Partial predicate" and E[18] "Empty predicate" might not be captured for the given instruction.

Workaround

There is no workaround.

2242397
Streaming writes to memory mapped Non-shareable and write-back might cause data corruption because of reordering

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Writes to contiguous bytes might be combined into one streaming write of 64 bytes. If such writes are performed to memory mapped Non-shareable and write-back, then two streaming writes to the same physical address might be performed in the wrong order.

Configurations Affected

This erratum affects all configurations.

Conditions

Write stream operations to memory mapped Non-shareable and write-back, or shareable and write-back with the BROADCASTOUTER pin deasserted can allocate the L2 cache without issuing a request on the CHI interface. This creates the possibility of two concurrent pending WriteNoSnpFull transactions of the same cache line on CHI, without the proper sequencing to guarantee the order they are performed.

Implications

If the above conditions are met, then the combined writes might be performed in the wrong order as determined by the sequential execution model.

Workaround

This erratum can be avoided by mapping all write-back memory as Inner or Outer Shareable and asserting the BROADCASTOUTER pin.

2242404
64 bit source SVE PMULLB/T not considered Cryptography instruction

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

64 bit source element variants of SVE PMULLB and PMULLT are incorrectly classified as non-cryptography instructions. When the **CRYPTODISABLE** pin is asserted, 64 bit source SVE PMULLB or SVE PMULLT instructions are executed rather than taking the expected undefined instruction exception. In addition to this, when the CRYPTODISABLE pin is deasserted, PMU counts for CRYPTO_SPEC (PMU event 0x77) do not include 64 bit source SVE PMULLB and PMULLT in their counts.

Configurations Affected

This erratum affects all configurations.

Conditions

Cryptodisable

1. **CRYPTODISABLE** pin is high.
2. 64 bit source SVE PMULLB or SVE PMULLT is executed.

PMU Counts

1. **CRYPTODISABLE** pin is low.
2. PMU Enabled to count PMU EVENT 0x77 (CRYPTO_SPEC).
3. 64 bit source SVE PMULLB or SVE PMULLT is executed.

Implications

If the above conditions are met, then the instructions will be executed instead of taking the undefined exception that is required by Arm architecture.
In addition, the PMU counter for the CRYPTO_SPEC event (PMU EVENT 0x77) will not increment for 64 bit source SVE PMULLB PMULLT instructions.

Workaround

There is no workaround.

2242416
An SError might not be reported for an atomic store that encounters data poison

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain conditions, an atomic store that encounters data poison might not report an SError.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. An atomic store that is unaligned to its data size but within a 16-byte boundary accesses memory.
2. The atomic store accesses multiple L1 data banks such that not all banks have data poison.

Implications

If the above conditions are met, an SError might not be reported although poisoned data is consumed. Note that the data remains poisoned in the L1 and will be reported on the next access.

Workaround

This erratum has no workaround.

2253154
ESR_ELx contents for a Data Abort exception might be incorrect when an L1D tag double bit error is encountered

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When an L1D tag double bit error is encountered, a Data Abort exception might be reported with an incorrect fault type of Synchronous Tag Check Fault in the ESR_ELx register under unusual micro architectural conditions.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging is enabled.
2. A precise checked access due to a load instruction encounters L1D tag double bit error.

Implications

If the previous conditions are met, a Data Abort exception will be generated with an incorrect Data Fault Status Code (DFSC) of Synchronous Tag Check Fault in the ESR_ELx register when it should have been Synchronous External Abort.
If this scenario occurred at EL0/EL1/EL2 and SCR_EL3.EA bit is set, then Data Abort will not get routed to EL3.
Likewise if this scenario occurred at EL0/EL1 and HCR_EL2.TEA bit is set, then Data Abort will not get routed to EL2. A fatal RAS error will still be reported.

Workaround

This erratum has no workaround.

2276004
Incorrect Fault Status Code reported on a SPE buffer translation fault

Status

Fault Type: Programmer Category C.
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain circumstances, the 'Fault Status Code' in PMBSR_EL1 on a buffer translation fault might be incorrectly reported as an "Address size fault, level 0 of translation or translation table base register" (FSC = 6'b00_0000).

Configurations Affected

This erratum affects all configurations.

Conditions:

1. *Statistical Profiling Extension* (SPE) sampling and SPE buffer is enabled.
2. *Processing Element* (PE) is in Secure State.
3. SPE Owning exception level is Secure EL2.
4. *Memory Management Unit* (MMU) is enabled for EL2 or EL2&0 stage 1 address translation (SCTLR_EL2.M = 1).
5. Buffer translation encounters a translation fault.

Implications

If the above conditions are met, then the fault status code in PMBSR_EL1 is incorrectly reported as 6'b00_0000 (Address size fault, level 0 of translation or translation table base register) instead of 6'b00_01xx (Translation fault at level xx) on an SPE buffer translation fault.

Workaround

There is no workaround.

2280302
Read or write from Secure EL1 for ICV_BPR1_EL1 register might not work

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Valid access to ICV_BPR1_EL1 from Secure EL1 when ICV_CTLR_EL1.CBPR is set to 1 should modify ICV_BPR0_EL1 on writes and return the value from ICV_BPR0_EL1 on reads. Instead, reads of ICV_BPR1_EL1 return ICV_BPR0_EL1 plus one, saturated to 0b111. Writes to ICV_BPR1_EL1 are ignored.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The PE is in Secure state in the EL1 exception level.
2. ICV_CTLR_EL1.CBPR is set to 1.
3. A valid read or write access to ICV_BPR1_EL1 occurs.

Implications

If the above conditions are met, then an incorrect value might be returned on read or a valid write might be ignored potentially, affecting the priority of interrupts in the CPU.

Workaround

This erratum has no workaround.

2280397
PMU L1D_CACHE_REFILL_OUTER is inaccurate

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The L1D_CACHE_REFILL_OUTER PMU event 0x45 is inaccurate due to ignoring refills generated from a system cache. The L1D_CACHE_REFILL PMU event 0x3 should be the sum of PMU events L1D_CACHE_REFILL_INNER 0x44 and L1D_CACHE_REFILL_OUTER 0x45, however, due to the inaccuracy of L1D_CACHE_REFILL_OUTER 0x45 it is possible that this might not be the case.

Note: L1D_CACHE_REFILL PMU event 0x3 does accurately count all L1D cache refills, including refills from a system cache.

Configurations Affected

This erratum affects all configurations which implement a system cache.

Conditions

This erratum occurs under the following conditions:

1. The L2 outer cache is allocated with data transferred from a system cache.

Implications

When the previous condition is met the L1D_CACHE_REFILL_OUTER PMU event 0x45 does not increment properly.

Workaround

The correct value of L1D_CACHE_REFILL_OUTER PMU event 0x45 can be calculated by subtracting the value of L1D_CACHE_REFILL_INNER PMU event 0x44 from L1D_CACHE_REFILL PMU event 0x3.

2307062
Reads of DISR_EL1 incorrectly return 0s while in Debug State

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When the Processing Element (PE) is in Debug State, reads of DISR_EL1 from EL1 or EL2 with SCR_EL3.EA=0x1 will incorrectly return 0s.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The PE is executing in Debug State at EL1 or EL2, with SCR_EL3.EA=0x1.
2. The PE executes an MRS to DISR_EL1.

Implications

If the above conditions are met, then the read of DISR_EL1 will incorrectly return 0s.

Workaround

No workaround is expected to be required.

2307063
DRPS instruction is not treated as UNDEFINED at EL0 in Debug state

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

In Debug state, DRPS is not treated as an UNDEFINED instruction.

Configurations Affected

This erratum affects all configurations.

Conditions

1. The Processing Element (PE) is in Debug state.
2. PE is executing at EL0.
3. PE executes DRPS instruction.

Implications

If the above conditions are met, then the PE will incorrectly execute DRPS as NOP instead of treating it as an UNDEFINFED instruction.

Workaround

There is no workaround.

2307064
ELR_ELx[63:48] might hold incorrect value when PE disables address translation

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When the CPU executes an exception return in order to switch context and the new context satisfies certain rare conditions, the top 16 bits of ELR_ELx might track an incorrect value.

Configurations Affected

The erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. CPUACTLR_EL1[22] is set to 1.
2. The PE executes an ERET, ERETAA or ERETAB instruction to switch to a new context.
3. Either stage 1 or stage 2 translation was enabled when ERET is executed. After ERET, both stage 1 and stage 2 translations are turned off.
4. ELR_ELx[63:48] specified by ERET is neither 0x0000 (all zero) nor 0xffff (all one).

Implications

When the above conditions are met, the PE takes instruction abort (address size fault) or asynchronous exception after ERET without executing the instruction in the context specified by ERET. After the exception is taken, ELR_ELx specified by ERET should hold the same value because no instruction is executed. However, PE might modify ELR_ELx[63:48] to zero.

ERET with non-zero ELR_ELx[63:48] causes an address size fault during address translation disabled because the CPU supports less than 256TB physical address space. Arm also assumes the new context is controlled by privileged software (for example, Hypervisor) because translation is turned off. Therefore, software can hit this erratum only when the system software uses this malicious address in the ELR_ELx register.

Workaround

This erratum has no workaround.

2307065
TRBE might use incorrect Cacheability attributes for TRBE data when address translation is disabled

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

Under certain conditions, Trace Buffer Extension (TRBE) might use incorrect Cacheability attributes for TRBE data when address translation is disabled.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. TRBE is enabled with TRBLIMITR_EL1.nVM == 1.
2. TRBMAR_EL1.Attr is programmed to use Cacheable attributes.
3. MDCR_EL2.E2TB = 2'b00 (EL2 owning)
4. HCR_EL2.CD=1 and HCR_EL2.VM=1
5. PE is executing at EL=1 or EL=0.
6. TRBE writes data to memory.

Implications

When the above conditions are met, PE might incorrectly use Non-Cacheable attribute instead of Cacheable attribute from TRBMAR_EL1.Attr[3:0] for TRBE data. Trace data might be lost if the memory location used by TRBE is present in cache when this write happens.

Workaround

This erratum has no workaround.

2307066
L1 MTE Tag poison is not cleared

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The MTE Tag poison is not cleared by an STG or DC G[Z]VA instruction.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under the following conditions:

1. A Processing Element (PE) accesses a line that encounters poison on the MTE Tag.
2. The PE executes an STG or DC G[Z]VA to the same 16-byte address.

Implications

If the above conditions are met, then the MTE Tag poison does not get cleared in the L1 Tag.

Workaround

There is no workaround.

2341660
ESR_ELx contents for a Data Abort exception might be incorrect when a data double bit error or external abort is encountered

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When a data double bit error or external abort is encountered on one half of an unaligned load, a Data Abort exception might be reported with an incorrect fault type of Synchronous Tag Check Fault in the ESR_ELx register. This occurs under unusual micro-architectural conditions.

Configurations Affected

This erratum affects all configurations with the BROADCASTMTE pin asserted.

Conditions

This erratum occurs under all of the following conditions:

1. Memory tagging is enabled.
2. A precise checked access due to an unaligned load instruction encounters a data double bit error or external abort.

Implications

If the previous conditions are met, a Data Abort exception will be generated with an incorrect Data Fault Status Code (DFSC) of Synchronous Tag Check Fault in the ESR_ELx register, when it should have been Synchronous External Abort.

If this scenario occurred at EL0/EL1/EL2, and the SCR_EL3.EA bit is set, then the Data Abort will not get routed to EL3.

Likewise, if this scenario occurred at EL0/EL1, and the HCR_EL2.TEA bit is set, then the Data Abort will not get routed to EL2. A RAS error will still be reported.

Workaround

This erratum has no workaround.

2341661
ESR_ELx.ISV can be set incorrectly for an external abort on translation table walk

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When a data double bit error or external abort is encountered during a translation table walk, synchronous exception is reported with ISV bit set in the ESR_ELx register.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under all of the following conditions:

1. Data double bit error or external abort is encountered during translation table walk and synchronous exception is reported.

Implications

If the previous conditions are met, ESR_ELx.ISV bit will be set.

Workaround

This erratum has no workaround.

2341669
SPE, PMU event for full/partial/empty/not full predicate might be incorrect for some SVE instructions

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The SPE, PMU events for full/partial/empty/not full predicate capture the cases where an instruction reads a full, not full, partial, or empty value for governing predicate according to the size of the instruction. Under certain circumstances, the event might be incorrectly captured.

Configurations Affected

This erratum affects all configurations.

Conditions

- PMU is configured to sample events for SVE_PRED_EMPTY_SPEC (0x8075), SVE_PRED_FULL_SPEC (0x8076), SVE_PRED_NOT_FULL_SPEC (0x8079), or SVE_PRED_PARTIAL_SPEC (0x8077).
- One of these SVE conversion instructions is executed: SCVTF, UCVTF, FCTVZU, FCVTZS, FCVT, FCVTX, FCVTXNT, or FCVTNT.
- Governing predicate used by instruction has a different value than All-Active or All-Empty.

or

- SPE samples one of these SVE conversion instructions: SCVTF, UCVTF, FCTVZU, FCVTZS, FCVT, FCVTX, FCVTXNT, or FCVTNT.
- Governing predicate used by instruction has a different value than All-Active or All-Empty.

Implications

If the previous conditions are met, the following events might be incorrectly captured:

- SPE event E[17] "Partial predicate"
- SPE event E[18] "Empty predicate"
- PMU event SVE_PRED_EMPTY_SPEC (0x8075)
- PMU event SVE_PRED_FULL_SPEC (0x8076)
- PMU event SVE_PRED_NOT_FULL_SPEC (0x8079)
- PMU event SVE_PRED_PARTIAL_SPEC (0x8077)

Workaround

This erratum has no workaround.

2341671
Lower priority exception might be reported when abort condition is detected at both stages of translation

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

When a permission fault or unsupported atomic fault is detected in the second stage of translation during stage 1 translation table walk, and there is a higher priority alignment fault due to SCTLR_EL1.C bit not being set, then Data Abort might be generated reflecting the lower priority fault.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs when all the following conditions apply:

1. The core executes an atomic, load/store exclusive, or load-acquire/store-release instruction.
2. SCTLR_EL1.C bit is not set and access is not aligned to size of data element.
3. A permission fault or unsupported atomic fault is detected in the second stage of translation during stage 1 translation table walk.

Implications

If the previous conditions are met, a Data Abort exception will be generated and incorrectly routed to EL2 with Data Fault Status Code (DFSC) of permission fault or unsupported atomic fault, when it should have been routed to EL1 with DFSC of alignment fault.

Workaround

This erratum has no workaround.

2346744
CSSELR_EL1.TnD is RAZ/WI when CSSELR_EL1.InD == 0x1

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

In some contexts when CSSELR_EL1.InD == 0x1, CSSELR_EL1.TnD is defined to be RES0.
In other contexts when CSSELR_EL1.InD == 0x0, CSSELR_EL1.TnD is defined to be R/W.
When a bit is RES0 in some contexts and R/W in other contexts, then it cannot be implemented as RAZ/WI for RES0 contexts.
In affected products, CSSELR_EL1.TnD is incorrectly treated as RAZ/WI instead of the correct R/W behavior when CSSELR_EL1.InD == 0x1.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. The PE is executing with CSSELR_EL1.InD == 0x1.
2. The PE attempts to read or write CSSELR_EL1.TnD.

Implications

Reads of CSSELR_EL1.TnD will return 0x0 and writes will be ignored.

Workaround

This erratum is not expected to require a workaround.

2346745
L2 tag RAM double-bit ECC error might lead to the PE not responding to a forwarding snoop

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

A double-bit ECC error in a cache line containing Memory Tagging Extensions (MTE) tags might result in the L1 and L2 caches becoming out-of-sync with respect to MTE tag validity. This can lead to a situation in which the L1 evicts dirty MTE tags to the L2 as part of a fill/evict sequence or a snoop. If this eviction satisfies an external forwarding snoop, the RN-F might fail to provide legal responses which might lead to a deadlock.

Configurations Affected

This erratum affects all configurations using the Memory Tagging Extensions.

Conditions

When using MTE, under specific microarchitectural and timing conditions, an L2 double-bit ECC error in the L2 tag RAMs might allow the L1 data cache to later evict a cache line with dirty MTE tags.
The erratum occurs if the eviction satisfies an external snoop of one of these types:

- SnpUniqueFwd
- SnpCleanFwd
- SnpSharedFwd
- SnpNotSharedDirtyFwd
- SnpPreferUniqueFwd

Implications

If the previous conditions are met, the PE might provide an SnpRespDataFwded response to the HN-F, but fail to provide a CompData response to the original requester, leading to a system deadlock.

Workaround

This erratum has no workaround.

2393116
L1 Data poison is not cleared by a store

Status

Fault Type: Programmer Category C
Fault Status: Present in r0p0. Fixed in r0p1.

Description

The L1 Data poison is not cleared by a store under certain conditions.

Configurations Affected

This erratum affects all configurations.

Conditions

This erratum occurs under the following conditions:

1. A Processing Element (PE) executes a store that does not write a full word to a location that has data marked as poison.
2. The PE executes another store that writes to all bytes that contain data poison before the previous store is globally observable.

Implications

If the above conditions are met, then the poison bit in the L1 Data cache does not get cleared.

Workaround

This erratum can be avoided by inserting a DMB before and after a word-aligned store that is intended to clear the poison bit.