Embedded Trace Macrocell Architecture Specification Revision O Errata

Processor Division

Document number:	PRD08-PRDC-010560 1.0
Date of Issue:	2 April 2009
Author:	ARM

Abstract

This document describes errata and clarifications to the Embedded Trace Macrocell Architecture Specification, ETMv1.0 to ETMv3.4, ARM IHI 0014 rev O.

Contents

1 ABOUT THIS DOCUMENT

1.1 Change control

1.1.1 Change history

Version	Released	Changes
1.0	2 April 2009	First release

1.2 References

This document refers to the following documents.

Ref	Doc No	Author(s)	Title
1	ARM IHI 0014 rev O	ARM	ETM Architecture Specification, ETMv1.0 to ETMv3.4

1.3 Terms and abbreviations

This document uses the following terms and abbreviations.

Term	Meaning
ETM	Embedded Trace Macrocell

2 INTRODUCTION

This document describes errata and clarifications to the Embedded Trace Macrocell Architecture Specification, ETMv1.0 to ETMv3.4, ARM IHI 0014 rev O.

3 ARM IHI 0014O ERRATA

3.1 Section 3.9, Access Permissions for ETM registers (DE 459890)

The footnotes for Tables 3-88, 3-90, 3-92 and 3-94 are incorrect. Footnote b in each table which reads as:

> Entries in the table do not apply to Reserved and UNDEFINED locations in the memory map of the registers.

is incorrect and must be ignored.

3.2 Section 3.9.5, Access Permissions for coprocessor accesses (DE 459890)

The behavior of Reserved Trace registers is not fully specified.

When the Sticky state is set or the OS lock is set, the behavior of accesses to Reserved Trace Registers is UNPREDICTABLE.

3.3 Section 7.7.3, I-Sync Instruction Synchronization (DE 591520)

Figure 7-44 on page 7-70 has an incorrect value for the header byte of the Load/Store In Progress I-Sync packet. The value currently reads as 01110000 but must be 00001000.

3.4 Section 7.3.5, Branch packets (DE 591522)

Table 7-12 on page 7-30 is incomplete.

The entry for Exception[3:0] with the value b0101, “Jazelle exception”, should read as:

Exception[3:0]	Exception
b0101	Jazelle exception, see the address for the type, or ThumbEE exception

3.5 Section 3.5.13, About the sequencer registers (DE 592975)

The paragraph on page 3-62 which reads:

> Programing any of the Sequencer State Transition Event Registers when the Programming bit is set to 1 resets the sequencer to State 1.

is incorrect and must be ignored.

4 ARM IHI 0014O CLARIFICATIONS

4.1 Section 3.5.17, Synchronization Frequency register (DE 680819)

In *Finding the access type, ETMv3.4 and later* on page 3-71, the final numbered point 5 incorrectly refers to numbered point 3.

This final numbered point 5 should read as:

> 5. If the Synchronization Frequency Register is implemented as read/write, write the value from stage 2 back to the register.