

ARM® CoreLink™ DPE-400 Data Parity Extension for NIC-400

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Technical Reference Manual



ARM® CoreLink™ DPE-400 Data Parity Extension for NIC-400

Technical Reference Manual

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Release Information

Document History

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Product Status

The information in this document is Final, that is for a developed product.

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Preface

This preface introduces the *ARM® CoreLink™ DPE-400 Data Parity Extension for NIC-400 Technical Reference Manual*.

It contains the following:

- [About this book on page 6.](#)
- [Feedback on page 9.](#)

About this book

This book is for the ARM® CoreLink™ DPE-400, which is an add-on to the NIC-400 product, enabling transportation of read and write data payload parity information.

Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

rm Identifies the major revision of the product, for example, r1.

pn Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the DPE-400.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter introduces the DPE-400 and its features.

Chapter 2 DPE-400 Overview

This chapter describes the signals that are used in the data parity extension process.

Appendix A Revisions

This appendix describes the changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the [ARM Glossary](#) for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

monospace italic

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

monospace bold

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

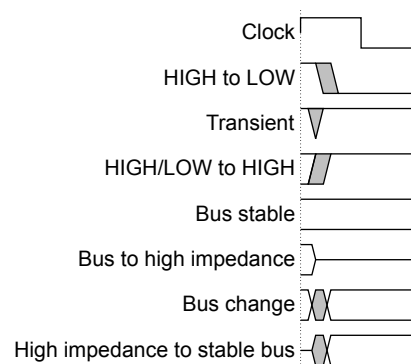


Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See *Infocenter* <http://infocenter.arm.com>, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DDI 0475).
- *ARM® CoreLink™ QoS-400 Network Interconnect Advanced Quality of Service Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0026).

Note

This product is separately licensed and not included in the NIC-400 base product.

- *ARM® CoreLink™ QVN-400 Network Interconnect Advanced Quality of Service using Virtual Networks, Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0027).

Note

This product is separately licensed and not included in the NIC-400 base product.

- *ARM® CoreLink™ TLX-400 Network Interconnect Thin Links, Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0028).

Note

This product is separately licensed and not included in the NIC-400 base product.

- *ARM® AMBA® Designer ADR-400 User Guide* (ARM DUI 0333).

The following confidential books are only available to licensees:

- *ARM® CoreLink™ DPE-400 Data Parity Extension for NIC-400 Configuration and Integration Manual* (ARM 100592).
- *ARM® CoreLink™ NIC-400 Network Interconnect Integration Manual* (ARM DII 0269).
- *ARM® CoreLink™ NIC-400 Network Interconnect Implementation Guide* (ARM DII 0273).
- *ARM® CoreLink™ NIC-400 Network Interconnect Supplement to ARM® CoreLink™ ADR-400 AMBA® Designer User Guide* (ARM DSU 0018).
- *ARM® CoreLink™ Creator User Guide* (ARM 100447).

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title *ARM® CoreLink™ DPE-400 Data Parity Extension for NIC-400 Technical Reference Manual*.
- The number ARM 100591_0100_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

————— **Note** —————

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Chapter 1

Introduction

This chapter introduces the DPE-400 and its features.

It contains the following sections:

- [1.1 About the DPE-400 on page 1-11.](#)
- [1.2 Key features on page 1-12.](#)
- [1.3 Product revisions on page 1-13.](#)

1.1 About the DPE-400

The ARM CoreLink DPE-400 Data Parity Extension for NIC-400 (DPE-400) is a licensable extension of Corelink NIC-400 Network Interconnect. DPE-400 provides transportation of read and write data payload parity information, using the AXI **WUSER** and **RUSER**, and AHB **HWUSER** and **HRUSER**, signals.

1.2 Key features

DPE-400 has a set of features, including transport of data parity information and support for data width management.

DPE-400 supports:

- Transport of parity information relating to read data and write data payloads.
- AMBA AHB-Lite, AXI3 and AXI4 protocols, and all intermediate protocol conversions.
- Data path width changes.
- Data widths that are wider than the current configuration, to enable easy integration into subsystems with larger data widths.

1.3 Product revisions

There can be differences in functionality between different product revisions. ARM records these differences in this section.

r0p3	First release.
r0p3-r1p0	No functional changes.

Chapter 2

DPE-400 Overview

This chapter describes the signals that are used in the data parity extension process.

It contains the following sections:

- [2.1 Overview on page 2-15.](#)
- [2.2 Limitations on page 2-16.](#)

2.1 Overview

DPE-400 enables transportation of bit-per-byte odd parity information plus one parity validity bit for AXI **WDATA** and **RDATA** (or AHB-Lite **HWDATA** and **HRDATA**) payload.

This information is transported on the **WUSER** and **RUSER** (or AHB-Lite **HWUSER** and **HRUSER**) bits. The **USER** signals can be used exclusively for parity information or they can also contain extra user-defined information.

In either case, the parity information resides in the lowest part of the **USER** signal vector. **USER[0]** describes the parity validity and **USER[(data_width div 8):1]** contains the bit per byte parity information.

Note

data_width is a parameter which can be set to 32-bit, 64-bit, 128-bit, or 256-bit.

The **data_width** must be large enough to accommodate the parity vector for the widest data width in the system. The **USER** bit reserved for parity information is a consistent width across all interfaces, regardless of the interface data width.

When an interface is the maximum system data width, all the parity bits are used to describe the parity of the data payload irrespective of transfer width.

When an interface is less than the system data width, the lowest indexed bits of the vector are used to describe the parity information of the interface. This is irrespective of transfer width, and the upper bits that are reserved for describing parity information, are ignored on input and driven to '0' on output.

When data width conversion is not present, the parity information and **WDATA** payload are not impacted by **WSTRB**.

When data width conversion occurs, **WDATA** is optimized depending on the value of **WSTRB**. In this case, data parity is modified to reflect the new **WDATA** value. A byte of **WDATA** is driven to 0x00 when the byte-lane's **WSTRB** is 1'b0. Therefore, the relevant bit is driven to 1'b1.

2.2 Limitations

DPE-400 cannot be configured with a QVN-400 configuration.

Appendix A

Revisions

This appendix describes the changes between released issues of this book.

It contains the following sections:

- [A.1 Revisions on page Appx-A-18.](#)

A.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue 0003-00

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue 0003-00 and issue 0100-00

Change	Location	Affects
No technical changes	-	All revisions