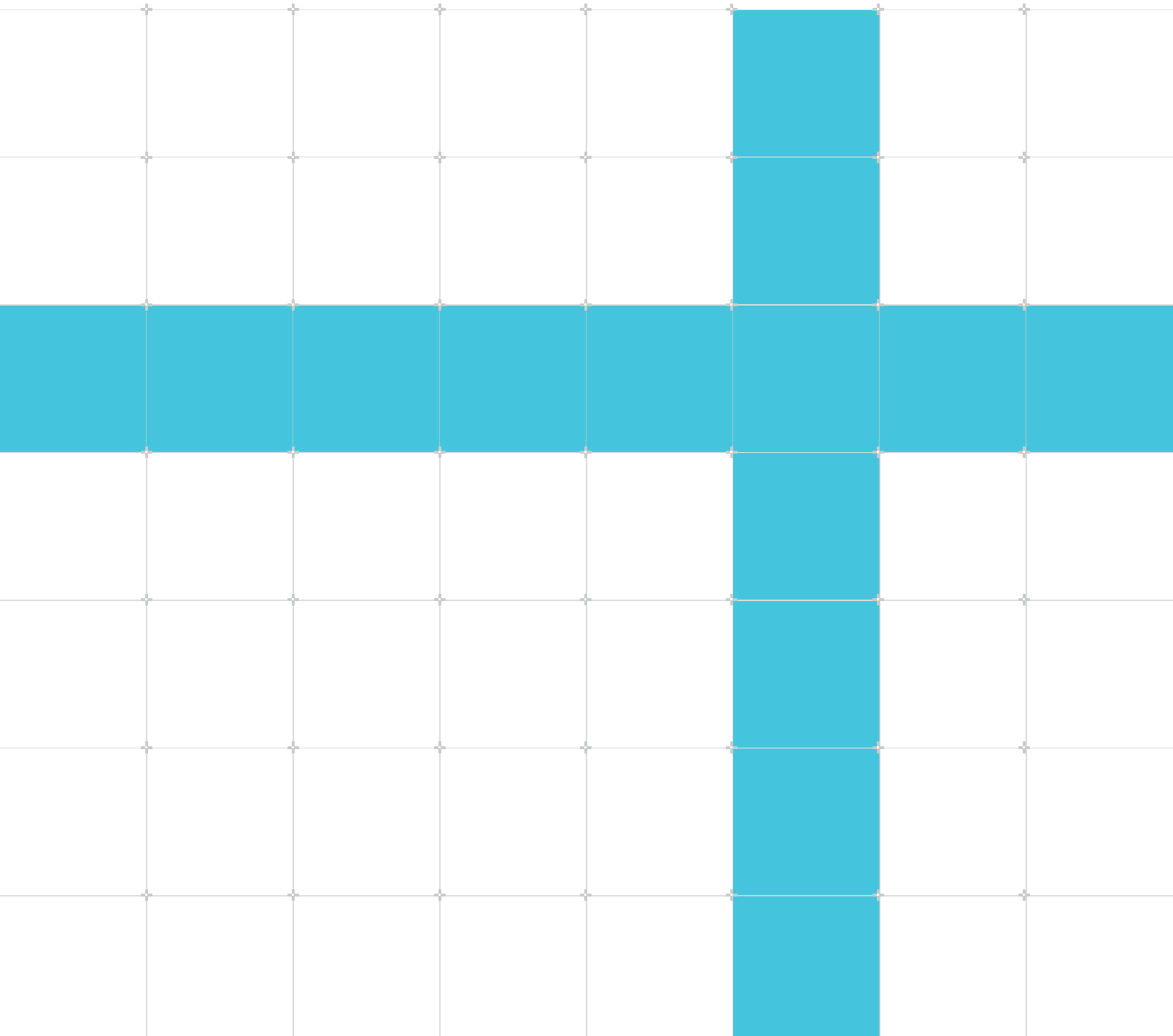
Release notes for the AArch32 Instruction Set Architecture for Arm A-profile Architecture

2023-09

Non-Confidential

Issue 01
109387_2023-09_01_en



Release notes for the AArch32 Instruction Set Architecture for Arm A-profile Architecture

Release information

Document history

Issue	Date	Confidentiality	Change
2023_09-01	29 September 2023	Non-Confidential	2023-09 release

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(LES-PRE-20349|version 21.0)

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29 September 2023

Product Status

The information in this release covers multiple versions of the architecture. The content relating to different versions is given different quality ratings.

The information relating to the 2023 Extensions of the A-profile Architecture and FEAT_D128 of the 2022 Extensions is at Alpha quality. Alpha quality means that most major features of the specification are described in this release, but some features and details might be missing.

The information relating to the remainder of the 2022 Extensions of the A-profile Architecture and the rest of the Architecture is at Beta quality. Beta quality means that all major features of the specification are described, but some details might be missing.

Change history

The following changes apply to this release:

- The title of the TSB CSYNC instruction page is changed.
- To improve clarity in the operational pseudocode of Advanced SIMD and floating-point instructions:
  - References to the FPSCR[] accessor are replaced by a call to the EffectiveFPCR() function.
  - Calls to the StandardFPSCRValue() function are replaced by a call to StandardFPCR().

Many simple clarifications and corrections are present, but are too small to be listed here. Some minor formatting changes are suppressed and not highlighted in the diff output.

Known issues

All issues identified in the below list will be fixed in a future release.

- There is a mismatch between the encoding for VMOVL and some other instructions and the conditions defined for the groups they appear in. The encoding is correct. The group conditions for affected instructions will be clarified.
- The setting of FPEXC.DEX and FPEXC.TFV bits for an invalid FPSCR.Len and FPSCR.Stride, for an allocated CP10 or CP11 instruction is missing from pseudocode.
- Some architectural features have limited or no descriptions in pseudocode and are not fully covered by the functional testing. Affected features are listed below:
  - Address translation, Instruction Cache, Data Cache System instructions.
  - Ordering of memory accesses.
  - Self-hosted trace and external trace.

- RAS architecture.
- Activity Monitors Extension.
- Generic Interrupt Controller.
- Multi-processing.