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ARM CoreSight ™
DK-A9 (TM096)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r2p0 of CoreSight Design Kit for Cortex-A9

Errata for the following components are listed separate errata documents:

TM917 : AHB Trace Macrocell

TM950 : CoreSight PTM-A9

TM093 : CoreSight Generic Parts

Proprietary notice

Document confidentiality status

This document is Non Confidential.

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Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Component Revisions

This document reports the errata for all revisions of CoreSight Design Kit for Cortex-A9 (DK-A9). Each release of DK-A9 contains several CoreSight sub-components, the revisions of each sub-component for each specific DK-A9 release are documented in Table 1 below. The errata for these sub-components are listed in separate errata documents.

Component	CoreSight Design Kit for Cortex-A9 Revision r0p0
CoreSight Generic Parts	r1p2
AHB Trace Macrocell	r0p4
CoreSight PTM-A9	r1p0

Table 1 CoreSight Design Kit for Cortex-A9 component revisions.

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

25 Sep 2009: Changes in Document v3

Page	Status	ID	Cat	Summary
10	New	712519	Cat 3	CORTEXA9INTEGRATION.v reset logic means debug connection is lost when after power-up of single CPU

15 Dec 2008: Changes in Document v2

No changes in this document revision

23 Apr 2008: Changes in Document v1

Initial Document Revision

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r1p0	r2p0
712519	Cat 3	CORTEXA9INTEGRATION.v reset logic means debug connection is lost when after power-up of single CPU	X	

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

There are no Errata in this Category

Errata - Category 3

712519: CORTEXA9INTEGRATION.v reset logic means debug connection is lost when after power-up of single CPU

Status

Affects: product CoreSight Design Kit for Cortex-A9.

Fault status: Cat 3, Present in: r1p0, Fixed in r2p0.

Description

The integration level includes an asynchronous APB bridge to allow access to all of the debug components within the system. The integration level also provides a separate debug reset for each cpu. In r0p0 and r1p0 of the Coresight design kit for PTM-A9, performing a debug reset of any core will also reset the APB bridge.

Conditions

1. One of the CPUs is held in debug reset
2. Debug APB accesses are performed to another CPU or PTM

Implications

It is not possible to perform debug of one core if the other cores in the cluster are allowed to dynamically power down.

The implications of this erratum will depend on the system level connection of debug resets. Typically, during debug, all CPUs will remain powered up and debug reset will not be asserted. In a system where individual CPUs are reset independently, the debug APB bridge can be disabled, and this will prevent debug accesses.

Workaround

To work around this erratum, tools can set DBGNOPWRDWN for all of the cores in the system.

Errata - Documentation

There are no Errata in this Category