

Core Tile for ARM1176JZF-S™

HBI-0154

User Guide



Core Tile for ARM1176JZF-S

User Guide

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Release Information

The following changes have been made to this book.

Change History			
Date	Issue	Confidentiality	Change
April 2007	A	Non-Confidential	First release
October 2007	B	Non-Confidential	Second release updated to fix documentation defects
May 2008	C	Non-Confidential	Third release updated to fix documentation defects.

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Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity



The system should be powered down when not in use.

The Core Tile generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- ensure attached cables do not lie across the card
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

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Preface

This preface introduces the RealView Core Tile for ARM1176JZF-S and its reference documentation. It contains the following sections:

- *About this book* on page xii
- *Feedback* on page xvii.

About this book

This book describes how to set up and use the Core Tile for ARM1176JZF-S (CT1176JZF-S).

Intended audience

This book has been written for experienced hardware and software developers to aid the development of ARM-based products using the CT1176JZF-S as part of a development system.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

This chapter introduces Core Tiles and the CT1176JZF-S.

Chapter 2 *Getting Started*

This chapter describes how to set up and prepare the CT1176JZF-S for use.

Chapter 3 *CT1176JZF-S Hardware Description*

This chapter describes the on-board hardware of the CT1176JZF-S.

Chapter 4 *Test Chip Hardware Description*

This chapter describes the features of the ARM1176JZF-S test chip which affect the CT1176JZF-S.

Chapter 5 *CT1176JZF-S Signal Descriptions*

This chapter provides a summary of signals present on the CT1176JZF-S connectors, test points, LED indicators, and the links that can be modified to change signal routing.

Appendix A *Specifications*

This appendix contains the electrical, timing, and mechanical specifications for the CT1176JZF-S.

Typographical conventions

The following typographical conventions are used in this document:

bold	Highlights ARM signal names within text, and interface elements such as menu names. This style is also used for emphasis in descriptive lists where appropriate.
<i>italic</i>	Highlights special terminology, cross-references and citations.
<code>monospace</code>	Denotes text that can be entered at the keyboard, such as commands, file names and program names, and source code.
<u>monospace</u>	Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.
<i>monospace italic</i>	Denotes arguments to commands or functions where the argument is to be replaced by a specific value.
monospace bold	Denotes language keywords when used outside example code.

Other conventions

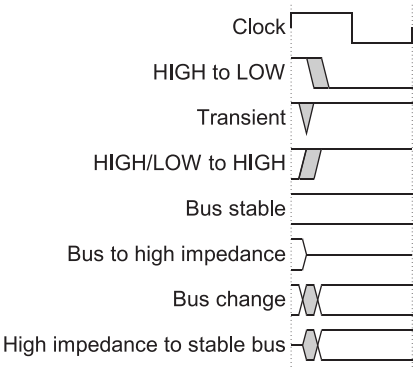
This document uses other conventions. They are described in the following sections:

- *Timing diagrams*
- *Signals* on page xiv
- *Bytes, Halfwords, and Words* on page xv
- *Bits, bytes, K, and M* on page xv
- *Register fields* on page xv.
- *Numbering* on page xvi.

Timing diagrams

The figure named *Key to timing diagram conventions* on page xiv explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Signals

When a signal is described as being asserted, the level depends on whether the signal is active HIGH or active LOW. Asserted means HIGH for active high signals and LOW for active low signals:

- Prefix n** Active LOW signals are prefixed by a lowercase n except in the case of AXI, AHB or APB reset signals. These are named **ARESETn**, **HRESETn** and **PRESETn** respectively.
- Prefix A** Denotes global *Advanced eXtensible Interface* (AXI) signals:
- Prefix AR** Denotes AXI read address channel signals.
- Prefix AW** Denotes AXI write address channel signals.
- Prefix B** Denotes AXI write response channel signals.
- Prefix C** Denotes AXI low-power interface signals.
- Prefix H** AHB signals are prefixed by an upper case H.
- Prefix P** APB signals are prefixed by an upper case P.
- Prefix R** Denotes AXI read data channel signals.
- Prefix W** Denotes AXI write data channel signals.

Bytes, Halfwords, and Words

Byte	Eight bits.
Halfword	Two bytes (16 bits).
Word	Four bytes (32 bits).
Quadword	16 contiguous bytes (128 bits).

Bits, bytes, K, and M

Suffix b	Indicates bits.
Suffix B	Indicates bytes.
Suffix K	When used to indicate an amount of memory means 1024. When used to indicate a frequency means 1000.
Suffix M	When used to indicate an amount of memory means $1024^2 = 1\,048\,576$. When used to indicate a frequency means 1 000 000.

Register fields

All reserved or unused address locations must not be accessed as this can result in unpredictable behavior of the device.

All reserved or unused bits of registers must be written as zero, and ignored on read unless otherwise stated in the relevant text.

All registers bits are reset to logic 0 by a system reset unless otherwise stated in the relevant text.

Unless otherwise stated in the relevant text, all registers support read and write accesses. A write updates the contents of the register and a read returns the contents of the register.

All registers defined in this document can only be accessed using word reads and word writes, unless otherwise stated in the relevant text.

Numbering

The document numbering convention is:

<base><number>

For example:

- 0x7B4 is a hexadecimal value of 7B4
- 9 is a decimal value of 9
- b00001111 is an eight-bit binary value of 00001111.

Further reading

The following publications by ARM Limited provide additional information on using the Core Tile and related products:

- *RealView® Emulation Baseboard User Guide* (ARM DUI 0303)
- *LT-XC2V4000+ User Guide* (ARM DUI 0186)
- *LT-XC4VLX100+ User Guide* (ARM DUI 0345)
- *ARM RealView ATI Analyzer Tile User Guide* (ARM DUI 0189)
- *AMBA® Specification* (ARM IHI 0011)
- *AMBA 3 AXI Protocol Specification* (ARM IHI 0022)
- *ARM Architecture Reference Manual* (ARM DDI 0100)
- *RealView Debugger User Guide* (ARM DUI 0153)
- *RealView Compilers and Libraries Guide* (ARM DUI 0205)
- *RealView Linker and Utilities Guide* (ARM DUI 0206)
- *RealView ICE User Guide* (ARM DUI 0155).

Feedback

ARM Limited welcomes feedback both on the ARM Core Tiles and on the documentation.

Feedback on this document

If you have any comments about this document, send email to errata@arm.com giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- an explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the ARM Core Tiles

If you have any comments or suggestions about these products, contact your supplier giving:

- the product name
- an explanation of your comments.

Chapter 1

Introduction

This chapter introduces Core Tiles. It contains the following sections:

- *About Core Tiles* on page 1-2
- *Overview of CT1176JZF-S* on page 1-3
- *Precautions* on page 1-11.

Note

This guide covers the HBI-0154 (CT1176JZF-S) printed-circuit board.

This board supports the ARM1176JZF-S test chip. The availability of Core Tiles however, depends on the availability of individual test chips. Contact your sales representatives for details on currently available Core Tiles.

1.1 About Core Tiles

Core Tiles are development boards that enable you to develop products based on ARM® processors and AMBA® interfaces. Core Tiles are built around test chips, which are ASIC implementations of one or more ARM processors. Core Tiles provide one or more AMBA interfaces from the processor so that it can be connected to an AMBA-based system. See the *AMBA Specification* (ARM IHI 0011) and the *AMBA 3 AXI Protocol Specification* (ARM IHI 0022) for further information.

The Core Tile must be used in conjunction with a specific baseboard that implements the necessary system and memory controllers. For example, the CT1176JZF-S when combined with the RealView® Emulation Baseboard (EB) will provide a standalone system for product development. Third-party or custom baseboards may also be used with a Core Tile.

———— **Note** —————

If a third-party or custom baseboard is used, ARM will only be able to provide limited support.

—————

Core Tiles do not have power or JTAG connectors. The tiles must be stacked on a baseboard that provides power and JTAG connections. The Core Tiles also require a reference clock (or clocks) to be supplied by the attached baseboard.

Through-board connectors on tile products allow stacking of multiple tiles. Multiple combinations of Core Tile and Logic Tile can be used to create a multiprocessor system.

———— **Note** —————

Although ARM does not offer an example at present, using the EB you can build a dual processor system using a Core Tile at each tile site without the need for Logic Tiles.

—————

For debug, a Realview Analyzer Tile should be used to provide access to signals on the tile header connectors.

See *ARM RealView AT1 Analyzer Tile User Guide* (ARM DUI 0189) for details.

1.2 Overview of CT1176JZF-S

The major components on the CT1176JZF-S are as follows:

- ARM1176JZF-S test chip
- tile headers on the top and bottom of the board
- bus interface logic
- clock selection and initialization logic
- controllable power supply for the test chip core and PLL
- test chip power monitoring logic
- configuration and control PLD
- AXI bus multiplexing logic.

Figure 1-1 shows the layout of a CT1176JZF-S.

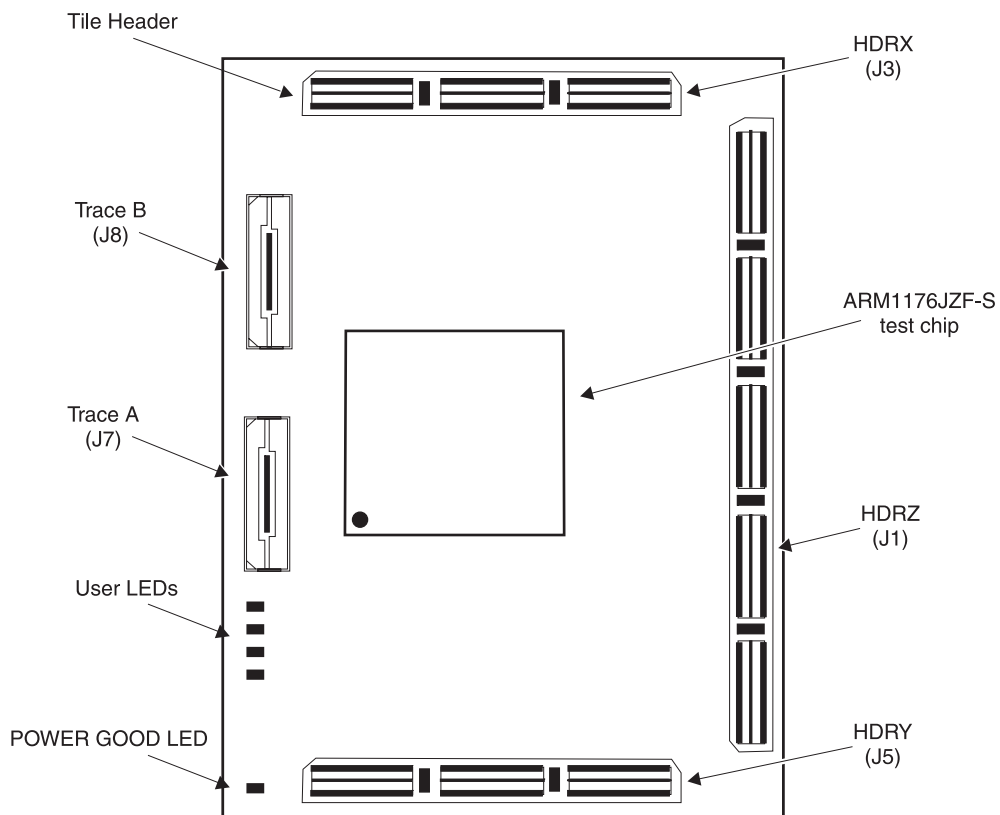


Figure 1-1 CT1176JZF-S layout

Figure 1-2 shows a CT1176JZF-S together with an EB. When using the EB, typically tile site 2 is occupied by a Logic Tile which can be used for custom peripheral development or to hold a synthesized core.

Refer to the *LT-XC2V4000+ Logic Tile User Guide* (ARM DUI 0186) and the *LT-XC4VLX100+ Logic Tile User Guide* (ARM DUI 0345) for details on the Logic Tiles which can be used for system prototyping.

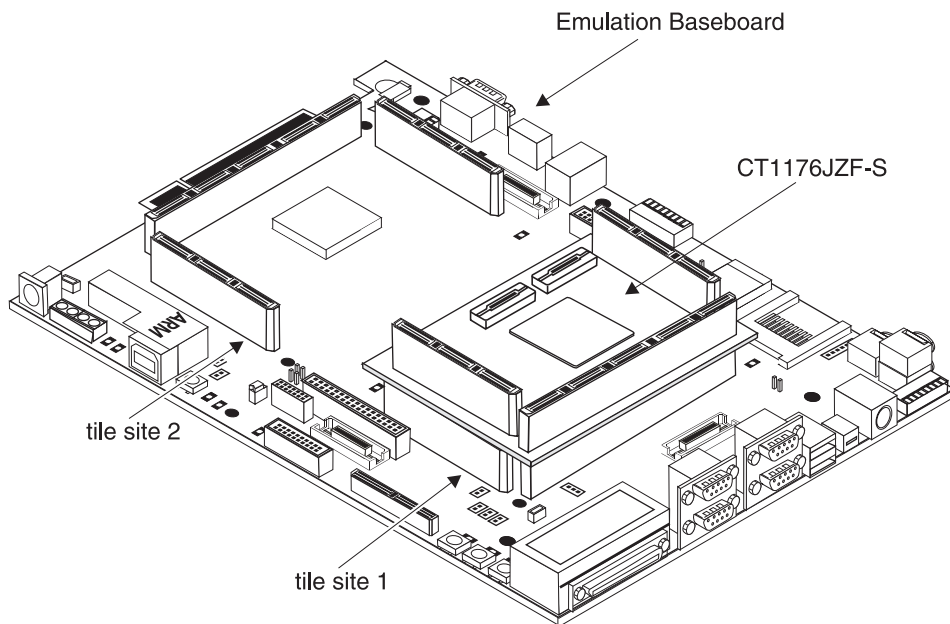


Figure 1-2 CT1176JZF-S and Emulation Baseboard

1.2.1 System architecture

Figure 1-3 on page 1-6 shows the architecture of a typical hardware development system consisting of a CT1176JZF-S and an EB. For details of the peripheral devices implemented on the EB and the available interfaces see *RealView Emulation Baseboard User Guide* (ARM DUI 0303).

1.2.2 External logic

The EB provides:

- power and JTAG connectors
- a reference clock
- a serial interface to the CT1176JZF-S PLD that loads the desired configuration
- initialization values to the PLD for the PLL and clock divider in the test chip
- peripheral devices (for example, memory controller, interrupt controller, system and reset controller, serial I/O). See *RealView Emulation Baseboard User Guide* (ARM DUI 0303) for details.

The external connectors and control logic are also provided by the EB. The FPGA on the EB provides system control functions for the CT1176JZF-S. See Chapter 3 *CT1176JZF-S Hardware Description*, and the documentation for your EB for more details.

————— Note —————

The FPGA on the external baseboard must be loaded with an appropriate image. An application note, giving information on the FPGA images for the combination of products that you are using may be available. Please refer to the documentation provided on the product CD and the ARM website (http://www.arm.com/documentation/Application_Notes/index.html)

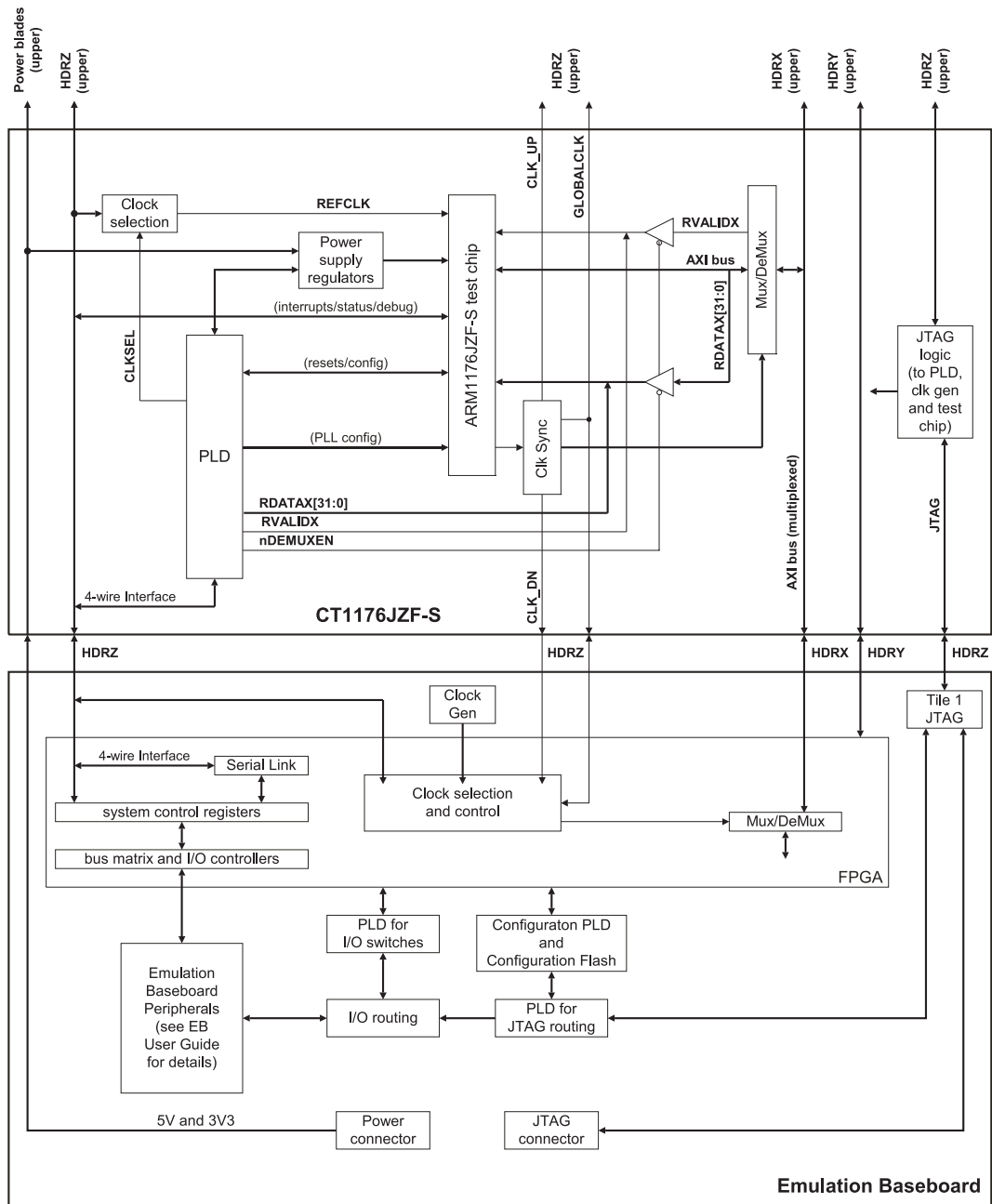


Figure 1-3 System block diagram

1.2.3 ARM processor test chip

The name of the Core Tile reflects the test chip fitted. The CT1176JZF-S has an ARM1176JZF-S test chip that includes an ARM1176JZF-S processor with *TrustZone*® security extensions, and a subsystem based on PrimeCell® components that is built around an AXI, AHB and APB infrastructure.

Note

For more details on the processor, see the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301).

Core configuration

The core configuration signals are driven by the PLD or the FPGA on the baseboard, or set by resistor links on the Core Tile. In a production ASIC, these core configuration signals are permanently tied HIGH or LOW. However, in order to experiment with different processor configurations, you can change the Core Tile PLD register values via a 4-wire serial link by writing values to the system registers in the baseboard. See *Overview of Core Tile configuration* on page 3-25 for details.

TrustZone security extensions

Caution

TrustZone security extensions enable a Secure software environment. The technology does not protect against all forms of hardware attack, and the implementer must take steps to achieve a suitable level of hardware security. The appropriate level of hardware protection depends on the sensitivity (value) of the code and data, so there are various possible compromises between cost and security.

The ARM1176JZF-S processor supports TrustZone security extensions to provide a secure environment for software. For details of the ARM1176JZF-S processor elements that TrustZone uses see the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301).

The TrustZone approach to integrated system security depends on an established trusted code base. The trusted code is a relatively small block that runs in the Secure world in the processor and provides the foundation for security throughout the system. This security applies from system boot and enforces a level of trust at each stage of a transaction.

The processor has seven operating modes, that can be either Secure or Non-Secure, and the Secure Monitor mode that is always Secure. The NS bit, in system control coprocessor CP15, determines if the processor runs code in the Secure or Non-Secure worlds, except for Secure Monitor mode that is always Secure.

Note

ARM do not provide TrustZone software or the hardware platform with this product, only the ARM1176JZF-S TrustZone registers and interface signals required by the user to implement TrustZone support are provided. See *TrustZone security control* on page 4-9 for details of the test chip TrustZone peripheral control registers.

1.2.4 PLD

The PLD on the Core Tile receives configuration signals from the serial link, controlled by the baseboard.

The CT1176JZF-S PLD outputs signals that control:

- the DACs that control the power supplies for the test chip
- the clock control registers that control the reference clock source to the core
- the multiplexed AXI bus interface
- the test chip resets and configuration signals.

The PLD transmits status signals to the serial link:

- Stable clocks indicators (PLLLOCK, PLLLOCKX, ISPnLOCK)
- the value of the test chip voltages
- the current drawn from the test chip core and PLL
- a PLD identifier (PLDVER) that can be used to identify the version of the PLD image
- a Core Tile build identifier (BUILDDID) that can be used to identify the CT1176JZF-S build variant.

Note

Different Core Tiles might also transmit signals that are specific to that tile. For example, the CT1176JZF-S transmits an ARM1176JZF-S test chip PLL locked signal, **PLLLOCKX**.

User control of the signals present in the serial interface is possible through the system control registers on the baseboard.

1.2.5 Processor bus

The test chip on the CT1176JZF-S has a single AXI bus interface. See *Bus interface characteristics* on page A-2 for parametric data.

1.2.6 Memory

The ARM1176JZF-S test chip has on chip memory. See *Memory configuration* on page 3-40 for details of the ARM1176JZF-S test chip memory system. If additional system memory is required, add PISMO Expansion Memory Modules to a baseboard that supports the PISMO standard. See the *Realview Emulation Baseboard User Guide* (ARM DUI 0303) for details.

1.2.7 Clock generation

The primary reference clock for the CT1176JZF-S is provided by the attached baseboard or a Logic Tile fitted above the CT1176JZF-S. See *Clocks* on page 3-5 for details of the CT1176JZF-S clocking system.

1.2.8 JTAG

The CT1176JZF-S does not have a JTAG connector. You must use the JTAG connector on the baseboard. See *JTAG support* on page 3-44 for details of the CT1176JZF-S JTAG interface.

1.2.9 Power supply control

Interface logic on the CT1176JZF-S enables you to control and read the test chip core and PLL supply voltages. The current drawn by the test chip core and PLL can also be read to monitor power. The voltage control range available is set during board manufacture.

The CT1176JZF-S uses 3V3 and 5V supplies connected through power-blades in the header connectors. See *Header connectors* on page 5-2 for details.

The 3V3 supply is used to directly power CT1176JZF-S components and to locally generate **ARM_VDDIO**, an optional 1V8 or 2V5 supply.

The 5V supply is used locally to generate three supplies:

- **VDDCORE1** (1V2)
- **VDDCORE2** (1V0)
- **VDDPLD** (1V8)

See *Power supply control* on page 3-16 for details on the voltage control logic.

1.2.10 Indicators

The CT1176JZF-S has a Power Good LED indicator for the VDDCORE 1V0 power supply and four User LEDs. See *LED indicators* on page 5-31 for details. For details on indicators present on the Logic Tiles, Interface Modules, and baseboard products, see the documentation supplied with the product.

1.3 Precautions

This section contains safety information and advice on how to avoid damage to the Core Tile.

1.3.1 Ensuring safety

The CT1176JZF-S is powered from 3V3 and 5V supplies provided by the baseboard.

———— **Warning** ————

To avoid a safety hazard, only *Safety Extra Low Voltage* (SELV) equipment must be connected to the Core Tile.

The test chip on the Core Tile can become very hot during continuous I/O activity. Take extra care when probing the test chip.

—————

1.3.2 Preventing damage

The Core Tile is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure and this leaves the board sensitive to electrostatic discharges and allows electromagnetic emissions.

———— **Caution** ————

To avoid damage to the Core Tile you must observe the following precautions:

- never subject the tile to high electrostatic potentials
- always wear a grounding strap when handling the tile
- only hold the tile by the edges
- avoid touching the component pins or any other metallic element.

Do not use the board near equipment that could be:

- sensitive to electromagnetic emissions (such as medical equipment)
 - a transmitter of electromagnetic emissions.
-

Chapter 2

Getting Started

This chapter describes how to set up and prepare the CT1176JZF-S for use. It contains the following sections:

- *Using the CT1176JZF-S with an Emulation Baseboard* on page 2-2
- *Connecting power* on page 2-4
- *Connecting JTAG debugging equipment* on page 2-6
- *Connecting Trace* on page 2-9
- *Using the CT1176JZF-S with a custom baseboard* on page 2-11

Note

The information in this chapter provides only a general overview. Details on using a Core Tile with different ARM products are covered in application notes. Ensure that you use the correct application note and FPGA image for your configuration.

The CT1176JZF-S must be used with a baseboard that provides configuration control and additional peripherals. This requirement is fully met by the EB. The FPGA on the baseboard must contain an image that is explicitly designed to interface with the CT1176JZF-S.

2.1 Using the CT1176JZF-S with an Emulation Baseboard

A typical processor development system is shown in Figure 2-1 on page 2-3.

To set up a development system using the CT1176JZF-S with an Emulation Baseboard (EB) refer to Application Note 177 (ARM DAI 0177) supplied on the Versatile Family CD.

Note

You may optionally place a RealView AT1 Analyzer Tile between the baseboard and the CT1176JZF-S to enable monitoring of signals using a logic analyzer.

To set up a development system using the CT1176JZF-S with an EB, that also includes a Logic Tile, refer to Application Note 151 (ARM DAI 0158) supplied on the Versatile Family CD.

Note

The Logic Tile can contain both additional master and slave peripherals. You may optionally place an IT1 Interface Tile above the Logic Tile to provide access to these additional peripherals.

Caution

Ensure that the correct FPGA image is used. An incorrect image can damage the boards.

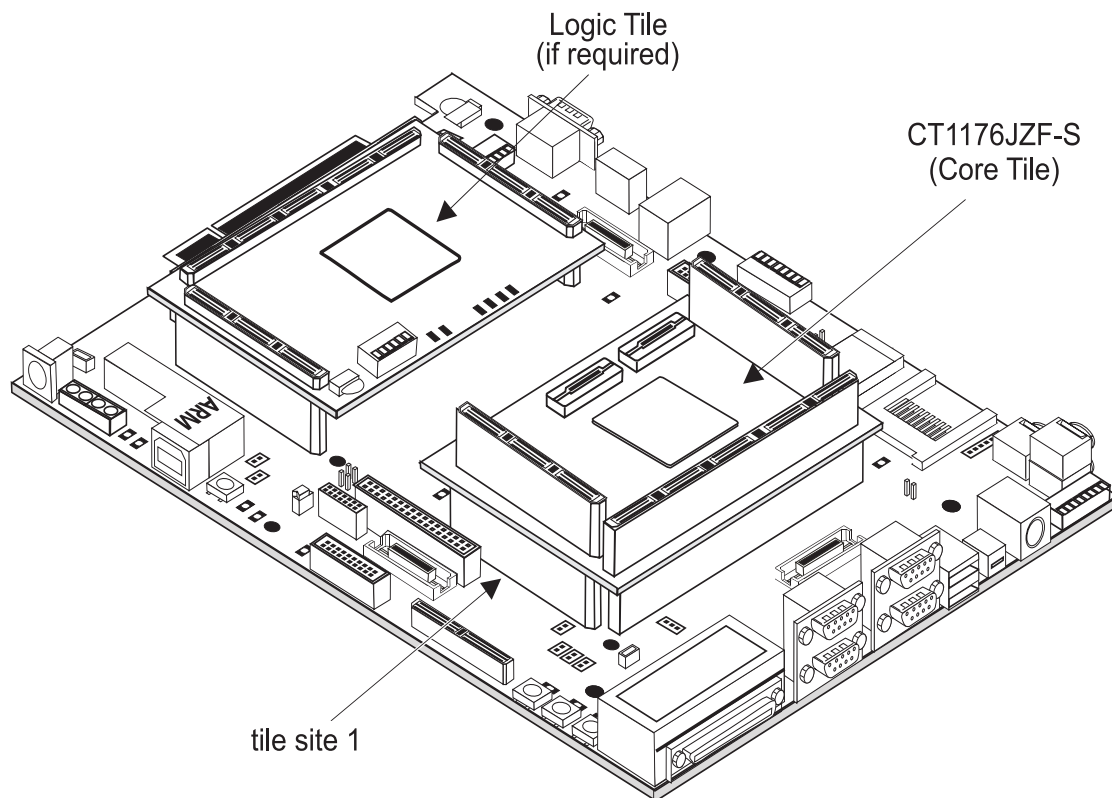


Figure 2-1 Core Tile, Logic Tile, and an Emulation Baseboard

Note

For details on how to load and run applications on an Emulation Baseboard system, see the *RealView Emulation Baseboard User Guide* (ARM DUI0303).

2.2 Connecting power

CT1176JZF-S power is supplied through power-blades in the header connectors. The power source is connected to the baseboard.

2.2.1 Supplying power to the EB

If the EB is not inserted into a PCI enclosure, you must connect the supplied 12VDC brick power supply to power socket J28 or an external bench power supply to the screw-terminal connector J27. See Figure 2-2.

Caution

You must only use one power source for the system. Use only the PCI connector, J27, or J28, do not, for example, use the PCI connector and J27 at the same time.

If you are using separate 5V and 3V3 bench supplies, always set sensible current limits. The 3V3 supply should follow the 5V supply on power up. On the EB, the 3V3 supply follows the 5V supply after an initial 1ms delay.

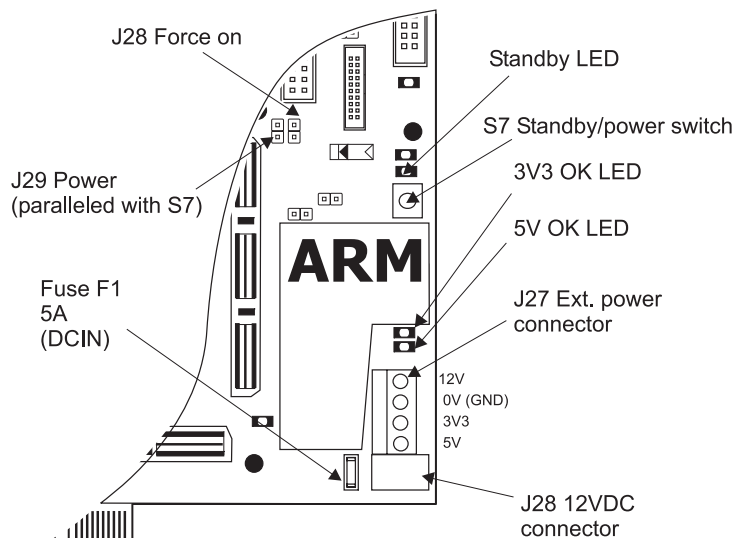


Figure 2-2 EB power connectors

Note

If you are using the supplied brick power supply connected to J28, the Standby/power push button S7 toggles the power on and off.

If you are using an external power supply connected to J27, or you are powering the board from the PCI backplane, the Standby/power switch is not used and power is controlled by shutting down the external power source.

2.3 Connecting JTAG debugging equipment

The Core Tile does not have a JTAG connector, but there are JTAG signals present on the header connectors. The Core Tile must be used with a baseboard that provides a JTAG connector. External JTAG equipment can be used to:

- Download and debug programs.
You can connect *RealView ICE* (RVI) or other JTAG debuggers to the external JTAG connector and download and debug programs.
- Download new images to the PLD on the Core Tile or to FPGAs or PLDs present on other attached boards.
For a CT1176JZF-S attached to an EB, either RVI or the USB debug port on the EB can be used for downloading FPGA images, but only RVI can be used for debug.

Selection between debugging programs and downloading new images to the FPGA is controlled by the CONFIG link or slide-switch on the baseboard. See the documentation supplied with the baseboard for more details on connecting JTAG and using the CONFIG link or slide-switch.

———— Caution ————

Because the Core Tile does not provide nonvolatile memory, programs are lost if the power is removed. Use flash memory for nonvolatile storage.

The flash memory can be:

- any unused space in the baseboard NOR flash
- nonvolatile memory available in the PISMO memory expansion slots on the baseboard.

Do not use spare EB configuration flash space (address range: 0x4C000000–0x4DFFFFFF) for program storage.

See the *Programmer's Reference* chapter in the *RealView Emulation Baseboard User Guide* (DUI0303) for details of the EB memory map.

The JTAG connector provides a set of signals that allow debugging equipment to be used. When debugging a development system with multiple tiles, connect the JTAG debugging equipment to the baseboard and the JTAG signals will be routed through any connected tiles. See *JTAG loopback control* on page 3-53 for details of the JTAG routing within a tile stack.

The JTAG debug and configuration paths are described in *JTAG support* on page 3-44 and *Debug and JTAG configuration* on page 4-37.

2.3.1 Connecting a JTAG device to the EB

The JTAG setup for the EB and RVI is shown in Figure 2-3 on page 2-8. (Refer to the documentation supplied with your debugger for information on connecting other JTAG interface products.)

Note

The low-density cable, shown in Figure 2-3 on page 2-8, can be used to connect the RealView ICE box directly to the baseboard JTAG connector, but this interface operates at lower speed.

The high-density cable from the RealView ICE box, shown in Figure 2-4 on page 2-10, operates at a higher speed but requires a buffer board to connect to the JTAG connector on the baseboard.

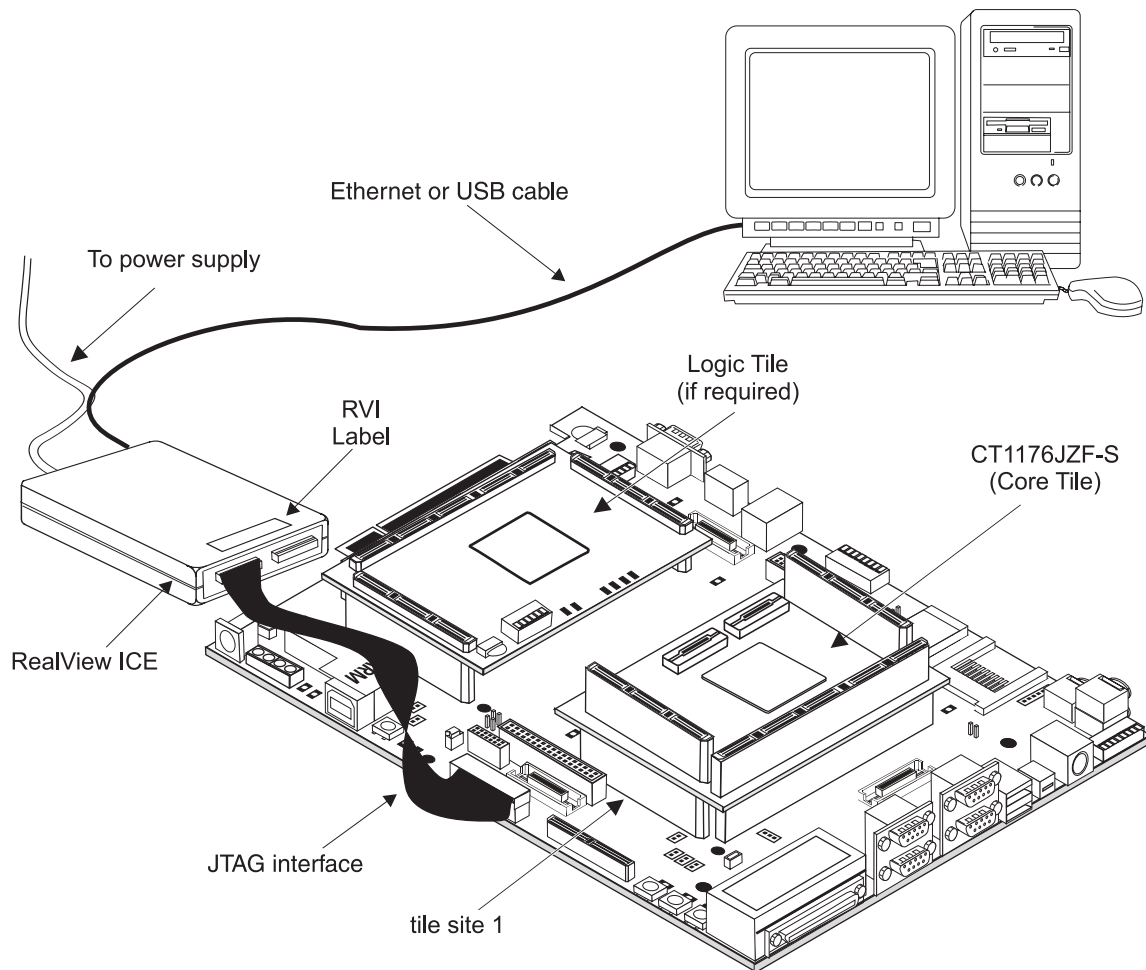


Figure 2-3 JTAG connection to an Emulation Baseboard

2.4 Connecting Trace

The ARM1176JZF-S test chip contains an *Embedded Trace Macrocell* (ETM) and Trace connectors are provided on the CT1176JZF-S. Use the JTAG connector on the baseboard to provide the JTAG signals that are required for controlling the ETM.

Note

Trace tools using multiplexed trace packets (such as RealView Trace) require only one Mictor® connector (Trace Port A). The CT1176JZF-S supports both multiplexed (one trace connector) and demultiplexed mode (two trace connectors). The second connector is present to support trace tools that use demultiplexed trace packets. The trace size supported by the connectors is medium (16-bit packets).

For details of the Mictor connector and the Trace port signals see *Trace Connectors* on page 5-22.

For more details on using Trace, see the documentation supplied with your Trace hardware.

2.4.1 Connecting the Trace Port Analyzer

For RealView Trace, connect the *Trace Port Analyzer* (TPA) to the adaptor board and plug the adaptor into the CT1176JZF-S as shown in Figure 2-4 on page 2-10. RealView Trace requires a RealView ICE JTAG unit connected to the baseboard. The Ethernet and power supply cables connect to the RealView ICE unit.

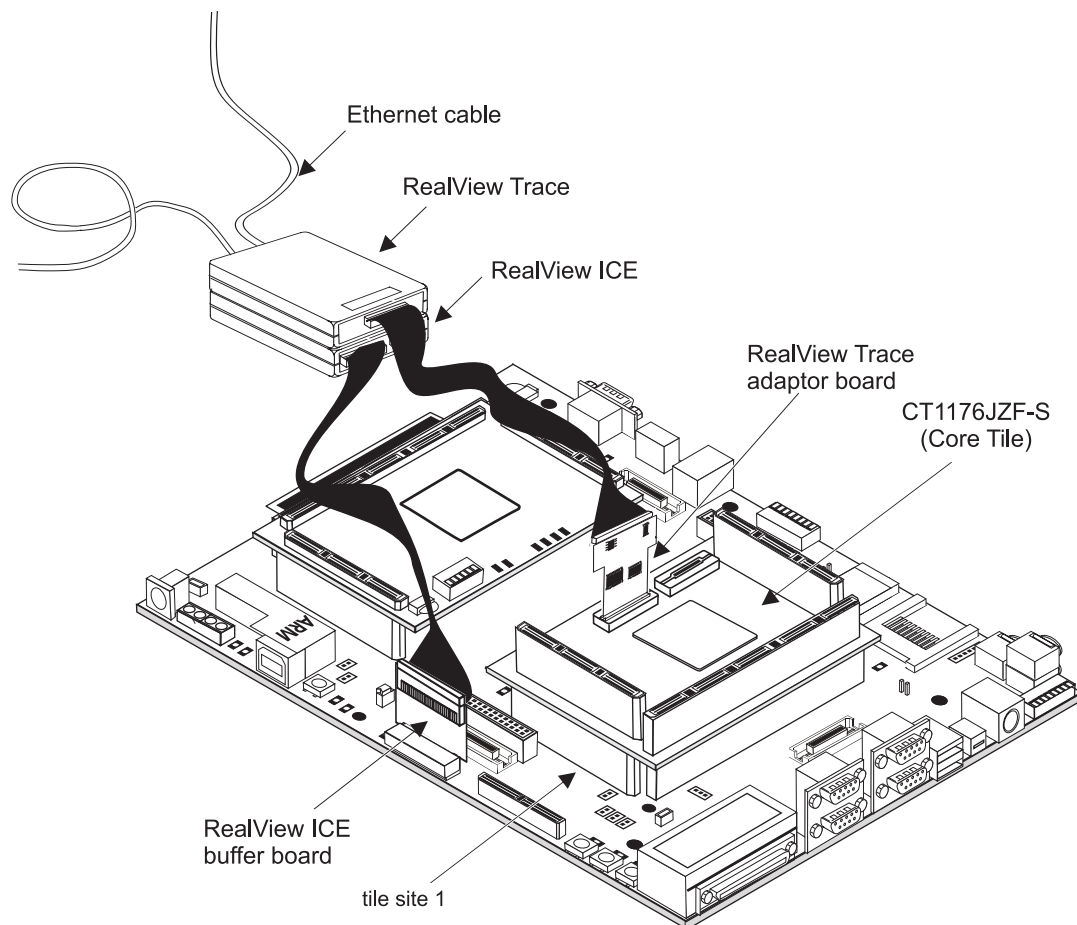


Figure 2-4 Trace connection with RealView Trace

2.5 Using the CT1176JZF-S with a custom baseboard

If you are designing a custom baseboard to accept a CT1176JZF-S, you must ensure that your board meets the following requirements:

Mechanical layout

The mechanical layout is described in *Mechanical details* on page A-5.

Note

Gerber files should be used for connector placement information. These are available from ARM Technical Support at:
www.arm.com/support/downloads/versatile.html

Power supplies

The CT1176JZF-S uses 3V3 and 5V supplies connected through power-blades in the header connectors. See *Header connectors* on page 5-2 for details.

The 3V3 supply (**3V3_VDDIO**) powers CT1176JZF-S components, the PLD bank that interfaces to the CT1176JZF-S I/O, and the test chip I/O (**VDDPAD**). Alternatively, an optional on-board supply (**ARM_VDDIO**) can provide the test chip I/O voltage (**VDDPAD**) at 1V8 or 2V5. When used, this supply also powers the three PLD I/O banks and the AXI bus demultiplexers that interface to the test chip I/O pins.

The 5V supply powers three onboard regulators that provide the **VDDCORE1**, **VDDCORE2**, and **VDDPLD** supplies required by the test chip and the CT1176JZF-S PLD:

VDDCORE1

A 1V2 power supply that provides internal power for:

- ARM1176JZF-S (**VDDCORE_ARM**)
- ETM11CS (**VDDCORE_ETM**)

VDDCORE2

A 1V0 power supply that provides internal power for:

- PLL circuitry (**PLLVDD25** and **PLLVDD10**)

Note

The signal naming is necessary for legacy reasons and does not reflect the actual voltages applied.

- test chip internal logic (**VDDCORE_TC**)

VDDPLD

A 1V8 power supply that provides internal power for the PLD (VDDPLD).

See *Typical current requirements* on page A-4 and *Power supply control* on page 3-16 for details on the voltage control logic.

Clock control

Your primary reference clock must be supplied by an attached Logic Tile or baseboard. The CT1176JZF-S clocking system is described in Chapter 3 *CT1176JZF-S Hardware Description* and the ARM1176JZF-S test chip specific clocking requirements are described in Chapter 4 *Test Chip Hardware Description*.

See also the *ARM1176JZF-S Processor Technical Reference Manual* (ARM DDI 0301).

JTAG control

The CT1176JZF-S does not have a JTAG connector. The baseboard must provide a JTAG connector and route the JTAG signals to the header signals on the Core Tile. JTAG routing is described in *JTAG support* on page 3-44 and *Debug and JTAG configuration* on page 4-37.

Bus configuration signals

Due to pin limitations on header HDRX, the ARM1176JZF-S AXI bus is distributed through multiplexers to the baseboard. The custom baseboard must use a similar multiplex scheme to access the ARM1176JZF-S AXI bus. See *AXI bus multiplexing* on page 3-21 for details.

AXI slaves

In order for the ARM1176JZF-S to run code, the entire memory must be decoded and either return a valid response or generate an error.

———— Note ————

ARM Support will only be able to provide limited help in solving problems associated with Custom Baseboard designs.

Chapter 3

CT1176JZF-S Hardware Description

This chapter describes the on-board hardware of the CT1176JZF-S. It contains the following sections:

- *Core Tile architecture* on page 3-2
- *About the ARM1176JZF-S test chip* on page 3-3
- *Clocks* on page 3-5
- *Resets and interrupts* on page 3-9
- *Power supply control* on page 3-16
- *AXI bus multiplexing* on page 3-21
- *Overview of Core Tile configuration* on page 3-25
- *Memory configuration* on page 3-40
- *Register configuration* on page 3-41
- *JTAG support* on page 3-44.

Note

The HBI-0154 board supports the ARM1176JZF-S test chip, but the availability of boards depends on the availability of test chips. Contact your sales representatives for details on currently available Core Tiles.

3.1 Core Tile architecture

The high level architecture of the CT1176JZF-S is shown in Figure 3-1.

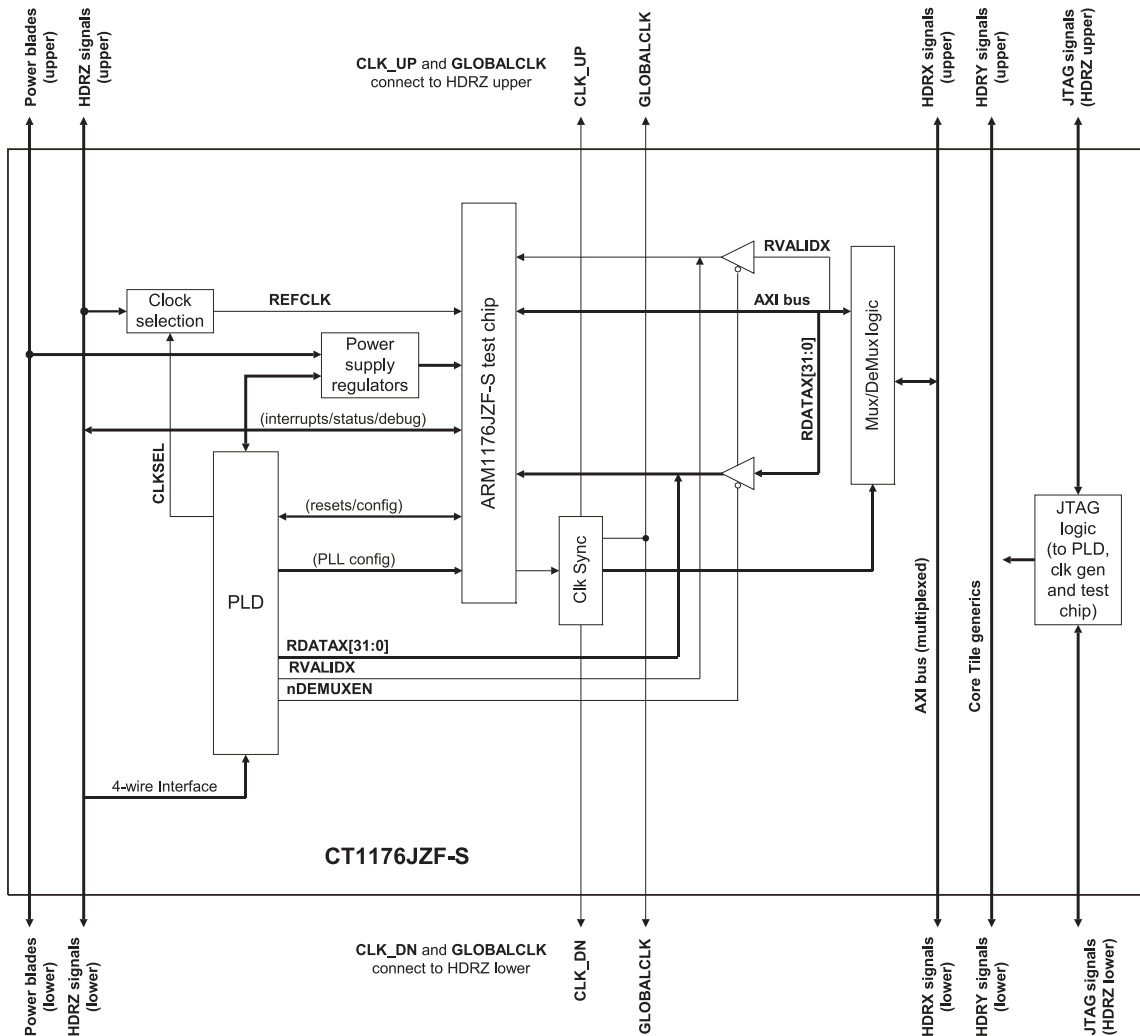


Figure 3-1 CT1176JZF-S block diagram

3.2 About the ARM1176JZF-S test chip

The ARM1176JZF-S test chip is a proof-of-concept vehicle for the ARM1176JZF-S processor and is built for two reasons:

- it enables you to functionally validate the ARM1176JZF-S processor on the silicon process it is built on
- you can use it as a building block to create prototype systems designed for product and operating system development.

The ARM1176JZF-S test chip functionality consists of:

- ARM1176JZF-S processor featuring
 - ARM11 ARM architecture v6
 - ARM and Thumb instruction sets
 - Single Instruction, Multiple-Data (SIMD) DSP instructions
 - Jazelle technology to enable direct execution of Java bytecodes
 - TrustZone™ security extensions
 - provision for *Intelligent Energy Management* (IEM™)

———— **Note** ————

The ARM1176JZF-S test chip does not support IEM. The four IEMslices in the test chip serve only as clock synchronizers, enabling the ARM1176JZF-S core to operate at a higher frequency than the AXI sub-system. See *ARM1176JZF-S test chip overview* on page 4-2 for details.

- 16KB ICache and 16KB DCache with parity checking
 - 16KB ITCM and 16KB DTCM
 - Instruction and Data *Memory Management Units* (MMUs)
 - *Vector Floating-Point* (VFP) coprocessor
 - AMBA 3 *Advanced eXtensible Interface* (AXI)
 - trace support
 - JTAG-based debug.
- Memory BIST Controller for testing RAM blocks within the ARM1176JZF-S processor
- *CoreSight ARM11 Embedded Trace Macrocell* (ETM11CS)
- *AXI Configurable Interconnect* (ACI)
- external AMBA 3 AXI interface
- AXI RAM blocks, 64KB x2
- *AHB Exclusive Access Monitor* (ExAcMo64) with byte writable AHB SRAM block, 16KB

- AHB sub-system comprising:
 - *Vectored Interrupt Controller* (VIC)
 - *Pin Capture Block* (PCAPT)
 - ETB11 AHB access
 - *AHB to APBv3 Bridge* (APB Bridge).
- APB sub-system comprising:
 - dummy slave (generates AXI SLVERR responses)
 - ETM11CS APB access
- PLL and clock generation
- boundary scan logic
- input and output pads.

See *ARM1176JZF-S test chip overview* on page 4-2 for a system block diagram, and details of the major test chip components.

3.3 Clocks

The CT1176JZF-S requires a single external reference clock, **REFCLK**. This clock is routed via header HDRZ either from the board below as **CLK_NEG_UP_IN**, or the board above as **CLK_NEG_DN_IN**, depending on the position of the CT1176JZF-S in the system stack and the board combination used.

The CT1176JZF-S also has an on-board 24MHz clock generator. This clock is required by logic inside the CT1176JZF-S control PLD.

As shown in Figure 3-2 on page 3-6 clock distribution and phase control of the AXI clock, **ACLKX** from the test chip is provided on board by an ispClock5620 programmable clock generator. The ispClock5620 is PLL based and provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile EEPROM memory. The CT1176JZF-S uses the ispClock5620 in a single pre-programmed standalone configuration.

Note

Figure 3-2 on page 3-6 is a simplified clock distribution diagram. The additional deskewed clock sources are used to multiplex the AXI port signals from the test chip onto the CT1176JZF-S header HDRX. See *AXI bus multiplexing* on page 3-21 for details.

3.3.1 Clock routing

The clock routing for the CT1176JZF-S and EB combination is shown in Figure 3-2 on page 3-6. This figure also shows the clock hardware initialization signals. See *Clocks* on page 4-22 details of the clock routing within the ARM1176JZF-S test chip.

Selection of the clock source for the Core Tile is controlled by **CLKSEL** from the CT1176JZF-S PLD. **CLKSEL** selects the clock source as **CLK_NEG_DN_IN** from the board above, or **CLK_NEG_UP_IN** from the board below. The value of **CLKSEL** is set locally during power up by the CT1176JZF-S PLD.

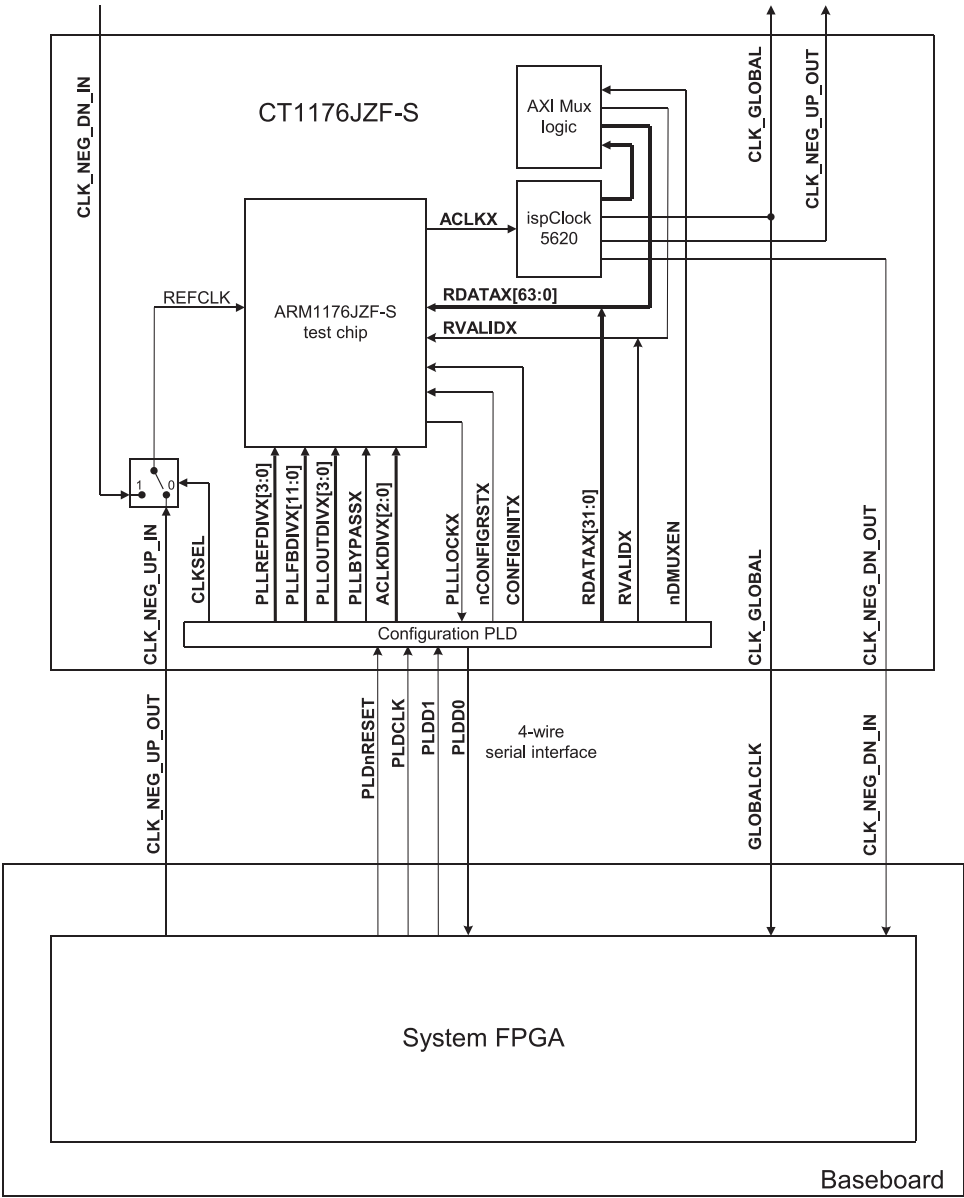


Figure 3-2 Clock routing and hardware initialization

3.3.2 Clock setting in reset mode

Clock setting in reset mode requires the initialization of the test chip PLL and the test chip Clock Divider. Hardware initialization is controlled by firmware on the system baseboard.

PLL initialization

The **PLLREFDIVX[3:0]**, **PLLFBDIVX[11:0]**, and **PLLOUTDIVX[3:0]** divider values for the test chip PLL are set directly by the PLD on the CT1176JZF-S using the pins provided on the test chip. During reset, initialization values for the test chip PLL are transferred from the system baseboard to the CT1176JZF-S PLD via the 4-wire serial interface. See *Clock routing and hardware initialization* on page 3-6 for interconnect details.

Clock Divider initialization

During reset the **CONFIGINITX**, **nCONFIGRSTX**, **RVALIDX**, and **RDATAX[31:10]** signals are driven by the CT1176JZF-S PLD to initialize the *Config-init register* in the test chip. The values written to this register are initialization values for fields in the test chip *ClkCtl register*. This register sets the division ratios of the test chip Clock Divider. See *Test chip configuration* on page 4-32 and *Clock divider* on page 4-26 for further information.

nCONFIGRSTX

Resets the *test chip configuration registers*.

CONFIGINITX

Enables clocking of the *test chip configuration registers*.

The **CONFIGINITX** pulse defines valid data on the **RDATAX[31:0]** bus and is HIGH for at least two **REFCLK** cycles.

———— Note ————

CONFIGINITX enables simultaneous clocking of all *test chip configuration registers*. To prevent corruption of data in the register set, **RVALIDX** and all bits of **RDATAX[31:0]** must be valid when **CONFIGINITX** is HIGH.

The **nCONFIGRSTX** and **CONFIGINITX** test chip configuration signals are controlled by the CT1176JZF-S PLD and are not accessible at the Core Tile headers.

The ARM1176JZF-S test chip power-on configuration timing is shown in Figure 3-3.

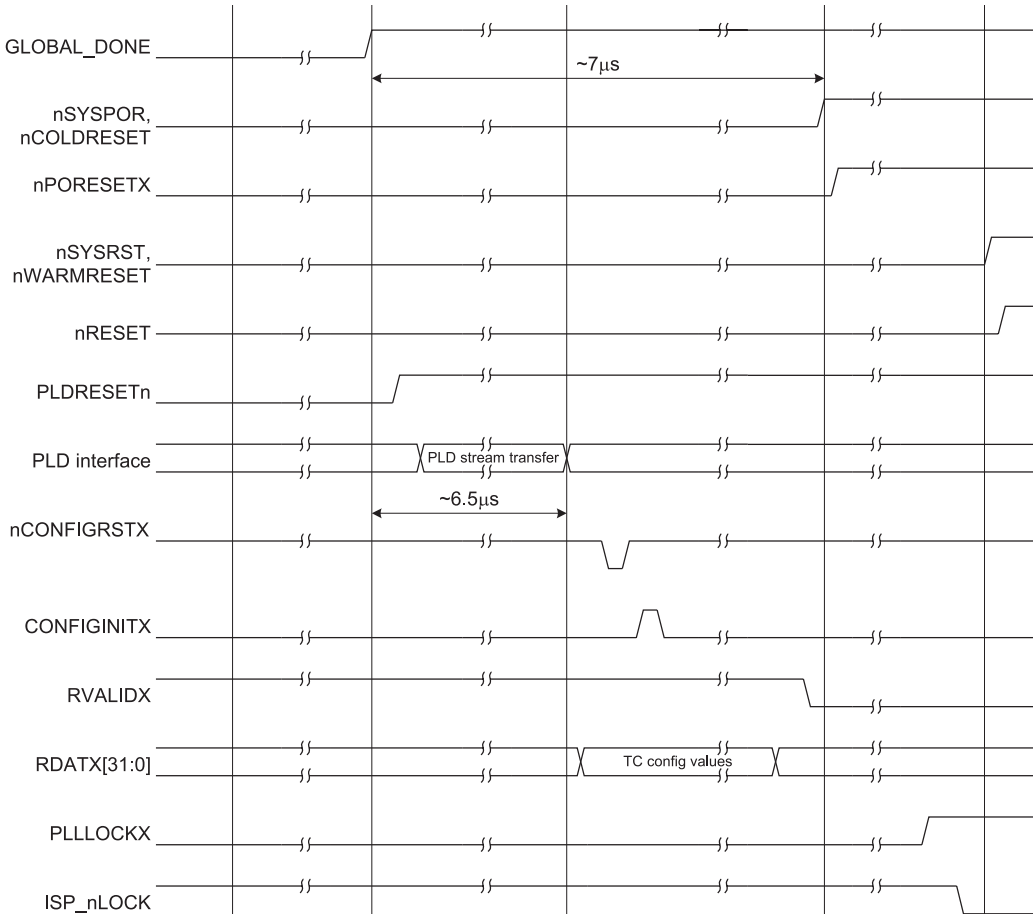


Figure 3-3 Power-on ARM1176JZF-S test chip configuration timing

3.4 Resets and interrupts

This section describes the reset and interrupt signals and contains the following sections:

- *Resets*
- *Interrupts* on page 3-14.

3.4.1 Resets

This section describes the resets and contains the following subsections:

- *Baseboard reset*
- *ARM1176JZF-S test chip reset*
- *Reset routing* on page 3-10
- *Reset sequence* on page 3-12.

Several resets are required by the baseboard and the CT1176JZF-S test chip.

Baseboard reset

The reset logic on the baseboard initializes attached Logic Tiles and Core Tiles, the system FPGA, and external controllers as a result of a reset. The baseboard has several reset sources and generates several reset signals.

The EB reset sources and the function of the EB reset signals are described in the *RealView Emulation Baseboard User Guide* (ARM DUI0303).

The baseboard generates the **nSYSPOR**, **nSYSRST**, **nWARMRST** and **nCOLDRST** signals for the CT1176JZF-S.

ARM1176JZF-S test chip reset

The following signals are used to reset the ARM1176JZF-S test chip:

- **nPORESETX**
- **nRESETX**.

The function of these signals is described in Chapter 4 *Test Chip Hardware Description*, in *Resets* on page 4-35.

Reset routing

The reset routing between the baseboard, CT1176JZF-S logic, and the ARM1176JZF-S test chip is shown in Figure 3-4 on page 3-11 and comprises of:

nSYSPOR	Power-on reset, active LOW.
nSYSRST	System reset, active LOW.
nCOLDRST	CT1176JZF-S specific software reset, active LOW.
nWARMRST	CT1176JZF-S specific system reset, active LOW.
PLLLOCKX	ARM1176JZF-S test chip PLL locked, active HIGH.
ISP_nLOCK	ispClock5620 clock generator PLL locked, active LOW.
GLOBAL_DONE	System FPGAs configured, active HIGH, open-drain.
D_nSRST	JTAG reset request signal to or from the CT1176JZF-S and the debugger, active LOW, open-drain.

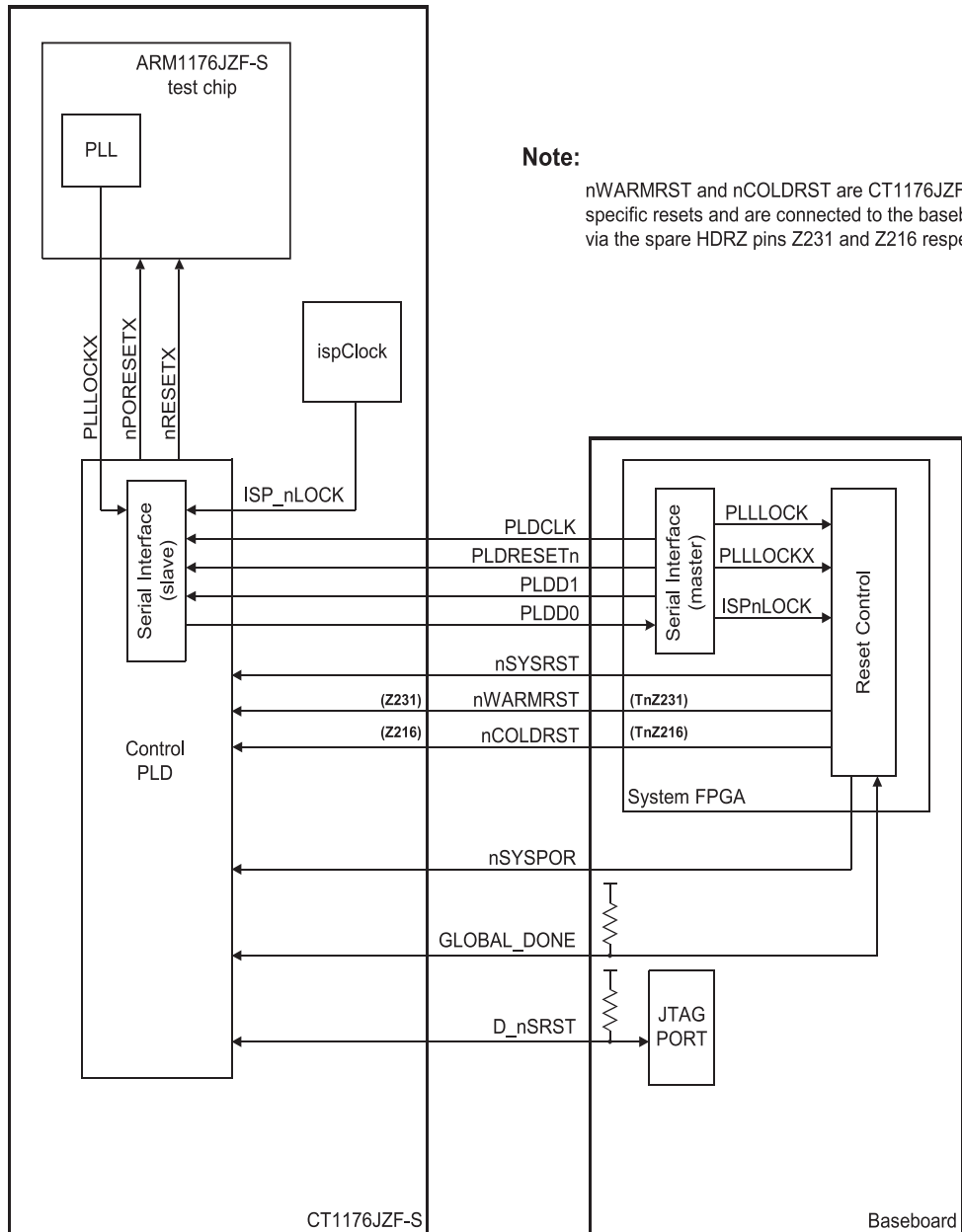


Figure 3-4 Reset routing

Reset sequence

Correct initialization of a Core Tile and its associated baseboard requires a timed reset sequence. Details of the EB reset sequence are detailed in the *RealView Emulation Baseboard User Guide* (ARM DUI 0303). The power-on reset timing required when using a CT1176JZF-S in combination with a baseboard is shown in Figure 3-5. The reset signals are described in Table 3-1 on page 3-13.

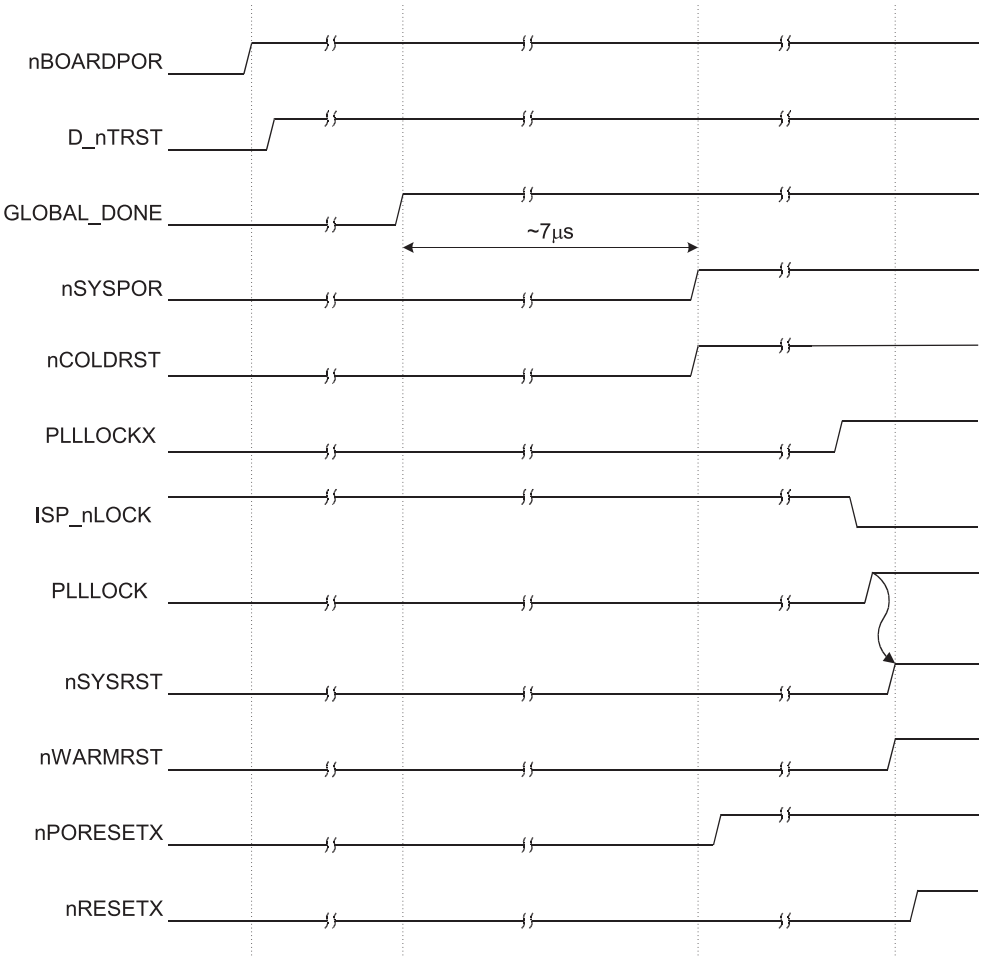


Figure 3-5 Baseboard and CT1176JZF-S power-on reset sequence

Reset signals

Table 3-1 describes the system reset signals. A reset controller, implemented in the baseboard system FPGA, monitors the reset sources and generates the appropriate reset signals. See *JTAG signal description* on page 3-45 for a description of the JTAG reset signals.

Table 3-1 Reset signals

Name	Function
nBOARDPOR	This signal resets the baseboard system FPGA. This signal is also used to generate D_nTRST at power on.
D_nSRST	System reset request to or from the CT1176JZF-S and an attached debugger, active LOW, open-drain.
GLOBAL_DONE	A configuration signal, active during reset. This is an open-collector configuration signal that goes HIGH when all FPGAs have finished configuring. The system is held in reset until this signal goes HIGH.
nSYSPOR	Power-on reset signal that initializes the reset level state machine in the baseboard system FPGA. There is a fixed 7μs delay after GLOBAL_DONE goes HIGH before nSYSPOR is released. Functions also as the power-on reset signal for the ARM1176JZF-S test chip logic.
nCOLDRST	A Core Tile specific software reset signal generated from nSYSPOR by the baseboard system FPGA.
ISP_nLOCK	An ispClock5620 clock generator status signal. ISP_nLOCK indicates when the clock generator is locked to ACLKX . It is used with PLLLOCKX to control the PLLLOCK bit that is used by the baseboard reset controller to determine when all clocks are stable and the main system reset, nSYSRST and the CT1176JZF-S specific reset, nWARMRST can be released. ISP_nLOCK is an active LOW signal.
PLLLOCKX	A PLL status signal. PLLLOCKX indicates when the ARM1176JZF-S test chip PLL is locked to REFCLK . It is used with ISP_nLOCK to control the PLLLOCK bit that is used by the baseboard reset controller to determine when all clocks are stable and the main system reset, nSYSRST and the CT1176JZF-S specific reset, nWARMRST can be released.
PLLLOCK	A CT1176JZF-S status signal sent to the baseboard via the 4-wire serial interface. PLLLOCK goes HIGH when PLLLOCKX and ISP_nLOCK indicate that all CT1176JZF-S derived clocks are stable.
nSYSRST	Main system reset.

Table 3-1 Reset signals (continued)

Name	Function
nWARMRST	A Core Tile specific system reset signal generated from nSYSRST by the baseboard system FPGA.
nPORESETX	ARM1176JZF-S test chip logic power-on reset.
nRESETX	ARM1176JZF-S test chip reset.

3.4.2 Interrupts

This section describes the interrupts and contains the following subsections:

- *FIQ and IRQ interrupts*
- *Debug communications interrupts* on page 3-15

FIQ and IRQ interrupts

The ARM1176JZF-S *Fast Interrupt Request*, **nFIQ** and normal interrupt request, **nIRQ** inputs are supported at the HDRZ header pins, Z205 and Z206 respectively. When used with the EB, the **nFIQ** and **nIRQ** inputs are controlled by separate *Generic Interrupt Controllers* (GICs) in the FPGA. The GICs service interrupt inputs from further FPGA devices, external peripherals, the PCI expansion bus, and the PISMO memory expansion bus. See *RealView Emulation Baseboard User Guide* (ARM DUI 0303) for further information on EB interrupt handling.

A FIQ is externally generated by taking the **nFIQ** signal input LOW. While the use of nested **nFIQ** interrupts is not recommended, if this cannot be avoided, you must save any corruptible registers and re-enable FIQs and interrupts after handling the exception.

———— **Note** ————

The **nFIQ** input is registered internally by the ARM1176JZF-S processor and it is the output of this register that is used by the ARM1176JZF-S processor control logic. See *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301) for further details on ARM1176JZF-S interrupt handling.

An IRQ is externally generated by a LOW level on the **nIRQ** input. An IRQ has a lower priority than a FIQ, and is masked on entry to a FIQ sequence.

Debug communications interrupts

The debug communication channel interrupts **COMMTX** and **COMMRX** from the ARM1176JZF-S are supported at the HDRZ header pins, Z211 and Z210 respectively. When used with the EB, the **COMMTX** and **COMMRX** outputs are routed as interrupt requests to the GIC in the FPGA that generates the IRQ to the ARM1176JZF-S.

COMMTX indicates that the communications channel is available for the processor to pass messages to the debugger.

COMMRX indicates to the processor that messages are available for the processor to read.

3.5 Power supply control

The baseboard system FPGA implements registers and a 4-wire serial interface to the CT1176JZF-S PLD to enable you to:

- change the voltage supplied to the ARM1176JZF-S test chip by writing values to the serially-programmed *digital to analog converters* (DACs)
- read CT1176JZF-S on-board voltages and currents from an 8-channel 12-bit *analog to digital converter* (ADC).

The voltage control and voltage and current monitoring scheme is shown in simplified form in Figure 3-6 on page 3-17.

The serial write data register in the CT1176JZF-S PLD is updated continuously with values from the system registers in the baseboard system FPGA. These values control **VOLTAGE_CTRLA** and **VOLTAGE_CTRLB** that set the voltages applied to the ARM1176JZF-S test chip.

The system registers in the baseboard system FPGA are continually updated with voltage and current monitoring values from the serial read data register in the CT1176JZF-S PLD.

The DAC and ADC data values are transferred via the 4-wire serial interface.

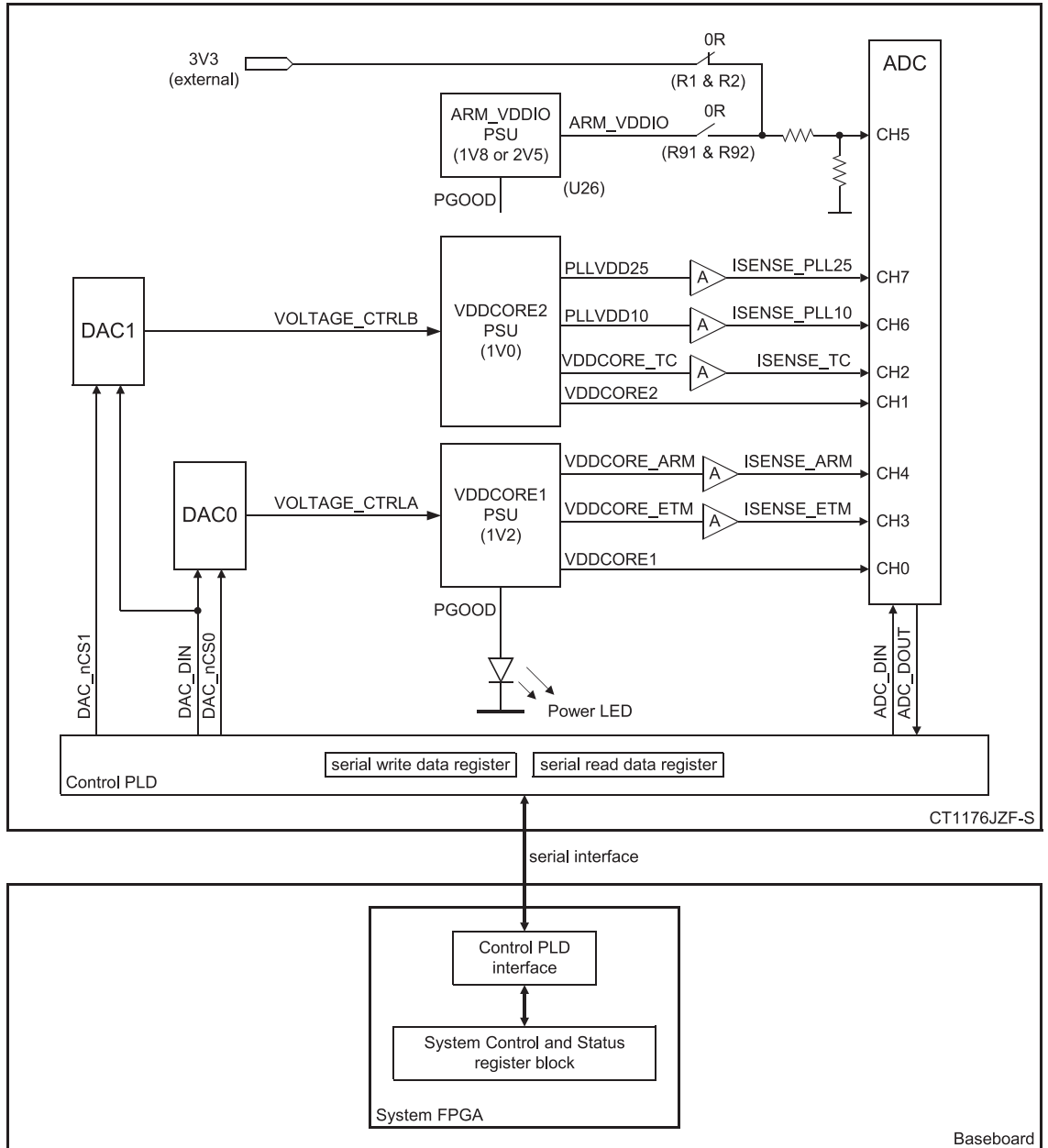


Figure 3-6 Voltage control and voltage and current monitoring

3.5.1 Setting the CT1176JZF-S test chip voltage

The core voltages depend on:

- The feedback resistors for the regulators
 - resistors R73, R74, and R75 are the feedback resistors for the **VDDCORE1** 1V2 supply that provides **VDDCORE_ARM** and **VDDCORE_ETM** voltages to the ARM1176JZF-S test chip
 - resistors R82, R83, and R84 are the feedback resistors for the **VDDCORE2** 1V0 supply that provides **VDDCORE_TC**, and **PLLVD10** and **PLLVD25** voltages to the ARM1176JZF-S test chip
 - resistors R88, R89, and R90 are the feedback resistors for the optional **ARM_VDDIO** 1V8 or 2V5 regulator (set at manufacture).

———— Note ————

The **ARM_VDDIO** supply can be set to 1V8, 2V5 or 3V3.

In the standard build, zero ohm resistors R1 and R2 are fitted and connect **ARM_VDDIO** to the 3V3 external supply. Zero ohm resistors R91, R92 and the **ARM_VDDIO** regulator U26 are not required, in the standard build, and are not fitted.

- resistors R126, and R127 are the feedback resistors for the **VDDPLD** 1V8 supply.

———— Warning ————

These resistors define all the supply voltages at power-on and also the adjustment range for the **VDDCORE1** and **VDDCORE2** supplies, These resistors are fitted at manufacture to give the correct core and PLL voltages for the ARM1176JZF-S test chip.

Unauthorized modification of these resistor values will invalidate the product warranty. You should only use the DAC and ADC interfaces provided to adjust and read the supply voltages.

- The values loaded into the PLD for the DAC settings. The values provide a positive or negative offset to the default power-on voltages.

The output voltages are given by

- $\text{VDDCORE1} = 0.8\text{V} * (1 + ([R75/R73]+[R75/R74])) - (I_{\text{dac}}*R75)$
- $\text{VDDCORE2} = 0.6\text{V} * (1 + ([R84/R82]+[R84/R83])) - (I_{\text{dac}}*R84)$
- $\text{ARM_VDDIO} = 0.8\text{V} * (1 + [R90/R88]+[R90/R89])$
- $\text{VDDPLD} = 0.6\text{V} * (1 + [R127/R126])$

Idac is the current sourced at **VOLTAGE_CTRLA** or **VOLTAGE_CTRLB** by the associated DAC. The current range is 0 to 50µA. At power up Idac is set to 25µA.

The resistor values are chosen to give a ±0.12V adjustment range for **VDDCORE1**, and a ±0.1V adjustment range for **VDDCORE2**. The default value loaded into the 8 bit DAC is 0x80. A value of 0xFF gives maximum negative offset from the default (-0.12V for **VDDCORE1** and -0.1V for **VDDCORE2**) and a value of 0x0 gives maximum positive offset from the default (+0.12V for **VDDCORE1** and +0.1V for **VDDCORE2**).

Note

See *Application Note* AN177 for details of the RealView Emulation Baseboard system registers that control the CT1176JZF-S voltages. *Application Notes* are available on the CD that accompanied the product and from the ARM website at:
http://www.arm.com/documentation/Application_Notes/index.html.

3.5.2 Reading the voltages and currents

The ADC on the CT1176JZF-S continuously reads the voltages and currents and updates the read serial data register in the CT1176JZF-S PLD. The PLD sends these values over the 4-wire serial interface to the baseboard.

The ADC is a 12 bit serial converter and uses an external 2.048V reference. The LSB of the ADC reading corresponds to 500µV (the 2.048V reference of the ADC divided by 4096).

The formulae to calculate the supply voltages are:

$$\text{VDDCORE1} = \text{INT}(\text{ADC}[11:0] * (500 * 10^{-6}))$$

$$\text{VDDCORE2} = \text{INT}(\text{ADC}[11:0] * (500 * 10^{-6}))$$

$$\text{ARM_VDDIO} = \text{INT}(\text{ADC}[11:0] * (1 * 10^{-3}))$$

Voltages proportional to the supply currents are developed across R_{sense} resistors. Each of the sense resistors has a voltage amplifier that has a fixed gain of 100. This is necessary because the voltage developed across the sense resistor is too low to measure directly with the ADC.

The formula to calculate the current (I) drawn by a supply is:

$$I = V / (100 * R_{\text{SENSE}})$$

The default R_{SENSE} values for the power supplies and the voltage to current relationship are shown in Table 3-2

Table 3-2 Supply current sensing

Power Supply	R_{SENSE}	Volt/Amp
VDDCORE_TC (1V0)	$R76 = 0.25\Omega$	25
VDDCORE_ETM (1V2)	$R77 = 0.2\Omega$	20
VDDCORE_ARM (1V2)	$R78 = 0.05\Omega$	5
PLLVDD10 (1V0)	$R79 = 1\Omega$	100
PLLVDD25 (1V0)	$R85 = 1\Omega$	100

Note

See the *Application Note* AN177 for details of the RealView Emulation Baseboard system registers that monitor the CT1176JZF-S currents. *Application Notes* are available on the CD that accompanied the product and from the ARM website at: http://www.arm.com/documentation/Application_Notes/index.html.

Power LED

The power-good signal (**PGOOD**) from the **VDDCORE1** and **ARM_VDDIO** supply step-down regulators is pulled LOW if the output voltage is not within $\pm 7.5\%$.

The **PGOOD** signal is buffered and drives the CT1176JZF-S on board POWER LED indicator, D1. See *LED indicators* on page 5-31 for details of all the CT1176JZF-S indicators.

3.6 AXI bus multiplexing

This section describes the AXI bus multiplexing. A multiplexing scheme is necessary to reduce the number of pins required on the HDRX header.

3.6.1 Multiplexing scheme

The CT1176JZF-S AXI bus multiplexing and demultiplexing scheme is shown in Figure 3-7.

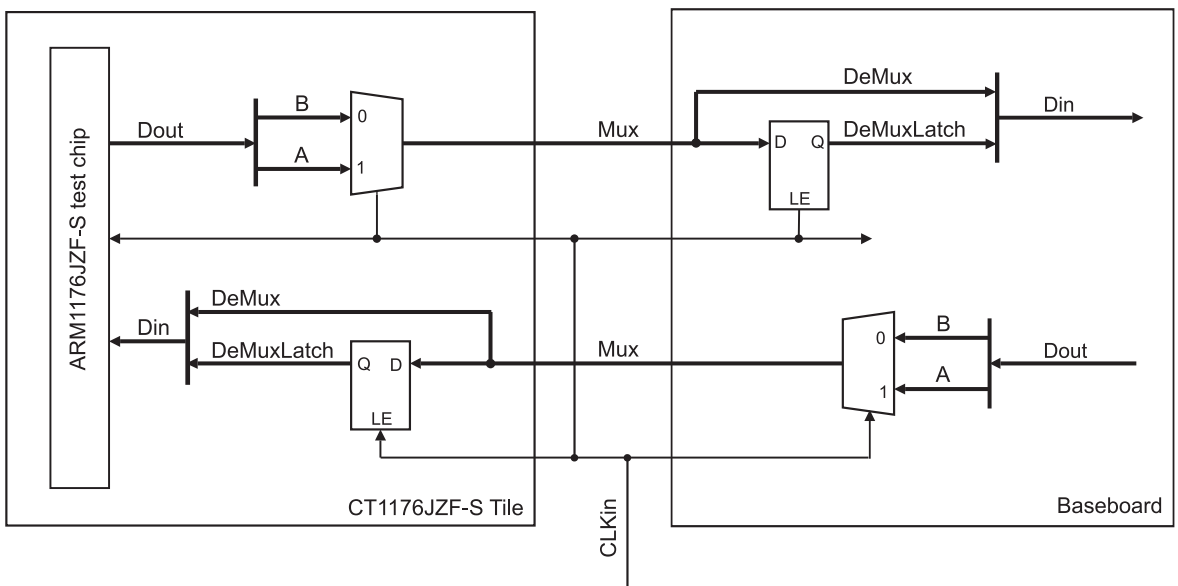


Figure 3-7 CT1176JZF-S AXI bus multiplexing scheme

Data is multiplexed as follows:

Dout is split bitwise into data **Dout/A** and **Dout/B** and is multiplexed onto **Mux** depending on the level of **CLKin**. When **CLKin** is HIGH, **Dout/A** is selected and when **CLKin** is LOW, **Dout/B** is selected. For example, when **CLKin** is HIGH, **WDATAX[31:0]** is selected and when **CLKin** is LOW, **WDATAX[63:32]** is selected. See *HDRX signals* on page 5-3 for details of the AXI multiplexed signals.

Data is de-multiplexed as follows:

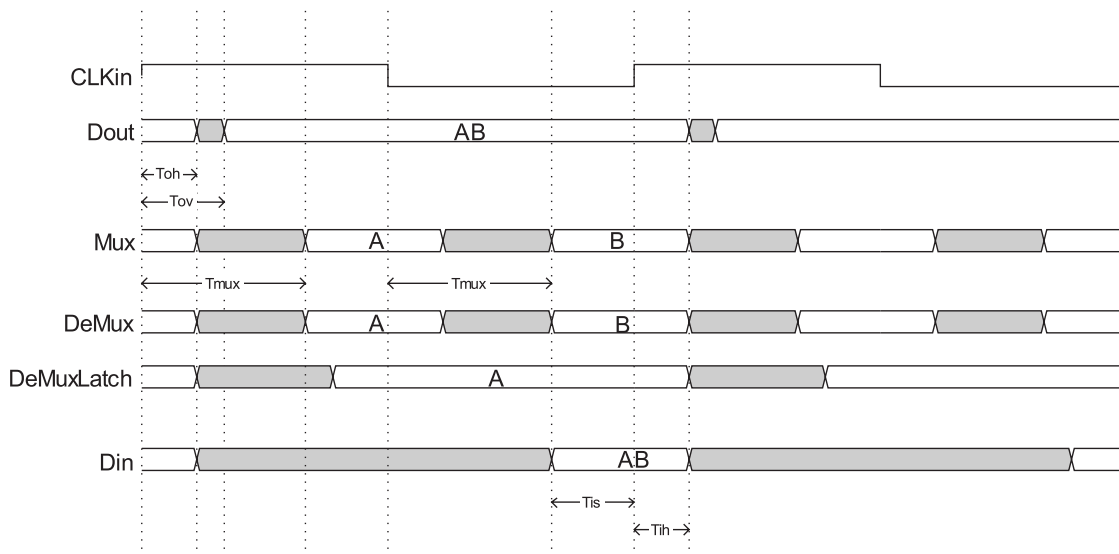
Dout/A is present on **Mux** when **CLKin** is HIGH and is latched onto **DeMuxLatch** when **CLKin** goes LOW. **Dout/B** is present on **Mux** when **CLKin** is LOW and is passed straight through as **DeMux**. **DeMuxLatch** and **DeMux** are combined bitwise as **Din**.

Note

CLKin is driven by distributed outputs from the ispClock5620 clock generator. The ispClock5620 clock generator is driven by **ACLKX** from the ARM1176JZF-S test chip.

This design requires that **Dout** is generated on the rising edge of **CLKin**, and that **Din** is captured on the rising edge of **CLKin**.

The multiplexer timing requirements at the board headers are shown in Figure 3-8.



Timing requirements;

Toh	min = 0ns	(output hold)
Tov	max = 2ns	(output valid)
Tis	max = 2ns	(Input setup)
Tih	max = 0ns	(input hold)
Tmux	max = 6ns	(multiplexer and board delay)

The CLKin is the clock driven into the ARM1176JZF-S Test Chip from the Core Tile.
All I/O timing must be with respect to this clock.

Figure 3-8 CT1176JZF-S AXI mux timing

AXI multiplexing logic

The practical implementation of the AXI multiplexing is shown in Figure 3-9.

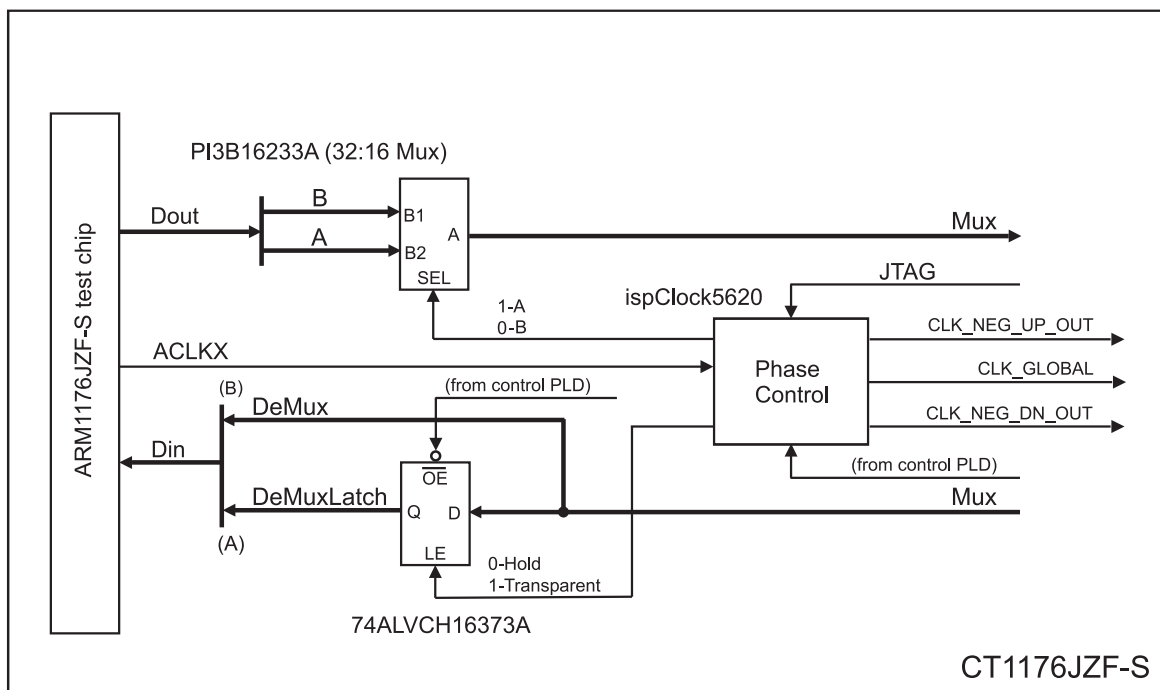


Figure 3-9 ARM1176JZF-S AXI multiplexing logic

The AXI bus clock, **ACLKX** from the ARM1176JZF-S test chip is distributed to the multiplexer, *PI3B16233A* and the latch, *74ALVCH16373A*. Phase control of these signals is critical for the correct operation of the mux/demux scheme at high AXI clock frequencies. Phase control is achieved with the ispClock5620 clock generator. This minimizes clock skew issues in the multiplexing logic. The clock generator non-volatile configuration settings are JTAG configurable when the CT1176JZF-S is in JTAG configuration mode. See *JTAG control and clock routing* on page 3-48 for further details.

AXI signal routing

The AXI bus signals are 2:1 multiplexed onto pins X0 through to X143 on the CT1176JZF-S HDRX header.

See *HDRX signals* on page 5-3 for pinout information.

Test chip signal routing

In addition to the Core Tile generic HDRZ connections, a number of signals are required when interfacing to the ARM1176JZF-S test chip. These signals are connected to pins Z205 through to Z231 on the CT1176JZF-S HDRZ header. These signals include interrupts, resets, debug, and trace support. Several of these signals are passed through the CT1176JZF-S PLD to provide CT1176JZF-S I/O to ARM1176JZF-S test chip I/O voltage translation. See *CT1176JZF-S PLD* on page 3-25 for further details.

3.7 Overview of Core Tile configuration

The ARM1176JZF-S test chip, clock source, voltage levels, and a number of system parameters are configurable on the CT1176JZF-S. In a final product, core configuration is static and the core configuration signals are tied HIGH or LOW and the voltage and clocks are fixed. However, the CT1176JZF-S allows you to program these signals for experimentation.

There are several ways that CT1176JZF-S configuration occurs:

- The CT1176JZF-S PLD.

This is the primary configuration source. The PLD serial registers are described in *CT1176JZF-S serial registers* on page 3-41.

———— Note ————

The extent of configuration performed by the CT1176JZF-S PLD is dependant on the type of reset applied to the Core Tile.

- CT1176JZF-S specific configuration registers in the baseboard system FPGA. These registers allow you to change several of the parameters controlled by the CT1176JZF-S PLD.

See *Application Note AN177* supplied on the Versatile CD for details of the registers implemented in the EB system FPGA.

- Signals present on the Core Tile connector HDRZ.

- Control registers in the ARM1176JZF-S test chip.

The control registers in the test chip are described in Chapter 4 *Test Chip Hardware Description*.

- Control registers in the ARM1176JZF-S.

For details of the registers in the ARM1176JZF-S see the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301)

3.7.1 CT1176JZF-S PLD

The CT1176JZF-S PLD performs the following functions:

- loading of data to the DACs that control the programmable power supplies (see *Power supply control* on page 3-16)
- reading of data from the ADCs that monitor the ARM1176JZF-S test chip voltages and currents (see *Reading the voltages and currents* on page 3-19)

- configuring the ARM1176JZF-S test chip PLL on power up (see *Clocks* on page 3-5)
- initializing the ARM1176JZF-S test chip *Config-init register* (see *Config-init register* on page 4-32)
- controlling resets to the ARM1176JZF-S test chip (see *Resets* on page 3-9)
- I/O voltage translation from **3V3_VDDIO** to **ARM_VDDIO** for the Z bus signals:
 - **DEWPT**
 - **IEBKPT**
 - **USERINX[3:0]**
 - **USEROUTX[3:0]**
 - **ETMEXTIN**
 - **ETMEXTOUT**
 - **EDBGRQ**

———— **Note** ————

The application notes supplied on the CD reference included FPGA and PLD images for the current ARM supported baseboard and tile combinations.

The CT1176JZF-S PLD is controlled by the serial interface signals listed in Table 3-3. These signals connect to the baseboard via the HDRZ header.

Table 3-3 PLD control signals

Signal	Description
PLDCLK	Clocks data into or out of the PLD
PLDD1	Serial data input to PLD
PLDD0	Serial data output from PLD
PLDRESETn	Resets the serial interface and signals the start of transfers

The baseboard system FPGA implements registers that hold values sent to and received from the CT1176JZF-S PLD using the 4-wire serial interface. The baseboard system FPGA provides the baseboard serialization and deserialization logic required for the interface. The CT1176JZF-S interface timing is shown in Figure 3-10 on page 3-27.

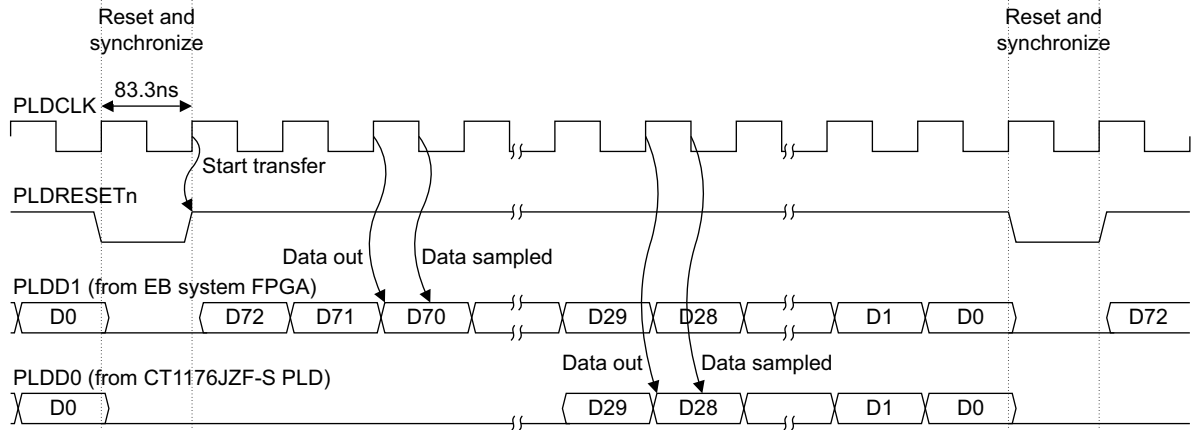


Figure 3-10 4-wire serial interface timing

Data is output on the rising edge of **PLDCLK** and sampled on the falling edge. The interface is reset and re-synchronized by **PLDRESETn** after each 73 bit serial transfer. The rising edge of **PLDRESETn** also indicates the start of a transfer. The data is transferred MSB first in both directions across the interface.

Note

The **PLDD0** serial data stream from the CT1176JZF-S PLD is only 30 bits long. Bits **PLDD0[29:0]** are used to transfer the data, **PLDD0[72:30]** are reserved and tied LOW.

The **PLDD0** output might take one cycle from initial reset to return data.

Table 3-4 on page 3-28 describes the CT1176JZF-S PLD *Serial write data register* fields and the corresponding PLD pins.

Note

Not all 73 bits in the *Serial write data register* serial data stream are used by the CT1176JZF-S, some are reserved for future use.

Table 3-4 Serial write data register

Field Name (Corresponding PLD Pins)	Serial Bits PLDD1	Reset Value	Definition
ACLKDIV (ACLKDIVX [2:0])	2:0	b000	Reserved (not used on CT1176JZF-S).
PLLREFDIV (PLLREFDIVX [3:0])	6:3	b0011	ARM1176JZF-S test chip PLL reference divider P[3:0]. Part of pre-scaler value for PLLCLK output. See <i>PLL</i> on page 4-23.
PLLFBDIV (PLLFBDIVX [11])	7	b0	Reserved (not used on CT1176JZF-S).
PLLFBDIV (PLLFBDIVX [10])	8	b0	ARM1176JZF-S test chip PLL output divider S[2]. Part of post-scaler value for PLLCLK output. See <i>PLL</i> on page 4-23.
PLLFBDIV (PLLFBDIVX [9:0])	18:9	b0010010000	ARM1176JZF-S test chip PLL feedback divider M[9:0]. See <i>PLL</i> on page 4-23.
PLLBYPASS (PLLBYPASSX)	19	b0	ARM1176JZF-S test chip PLL bypass select. See <i>PLL</i> on page 4-23.
PLLOUTDIV (PLLOUTDIVX [3:2])	21:20	b00	ARM1176JZF-S test chip PLL reference divider P[5:4]. Part of pre-scaler value for PLLCLK output. See <i>PLL</i> on page 4-23.
PLLOUTDIV (PLLOUTDIVX [1:0])	23:22	b01	ARM1176JZF-S test chip PLL output divider S[1:0]. Part of post-scaler value for PLLCLK output. See <i>PLL</i> on page 4-23.
PLLCTRL (PLLCTRLX [1:0])	25:24	b00	ARM1176JZF-S test chip PLL control. See <i>PLL</i> on page 4-23.
REMAP-init (RDATA [0])	26	b0	Reserved (not used on CT1176JZF-S).
BLKDISABL-init[7:1] (RDATA [7:1])	33:27	b00000000	Initial value for the test chip BLKDISABL register. See <i>BLKDISABL</i> on page 4-20.

Table 3-4 Serial write data register (continued)

Field Name (Corresponding PLD Pins)	Serial Bits PLDD1	Reset Value	Definition
DivCore-init[5:0] (RDATA[13:8])	39:34	b000000	Initial value for the DivCore field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.
DivInt-init[5:0] (RDATA[19:14])	45:40	b000010	Initial value for the DivInt field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.
DivExt-init[5:0] (RDATA[25:20])	51:46	b000011	Initial value for the DivExt field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.
SYNCMODEREQI/RW-init (RDATA[26])	52	b0	Initial value for the SYNCMODEREQI and SYNCMODEREQRW fields in the test chip IEMCtl-register. See <i>IEMCtl</i> on page 4-13 for details.
SYNCMODEREQD/P-init (RDATA[27])	53	b0	Initial value for the SYNCMODEREQP field in the test chip IEMCtl-register. See <i>IEMCtl</i> on page 4-13 for details.
AMBAClkSource-init (RDATA[28])	54	b0	Initial value for the AMBAClkSource field in the test chip ClkCtl register and the ACLKSource field in the test chip ClkEnCtl register. See <i>ClkCtl</i> on page 4-28 and <i>ClkEnCtl</i> on page 4-30.
TRUSTZONESD-init (RDATA[29])	55	b0	Initial value for the TRUSTZONESD field in the test chip register.
TRUSTZONENSA-init (RDATA[30])	56	b1	Initial value for the TRUSTZONENSA field in the test chip register.
AXIrandom-init (RDATA[31])	57	b0	Reserved (set to zero).
UBITINIT (UBITINITX)	58	b0	Initial value of the ARM1176JZF-S UBIT.
VINITHI (VINITHIX)	59	b0	Location of exception vectors at reset. When HIGH: Indicates High Vecs mode.
INITRAM (INITRAMX)	60	b0	Enables the ARM1176JZF-S test chip internal RAM at reset.

Table 3-4 Serial write data register (continued)

Field Name (Corresponding PLD Pins)	Serial Bits PLDD1	Reset Value	Definition
BIGENDIN (BIGENDINX)	61	b0	Selects big endian mode for the ARM1176JZF-S test chip.
DBGEN (DBGENX)	62	b1	Debug enable - synchronous. When DBGEN is LOW the ARM1176JZF-S processor behaves as if in debug disabled mode. To enable ARM1176JZF-S debug, program the DBGEN bit HIGH in the Serial Write Data stream.
DACDAT[7:0] (DAC_DIN)	70:63	0x80	DAC 8-bit data. Sets the VDDCORE1 or VDDCORE2 voltage by controlling the DAC0 or DAC1 output current dependant on the value of DACSEL.
DACSEL (DAC_nCS[1:0])	71	b0	Selects either the VDDCORE1 or the VDDCORE2 voltage control DAC to receive data by setting DAC_nCS[0] or DAC_nCS[1] LOW. When DACSEL is LOW: VDDCORE2 DAC1 output current is set by DACDA[7:0]. When DACSEL is HIGH: VDDCORE1 DAC0 output current is set by DACDA[7:0].
CLKSEL (CLKSEL)	72	b0	Controls the input clock multiplexer. This multiplexer selects the REFCLK source for the CT1176JZF-S. When CLKSEL is LOW: CLK_NEG_UP_OUT from the board below is selected as the clock source. When CLKSEL is HIGH: CLK_NEG_DN_IN from the board above is selected as the clock source.

Table 3-5 on page 3-31 describes the *Serial read data register* of the CT1176JZF-S PLD and the corresponding PLD pins.

———— **Note** ————

There are a total of 30 bits used in the *Serial read data register* data stream.

Register contents is undefined at reset.

Table 3-5 Read serial data register

Field Name (Corresponding PLD Pins)	Serial Bits PLDD0	Definition
PLLLOCK (PLLLOCKX , ISPnLOCK)	0	<p>CT1176JZF-S stable clocks indicator. When PLLLOCK is HIGH:</p> <ul style="list-style-type: none"> ARM1176JZF-S test chip PLL is locked to REFCLK CT1176JZF-S ispClock5620 PLL is locked to ACLKX. <p>See <i>Clock setting in reset mode</i> on page 3-7.</p>
ARM_PLLLOCKX (PLLLOCKX)	1	<p>When ARM_PLLLOCKX is HIGH: ARM1176JZF-S test chip PLL is locked to REFCLK.</p> <p>See <i>Clock setting in reset mode</i> on page 3-7.</p>
ISPnLOCK (ISPnLOCK)	2	<p>When ISPnLOCK is LOW: CT1176JZF-S ispClock5620 PLL is locked to ACLKX.</p> <p>See <i>Clock setting in reset mode</i> on page 3-7.</p>
ADCDAT[11:0] (ADC_nCS , ADC_DIN , ADC_CLK , ADC_SSTRB , ADC_DOUT)	14:3	<p>Power sensing 12-bit ADC interface. ADC supply voltage measurement from channels 0 to 7. Current channel is indicated by ADCSEL.</p> <p>See <i>Reading the voltages and currents</i> on page 3-19.</p>
ADCSEL[2:0] (ADC_nCS , ADC_DIN , ADC_CLK , ADC_SSTRB , ADC_DOUT)	17:15	<p>Indicates the ADC channel currently being converted:</p> <p>b000 = channel 0 – VDDCORE1 voltage b001 = channel 2 – VDDCORE_TC current b010 = channel 4 – VDDCORE_ARM current b011 = channel 6 – PLLVDD10 current b100 = channel 1 – VDDCORE2 voltage b101 = channel 3 – VDDCORE_ETM current b110 = channel 5 – ARM_VDDIO voltage b111 = channel 7 – PLLVDD25 current</p> <p>See <i>Reading the voltages and currents</i> on page 3-19.</p>
PLDVER	21:18	PLD build version.
BUILDID	29:22	Build variant.

3.7.2 ARM1176JZF-S test chip configuration

The CT1176JZF-S PLD configures the ARM1176JZF-S test chip PLL and the Config-init register during reset.

Caution

During normal operation, the test chip PLL and Config-init register configuration values are continually sent from the baseboard via the 4-wire serial interface. ARM recommend that the PLL configuration values sent are only changed when the CT1176JZF-S is in reset.

The CT1176JZF-S reset signals involved in ARM1176JZF-S test chip configuration are:

nSYSPOR	Power-on reset.
nCOLDRST	Full software reset.
nWARMRST	System reset.

See *Reset signals* on page 3-13 for details.

Note

The baseboard determines the conditions under which a **nCOLDRST** or **nWARMRST** are issued. See *Application Note AN158 (ARM DAI 0158)* supplied on the Versatile CD for details on how these resets are controlled by the system FPGA on the EB.

PLL configuration

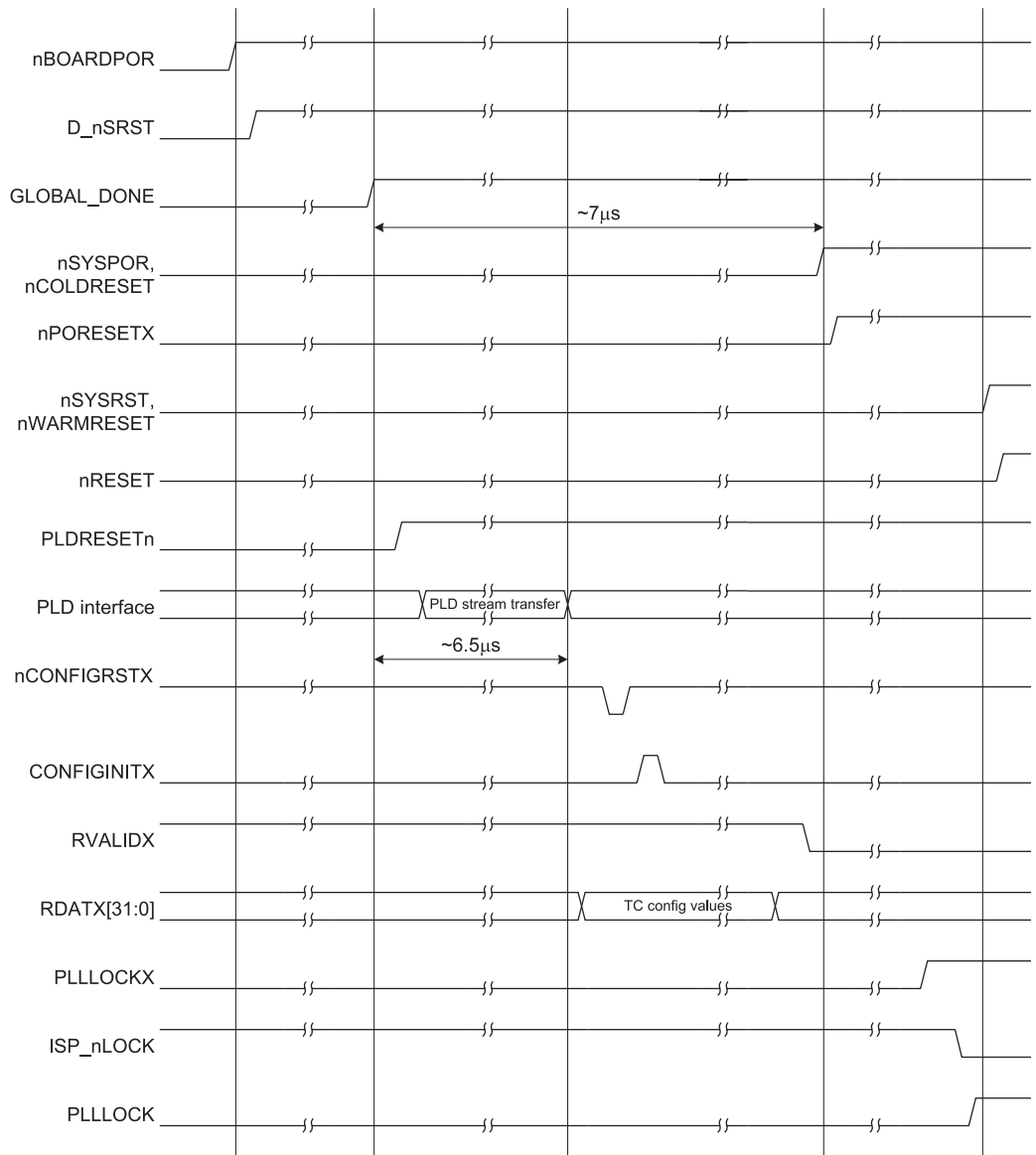
The ARM1176JZF-S test chip PLL is configured during:

- a power-on reset (**nSYSPOR**)
- a full software reset (**nCOLDRST**)
- a system reset (**nWARMRST**).

Config-init register configuration

The ARM1176JZF-S test chip Config-init register is configured during:

- a power-on reset (**nSYSPOR**)
- a full software reset (**nCOLDRST**).

Figure 3-11 shows the initialization timing during a power-on reset (**nSYSPOR**),**Figure 3-11 Configuration timing – power-on reset**

The initialization steps during a power-on reset are:

1. Baseboard system FPGA applies the resets **nSYSPOR**, **nCOLDRESET**, **nSYSRST**, **nWARMRESET** and **PLDRESETn** to the CT1176JZF-S.
2. CT1176JZF-S PLD generates **nPORESETX** and **nRESETX** to the ARM1176JZF-S test chip in response to **nCOLDRST** and **nWARMRST** respectively.
3. Baseboard FPGA waits for **GLOBAL_DONE**.
4. **GLOBAL_DONE** goes HIGH indicating that all system FPGAs have been configured.
5. Baseboard system FPGA generates **PLDRESETn** and starts sending the PLD stream with the initial values for PLL control and the ARM1176JZF-S Config-init register.
6. After the PLD stream is sent the CT1176JZF-S PLD sets up the PLL value directly on the ARM1176JZF-S test chip pins and the Config-init register values are placed on the **RDATAx[31:0]** bus.
7. CT1176JZF-S PLD generates the **nCONFIGRSTX** and **CONFIGINITX** sequence to load the Config-init register.
8. If **nCOLDRST** is HIGH the CT1176JZF-S PLD sets **nPORESETX** to the ARM1176JZF-S test chip HIGH.
9. Baseboard waits until PLLLOCK (transmitted from the CT1176JZF-S PLD by the PLD stream) is HIGH and then releases **nWARMRST**.
10. **nWARMRST** is released and the CT1176JZF-S PLD releases **nRESETX** to the ARM1176JZF-S test chip.

Figure 3-12 on page 3-35 shows the configuration timing during a full software reset (**nCOLDRST**).

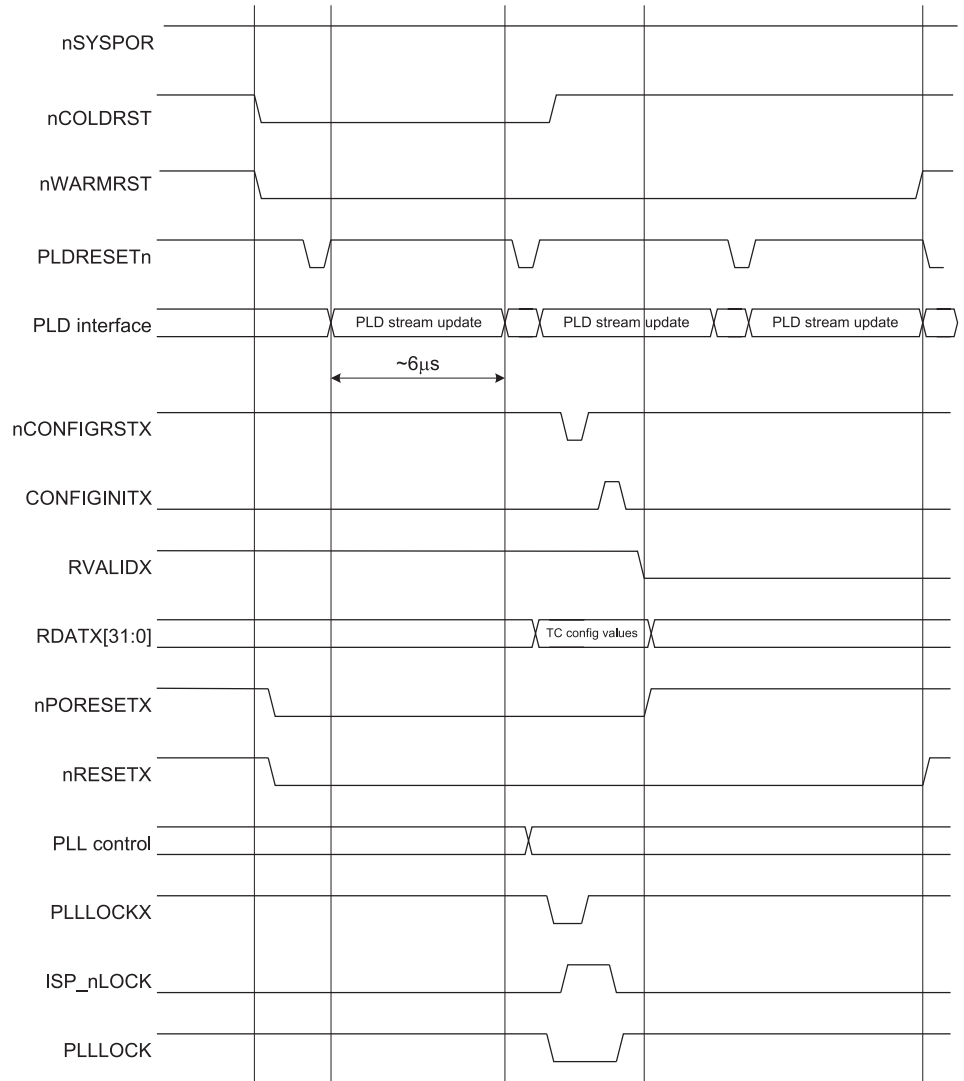


Figure 3-12 Configuration timing – full software reset

The configuration steps during a full software reset are:

1. Baseboard system FPGA generates **nCOLDRST** and **nWARMRST**.
2. CT1176JZF-S PLD generates **nPORESETX** and **nRESETX** to the ARM1176JZF-S test chip in response to **nCOLDRST** and **nWARMRST** respectively.

3. Baseboard system FPGA generates **PLDRESETn** and starts sending the PLD stream with the new values for PLL control and the Config-init register.
4. After the PLD stream is sent the CT1176JZF-S PLD sets up the new PLL value directly on the ARM1176JZF-S test chip pins and the Config-init register values are placed on the **RDATAx[31:0]** bus.
5. CT1176JZF-S PLD generates the **nCONFIGRSTx** and **CONFIGINITx** sequence to load the Config-init register.
6. If **nCOLDRST** is HIGH the CT1176JZF-S PLD sets **nPORESETx** to the ARM1176JZF-S test chip HIGH.
7. Baseboard waits until PLLLOCK (transmitted from the CT1176JZF-S PLD by the PLD stream) is HIGH and then releases **nWARMRST**.
8. **nWARMRST** is released and the CT1176JZF-S PLD releases **nRESETx** to the ARM1176JZF-S test chip.

Figure 3-13 on page 3-37 shows the configuration timing during a system reset (**nWARMRST**).

———— **Note** ————

A system reset (**nWARMRST**) enables reprogramming of the ARM1176JZF-S test chip PLL without reinitializing the ARM1176JZF-S test chip configuration registers.

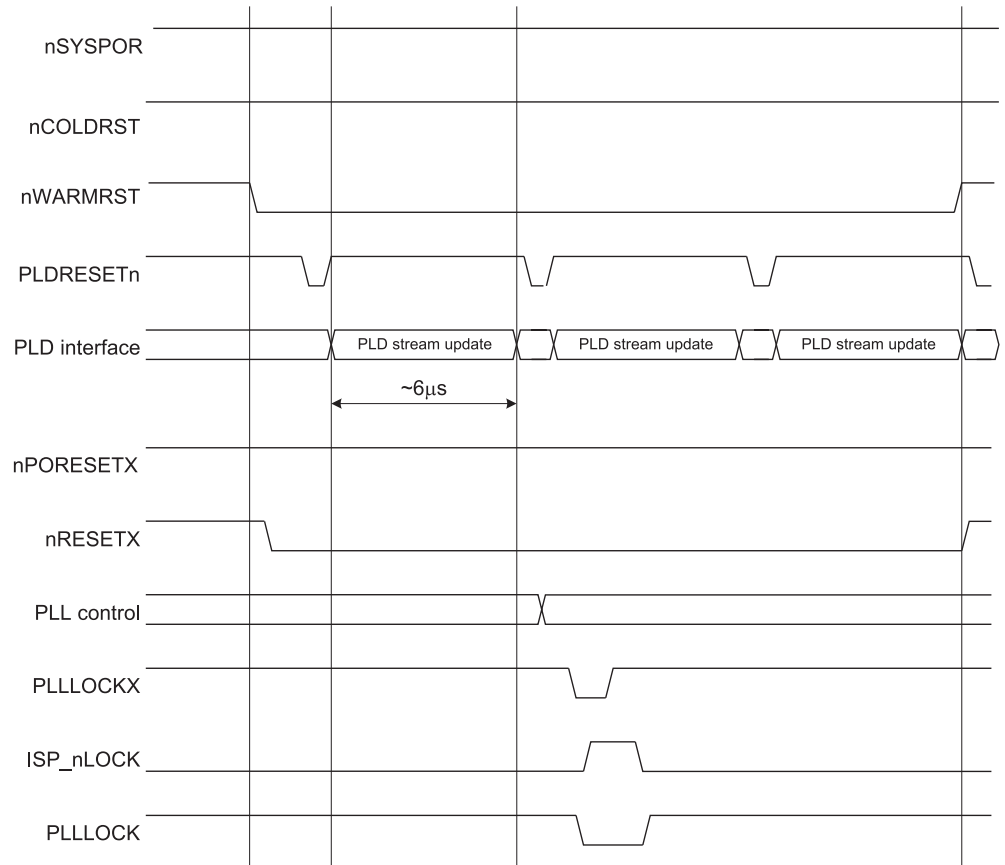


Figure 3-13 Configuration timing – system reset

The configuration steps during a system reset are:

1. Baseboard system FPGA generates a **nWARMRST**.
2. CT1176JZF-S PLD generates **nRESETX** to the ARM1176JZF-S test chip in response to **nWARMRST**.
3. Baseboard system FPGA generates **PLDRESETn** and starts sending the PLD stream with new values for PLL control.
4. After the PLD stream is sent the CT1176JZF-S PLD sets up the new PLL value directly on the ARM1176JZF-S test chip pins.
5. Baseboard waits until **PLLLOCK** (transmitted from the CT1176JZF-S PLD by the PLD stream) is HIGH and then releases **nWARMRST**.

6. **nWARMRST** is released and the CT1176JZF-S PLD releases **nRESETX** to the ARM1176JZF-S test chip.

3.7.3 Core configuration from ARM CP15

The purpose of the system control coprocessor, CP15, is to control and provide status information for the functions implemented in the ARM1176JZF-S processor.

The main functions controlled by CP15 are:

- overall system control and configuration of the ARM1176JZF-S
- optional cache configuration and management
- optional Tightly-Coupled Memory (TCM) configuration and management
- optional Memory Management Unit (MMU) configuration and management
- debug accesses to the caches
- system performance monitoring.

See the *ARM1176JZF-S Processor Technical Reference Manual* (ARM DDI 0301) for details on the CP15 registers.

3.7.4 TrustZone configuration

The ARM1176JZF-S processor supports TrustZone security extensions to provide a secure environment for software.

The CT1176JZF-S provides the necessary signals and controls to enable:

- peripherals within the ARM1176JZF-S test chip to function as secure peripherals
- secure peripherals to be added to the baseboard providing the correct TrustZone modules are also implemented
- secure debug support.

ARM1176JZF-S test chip peripheral control

The TRUSTZONENSA and TRUSTZONESD registers in the test chip determine the security policy that is applied to accesses to individual peripherals in the test chip. See *TrustZone security control* on page 4-9 for details. The initial register values are set as a group during CT1176JZF-S configuration by writing values via the *Serial write data*

register to the Config-init register. See *Config-init register* on page 4-32 for details. The default security policy set by *Application Note* AN177 is for both secure and non-secure access to all test chip peripherals.

AXI signals

The AXI bus connected through header HDRX is a full AXI bus implementation and includes the **ARPROTX[1]** and **AWPROTX[1]** TrustZone signals from the ARM1176JZF-S test chip. See the *AMBA 3 AXI Protocol Specification* (ARM IHI 002) for details. These signals when LOW indicate a secure access and when HIGH indicate a non-secure access. This allows secure peripherals to be added to a baseboard providing the correct TrustZone modules are also implemented.

Secure debug support

To support Secure debug, access is provided to two enable signals from the ARM1176JZF-S processor:

SPIDENX Secure Privilege Intrusive Debug enable.

SPNIDENX Secure Privilege Non-intrusive Debug enable.

SPIDENX is controlled by pin **USERINX2** on the ARM1176JZF-S test chip and **SPNIDENX** is controlled by pin **USERINX3**. These signals are passed through the PLD unchanged and are connected to the HDRZ header as **USERIN2** and **USERIN3** respectively. See *HDRZ signals* on page 5-14 for details.

Note

When used with an EB system running *Application Note* AN177, **SPIDEN** is controlled by User switch 7 on the EB and **SPNIDEN** is controlled by User switch 8. See AN177 for details.

3.8 Memory configuration

The memory subsystems implemented by the ARM1176JZF-S test chip are:

ARM1176JZF-S Level 1 (L1)

- 16KB of instruction cache
- 16KB of data cache
- 16KB of instruction TCM
- 16KB of data TCM.

AXI memory sub-system Level 3 (L3)

Two 64KB interleaved memory blocks are provided for local data and instruction storage. Memory can be clocked at the same frequency as the processor or at a synchronous lower frequency.

AHB Exclusive Access memory sub-system Level 3 (L3)

A 16KB memory block is provided at Master Interface 2 (M2) of the AXI interconnect to enable testing of Exclusive Access memory. It is connected via an AXI to AHB bridge (AXI2AHB) and Exclusive Access Monitor block (ExAcMn64). The memory block is provided to test *Exclusive Memory Access* LDREX and STREX processor instructions. The memory is byte writable SRAM, implemented as two blocks of 2048x32. See *ARM1176JZF-S test chip overview* on page 4-2 for further details of the test chip AXI interconnect.

There is no provision for PISMO Expansion Memory Modules on the CT1176JZF-S. Main system *Level 3* (L3) memory should be located on the baseboard. If additional L3 memory is required, you can add PISMO Expansion Memory Modules to a baseboard such as the EB. Additional L3 memory may also be made available via the EB second tile site, see *Realview Emulation Baseboard User Guide* (ARM DUI 0303) for system memory details.

For details of the memory map implemented in the ARM1176JZF-S test chip see *Memory map* on page 4-6.

For general information about the L1 and L3 memory subsystems see the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301).

3.9 Register configuration

This section describes the CT1176JZF-S specific registers and contains the following subsections:

- *ARM1176JZF-S test chip registers*
- *CT1176JZF-S serial registers*
- *Baseboard system FPGA registers* on page 3-42

3.9.1 ARM1176JZF-S test chip registers

The ARM1176JZF-S test chip peripheral space is distributed across the 32-bit processor address space (0x00000000 to 0xFFFFFFFF). Peripherals are aliased throughout their allocated address range. Three areas are reserved for external AXI port accesses. In addition, if a peripheral is disabled by writing to the ARM1176JZF-S test chip BLKDISABL register, accesses to the disabled peripheral are redirected to the external AXI interface. See *Memory map* on page 4-6 for details of a peripheral's base address and register offset values.

Caution

When you access the ARM1176JZF-S test chip peripheral space, you must use single accesses of 32-bit aligned type, otherwise an abort, due to slave error, is generated.

3.9.2 CT1176JZF-S serial registers

The CT1176JZF-S PLD implements two registers, the *Serial write data register* and the *Serial read data register*. These registers mirror the content of CT1176JZF-S specific registers implemented in the baseboard system FPGA. The registers are continually updated via a 4-wire serial link to ensure that the content of the CT1176JZF-S and baseboard registers remains coherent.

The bit allocations for the *Serial write data register* are shown in *Serial write data register* on page 3-28. The bit allocations for the *Serial read data register* are shown in *Read serial data register* on page 3-31.

Note

The *Serial write data register* and the *Serial read data register* are only accessible via the 4-wire serial link. Changing or reading the contents of these registers is only possible by using Core Tile specific registers implemented in the baseboard system FPGA. Not all fields in the *Serial write data register* are user configurable, some are pre-configured by the baseboard system FPGA.

3.9.3 Baseboard system FPGA registers

A baseboard configures and reads the status of a Core Tile using system registers implemented in the baseboard FPGA. The baseboard communicates with the Core Tile using a 4-wire serial interface. See *Serial write data register* on page 3-28 and *Read serial data register* on page 3-31 for details of the CT1176JZF-S serial registers.

The system registers implemented in the baseboard FPGA are specific to the combination of baseboard and Core Tile used and are described in a separate *Application Note* supplied on the CD that accompanied the product.

Application Notes are also available from the ARM website at:
www.arm.com/documentation/Application_Notes/index.html.

The 4-wire write serial interface transfers:

ARM1176JZF-S test chip initialization values

These fields in the serial stream initialize the ARM1176JZF-S test chip:

————— **Note** —————

These values are only written to the ARM1176JZF-S test chip during power-on reset (**nSYSPOR**) or a system reset (**nCOLDRESET**).

- REMAP-init
- BLKDISABLE-init[7:1]
- DivCore-init[5:0]
- DivInt-init[5:0]
- DivExt-init[5:0]
- SYNCMODEREQI/RW-init
- SYNCMODEREQD/P-init
- AMBAClkSource-init
- TRUSTZONESD-init
- TRUSTZONENSA-init
- AXIrandom-init (reserved – set to zero)

The ARM1176JZF-S test chip initialization fields are described in *Serial write data register* on page 3-28.

ARM1176JZF-S test chip configuration values

These fields in the serial stream allow configuration of the CT1176JZF-S:

- ACLKDIV
- PLLREFDIV
- PLLFBDIV
- PLLBYPASS
- PLLOUTDIV
- PLLCTRL
- UBITINIT
- VINITHI
- INITRAM
- BIGENDIN
- DBGGEN
- DACDA
- DACSEL
- CLKSEL

The CT1176JZF-S configuration fields are described in *Serial write data register* on page 3-28.

The 4-wire read serial interface transfers:

CT1176JZF-S status values These fields in the serial stream allow status monitoring of the CT1176JZF-S:

- PLLLOCK
- ARM_PLLLOCKX
- ISPnLOCK
- ADCDAT
- ADCSEL
- PLDVER
- BUILDID

The CT1176JZF-S status monitoring fields are described in *Read serial data register* on page 3-31.

3.10 JTAG support

JTAG signals are present on both the upper and lower HDRZ connectors. An external board provides the JTAG connector and the routing of the JTAG signals from the connector to HDRZ (see *JTAG control and clock routing* on page 3-48). The Core Tile routes the JTAG scan path through devices on the board. The logic devices that are placed in the Core Tile scan chain depend on the JTAG mode:

Debug mode Debug mode is the default mode used for general system development and debug. In this mode, the JTAG signals flow through the Debug Scan Chain (this scan chain connects to the ARM1176JZF-S test chip only). The JTAG signals used for debug are identified by the **D_** prefix.

Note

Common access to the ARM1176JZF-S DBGTAP controllers is available in this mode. See *Debug* on page 4-38.

Configuration mode

In configuration mode the PLD, clock generator, and the ARM1176JZF-S test chip are placed into the scan chain. This mode allows the programmable logic devices in the system to be reprogrammed and the ARM1176JZF-S test chip registers to be configured.

To select configuration mode, the baseboard pulls the **nCFGEN** signal LOW on the Core Tile. This reroutes the JTAG scan path. The JTAG signals used for configuration are identified by the **C_** prefix.

Note

Access to the ARM1176JZF-S test chip boundary scan TAP controller is available in this mode. See *JTAG Configuration* on page 4-38.

Table 3-6 on page 3-45 provides a description of the JTAG signals.

Note

In the description in Table 3-6 on page 3-45, the term JTAG equipment refers to any hardware that can drive the JTAG signals to devices in the scan-chain. Typically, RealView ICE is used, although you can also use hardware from third-party suppliers to debug ARM processors.

Table 3-6 JTAG signal description

Name	Description	Function
nBSTAPEN	Boundary scan TAP enable	<p>In configuration mode, the boundary scan TAP logic in a test chip is enabled.</p> <p>———— Note ————</p> <p>nBSTAPEN drives the nBSTAPENX control pin on the ARM1176JZF-S test chip. In JTAG configuration mode, nBSTAPEN is LOW and the ARM1176JZF-S test chip TAP controller is enabled. In JTAG debug mode, nBSTAPEN is HIGH and the DBG TAP controller in the ARM1176JZF-S is enabled.</p>
EDBGRQ	Debug request	<p>EDBGRQ is a request to the ARM1176JZF-S to enter the debug state.</p> <p>———— Note ————</p> <p>EDBGRQ is routed to the HDRZ header for optional use in custom designs. It is tied LOW in Application Note AN177 <i>Using a CT1176JZF-S with the RealView Emulation Baseboard</i>.</p>
DBGACK	Debug acknowledge	<p>DBGACK indicates that the ARM1176JZF-S has entered debug state.</p> <p>———— Note ————</p> <p>DBGACK is routed to the HDRZ header for optional use in custom designs. It is not used in Application Note AN177 <i>Using a CT1176JZF-S with the RealView Emulation Baseboard</i>.</p>
nCFGEN	Configuration enable (controlled by config slide-switch on the EB)	nCFGEN is an active LOW signal used to put all boards in the tile stack into configuration mode. In configuration mode all FPGAs and PLDs are connected to the scan chain so that they can be configured by the JTAG equipment.
nRTCKEN	Return TCK enable (from Core Tile to EB)	nRTCKEN is an active LOW signal driven by any Core Tile that requires RTCK to be routed back to the JTAG equipment. If nRTCKEN is HIGH, the baseboard drives RTCK LOW. If nRTCKEN is LOW, the baseboard drives the TCK signal back up the stack to the JTAG equipment.

Table 3-6 JTAG signal description (continued)

Name	Description	Function
nTRST , D_nTRST , C_nTRST	Test reset (from JTAG equipment)	<p>This active LOW open-collector signal is used to reset the JTAG port and the associated debug circuitry on the test chip. It is asserted at power-up by each module, and can be driven by the JTAG equipment.</p> <p>D_nTRST is the reset for the debug mode scan chain and C_nTRST is the reset for the configuration mode scan chain.</p> <p>———— Note —————</p> <p>D_nTRST is always tied to D_nSRST. C_nTRST is tied to D_nTRST when configuration mode is enabled.</p>
nSRST , D_nSRST , C_nSRST		<p>This active LOW open-collector signal can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when a board has been reset by the user.</p> <p>Though not a JTAG signal, nSRST is described because it can be controlled by JTAG equipment.</p> <p>D_nSRST is the reset for the debug mode scan chain and C_nSRST is the reset for the configuration mode scan chain.</p> <p>———— Note —————</p> <p>Only D_nSRST is utilized by the CT1176JZF-S.</p>
RTCK , D_RTCK	Return TCK (to JTAG equipment)	<p>Some devices sample TCK (for example a synthesizable core with only one clock), and this has the effect of delaying the time when a component actually captures data. RTCK is a mechanism for returning the sampled clock to the JTAG equipment, so that the clock is not advanced until the synchronizing device has captured the data. In a multiple device JTAG chain, the D_RTCK output from a component connects to the TCK input of the down-stream device. The RTCK signal on the EB connector HDRZ returns TCK to the JTAG equipment.</p> <p>D_RTCK is the RTCK signal in the debug scan chain. RTCK is not available in the configuration mode scan chain.</p>

Table 3-6 JTAG signal description (continued)

Name	Description	Function
TCK, D_TCK, C_TCK	Test clock (from JTAG equipment)	<p>TCK synchronizes all JTAG transactions. TCK connects to all JTAG components in the scan chain. Series termination resistors are used to reduce reflections and maintain good signal integrity. TCK flows up the stack of modules and connects to each JTAG component. However, if there is a device in the scan chain that synchronizes TCK to some other clock, then all down-stream devices are connected to the RTCK signal on that component (see RTCK).</p> <p>D_TCK is the clock for the debug mode scan chain and C_TCK is the clock for the configuration mode scan chain.</p>
TDI, D_TDI, C_TDI	Test data in (from JTAG equipment)	<p>TDI goes up the stack of tiles from the baseboard (or Interface Module) and then back down the stack (as TDO) connecting to each component in the scan chain.</p> <p>D_TDI is the data signal for the debug mode scan chain and C_TDI is the data signal for the configuration mode scan chain.</p>
TDO, D_TDO, C_TDO	Test data out (to JTAG equipment)	<p>TDO is the return path of the data input signal TDI. For a stack of RealView products, TDI goes up to the top of the stack and returns down as TDO. The JTAG components are connected in the return path so that the length of track driven by the last component in the chain is kept as short as possible.</p> <p>D_TDO is the data signal for the debug mode scan chain and C_TDO is the data signal for the configuration mode scan chain.</p>
TMS, D_TMS, C_TMS	Test mode select (from JTAG equipment)	<p>TMS controls transitions in the tap controller state machine. TMS connects to all JTAG components in the scan chain.</p> <p>D_TMS is the control signal for the debug mode scan chain and C_TMS is the control signal for the configuration mode scan chain.</p>

3.10.1 JTAG control and clock routing

Figure 3-14 shows the JTAG *Debug Mode* routing of the **D_nTRST**, **D_TCK**, and **D_TMS** signals to the ARM1176JZF-S test chip. The bus switches, unless otherwise indicated, are controlled by **nCFGEN** from the baseboard. JTAG debug mode routing is selected when **nCFGEN** is HIGH. This is the default baseboard setting.

Note

At power-up, the baseboard **nSYSPOR** power-on-reset signal initializes the boundary scan tap controller and the DBGTAP controller in the ARM1176JZF-S test chip by forcing **ARM_nTRST** LOW.

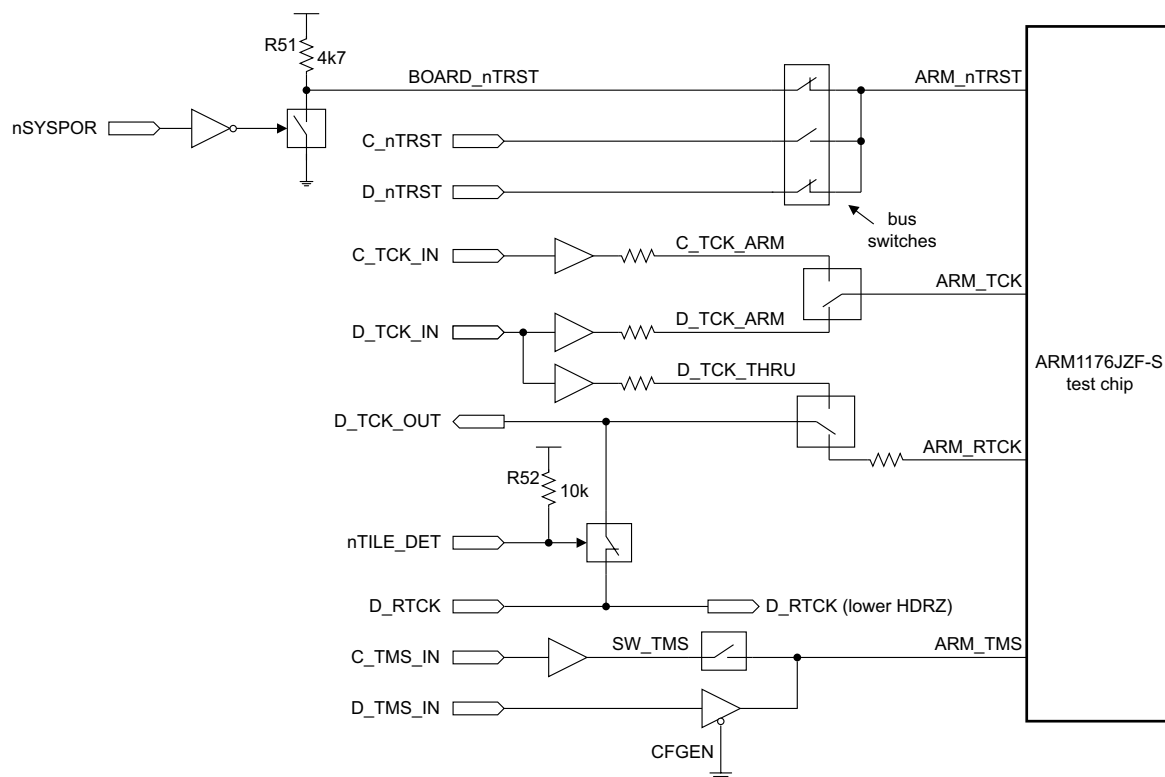


Figure 3-14 JTAG debug mode routing (nCFGEN=1)

The JTAG input and output routing shown in Figure 3-14 on page 3-48 is for a single tile. In this case, no tile is connected to the upper HDRZ header and **D_TCK_OUT**, and **D_RTCK** from the upper HDRZ header, are not used. For details on JTAG input and output routing in a tile stack, see *JTAG loopback control* on page 3-53. JTAG loopback routing is controlled by **nTILE_DET**.

Figure 3-15 shows the JTAG *Configuration Mode* routing of the **C_nTRST**, **C_TCK**, and **C_TMS** signals to the ARM1176JZF-S test chip. The bus switches, unless otherwise indicated, are controlled by **nCFGEN** from the baseboard. JTAG configuration mode routing is selected when **nCFGEN** is LOW.

Note

To select JTAG configuration mode, pull the **nCFGEN** signal LOW on the CT1176JZF-S to reroute the JTAG scan path.

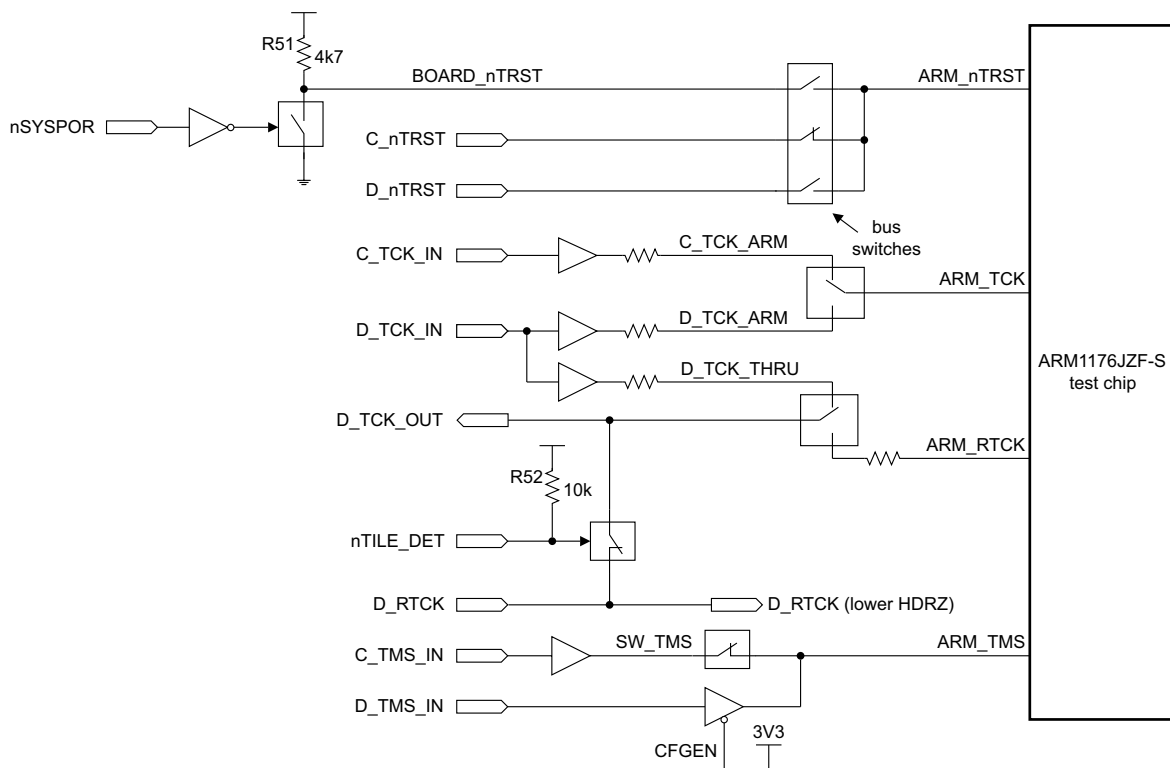


Figure 3-15 JTAG configuration mode routing (**nCFGEN**=0)

The Core Tile JTAG input and output routing shown in Figure 3-15 on page 3-49 is for a single tile. In this case, no tile is connected to the upper HDRZ header and **D_TCK_OUT**, and **D_RTCK** from the upper HDRZ header, are not used. For details on Core Tile JTAG input and output routing in a tile stack, see *JTAG loopback control* on page 3-53. JTAG loopback routing is controlled by **nTILE_DET**.

———— **Note** ————

The ispClock generator does not have a **nTRST** pin. The TAP controller is reset by keeping **TMS** HIGH, this forces its TAP controller into the *Test-Logic-Reset* steady state within 5 **TCK** cycles. *Test-Logic-Reset* is also the power-on default state.

Figure 3-16 shows the distribution of the critical **C_TCK** and **C_TMS** signals to the remaining JTAG configurable devices on the CT1176JZF-S. Buffered versions of the signals, **C_TCK_OUT** and **C_TMS_OUT** are provided at the upper HDRZ header to drive the **C_TCK** and **C_TMS** inputs of the next tile in a tile stack.

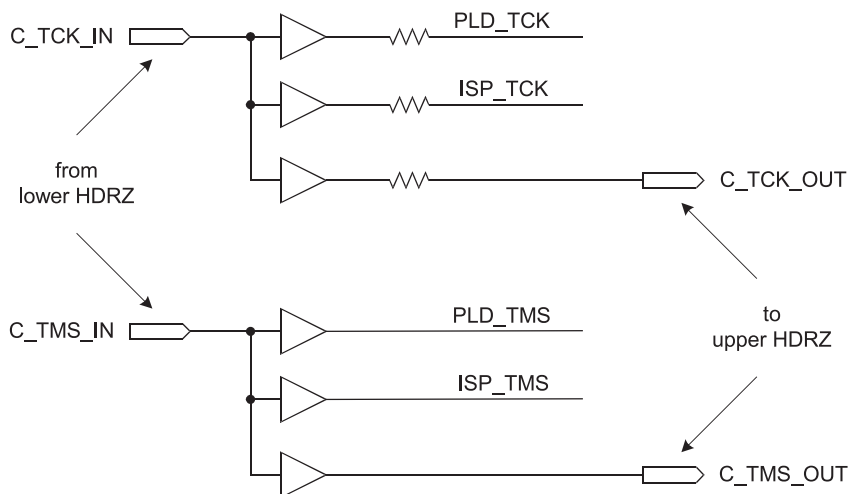


Figure 3-16 Additional JTAG configuration mode routing

3.10.2 JTAG debug mode scan chain routing

Figure 3-17 shows the JTAG *Debug Mode* scan chain routing.

In JTAG debug (normal) mode the ARM1176JZF-S test chip is connected in the debug scan chain. The bus switches, unless otherwise indicated, are controlled by **nCFGEN** from the baseboard. JTAG debug mode routing is selected when **nCFGEN** is **HIGH**. This is the default baseboard setting.

The JTAG input and output routing shown in Figure 3-17 is for a single tile. In this case, no tile is connected to the upper HDRZ header and **D_TDO_IN** and **C_TDO_IN** are not used. For details on JTAG input and output routing in a tile stack, see *JTAG loopback control* on page 3-53. JTAG loopback routing is controlled by **nTILE_DET**.

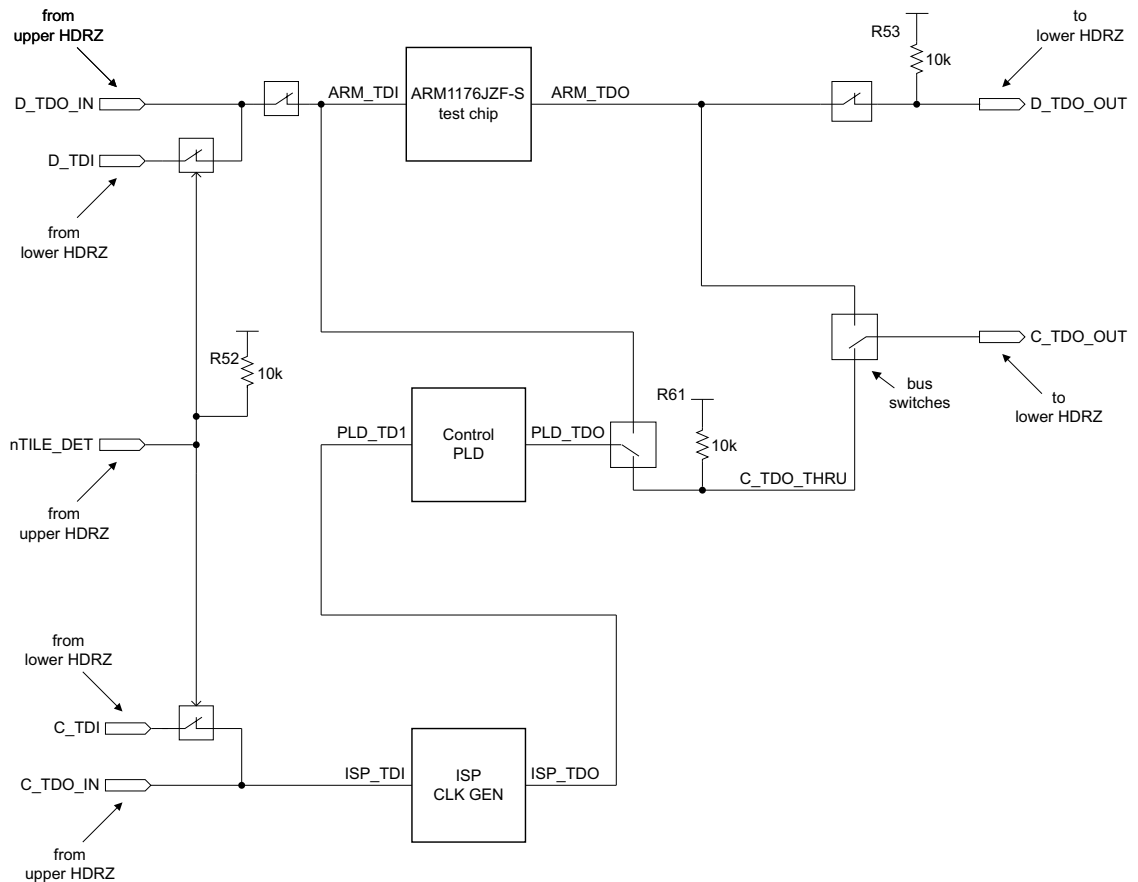


Figure 3-17 JTAG debug (normal) mode scan chain routing (nCFGEN=1)

3.10.3 JTAG configuration mode scan chain routing

Figure 3-18 shows the JTAG *Configuration Mode* routing.

In JTAG configuration mode all the JTAG configurable devices (ISP clock generator, PLD, and ARM1176JZF-S test chip) are connected in the configuration scan chain. The bus switches are controlled by **nCFGEN** from the baseboard. JTAG configuration mode routing is selected when **nCFGEN** is LOW.

The JTAG input and output routing shown in Figure 3-18 is for a single tile. In this case, no tile is connected to the upper HDRZ header and **D_TDO_IN** and **C_TDO_IN** are not used. For details on JTAG input and output routing in a tile stack, see *JTAG loopback control* on page 3-53. JTAG loopback routing is controlled by **nTILE_DET**.

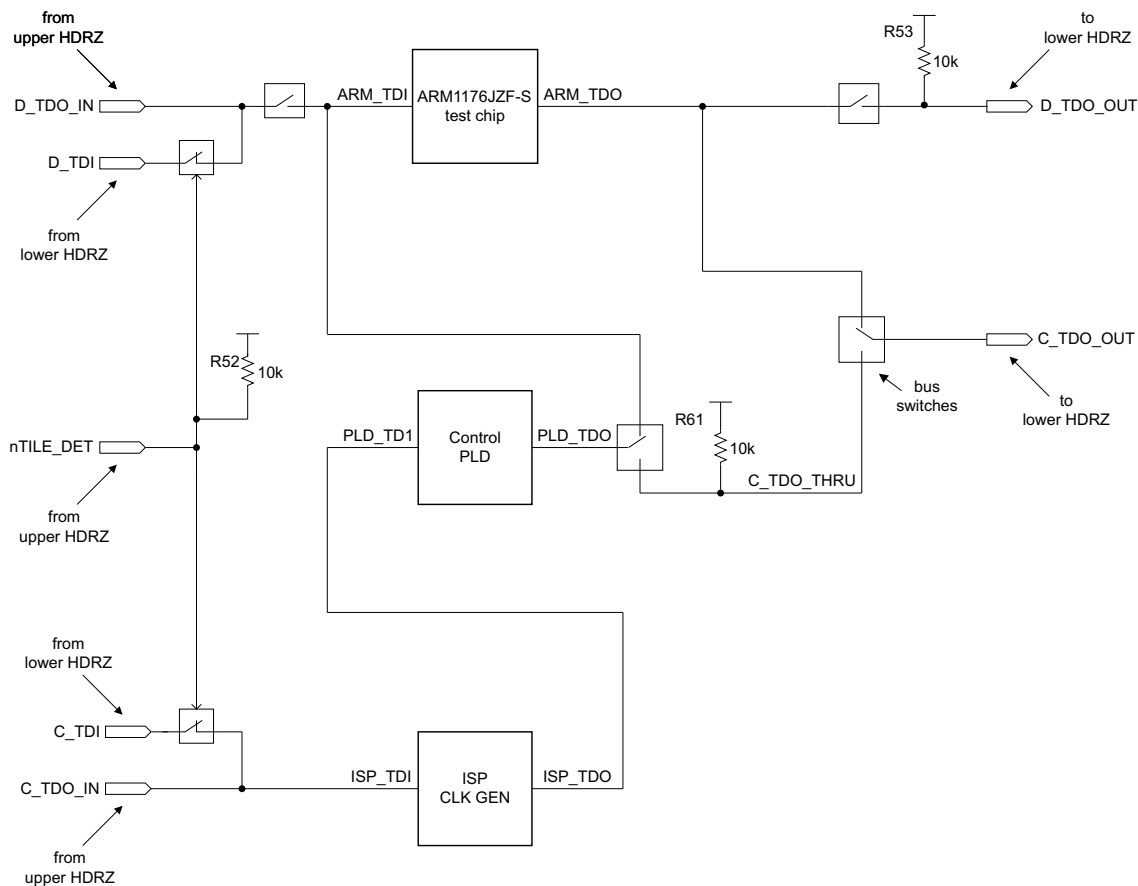


Figure 3-18 JTAG configuration mode scan chain (nCFGEN=0)

3.10.4 JTAG loopback control

A number of tiles may be stacked above the baseboard. Figure 3-19 shows the TDI, TDO, and RTCK loopback control for a multi-tile stack. The JTAG debug and configuration TDI signals from the baseboard, **D_TDI** and **C_TDI** are made available to every tile in the stack by feeding through from the lower to the upper header HDRZ on each tile. The bus switches are controlled by **nTILE_DET**. If a tile is the top tile in the stack **nTILE_DET** remains pulled HIGH. **C_TDI** and **D_TDI** loopback is then achieved by the bus switches connecting this last tile in the stack to the **C_TDI** and **D_TDI** signals. For tiles further down the stack **nTILE_DET** is pulled LOW by the tile above and these tiles connect to the **C_TDO_OUT** and **D_TDO_OUT** signals from the tile above.

D_RTCK is made available from every tile in the stack by feeding through from the upper to the lower header HDRZ on each tile. The bus switches are controlled by **nTILE_DET**. If a tile is the top tile in the stack **nTILE_DET** remains pulled HIGH. **D_RTCK** loopback is then achieved by the bus switches connecting **D_TCK_OUT** from this last tile in the stack to **D_RTCK**. For tiles further down the stack **nTILE_DET** is pulled LOW by the tile above and these tiles connect to the **D_TCK_OUT** signal from the tile below.

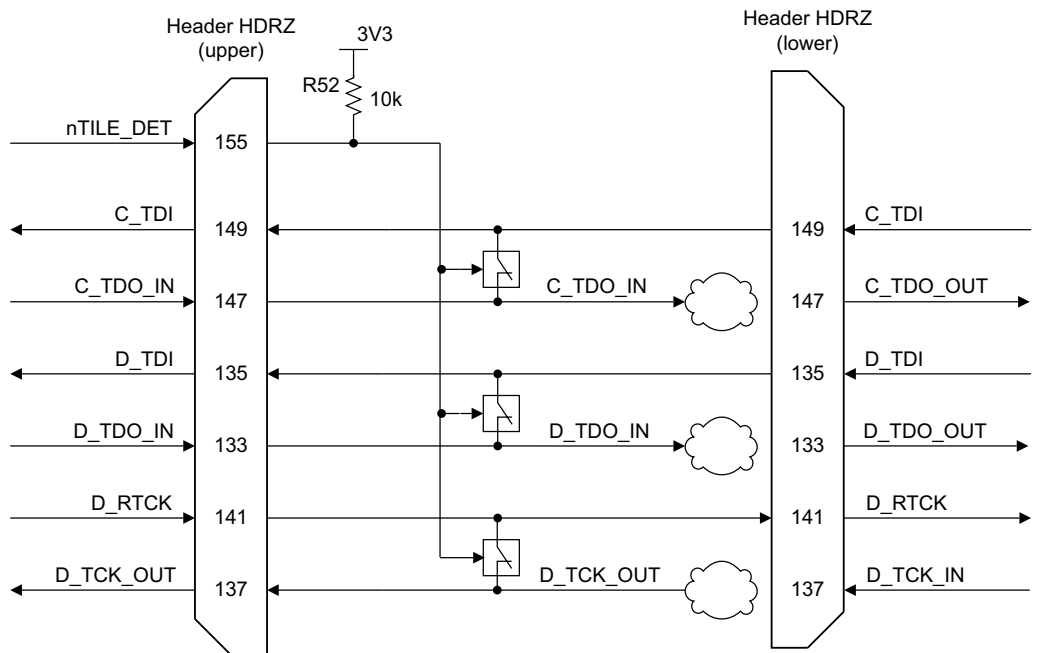


Figure 3-19 JTAG loopback control

3.11 Trace support

The ARM1176JZF-S test chip contains an *Embedded Trace Macrocell* (ETM11CS). Trace connectors are provided on the CT1176JZF-S. The JTAG connector on the baseboard provides the JTAG signals that are required for controlling the ETM11CS in the test chip.

See *Connecting Trace* on page 2-9 for details on connecting *RealView Trace* (RVT).

———— **Note** ————

Trace tools such as *RealView Trace* (RVT) that use multiplexed trace packets, require only one Mictor connector (Trace Port A). The CT1176JZF-S supports both multiplexed (one trace connector) and demultiplexed mode (two trace connectors). The second connector is present to support trace tools that use demultiplexed trace packets.

See *Trace Connectors* on page 5-22 for details of the connector pinout and the Mictor connector used on the CT1176JZF-S.

Chapter 4

Test Chip Hardware Description

This chapter provides details of the ARM1176JZF-S test chip which affect the CT1176JZF-S.

It contains the following sections:

- *ARM1176JZF-S test chip overview* on page 4-2
- *Memory map* on page 4-6
- *Pin capture block* on page 4-10
- *Clocks* on page 4-22
- *Resets and interrupts* on page 4-35
- *Debug and JTAG configuration* on page 4-37

Note

Refer to the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0301), *CoreSight ETM11 Technical Reference Manual* (ARM DDI 0318), *Vectored Interrupt Controller Technical Reference Manual* (ARM DDI 0273), and the *PrimeCell AXI Configurable Interconnect (PL300) Technical Reference Manual* (ARM DDI 0354) for further details on the major test chip components.

4.1 ARM1176JZF-S test chip overview

Figure 4-1 shows, in simplified form, the top-level functionality of the test chip.

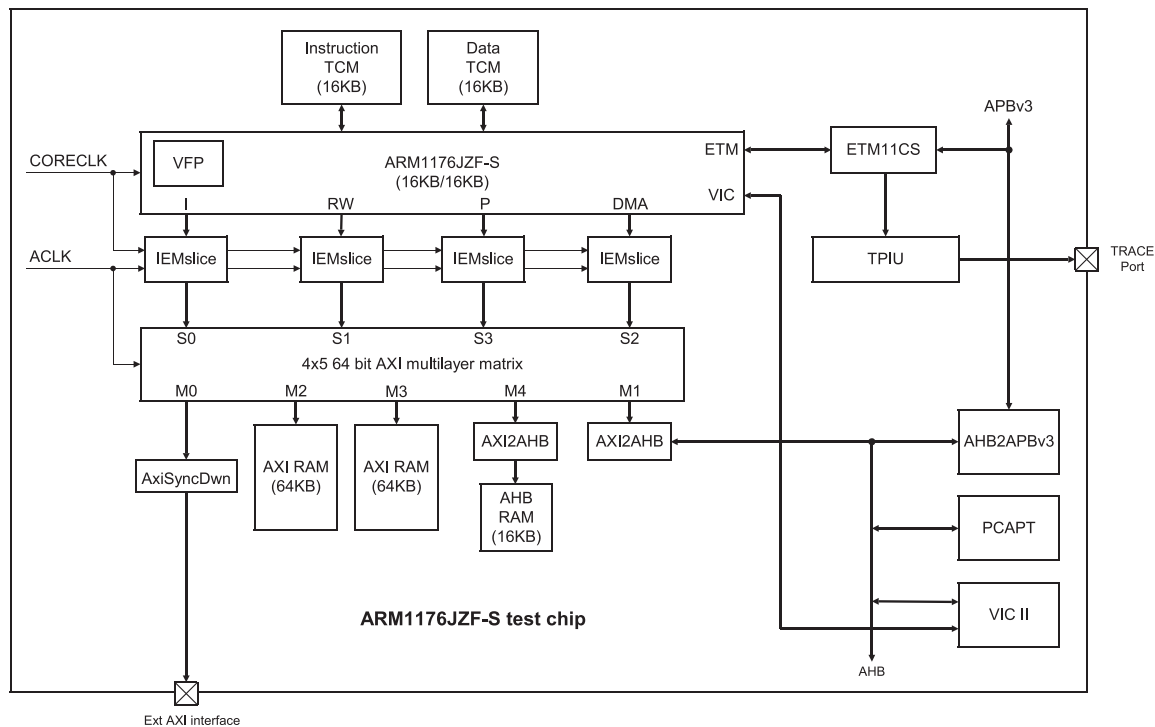


Figure 4-1 Top-level view of ARM1176JZF-S test chip

4.1.1 Block descriptions

The test chip is based on the standard generic test chip used in the validation of ARM processors. It differs from the generic test chip in having an AXI primary interface rather than the AHB interface of the generic test chip.

ARM1176JZF-S

The ARM1176JZF-S has a number of configuration options. The configuration options chosen for the test chip are:

- vector floating point unit (VFP)
- 16KB instruction cache
- 16KB data cache
- cache parity
- *Memory Management Unit* (MMU).

Tightly coupled memory

The test chip implements 16KB of instruction tightly coupled memory (ITCM) and 16KB of data tightly coupled memory (DTCM). The RAM blocks are external to the ARM1176JZF-S. This memory provides single core cycle access.

CoreSight embedded trace macrocell

The CoreSight embedded trace macrocell (ETM11CS) allows real time trace of program execution.

Trace Port Interface Unit

The *Trace Port Interface Unit* (TPIU) converts the internal Trace Bus (ATB) into an external trace bus that is compatible with a Trace Port Analyzer (TPA) such as RealView Trace.

IEM slices

These components are from the ARM *Intelligent Energy Management* (IEM) portfolio and allow the ARM1176JZF-S to run at a higher clock frequency than the on-chip AXI sub-system. These blocks are capable of supporting asynchronous clocks, but they are restricted to synchronous clocking in the ARM1176JZF-S test chip.

Note

These blocks serve only as clock synchronizers and do not provide dynamic clock switching for IEM use.

AXI bus matrix

The bus matrix is a four master, five slave component that allows any master to access any of the five slaves.

The slave ports on the AXI matrix are:

- external AXI interface
- test chip RAM block 0
- test chip RAM block 1
- AHB RAM block
- AHB sub-system.

See *PrimeCell AXI Configurable Interconnect (PL300) Technical Reference Manual* (ARM DDI 0354) for further details on the AXI bus matrix component. The address ranges covered by each of these slave ports is documented in the *Memory map* on page 4-6.

Synchronous AXI bridge

The Synchronous AXI bridge (AxiSyncDwn) between the slave port (M0) of the AXI bus matrix and the external AXI port interfaces the internal AXI buses, running at over 100MHz, to the external AXI bus to the *Emulation Baseboard* (EB) that runs at a maximum of 30MHz.

AXI RAM blocks

Two 64KB blocks of on-chip RAM are provided. These blocks enable instructions and data to be stored on chip, and benchmarks to be performed without the penalties incurred when accessing slow external memory. The RAM blocks can run either at the same clock frequency as the ARM1176JZF-S or at a synchronous lower frequency.

AHB RAM block

The AHB RAM block is used to verify the correct operation of exclusive memory accesses LDREX and STREX to L3 shared memory. It is not intended to be used as general purpose SRAM. It is a small 16KB SRAM, and implemented as two blocks of 2048x32 RAM.

AXI to AHB bridge

The AXI to AHB bridge (AXI2AHB) converts the AXI bus protocol into the AHB-lite bus protocol to enable access to AHB memory through an exclusive access monitor.

AHB sub-system

A number of components within the test chip use the AHB bus protocol rather than the AXI protocol. The slave port (M1) of the AXI bus matrix is used to service these AHB components.

AXI to AHB bridge

The AXI to AHB bridge (AXI2AHB) converts the AXI bus protocol into the AHB-lite bus protocol to allow access to the AHB sub-system.

Vectored interrupt controller

The vectored interrupt controller is included to reduce interrupt latency. The PL192 PrimeCell is used and provides ARM v6 processor VIC port support in synchronous and asynchronous mode. This enables faster interrupt servicing when used with the ARM1176JZF-S processor.

See *Interrupts* on page 4-35, and the *ARM PrimeCell Vectored Interrupt Controller (PL192) Technical Reference Manual* (ARM DDI 0273) for details.

Pin Capture block

The pin capture block (PCAPT) provides control and monitoring of the configuration pins of the ARM1176JZF-S. See *Pin capture block* on page 4-10 for register details.

APB bridge

The APB bridge (AHB2APBv3) translates the AHB bus protocol into the APBv3 bus protocol for connection to the ETM11CS Debug APB port.

4.2 Memory map

The address map of the ARM1176JZF-S test chip is shown in Table 4-1.

Note

Peripherals are multiple mapped throughout their allocated address range.

Each of the peripherals may be disabled by programming the BLKDISABL register. Any access to a disabled peripheral is redirected to the external AXI interface. See *Block disables* on page 4-8 and *Pin capture block* on page 4-10 for further information on the BLKDISABL register.

Table 4-1 ARM1176JZF-S test chip address map

Block	Address	Size	Description
EXT_AXI_1	0x00000000 to 0x3EFFFFFFF	1008MB	Access to external AXI port.
Dummy	0x3F000000 to 0x3F07FFFF	512KB	Dummy slave. Generates AXI SLVERR error responses. Can be disabled.
Spare	0x3F080000 to 0x3F0FFFFFFF	512KB	Spare region. Generates AXI DECERR error responses. Can be disabled.
AHBVIC	0x3F100000 to 0x3F1FFFFFFF	1MB	Control port for vectored interrupt controller (VIC).
PCAPT	0x3F200000 to 0x3F2FFFFFFF	1MB	Pin capture and TZ control.
Reserved	0x3F300000 to 0x3F37FFFF	512KB	Reserved memory space.
Reserved	0x3F380000 to 0x3F3FFFFFFF	512KB	Reserved memory space.
ETM	0x3F400000 to 0x3F4FFFFFFF	1MB	ETM control port.
External	0x3F500000 to 0x3F5FFFFFFF	1MB	Recommended for IEM components.
External	0x3F600000 to 0x3F6FFFFFFF	1MB	Recommended for Level 2 cache controller.
AHBRAM	0x3F700000 to 0x3F7FFFFFFF	1MB	SRAM, 16KB, wrapped.

Table 4-1 ARM1176JZF-S test chip address map (continued)

Block	Address	Size	Description
AXIRAM1	0x3F800000 to 0x3FFFFFFF	4MB max	SRAM, interleaved on 1KB boundaries with AXIRAM0 and wrapped.
AXIRAM0	0x3F800000 to 0x3FFFFFFF	4MB max	SRAM, interleaved on 1KB boundaries with AXIRAM1 and wrapped.
EXT_AXI_2	0x40000000 to 0xCF1FFFFF	2290MB	External AXI access.
Reserved	0xCF200000 to 0xCF2FFFFF	1MB	Reserved memory space.
Reserved	0xCF300000 to 0xCF3FFFFF	1MB	Reserved memory space.
ETM	0xCF400000 to 0xCF4FFFFF	1MB	ETM control registers.
EXT_AXI_3	0xCF500000 to 0xFFFFFFFF	779MB	External AXI access.

4.3 Block disables

You can disable individual on-chip memory-mapped peripherals by writing to the block disable register (BLKDISABL). Each bit in this register corresponds to a particular area of the memory map. Setting a single bit causes all accesses to that area of memory to go to the external AXI port rather than to the peripheral.

Bit 0 of this register is the REMAP control. It causes the test chip RAM AXIRAM0 and AXIRAM1 to occupy memory addresses starting at 0x0, in addition to addresses starting 0x3F800000, their usual address. Table 2-3 shows the block disable control signals.

Table 4-2 Disable controls

Signal	Description
BLKDISABL[7]	Disables the AXIRAM0 and AXIRAM1 blocks. Accesses go to external AXI interface instead when this signal is HIGH.
BLKDISABL[6]	Disables the AHB ETM block. Accesses go to the external AXI interface instead when this signal is HIGH.
BLKDISABL[5]	Unused.
BLKDISABL[4]	Disables the PCAPT block. Accesses go to the external AXI interface instead when this signal is HIGH.
BLKDISABL[3]	Disables the AHB VIC block. Accesses go to the external AXI interface instead when this signal is HIGH.
BLKDISABL[2]	Disables the AHB RAM2 block. Accesses go to the external AXI interface instead when this signal is HIGH.
BLKDISABL[1]	Disables the DUMMY blocks. Accesses go to the external AXI interface instead when this signal is HIGH.

4.4 TrustZone security control

Two control registers enable you to configure the security level of individual on-chip peripherals. One bit in each register is associated with each peripheral. Table 4-3 and Table 4-4 show the associations between the bits in these registers and the peripherals. If both registers are at zero, secure AXI accesses are permitted, and non-secure AXI accesses are denied. When bits in TRUSTZONESD are set, secure accesses made to the peripherals are denied. When bits in TRUSTZONENSA are set, non-secure accesses made to the peripherals are permitted.

Table 4-3 TRUSTZONESD Register contents

Bit	Name	Function
[31:7]	-	Undefined.
[6]	RAM2SD	AHBRAM cannot be accessed from secure state when set.
[5]	TCRAMSD	AXIRAM0 and AXIRAM1 cannot be accessed from secure state when set.
[4:3]	-	Unused.
[2]	PCAPTSD	PCAPT cannot be accessed from secure state when set.
[1]	ETMSD	ETM cannot be accessed from secure state when set
[0]	VICSD	VIC cannot be accessed from secure state when set

Table 4-4 TRUSTZONENSA Register contents

Bit	Name	Function
[31:7]	-	Undefined.
[6]	RAM2NSA	You can access AHBRAM from a non-secure state when set.
[5]	TCRAMNSA	You can access AXIRAM0 and AXIRAM1 from a non-secure state when set.
[4:3]	-	Unused.
[2]	PCAPTNSA	You can access PCAPT from a non-secure state when set.
[1]	ETMNSA	You can access ETM from a non-secure state when set.
[0]	VICNSA	You can access VIC from a non-secure state when set.

4.5 Pin capture block

The Pin Capture block (PCAPT) within the ARM1176JZF-S test chip contains registers for configuring and monitoring pins on the ARM1176JZF-S processor. The PCAPT registers are primarily used to validate the ARM1176JZF-S processor. Only the subset of registers that are required to configure the CT1176JZF-S are described here.

———— **Caution** ————

The PCAPT address allocation is 1MB in the range 0x3F200000 to 0x3F2FFFFF. Several addresses within this range select registers reserved for ARM1176JZF-S processor validation. Accesses to these addresses will have unpredictable results and may result in a system failure. See Table 4-5 for the reserved address locations.

4.5.1 Register Definitions

The PCAPT registers are listed in Table 4-5.

Table 4-5 Pin Capture registers

Name	Address	Description
-	0x3F200000 to 0x3F20005C	Reserved.
ASYNCVIC	0x3F200070	Reads the value of the ASYNCVIC control signal and enables writing of a new value pending a system reset. See <i>ASYNCVIC</i> on page 4-11.
ClkCtl	0x3F200080	Controls Clock divider division values. See <i>ClkCtl</i> on page 4-28.
ClkEnCtl	0x3F200084	Controls Clock divider division values and clock sources. See <i>ClkEnCtl</i> on page 4-30.
-	0x3F200100 to 0x3F200114	Reserved.
ETMCtl	0x3F20011C	Controls the source of ETMEXTINX to the ETM. See <i>ETMCtl</i> on page 4-12
-	0x3F200118	Reserved.

Table 4-5 Pin Capture registers (continued)

Name	Address	Description
IEMCtl	0x3F200090	Reads the SYNCMODEACK outputs and allows the SYNCMODEREQ inputs to the ARM1176JZF-S to be controlled. See <i>IEMCtl</i> on page 4-13.
TRUSTZONENSA	0x3F2000A0	Controls whether non-secure accesses made to the peripherals are permitted. See <i>TrustZone Control Registers</i> on page 4-16
TRUSTZONESD	0x3F2000B0	Controls whether secure accesses made to the peripherals are denied. See <i>TrustZone Control Registers</i> on page 4-16
TC-Control	0x3F2000C0	Controls a number of features of the ARM1176JZF-S test chip. See <i>TC-Control</i> on page 4-19.
-	0x3F2000D0	Reserved.
BLKDISABL	0x3F2000E0	Controls the memory map decoders in the AXI bus matrix. Enables peripherals to be removed from the memory map and the released memory space to be redirected to the external AXI interface. See <i>BLKDISABL</i> on page 4-20.
—	0x3F200200 to 0x3F2FFFFF	Reserved.

ASYNCVIC

The ASYNCVIC register allows setting and reading of **ASYNCVIC** that is used to drive the VIC interface signals **IRQADDRVSYNCEN**, **INTSYNCEN** and **nVICSYNCEN**. See *ARM PrimeCell Vectored Interrupt Controller Technical Reference Manual (PL192)* (DDI 0273) for details of the VIC port connections. By default, out of reset, this signal is driven HIGH to enable asynchronous interfaces. By writing to register bit [0] the state of the signal can be changed. Writes are held pending until the next system reset. Register bit [1] always reflects the actual state of **ASYNCVIC** and will only change after a system reset.

This register is located at PCAPTBASE+0x70 as follows:

Address [31:0]=0x3F200070

Reset by: **nPORESETX** (power-on reset).

Figure 4-2 shows the ASYNCVIC register bit assignments.

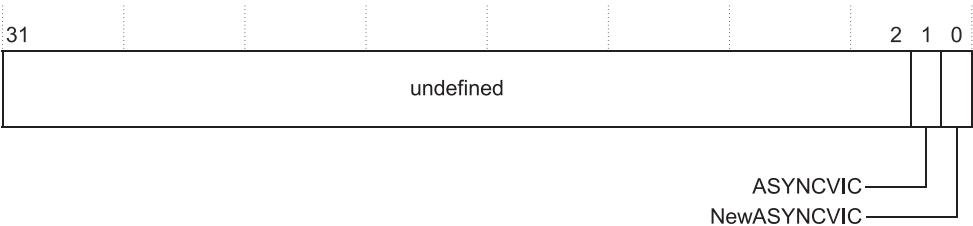


Figure 4-2 ASYNCVIC register bit assignments

Table 4-6 describes the ASYNCVIC register fields.

Table 4-6 ASYNCVIC register

Bits	Access	Name	Reset value	Description
[31:4]	Read only	-	0x00000000	Unused
[3:2]	Read only	-	b00	Unused
[1]	Read only	ASYNCVIC	b1	Reads the value of the ASYNCVIC control signal being driven to ARM1176JZF-S processor and VIC
[0]	Read/Write	NewASYNCVIC	b1	Write new value for the ASYNCVIC control signal, to be driven at next system reset

Clock control registers

The ClkCtl, and ClkEnCtl clock registers control clock distribution in the ARM1176JZF-S test chip and are described in *Clocks* on page 4-22.

ETMCtl

The ETM Control Register selects the input sources for the CoreSight ETM11 **EXTIN[3:0]** bus.

This register is located at PCAPTBASE+0x11C as follows:

Address [31:0]=0x3F20011C

Reset by: **nRESETX** (system reset).

Figure 4-4 on page 4-14 shows the ETMCtl register bit assignments.

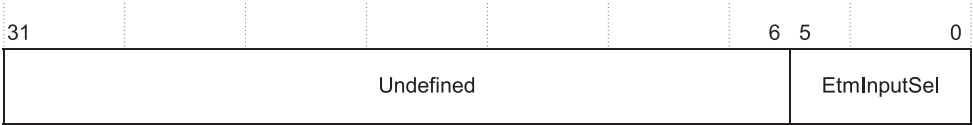


Figure 4-3 ETMCtl register bit assignments

Table 4-7 describes the ETMCtl register fields.

Table 4-7 ETMCtl register bit assignments

Bits	Access	Name	Reset Value	Description
[31:6]	Read/Write	-	SBZ/UNP	Unused
[5:0]	Read/Write	EtmInputSel	b000000	Selects input sources for the ETM11: <ul style="list-style-type: none">bits [5:2] are reserved and must be left at the reset value b0000set bits [1:0] to b11 to select the ETMEXTIN input from the CT1176JZF-S HDRZ header as the source for the ETM11 EXTIN[0] input.

IEMCtl

The IEMCtl register allows the IEM register slices SYNCMODEREQ inputs to be controlled and the SYNCMODEACK outputs to be read. There are also bits that allow pseudo-random strobing of SYNCMODEREQ. This can only be enabled when the corresponding SYNCMODEREQ control bit is set.

This register is located at PCAPTBASE+0x90 as follows:

Address [31:0]=0x3F200090

Reset by: **nPORESETX** (power-on reset).

Figure 4-4 on page 4-14 shows the IEMCtl register bit assignments.

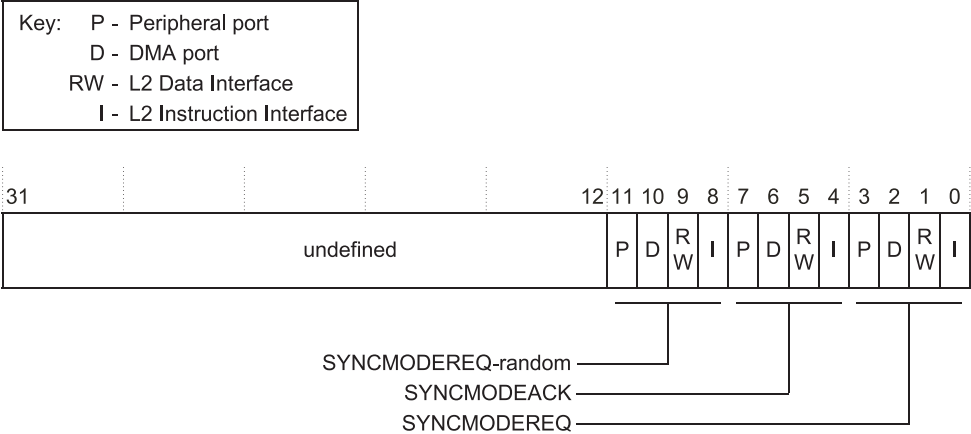


Figure 4-4 IEMCtl register bit assignments

Table 4-8 describes the IEMCtl register fields.

Table 4-8 IEMCtl register

Bits	Access	Name	Reset value	Description
[31:12]	Read as zero, write ignored.	-	0x000000	Undefined.
[11]	Read/Write	SYNCMODEREQP-random	b0	When HIGH enables random strobing of the SYNCMODEREQ input to the P-port IEM register slice. At pseudo-random times SYNCMODEREQP is toggled and then waits for SYNCMODEACKP before toggling again.
[10]	Read/Write	SYNCMODEREQD-random	b0	When HIGH enables random strobing of the SYNCMODEREQ input to the D-port IEM register slice. At pseudo-random times SYNCMODEREQD is toggled and then waits for SYNCMODEACKD before toggling again.

Table 4-8 IEMCtl register (continued)

Bits	Access	Name	Reset value	Description
[9]	Read/Write	SYNCMODEREQRW-random	b0	When HIGH enables random strobing of the SYNCMODEREQ input to the RW-port IEM register slice. At pseudo-random times SYNCMODEREQRW is toggled and then waits for SYNCMODEACKRW before toggling again.
[8]	Read/Write	SYNCMODEREQI-random	b0	When HIGH enables random strobing of the SYNCMODEREQ input to the I-port IEM register slice. At pseudo-random times SYNCMODEREQI is toggled and then waits for SYNCMODEACKI before toggling again.
[7]	Read only	SYNCMODEACKP	b0	When HIGH indicates that the P-port IEM register slice has transitioned to synchronous mode
[6]	Read only	SYNCMODEACKD	b0	When HIGH indicates that the D-port IEM register slice has transitioned to synchronous mode
[5]	Read only	SYNCMODEACKRW	b0	When HIGH indicates that the RW-port IEM register slice has transitioned to synchronous mode
[4]	Read only	SYNCMODEACKI	b0	When HIGH indicates that the I-port IEM register slice has transitioned to synchronous mode
[3]	Read/Write	SYNCMODEREQP	SYNCMODEREQD/P-init	IEM register slice control for the ARM1176JZF-S P-port. When HIGH the contents of the IEM register slice FIFO is multiplexed out of the AXI bus.

Table 4-8 IEMCtl register (continued)

Bits	Access	Name	Reset value	Description
[2]	Read/Write	SYNCMODEREQD	SYNCMODEREQD/P-init	IEM register slice control for the ARM1176JZF-S D-port. When HIGH the contents of the IEM register slice FIFO is multiplexed out of the AXI bus.
[1]	Read/Write	SYNCMODEREQRW	SYNCMODEREQI/RW-init	IEM register slice control for the ARM1176JZF-S RW-port. When HIGH the contents of the IEM register slice FIFO is multiplexed out of the AXI bus.
[0]	Read/Write	SYNCMODEREQI	SYNCMODEREQI/RW-init	IEM register slice control for the ARM1176JZF-S I-port. When HIGH the contents of the IEM register slice FIFO is multiplexed out of the AXI bus.

———— **Note** ————

The *Config-init* register on page 4-33 holds the programmable *Reset values*.

TrustZone Control Registers

There are two TrustZone control registers:

- TRUSTZONENSA
- TRUSTZONESD

The two TrustZone Control Registers control the security policy that is applied to accesses to the various peripherals on the ARM1176JZF-S test chip. With both registers set to 0x0, only secure accesses to the various peripherals are permitted. All non-secure accesses return an error.

Setting bits in TRUSTZONENSA enables non-secure accesses to the peripherals. Setting bits in TRUSTZONESD denies secure access to the peripherals (this is not intended to reflect typical usage of TrustZone memory controls).

———— **Note** ————

- By setting bits in TRUSTZONESD, and clearing them in TRUSTZONENSA, you can deny all accesses to a peripheral.

- The TRUSTZONESD register is contained within the pin capture block.
If accesses to the pin capture block are denied, subsequent writes to this register are not possible. That is, you cannot re-enable accesses to the pin capture block.

TRUSTZONENSA is located at PCAPTBASE+0xA0 as follows:

Address [31:0]=0x3F2000A0

Reset by: **nPORESETX** (power-on reset).

Figure 4-5 shows the TRUSTZONENSA register bit assignments.

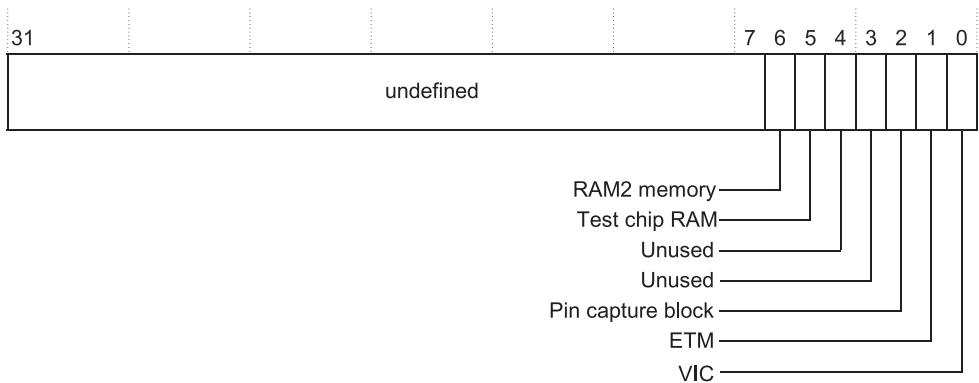


Figure 4-5 TRUSTZONENSA control register bit assignments

Table 4-9 describes the TRUSTZONENSA register fields.

Table 4-9 TRUSTZONENSA register

Bit	Access	Reset value	Peripheral
[31:8]	Read only	0x000000	Unused
[7]	Read only	b1	Unused
[6]	Read/Write	TRUSTZONENSA-init	RAM2 memory
[5]	Read/Write	TRUSTZONENSA-init	Test chip RAM
[4]	Read/Write	b1	Unused
[3]	Read/Write	TRUSTZONENSA-init	Unused

Table 4-9 TRUSTZONENSA register (continued)

Bit	Access	Reset value	Peripheral
[2]	Read/Write	TRUSTZONENSA-init	Pin capture block
[1]	Read/Write	TRUSTZONENSA-init	ETM
[0]	Read/Write	TRUSTZONENSA-init	VIC

TRUSTZONESD is located at PCAPTBASE+0xB0 as follows:

Address [31:0]=0x3F2000B0

Reset by: **nPORESETX** (power-on reset).

Figure 4-6 shows the TRUSTZONESD register bit assignments.

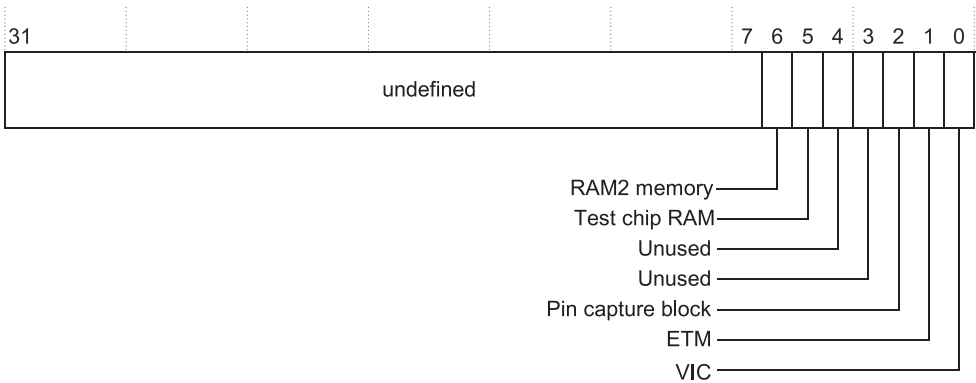


Figure 4-6 TRUSTZONESD control register bit assignments

Table 4-10 describes the TRUSTZONESD register fields.

Table 4-10 TRUSTZONESD register

Bit	Access	Reset value	Peripheral
[31:8]	Read only	0x000000	Unused
[7]	Read only	b0	Unused
[6]	Read/Write	TRUSTZONESD-init	RAM2 memory

Table 4-10 TRUSTZONESD register (continued)

Bit	Access	Reset value	Peripheral
[5]	Read/Write	TRUSTZONESD-init	Test chip RAM
[4]	Read/Write	b0	Unused
[3]	Read/Write	TRUSTZONESD-init	Unused
[2]	Read/Write	TRUSTZONESD-init	Pin capture block
[1]	Read/Write	TRUSTZONESD-init	ETM
[0]	Read/Write	TRUSTZONESD-init	VIC

TC-Control

The TC-Control register controls a number of the features of the ARM1176JZF-S test chip.

This register is located at PCAPTBASE+0xC0 as follows:

Address [31:0]=0x3F2000C0

Reset by: **nPORESETX** (power-on reset).

Figure 4-7 shows the TC-Control register bit assignments.

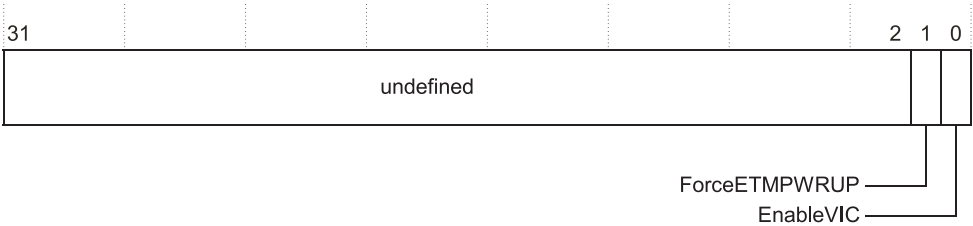


Figure 4-7 TC-Control register bit assignments

Table 4-11 describes the TC-Control register fields.

Table 4-11 TC-Control register

Bits	Access	Name	Reset value	Description
[31:4]	Read as zero, write ignored.	-	0x0000000	Undefined
[3:2]	Read as zero, write ignored.	-	b00	Undefined
[1]	Read/Write	ForceETMPWRUP	b0	When HIGH forces ETMPWRUP (ETM powered up indicator) to the ARM1176JZF-S HIGH
[0]	Read/Write	EnableVIC	b0	When HIGH connects interrupt inputs nIRQ and nFIQ via the VIC

BLKDISABL

The BLKDISABL register controls the memory map decoders in the AXI bus matrix. By setting the appropriate register bit each of the peripherals can be removed from the memory map and the memory space automatically re-allocated to the external AXI interface. When all the register bits are set, all memory accesses are routed to the external AXI interface.

When you set the Test chip RAM remap bit, the test chip memory (RAM0 and RAM1) appears at address 0x0, in addition to address 0x3F800000. This is independent of the test chip RAM disable control.

———— **Caution** ————

This register is implemented within the pin capture block. If the pin capture block is disabled, further writes to this register will not be possible and it will not be possible to re-enable the pin capture block.

This register is located at PCAPTBASE+0xE0 as follows:

Address [31:0]=0x3F2000E0

Reset by: **nPORESETX** (power-on reset)

Figure 4-8 on page 4-21 shows the BLKDISABL bit assignments.

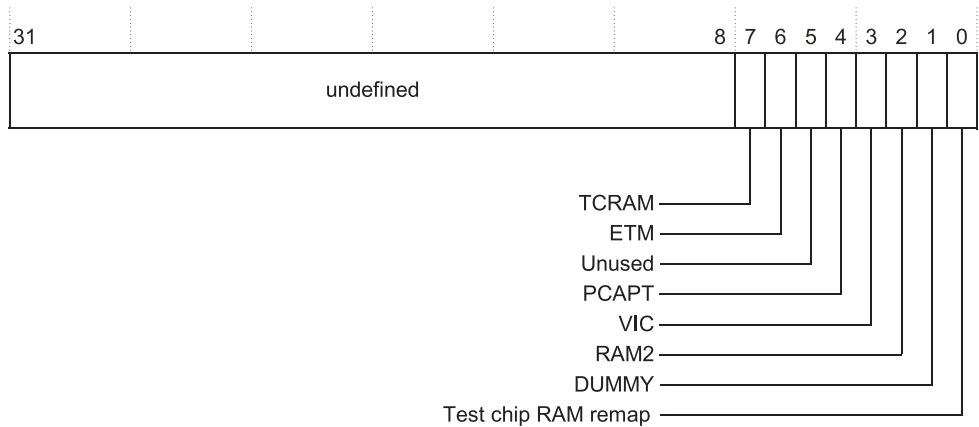


Figure 4-8 BLKDISABL register bit assignments

Table 4-12 describes the BLKDISABL register fields.

Table 4-12 BLKDISABL register

Bits	Access	Name	Reset value	Description
[31:8]	Read as zero, write ignored.	-	0x000000	Undefined
[7]	Read/Write	TCRAM	BLKDISABL-init[7]	Test chip RAM disable
[6]	Read/Write	ETM	BLKDISABL-init[6]	ETM disable
[5]	Read/Write	-	b0	Unused
[4]	Read/Write	PCAPT	BLKDISABL-init[4]	Pin Capture block disable
[3]	Read/Write	VIC	BLKDISABL-init[3]	VIC disable
[2]	Read/Write	RAM2	BLKDISABL-init[2]	RAM2 memory disable
[1]	Read/Write	SPARE/DUMMY	BLKDISABL-init[1]	SPARE/DUMMY region disable
[0]	Read/Write	REMAP-init	REMAP-init	Test chip RAM remap

Note

The *Config-init* register on page 4-32 holds the programmable *reset values*.

4.6 Clocks

This section describes the clocking requirements for the ARM1176JZF-S test chip and contains the following subsections:

- *Clocking overview*
- *PLL* on page 4-23
- *Clock divider* on page 4-26
- *Clock control registers* on page 4-28

4.6.1 Clocking overview

The CT1176JZF-S clocking scheme consists of an on-chip PLL and a programmable clock divider chain.

The PLL is programmed by the CT1176JZF-S PLD during a power-on reset or a system reset.

———— Note —————

To maintain system integrity, PLL programming is only possible during a power-on reset or a system reset.

The clock divider chain is controlled by configuring the ClkCtl, and ClkEnCtl registers in the PCAPT block in the ARM1176JZF-S test chip. Initial register values are determined by the Config-init register. The Config-init register is configured by the CT1176JZF-S PLD during power-on reset. See *Config-init register* on page 4-32.

The clock divider provides the following clocks:

- **ACLKENRW**
- **ACLKENI**
- **ACLKENP**
- **CORECLK**
- **ACLKint**
- **ACLKENext**
- **ACLKext**

4.6.2 PLL

A block diagram of the PLL is shown in Figure 4-9.

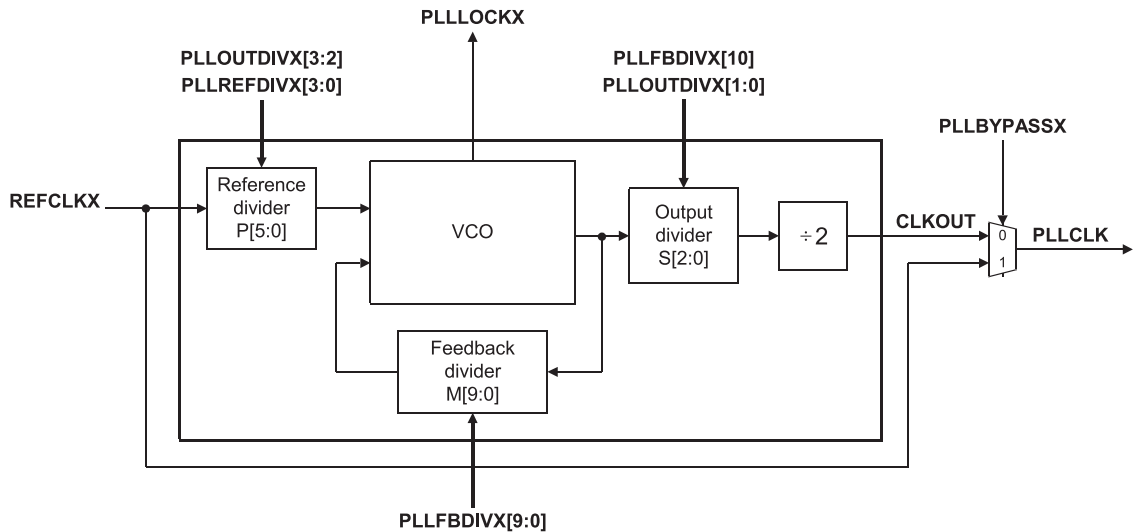


Figure 4-9 PLL block diagram

The output clock frequency is given by:

$$F_{\text{clkout}} = \frac{F_{\text{refclk}} \times M[9:0]}{P[5:0] \times 2^{S[2:0]} \times 2}$$

The operating ranges are:

VCO range 1GHz – 2GHz

PLL range 31.25MHz – 2GHz (before output divide-by-2)

———— **Note** ————

These operating frequencies apply to internal test chip buses only. For details of the baseboard operating constraints see *AXI bus timing specification* on page 5-33.

Table 4-13 provides a description of the PLL signals.

Table 4-13 PLL signal description

Name	Description	Function
REFCLKX	Input clock	The input clock provides the reference frequency for the PLL. It is supplied either by the baseboard or another tile in the tile stack. See <i>Clocks</i> on page 3-5.
PLLOUTDIVX[3:2] PLLREFDIVX[3:0]	Reference divisor	<p>The Reference divider value, P[5:0] sets the input frequency scaling for the PLL. It is set by the PLLREFDIV field and part of the PLLOUTDIV field in the <i>Serial write data register</i> .</p> <p>———— Note ————</p> <p>This mapping is to maintain pin compatibility with the ARM1156T2F-S test chip PLL configuration pinout. See Table 4-14 on page 4-25 for mapping details.</p> <p>—————</p> <p>Default value is b000011. See <i>Baseboard system FPGA registers</i> on page 3-42.</p>
PLLFBDIVX[9:0]	Feedback divisor	<p>The Feedback divider value, M[9:0] sets the input to output frequency scaling for the PLL. The frequency multiplier applied is equal to M divided by 2. M=0 is not permitted. It is set by the PLLFBDIV field in the <i>Serial write data register</i>. Default value is 0x090. See <i>Baseboard system FPGA registers</i> on page 3-42.</p>

Table 4-13 PLL signal description (continued)

Name	Description	Function
PLLFBDIVX[10] PLLOUTDIVX[1:0]	Output divisor	<p>The Output divider value, S[2:0] sets the output frequency scaling for the PLL. It is set by part of the PLLOUTDIV field and part of the PLLFBDIV field in the <i>Serial write data register</i>.</p> <hr/> <p>Note</p> <p>This mapping is to maintain pin compatibility with the ARM1156T2F-S test chip PLL configuration pinout. See Table 4-14 for the mapping details.</p> <hr/> <p>Default value is b001. See <i>Baseboard system FPGA registers</i> on page 3-42.</p>
PLLLOCKX	PLL locked	When HIGH indicates that the output clock PLLCLK is phase locked to the input clock REFCLKX .
PLLBYPASSX	PLL bypass	<p>When HIGH bypasses the PLL and routes the input clock, REFCLKX as the PLL output clock, PLLCLK. It is controlled by the PLLBYPASS field in the <i>Serial write data register</i>. PLL bypass is used for test purposes and in the initial stages of booting the ARM1176JZF-S test chip.</p> <p>Default value is b0. See <i>Baseboard system FPGA registers</i> on page 3-42.</p>

Table 4-14 PLL configuration mapping

External PLL control	Internal divisor	PLL divider	Permitted range
PLLFBDIVX[9:0]	M[9:0]	Feedback divider	$56 \leq M \leq 1023$
PLLOUTDIVX[3:2]	P[5:4]	Reference divider	$1 \leq P \leq 63$
PLLREFDIVX[3:0]	P[3:0]		
PLLFBDIVX[10]	S[2]	Output divider	$0 \leq S \leq 5$
PLLOUTDIVX[1:0]	S[1:0]		

Caution

The feedback frequency should be kept between 1GHz and 2GHz and **PLLCLK** between 15.625MHz and 1GHz. If you need to change the default values you should contact ARM Support for advice on selecting the M, P, and S divisor values.

4.6.3 Clock divider

A simplified block diagram of the clock divider is shown in Figure 4-10.

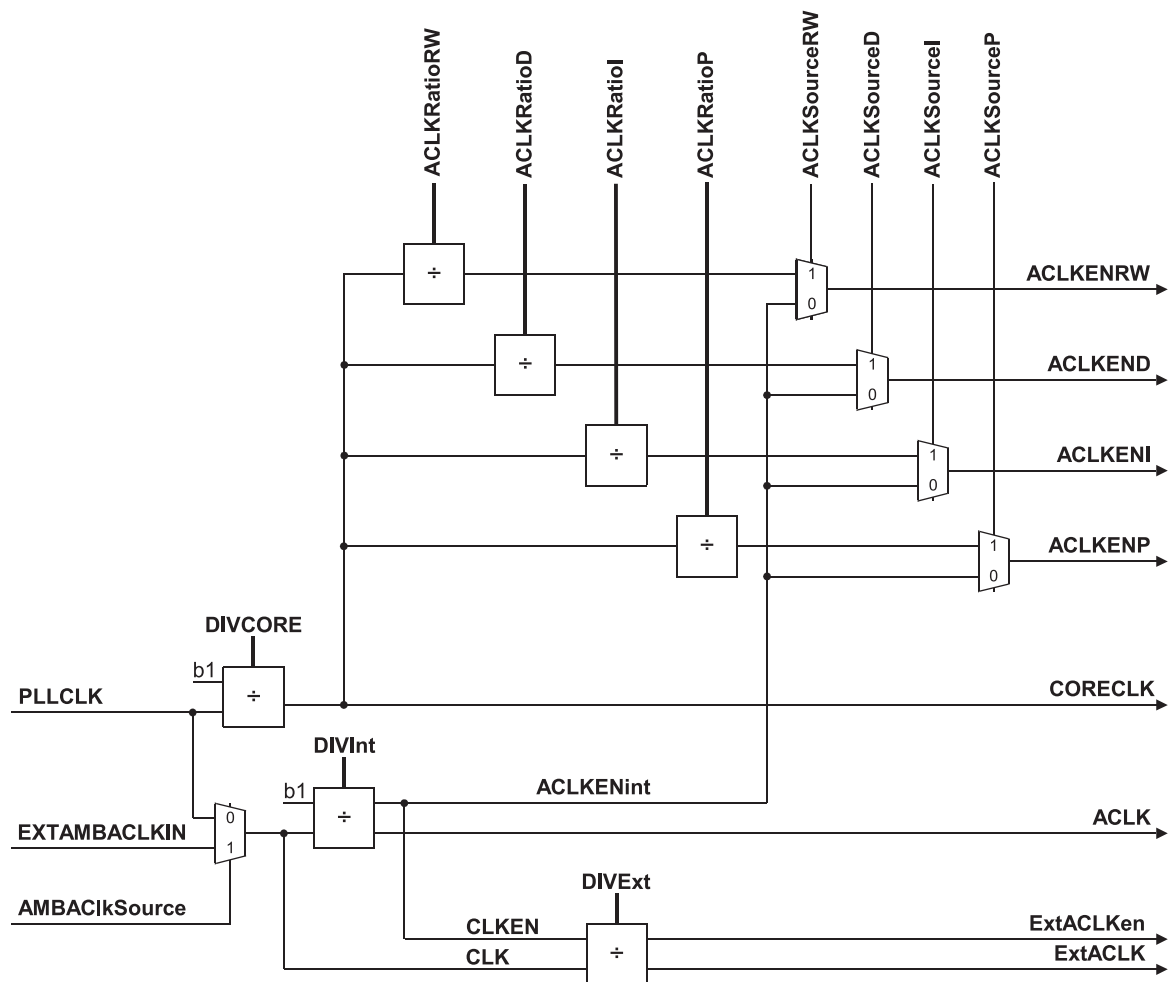


Figure 4-10 Clock divider block diagram

Table 4-15 provides a description of the Clock divider signals.

Table 4-15 Clock divider signal description

Name	Description	Function
PLLCLK	PLL clock	The PLL clock provides the reference frequency for the Clock divider. See <i>PLL</i> on page 4-23 for details.
DIVCORE	CORECLK divisor	This is the CORECLK divider value. It is controlled by the DivCore field in the ClkCtl register. A default value is set in the DivCore-init field in the Config-init register by the CT1176JZF-S PLD during test chip initialization.
DIVInt	ACLK and ACLKENint divisor	This is the ACLK and ACLKENint divider value. It is controlled by the DivInt field in the ClkCtl register. A default divider value is set in the DivInt-init field in the Config-init register by the CT1176JZF-S PLD during test chip initialization.
DIVExt	ExtACLK and ExtACLKEN divisor	This is the ExtACLK and ExtACLKEN divider value. It is controlled by the DivExt field in the ClkCtl register. A default divider value is set in the DivExt-init field in the Config-init register by the CT1176JZF-S PLD during test chip initialization.
ACLKRatioRW	ACLKENRW divisor	This is the ACLKENRW divider value. It sets the CORECLK to ACLKENRW ratio. It is controlled by the ACLKRatioRW[3:0] field in the ClkEnCtl register.
ACLKSourceRW	ACLKENRW selector	When HIGH ACLKENRW is sourced from the ACLKENRW divider. When LOW ACLKENRW is sourced from the ACLKENint divider. It is controlled by the ACLKSourceRW bit in the ClkEnCtl register.
ACLKRatioD	ACLKEND divisor	This is the ACLKEND divider value. It sets the CORECLK to ACLKEND ratio. It is controlled by the ACLKRatioD[3:0] field in the ClkEnCtl register.
ACLKSourceD	ACLKEND selector	When HIGH ACLKEND is sourced from the ACLKEND divider. When LOW ACLKEND is sourced from the ACLKENint divider. It is controlled by the ACLKSourceD bit in the ClkEnCtl register.
ACLKRatioI	ACLKENI divisor	This is the ACLKENI divider value. It sets the CORECLK to ACLKENI ratio. It is controlled by the ACLKRatioI field in the ClkEnCtl register.

Table 4-15 Clock divider signal description (continued)

Name	Description	Function
ACLKSourceI	ACLKENI selector	When HIGH ACLKENI is sourced from the ACLKENI divider. When LOW ACLKENI is sourced from the ACLKENint divider. It is controlled by the ACLKSourceI bit in the ClkEnCtl register.
ACLKRatioP	ACLKENP divisor	This is the ACLKENP divider value. It sets the CORECLK to ACLKENP ratio. It is controlled by the ACLKRatioP field in the ClkEnCtl register.
ACLKSourceP	ACLKENP selector	When HIGH ACLKENP is sourced from the ACLKENP divider. When LOW ACLKENP is sourced from the ACLKENint divider. It is controlled by ACLKSourceP bit in the ClkEnCtl register.

4.6.4 Clock control registers

The Pin Capture block (PCAPT) within the ARM1176JZF-S test chip contains the ClkCtl and ClkEnCtl registers that control the ARM1176JZF-S test chip clocks.

Caution

There are a number of restrictions to the way that clock generation can be controlled by the clock control registers. It is strongly advised that you use the default clock configuration settings applied by the CT1176JZF-S PLD during power-on reset.

The Pin Capture block base address, PCAPTBASE, is 0xCF20,0000.

The clock control register definitions are:

ClkCtl

This register is located at PCAPTBASE+0x80 as follows:

Address [31:0]=0x3F200080

Reset by: **nPORESETX** (power-on reset)

Figure 4-11 on page 4-29 shows the ClkCtl register bit assignments.

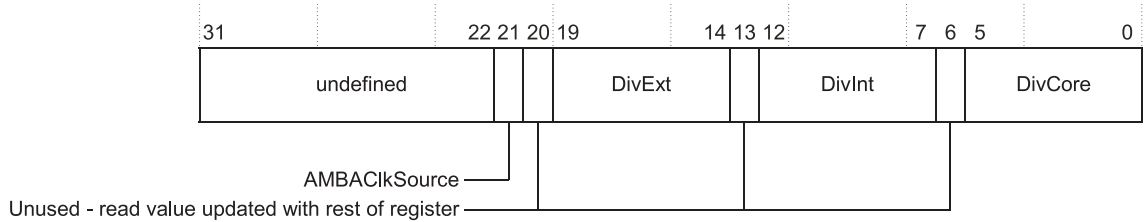


Figure 4-11 ClkCtl bit assignments

Table 4-16 lists the ClkCtl register fields.

Table 4-16 ClkCtl register

Bits	Access	Name	Reset value	Description
[31:22]	Read as zero, write ignored.	-	b0	Undefined.
[21]	Read/Write	AMBAClkSource	AMBAClkSource-init	Selects PLLCLK or EXTAMBACLKIN as the source for the ACLKint and divider ACLKext dividers. See <i>Clock divider</i> on page 4-26 for details.
[20]	Read/Write	-	b0	Unused but read value updates with rest of register.
[19:14]	Read/Write	DivExt	DivExt-init[5:0]	Sets the PLLCLK to ExtACLK and ExtACLKEN divisor in the test chip Clock divider. See <i>Clock divider</i> on page 4-26.
[13]	Read/Write	-	b0	Unused but read value updates with rest of register.
[12:7]	Read/Write	DivInt	DivInt-init[5:0]	Sets the PLLCLK to ACLK and ACLKENint divisor in the test chip Clock divider. See <i>Clock divider</i> on page 4-26.
[6]	Read/Write	-	b0	Unused but read value updates with rest of register.
[5:0]	Read/Write	DivCore	DivCore-init[5:0]	Sets the PLLCLK to CORECLK divisor in the test chip Clock divider. See <i>Clock divider</i> on page 4-26.

Note

The *Config-init* register on page 4-32 holds the programmable *reset values*.

ClkEnCtl

This register is located at PCAPTBASE+0x84 as follows:

Address [31:0]=0x3F200084

Reset by: **nPORESETX** (power-on reset).

Figure 4-12 shows the ClkEnCtl register bit assignments.

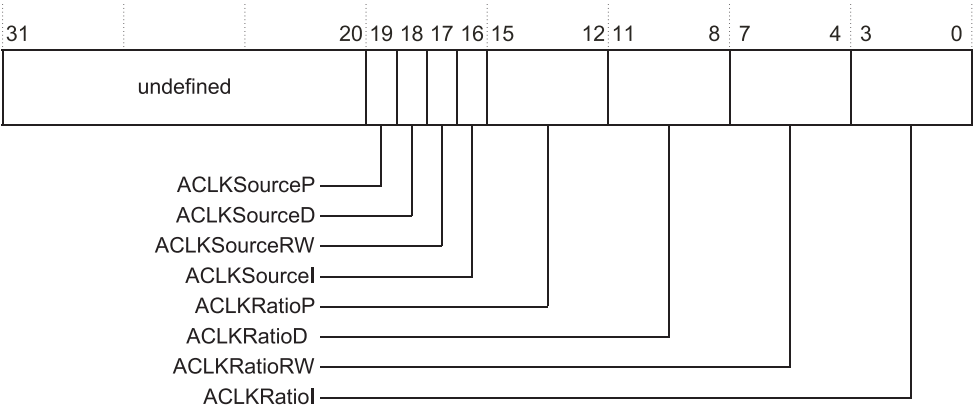


Figure 4-12 ClkEnCtl bit assignments

Table 4-17 lists the ClkEnCtl register fields.

Table 4-17 ClkEnCtl register

Bits	Access	Name	Reset value	Description
[31:20]	Read as zero, write ignored.	-	0x000	Undefined.
[19]	Read/Write	ACLKSourceP	AMBAClkSource-init	When HIGH: Sources ACLKENP from the ACLKRatioP divider. When LOW: Sources ACLKENP from the ACLKENint divider. See <i>Clock divider</i> on page 4-26.
[18]	Read/Write	ACLKSourceD	AMBAClkSource-init	When HIGH: Sources ACLKEND from the ACLKRatioD divider. When LOW: Sources ACLKEND from the ACLKENint divider. See <i>Clock divider</i> on page 4-26.
[17]	Read/Write	ACLKSourceRW	AMBAClkSource-init	When HIGH: Sources ACLKENRW from the ACLKRatioRW divider. When LOW: Sources ACLKENRW from the ACLKENint divider. See <i>Clock divider</i> on page 4-26.
[16]	Read/Write	ACLKSourceI	AMBAClkSource-init	When HIGH: Sources ACLKENI from the ACLKRatioI divider. When LOW: Sources ACLKENI from the ACLKENint divider. See <i>Clock divider</i> on page 4-26.
[15:12]	Read/Write	ACLKRatioP	0x0	Sets the CORECLK to ACLKENP ratio.
[11:8]	Read/Write	ACLKRatioD	0x0	Sets the CORECLK to ACLKEND ratio.
[7:4]	Read/Write	ACLKRatioRW	0x0	Sets the CORECLK to ACLKENRW ratio.
[3:0]	Read/Write	ACLKRatioI	0x0	Sets the CORECLK to ACLKENI ratio.

Note

The *Config-init register* on page 4-32 holds the programmable *reset values*.

4.7 Test chip configuration

The ARM1176JZF-S is configured by the CT1176JZF-S PLD using the **nCONFIGRSTX**, **CONFIGINITX**, **RVALIDX**, and **RDATAX[31:0]** inputs,

The Config-init register is mapped to **RDATAX[31:0]** for ARM1176JZF-S test chip power-on configuration. After a **nCONFIGRSTX** reset and if **RVALIDX** is HIGH, the Config-init register is loaded from **RDATAX[31:0]** on the rising edge of **CONFIGINITX**.

See *Power-on ARM1176JZF-S test chip configuration timing* on page 3-8 for details.

4.7.1 Config-init register

Figure 4-13 shows the Config-init register bit assignments.

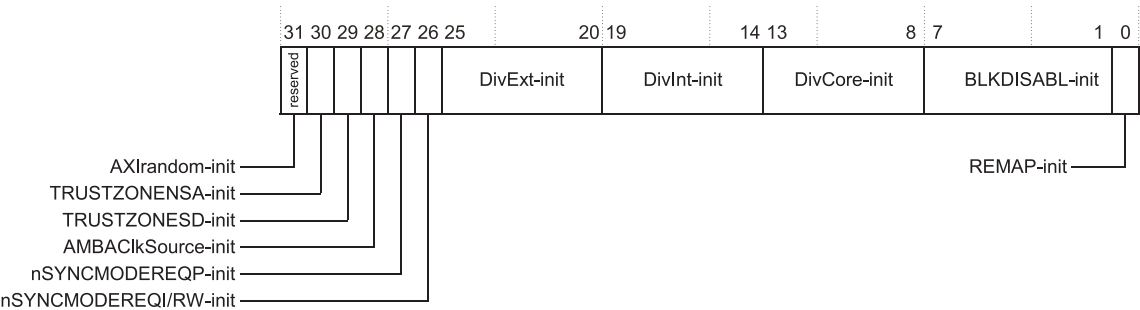


Figure 4-13 Config-init bit assignments

Table 4-18 on page 4-33 lists the Config-init register fields.

Table 4-18 Config-init register

Bits	Access	Name	Reset value	Description
[31]	RDATA[31] qualified by CONFIGINITX and RVALIDX	AXIrandom-init	b0	Reserved (set to zero).
[30]	RDATA[30] qualified by CONFIGINITX and RVALIDX	TRUSTZONENSA	b1	Sets the initial value of the TRUSTZONENSA register. Non-secure accesses to the test chip peripherals are allowed. See <i>TrustZone Control Registers</i> on page 4-16.
[29]	RDATA[29] qualified by CONFIGINITX and RVALIDX	TRUSTZONESD	b0	Sets the initial value of the TRUSTZONESD register. Secure accesses to the test chip peripherals are allowed. See <i>TrustZone Control Registers</i> on page 4-16.
[28]	RDATA[28] qualified by CONFIGINITX and RVALIDX	AMBAclkSource-init	b1	Sets the initial value of the ACLKSource field in the test chip ClkEnCtl register. See <i>ClkEnCtl</i> on page 4-30.
[27]	RDATA[27] qualified by CONFIGINITX and RVALIDX	nSYNCMODEREQP-init	b0	Sets the initial value of the SYNCMODEREQ P-port bit in the test chip IEMCtl-register. See <i>IEMCtl</i> on page 4-13 for details.
[26]	RDATA[26] qualified by CONFIGINITX and RVALIDX	nSYNCMODEREQI/RW-init	b0	Sets the initial value of the SYNCMODEREQ I-port and RW-port bits in the test chip IEMCtl-register. See <i>IEMCtl</i> on page 4-13 for details.
[25:20]	RDATA[25:20] qualified by CONFIGINITX and RVALIDX	DivExt-init	b000101	Sets the initial value of the DivExt field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.

Table 4-18 Config-init register (continued)

Bits	Access	Name	Reset value	Description
[19:14]	RDATA[19:14] qualified by CONFIGINITX and RVALIDX	DivInt-init	b0000000	Sets the initial value of the DivInt field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.
[13:8]	RDATA[13:8] qualified by CONFIGINITX and RVALIDX	DivCore-init	b0000000	Sets the initial value of the DivCore field in the test chip ClkCtl register. See <i>ClkCtl</i> on page 4-28.
[7:1]	RDATA[7:1] qualified by CONFIGINITX and RVALIDX	BLKDISABL-init	b00000000	Sets the initial value of the BLKDISABL field in the test chip BLKDISABL register. See <i>BLKDISABL</i> on page 4-20.
[0]	RDATA[0] qualified by CONFIGINITX and RVALIDX	REMAP-init	b0	Sets the initial value of the Test chip RAM REMAP field in the BLKDISABL register. See <i>BLKDISABL</i> on page 4-20

4.8 Resets and interrupts

This section describes the reset and interrupt signals that enter the ARM1176JZF-S test chip pins and contains the following sections:

- *Resets*
- *Interrupts*

4.8.1 Resets

The ARM1176JZF-S test chip has the following reset lines:

- | | |
|--------------------|--|
| nPORESETX | This is the power-on reset to the test chip. It is a full system reset that also initializes the CP14 debug logic in the ARM1176JZF-S. |
| nRESETX | This is the main test chip reset. It initializes the majority of the processor and test chip peripheral logic. |
| nCONFIGRSTX | This is the configuration reset. It initializes the configuration logic in the ARM1176JZF-S test chip including the PLL control registers. |

4.8.2 Interrupts

This section describes the interrupt signals that enter the test chip and the internal *Vectored Interrupt Controller (VIC)* interrupt sources.

The ARM1176JZF-S test chip has the following interrupt lines:

- | | |
|--------------|---|
| nFIQX | This is the fast interrupt input to the ARM1176JZF-S test chip. |
| nIRQX | This is the normal interrupt input to the ARM1176JZF-S test chip. |

Interrupt Routing

Two routing options are available:

- By default, following a reset, the VIC is disabled and the **nIRQX** and **nFIQX** interrupt inputs are passed directly to the **nFIQ** and **nIRQ** inputs of the ARM1176JZF-S processor.
- If bit[0] of the TC-Control register in the PCAPT block is set HIGH, the VIC is enabled and the **nFIQX** and **nIRQX** interrupt inputs are routed to the VIC interrupt sources VICINTSOURCE[0] and VICINTSOURCE[10] respectively. The VIC **nVICFIQ** and **nVICIRQ** outputs are passed to the **nFIQ** and **nIRQ** inputs of the ARM1176JZF-S processor.
See *TC-Control* on page 4-19 and *VIC interrupt sources* on page 4-36.

Vectored Interrupt Controller

The *Vectored Interrupt Controller* (VIC) is a 32-bit AHB peripheral. The AHB slave interface that controls the VIC is located at VICBASE = 0x3F100000 and has the allocated 1MB address range 0x3F100000 to 0x3F1FFFFFF. VIC register addresses alias throughout this range. See the *ARM PrimeCell Vectored Interrupt Controller (PL192) Technical Reference Manual* (DDI 0273) for register details and base address offsets.

The VIC supports 32 vectored IRQ interrupts. The interrupt sources in the CT1176JZF-S test chip are listed in Table 4-19.

Table 4-19 VIC interrupt sources

Interrupt source	Connects to	Description
VICINTSOURCE[0]	~nFIQX	Test chip nFIQ input
VICINTSOURCE[1]	~nVALFIQ	Request for a Fast Interrupt (test signal from ARM1176JZF-S)
VICINTSOURCE[2]	~nDMASIRQ	DMA controller secure interrupt
VICINTSOURCE[3]	~nDMAEXTERRIRQ	Non-maskable DMA error interrupt
VICINTSOURCE[5:4]]	Logic 0	Unused
VICINTSOURCE[6]	COMMRX	Comms channel receive
VICINTSOURCE[7]	COMMTX	Comms channel transmit
VICINTSOURCE[9:8]	Logic 0	Unused
VICINTSOURCE[10]	~nIRQ	Test chip nIRQ input
VICINTSOURCE[11]	~nVALIRQ	Request for an Interrupt (test signal from ARM1176JZF-S)
VICINTSOURCE[12]	~nDMAIRQ	DMA controller non-secure interrupt
VICINTSOURCE[13]	~nPMUIRQ	Interrupt request from System Metrics
VICINTSOURCE[14]	~nVALRESET	Request for Reset (test signal from ARM1176JZF-S)
VICINTSOURCE[31:15]	Logic 0	Unused

——— **Note** ———

The VIC interrupt sources are level sensitive, active HIGH. Active LOW interrupts that connect to the VIC, such as **nFIQ**, are inverted by the CT1176JZF-S test chip.

4.9 Debug and JTAG configuration

This section describes the Debug and JTAG hardware of the test chip. It contains the following sections:

- *TAP controller*
- *Debug* on page 4-38
- *JTAG Configuration* on page 4-38
- *TAP ID registers* on page 4-39

4.9.1 TAP controller

An IEEE 1149.1 TAP controller is instantiated at the top-level of the test chip to provide a boundary scan chain. The IEEE 1149.1 TAP controller uses the same IEEE 1149.1 pins that the RealView ICE communication uses, so that the number of additional pins required is kept to a minimum.

BYPASS, EXTEST, and SAMPLE/PRELOAD instructions are the minimum functionality you require to perform the boundary scan during JTAG configuration of the test chip.

The test chip provides a specific ID code and you can obtain this using the IDCODE instruction. Table 4-20 lists the test chip TAP instructions.

Table 4-20 Test chip TAP instructions

TAP controller instruction	Instruction encoding
BYPASS	b11111
EXTEST	b00000
IDCODE	b00001
SAMPLE/PRELOAD	b00010

A separate control pin, **nBSTAPEN**, multiplexes the IEEE 1149.1 port. See Figure 4-14 on page 4-38.

Note

When **nBSTAPEN** is HIGH, the TAP controller of the ARM1176JZF-S is used. A JTAG port synchronizer is also included as part of the ARM1176JZF-S.

Figure 4-14 shows the test chip and ARM1176JZF-S TAP controller connections.

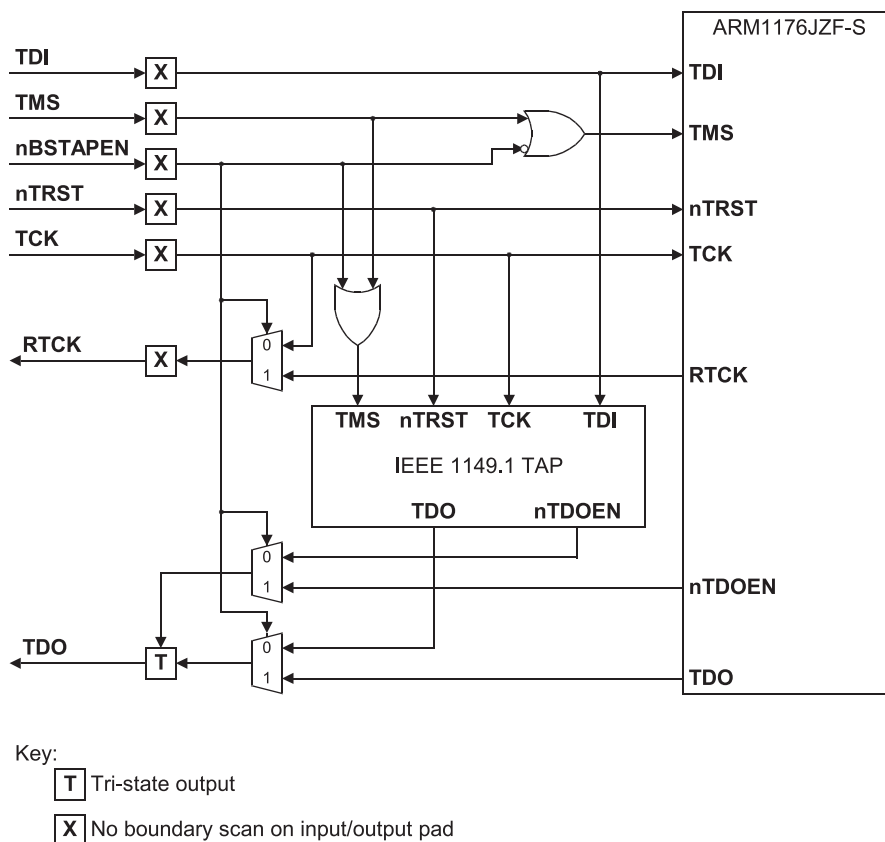


Figure 4-14 Test chip and ARM1176JZF-S TAP controller connections

4.9.2 Debug

When the **nBSTAPEN** input is HIGH the ARM1176JZF-S DBG TAP controller is selected. You can now debug the ARM1176JZF-S using a DBG TAP debugger such as RealView ICE.

4.9.3 JTAG Configuration

When the **nBSTAPEN** input is LOW the test chip boundary scan chain cells are controlled using the test chip TAP controller. You can now configure the test chip using its input and output pins.

All inputs and outputs, except for the 5-pin JTAG interface, **RTCK** and **nBSTAPEN**, have boundary scan cells on them.

4.9.4 TAP ID registers

The TAP ID code is a 32-bit number divided into multiple fields. Figure 4-15 shows the TAP ID register bit assignments.

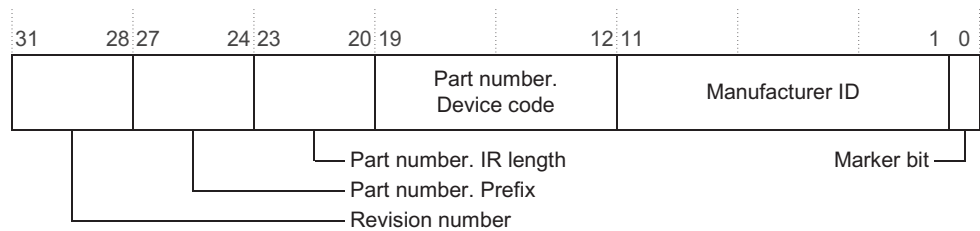


Figure 4-15 TAP ID register

You can access the *ARM1176JZF-S TAP ID code* when the CT1176JZF-S is in Debug mode.

The ARM1176JZF-S TAP ID code is:

0x07B76F0F

Table 4-21 lists how the register divides the number.

Table 4-21 ARM1176JZF-S TAP ID register

Bit field	Use	Description	Value
[31:28]	Revision number	Revision number for the ARM1176JZF-S, not necessarily the same as the test chip revision number.	0x0
[27:12]	Device ID	Holds the ARM specific device ID	0x7B76
[11:1]	Manufacturer ID	Holds the officially registered pattern.	b11110000111
[0]	Marker bit	Always set to 1, as required by the JTAG specification.	b1

See the *ARM1176JZF-S Technical Reference Manual* (ARM DDI 0360) for details of the remaining Debug registers in the ARM1176JZF-S.

You can access the *test chip boundary scan TAP ID code* when the CT1176JZF-S is in JTAG Configuration mode.

The test chip TAP ID is:

0x0F21DF0F

Table 4-22 lists how the register divides the number.

Table 4-22 Test chip TAP ID register

Bit field	Use	Description	Value
[31:28]	Revision number	Revision number for the test chip, not necessarily the same as the core revision number.	0x0
[27:12]	Part number	[27:24] prefix. This is a fixed pattern.	0xF
		[23:20] IR length. Identifies the length of the instruction register within the TAP.	0x2
		[19:12] device code. This pattern identifies the test chip.	0x1D
[11:1]	Manufacturer ID	Holds the officially registered pattern.	b11110000111
[0]	Marker bit	Always set to 1, as required by the JTAG specification.	b1

Chapter 5

CT1176JZF-S Signal Descriptions

This chapter provides a summary of signals present on the CT1176JZF-S connectors, test points, and the links that can be modified to change signal routing. It contains the following sections:

- *Header connectors* on page 5-2
- *Trace Connectors* on page 5-22
- *Links, test points, and LED indicators* on page 5-25
- *AXI bus timing specification* on page 5-33.

5.1 Header connectors

Figure 5-1 shows the pin numbers and power-blade usage of the HDRX, HDRY, and HDRZ headers on the upper side of the CT1176JZF-S. For details on power supply usage see *Power supply control* on page 3-16.

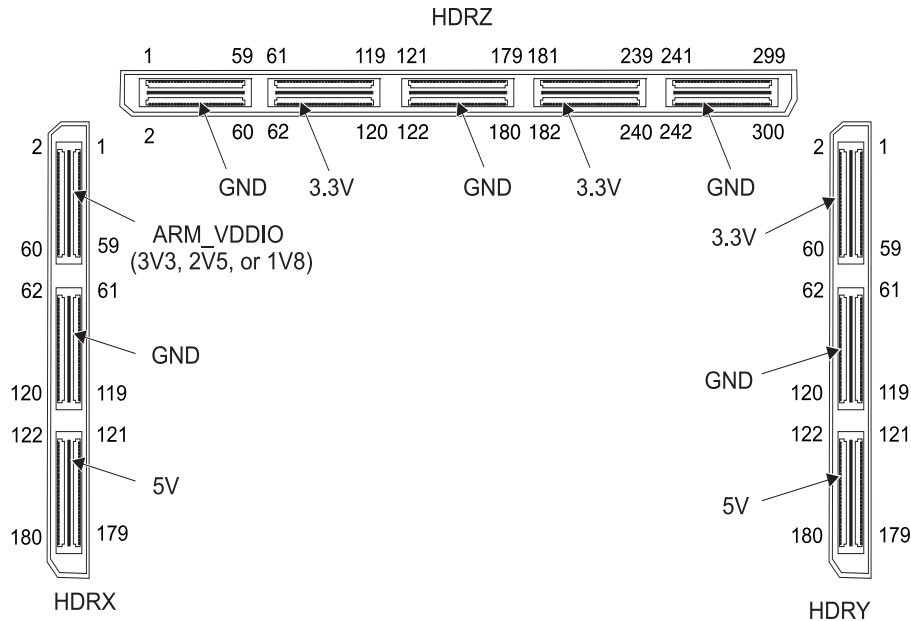


Figure 5-1 HDRX, HDRY, and HDRZ (upper) pin numbering

Table 5-1 on page 5-3 lists the Samtec part numbers.

The CT1176JZF-S uses the Samtec -05- connectors on the top and the Samtec -01- connectors on the bottom of the board. The total board separation is 20mm. The Core Tiles have a maximum component height of 2.5mm on the bottom and 6mm on the top of the board. This ensures that there are no component interference problems with mated boards.

———— **Note** ————

Samtec describes the QTH connector (used on the upper side of the tile) as a header and the QSH connector (used on the lower side of the tile) as a socket.

Table 5-1 Samtec part numbers

Header	Part number	Mating height (mm)
HDRX (upper)	QTH-090-05-F-D-A	12
HDRXL (lower)	QSH-090-01-F-D-A-K	8
HDRY (upper)	QTH-090-05-F-D-A	12
HDRYL (lower)	QSH-090-01-F-D-A-K	8
HDRZ (upper)	QTH-150-05-F-D-A	12
HDRZL (lower)	QSH-150-01-F-D-A-K	8

5.1.1 HDRX signals

Table 5-2 on page 5-4 lists the signals on the HDRX pins for the CT1176JZF-S and the baseboard. The ARM1176JZF-S AXI port signals are multiplexed onto the pins on this header.

Note

Corresponding pins on the upper and lower headers feed the signals through the tile stack.

The signal on the upper header of the CT1176JZF-S is named XUn and the signal on the lower header is named XLn , the table entry is Xxn . Replace x by L for the signal on the lower header and by U for the signal on the upper header. For example, the pin 1 signal for the lower header is **XL90** and the pin 1 signal for the upper header is **XU90** and the corresponding CT1176JZF-S signal is **ARADDRX13 / ARADDRX29**. This example also illustrates the designation used for a multiplexed signal, X / Y where signal X is present when **CLKOUTDIV** is HIGH and signal Y is present when **CLKOUTDIV** is LOW. See *Multiplexing scheme* on page 3-21 for further details of the AXI signal multiplexing.

For the EB there are two HDRX headers (tile site 1 and tile site 2). Replace the **TnX** signal prefix in the table by **T1X** or **T2X** to get the signal name for tile site 1 or 2 respectively.

Table 5-2 HDRX signals

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
ARADDRX12 / ARADDRX28	TnX89	2	1	TnX90	ARADDRX13 / ARADDRX29
ARADDRX11 / ARADDRX27	TnX88	4	3	TnX91	ARADDRX14 / ARADDRX30
ARADDRX10 / ARADDRX26	TnX87	6	5	TnX92	ARADDRX15 / ARADDRX31
ARADDRX9 / ARADDRX25	TnX86	8	7	TnX93	ARIDX0 / ARIDX2
ARADDRX8 / ARADDRX24	TnX85	10	9	TnX94	ARIDX1 / ARIDX3
ARADDRX7 / ARADDRX23	TnX84	12	11	TnX95	ARLENX0 / ARLENX2
ARADDRX6 / ARADDRX22	TnX83	14	13	TnX96	ARLENX1 / ARLENX3
ARADDRX5 / ARADDRX21	TnX82	16	15	TnX97	ARSIZEX0 / ARSIZEX1
ARADDRX4 / ARADDRX20	TnX81	18	17	TnX98	b0 / ARPROTX2
ARADDRX3 / ARADDRX19	TnX80	20	19	TnX99	ARPROTX0 / ARPROTX1
ARADDRX2 / ARADDRX18	TnX79	22	21	TnX100	ARBURSTX0 / ARBURSTX1
ARADDRX1 / ARADDRX17	TnX78	24	23	TnX101	ARLOCKX0 / ARLOCKX1
ARADDRX0 / ARADDRX16	TnX77	26	25	TnX102	ARCACHEX0 / ARCACHEX2
BREADYX	TnX76	28	27	TnX103	ARCACHEX1 / ARCACHEX3

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
BVALIDX	TnX75	30	29	TnX104	ARVALIDX / b0
BRESPX0 / BRESPX1	TnX74	32	31	TnX105	ARREADYX
Xx73 (BIDX4)	TnX73	34	33	TnX106	RDATAx0 / RDATAx32
BIDX1 / BIDX3	TnX72	36	35	TnX107	RDATAx1 / RDATAx33
BIDX0 / BIDX2	TnX71	38	37	TnX108	RDATAx2 / RDATAx34
AWREADYX	TnX70	40	39	TnX109	RDATAx3 / RDATAx35
AWVALIDX / b0	TnX69	42	41	TnX110	RDATAx4 / RDATAx36
AWCACHEX1 / AWCACHEX3	TnX68	44	43	TnX111	RDATAx5 / RDATAx37
AWCACHEX0 / AWCACHEX2	TnX67	46	45	TnX112	RDATAx6 / RDATAx38
AWLOCKX0 / AWLOCKX1	TnX66	48	47	TnX113	RDATAx7 / RDATAx39
AWBURSTX0 / AWBURSTX1	TnX65	50	49	TnX114	RDATAx8 / RDATAx40
AWPROTX0 / AWPROTX1	TnX64	52	51	TnX115	RDATAx9 / RDATAx41
Xx63 (ARM_nRESET)	TnX63	54	53	TnX116	RDATAx10 / RDATAx42
b0 / AWPROTX2	TnX62	56	55	TnX117	RDATAx11 / RDATAx43
AWSIZEX0 / AWSIZEX1	TnX61	58	57	TnX118	RDATAx12 / RDATAx44

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
AWLENX1 / AWLENX3	TnX60	60	59	TnX119	RDATAX13 / RDATAX45
AWLENX0 / AWLENX2	TnX59	62	61	TnX120	RDATAX14 / RDATAX46
AWIDX1 / AWIDX3	TnX58	64	63	TnX121	RDATAX15 / RDATAX47
AWIDX0 / AWIDX2	TnX57	66	65	TnX122	RDATAX16 / RDATAX48
AWADDRX15 / AWADDRX31	TnX56	68	67	TnX123	RDATAX17 / RDATAX49
AWADDRX14 / AWADDRX30	TnX55	70	69	TnX124	RDATAX18 / RDATAX50
AWADDRX13 / AWADDRX29	TnX54	72	71	TnX125	RDATAX19 / RDATAX51
AWADDRX12 / AWADDRX28	TnX53	74	73	TnX126	RDATAX20 / RDATAX52
AWADDRX11 / AWADDRX27	TnX52	76	75	TnX127	RDATAX21 / RDATAX53
AWADDRX10 / AWADDRX26	TnX51	78	77	TnX128	RDATAX22 / RDATAX54
AWADDRX9 / AWADDRX25	TnX50	80	79	TnX129	RDATAX23 / RDATAX55
AWADDRX8 / AWADDRX24	TnX49	82	81	TnX130	RDATAX24 / RDATAX56
AWADDRX7 / AWADDRX23	TnX48	84	83	TnX131	RDATAX25 / RDATAX57
AWADDRX6 / AWADDRX22	TnX47	86	85	TnX132	RDATAX26 / RDATAX58
AWADDRX5 / AWADDRX21	TnX46	88	87	TnX133	RDATAX27 / RDATAX59

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
AWADDRX4 / AWADDRX20	TnX45	90	89	TnX134	RDATAx28 / RDATAx60
AWADDRX3 / AWADDRX19	TnX44	92	91	TnX135	RDATAx29 / RDATAx61
AWADDRX2 / AWADDRX18	TnX43	94	93	TnX136	RDATAx30 / RDATAx62
AWADDRX1 / AWADDRX17	TnX42	96	95	TnX137	RDATAx31 / RDATAx63
AWADDRX0 / AWADDRX16	TnX41	98	97	TnX138	RIDX0 / RIDX2
WREADYX	TnX40	100	99	TnX139	RIDX1 / RIDX3
WVALIDX / b0	TnX39	102	101	TnX140	RRESPX0 / RRESPX1
WLASTX / b0	TnX38	104	103	TnX141	RLASTX / (not connected)
WSTRBX3 / WSTRBX7	TnX37	106	105	TnX142	RVALIDX / (not connected)
WSTRBX2 / WSTRBX6	TnX36	108	107	TnX143	RREADYX
WSTRBX1 / WSTRBX5	TnX35	110	109	TnX144	Xx144
WSTRBX0 / WSTRBX4	TnX34	112	111	TnX145	Xx145
WIDX1 / WIDX3	TnX33	114	113	TnX146	Xx146
WIDX0 / WIDX2	TnX32	116	115	TnX147	Xx147
WDATAx31 / WDATAx63	TnX31	118	117	TnX148	Xx148

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
WDATAx30 / WDATAx62	TnX30	120	119	TnX149	Xx149
WDATAx29 / WDATAx61	TnX29	122	121	TnX150	Xx150
WDATAx28 / WDATAx60	TnX28	124	123	TnX151	Xx151
WDATAx27 / WDATAx59	TnX27	126	125	TnX152	Xx152
WDATAx26 / WDATAx58	TnX26	128	127	TnX153	Xx153
WDATAx25 / WDATAx57	TnX25	130	129	TnX154	Xx154
WDATAx24 / WDATAx56	TnX24	132	131	TnX155	Xx155
WDATAx23 / WDATAx55	TnX23	134	133	TnX156	Xx156
WDATAx22 / WDATAx54	TnX22	136	135	TnX157	Xx157
WDATAx21 / WDATAx53	TnX21	138	137	TnX158	Xx158
WDATAx20 / WDATAx52	TnX20	140	139	TnX159	Xx159
WDATAx19 / WDATAx51	TnX19	142	141	TnX160	Xx160
WDATAx18 / WDATAx50	TnX18	144	143	TnX161	Xx161
WDATAx17 / WDATAx49	TnX17	146	145	TnX162	Xx162
WDATAx16 / WDATAx48	TnX16	148	147	TnX163	Xx163

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
WDATA15 / WDATA47	TnX15	150	149	TnX164	Xx164
WDATA14 / WDATA46	TnX14	152	151	TnX165	Xx165
WDATA13 / WDATA45	TnX13	154	153	TnX166	Xx166
WDATA12 / WDATA44	TnX12	156	155	TnX167	Xx167
WDATA11 / WDATA43	TnX11	158	157	TnX168	Xx168
WDATA10 / WDATA42	TnX10	160	159	TnX169	Xx169
WDATA9 / WDATA41	TnX9	162	161	TnX170	Xx170
WDATA8 / WDATA40	TnX8	164	163	TnX171	Xx171
WDATA7 / WDATA39	TnX7	166	165	TnX172	Xx172
WDATA6 / WDATA38	TnX6	168	167	TnX173	Xx173
WDATA5 / WDATA37	TnX5	170	169	TnX174	Xx174
WDATA4 / WDATA36	TnX4	172	171	TnX175	Xx175
WDATA3 / WDATA35	TnX3	174	173	TnX176	Xx176

Table 5-2 HDRX signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
WDATA _{X2} / WDATA _{X34}	TnX2	176	175	TnX177	Xx177
WDATA _{X1} / WDATA _{X33}	TnX1	178	177	TnX178	Xx178
WDATA _{X0} / WDATA _{X32}	TnX0	180	179	TnX179	Xx179

For a description of the AXI bus signals see *AMBA AXI Protocol Specification* (ARM IHI 0022), *Chapter 2 Signal Descriptions*.

5.1.2 HDRY signals

Table 5-3 on page 5-11 describes the signals on the HDRY pins for the CT1176JZF-S and the baseboard. None of the HDRY pins are utilized by the CT1176JZF-S. The generic HDRY Y bus signals are listed in Table 5-3 on page 5-11 for reference only.

———— **Note** —————

Corresponding pins on the upper and lower headers feed the generic signals through the tile stack.

The signal on the upper header is named YUn and the signal on the lower header is named YLn, the table entry is Yxn. Replace x by L for the signal on the lower header and by U for the signal on the upper header. For example, the pin 1 signal for the lower header is **YL89** and the pin 1 signal for the upper header is **YU89**.

For the EB there are two HDRY headers (tile site 1 and tile site 2). Replace the **TnY** signal prefix in the table by **T1Y** or **T2Y** to get the signal name for tile site 1 or 2 respectively.

Table 5-3 HDRY signals

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Yx90	TnY90	2	1	TnY89	Yx89
Yx91	TnY91	4	3	TnY88	Yx88
Yx92	TnY92	6	5	TnY87	Yx87
Yx93	TnY93	8	7	TnY86	Yx86
Yx94	TnY94	10	9	TnY85	Yx85
Yx95	TnY95	12	11	TnY84	Yx84
Yx96	TnY96	14	13	TnY83	Yx83
Yx97	TnY97	16	15	TnY82	Yx82
Yx98	TnY98	18	17	TnY81	Yx81
Yx99	TnY99	20	19	TnY80	Yx80
Yx100	TnY100	22	21	TnY79	Yx79
Yx101	TnY101	24	23	TnY78	Yx78
Yx102	TnY102	26	25	TnY77	Yx77
Yx103	TnY103	28	27	TnY76	Yx76
Yx104	TnY104	30	29	TnY75	Yx75
Yx105	TnY105	32	31	TnY74	Yx74
Yx106	TnY106	34	33	TnY73	Yx73
Yx107	TnY107	36	35	TnY72	Yx72
Yx108	TnY108	38	37	TnY71	Yx71
Yx109	TnY109	40	39	TnY70	Yx70
Yx110	TnY110	42	41	TnY69	Yx69
Yx111	TnY111	44	43	TnY68	Yx68
Yx112	TnY112	46	45	TnY67	Yx67

Table 5-3 HDRY signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Yx113	TnY113	48	47	TnY66	Yx66
Yx114	TnY114	50	49	TnY65	Yx65
Yx115	TnY115	52	51	TnY64	Yx64
Yx116	TnY116	54	53	TnY63	Yx63
Yx117	TnY117	56	55	TnY62	Yx62
Yx118	TnY118	58	57	TnY61	Yx61
Yx119	TnY119	60	59	TnY60	Yx60
Yx120	TnY120	62	61	TnY59	Yx59
Yx121	TnY121	64	63	TnY58	Yx58
Yx122	TnY122	66	65	TnY57	Yx57
Yx123	TnY123	68	67	TnY56	Yx56
Yx124	TnY124	70	69	TnY55	Yx55
Yx125	TnY125	72	71	TnY54	Yx54
Yx126	TnY126	74	73	TnY53	Yx53
Yx127	TnY127	76	75	TnY52	Yx52
Yx128	TnY128	78	77	TnY51	Yx51
Yx129	TnY129	80	79	TnY50	Yx50
Yx130	TnY130	82	81	TnY49	Yx49
Yx131	TnY131	84	83	TnY48	Yx48
Yx132	TnY132	86	85	TnY47	Yx47
Yx133	TnY133	88	87	TnY46	Yx46
Yx134	TnY134	90	89	TnY45	Yx45
Yx135	TnY135	92	91	TnY44	Yx44
Yx136	TnY136	94	93	TnY43	Yx43

Table 5-3 HDRY signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Yx137	TnY137	96	95	TnY42	Yx42
Yx138	TnY138	98	97	TnY41	Yx41
Yx139	TnY139	100	99	TnY40	Yx40
Yx140	TnY140	102	101	TnY39	Yx39
Yx141	TnY141	104	103	TnY38	Yx38
Yx142	TnY142	106	105	TnY37	Yx37
Yx143	TnY143	108	107	TnY36	Yx36
Yx144	TnY144	110	109	TnY35	Yx35
Yx145	TnY145	112	111	TnY34	Yx34
Yx146	TnY146	114	113	TnY33	Yx33
Yx147	TnY147	116	115	TnY32	Yx32
Yx148	TnY148	118	117	TnY31	Yx31
Yx149	TnY149	120	119	TnY30	Yx30
Yx150	TnY150	122	121	TnY29	Yx29
Yx151	TnY151	124	123	TnY28	Yx28
Yx152	TnY152	126	125	TnY27	Yx27
Yx153	TnY153	128	127	TnY26	Yx26
Yx154	TnY154	130	129	TnY25	Yx25
Yx155	TnY155	132	131	TnY24	Yx24
Yx156	TnY156	134	133	TnY23	Yx23
Yx157	TnY157	136	135	TnY22	Yx22
Yx158	TnY158	138	137	TnY21	Yx21
Yx159	TnY159	140	139	TnY20	Yx20
Yx160	TnY160	142	141	TnY19	Yx19

Table 5-3 HDRY signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Yx161	TnY161	144	143	TnY18	Yx18
Yx162	TnY162	146	145	TnY17	Yx17
Yx163	TnY163	148	147	TnY16	Yx16
Yx164	TnY164	150	149	TnY15	Yx15
Yx165	TnY165	152	151	TnY14	Yx14
Yx166	TnY166	154	153	TnY13	Yx13
Yx167	TnY167	156	155	TnY12	Yx12
Yx168	TnY168	158	157	TnY11	Yx11
Yx169	TnY169	160	159	TnY10	Yx10
Yx170	TnY170	162	161	TnY9	Yx9
Yx171	TnY171	164	163	TnY8	Yx8
Yx172	TnY172	166	165	TnY7	Yx7
Yx173	TnY173	168	167	TnY6	Yx6
Yx174	TnY174	170	169	TnY5	Yx5
Yx175	TnY175	172	171	TnY4	Yx4
Yx176	TnY176	174	173	TnY3	Yx3
Yx177	TnY177	176	175	TnY2	Yx2
Yx178	TnY178	178	177	TnY1	Yx1
Yx179	TnY179	180	179	TnY0	Yx0

For a description of the AXI bus signals see *AMBA AXI Protocol Specification* (ARM IHI 0022), *Chapter 2 Signal Descriptions*.

5.1.3 HDRZ signals

Table 5-4 on page 5-15 describes the signals on the HDRZ pins for the CT1176JZF-S and the baseboard.

Note

Except for the clock and JTAG signals, and **nTILE_DET**, the CT1176JZF-S either has the same signal on the corresponding pin on the upper and lower header or a signal on the lower header only. Where there are different signals on corresponding pins, they are shown in the table with the suffix (U) and (L) to indicate an upper or lower header connection respectively.

The signal on the upper header of the CT1176JZF-S is named **ZUn** and the signal on the lower header is named **ZLn**, the table entry is **Zxn**. Replace **x** by **L** for the signal on the lower header and by **U** for the signal on the upper header. For example, the pin 1 signal for the lower header is **ZL128** and the pin 1 signal for the upper header is **ZU128**.

For the EB there are two HDRZ headers (tile site 1 and tile site 2). Replace the **TnZ** signal prefix in the table by **T1Z** or **T2Z** to get the signal name for tile site 1 or 2 respectively.

Table 5-4 HDRZ signals

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Z255	TnZ255	2	1	TnZ128	Zx128
Z254	TnZ254	4	3	TnZ129	Zx129
Z253	TnZ253	6	5	TnZ130	Zx130
Z252	TnZ252	8	7	TnZ131	Zx131
Z251	TnZ251	10	9	TnZ132	Zx132
Z250	TnZ250	12	11	TnZ133	Zx133
Z249	TnZ249	14	13	TnZ134	Zx134
Z248	TnZ248	16	15	TnZ135	Zx135
Z247	TnZ247	18	17	TnZ136	Zx136
Z246	TnZ246	20	19	TnZ137	Zx137
Z245	TnZ245	22	21	TnZ138	Zx138
Z244	TnZ244	24	23	TnZ139	Zx139
Z243	TnZ243	26	25	TnZ140	Zx140

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Z242	TnZ242	28	27	TnZ141	Zx141
Z241	TnZ241	30	29	TnZ142	Zx142
Z240	TnZ240	32	31	TnZ143	Zx143
Z239	TnZ249	34	33	TnZ144	Zx144
Z238	TnZ248	36	35	TnZ145	Zx145
Z237	TnZ237	38	37	TnZ146	Zx146
Z236	TnZ236	40	39	TnZ147	Zx147
Z235	TnZ235	42	41	TnZ148	Zx148
Z234	TnZ234	44	43	TnZ149	Zx149
Z233	TnZ233	46	45	TnZ150	Zx150
Z232	TnZ232	48	47	TnZ151	Zx151
nWARMRST	TnZ231	50	49	TnZ152	Zx152
PLDCLK	TnZ230	52	51	TnZ153	Zx153
PLDRESETn	TnZ229	54	53	TnZ154	Zx154
PLDD0	TnZ228	56	55	TnZ155	Zx155
PLDD1	TnZ227	58	57	TnZ156	Zx156
ETMEXTOUT	TnZ226	60	59	TnZ157	Zx157
USEROUT3	TnZ225	62	61	TnZ158	Zx158
USEROUT2	TnZ224	64	63	TnZ159	Zx159
USEROUT1	TnZ223	66	65	TnZ160	Zx160
USEROUT0	TnZ222	68	67	TnZ161	Zx161
ETMEXTIN	TnZ221	70	69	TnZ162	Zx162
USERIN3 (SPNIDENX)	TnZ220	72	71	TnZ163	Zx163

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
USERIN2 (SPIDENX)	TnZ219	74	73	TnZ164	Zx164
USERIN1	TnZ218	76	75	TnZ165	Zx165
USERIN0	TnZ217	78	77	TnZ166	Zx166
nCOLDRST	TnZ216	80	79	TnZ167	Zx167
EDBGRQ	TnZ215	82	81	TnZ168	Zx168
IEBKPT	TnZ214	84	83	TnZ169	Zx169
DEWPT	TnZ213	86	85	TnZ170	Zx170
EXTTRIG	TnZ212	88	87	TnZ171	Zx171
COMMTX	TnZ211	90	89	TnZ172	Zx172
COMMRX	TnZ210	92	91	TnZ173	Zx173
BIGENDOUT	TnZ209	94	93	TnZ174	Zx174
STANDBYWFI	TnZ208	96	95	TnZ175	Zx175
DBGACK	TnZ207	98	97	TnZ176	Zx176
nIRQ	TnZ206	100	99	TnZ177	Zx177
nFIQ	TnZ205	102	101	TnZ178	Zx178
PLD_SPARE4	TnZ204	104	103	TnZ179	Zx179
PLD_SPARE3	TnZ203	106	105	TnZ180	Zx180
PLD_SPARE2	TnZ202	108	107	TnZ181	Zx181
PLD_SPARE1	TnZ201	110	109	TnZ182	Zx182
PLD_SPARE0	TnZ200	112	111	TnZ183	Zx183
Zx199 (STNBYWFI3)	TnZ199	114	113	TnZ184	Zx184
Zx198	TnZ198	116	115	TnZ185	Zx185
Zx197	TnZ197	118	117	TnZ186	Zx186
Zx196	TnZ196	120	119	TnZ187	Zx187

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Zx195 (SMPnAMP3)	TnZ195	122	121	TnZ188	Zx188
Zx194 (SMPnAMP2)	TnZ194	124	123	TnZ189	Zx189
Zx193 (SMPnAMP1)	TnZ193	126	125	TnZ190	Zx190
Zx192 (SMPnAMP0)	TnZ192	128	127	TnZ191	Zx191
CLK_POS_DN	CLK_POS_DN_IN	130	129	D_nSRST	D_nSRST
CLK_NEG_DN_IN CLK_NEG_DN_OUT	CLK_NEG_DN_IN	132 (U) 132 (L)	131	D_nTRST	D_nTRST
CLK_POS_UP	CLK_POS_UP_OUT	134	133 (U) 133 (L)	D_TDO_IN	D_TDO_IN D_TDO_OUT
CLK_NEG_UP_OUT CLK_NEG_UP_IN	CLK_NEG_UP_OUT	136 (U) 136 (L)	135	D_TDI	D_TDI
CLK_UP_MINUS2	CLK_UP_THRU	138	137 (U) 137 (L)	D_TCK_OUT	D_TCK_OUT D_TCK_IN
CLK_UP_MINUS1	CLK_OUT_PLUS1	140	139 (U) 139 (L)	D_TMS_OUT	D_TMS_OUT D_TMS_IN
CLK_UP_THRU	CLK_OUT_PLUS2	142	141	D_RTCK	D_RTCK
CLK_DN_PLUS2	CLK_IN_PLUS2	144	143	C_nSRST	C_nSRST
CLK_DN_PLUS1	CLK_IN_PLUS1	146	145	C_nTRST	C_nTRST
CLK_DN_THRU	CLK_DN_THRU	148	147 (U) 147 (L)	C_TDO_IN	C_TDO_IN C_TDO_OUT
CLK_GLOBAL	CLK_GLOBAL	150	149	C_TDI	C_TDI
FPGA_IMAGE	FPGA_IMAGE	152	151 (U) 151 (L)	C_TCK_OUT	C_TCK_OUT C_TCK_IN
nSYSPOR	nSYSPOR	154	153 (U) 153 (L)	C_TMS_OUT	C_TMS_OUT C_TMS_IN
nSYSRST	nSYSRST	156	155 (U) 155 (L)	nTILE_DET	nTILE_DET GND
nRTCKEN	nRTCKEN	158	157	nCFGEN	nCFGEN

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
SPARE12	SPARE12 (reserved)	160	159	GLOBAL_DONE	GLOBAL_DONE
SPARE10	SPARE10 (reserved)	162	161	SPARE11 (reserved)	SPARE11
SPARE8	SPARE8 (reserved)	164	163	SPARE9 (reserved)	SPARE9
SPARE6	SPARE6 (reserved)	166	165	SPARE7 (reserved)	SPARE7
SPARE4	SPARE4 (reserved)	168	167	SPARE5 (reserved)	SPARE5
SPARE2	SPARE2 (reserved)	170	169	SPARE3 (reserved)	SPARE3
SPARE0	SPARE0 (reserved)	172	171	SPARE1 (reserved)	SPARE1
Zx64	TnZ64	174	173	TnZ63	Zx63
Zx65	TnZ65	176	175	TnZ62	Zx62
Zx66	TnZ66	178	177	TnZ61	Zx61
Zx67	TnZ67	180	179	TnZ60	Zx60
Zx68	TnZ68	182	181	TnZ59	Zx59
Zx69	TnZ79	184	183	TnZ58	Zx58
Zx70	TnZ70	186	185	TnZ57	Zx57
Zx71	TnZ71	188	187	TnZ56	Zx56
Zx72	TnZ72	190	189	TnZ55	Zx55
Zx73	TnZ73	192	191	TnZ54	Zx54
Zx74	TnZ74	194	193	vZ53	Zx53
Zx75	TnZ75	196	195	TnZ52	Zx52
Zx76	TnZ76	198	197	TnZ51	Zx51
Zx77	TnZ77	200	199	TnZ50	Zx50
Zx78	TnZ78	202	201	TnZ49	Zx49
Zx79	TnZ79	204	203	TnZ48	Zx48
Zx80	TnZ80	206	205	TnZ47	Zx47

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Zx81	TnZ81	208	207	TnZ46	Zx46
Zx82	TnZ82	210	209	TnZ45	Zx45
Zx83	TnZ83	212	211	TnZ44	Zx44
Zx84	TnZ84	214	213	TnZ43	Zx43
Zx85	TnZ85	216	215	TnZ42	Zx42
Zx86	TnZ86	218	217	TnZ41	Zx41
Zx87	TnZ87	220	219	TnZ40	Zx40
Zx88	TnZ88	222	221	TnZ39	Zx39
Zx89	TnZ89	224	223	TnZ38	Zx38
Zx90	TnZ90	226	225	TnZ37	Zx37
Zx91	TnZ91	228	227	TnZ36	Zx36
Zx92	TnZ92	230	229	TnZ35	Zx35
Zx93	TnZ93	232	231	TnZ34	Zx34
Zx94	TnZ94	234	233	TnZ33	Zx33
Zx95	TnZ95	236	235	TnZ32	Zx32
Zx96	TnZ96	238	237	TnZ31	Zx31
Zx97	TnZ97	240	239	TnZ30	Zx30
Zx98	TnZ98	242	241	TnZ29	Zx29
Zx99	TnZ99	244	243	TnZ28	Zx28
Zx100	TnZ100	246	245	TnZ27	Zx27
Zx101	TnZ101	248	247	TnZ26	Zx26
Zx102	TnZ102	250	249	TnZ25	Zx25
Zx103	TnZ103	252	251	TnZ24	Zx24
Zx104	TnZ104	254	253	TnZ23	Zx23

Table 5-4 HDRZ signals (continued)

Core Tile signals	Baseboard signals	Even pins	Odd pins	Baseboard signals	Core Tile signals
Zx105	TnZ105	256	255	TnZ22	Zx22
Zx106	TnZ106	258	257	TnZ21	Zx21
Zx107	TnZ107	260	259	TnZ20	Zx20
Zx108	TnZ108	262	261	TnZ19	Zx19
Zx109	TnZ109	264	263	TnZ18	Zx18
Zx110	TnZ110	266	265	TnZ17	Zx17
Zx111	TnZ111	268	267	TnZ16	Zx16
Zx112	TnZ112	270	269	TnZ15	Zx15
Zx113	TnZ113	272	271	TnZ14	Zx14
Zx114	TnZ114	274	273	TnZ13	Zx13
Zx115	TnZ115	276	275	TnZ12	Zx12
Zx116	TnZ116	278	277	TnZ11	Zx11
Zx117	TnZ117	280	279	TnZ10	Zx10
Zx118	TnZ118	282	281	TnZ9	Zx9
Zx119	TnZ119	284	283	TnZ8	Zx8
Zx120	TnZ120	286	285	TnZ7	Zx7
Zx121	TnZ121	288	287	TnZ6	Zx6
Zx122	TnZ122	290	289	TnZ5	Zx5
Zx123	TnZ123	292	291	TnZ4	Zx4
Zx124	TnZ124	294	293	TnZ3	Zx3
Zx125	TnZ125	296	295	TnZ2	Zx2
Zx126	TnZ126	298	297	TnZ1	Zx1
Zx127	TnZ127	300	299	TnZ0	Zx0

5.2 Trace Connectors

Trace connectors are provided on the CT1176JZF-S. Use the JTAG connector on the baseboard to provide the JTAG signals that are required for controlling the ETM in the ARM1176JZF-S test chip.

———— **Note** ————

The baseboard trace port cannot be used to trace ARM1176JZF-S execution, you must use the trace connector TRACEA on the CT1176JZF-S when using RealView Trace (RVT).

5.2.1 Trace connector pinout

Table 5-5 and Table 5-6 on page 5-23 list the pinout of the trace connectors J7 (TRACEA) and J8 (TRACEB).
The Mictor® connector (part number AMP 2-767004-2) is shown in Figure 5-2.

———— **Note** ————

Agilent (formerly HP) and Tektronix label these connectors differently, but the assignments of signals to physical pins is appropriate for both systems and pin 1 is always in the same position. The figure is labelled according to the Agilent pin assignment.

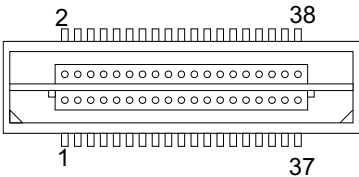


Figure 5-2 AMP Mictor connector

Table 5-5 Trace Port A (TRACEA) connector J7

Trace Port signal	Pin	Pin	Trace Port signal
Not connected	1	2	Not connected
GND	3	4	Not connected
Not connected	5	6	TRACECLKAX

Table 5-5 Trace Port A (TRACEA) connector J7 (continued)

Trace Port signal	Pin	Pin	Trace Port signal
Not connected	7	8	Not connected
Not connected	9	10	EXTTRIGX
Not connected	11	12	VSUPPLYA_R
Not connected	13	14	VTREFA_R
Not connected	15	16	TRACEPKTAX7
Not connected	17	18	TRACEPKTAX6
Not connected	19	20	TRACEPKTAX5
Not connected	21	22	TRACEPKTAX4
TRACEPKTAX15	23	24	TRACEPKTAX3
TRACEPKTAX14	25	26	TRACEPKTAX2
TRACEPKTAX13	27	28	TRACEPKTAX1
TRACEPKTAX12	29	30	TRACEPKTAX0
TRACEPKTAX11	31	32	TRACESYNCA
TRACEPKTAX10	33	34	PIPESTATAX2
TRACEPKTAX9	35	36	PIPESTATAX1
TRACEPKTAX8	37	38	PIPESTATAX0

Table 5-6 Trace Port B (TRACEB) connector J8

Trace Port signal	Pin	Pin	Trace Port signal
Not connected	1	2	Not connected
GND	3	4	Not connected
Not connected	5	6	TRACECLKBX
Not connected	7	8	Not connected
Not connected	9	10	Not connected

Table 5-6 Trace Port B (TRACEB) connector J8 (continued)

Trace Port signal	Pin	Pin	Trace Port signal
Not connected	11	12	VSUPPLYB_R
Not connected	13	14	VTREFB_R
Not connected	15	16	TRACEPKTBX7
Not connected	17	18	TRACEPKTBX6
Not connected	19	20	TRACEPKTBX5
Not connected	21	22	TRACEPKTBX4
TRACEPKTBX15	23	24	TRACEPKTBX3
TRACEPKTBX14	25	26	TRACEPKTBX2
TRACEPKTBX13	27	28	TRACEPKTBX1
TRACEPKTBX12	29	30	TRACEPKTBX0
TRACEPKTBX11	31	32	TRACESYNCBX
TRACEPKTBX10	33	34	PIPESTATBX2
TRACEPKTBX9	35	36	PIPESTATBX1
TRACEPKTBX8	37	38	PIPESTATBX0

5.3 Links, test points, and LED indicators

This section describes the links, test points and LED indicators present on the CT1176JZF-S.

5.3.1 Links

There are several build options available for the CT1176JZF-S. These options are fixed at manufacture by fitting links to the HBI-0154 printed-circuit board. A combination of zero ohm resistor networks and resistors are used.

Figure 5-3 shows the location of the links on the top of the CT1176JZF-S.

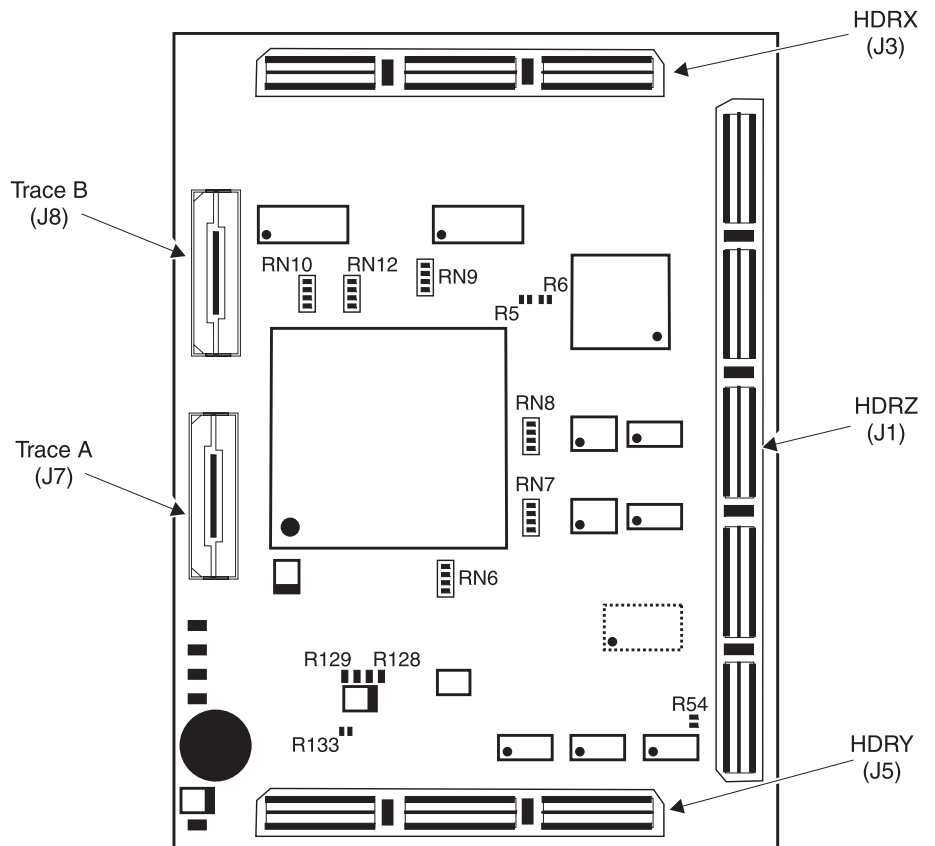


Figure 5-3 Location of links (top)

Figure 5-4 on page 5-26 shows the location of the links on the bottom of the CT1176JZF-S.

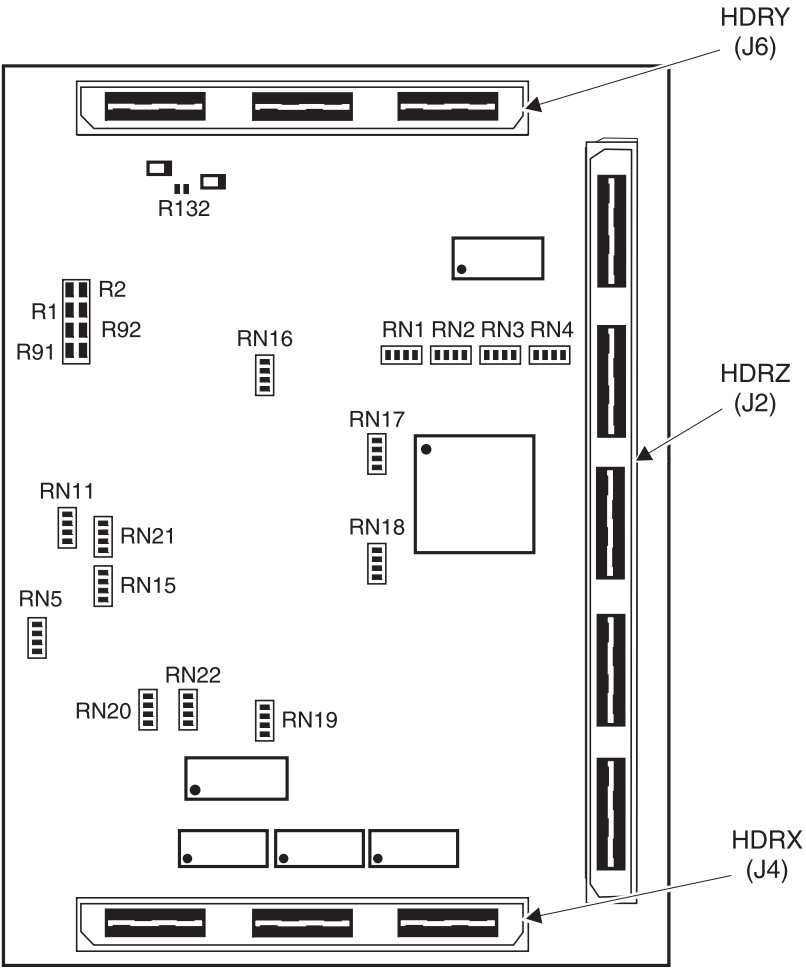


Figure 5-4 Location of links (bottom)

Table 5-7 lists the link default build for the CT1176JZF-S.

The default build provides:

- 3.3V interface from the tile headers to the ARM test chip I/O

Note

Level translator U12 is not fitted for this build.

- ARM1176JZF-S test chip pin compatibility
- JTAG return TCK (**D_RTCK**) enabled during debug.

Table 5-7 Default links

Link	Default Build	Schematic Location
R1, R2	Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
R91, R92	Not Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
R128	Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
R129	Not Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
R132	Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
R133	Not Fitted	CT1156T2F-S / CT1176JZF-S - Power Sheet 7 of 9
RN1 - RN4	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
R5	Not Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
R6	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
RN5, RN6	Not Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
RN15, RN16	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9

Table 5-7 Default links (continued)

Link	Default Build	Schematic Location
RN11. R12	Not Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
RN21, RN22	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
R11	Not Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
R12	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
RN7 - RN10	Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
RN17 - RN20	Not Fitted	CT1156T2F-S / CT1176JZF-S - Test Chip Sheet 3 of 9
R54	Fitted	CT1156T2F-S / CT1176JZF-S - JTAG, Trace and Resets Sheet 6 of 9

Caution

The link information is for reference only.
Removing or adding any of the links may result in damage to the board.

5.3.2 Test points

Figure 5-5 shows the location of test points on the CT1176JZF-S. Table 5-8 on page 5-30 lists the function of the signal at each test point.

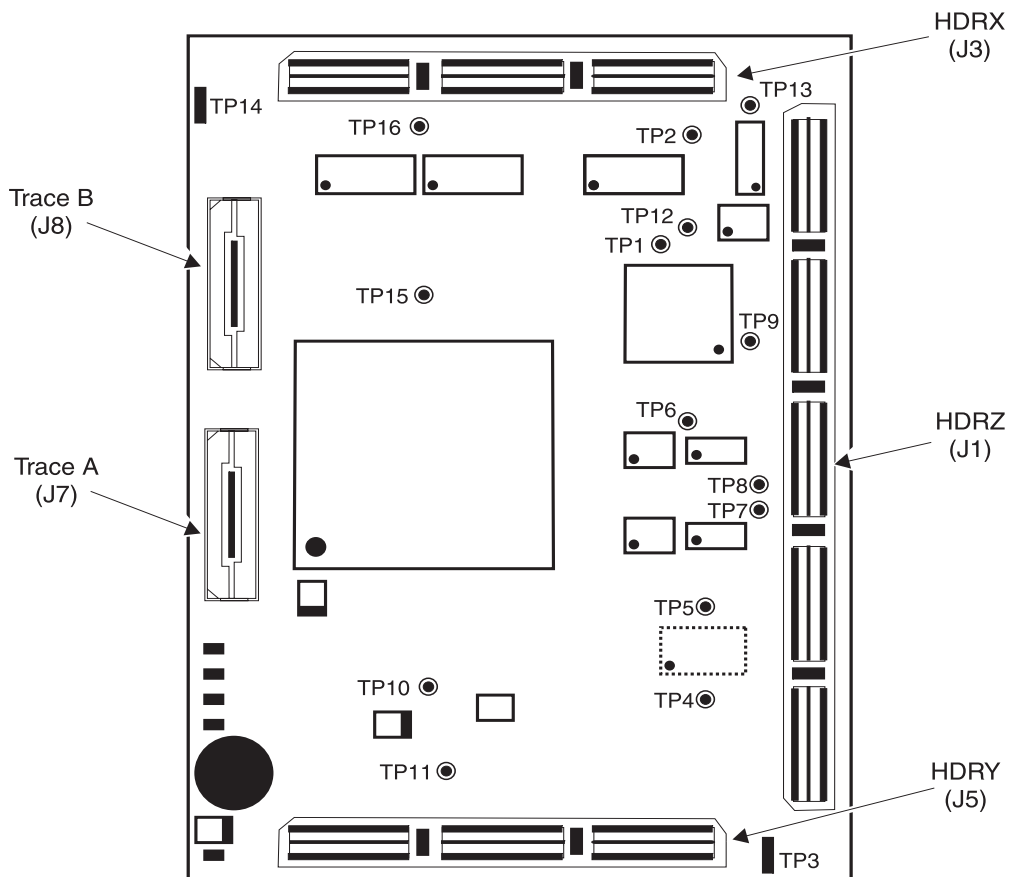


Figure 5-5 Test point location

Table 5-8 Test point signal and description

Test point	Signal	Description
TP1	PLD_TESTPOINT	General purpose testpoint (pin P13 on PLD). Signal being monitored is determined by PLD image.
TP2	REFOUT0	Buffered version of locally generated 24MHz clock, REFCLK24MHZ .
TP3	GND	Ground (0V) reference loop for signal measurements.
TP4	REFCLK	External reference clock to CT1176JZF-S.
TP5	REFCLKX	Level-shifted version of external reference clock for ARM1176JZF-S test chip.
TP6	ACLKX	System clock from ARM1176JZF-S test chip.
TP7	ISP_9A	Buffered ACLKX from Bank 9A of the ispClock5620 clock generator.
TP8	ISP_9B	Buffered ACLKX from Bank 9B of the ispClock5620 clock generator.
TP9	ISP_nLOCK	Lock indicator from the ispClock5620 clock generator.
TP10	VDDCORE1	1V2 supply for ARM1176JZF-S and ETM.
TP11	VDDCORE2	1V0 supply for ARM1176JZF-S test chip and PLL.
TP12	ARM_VDDIO	1V8, 2V5 or 3V3 supply for ARM1176JZF-S test chip IO (set at manufacture).
TP13	1V8	1V8 supply for ARM1176JZF-S test chip PLL analog circuits.
TP14	GND	Ground (0V) reference loop for signal measurements.
TP15	RVALIDX	Demultiplexed AXI bus signal. When HIGH indicates that the required read data is available and the read transfer can complete.
TP16	ARVALIDX_MUX	Multiplexed AXI bus signal. When HIGH indicates that the read address and control information is valid and will remain stable until the address acknowledge signal, ARREADYX is HIGH.

5.3.3 LED indicators

Figure 5-6 shows the location of LED indicators on the CT1176JZF-S. Table 5-9 on page 5-32 lists the function of each LED indicator.

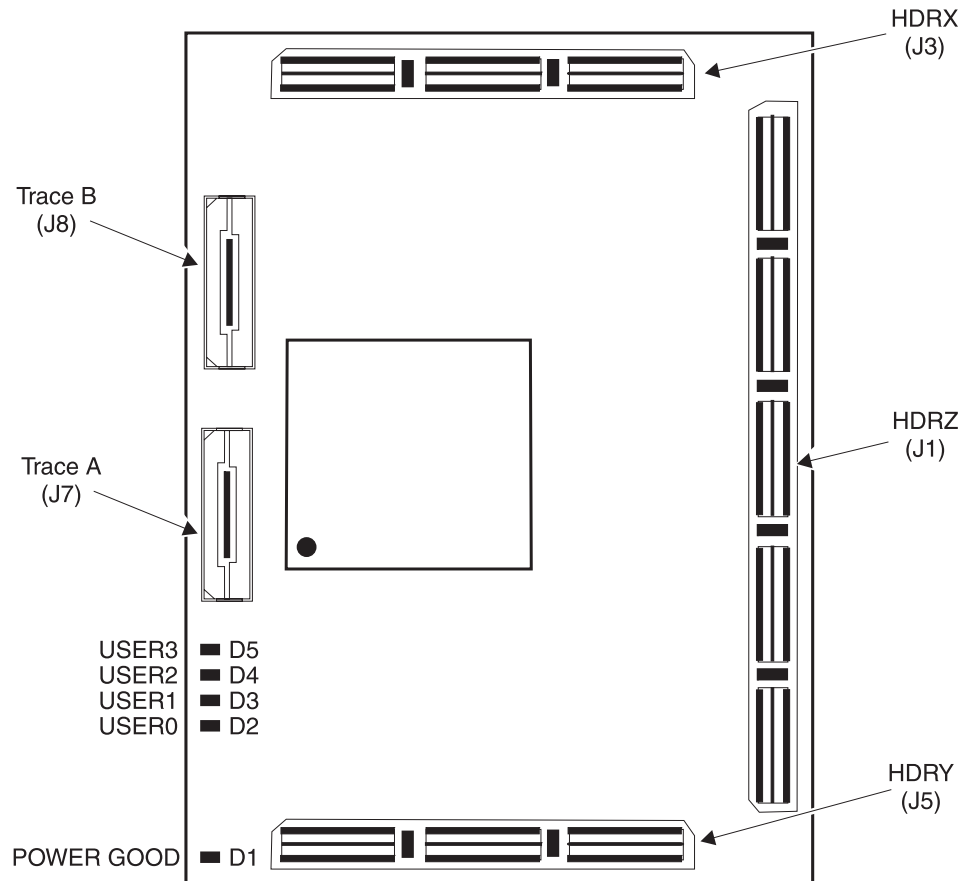


Figure 5-6 LED indicator location

Table 5-9 LED functions

LED	Color	Description
POWER	Green	Indicator is ON when the ARM1176JZF-S test chip VDDCORE1 and ARM_VDDIO power supplies are ON and within tolerance.
USER0	Green	Indicator flashes when the 4-wire serial link is active.
USER1	Green	Indicator is ON when the ARM1176JZF-S test chip PLL and ispClock5620 clock generator PLL are both locked (PLLLOCK is HIGH).
USER2	Green	Indicator is OFF when the system reset to the ARM1176JZF-S test chip is active (nRESETX is LOW).
USER3	Green	Indicator is OFF when the power on reset to the CT1176JZF-S is active (nPORESETX is LOW).

———— **Note** ————

The USER[3:0] LED functions are programmable. The functions listed in Table 5-9 are the default functions pre-programmed by *Application Note* AN177.

————

5.4 AXI bus timing specification

This section describes the timing for the CT1176JZF-S multiplexed AXI system bus.

5.4.1 Core Tile timing and the AMBA 3 AXI Protocol

The worst case timing figures at the CT1176JZF-S headers are shown in Table 5-10 on page 5-35 and Table 5-11 on page 5-36. You must use these figures as a guideline when designing your own boards.

The system bus on RealView Logic Tiles and baseboards is routed between FPGAs. The exact performance of a system depends on the timing parameters of the baseboard and all tiles in the system. Some allowance also has to be made for clock skew, routing delays and number of modules (that is, loading).

Not all Logic Tile or baseboard FPGA implementations meet the ideal timing parameters, due to the complexity of the design or routing congestion within the device. For this reason, the PLL clock generators on baseboards default to a safe low value that all modules can achieve. See the documentation supplied with your baseboard for details on changing the clock frequency.

A detailed timing analysis involves calculating the input/output delays between modules for all timing parameters. In general, the simplest approach to determine the maximum operating frequency is to increase the frequency of the clock generators until the system becomes unstable.

AXI Clock

The AMBA 3 AXI protocol includes a single clock signal, **ACLK**. All input signals are sampled on the rising edge of **ACLK**. All output signal changes must occur after the rising edge of **ACLK**.

There must be no combinatorial paths between input and output signals on both master and slave interfaces.

The CT1176JZF-S clocks are:

ACLKX	This is the external AXI clock from the ARM1176JZF-S test chip. It is the reference clock for the CT1176JZF-S on-board ispClock generator. The ispClock generator controls the AXI port signal multiplexers and distributes the remaining CT1176JZF-S clocks.
PLD_ACLK	This is a buffered version of ACLKX from Bank 8A of the ispClock generator. It is the CT1176JZF-S PLD clock.

REFCLK24MHZ

This clock is generated on-board and is used internally to drive logic in the CT1176JZF-S PLD.

CLK_NEG_UP_OUT

This is a buffered version of **ACLKX** from Bank 7A of the ispClock generator. It is connected to the upper HDRZ header for distribution up the tile stack.

CLK_NEG_DN_OUT

This is a buffered version of **ACLKX** from Bank 7B of the ispClock generator. It is connected to the lower HDRZ header for distribution down the tile stack.

CLK_GLOBAL

This clock is the global system clock. It is provided either by the baseboard or a tile in the tile stack. When provided by the CT1176JZF-S it is a buffered version of **ACLKX** from Bank 6A of the ispClock generator. It is connected to the upper and lower HDRZ headers for distribution up and down the tile stack.

AXI Reset

The AMBA 3 AXI protocol includes a single active LOW reset signal, **ARESETn**. The reset signal can be asserted asynchronously, but deassertion must be synchronous after the rising edge of **ACLK**.

Note

nPORESETX is the CT1176JZF-S global AXI reset (**ARESETn**).

During reset the following interface requirements apply:

- a master interface must drive **ARVALID**, **AWVALID**, and **WVALID** LOW
- a slave interface must drive **RVALID** and **BVALID** LOW.

All other signals can be driven to any value.

A master interface must begin driving **ARVALID**, **AWVALID**, or **WVALID** HIGH only at a rising **CLK_GLOBAL** edge after **nPORESETX** is HIGH.

5.4.2 Timing parameters

The following timings are based on the grouped delays for the CT1176JZF-S. They include the test chip input and output delay, and the delay due to the AXI bus multiplexing.

Note

The timings do not include the skew between **ACLKX** and **CLK_GLOBAL**. This delay is controlled by the on-board programmable ispClock5620 clock generator and is dependant on the baseboard used.

Table 5-10 shows the Global timing parameters.

Table 5-10 Global timing parameters

Parameter	Description	Max
T_{clk}	CLK_GLOBAL clock frequency	35MHz

The CT1176JZF-S uses a multiplexed AXI bus. Figure 5-7 shows the CT1176JZF-S multiplexed AXI bus input setup timing.

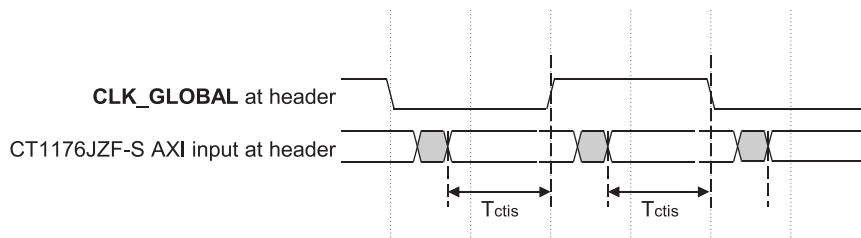


Figure 5-7 CT1176JZF-S multiplexed AXI bus input setup timing

T_{ctis} Input setup to clock

This is the longest time that the CT1176JZF-S requires a valid AXI bus signal level to be presented at the Core Tile header before a rising or falling edge of **CLK_GLOBAL**.

Figure 5-8 on page 5-36 shows the CT1176JZF-S multiplexed AXI bus output valid timing.

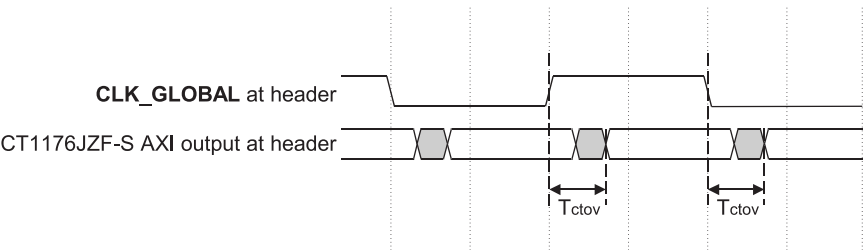


Figure 5-8 CT1176JZF-S multiplexed AXI bus output valid timing

T_{ctov} Core Tile output valid after clock

This is the longest delay between a rising or falling edge of **CLK_GLOBAL** and a valid AXI bus output signal level arriving at the CT1176JZF-S header.

Table 5-11 shows the CT1176JZF-S AXI bus worst case timings when characterized for a slow process, a **VDDCORE** voltage of 1.1V, and a core temperature of 85°C.

Table 5-11 CT1176JZF-S multiplexed AXI bus timing parameters

Parameter	Description	Max
T _{ctis}	Input setup time to either edge of CLK_GLOBAL	9.9ns
T _{ctov}	Output valid time from either edge of CLK_GLOBAL	10.5ns

Appendix A

Specifications

This appendix contains the specifications for the CT1176JZF-S. It contains the following sections:

- *Electrical specification* on page A-2
- *Mechanical details* on page A-5.

———— **Note** —————

See *AXI bus timing specification* on page 5-33 for the timing specifications for Core Tiles that use the HBI-0154 board.

—————

A.1 Electrical specification

This section provides details of the voltage and current characteristics for the CT1176JZF-S.

A.1.1 Bus interface characteristics

Table A-1 shows the Core Tile electrical characteristics for the 3V3 system bus interface. The CT1176JZF-S uses 3.3V and 5V sources.

Table A-1 Core Tile interface electrical characteristics at 3.3V				
Symbol	Description	Min	Max	Unit
3V3	Supply voltage (interface signals)	3.0	3.6	V
5V	Supply voltage (regulators)	4.75	5.25	V
V _{IH}	High-level input voltage	2.0	3.6	V
V _{IL}	Low-level input voltage	0	0.8	V
V _{OH}	High-level output voltage	2.4	-	V
V _{OL}	Low-level output voltage	-	0.4	V
C _{IN}	Input capacitance	-	20	pF

Table A-2 shows the Core Tile electrical characteristics for the 2.5V system bus interface. The CT1176JZF-S uses 3.3V and 5V sources.

Table A-2 Core Tile interface electrical characteristics at 2.5V				
Symbol	Description	Min	Max	Unit
3V3	Supply voltage (interface signals)	3.0	3.6	V
5V	Supply voltage (regulators)	4.75	5.25	V
V _{IH}	High-level input voltage	1.7	-	V
V _{IL}	Low-level input voltage	-	0.7	V
V _{OH}	High-level output voltage	1.7	-	V
V _{OL}	Low-level output voltage	-	0.4	V
C _{IN}	Input capacitance	-	20	pF

Note

V_{OH} is measured at $I_{OH} = -8\text{mA}$ and **ARM_VDDIO** = 2.3V.

V_{OL} is measured at $I_{OL} = -8\text{mA}$ and **ARM_VDDIO** = 2.3V.

Table A-3 shows the Core Tile electrical characteristics for the 1.8V system bus interface. The CT1176JZF-S uses 3.3V and 5V sources.

Table A-3 Core Tile interface electrical characteristics at 1.8V

Symbol	Description	Min	Max	Unit
3V3	Supply voltage (interface signals)	3.0	3.6	V
5V	Supply voltage (regulators)	4.75	5.25	V
V_{IH}	High-level input voltage	1.2	-	V
V_{IL}	Low-level input voltage	-	0.6	V
V_{OH}	High-level output voltage	1.3	-	V
V_{OL}	Low-level output voltage	-	0.3	V
C_{IN}	Input capacitance	-	20	pF

Note

V_{OH} is measured at $I_{OH} = -2\text{mA}$ and **ARM_VDDIO** = 1.6V.

V_{OL} is measured at $I_{OL} = -2\text{mA}$ and **ARM_VDDIO** = 1.6V.

A.1.2 Current requirements

Table A-4 shows current requirements measured at room temperature and nominal voltage.

Apart from the ARM_VDDIO regulator, all power regulators are powered from the 5V supply. Board interface logic levels are defined at manufacture. The interface logic is either powered from the 3V3 supply directly, or from the on board ARM_VDDIO regulator that regulates the 3V3 supply to either 2V5 or 1V8.

Table A-4 Typical current requirements

Component	VDDCORE1 (1V2)	VDDCORE2 (1V0)	AVDD (1V8)	ARM_VDDIO or 3V3 Supply (1V8, 2V5 or 3V3)	3V3 supply
ARM1176JZF-S core	120mA	-	-	-	-
ETM11CS core	30mA	-	-	-	-
Test chip logic	-	45mA	-	-	-
Control PLD core	-	-	100µA	-	-
ARM1176JZF-S I/O, Control PLD I/O (3 banks) and Mux logic	-	-	-	1A at 3V3	-
Control PLD I/O (1 bank) ADC, DAC and logic	-	-	-	-	250mA

————— **Note** —————

The current requirements shown are typical and are dependant on the application being run and are 50mA for the external 5V supply and 1.25A for the external 3V3 supply.

A.2 Mechanical details

Figure A-1 shows the mechanical outline of the CT1176JZF-S.

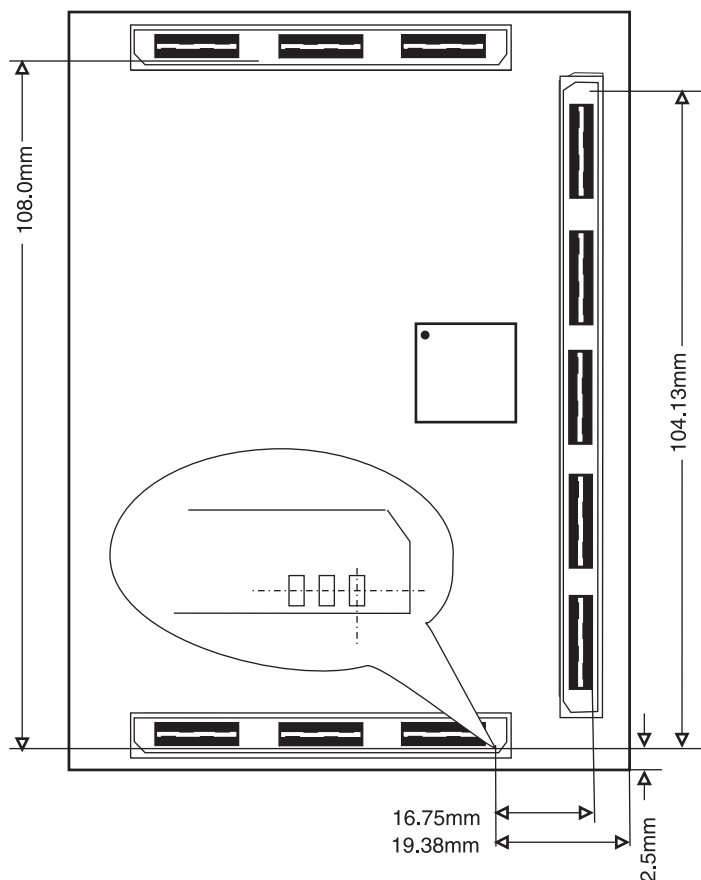


Figure A-1 Board outline (bottom view)

Note

To ensure accurate connector placement you should refer to the CT1176JZF-S Gerber files.

PCB data for the CT1176JZF-S is available from ARM Technical Support at:
www.arm.com/support/downloads/versatile.html

Glossary

This glossary lists all the abbreviations used in the User Guide.

ASIC	Application Specific Integrated Circuit.
ADC	Analog to Digital Converter. A device that converts an analog signal into digital data.
AHB	Advanced High-performance Bus. An ARM open standard bus protocol.
AMBA 3	Advanced Microcontroller Bus Architecture version 3.
AXI	AMBA 3 Advanced eXtensible Interface. An ARM open standard bus protocol.
BIST	Built In Self Test
DAC	Digital to Analog Converter. A device that converts digital data into analog level signals.
EB	RealView Emulation Board. A hardware platform used for system prototyping and debugging of ARM microprocessors.
FPGA	Field Programmable Gate Array.
ICE	In Circuit Emulator. A interface device for configuring and debugging processor cores.
I/O	Input/Output.

JTAG	Joint Test Action Group. The committee which defined the IEEE test access port and boundary-scan standard.
LED	Light Emitting Diode.
Multi-ICE	Equipment for running and controlling a JTAG interface for system debug. This is legacy JTAG equipment. Does not support the ARM1176JZF-S processor.
PCI	Peripheral Component Interconnect. A circuit board level bus interconnect.
PISMO	Memory specification for plug in memory modules.
PLD	Programmable Logic Device.
PLL	Phase-Locked Loop. A type of programmable oscillator that tracks the input frequency and can generate arbitrary multiples or divisions of the input frequency.
RAM	Random Access Memory.
RVI	RealView ICE. Equipment for running and controlling a JTAG interface for system debug. This is current JTAG equipment. Supports the ARM1176JZF-S processor.
TCM	Tightly Coupled Memory, a fast memory block that connects directly to a dedicated I/O port on the processor.
USB	Universal Serial Bus. Hardware interface for connecting peripheral devices.