ARM PrimeCell
PL340 AXI Memory Controller
Errata Notice

This document contains all errata known at the date of issue in releases from revision r1p0 up to and including revision r3p0

Errata present in prior revisions of the IP are detailed in earlier revisions of the document.

Proprietary notice

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Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

10 Sep 2008: Changes in Document v12

Page	Status	ID	Cat	Summary
19	Updated	520613	Cat 2	Same row opened in two different RDBs of an NVM memory device
18	Updated	493218	Cat 2	Potential deadlock when 2 AXI transactions are allocated the same NVM RDB, but have different rows

01 Sep 2008: Changes in Document v11

Page	Status	ID	Cat	Summary
19	New	520613	Cat 1	Same row opened in two different RDBs of an NVM memory device
18	New	493218	Cat 1	Potential deadlock when 2 AXI transactions are allocated the same NVM RDB, but have different rows
29	New	497767	Cat 3	MRS entry incorrectly updates bank bits
31	New	579015	Cat 3	AUTOREFRESH generated while in PAUSED state may cause wake-up with tXSR violation when coincident with SLEEP command
30	New	500213	Cat 3	tRC parameter not implemented as delay between ACTIVE-AUTOREFRESH command
32	New	583771	Cat 3	DMC may not enter self refresh mode via auto self-refresh

04 Jan 2008: Changes in Document v10

Page	Status	ID	Cat	Summary
15	Updated	484165	Cat 2	Auto power down de-asserts CKE while banks not idle
14	Updated	481517	Cat 2	tCKE restriction is only enforced for 1 cycle in power down mode
17	New	489913	Cat 2	For NVM Config only - RAB status tracking may not match NVM memory status after a low power request
16	New	489770	Cat 2	tESR of more than one is not supported for Auto self refresh.
22	Updated	463565	Cat 3	At least one NOP command should be sent when exiting clock stop mode
21	Updated	413776	Cat 3	Manager FSM does not move to low-power state through active pause command
24	Updated	484817	Cat 3	tXP violation when disabling auto_power_down
23	Updated	469863	Cat 3	Write address issue on configurations with memory interface type 4
26	Updated	485872	Cat 3	Limitation of simultaneous DPD and self refresh modes of operations of SDRAM
25	Updated	484963	Cat 3	Potential read data error for combined memory interface in SDR mode
28	New	489914	Cat 3	Setting t_wtr less than t_wr gives timing violations
34	Updated	413769	Doc	Incorrect table name in DDI0331D TRM
33	Updated	402617	Doc	TRM has incorrect naming in Figure 2-15
36	Updated	442622	Doc	Correction to auto self-refresh entry delay in Fig 2-24 of DDI0331E TRM
35	Updated	442486	Doc	Register reset value and field width corrections in DDI0331E TRM

41	Updated	484413	Doc	Table 2-4 has incorrect naming for system state 11 in DDI0331E TRM
40	Updated	484364	Doc	Restriction with auto self-refresh and global CKE in DDI0031E TRM
39	Updated	460267	Doc	Incorrect power down sequence in DDI0331E TRM
38	Updated	459965	Doc	aclk domain state diagram errors in DDI0331E TRM
37	Updated	454320	Doc	Incorrect description of mclkn signal in Table A-1 in DDI0331E TRM

21 Dec 2007: Changes in Document v9

Page	Status	ID	Cat	Summary
15	Updated	484165	Cat 2	Auto power down de-asserts CKE while banks not idle
26	New	485872	Cat 3	Limitation of simultaneous DPD and self refresh modes of operations of SDRAM

13 Dec 2007: Changes in Document v8

Page	Status	ID	Cat	Summary
15	New	484165	Cat 2	Auto power down de-asserts CKE while banks not idle
14	New	481517	Cat 2	tCKE restriction is only enforced for 1 cycle in power down mode
22	New	463565	Cat 3	At least one NOP command should be sent when exiting clock stop mode
21	Updated	413776	Cat 3	Manager FSM does not move to low-power state through active pause command
24	New	484817	Cat 3	tXP violation when disabling auto_power_down
23	New	469863	Cat 3	Write address issue on configurations with memory interface type 4
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34	Updated	413769	Doc	Incorrect table name in DDI0331D TRM
33	Updated	402617	Doc	TRM has incorrect naming in Figure 2-15
36	New	442622	Doc	Correction to auto self-refresh entry delay in Fig 2-24 of DDI0331E TRM
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41	New	484413	Doc	Table 2-4 has incorrect naming for system state 11 in DDI0331E TRM
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39	New	460267	Doc	Incorrect power down sequence in DDI0331E TRM
38	New	459965	Doc	aclk domain state diagram errors in DDI0331E TRM
37	New	454320	Doc	Incorrect description of mclkn signal in Table A-1 in DDI0331E TRM

21 May 2007: Changes in Document v7

Page	Status	ID	Cat	Summary
21	New	413776	Cat 3	Manager FSM does not move to low-power state through active pause command
34	New	413769	Doc	Incorrect table name in TRM
33	Updated	402617	Doc	TRM has incorrect naming in Figure 2-15

28 Sep 2006: Changes in Document v6

Page	Status	ID	Cat	Summary
33	New	402617	Doc	TRM has incorrect naming in Figure 2-15

14 Aug 2006: Changes in Document v5

History of closed defects retained for information purposes only. For information on any of these defects please see PL340-RLNC-000184 v6.0 (PL340-DC-11001-r1p0-00rel0)

Page	Status	ID	Cat	Summary
N/A	New	400912	Cat 2	Arbiter can cause lock up if a qos_min transaction has non-qos_min dependancy's
N/A	New	400907	Cat 3	QOS_override setting can be missed or applied to wrong transaction
N/A	Updated	400134	Cat 2	tRFC violation when entering low-power mode
N/A	New	395374	Cat 3	Minimum-latency QoS is not enabled with QoS-Enable
N/A	Updated	365763	Doc	DDI0331C DMC TRM is missing EBI interface signal descriptions.
N/A	Updated	339892	Doc	TRM has wrong description for read/write conditions for some APB registers

03 Aug 2006: Changes in Document v4

Page	Status	ID	Cat	Summary
N/A	New	400134	Cat 2	tRFC violation when entering low-power mode
N/A	New	365763	Doc	DDI0331C DMC TRM is missing EBI interface signal descriptions.

01 Nov 2005: Changes in Document v3

Page	Status	ID	Cat	Summary
N/A	New	364096	Cat 2	WDATA FIFO can underflow causing incorrect data to be written

22 Sep 2005: Changes in Document v2

Page	Status	ID	Cat	Summary
N/A	New	350351	Cat 2	Incorrect operation when aclk and mclk are synchronous and aclk is faster than mclk
N/A	New	350352	Cat 2	Starting the memory clock after a period of inactivity does not conform to the JEDEC specification
N/A	New	350353	Cat 3	Issue with the AXI-C interface when the PL340 is in Config state

27 May 2005: Changes in Document v1

Page	Status	ID	Cat	Summary
N/A	New	350403	Cat 2	Exclusive accesses may incorrectly appear successful
N/A	New	345003	Doc	Error in TRM diagram label
N/A	New	343402	Cat 3	Auto-refresh commands may still be issued while device is entering LOW POWER state
N/A	New	342653	Cat 3	Disabling auto power down mode while the DMC is in power down mode
N/A	New	340242	Doc	Incorrect Document ref to AMBA 3.0 APB spec
N/A	New	339892	Doc	TRM has wrong description for read/write conditions for some APB registers

N/A	New	339140	Cat 2	Exclusive accesses incorrect when store is bigger than load
N/A	New	338366	Cat 2	EBI interface can release EBIREQ when data bus is not idle
N/A	New	337663	Doc	TRM incorrectly references AMBA AXI Protocol Specification
N/A	New	333851	Doc	Memory Controller Status Register error in TRM
N/A	New	331765	Cat 2	Incorrect Behaviour of EBI interface
N/A	New	331762	Cat 3	Paused state can be entered when the PL340 is not quiescent
N/A	New	331739	Doc	TRM: Incorrect PERIPH_ID values listed for part in table 3-26 and 3-27
N/A	New	329208	Cat 3	Unnecessary cycle of delay added following an activate command
N/A	New	329206	Cat 3	Inefficient arbitration
N/A	New	328245	Doc	Update table 1-3 with values
N/A	New	328053	Cat 2	Incorrect gray encoding in FIFOs for asynchronous operation

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r1p0-00rel0	r2p0-00rel0	r3p0-00rel0
481517	Cat 2	tCKE restriction is only enforced for 1 cycle in power down mode		X	
484165	Cat 2	Auto power down de-asserts CKE while banks not idle		X	X
489770	Cat 2	tESR of more than one is not supported for Auto self refresh.		X	X
489913	Cat 2	For NVM Config only - RAB status tracking may not match NVM memory status after a low power request			X
493218	Cat 2	Potential deadlock when 2 AXI transactions are allocated the same NVM RDB, but have different rows			X
520613	Cat 2	Same row opened in two different RDBs of an NVM memory device			X
413776	Cat 3	Manager FSM does not move to low-power state through active pause command	X		
463565	Cat 3	At least one NOP command should be sent when exiting clock stop mode		X	X
469863	Cat 3	Write address issue on configurations with memory interface type 4		X	
484817	Cat 3	tXP violation when disabling auto_power_down		X	
484963	Cat 3	Potential read data error for combined memory interface in SDR mode		X	X
485872	Cat 3	Limitation of simultaneous DPD and self refresh modes of operations of SDRAM		X	X
489914	Cat 3	Setting t_wtr less than t_wr gives timing violations	X	X	X
497767	Cat 3	MRS entry incorrectly updates bank bits			X
500213	Cat 3	tRC parameter not implemented as delay between ACTIVE-AUTOREFRESH command	X	X	X
579015	Cat 3	AUTOREFRESH generated while in PAUSED state may cause wake-up with tXSR violation when coincident with SLEEP command	X	X	X
583771	Cat 3	DMC may not enter self refresh mode via auto self-refresh		X	X
402617	Doc	TRM has incorrect naming in Figure 2-15	X		
413769	Doc	Incorrect table name in DDI0331D TRM	X		
442486	Doc	Register reset value and field width corrections in DDI0331E TRM		X	

ID	Cat	Summary of Erratum	r1p0-00rel0	r2p0-00rel0	r3p0-00rel0
442622	Doc	Correction to auto self-refresh entry delay in Fig 2-24 of DDI0331E TRM		X	
454320	Doc	Incorrect description of mclkn signal in Table A-1 in DDI0331E TRM		X	
459965	Doc	aclk domain state diagram errors in DDI0331E TRM		X	
460267	Doc	Incorrect power down sequence in DDI0331E TRM		X	
484364	Doc	DDI0331E PL340 r2p0 TRM - Restriction with auto self-refresh and global CKE		X	X
484413	Doc	DDI0331E PL340 r2p0 TRM - Table 2-4 has incorrect naming for System state 11		X	X

Errata - Category 1

Errata - Category 2

481517: tCKE restriction is only enforced for 1 cycle in power down mode

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

The JEDEC standard specifies a timing parameter tCKE, which is defined as the minimum allowed time a device can spend in power down mode.

For some devices, this parameter is 2 cycles. The PL340 only enforces a minimum of 1 cycle.

Implications

If the PL340 controller is used with a device that requires tCKE=2, and the auto power down feature is enabled, the tCKE restriction will potentially be violated.

This could cause data corruption in the memory.

Workaround

To ensure safe operation, disable the auto power down feature using the auto_power_down bit of the memory configuration register.

484165: Auto power down de-asserts CKE while banks not idle

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

This defect applies when the configuration option "global cke" is chosen with multiple chip selects.

The power down finite state machine inspects the bank idle flags from the bank finite state machines. This is designed to prevent the controller from de-asserting CKE when all banks are not idle.

However, the bank idle flags are not being considered correctly in the auto power down logic. Hence, the auto power down logic may de-assert CKE when the banks are not idle.

This defect can be observed when some but not all banks are idle and there is nothing being arbitrated.

Implications

When auto power down is enabled, it is possible for the controller to de-assert CKE when all banks are not idle.

Workaround

The failure mode can be prevented by programming the memory configuration register to either:

1. disable the auto power down feature.
2. if using a single-chip or multi-chip configuration with active_chips=chips then set power_down_prd > tRCD+1
3. if using a multi-chip configuration with some inactive chips then set power_down_prd > tXSR+1

489770: tESR of more than one is not supported for Auto self refresh.

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

For PL340 configurations that support the auto self refresh entry functionality and have sr_enable set, then when self refresh is entered via the auto self refresh logic no timing of the t_esr parameter is carried out.

This only affects memory devices that conform to JEDEC specification and require a self-refresh time of tRFC or greater.

Implications

For memory devices that require tCKE value to be 2 or higher, PL340 may violate their tCKE timing requirements after auto self-refresh entry.

Workaround

Disable the auto self refresh functionality.

489913: For NVM Config only - RAB status tracking may not match NVM memory status after a low power request

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r3p0-00rel0, Open.

Description

This defect applies to NVM configurations only.

When the PL340 enters Low_power mode after a request from either the AXI-C channel interface or via the APB interface, if there are any memory devices that have an open row then a PRECHARGEALL command is sent to all LPDDR devices before self refresh is entered.

This command although not sent to the NVM devices updates the status of the RAB tracking indicating that all RAB's have valid PRE-ROW information.

Implications

The consequences of this are:

1. A simulation may lock up if an RAB is flagged as open when previously no RAB has open and the stored row is still uninitialised.

2. Silicon may flag a "prerow" as being open when in fact it isn't. Therefore it may be possible to activate an RDB with no written or incorrect RAB value.

Workaround

Whenever the Low_power state is entered, either via the APB interface or via the AXI-C channel, a nvm_clr_rab command to the Row Cache Invalidation Register via the APB interface is required before exiting the SLEEP state to ensure coherency is maintained between the row cache state tracker and the NVM memory devices.

493218: Potential deadlock when 2 AXI transactions are allocated the same NVM RDB, but have different rows

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r3p0-00rel0, Open.

Description

If an AXI transaction increments out of one page into the next page then the queue entry for the transaction will request re-allocation of a RDB. A deadlock situation can occur if a new transaction queue entry is received and:

1. The row of the new transaction matches the current page of the RDB that is allocated to the incrementing transaction.

2. Neither the incrementing transaction or new transaction are arbitrated and open their row.

3. The two transactions have different AXI IDs.

The end result of this sequence of events is that the bank will be allocated to two transactions entries at the same time with different page addresses. These transaction entries will compete to open their row causing deadlock in the controller.

Implications

The two entries allocated the same row will be alternatively arbitrated sending out a sequence of competing memory operations trying to open their respective rows causing the controller to deadlock.

Workaround

None, however if NVM support is required then contact support-primecell@arm.com as an RTL fix does exist.

520613: Same row opened in two different RDBs of an NVM memory device

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 2, Present in: r3p0-00rel0, Open.

Description

In a remote scenario, a low priority NVM read request may have its RDB allocated to a higher priority request. It will then be re-allocated a new RDB. Before the higher priority request can open its row the lower priority request may be increased in priority ahead of the previously higher priority request. This request will then be arbitrated into the cmdfmt and end up opening the same row in another RDB.

This can't happen between entries with the same ID as a hazard would prevent the later command being arbitrated. Therefore if there is only one thread of single ID transactions then this scenario can't exist.

If queue entries don't increment out of an RDB then this scenario can't happen as re-allocation will never be required for any entries.

Implications

It may be possible for two RDBs of an NVM memory device to contain the same row. Although the internal status tracking of the PL340 will prevent any data incoherency problems the Jedec protocol will have been violated.

Workaround

None

Errata - Category 3

413776: Manager FSM does not move to low-power state through active pause command

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r1p0-00rel0, Fixed in r2p0-00rel0.

Description

If PL340 was moved to the Pause state through the Active Pause command, then issuing a Sleep command may not move PL340 into Low Power state. If there are any outstanding transaction within the PL340 it stays in Paused state.

Implications

This reliably stops the user from moving the PL340 into Low Power state and changing the configuration of PL340 and the memory until the arbiter is empty.

Instead now the Pause command has to be used to move the controller into Pause state and then into Low Power state, to reprogram the memory controller and the memory. This takes more time than using Active Pause command to move the controller into Pause state and then into Low Power state. This is because in the latter case, the arbiter queue need not be emptied.

Workaround

Always enter the PAUSE state using the Pause command instead of the Active Pause command.

463565: At least one NOP command should be sent when exiting clock stop mode

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

The JEDEC spec for LPDDR states that at least one NOP command must be sent after exiting clock stop mode before another command can be issued to the memory. It is possible to program the PL340 to not provide this extra NOP cycle if both the statements below are true:

1. stop_mem_clock is enabled.

2. auto_power_down is not enabled or auto_power_down is enabled but t_XP is set to zero.

Implications

Memory devices that strictly follow the JEDEC spec may show undefined behaviour.

Workaround

Disable dynamic clock stop functionality or enable auto_power_down mode.

469863: Write address issue on configurations with memory interface type 4

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

This defect occurs for configurations of PL340 with memory type set to 4, i.e. combined memory support (LP)DDR or SDR and for the following conditions:

1. Memory type is set to SDR

2. AXI width is less than or equal to the memory width

The AXI write logic incorrectly merges write data to the effective memory width of DDR instead of SDR and therefore write data can be lost.

The RTL is rendered using the effective memory width of DDR to determine when to check for write data manipulation in the write merge logic. However, when programmed for SDR operation the effective memory width is half of that of DDR hence the problem occurs.

Implications

Write data may not be correctly written to SDR.

Workaround

None

484817: tXP violation when disabling auto_power_down

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

The auto power down feature allows the memory to be placed into power down mode following a period of inactivity.

The timing parameter tXP governs the delay between exiting a power down state and the first command made to the memory.

If the auto power down feature is disabled whilst the memory is in power down state, then the command that causes the exit from power down does not observe the tXP restriction.

Implications

If the auto power down feature has been enabled, and is subsequently disabled whilst in CONFIG state, then unless the User issues a NOP via the direct command register the next command will violate tXP.

Workaround

There are a number of potential workarounds:

1. Leave auto power down disabled/enabled
2. Only disable auto power down in LOW_POWER state
3. Issue a NOP after having disabled auto power down

484963: Potential read data error for combined memory interface in SDR mode

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

For combined pad interfaces (memory interface type 4), when a long write burst to SDR devices is made that is terminated by a read command, the read command could return incorrect data.

This is because **DQM** may go to 1 for a read data beat instead of 0 if the following condition occurs:
`((number of requested write beats) + tWTR + 1) > Burst length`

Implications

Under the conditions described in the "Description" section, incorrect read data can be returned.

Workaround

If you intend to use a SDR SDRAM that uses DQM for read bursts as an output enable, then to guarantee no read data errors:

1. Ensure all AXI write data bursts align to the programmed memory burst.
2. Program the memory burst length to be less than (tWTR + 1 + minimum possible write burst).

485872: Limitation of simultaneous DPD and self refresh modes of operations of SDRAM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

There is a usage case where a DMC configuration may support multiple chip selects but an operating mode may have the most significant chip selects in Deep Power Down Mode.

In this instance a DMC SLEEP command will put the active chip(s) into self refresh mode correctly but will not enter the DMC into the SLEEP state and will not update the Memory Controller Status Register.

Implications

The operating state of the memory controller and status register will not correctly match the state of the active SDRAM chip selects.

Workaround

If this behaviour is required it can be achieved by ensuring that before the DMC is requested to enter SLEEP mode the DMC is previously set to have the chip selects active. Note that this has to be set in the CONFIG state. The sequence from the READY state required is:

Set PAUSE

Set CONFIG

Set Active chips to enable all chips

Send NOP to wake up all chip selects that had been in DPD mode.

Set GO

Set PAUSE

Set SLEEP

To wake up the DMC and put chip selects back into DPD mode:

Set WAKEUP

Set CONFIG

Set DPD direct command to put all required chips back into DPD mode

Set Active Chips to the required number

Set GO

Alternatively for configurations that have auto self refresh then chip selects can be put into deep power down mode and active chip selects will automatically enter self refresh mode whenever that chip has been idle for the auto_power_down time. Note that this power down timeout can be extended with the prescaler counter.

489914: Setting t_wtr less than t_wr gives timing violations

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r1p0-00rel0,r2p0-00rel0,r3p0-00rel0, Open.

Description

PL340 uses the t_wtr timing parameter to determine when it is legal to stop the clock after a write. However, the t_wr parameter for each chip select should be used.

Implications

If t_wtr value is programmed to be less than t_wr, then PL340 may stop the clock sooner than required by the memory device specification and hence violates the device's timing requirements.

Workaround

Setting t_wtr to be greater than or equal to t_wr eliminates any possible post write clock stopping violations.

497767: MRS entry incorrectly updates bank bits

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r3p0-00rel0, Open.

Description

An MRS queue entry for NVM could possibly have the bank bits incorrectly updated if the MRS address happens to match an existing open page in the NVM therefore the MRS command could access the incorrect register.

Implications

Incorrect register is accessed during MRS access.

Workaround

Before executing any MRS commands to an NVM memory write a nvm_rowcache_clr command to close any open pages in RDB's for that required memory device.

500213: tRC parameter not implemented as delay between ACTIVE-AUTOREFRESH command

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r1p0-00rel0,r2p0-00rel0,r3p0-00rel0, Open.

Description

PL340 inserts a delay of tRAS + tRP between ACTIVATE and AUTOREFRESH command. However, memory devices require this delay to be tRC.

This becomes a problem when the required tRC > programmed (tRAS + tRP).

Note that for all speed bins defined in the jedec spec, apart from the 266 bin tRC=(tRAS + tRP).

This is not expected to be an issue but should be verified against specific memory data sheets.

Implications

There will be timing violations of memory device's tRC parameter if required tRC is greater then (tRAS + tRP).

Workaround

This potential violation can be fixed if tRAS and tRP is so programemd such that:

(tRAS + tRP) = tRC.

579015: AUTOREFRESH generated while in PAUSED state may cause wake-up with tXSR violation when coincident with SLEEP command

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r1p0-00rel0,r2p0-00rel0,r3p0-00rel0, Open.

Description

An unexpected self-refresh exit may occur, which will leave the SDRAM in an unexpected powered up state even though the DMC is in the LOW_POWER state and will also violate the t_xsr time period.

The scenario for this failure condition would be:

1) PL340 is put into PAUSED state via an APB PAUSE or ACTIVE_PAUSE command

2) PL340 stays in PAUSED state whilst a refresh command is generated

3) PL340 received a SLEEP command via the APB interface

4) The enter self-refresh command is interleaved with the AUTOREFRESH commands, such that a subsequent AUTOREFRESH wakes up the interface.

In this case, the AUTOREFRESH command will be issued within the t_xsr time period and the SDRAM will not be put back into self refresh.

Implications

If using the APB interface to enter self-refresh, the JEDEC timing parameter tXSR can be violated with an AUTOREFRESH command. Attached memory devices may not support this behaviour.

Additionally, the memc_status register will not accurately reflect the state of the memory devices.

Workaround

The failing scenario can be avoided if any of the following is true

1. schedule_trp is set to 0, 1 or 2 (for 1:1 sync operation should be t_rp -3)

2. (time in PAUSE state before SLEEP command is received) > fp_time

3. (time in PAUSE state before SLEEP command is received) > (refresh_prd + tRP)

583771: DMC may not enter self refresh mode via auto self-refresh

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Cat 3, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

The PL340 controller should, when programmed, enter self-refresh mode automatically after the programmed delay, relying on the force precharge function to ensure that no open rows prevent auto self refresh entry.

The logic that checks if there are any open rows is defective in that if a PRECHARGEALL command is used to close any open rows it will not acknowledge that rows in banks other than bank 0 are closed. This results in the controller never issuing the self-refresh entry command.

A PRECHARGEALL is used by the AUTOREFRESH logic to close banks prior to performing the AUTOREFRESH command.

Implications

This defect may mean the controller will not always place the memory device into self-refresh after the programmed delay.

Workaround

Setting fp_time to 0 and fp_enable to 1 will mean this defect cannot occur.

Errata - Documentation

402617: TRM has incorrect naming in Figure 2-15

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r1p0-00rel0, Fixed in r2p0-00rel0.

Description

In the Technical Reference Manual, Figure 2-15, the timing parameters tXSR and tESR have been interchanged.

tXSR is the time between self-refresh exit and the next command and tESR is the self-refresh command time. Hence, in the diagram, tXSR should be in place of tESR and vice versa.

Implications

none

Workaround

none

413769: Incorrect table name in DDI0331D TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r1p0-00rel0, Fixed in r2p0-00rel0.

Description

In the Technical Reference Manual, DDI0331, Table 3-24 on page 3-22 should be labelled 'user_config Registers bit assignments' to match the heading (section 3.3.23), and not 'user_status Registers bit assignments'.

Implications

None

Workaround

None

442486: Register reset value and field width corrections in DDI0331E TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

On Page 3-5 of the Technical Reference Manual, Table 3-1 shows an incorrect reset value of 0x00000006 for the memory_cfg3 register. The correct reset value for the memory_cfg3 register should be 0x00000007.

On page 3-25 of the Technical Reference Manual, Table 3-23 shows incorrect field bit widths for the memory_cfg3 register:

```
Table 3-23 memory_cfg3 Register bit assignments
Bits         Name             Function
[31:12]       -               Read undefined
[11:3]       prescale         Prescalar counter value
[2:0]        max_outs_refs    Maximum number of outstanding refresh commands
```

The correct field widths for the memory_cfg3 register should read:

```
Table 3-23 memory_cfg3 Register bit assignments
Bits         Name             Function
[31:13]       -               Read undefined
[12:3]       prescale         Prescalar counter value
[2:0]        max_outs_refs    Maximum number of outstanding refresh commands
```

Implications

none

Workaround

none

442622: Correction to auto self-refresh entry delay in Fig 2-24 of DDI0331E TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

Figure 2-24 entitled "Auto self-refresh entry" incorrectly shows the delay for entering self-refresh to be `(power_dwn_prd + prescale)`. This should read

`(power_dwn_prd * prescale + 1)`.

Implications

The figure is misleading and might lead to the wrong value being programmed for the prescalar.

Workaround

None

454320: Incorrect description of mclkn signal in Table A-1 in DDI0331E TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

Table A-1 entitled "Clock and reset signals" incorrectly describes **mclkn** as 'Optional clock for pad interface block.'

This should say 'Mandatory clock for pad interface block.'

Implications

none

Workaround

none

459965: aclk domain state diagram errors in DDI0331E TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

The aclk domain state diagram in Figure 2-19 of the DDI0331E TRM contains the following errors and omissions:

1. The transition labelled 'Sleep' going from the Config state to the Low Power state should be removed.
2. The transition from the Pause state to the Reset state should be labelled 'Reset'.
3. The transition from the POR state to the Reset state should be labelled 'Reset'.
4. The transition from the Reset state to the Config state should be labelled 'Configure'
5. The transition from the Config state to the Reset state should be labelled 'Reset'

Implications

none

Workaround

none

460267: Incorrect power down sequence in DDI0331E TRM

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r3p0-00rel0.

Description

Section 2.13.3 entitled "Deep power-down" gives the flow for entering power-down mode as follows:

1. Enter Pause state

2. Enter Low-power state

Point 2 is incorrect and should say:

2. Enter Config state

Implications

none

Workaround

none

484364: DDI0331E PL340 r2p0 TRM - Restriction with auto self-refresh and global CKE

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

Section 2.13.2 entitled "Dynamic low-power mode control" should contain the following note:

"Auto self-refresh and global CKE cannot be both enabled at the same time".

Implications

None.

Workaround

None

484413: DDI0331E PL340 r2p0 TRM - Table 2-4 has incorrect naming for System state 11

Status

Affects: product PL340 AXI Mem Controller.

Fault status: Doc, Present in: r2p0-00rel0,r3p0-00rel0, Open.

Description

Table 2-4 entitled "Recommended power states" incorrectly describes system state 11 as 'Shallow self-refresh or auto self-refresh'. This description should say 'Shallow self-refresh'.

The text immediately below Table 2-3 says:

"The ranking of system power states, from highest power to lowest power, is as follows:

6, 7, 8, 10, 9, 11, 13, 12"

The list of power states given in the above sentence is incorrect and should say:

"6, 7, 8, 10, 9, 11, 18, 13, 12"

Implications

None.

Workaround

None.

Errata – Driver Software

There are no Errata in this Category