BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING AND TECHNOLOGY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN ENCS3310
COURSE PROJECT

Dr. Abdellatif Abu-Issa

Objective:

The task is to design a special counter that can count two different sequences, Prime Numbers Sequence and Fibonacci sequence, both in up and down manners.

The Task:

Your task is to build a structural circuit using T-Flip Flops and combination logic, that can count either Prime numbers or Fibonacci depends on a value of an input. Also, it can count them either up or down depends on the value of another input. The counter should count the first 11 numbers of any sequence.

After that, you have to write a testbench to verify that your design is working properly, and print any error. Finally, each student will be given the design of other two students to run his testbench.

Your circuit will also include reset input (asynchronous) to reset the circuit. Also enable input (synchronous) to enable/disable the circuit from counting.

Format of the report:

This project should be written as **formal report.** The report should include sections on the following:

- Brief introduction and background
- Design philosophy
- Results
- Conclusion and Future works

The report must be submitted as pdf file and the code should be submitted on one file (as .v or .txt).

Key Points:

- Any type of plagiarism or cheating will be penalized by **0** mark, and the cheaters will be treated according to the university laws.
- The design description should include diagrams of the design, and give a justification of the decisions made.
- Technical achievement in design is linked to the degree of functionality that was attempted, as explained below.

- Technical achievement in implementation is based on the quality of your Verilog code. This includes issues such as legibility of code, use of meaningful variable names, good comments, clear structure, and modifiability of the design.

- Technical achievement in evaluation is based on the quality of your simulation results.

Deadline (strict – no extension):

- The project should be submitted before midnight on Friday 23-06-2023.
- Late submission is penalized at a rate of 10% marks per day until 27-06-2023.

Assessment Form (Feedback):

The following is the assessment form for this project:

جامعة بيرزيت
BIRZEIT UNIVERSITY

Electrical and Computer Engineering Department
Project Assessment Feedback
Advanced Digital Design (ENCS3310)

Dr. Abdellatif Abu-Issa

Student Name:…….. **Student ID:**…….

	Marks
Report Presentation (10%) Language (Spelling and Grammar), style of the report, caption of figures, page numbering…etc.	
Design Process and Outcome (70%)	
• Description of the system and design process **(20%)**	
• Technical Achievement in System Design and Evaluation **(50%)**	
Judgement and Creativity (20%) Demonstration of good judgment, imagination and creativity in selecting and applying design methods. Good discussion and analysing of the system and suggested improvements.	
Total Mark (Out of 100)	
Deducted Marks: ____ late days * 10% per day	
FINAL ALLOCATED MARK (Out of 100)	

Any evidence for any type of cheating: yes no