

Week 1 2018 lecture note	2
Week 2 2018 lecture note	17
Week 3 2018 lecture note	37
Week 4 2018 lecture note	61
Week 6 2018 lecture note	86
Week 7 2018 lecture note	123
Week 8 2018 lecture note	165
Week 9 2018 lecture note	184
Week 10 2017 lecture note	196
Stepsinamplifieranalysis	231
Information sheet	237

## **SECTION – 0: INTRODUCTION**

### **0.1 General Circuit Concepts & Revision**

- 0.1.1 Ideal & Non-Ideal Sources**
- 0.1.2 Kirchhoff's Law**
- 0.1.3 Thévenin's Theorem**
- 0.1.4 Norton's Theorem**
- 0.1.5 Two-Port Parameters**
- 0.1.6 Input & Output Impedances**

### **0.2 Frequency Analysis Revision**

- 0.2.1 Introduction**
- 0.2.2 Signal Amplitudes & Decibels**
- 0.2.3 Bode Plots**

### **0.3 What this Course Aims to Teach**

Section-0 summarises the assumed knowledge required for ELEC2133, this has been covered previously in ELEC1011, ELEC2031 & ELEC2032. You **MUST** understand all of this to deal with the material in Sections 1-7.

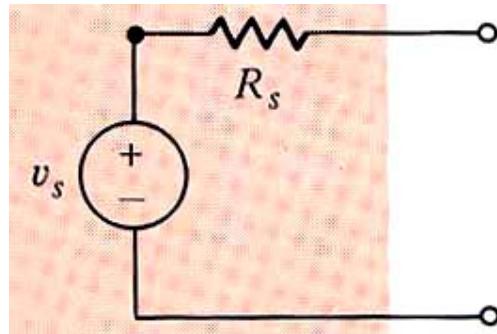
- Section-1: Operational Amplifiers
- Section-2: Semiconductor Devices for Electronics
- Section-3: Transistor Amplifiers: Small Signal and DC
- Section-4: Frequency Response of Amplifiers
- Section-5: Feedback in Amplifiers
- Section-6: Feedback and Stability
- Section-7: Non-Linear Circuits – Waveform generation
- Section-8: Digital-Analogue Interface

# 0.1 General Circuit Concepts & Revision

## 0.1.1 Ideal & Non-Ideal Sources

### Voltage Source

non-ideal voltage source

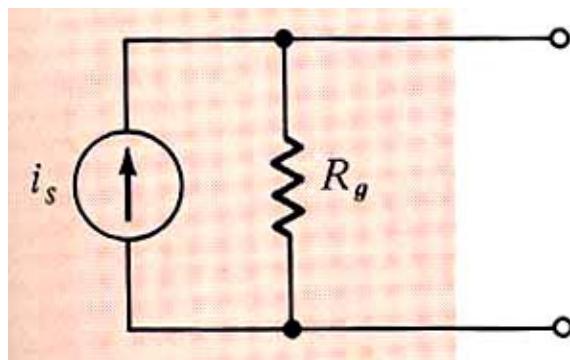


For an ideal voltage source, the resistance  $R_s$  should be zero.

- Example: Battery, power supply.
- In practice we want  $R_s$  as small as possible.

### Current Source

non-ideal current source



For an ideal current source the resistance  $R_g$  should be infinite.

Example: Current mirror

In practice, we want  $R_g$  as large as possible.

## 0.1.2 Kirchhoff's Laws

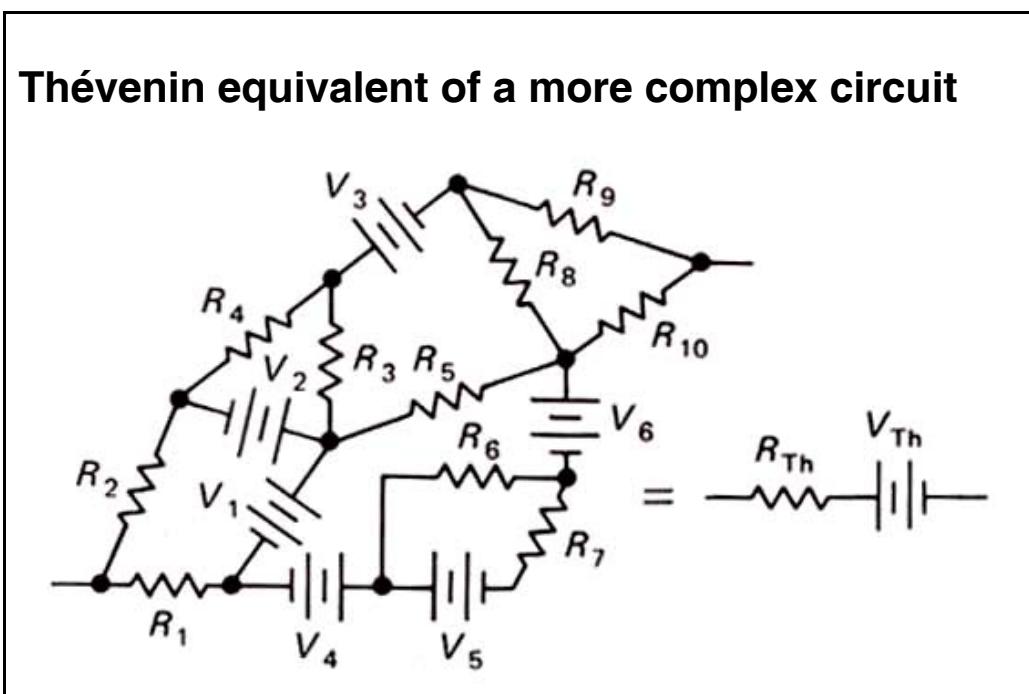
**Voltage Law:** Algebraic sum of all voltages around any loop in a circuit must be zero.

**Current Law:** Algebraic sum of all currents at any node, (i.e., connection of two or more circuit elements) must be zero.

These laws form the basis of nodal analysis and mesh analysis – both powerful tools for analysis of circuits. The student should know which law is needed in which analysis and understand how to use each approach.

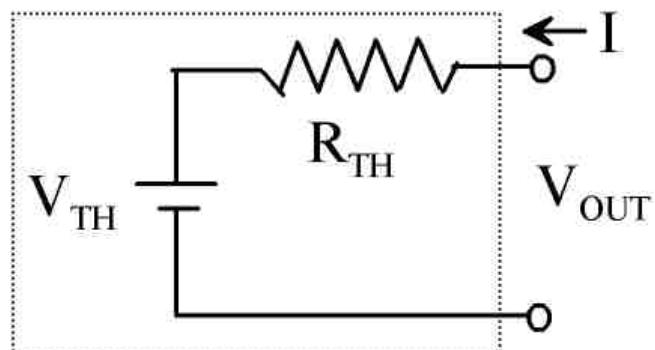
## 0.1.3 Thévenin's Theorem

Any two-terminal network of resistors and voltage sources is equivalent to a single resistor in series with a voltage source.

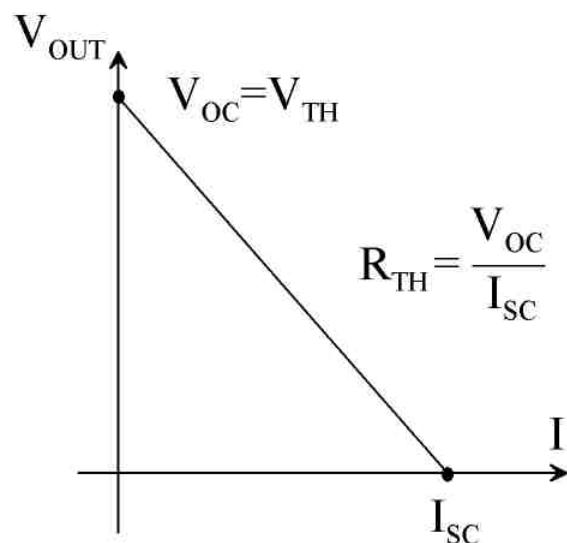


The Thévenin equivalent circuit is found in two stages:

1. Find the open circuit voltage. Have no load attached to the circuit and work out by the usual circuit analysis what the voltage is at the output terminals.
2. Determine the output resistance with all independent sources turned off (set to zero).



the Thévenin equivalent circuit



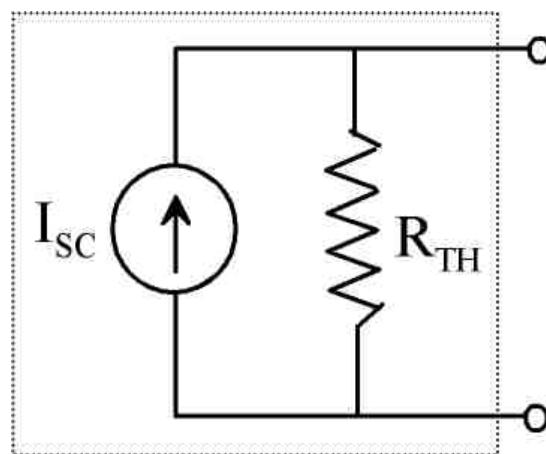
the I-V characteristic of the Thévenin equivalent circuit

## 0.1.4 Norton's Theorem

Similar to Thévenin's theorem, although the equivalent circuit is taken to be a current source in parallel with a resistor of value  $R_{TH}=V_{OC}/I_{SC}$ .

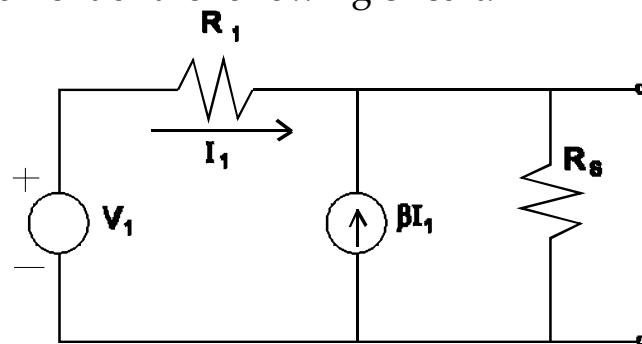
The Norton equivalent circuit can be found from the Thévenin equivalent or if this hasn't been found:

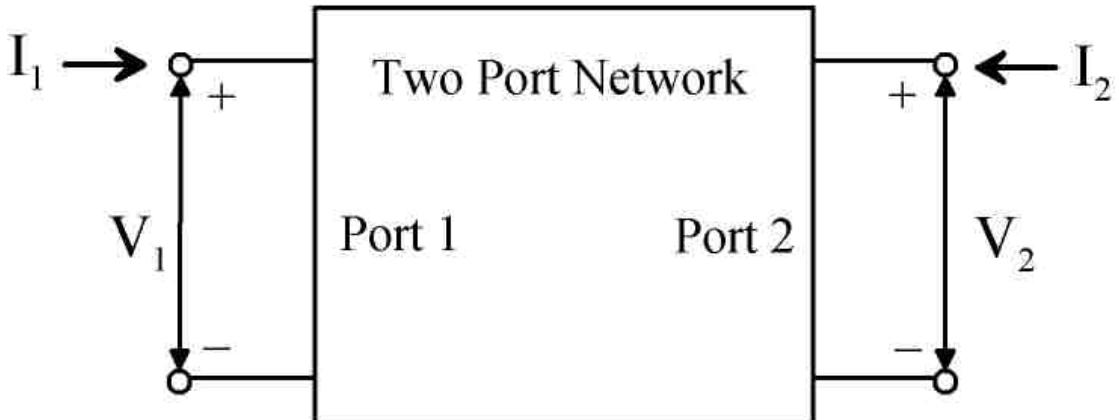
1. Find the short circuit  $I_{SC}$  current by placing a short circuit across the output terminals of the circuit and finding the current flowing through it.
2. The output resistance can be calculated (see Thévenin) or the open circuit voltage can be found (see Thévenin).



The V-I characteristic of both the Thévenin and Norton equivalent circuits are identical.

**EXAMPLE:** Determine the Thevenin voltage, Thevenin resistance and Norton current of the following circuit.





### Admittance Parameters

$$I_1 = y_{11}V_1 + y_{12}V_2 \quad I_2 = y_{21}V_1 + y_{22}V_2$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0} \quad y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} \quad y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} \quad y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

### Impedance Parameters

$$V_1 = z_{11}I_1 + z_{12}I_2 \quad V_2 = z_{21}I_1 + z_{22}I_2$$

$$z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \quad z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \quad z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \quad z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}$$

### Hybrid Parameters

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad I_2 = h_{21}I_1 + h_{22}V_2$$

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} \quad h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \quad h_{21} = \left. \frac{I_1}{I_2} \right|_{V_2=0} \quad h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

### g - Parameters

$$I_1 = g_{11}V_1 + g_{12}I_2 \quad V_2 = g_{21}V_1 + g_{22}I_2$$

$$g_{11} = \left. \frac{I_1}{V_1} \right|_{I_2=0} \quad g_{12} = \left. \frac{I_1}{I_2} \right|_{V_1=0} \quad g_{21} = \left. \frac{V_2}{V_1} \right|_{I_2=0} \quad g_{22} = \left. \frac{V_2}{I_2} \right|_{V_1=0}$$


---

## 0.1.6 Input & Output Impedance

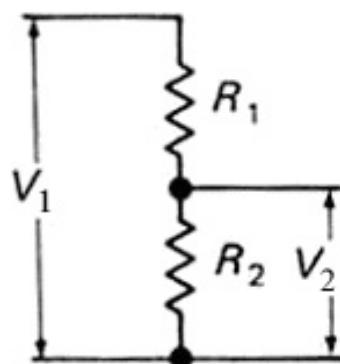
Input impedance refers to the impedance seen by a signal entering any general circuit or the impedance of the circuit ‘looking’ into the input stage of the circuit. Similarly, the output impedance is that seen by a signal leaving the circuit. Both input and output impedances can be calculated by applying a test signal to the input and output stages respectively.

The input and output impedances of stages are a very important consideration when building real circuits. Numerous times in this subject, the student will be asked to calculate both of these quantities for a given circuit. In the feedback section of the course, the effect of the feedback on both of these quantities will be investigated. The question is – why are these values so important so that so much time is devoted to finding their values?

The best way to explain the importance of these two resistances is to look at the simple voltage-divider circuit shown below. How is  $V_2$  related to  $V_1$ ?

Easy. Assuming there’s no load on  $V_2$  the current flowing through both resistors is the same and equal to  $I = \frac{V_1}{R_1 + R_2}$  and so

we can show that  $V_2 = V_1 \frac{R_2}{R_1 + R_2}$ .

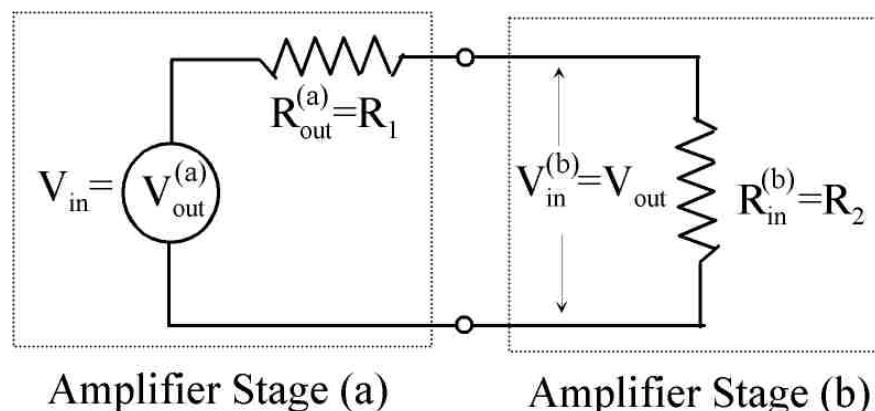


What this means is that  $V_2$  can only ever equal  $V_1$  and never be bigger, in fact in reality it will **always be smaller**. If we extend this result to a number of sub-circuits connected together we can think of  $V_1$  as the output of a previous stage with output resistance  $R_1$  and  $V_2$  to be the input of a following stage with input resistance  $R_2$ .

This means that every time we connect one stage of a circuit to another stage, we are in fact **losing some of our signal**. If  $R_1$  and  $R_2$  are similar values then the signal can be reduced very quickly. This can be avoided by trying to fashion a design in which  $V_1 \approx V_2$ .

By setting  $R_1$  (output resistance) to be very small or by making  $R_2$  (input resistance) very large this will be the case. A better approach is to try and make both true.

**This is why for a circuit where we are interested in the voltage, we want the input resistance to be as high as possible and the output resistance to be as low as possible.**



Q. Is the same true if we are interested in the current? If not what should be the values for the input and output impedances?

?? Condition for maximum power transfer?

?? impedance matching?

## 0.2 Frequency Analysis Revision

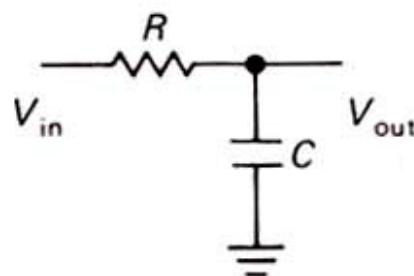
### 0.2.1 Introduction

When a **linear** circuit has an input signal that varies with time as a sinusoid, then the behaviour of the circuit can be analysed as a function of the frequency of the applied signal. This type of analysis will be heavily used throughout this course, as we are interested in how a circuit behaves as a function of frequency.

The first thing to realise is that if the circuit is described in the frequency domain, i.e., in terms of phasor and impedances, resistive-network concepts such as Thévenin's and Norton's theorems apply. Analysis methods such as mesh and nodal analysis can also be used in the frequency domain. This is because the frequency of the signal applied to the circuit does not change, only the amplitude and phase.

---

#### Example Low-Pass Filter



The low pass filter can be viewed in much the same way as a voltage divider that is more general with  $R$  and  $C$  being impedances. The impedance of  $C$  labelled  $Z_C$  is equal to  $-j/\omega C$  where  $\omega$  is the angular frequency and  $j^2 = -1$ . The  $j$  represents the phase-shifting nature of the capacitor in an easy-to-handle form.

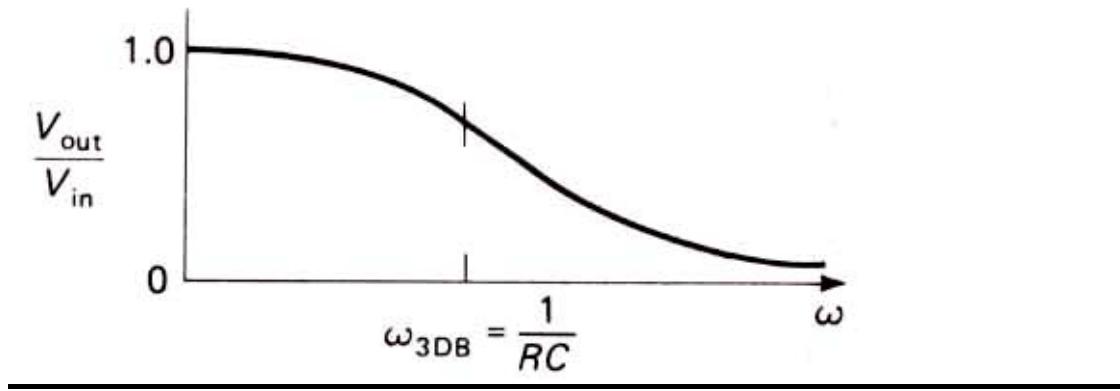
The current flow through the circuit, given by the complex version of Ohm's law, is:

$$I = \frac{V_{in}}{R - (j/\omega C)}$$

So the voltage  $V_{out}$  is the voltage across the capacitor and is found by multiplying this current by the capacitor's impedance.

$$V_{out} = IZ_C = \frac{-(j/\omega C)V_{in}}{R - (j/\omega C)} = \frac{1}{(1 + \omega^2 R^2 C^2)^{1/2}} V_{in}$$

If we plot the gain of this circuit as a function of  $\omega$ , we get the curve below with the low-pass behaviour we expect. The  $-3\text{dB}$  breakpoint is indicated and is equal to  $1/RC$ .



### 0.2.1 Signal Amplitudes & Decibels

There are a number of different ways to compare the relative amplitudes of two signals. One way is to simply give the ratio of the output and input voltages directly. This is fine if the gain is say 10, but what if the gain is around 1 million? In this case it is easier to use a logarithmic measure and, to this end, we can use the decibel. By definition the ratio of two signals, in decibels, is:

$$\text{dB}_A = 20 \log_{10} \frac{A_2}{A_1}$$

where  $A_1$  and  $A_2$  are the two signal amplitudes. It is also sometimes useful to express the ratio of two signals in terms of the power levels:

$$\text{dB}_P = 10 \log_{10} \frac{P_2}{P_1}$$

where  $P_1$  and  $P_2$  represent the power of the two signals respectively. The power level definition is used when comparing unlike waveforms.

The  $-3\text{dB}$  point, which is typically quoted for filters, is where the amplitude of the output signal has fallen to  $1/\sqrt{2} \approx 0.707$  of the input signal. In terms of power the output signal has power equal to half of the input signal. A filter can have a  $-3\text{dB}$  point at a low and a high frequency and so there is a band of frequencies where the signal can pass – this range of these frequencies is referred to as the bandwidth of a circuit.

### 0.2.3 Bode Plots

More usually, the gain of a filter circuit is given as a transfer function  $G$  or  $H$ . The transfer functions can usually be written in the general form:

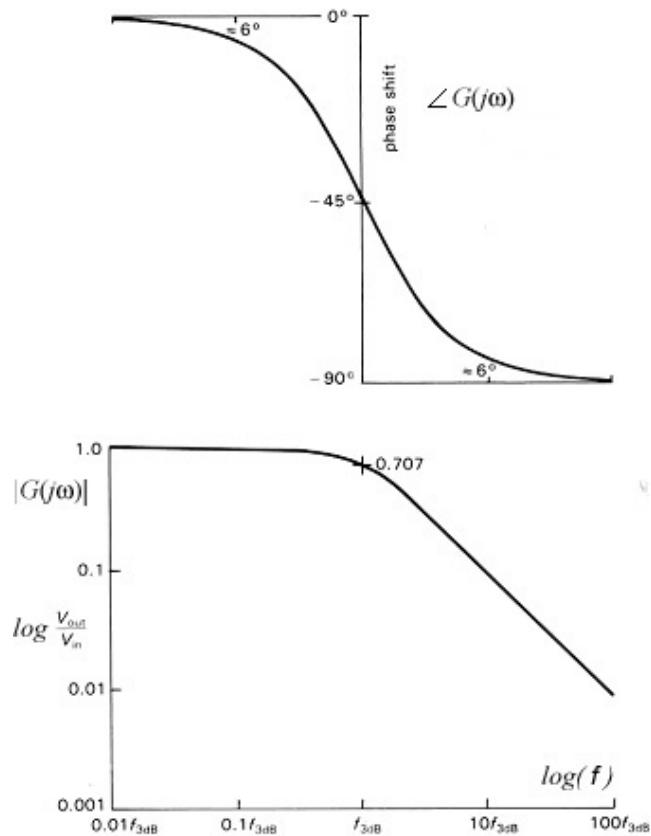
$$G(j\omega) = \frac{A(1 + j\omega/\omega_0)(\dots)(\dots)}{(1 + j\omega/\omega_p)(\dots)(\dots)}$$

Taking the absolute value of  $G$  gives the magnitude response that we have already found. If we want to look at how the phase behaves, we find the angle of  $G$ .

$$\angle G(j\omega) = \tan^{-1}(\omega/\omega_0) + \dots - \tan^{-1}(\omega/\omega_p)$$

Typically we look at the magnitude response as a log-log plot against frequency as well as the phase (linear-log), referred to together as a Bode Plot.

For the case of the low pass filter the Bode plots are shown below.



Note the  $-3\text{dB}$  frequency has been marked. It is sometimes referred to as the corner or break frequency. The roll-off of the frequency response is  $-20\text{db}$  per decade.

## 0.3 Transistors

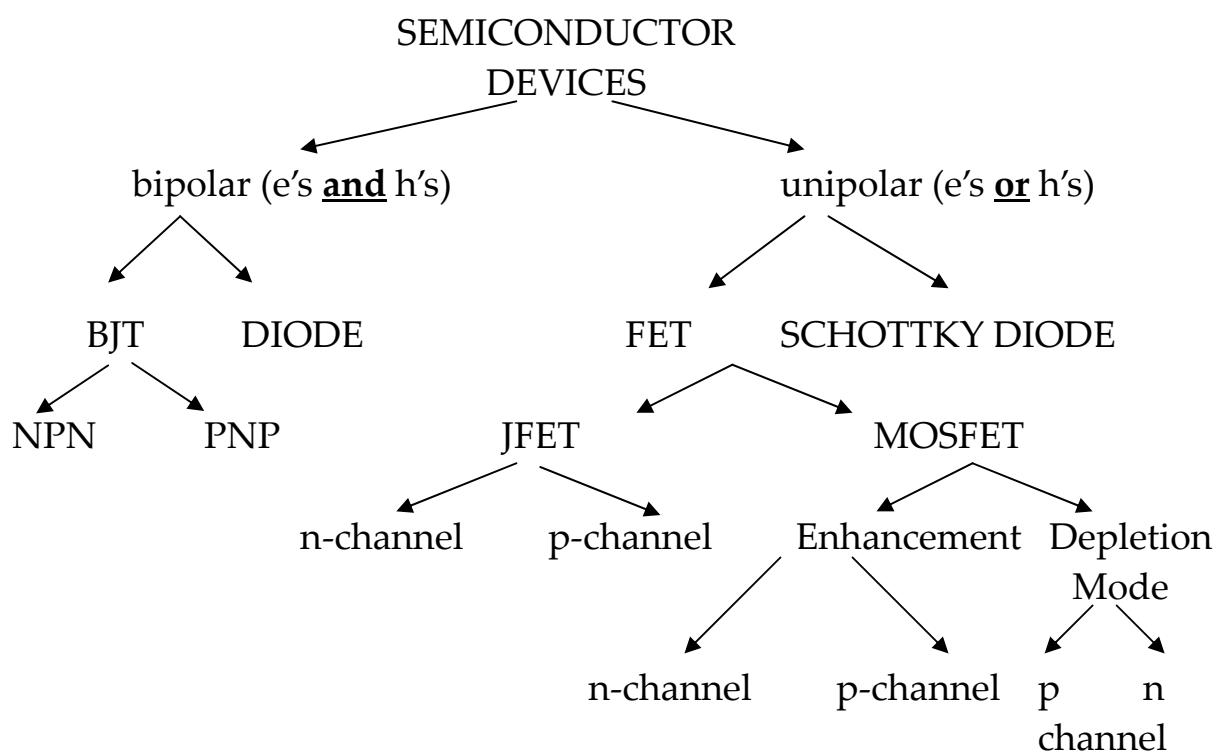
### 0.3.1 Introduction

There are two main uses for transistors in electronics:

1. as an **amplifier** of signals (**analogue** applications); and
2. as a **switch** (typically **digital** applications)

Both of these applications will be covered in this course, as well as a few other applications, e.g., current mirrors.

There are two types of transistors that will be encountered. The student should already be familiar with both but the following is included as a memory aid.

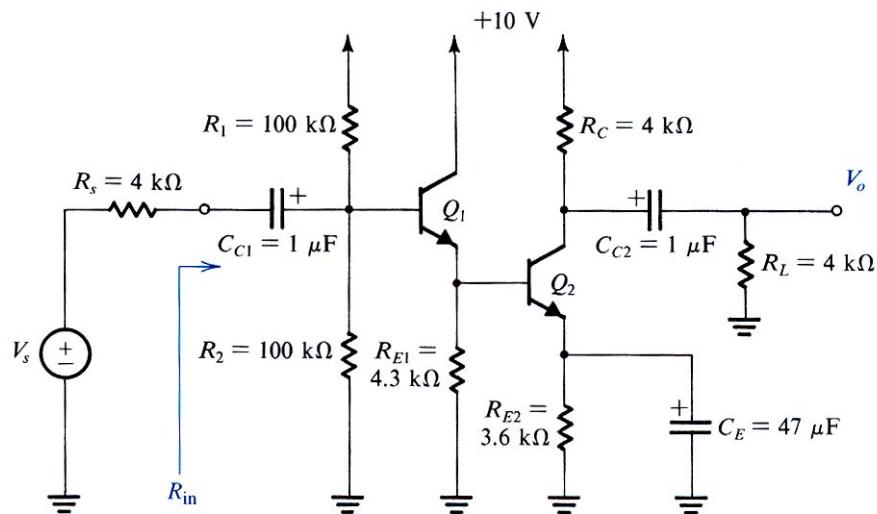


## 0.3 What this Course Aims to Teach

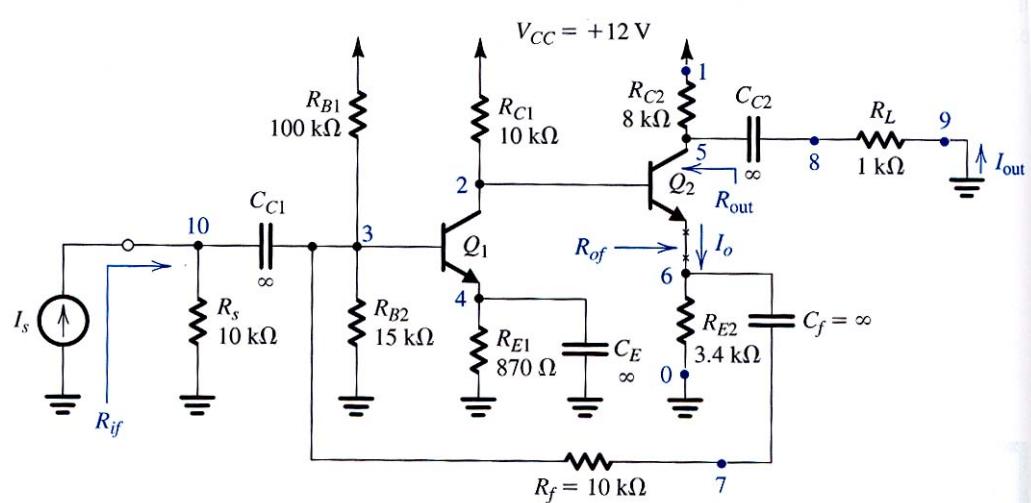
- Develop an intuitive feel for how the circuit works

Section 2 - 4: By the end of this course, the student will see the circuit below and be able to find the mid-band gain or perhaps the high corner frequency. The course aims to equip the student with the tools to essentially analyse **ANY** circuit by turning the one big problem into a series of smaller problems.

Also the student should develop an appreciation for when an answer is 'right', i.e., does your answer make sense?



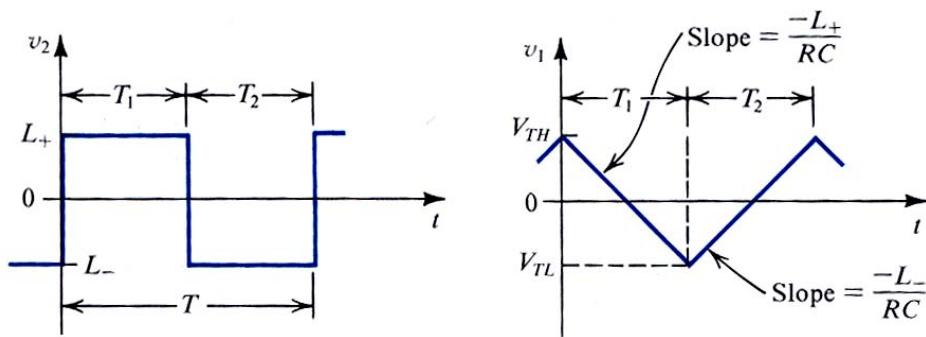
Sections 5 & 6: The student should be able to explain the improvements to circuit operation made possible by the circuit that is shown below, and also be able to calculate the changes in such parameters as the gain, input impedance, etc...



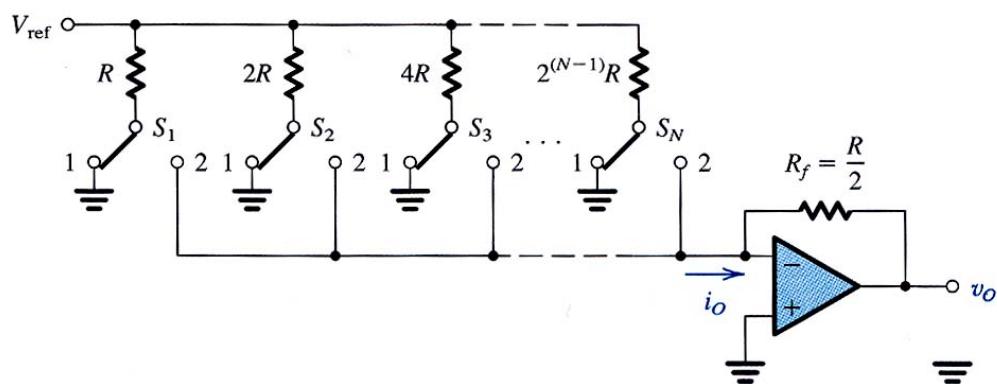
In particular, the student should realise that this circuit is using feedback and know whether the feedback is positive or negative and what topology is being used.

### Understand the role of various components and its influence on circuit performance

Section 7 (Non-linear ccts): The student should also, by the end of the course, be familiar with the circuits used to generate the waveforms shown below and others, and be able to explain the operation of the circuit. You should also have some expertise at designing a circuit to give a desired output waveform.



Section 8(Digital-Analog conversion and vice versa): As well as this, the student should be familiar with the circuit below and be able to give a description of its operation and, at the very least, say what it can be used for.



This is by no means an exhaustive list of the things that will be covered in the course, but it is hoped that it gives the student a taste of what the course has to offer.

# **SECTION 1 – OPERATIONAL AMPLIFIERS**

## **1.1 The Ideal Op-Amp – Basic Properties**

## **1.2 Op-Amp Golden Rules**

## **1.3 Non-Ideal Op-Amps**

## **1.4 Some Useful Op-Amp Circuits**

### **1.4.1 Non-Inverting Amplifier**

### **1.4.2 Unity Gain Buffer (voltage follower)**

### **1.4.3 Summing Amplifier**

### **1.4.4 Integrator**

### **1.4.5 Instrumentation (Difference) Amplifier**

## **1.5 DC Imperfections of Op-Amps**

### **1.5.1 Calculation of Output-Offset Voltages Due To Input-Offset Current**

### **1.5.2 Calculation of Output-Offset Voltages Due to Input-Offset Voltages**

### Aims

- Operational Amplifiers are briefly looked at, with the golden rules used for circuit analysis given.
- Additionally some common and very useful circuits are presented.
- Finally the effect of d.c. imperfections of real op-amps are looked at.

### What is missing?

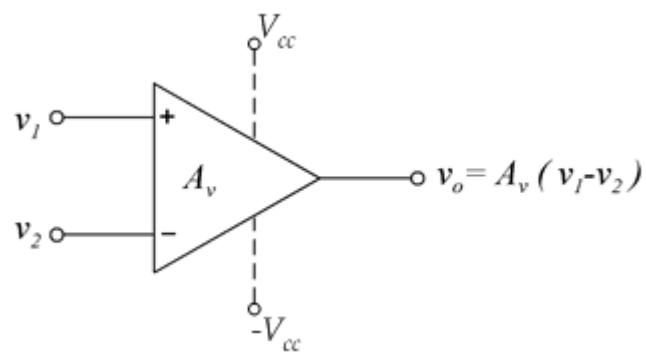
- The internal circuitry of real op-amps will be presented, but only after the small-signal analysis of transistor circuits has been presented. After Section 2, the internal circuitry of an op-amp should mean something to you.
- The behaviour of the op-amp as the frequency of the input signal is varied. As will become apparent, the behaviour of op-amps as a function of frequency is a direct consequence of

its internal circuitry.

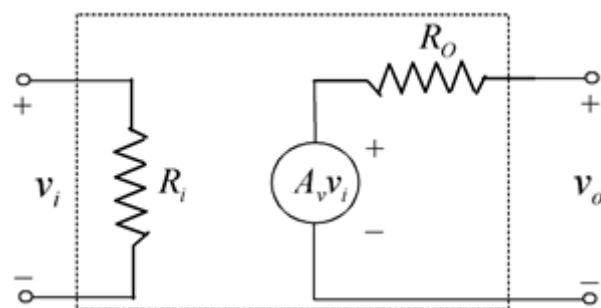
## 1.1 The Ideal Op-Amp – Basic Properties

1. Direct coupled, i.e., not capacitively.
2. High gain.
3. Basic linear (analogue) integrated circuit.
4. Differential input— + and – non-inverting or inverting input.
5. Single-ended output, usually.

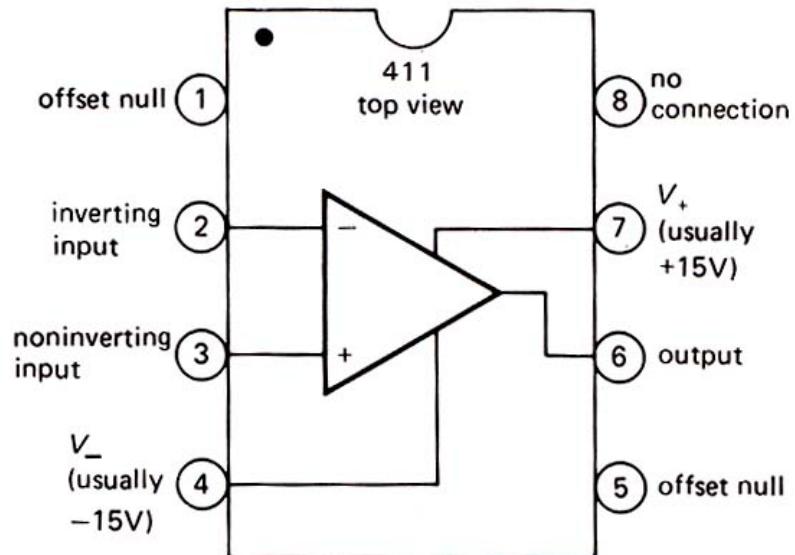
Symbol



Equivalent circuit.



## Typical Pin Design Of Actual Device



## Parameters characterising Op-Amps

1. Open loop voltage gain
2. CMRR
3. Input resistance
4. Output resistance
5. Input bias current
6. Offset voltages and currents.
7. Bandwidth.

**Ideal Op-Amps** have the following characteristics:

1. input resistance  $R_i \rightarrow \infty$   
i.e., no current enters either the + or - input terminals.
2. output resistance  $R_o = 0$
3. voltage gain (open loop)  $A_v \rightarrow \infty$  [in practice,  $10^4 - 10^6$ ]  
But  $v_o = A_v v_i$  has to be finite, i.e.,  $v_+ = v_-$  'virtual ground'.
4. infinite bandwidth

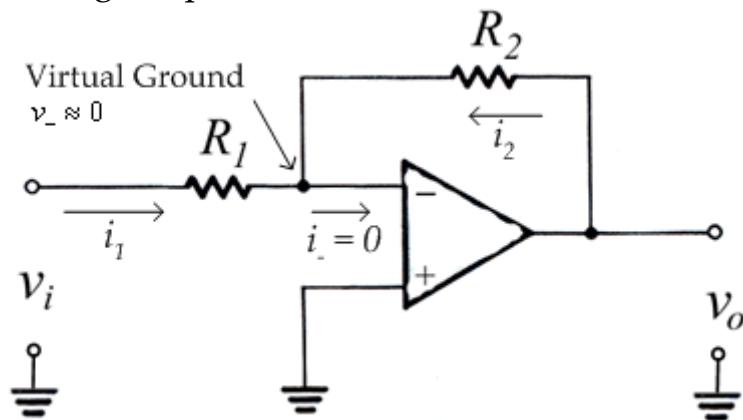
## 1.2 Op-Amp Golden Rules

- I. The output attempts to do whatever is necessary to make the voltage difference between the inputs zero. (Virtual Ground)
- II. The inputs draw no current.

As will be shown, this is not true in reality, but, for analysis purposes, the rules are remarkably useful and allow a large number of circuits to be designed and analysed. A simple example is the inverting amplifier circuit shown below.

---

### Example Inverting Amplifier



The non-inverting input is at ground, so from Rule I, the inverting input must also be at ground. Since, by Rule II, no current is drawn by the inverting input, we have:

$$i_1 + i_2 = i_- = 0$$

$$\frac{v_i}{R_1} + \frac{v_o}{R_2} = 0$$

which when rearranged gives the following result of closed-loop gain:

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \quad (\text{180}^\circ \text{ phase difference between i/p and o/p})$$

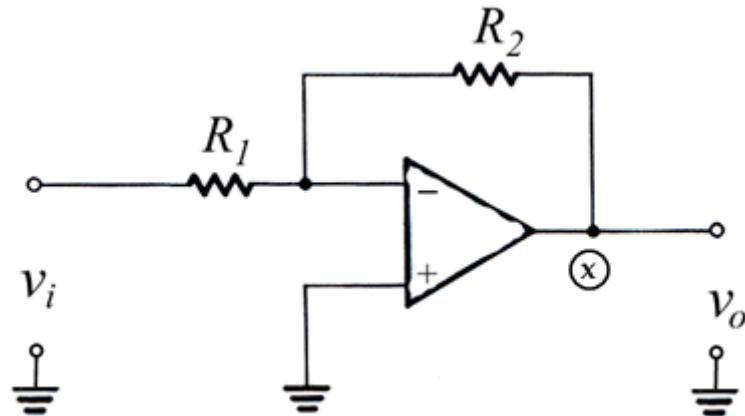
---

NB: we are talking about a.c. signals, so the negative sign of the gain means that the input signal is inverted at the output. You should check that you understand this.

## 1.3 Non-ideal Op-Amps

Consider the inverting amplifier once again.

### Inverting Amplifier



$$v_+ = 0 \text{ (note 3)}, i_- = 0 \text{ (note 1)}$$

$$\text{Current flowing through } R_1: I = \frac{v_i - v_-}{R_1} = \frac{v_i}{R_1}$$

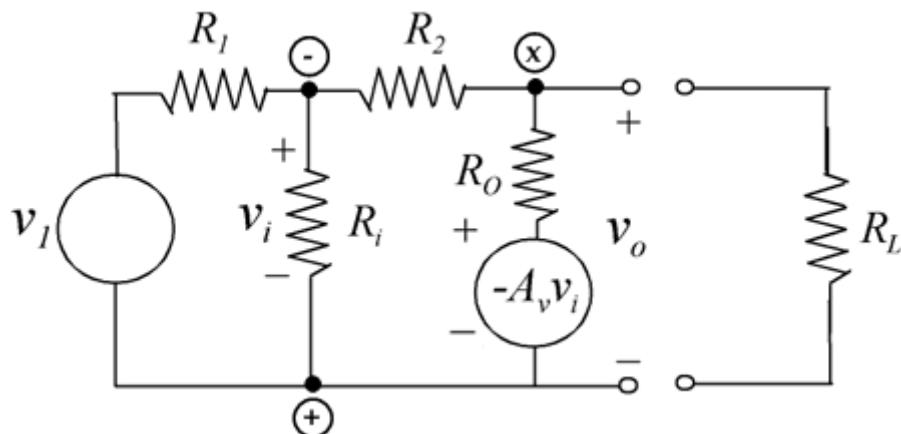
This same current flows through  $R_2$  (though in opposite direction):

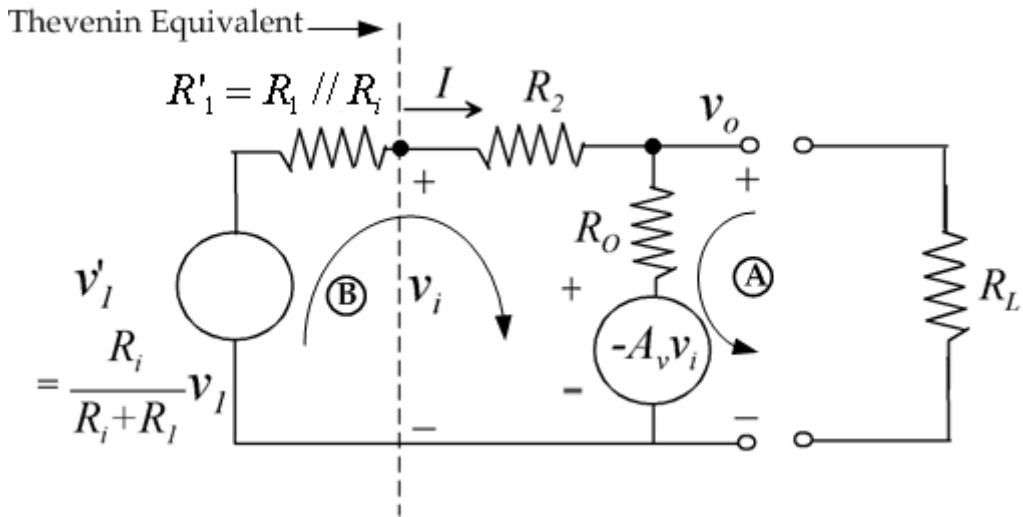
$$\therefore v_o = -IR_2 \Rightarrow \frac{v_o}{v_i} = -\frac{R_2}{R_1}$$

This is for an ideal op-amp but what if the op-amp is behaving non-ideally.

Suppose  $A_v < \infty, R_i < \infty, R_o > 0$ .

Then the equivalent circuit for the inverting amplifier becomes:





Loop A:

$$v_o = -A_v v_i + I R_o$$

$$v_i = v_o + I R_2$$

$$\Rightarrow I = \frac{(1 + A_v) v_o}{R_o - A_v R_2}$$

Taking KVL in the circuit loop (Loop B):

$$v'_I = I(R'_1 + R_2 + R_o) - A_v v_i$$

Substituting for  $I$  and  $v_i$ , yields the closed-loop gain

$$\frac{v_o}{v_i} = A_{vf} = \frac{-A_v R_2 + R_o}{R'_1(1 + A_v) + R_2 + R_o}$$

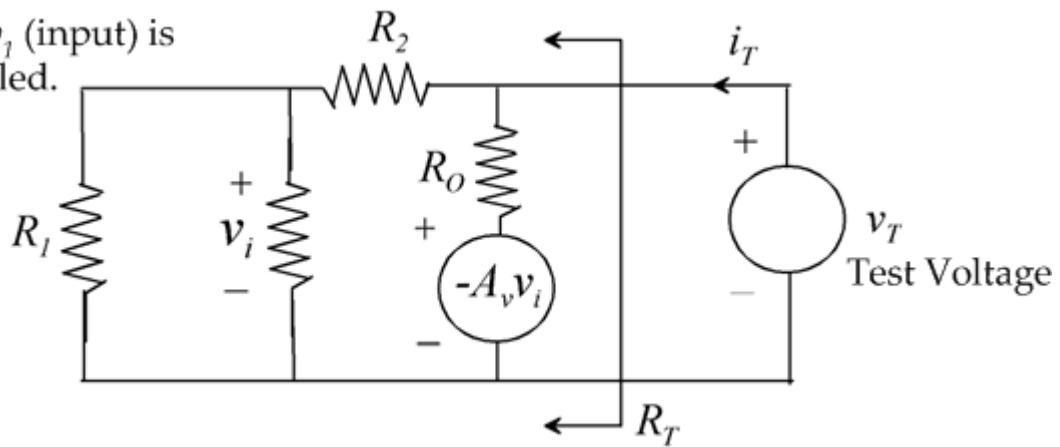
- If  $R_i$  very large compared to  $R_1 \rightarrow R'_1 \approx R_1$  [Golden Rule #2]
- If  $A_v \gg 1$  such that  $A_v R_1 \gg R_2 + R_o$  [Golden Rule #1]

Then  $A_v = -\frac{R_2}{R_1}$  ..... ideal case

As long as  $A_v R_1 + A_v R_2 \gg R_o$ , the open circuit output voltage  $v_o$  is independent of deviations from the ideal op-amp. This  $v_o$  is the Thévenin voltage at the output.

## What is the Thévenin resistance seen at the output?

**NB:**  $v_i$  (input) is disabled.



Apply a test voltage  $v_T = \left( i_T - \frac{v_T}{R'_1 + R_2} \right) R_o - A_v v_i$  where  $R'_1 = R_1 // R_i$

$$v_i = \frac{R'_1}{R'_1 + R_2} v_T$$

$$\frac{v_T}{i_T} = R_T = \frac{(R'_1 + R_2) R_o}{R'_1 (1 + A_v) + R_2 + R_o} \rightarrow \frac{R_o}{A_v} \text{ as } -A_v \rightarrow \infty$$

$R_T \rightarrow 0$  as  $A_v \rightarrow \infty$

Methodology to calculate output impedance:

1. Disable inputs (**only independent sources**)
2. Apply test voltage  $v_T$
3. Calculate test current resulting  $i_T$
4. Then,  $R_T \equiv \frac{v_T}{i_T}$

## Comparison between an actual device and the ideal model.

### Non-Ideal (actual)

$$R_1 = 5 \text{ k}\Omega, R_2 = 10 \text{ k}\Omega, A_v = 5 \times 10^4, R_o = 500 \Omega, R_i = \infty, R_L = 100 \Omega.$$

Apply a signal  $v_i = 1.5 \text{ V}$ .

$$A_v v_i = \frac{-5 \times 10^4 \times 10 + 0.5}{5(1 + 5 \times 10^4) + 10 + 0.5} \cdot 1.5 = -2.9998 \text{ V} \quad [\text{Using expression on page 6}]$$

$$R_T = 0.027 \Omega \quad [\text{From page 7}]$$

$$v_o = \frac{R_L}{R_L + R_T} \cdot A_v v_i = -2.999 \text{ V} \approx -3.0 \text{ V}$$

### Ideal

$$v_o = -\frac{R_2}{R_1} \times 1.5 = -3.0 \text{ V}$$

With typical values of  $A_v$  &  $R_o$ , the difference between the actual and ideal values is insignificant.

This means that for most situations we can assume that an op-amp is behaving ideally.

## Summary of Op-amp Characteristics

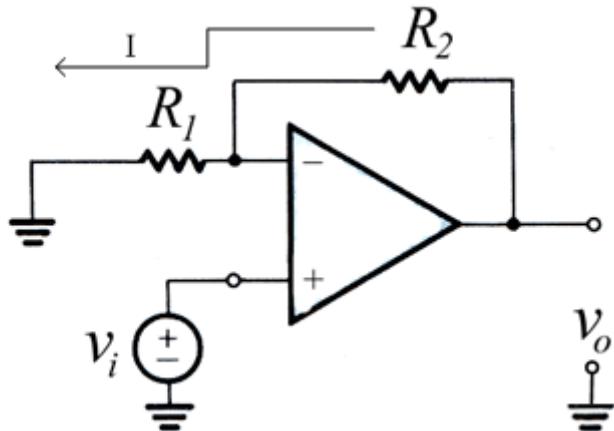
	Ideal	Typical
open-loop gain	$\infty$	$>10^4$
open-loop bandwidth	$\infty$	single pole ( $\sim 10$ Hz)
CMRR	$\infty$	$\geq 70$ dB
$R_i$	$\infty$	$\geq 10$ M $\Omega$
$R_o$	0	$< 500$ $\Omega$
input currents	0	$< 0.5$ $\mu$ A
offset voltage	0	$< 10$ mV
offset current	0	$< 0.2$ nA

## Important Points

- The large open-loop gain ensures an exclusive dependence of the closed-loop gain on external impedances (ie. **What external components connected**).
- **The dominant-pole** transfer function for open-loop gain ensures that, for a specified closed-loop gain, the bandwidth is readily determined.
- A large **CMRR** ensures that the output signal is proportional to the difference between the input voltages and common signals (d.c. components have only a small effect on the amplifier output).

## 1.4 Some Useful Op-Amp Circuits

### 1.4.1 Non-Inverting Amplifier

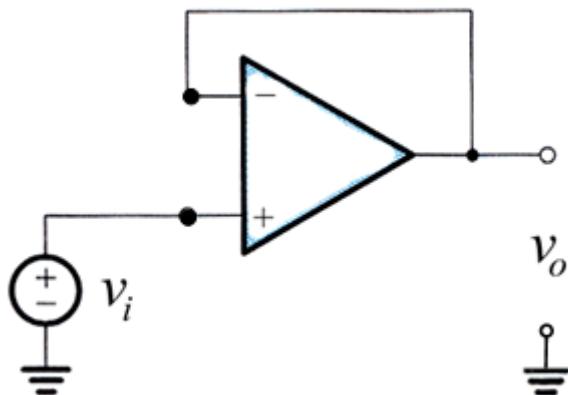


$$v_+ = v_- = v_i, \quad v_o - v_- = IR_2 \text{ and } v_- = IR_1$$

$$v_o = \frac{v_-}{R_1} (R_1 + R_2) = \left(1 + \frac{R_2}{R_1}\right) \cdot v_-$$

$$\therefore A_{vf} = \left(1 + \frac{R_2}{R_1}\right) \quad [A_{vf} \equiv \frac{v_o}{v_i}]$$

### 1.4.2 Unity Gain Buffer (voltage follower)



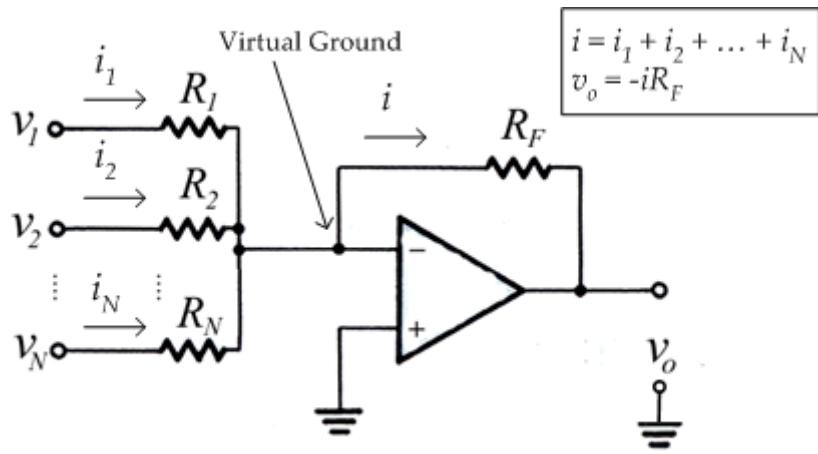
Same as above with:  $R_2 = 0$  and  $R_1 = \infty$

$$v_- = v_+ = v_i \text{ and } v_- = v_o \Rightarrow v_o = v_i \text{ or } A_{vf} = 1$$

What is the purpose of such a circuit?

It has very high input impedance and very low output impedance.

### 1.4.3 Summing Amplifier (Inverting)



The current flowing through  $R_F$  will be equal in magnitude to the sum of the input currents:

$$\begin{aligned} v_o &= -R_F \left( \frac{v_1}{R_1} + \frac{v_2}{R_2} + \dots + \frac{v_N}{R_N} \right) \\ &= -\left( \frac{R_F}{R_1} \cdot v_1 + \frac{R_F}{R_2} \cdot v_2 + \dots + \frac{R_F}{R_N} \cdot v_N \right) \end{aligned}$$

Weighted summer – the value of the input resistor weights each input.

If we then make all of the input resistors equal in value, i.e.,

$$R_1 = R_2 = \dots = R_N = R^*$$

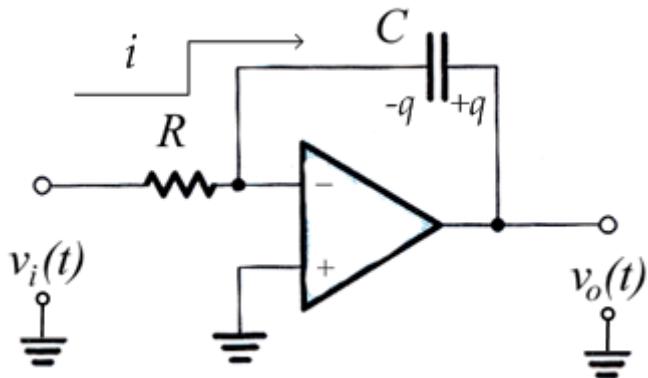
Then we will have for the output voltage:

$$v_o = -\frac{R_F}{R^*} (v_1 + v_2 + \dots + v_N)$$

Output is proportional to sum of the inputs.

**Question: Find or deduce the configuration for a non-inverting summing amplifier and derive the gain expression.**

## 1.4.4 Integrator



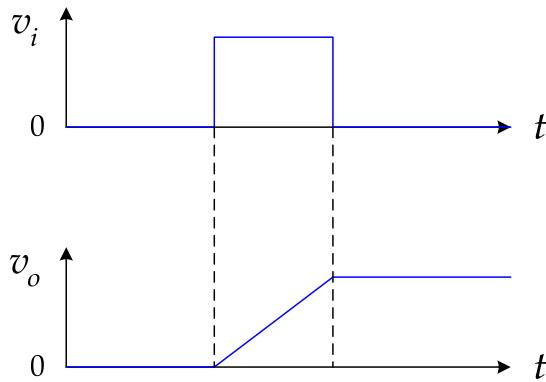
Recall:  $q = CV \rightarrow q = Cv_0$

$$\text{Here : } i = -\frac{dq}{dt} = -C \frac{dv_o}{dt}$$

$$i = \frac{v_i}{R} = -C \frac{dv_o}{dt}$$

$$v_o(t) = v_o(t=0) - \frac{1}{RC} \int v_i(t) dt$$

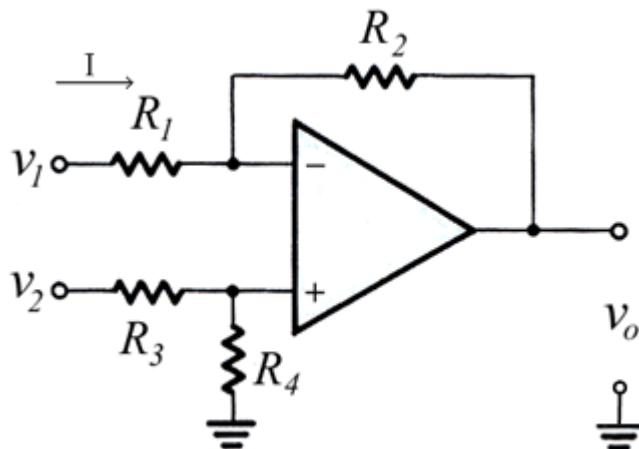
The output voltage is proportional to the integral of the input voltage. So if  $v_i(t)$  is constant then  $v_o(t)$  will be a linear ramp.



**Question:** How can we get a differentiator?

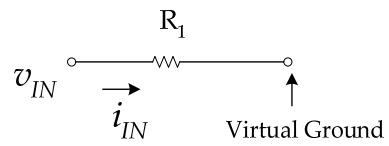
**Reverse the roles of  $R$  and  $C$  in the circuit.  
Prove this to yourself and your friends.**

## 1.4.5 Instrumentation (Difference) amplifier



Input  $R$ :

Assume  $v_2 = 0$ :



By definition:

$$R_{IN} = \frac{v_{IN}}{i_{IN}} = R_1$$

$$v_+ = \frac{R_4}{R_3 + R_4} \cdot v_2 = v_-$$

$$I = \text{current through } R_1 = \frac{v_1 - v_-}{R_1} = \frac{v_1 - \frac{R_4}{R_3 + R_4} v_2}{R_1}$$

$$v_o = v_- - IR_2$$

$$v_o = \frac{R_4}{R_3 + R_4} \left( 1 + \frac{R_2}{R_1} \right) v_2 - \frac{R_2}{R_1} v_1$$

If we have that  $R_3 / R_4 = R_1 / R_2$

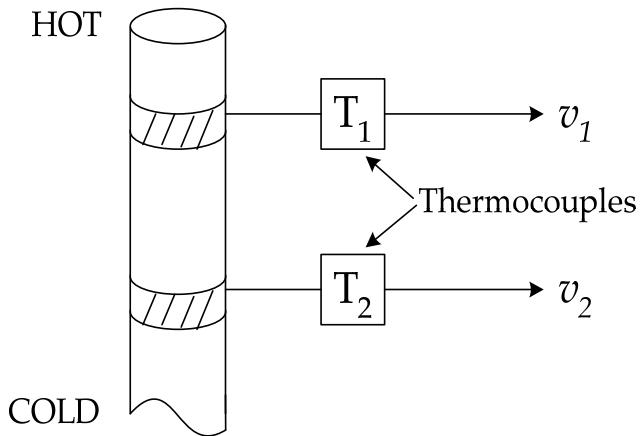
Then:  $v_o = \frac{R_2}{R_1} (v_2 - v_1)$

i.e., the difference in input voltages is amplified; hence it is called a difference or differential amplifier.

Uses: monitoring strain gauges, thermocouples, hot-wire anemometers (fluid flow).

Note that the source resistances have to be included in  $R_1$  &  $R_3$ .

May need buffers.



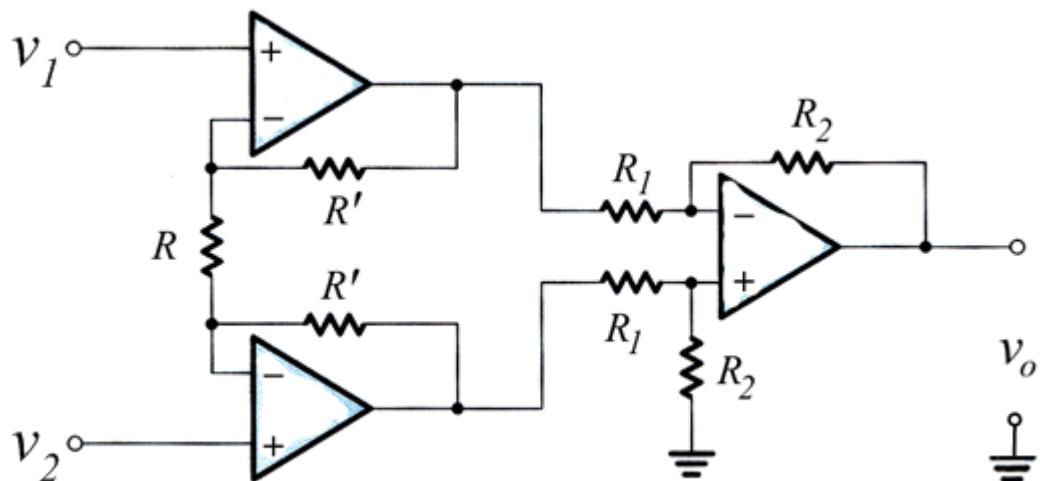
## What is the input resistance of this circuit?

Assuming  $R_1 = R_3$  and  $R_2 = R_4$ , if we apply a signal  $v_2 - v_1$  across the two inputs, what is  $R_{in} = \frac{v_2 - v_1}{i}$ ? Since the two inputs to the op-amp track each other, there is a virtual short-circuit between them. Hence, the magnitude of the current flowing through each input resistor is equal:

$$R_{in} = 2R_1$$

Can we improve on this circuit?

Yes, and here it is in all its glory.



$$v_o = \left(1 + \frac{2R'}{R}\right) \left(\frac{R_2}{R_1}\right) (v_2 - v_1)$$

Advantages over difference amplifier:

- higher input resistance (input signal ‘sees’ the op-amps to the left of the circuit)
- higher common-mode rejection ratio

## 1.5 D.C. Imperfections Of Op-Amps

We saw in the previous section that a real op-amp consists of multiple stages consisting of numerous transistors. Due to the input stage being a differential amplifier we will see two d.c. input offsets in real devices – namely, the offset voltage and offset currents.

For an ideal op-amplifier, if both inputs  $v_+ = v_- = 0$ , then  $v_o = 0$ .  
For a non-ideal (typical) op-amp,

$v_o \neq 0$  even when  $v_+ = v_- = 0$ .  
 $= V_{OS}$       **OUTPUT OFFSET VOLTAGE**

- The output offset voltage is like a d.c. bias level in the output of a conventional amplifier in that it is added to whatever signal variation occurs there.
- Such imbalance is a result of mismatch in the input transistors, e.g., unequal input bias currents and unequal base-emitter voltages.
- Often, an *input offset voltage* applied between the two input terminals is *required to balance the amplifier*.
  - Generally, the output offset voltage is not specified in data sheets because it depends on the closed loop gain, which is a design choice. Instead, the *INPUT OFFSETS* are specified.

**Output offset voltages are the result of two distinct input phenomena: input bias currents and input offset voltage.**

## Basic Definitions:

- **input bias current** =  $\frac{1}{2}$  the sum of the separate currents entering the two input terminals of a balanced amplifier.

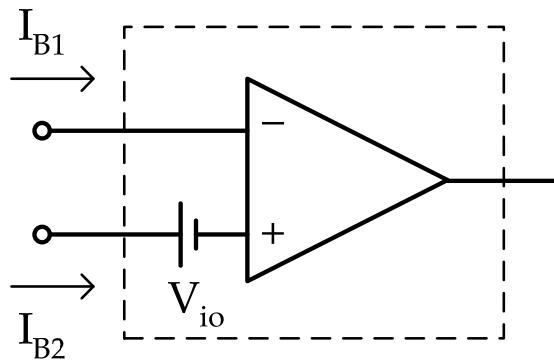
$$I_B = \frac{I_{B1} + I_{B2}}{2} \quad (1)$$

- **input offset current** =  $I_{io}$  - difference between the separate currents entering the input terminals of a balanced amplifier.

$$I_{io} = I_{B1} - I_{B2} \quad (2)$$

- **input offset voltage** =  $V_{io}$  - that voltage which must be applied between the input terminals to balance the amplifier.

Input Offset Drift  $\equiv \frac{dI_{io}}{dt}$  &  $\frac{dV_{io}}{dt}$



- NB: (1) and (2) above also give the following useful relations:

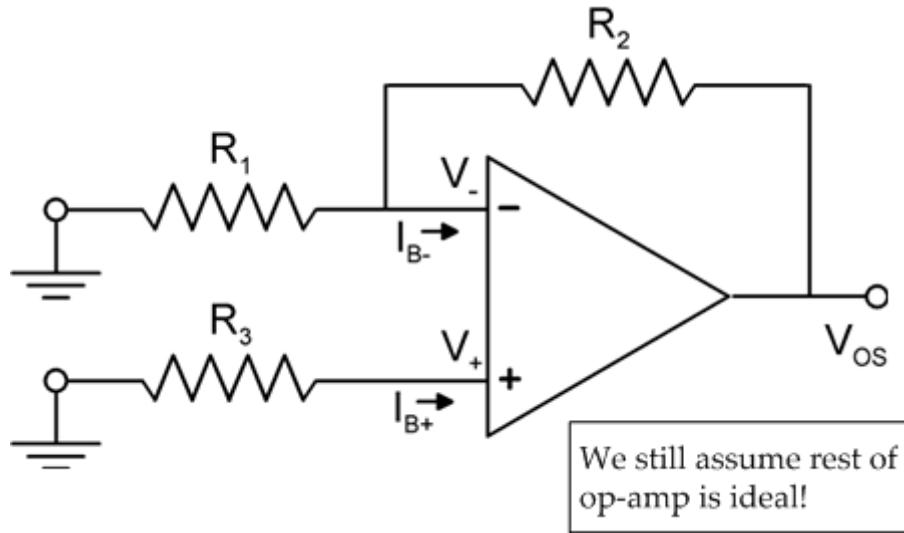
$$I_{B+} = I_B + 0.5|I_{io}|$$

$$I_{B-} = I_B - 0.5|I_{io}|$$

- NB: Can interchangeably use:

$$I_{B+} = I_{B2} \quad I_{B-} = I_{B1}$$

### 1.5.1 Calculation of Output Offset Voltages Due To Input Offset Current (assuming $V_{io} = 0$ )



$I_{B+}$  and  $I_{B-}$  are the input currents.

Need to calculate output offset voltage due to input currents.  
Use superposition.

(1) Consider first,  $I_{B+} = 0, I_{B-} \neq 0$ .

Then  $V_+ = 0$  since there is no voltage drop across  $R_3$ .

$\Rightarrow V_- = 0$ .  $\Rightarrow$  No voltage drop across  $R_1$ .

$\Rightarrow I_{B-}$  must flow through  $R_2$

$\Rightarrow V_{OS1} = R_2 I_{B-}$

(2) Next consider,  $I_{B-} = 0, I_{B+} \neq 0$ .

Then  $V_+ = -I_{B+} R_3 = V_-$

Current through  $R_1$  (also equal to current through  $R_2$ , since  $I_{B-}=0$ ):

$$\frac{V_-}{R_1} = \frac{-I_{B+} R_3}{R_1}$$

$$\therefore V_{OS2} = V_- + \left( \frac{-I_{B+} R_3}{R_1} \right) R_2 = -I_{B+} R_3 \left( 1 + \frac{R_2}{R_1} \right)$$

(3) Add:

∴ Output offset voltage due to input current (by superposition):

$$V_{OS} = V_{OS1} + V_{OS2}$$

$$= R_2 I_{B-} - R_3 \left( 1 + \frac{R_2}{R_1} \right) I_{B+} \quad (\text{A})$$

Depending on the relative sizes of the two terms on the right hand side, the offset voltage,  $V_{os}$ , can be positive or negative.

More interested in  $|V_{OS}(I_B)|$  if  $I_{B+} = I_{B-} = I_B$ , then have:

$$V_{OS}(I_B) = \left[ R_2 - R_3 \left( 1 + \frac{R_2}{R_1} \right) \right] I_B$$

For the output offset voltage to be zero, then

$$R_2 = R_3 \left( 1 + \frac{R_2}{R_1} \right)$$

$$\Rightarrow R_3 = R_1 // R_2$$

i.e., the output effect due to input bias currents can be **minimised** by connecting  $R_3$  having a value  $R_1//R_2$  in series with the non-inverting input—because the calculation is based on the assumption that  $I_{B-}=I_{B+}$ .

- Nevertheless, if we choose  $R_3=R_1//R_2$  then:

$$V_{OS}(I_B) = (I_{B-} - I_{B+}) R_2 \quad [\text{from (A)}]$$

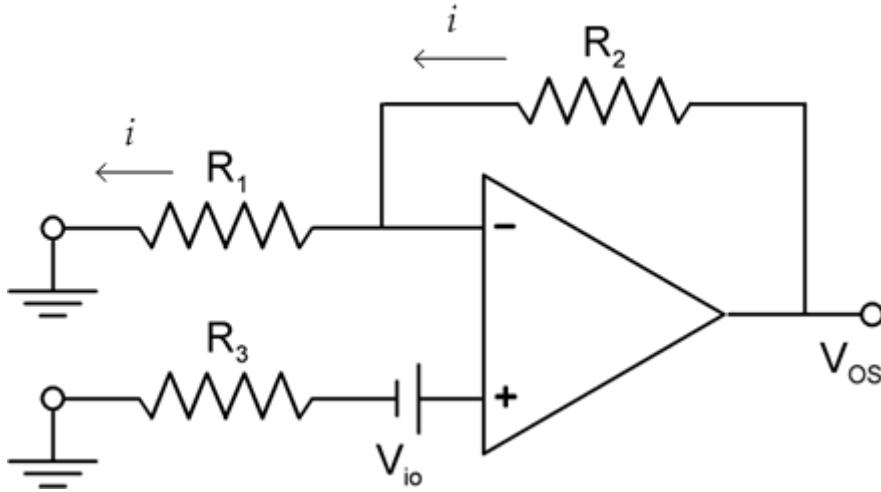
$$|V_{OS}(I_B)| = |I_{io} R_2|$$

i.e. Output offset voltage is proportional to the input offset current.  $I_B$  and  $I_{io}$  are specified by the manufacturers.

- Now using:
- $$I_{B+} = I_B \pm 0.5|I_{io}|$$
- $$I_{B-} = I_B \mp 0.5|I_{io}|$$

and given manufacturer values for  $I_B$  and  $I_{io}$ , we could calculate expected  $V_{os}$  for different configurations.

## 1.5.2 Calculation of Output Offset Voltages Due to Input Offset Voltage (assume $I_{B+} = I_{B-} = 0$ )



Thus  $V_+ = V_{io} = V_-$

Current through  $R_1$ :

$$i = \frac{V_-}{R_1} = \frac{V_{io}}{R_1}$$

$$\therefore V_{os}(V_{io}) = V_- + \left( \frac{V_{io}}{R_1} \right) R_2 = V_{io} \left( 1 + \frac{R_2}{R_1} \right)$$

### Note

- 1)  $R_3$  has no effect on  $V_{os}(V_{io})$ .
- 2) Input offset voltage is magnified by the factor equal to the closed-loop gain of the non-inverting amplifier.

$\therefore$  Total output offset voltage

$$|V_{os}| = |V_{os}(I_B)| + |V_{os}(V_{io})|$$

for the worst case analysis.

- So: Given  $I_B$ ,  $I_{io}$  and  $V_{io}$  from manufacturer, you could calculate the 'worst case' value of  $|V_{os}|$  by considering:

$$\left. \begin{aligned} I_{B+} &= I_B + \frac{1}{2} I_{io} \\ \text{or } I_{B+} &= I_B - \frac{1}{2} I_{io} \end{aligned} \right\} \begin{array}{l} \text{Choose whichever gives} \\ \text{biggest } |V_{os}(I_B)| \end{array}$$

## **SECTION – 2: SEMICONDUCTOR DEVICES FOR ELECTRONICS**

### **2.1 Semiconductor Basics**

- 2.1.1 Charge Carriers - Electronics & Holes**
- 2.1.2 Semiconductor Doping**

### **2.2 PN Junction Diodes**

- 2.2.1 PN Junctions**
- 2.2.2 Ideal & Non-Ideal Diode I-V Characteristics**
- 2.2.3 Reverse Bias Breakdown in Diodes**
- 2.2.4 Diodes as Voltage Limiters**

### **2.3 Bipolar Junction Transistors (BJTs)**

- 2.3.1 Modes of Operation**
- 2.3.2 Forward Active Mode, Basic I-V Relations & Current Gain  $\beta$**
- 2.3.3 Graphical Representation of BJT I-V Characteristics**
- 2.3.4 Ebers-Moll Model of BJT**
- 2.3.5 Base-Width Modulation (The Early Effect)**

### **2.4 MOS Field-Effect Transistors (MOSFETs)**

- 2.4.1 Device Structure and Physical Operation**
- 2.4.2 Current-Voltage Characteristics. Triode Region. Saturation Region.**
- 2.4.3 Threshold Voltage. Enhancement and Depletion Mode MOSFETs.**

## Aims

After this section the student should know:

- The Basics of charge carriers & doped semiconductors
- The behaviour of pn junctions in simple devices such as diodes and transistors
- The different modes of operation and characteristic curves of BJT and MOSFET devices.
- The cause of the Early effect

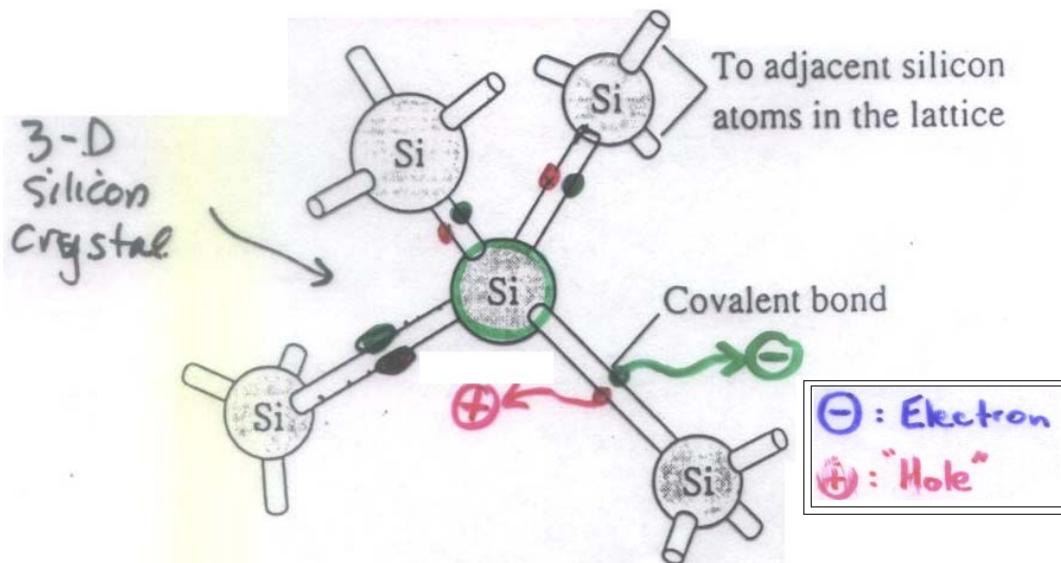
## 2.1 Semiconductor Basics

### Key Concepts:

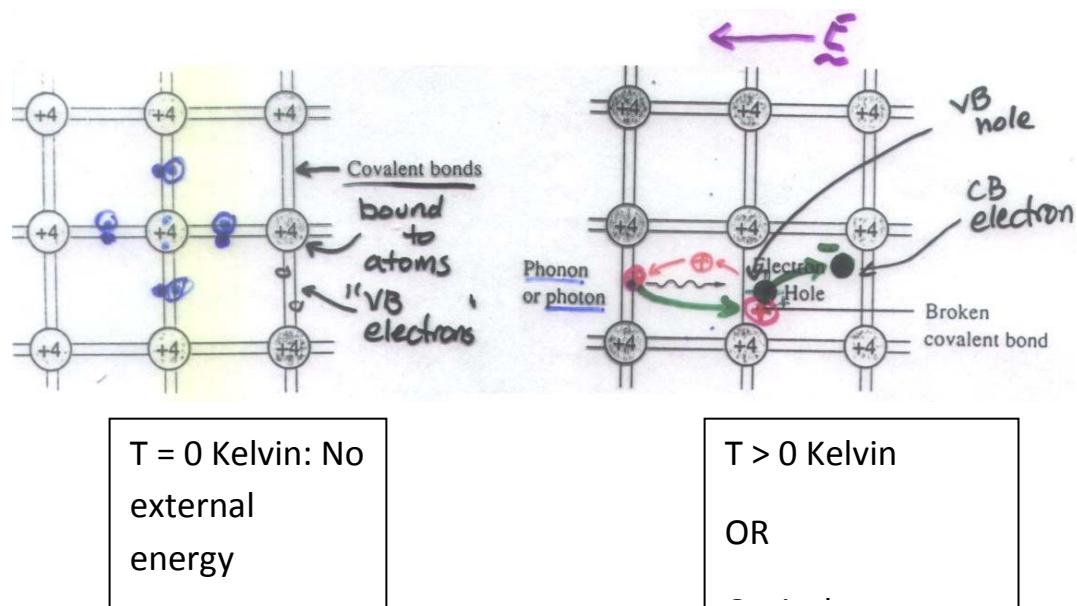
- Intrinsic (pure) semiconductors:  
(-) Electrons & (+) Holes for e.g. Si – Group IV
- Extrinsic (doped) semiconductors:
  - n-doped => mobile (-) e.g. P, As – Group V
  - p-doped => mobile (+) e.g. B, Ga – Group III
- p-n Junction => Diode
  - Ideal:  $I = I_o \left[ \exp\left(\frac{V_a}{V_T}\right) \right]$
  - Non-Ideal:  $I = I_o \left[ \exp\left(\frac{V_a}{nV_T}\right) \right]$
- Zener Diode
- Bipolar Junction Transistor (BJT)
  - Doping profile, current flows
  - $I_C = \beta I_B$   
 $V_{BE} \sim 0.7V$
  - Modes of Operation: Forward Active, Reverse Active
  - Ebers-Moll Model
  - Early Voltage ☐ "Base Width Modulation"
- MOSFETs
  - Qualitative description of MOSFET operation

- Current-Voltage characteristics
- Definition of threshold voltage
- Enhancement and Depletion mode MOSFETs

## 2.1.1 Charge Carriers – Electrons & Holes



### I. Intrinsic Silicon – Pure Silicon Only



CB(conduction band) electrons and VB(valence band) holes can move through semiconductor crystal

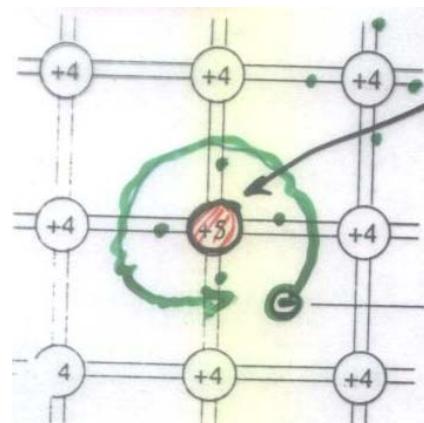
VB holes move by VB electrons hopping.



## 2.1.2 Semiconductor Doping.

Extrinsic (Doped) semiconductors contain small amounts of impurities. Typical doping levels are  $\sim 10^{19} \text{ cm}^{-3}$  -  $10^{18} \text{ cm}^{-3}$ .

### I. n-type (E.g. $^{15}\text{P}$ )



Group V impurities have 5 valence electrons – they “donate” the extra electron to the crystal: e.g. phosphorus, arsenic, antimony

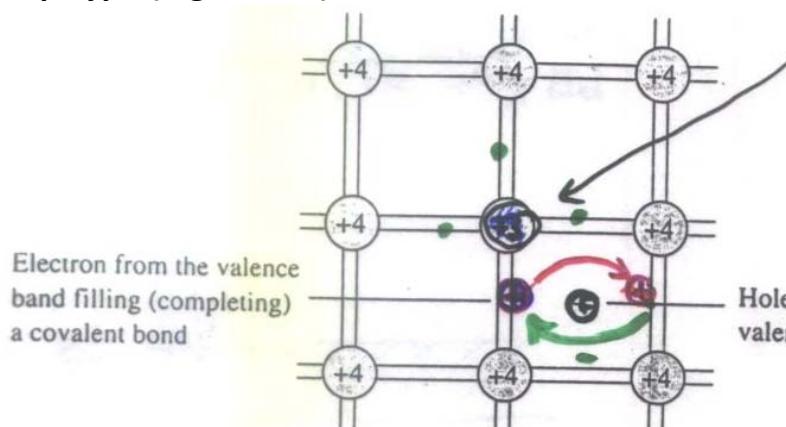
Fifth electron from column V dopant – very loosely bound

*Donor Impurities* – the fifth electron is weakly bound to the donor impurity, i.e. only a small energy is needed to move the electron into the CB.

This is called “n-type” because the electrons are extra negative carriers.

$$n = N_D + p \approx N_D \text{ for } N_D \gg p. \quad (\text{D = donors})$$
$$np = n_i^2$$

### II. p-type (E.g. Boron)



Group III impurities have 3 valence electrons – they “accept” a VB electron from the crystal: e.g. boron, gallium, indium.

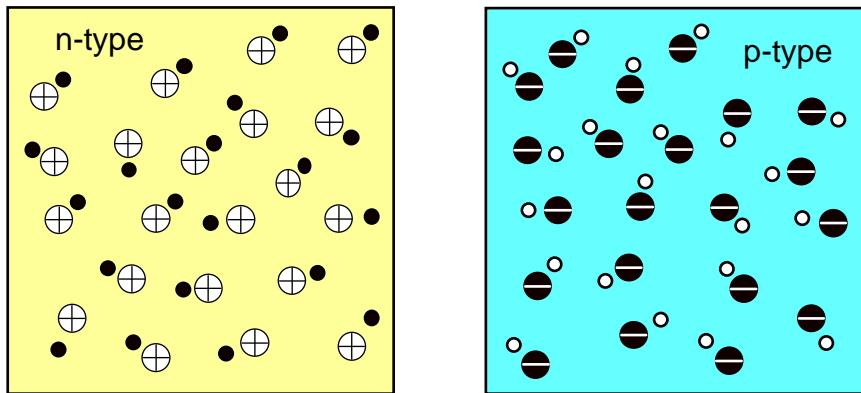
*Acceptor Impurities* – a valence band electron is accepted by the impurity leaving a weakly bound VB hole, i.e. only a small energy is needed to move this hole into the VB.

This is called p-type because the extra hole is a positive carrier

$$p = N_A + n \approx N_A \text{ for } N_A \gg n. \quad (\text{A} = \text{Acceptors})$$

## 2.2 PN Junctions

### 2.2.1 PN Junctions

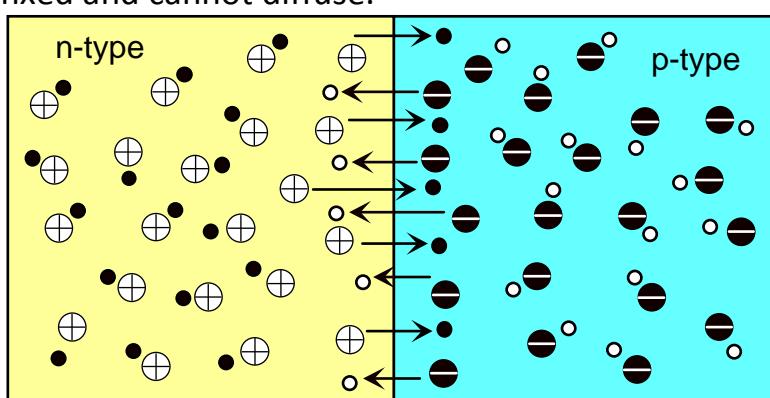


When n-type and p-type semiconductors are brought together, they form a *PN Junction*.

To start with, we will consider the case at *Thermal Equilibrium*, where there is no applied voltage bias or light or temperature.

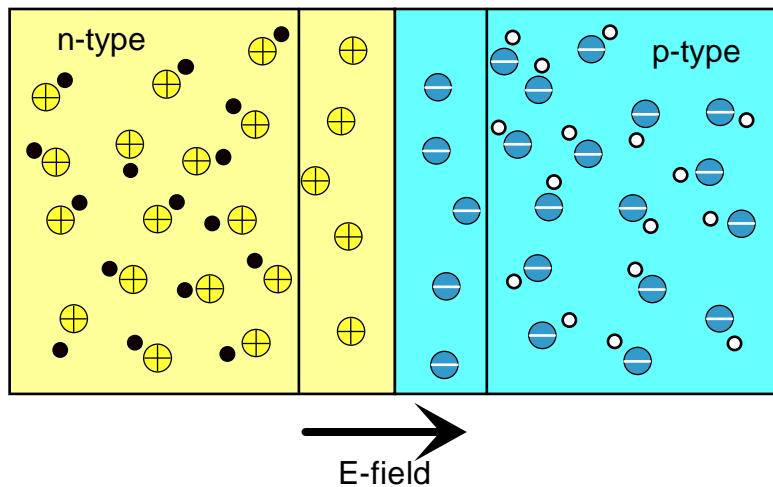
**Diffusion Current** consists of majority charge carriers moving from one side of the junction to the other due to a concentration gradient.

In pn junctions, electrons will diffuse from the n-type region to the p-type region while holes move from the p-type to n-type material. Donor atoms are fixed and cannot diffuse.



Movement across the junction causes recombination of electrons and holes, leaving the charged donors. The electric field that results presents a barrier to the diffusion current.

The region where this occurs is called the **depletion region** and has few electrons or holes.

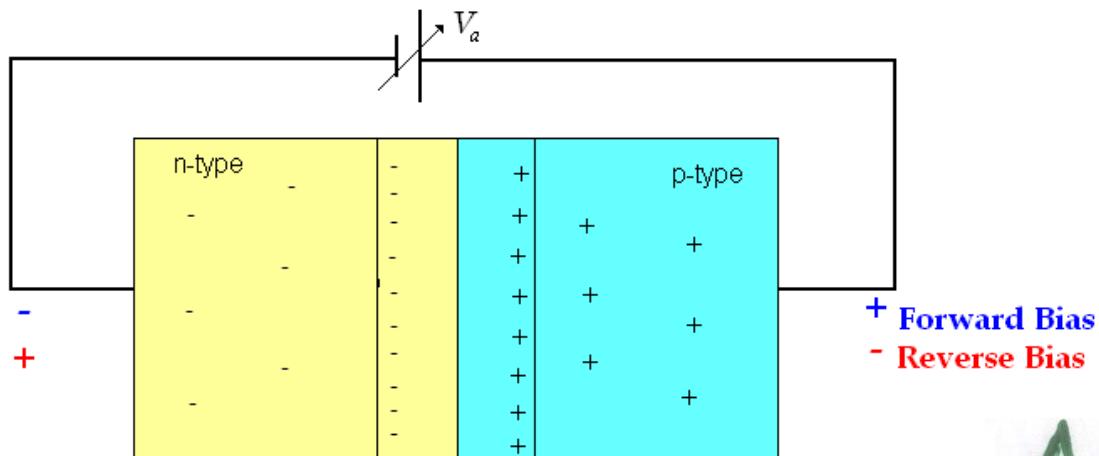


The **Drift Current** is the movement of carriers due to the internal electric field shown. The drift current will move *minority carriers* across the junction.

Normally, the drift current is very small unless the carrier concentration is increased due to temperature, optical generation or injection of carriers.

**Under equilibrium conditions, the net current is 0. The diffusion current equals the drift current for both electron and holes currents.**

## 2.2.2 Ideal and Non-Ideal Diodes

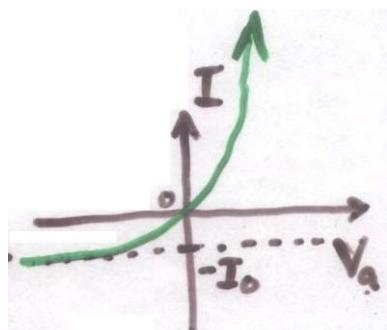


If we apply a voltage across a PN junction like the one above, it will behave as a **diode**.

The current through an *ideal* diode is given by:

$$I = I_0 \left[ \exp\left(\frac{qV_a}{kT}\right) - 1 \right]$$

$$I = I_0 \left[ \exp\left(\frac{V_a}{V_T}\right) - 1 \right]$$



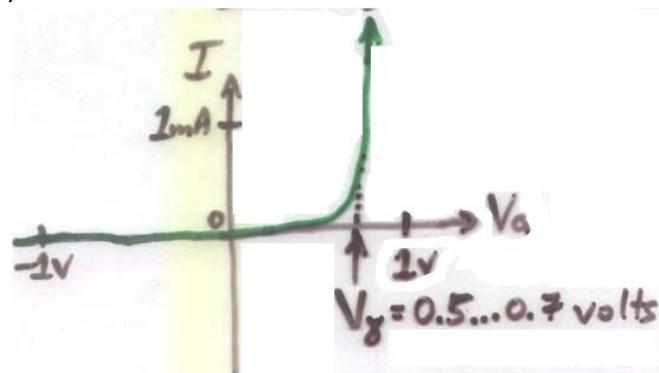
Where

$$V_T = kT/q = 25mV \text{ at } 300K \text{ and } I_0 = qA \left( \frac{D_n n_i^2}{L_n N_A} + \frac{D_p n_i^2}{L_p N_D} \right)$$

A real diode has a non-ideality factor  $n \geq 1$ . In this case:

$$I = I_0 \left[ \exp\left(\frac{V_a}{nV_T}\right) - 1 \right]$$

For this course, we assume  $n=1$ .



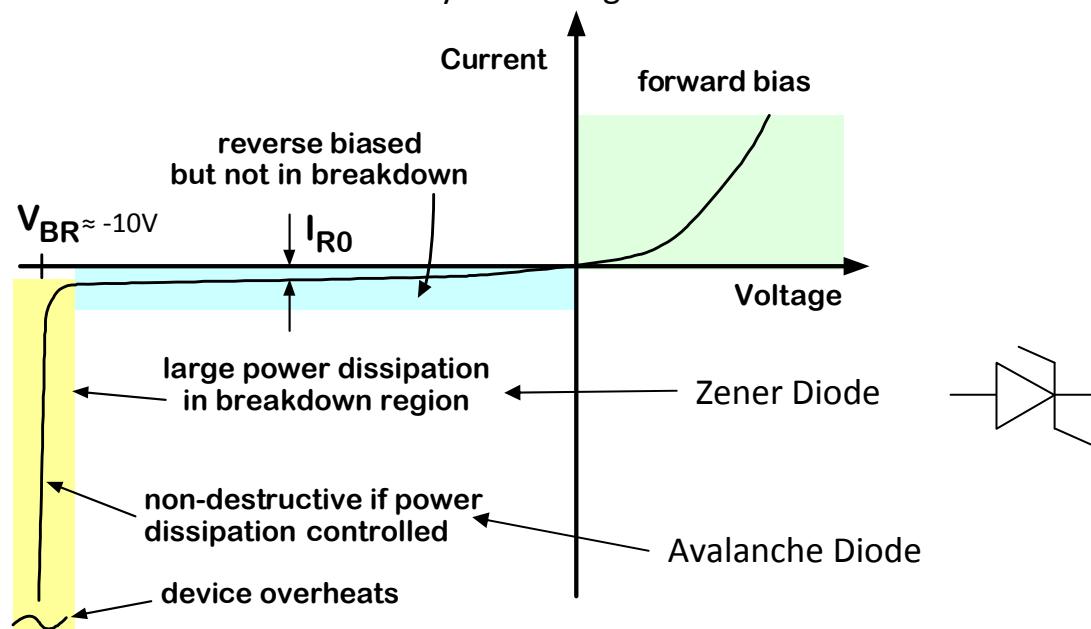
### Comments on currents in PN Junctions

- The majority carrier current is comprised of both diffusion and drift components. This means that the *electric field cannot be zero*. **Majority current is predominantly drift current.**
- Physically, the majority carriers corresponds to the carriers that must be supplied from the other side of the junction to recombine with the minority carriers.
- Increasing the *recombination rate* or increasing the *mobility increases the forward bias current.*
- The higher the minority carrier concentration, the greater the forward bias current. The minority carrier concentration decreases as the doping increases, so the more heavily doped side dominates the current flow.

## 2.2.3 Reverse Bias Breakdown

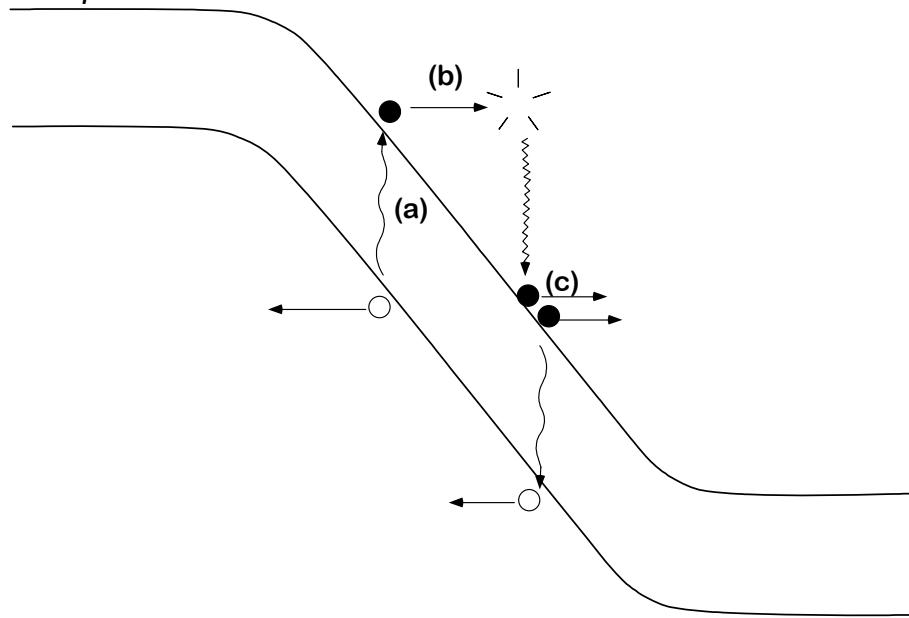
### Reverse Biased PN Junction

- Reverse bias increases the electric field at the junction.
- Barrier to diffusion current is increased, reducing the diffusion current.
- Drift current remains unchanged, or increases slightly as the depletion region is enlarged.
- According to diode equation, only very small current flows, but there are several mechanisms by which larger currents flow.



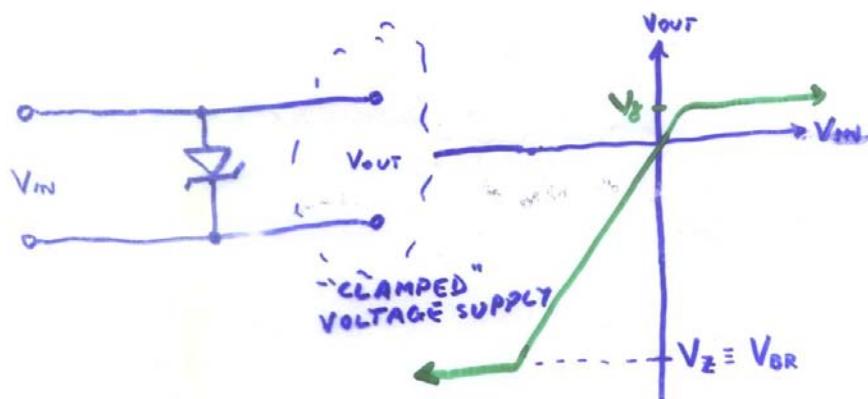
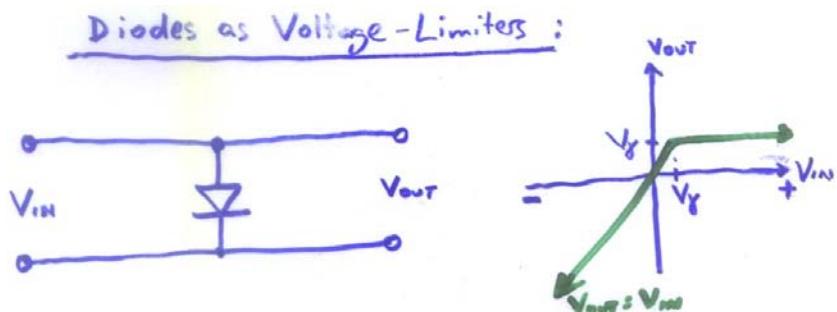
### Avalanche breakdown

- Increasing electric field in depletion region will increase force with which carriers collide with lattice atoms.
- At a certain critical energy, the collision between the carrier and the atoms ionises the atom (removes a carrier, such that it is free). This is called impact ionisation.



## 2.2.4 Diodes as voltage-limiters

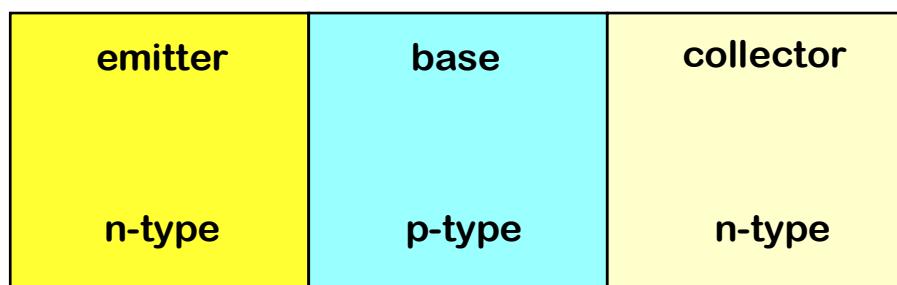
Diodes can be used to fix a voltage as shown in these two diagrams of a diode and zener diode.



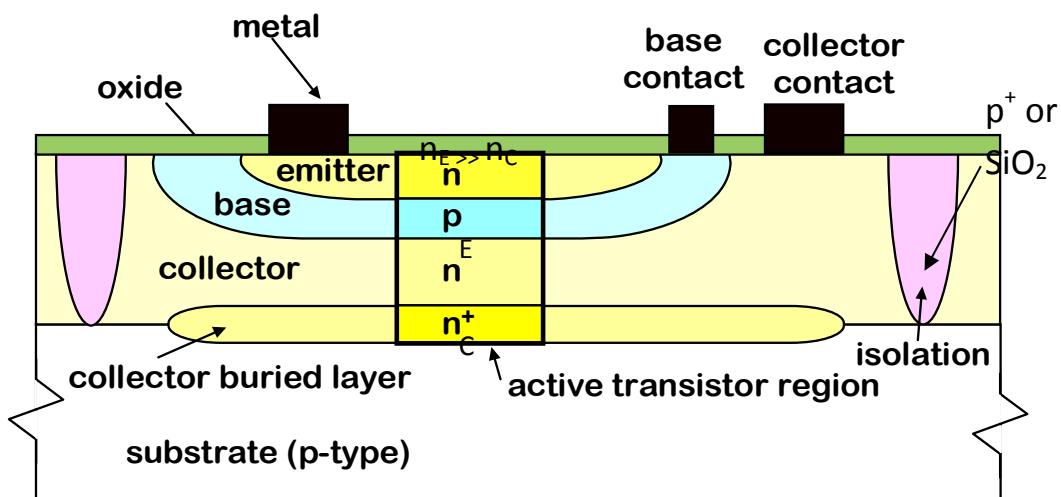
## 2.3 Bipolar Junction Transistors (BJTs)

### 2.3.1 Modes of Operation

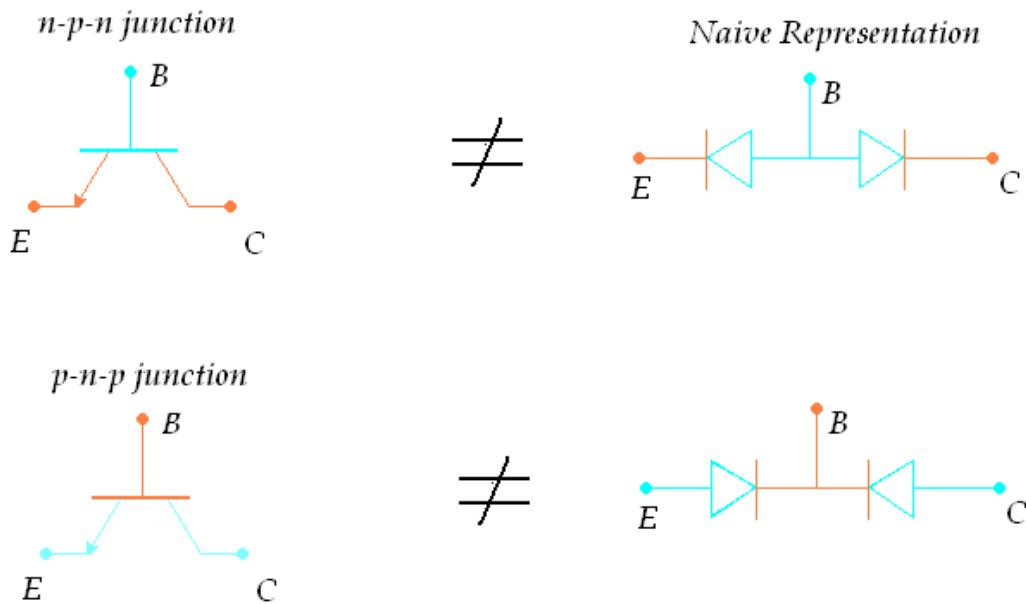
A bipolar junction transistor is a three terminal device which consists of two pn-junctions. A simplified cross section is simply two back-to-back pn junctions.



The actual cross section of the device would look more like:



- The key to the operation of a BJT is that the central region is thin enough such that minority carriers can cross the base, allowing the emitter and collector to “communicate”.
- BJTs are extensively used in many applications including both analog circuits and digital ICs.



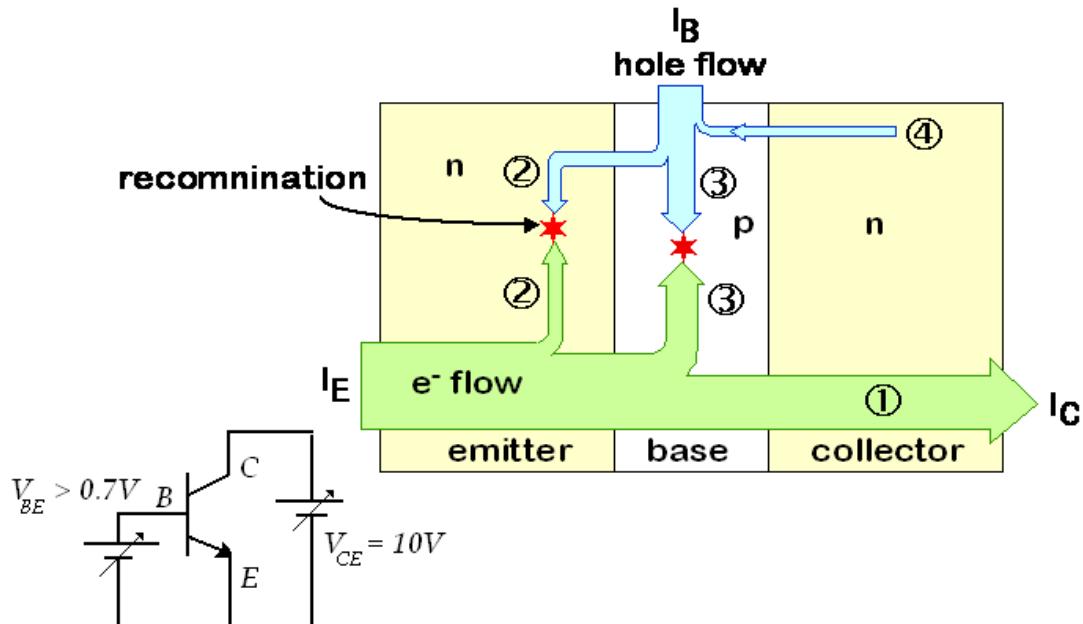
**Key Understanding:** Thin enough base layer to allow transmission of minority carriers without recombination

Depending on the biasing of the two junctions, the device can be operating in one of three basic modes:

- **Active mode** (one junction forward biased and one reverse biased): If EB is forward biased, called forward active. If other way around called reverse active. Transistor acts like a current-controlled constant current source. Most commonly used mode of operation.
- **Saturation** (both junctions forward biased): Not many applications actually use the saturation mode intentionally, but in many circuits the transistors enter the saturation region while switching between active and cut-off.
- **Cut-off** (both junctions reverse biased): no current flows in the transistor.

## 2.3.2 Forward Active Mode - Basic I-V relations

- The base-collector junction is reverse biased and has a strong electric field across it which will sweep any minority carriers reaching the BC junction into the collector.
- In the collector, the carriers are majority carriers and the collector current will be the number of minority carriers injected into the base at the EB junction which make it across the base.
- Because there are not many carriers recombining in the base region, the base current will be small.



The **emitter current** is a combination of

- electrons injected into base from emitter (① + ③ on diagram)
- electrons replacing electrons recombining with holes injected from base into emitter (② on diagram).

The **base current** is comprised of

- holes injected into emitter from forward bias of EB junction ②
- holes replacing holes which have recombined with electrons in base ③
- holes generated in collector (usually due to thermal generation) and swept across BC junction into base ④. This term is very small term and is often neglected.

The **collector current** is primarily electrons in the base being swept from base to collector due to E-field at BC junction ①.

### Basic I-V Relations

A BJT is similar to a current-controlled current source.

The **base current is the controlling current**, with the emitter and collector currents related to the base current by the **current gain** or beta

value ( $\beta$  or  $h_{FE}$ ), which is typically quite large (50-100), providing **current amplification**. For an *npn* BJT, we have:

$$\begin{aligned} I_C &= \beta I_B = h_{FE} I_B \\ I_E &= I_C + I_B \\ I_E &= (\beta + 1) I_B \\ I_C &= \alpha I_E \\ \beta &= \frac{\alpha}{1 - \alpha} \end{aligned}$$

The factor  $\alpha$  is a measure of how much of the emitter current makes it across the base region to the collector. The value for  $\alpha$  is typically  $> 0.99$  for a high-quality BJT. The higher the value of  $\alpha$ , the higher the value of  $\beta$ .

The emitter current  $I_E$  can be approximated, as for a diode, consisting of the emitter and base regions:

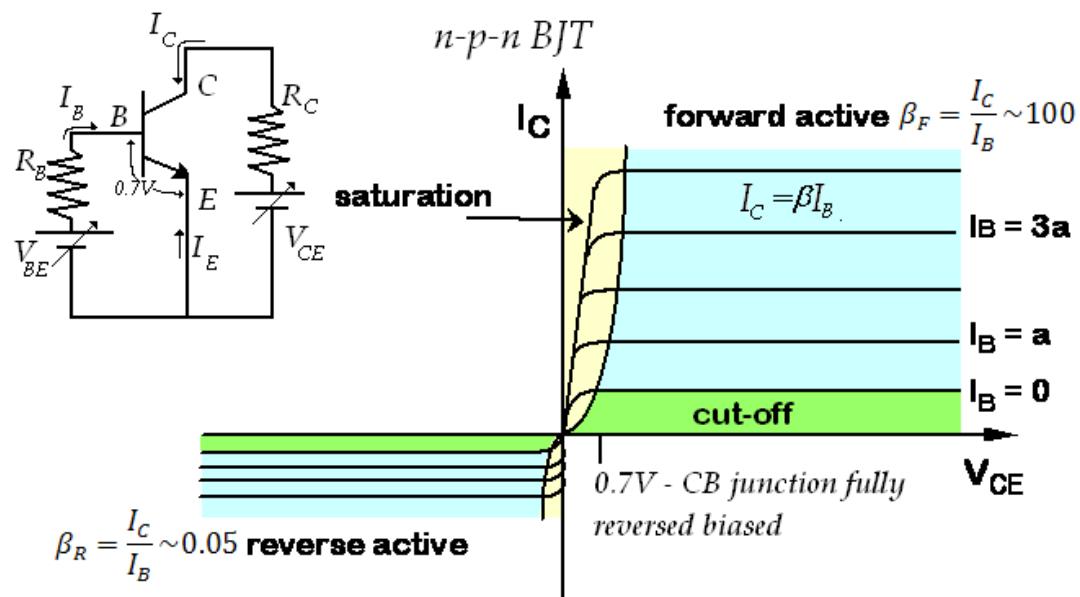
$$\begin{aligned} I_E &= I_S [e^{qV_{BE}/kT} - 1] = I_S [e^{V_{BE}/V_T} - 1] \\ V_T &= kT/q \approx 25.8 \text{ mV at } T = 300K \end{aligned}$$

**N.B.:** Rarely use this to solve circuits – if you find yourself using it, then chances are you have got the question wrong so start again!

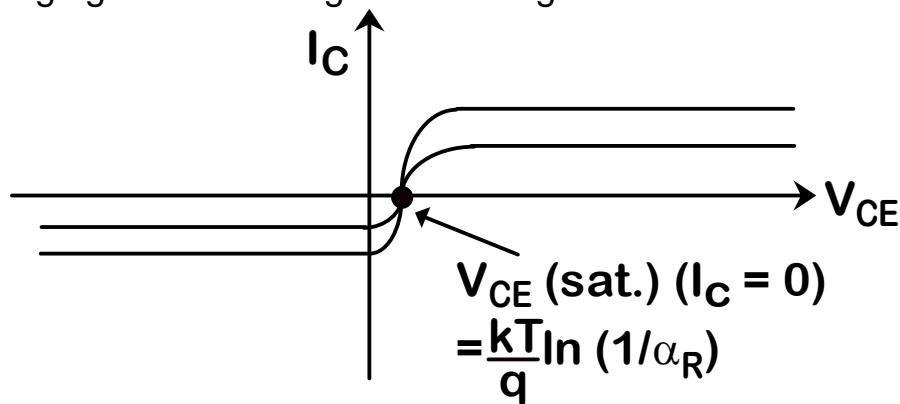
Typically,  $V_{BE} = 0.6\text{-}0.7 \text{ V}$  for a silicon BJT when the emitter current is flowing. Typically, the saturation current is  $I_S \sim 10^{-14} \text{ A}$ .

It must be stressed that using a particular value of  $\beta$  is a bad way to design a circuit. It can vary an enormous amount since it depends on collector current, collector-to-emitter voltage and temperature, amongst other things. A circuit using a BJT should be designed to operate with  $\beta$  in its specified range, but should be immune to changes in  $\beta$ , which can be achieved using feedback.

## 2.3.3 Graphical Representation of I-V Characteristics



- $\beta$  in reverse mode is smaller than  $\beta_F$  due to doping gradients
- Unless the emitter and collector junction are identically the same and there is zero recombination in the base,  $V_{CE} \neq 0$  when  $I_C = 0$ .
- Note that  $I_C = \beta I_B$  only applies in the active region.
- Enlarging the low voltage current region:



## 2.3.4 Ebers-Moll model of a BJT

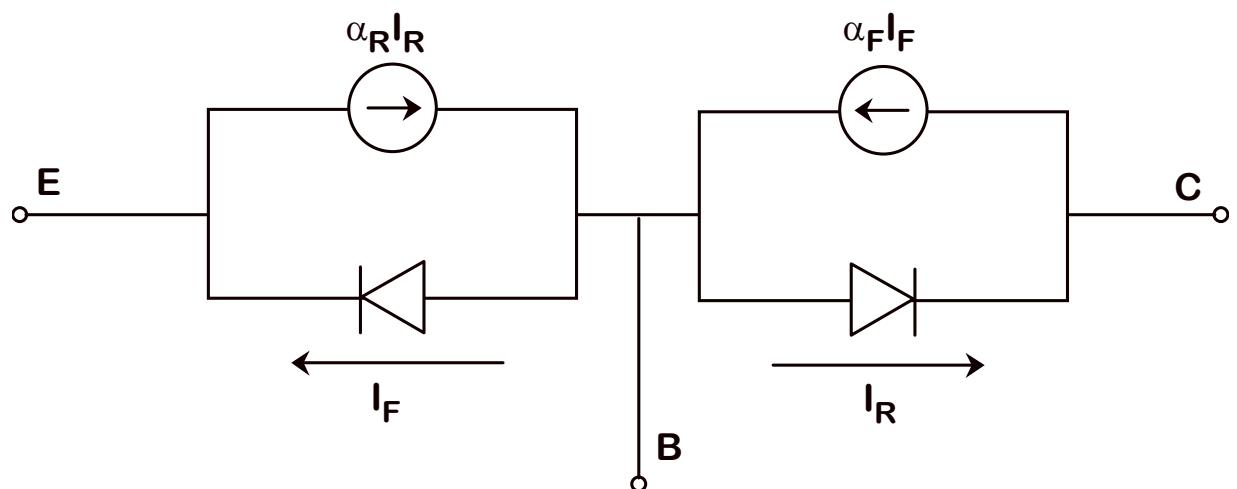
Ideal D.C. properties of a transistor result in terminal properties which can be described by the Ebers-Moll equations:

$$I_E = -I_F + \alpha_R I_R = -I_{ES} \left( e^{\frac{qV_{BE}}{kT}} - 1 \right) + \alpha_R I_{CS} \left( e^{\frac{qV_{BC}}{kT}} - 1 \right)$$

$$I_C = \alpha_F I_F - I_R + \alpha_R I_R = \alpha_F I_{ES} \left( e^{\frac{qV_{BC}}{kT}} - 1 \right) - I_{CS} \left( e^{\frac{qV_{BE}}{kT}} - 1 \right)$$

$$I_B = I_E - I_C$$

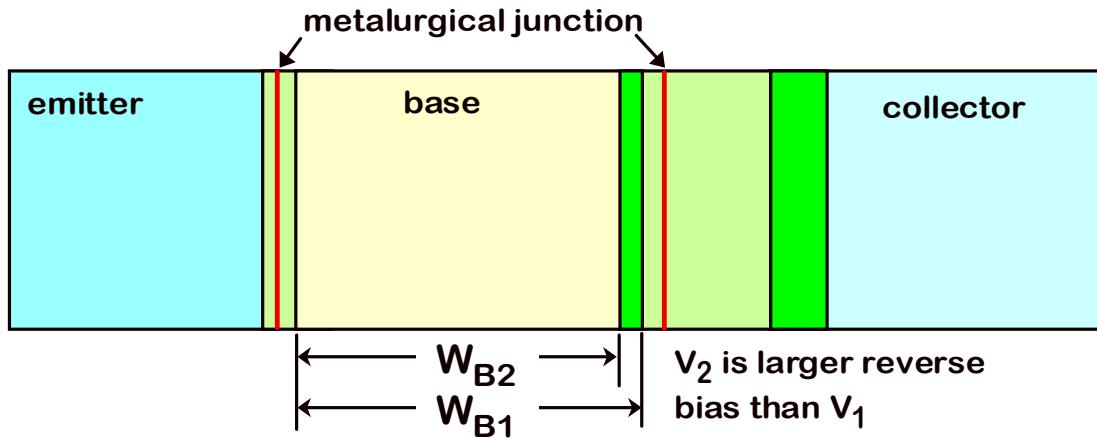
Equivalent Circuit:



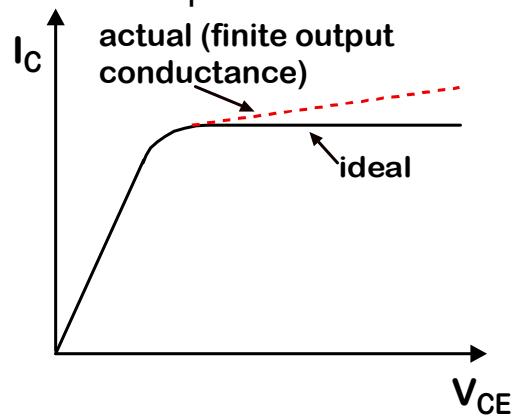
## 2.3.5 Base-Width Modulation (The Early Effect)

### Base Width Modulation

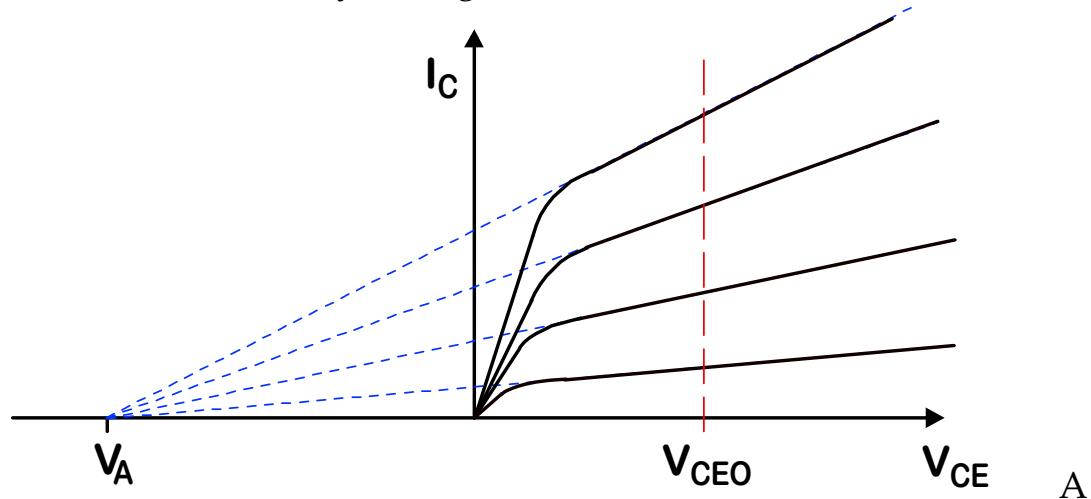
- So far, we have assumed the base-width is constant.
- In fact, the base width varies with applied voltage due to differences in the width of the quasi-neutral region and the distance between the metallurgical junctions



- This results in a finite output conductance



- Experimentally, tangents to common emitter curves at fixed  $V_{CE}$  can intercept voltage axis at an approximately constant voltage  $V_A$  called the Early Voltage.



sufficient condition to get an Early voltage is that  $\beta_F = f(V_{CE})g(V_{EB})$  where  $f$  and  $g$  are functions of the stated variables only.

- **Punch-through** is an extreme of base-width modulation which occurs when the entire base region becomes depleted.
- When the base region is depleted, there is no barrier to current flow such that the emitter and collector are effectively shorted.
- When punch-through occurs, current increases suddenly and sharply.
- Occurs primarily in transistors with narrow and/or lightly doped base

## 2.4 MOS Field Effect Transistors

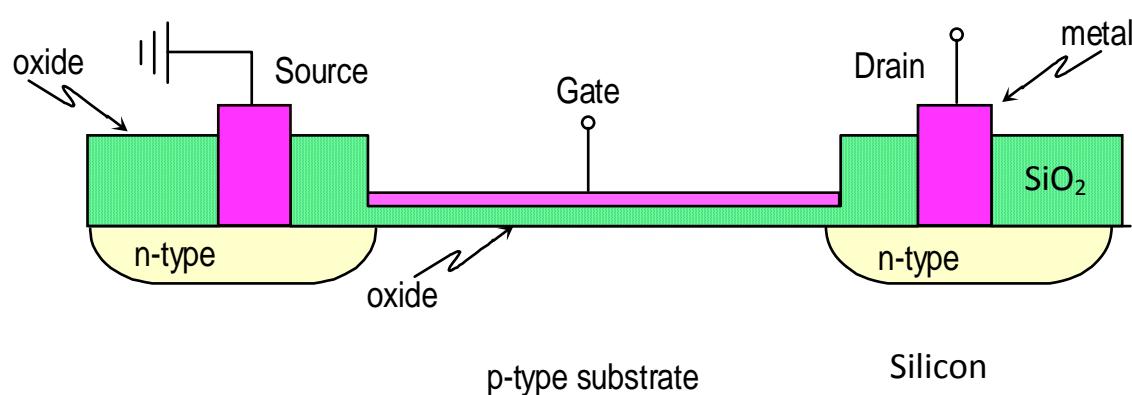
(Metal Oxide Semiconductor Field Effect Transistor)

### 2.4.1 Device Structure and Physical Operation

- I-V curve of a MOSFET is similar to that of a BJT, but it is based on different principles.
- MOSFETs were first proposed in 1930's, although technological problems with surface states prevented fabrication of useful devices before 1960's.
- Subsequently, MOSFETs have experienced rapid increase and today are the dominant IC technology.
- MOSFETs are unipolar devices - majority carriers only.

#### Qualitative Description of MOSFETs

- A MOSFET consists of two back to back diodes.



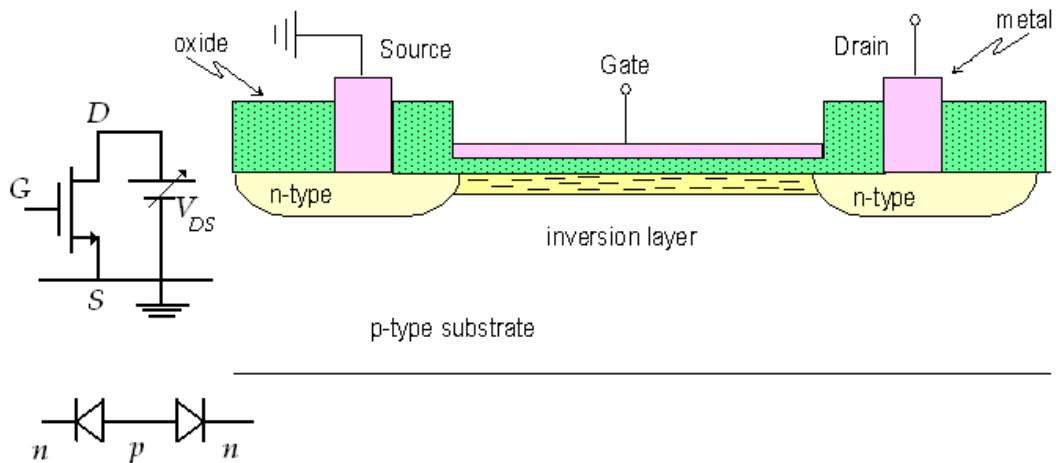
- If a voltage is applied across the source and drain, the current flow between the drain and source is very small (typically on the order of the reverse current in a diode). This region of operation is called **cut-off**.

### 2.4.2 Current Voltage Characteristics

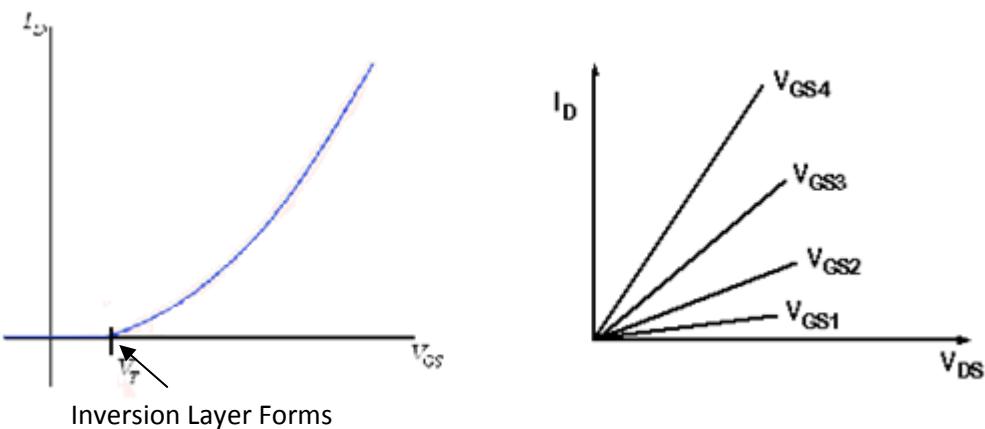
#### Triode Region

- The current from the source to the drain can be increased by connecting the two with a conductive channel.

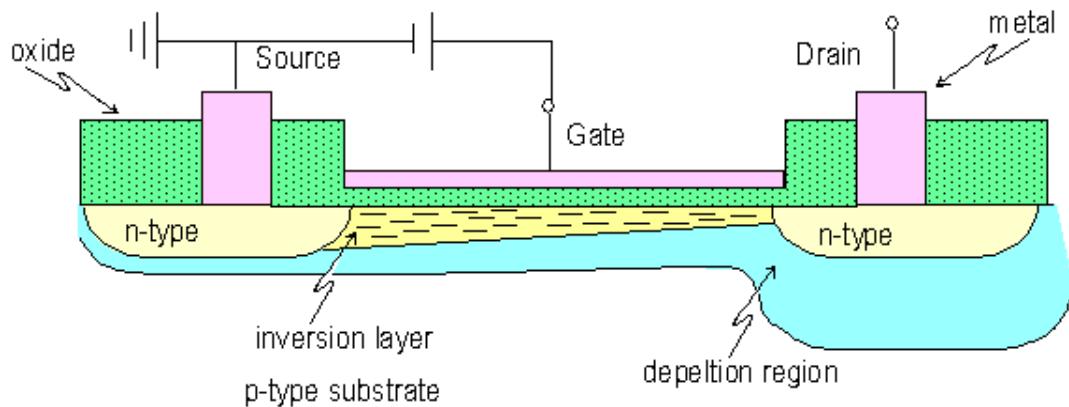
- An n-channel device refers to a channel with electrons (i.e., a p-type substrate), p-channel refers to a channel formed from holes (i.e., an n-type substrate).
- A channel between the source and drain can be formed by creating an inversion layer under the gate.
- For p-type substrates, this voltage should be positive such that negative charges are attracted under the gate.



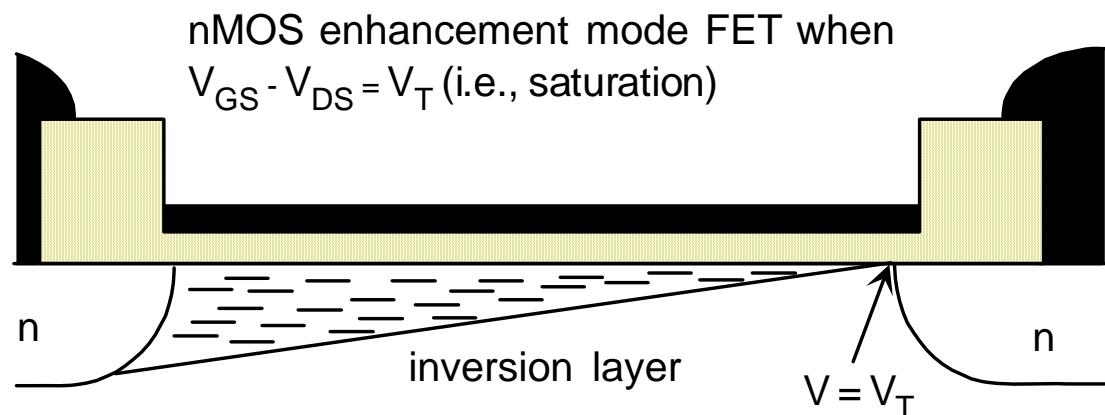
- The **threshold voltage** ( $V_T$ ) is the minimum voltage to create an inversion layer under the gate.
- When there is an inversion layer across the entire channel and there is an applied voltage across the source and drain, the device is in the *ohmic* or *triode* region.
- The resistance of the conducting channel depends on the length of the channel (i.e., the source-drain distance) and on the “depth” or number of carriers in the channel (which in turn depends on the applied gate voltage).
- In this region, the device acts as a voltage controlled resistance.



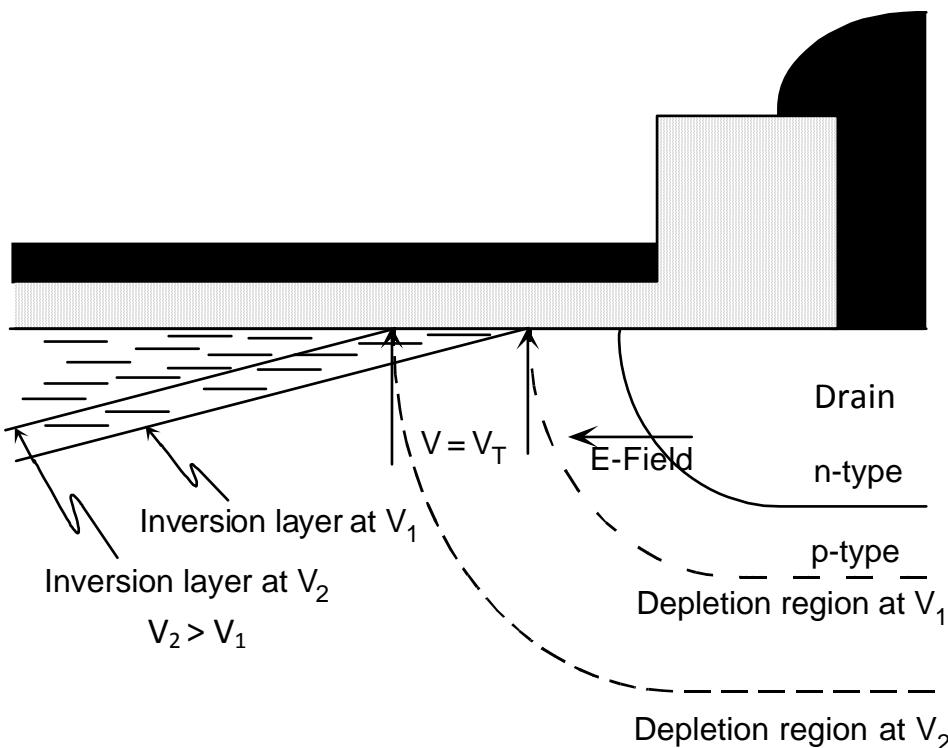
## Saturation Region



- In order to maintain an inversion layer, the gate voltage must always be **LARGER** than the drain voltage by at least  $V_T$ .
- When  $V_G - V_D < V_T$ , then there is no longer an inversion layer near the drain and the MOSFET is in the saturation region.

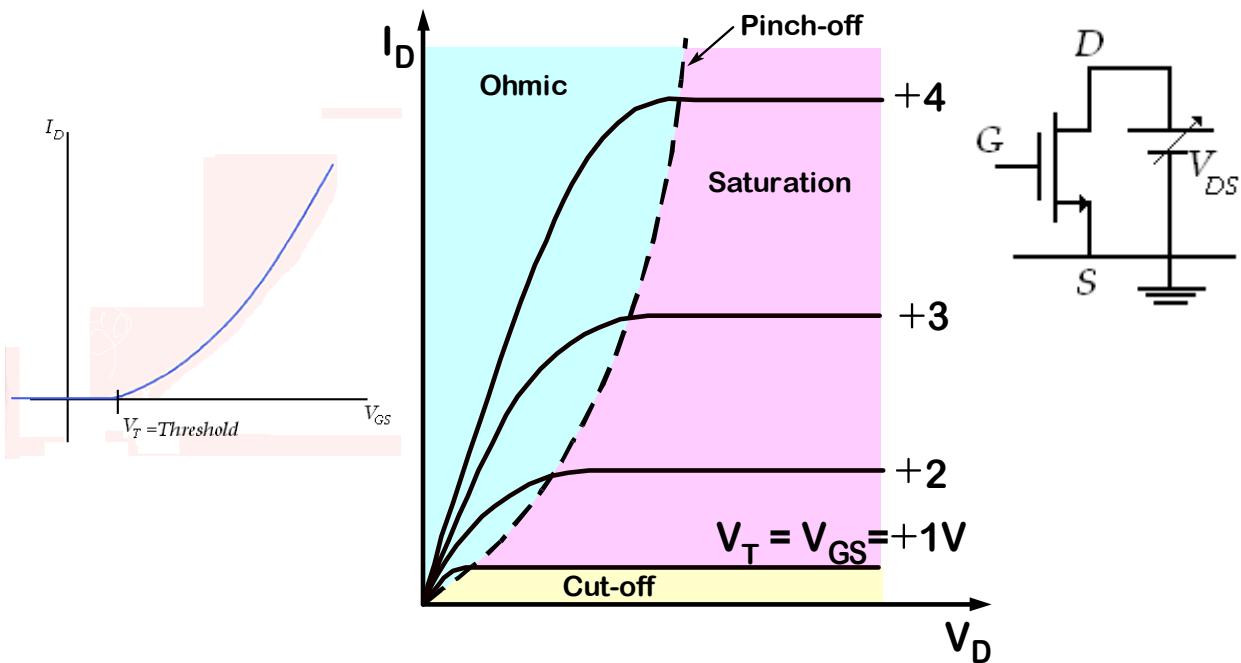


- As  $V_D$  is further increased, the voltage in the semiconductor surrounding the drain also increases. Therefore, the voltage where  $V_G - V_D = V_T$  moves further away from the drain, into the channel.



- The voltage at the edge of the inversion layer always equals  $V_T$  and the voltage at the source remains constant as well. Therefore, once the device is in saturation, the voltage across the channel is constant.
- The change in distance at which  $V=V_T$  is relatively small, since in the depletion region of a semiconductor the voltage drop can be large. *Therefore, the channel length, to first order does not change.*
- Since neither the channel resistance nor voltage change, the current through the inversion region does not change. Consequently, as  $V_D$  is further increased past the onset of saturation, the *current flowing through the device remains constant*.
- The electric field at the boundary does not provide a barrier to current flow. The depleted region is a reverse biased diode, and incident minority carriers are swept across this region very quickly.

- The I-V curves then are:



### 2.4.3 Threshold Voltage – Enhancement and Depletion mode MOSFETs

- Inversion is defined as the condition at which the device has the same number of carriers as the substrate, but of opposite polarity.
- Threshold voltage is voltage required to achieve this condition.
- Mathematically, work function is voltage to get flat band + enough voltage at surface of semiconductor to get inversion.
- The chart on the next page shows how the threshold voltage determines whether a MOSFET is depletion or enhancement mode based on the type of charge carrier in the channel.

PG 309 SCE

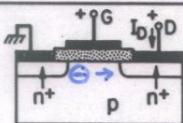
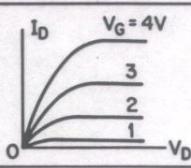
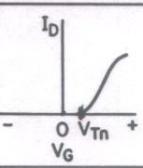
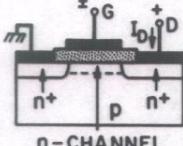
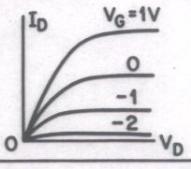
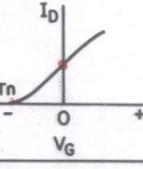
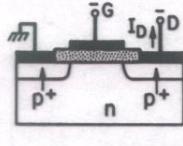
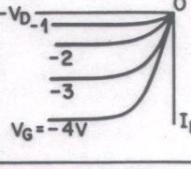
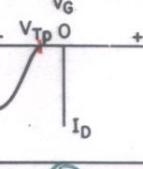
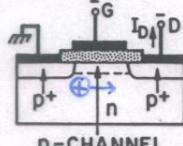
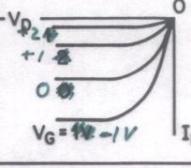
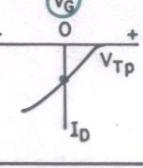
TYPE	CROSS SECTION	OUTPUT CHARACTERISTICS	TRANSFER CHARACTERISTICS
n-CHANNEL ENHANCEMENT (NORMALLY OFF)			
n-CHANNEL DEPLETION (NORMALLY ON)			
p-CHANNEL ENHANCEMENT (NORMALLY OFF)			
p-CHANNEL DEPLETION (NORMALLY ON)			

Fig. 40 Cross sections and output and transfer characteristics of four types of MOSFETs.

$V_{Tn}$  for n-ch.  
 $V_{Tp}$  for p-ch.

# **SECTION 3: TRANSISTOR AMPLIFIERS: SMALL SIGNAL ANALYSIS & DC BIASING**

## **3.1 The BJT Small-Signal Model**

- 3.1.1 Linearization and Definition of g-parameters**
- 3.1.2 Early effect and Determination of  $r_o$**
- 3.1.3 Low Frequency Hybrid- $\pi$  Model**
- 3.1.4 Full Hybrid- $\pi$  Model (for High-Frequency)**
- 3.1.5 Small-Signal Analysis – Converting from DC to AC**
- 3.1.6 The Common Emitter Amplifier**

## **3.2 MOSFET Small-Signal Model**

- 3.2.1 Linearization and Graphical Analysis**
- 3.2.2 Small Signal Model**
- 3.2.3 The Common-Source Amplifier**

## **3.3 DC Biasing of Transistor Amplifiers**

- 3.3.1 Basic DC Analysis of BJT Circuits**
- 3.3.2 Biasing of BJT Amplifier Circuits. Discrete Biasig.  
Current Mirrors**
- 3.3.3 Basic DC Analysis of MOSFET circuits**
- 3.3.4 Biasing of MOSFET Amplifier Circuits**

### **Aims**

After this section the student should know:

- Hybrid- $\pi$  model for BJT's in the cases of high, low and mid-band frequencies.
- Transistor arrangements to construct current sources.
- How to perform mid-band analysis of transistor circuits.

In this section, we shall look at the development of circuit models for the BJT. These models will be used for the analysis of amplifier circuits using transistors. For all of the analysis, the following will be assumed:

- The transistor is operating in the appropriate mode. For a BJT this is the active mode.
- The biasing of the circuit has established the desired DC conditions to give the required large-signal output voltage swing.

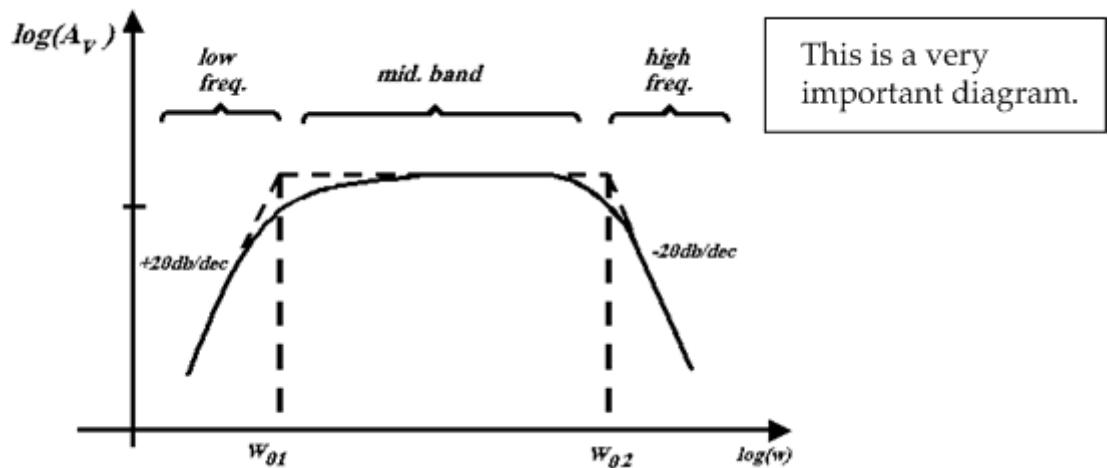
For each analysis we will try to calculate:

1. **Amplifier gain.**
2. **Input impedance.**
3. **Output impedance.**
4. **Frequency response.**

Our approach to the analysis of the amplifier circuits will be the following:

1. Model the circuit in a form suitable for AC analysis, i.e., connect all points at the same AC potential together.
2. Model the active devices in terms of small-signal linear approximations.

The frequency response of the amplifier circuits can be broken down typically into three regions: **low frequency**, **mid-band** and **high frequency**. The graph below illustrates these different regions of operation.



In general, the gain of the circuit will drop off at high and low frequencies, with a range of frequencies at which the gain remains constant. As will be shown, there are designs that can remove the low-frequency drop-off and also to push the drop-off at high frequencies further out. Furthermore, knowing which region of frequency the input signal is in helps to simplify our task.

## 3.1 BJT Small Signal Model

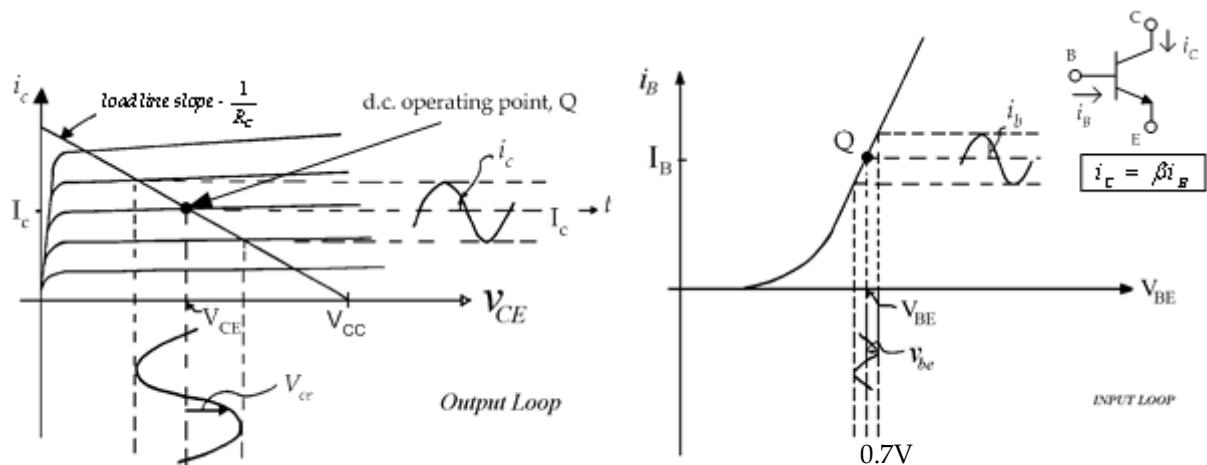
[See Sedra & Smith Section 4.8.]

### 3.1.1 Linearization and Definition of g-parameters

In this section we will look at the complete hybrid- $\pi$  model for BJT's and its use to analyse circuits of varying complexity.

The small-signal model will not consist of only resistors and a controlled current source. If we recall the properties of a  $p-n$  diode, one important property was that there is a capacitance between the  $p$  and  $n$  regions of the diode. Since a BJT is essentially two diodes back to back, we would expect there to be capacitances between the  $p$  and  $n$  regions of the BJT.

The input and output loops for a transistor in an amplifier circuit is shown below.



The variations in the base and collector currents can be written in the following form:

$$i_b(v_{be}, v_{ce}) = g_\pi v_{be} + g_\mu v_{ce}$$

$$i_c(v_{be}, v_{ce}) = g_m v_{be} + g_o v_{ce}$$

so that a linear mathematical model can be constructed for small-signal incremental variables of a transistor about a given operating Q-point. The g-parameters are incremental conductances and are functions of the operating Q-point.

The transistor characteristics can be conveniently expressed as:

$$i_B(v_{BE}, v_{CE}) \quad , \quad i_C(v_{BE}, v_{CE})$$

where the labelling convention is such that the total base current

$$i_B = I_B + i_b \quad \text{small signal variations about the Q-point}$$

↑      ↘  
DC base current at Q-point

$$i_C = I_C + i_c = i_C^Q + di_C$$

$$\text{Similarly, } v_{BE} = V_{BE} + v_{be}$$

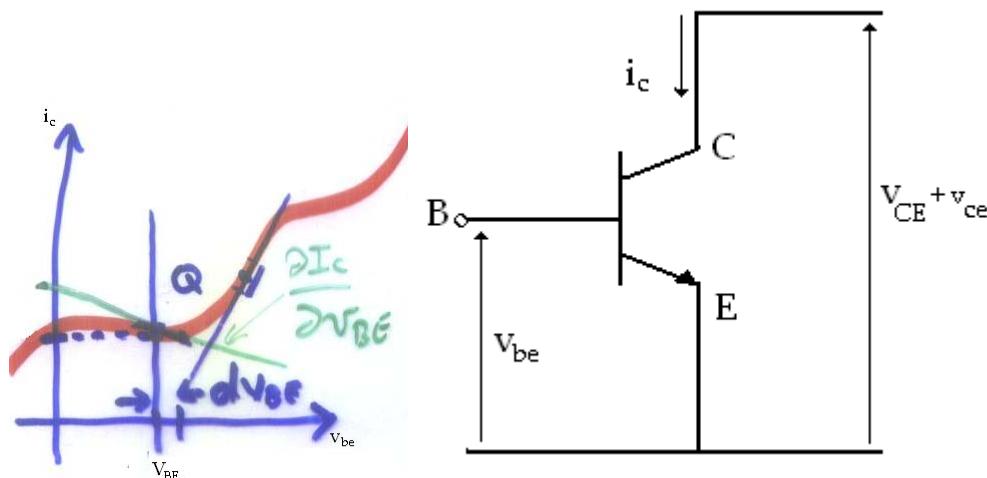
$$v_{CE} = V_{CE} + v_{ce}$$

Now  $i_B$  and  $i_C$  are functions of two variables; we take a Taylor expansion of the function about the Q-point and consider only the first-order terms by assuming that the small signal inputs are small

$$di_C = \left( \frac{\partial i_C}{\partial v_{BE}} \Big|_Q \right) \cdot dv_{BE} + \left( \frac{\partial i_C}{\partial v_{CE}} \Big|_Q \right) \cdot dv_{CE} = g_m v_{be} + g_o v_{ce}$$

$$di_B = \left( \frac{\partial i_B}{\partial v_{BE}} \Big|_Q \right) \cdot dv_{BE} + \left( \frac{\partial i_B}{\partial v_{CE}} \Big|_Q \right) \cdot dv_{CE} = g_\pi v_{be} + g_\mu v_{ce}$$

**NB:** The  $g_m$ ,  $g_\pi$ ,  $g_o$  and  $g_\mu$  are just parameters that we choose to define as the differential conductances:  $\left. \frac{\partial i}{\partial v} \right|_Q$



$$i_c(V_{BE} + dv_{be}) = I_C + \left( \frac{\partial I_c}{\partial v_{be}} \right) \cdot dv_{be} = I_C + i_c$$

### (i) $g_m$ & $g_\pi$ in the hybrid- $\pi$ model

Assume, for convenience, an  $npn$  transistor in the forward active mode.

The collector current is given by

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right) \quad \text{where } I_S = \text{saturation current}$$

and the base current

$$i_B = \frac{I_S}{\beta} \exp\left(\frac{v_{BE}}{V_T}\right) \quad \text{where } V_T = \frac{KT}{q} = 26mV \text{ at } 300K$$

Assuming  $I_S$  and  $\beta$  are constant,  $g_m$  and  $g_\pi$  can be obtained by differentiating the above expressions w.r.t.  $v_{BE}$  and evaluating at the Q-point values. Giving:

$$g_m \equiv \left. \frac{\partial i_C}{\partial v_{BE}} \right|_Q = \frac{1}{V_T} \cdot I_S \exp\left(\frac{v_{BE}}{V_T}\right)$$

$$= \frac{1}{V_T} \cdot i_C \approx \frac{I_C}{V_T}$$

$$g_m = \frac{I_C}{V_T}, \quad g_\pi = \frac{I_B}{V_T} = \frac{g_m}{\beta} = \frac{I_C}{\beta V_T}$$

$$g_\pi = \frac{1}{r_\pi}$$

### (ii) $g_o$ and $g_\mu$ in the hybrid- $\pi$ model

$$\text{By definition, } g_o \equiv \left. \frac{\partial i_C}{\partial v_{CE}} \right|_Q$$

This is the slope of the  $i_C(v_{CE})$  characteristic, given by the Early effect as:

$$g_o = \frac{I_C}{V_A} \quad \text{where } V_A \equiv \text{Early voltage}$$

$$g_\mu \equiv \left. \frac{\partial i_B}{\partial v_{CE}} \right|_Q = \frac{1}{\beta} \cdot \left. \frac{\partial i_C}{\partial v_{CE}} \right|_Q = \frac{1}{\beta} \cdot g_o \quad \text{giving:}$$

$$g_\mu = \frac{g_o}{\beta} = \frac{I_C}{\beta V_A}$$

**A Note on Magnitudes:** The  $g$  parameters are related by

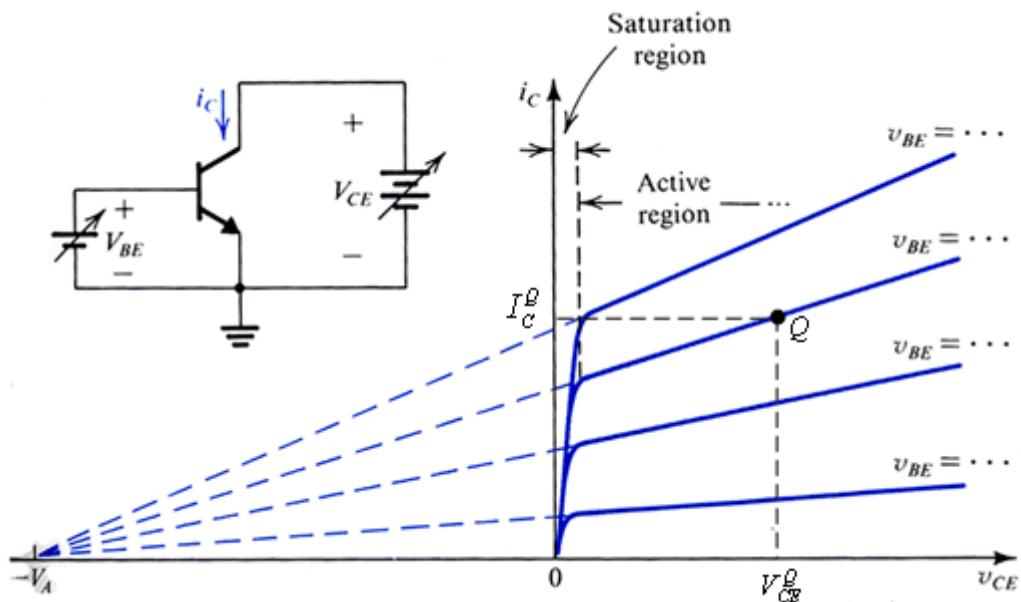
$$g_\pi = \beta g_\mu, \quad g_o = \beta g_\mu, \text{ so in general } g_m \gg g_\pi \gg g_o \gg g_\mu$$

### 3.1.2 Early Effect and Determination of $r_o$

#### Base Width Modulation (The Early Effect)

[See Sedra & Smith Section 4.5]

When practical BJT's are operating in the active region, you will notice that the  $i_C-v_{CE}$  curves are not perfectly horizontal lines, but have finite slopes (as shown in the graph below). This is caused by an effect known as Base-Width Modulation (also referred to as the Early Effect).



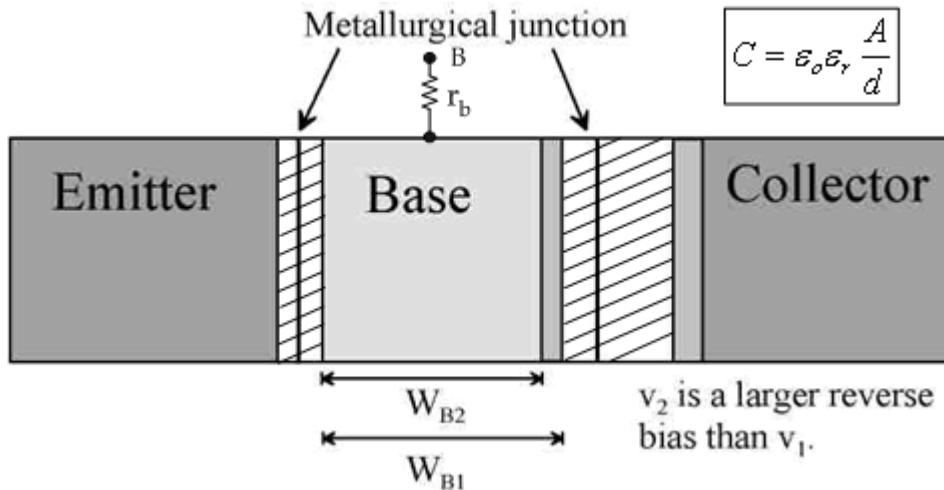
Source: Microelectronic Circuits 4<sup>th</sup> Ed. By Sedra & Smith.

Experimentally, tangents to common emitter curves at fixed  $v_{CE}$  can intercept the voltage axis at an approximate constant voltage  $V_A$  called the *Early voltage*.

**NB:** The slope is  $\frac{\partial i_C}{\partial v_{CE}} = \frac{I_C^Q}{(V_A + V_{CE}^Q)} \approx \frac{I_C^Q}{V_A}$  since usually  $V_A \gg V_{CE}^Q$

## How Base-Width Modulation Works

At a given value of  $v_{BE}$ , variation in  $v_{CE}$  changes the size of the depletion width at the C-B junction and changes the effective base width,  $W$ .



As illustrated in the diagram above:

By increasing  $v_{CE}$ , we are really increasing the reverse-bias voltage across the C-B junction.

The depletion region of this junction is thus increased, resulting in a decrease in the effective base width,  $W$ .

Since  $I_S$  is inversely proportional to  $W$ ,  $I_S$ , and hence  $i_C$ , will increase. This is base-width modulation.

**Note:** Each of the incremental conductances is directly proportional to the quiescent collector current  $I_C$  and are functions of temperature and collector voltage.

For  $\beta$  large and  $V_T/V_A < 1/\beta$ , typically:

$$g_m \gg g_\pi \gg g_o \gg g_\mu \quad r_\mu \gg r_o \gg r_\pi \gg \frac{1}{g_m}$$

If we neglect the effects of base-width modulation [i.e.,  $V_A = -\infty$ ],

$$g_o = g_\mu = 0$$

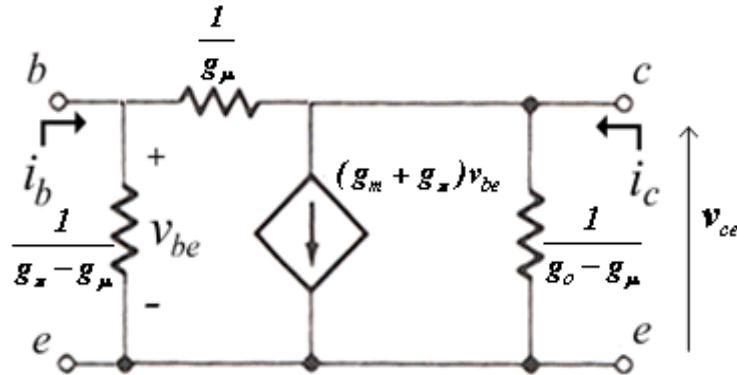
Example: given an *n-p-n* transistor  $\beta = 40$ ,  $I_C = 2\text{mA}$ ,  $V_A = -65$  volts

$$g_m = 80 \text{ m}\Omega^{-1} \quad g_\pi = 2 \text{ m}\Omega^{-1}$$

$$g_o = 0.031 \text{ m}\Omega^{-1} \quad g_\mu = 0.00077 \text{ m}\Omega^{-1}$$

### 3.1.3 Low Frequency Hybrid- $\pi$ Model

The following linear incremental circuit model can be derived.

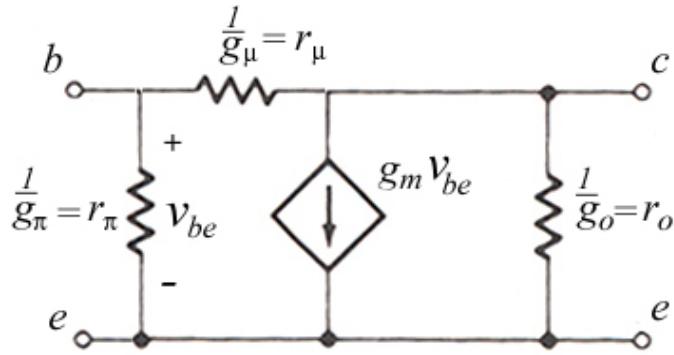


Because of the relative sizes of the g-parameters, we can simplify the above model to this. This model suffices for low-frequency analysis.

Low-Freq Small Signal Model for BJT

$$g_m \gg g_\pi \gg g_o \gg g_\mu$$

$$r_\mu \gg r_o \gg r_\pi \gg \frac{1}{g_m}$$



$$\begin{aligned} \text{Eg: } g_o &= 1 \mu\text{s} \\ &= 10^{-6} \Omega^{-1} \\ \Rightarrow r_o &= \frac{1}{g_o} \\ &= 10^6 \Omega = 1 \text{ M}\Omega \end{aligned}$$

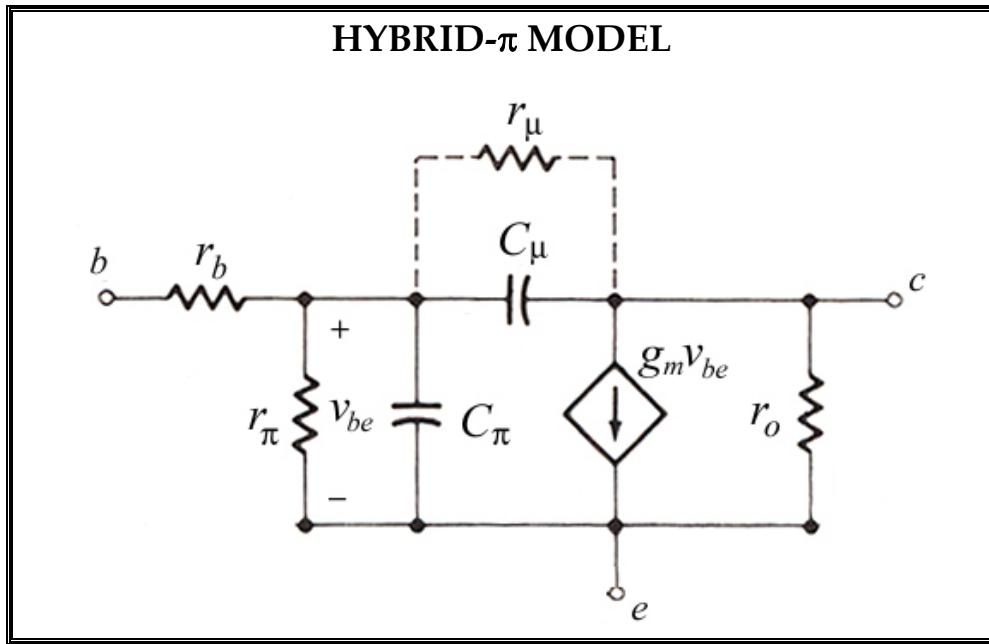
In this course, the above model will also suffice for mid-band analysis.

At this level, the small-signal model for the BJT is only partially complete. We need to augment the model to incorporate other parameters that relate to the physical structure and physics of operation of the device:

- extrinsic resistances
- parasitic capacitances
- charge-storage capacitances

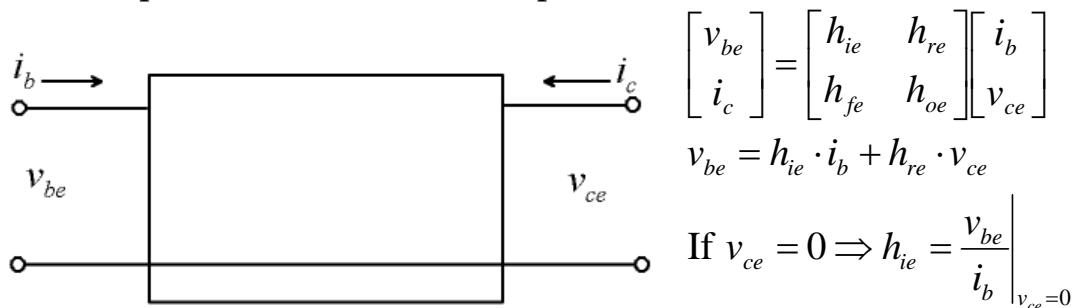
### 3.1.4 Full hybrid- $\pi$ Model (for High-Freq)

For this course, our complete model for high-frequency analysis will be as follows. **You must MEMORIZE this model:**



Typically,  $C_\pi \approx 10\text{-}20\text{ pF}$ , while  $C_\mu$  will be approximately an order of magnitude smaller

- We can also express a BJT as a two port network by specifying a common emitter (CE).
- Some transistor data-sheets provide information in terms of h-parameters for this two-port network.



The h-parameters and the g-parameters are related by the following expressions.

$$\left. \begin{array}{l} h_{ie} = r_b + r_\pi \\ h_{re} = \frac{r_\pi}{r_\mu} \\ h_{fe} = g_m r_\pi \\ h_{oe} = g_o + g_m h_{re} \end{array} \right\} \text{(taking } g_m \gg g_\pi \gg g_o \gg g_u \text{), so}$$

$$\begin{aligned} g_m &= \frac{|I_C|}{V_T} \\ r_\pi &= \frac{h_{fe}}{g_m} \\ r_b &= h_{ie} - r_\pi \\ r_o &= \frac{1}{h_{oe} - g_m h_{re}} \\ r_\mu &= \frac{r_\pi}{h_{re}} \end{aligned}$$

Note that  $h_{fe}$  is equivalent to  $\beta$ .

### 3.1.5 Converting from DC to AC Equivalent

To convert a DC circuit to an AC equivalent for small signal analysis, there are two steps.

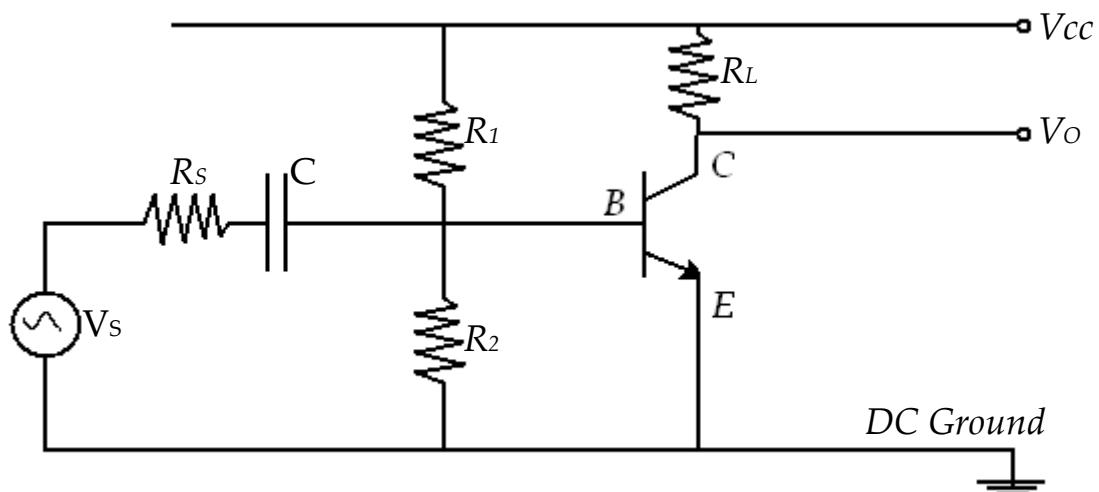
Step 1:

- Convert to AC equivalent circuit
- DC voltage sources  $\equiv$  AC Ground

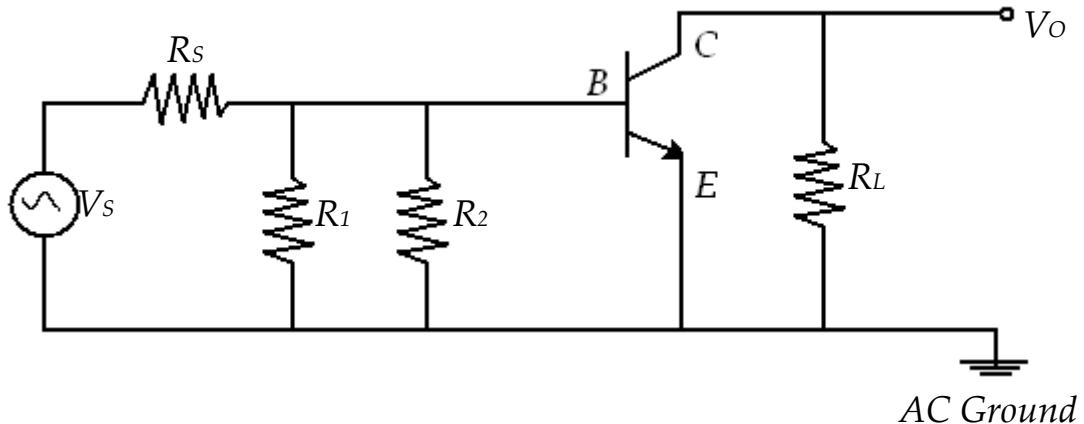
Step 2:

- Replace non-linear transistor with linear small signal model.

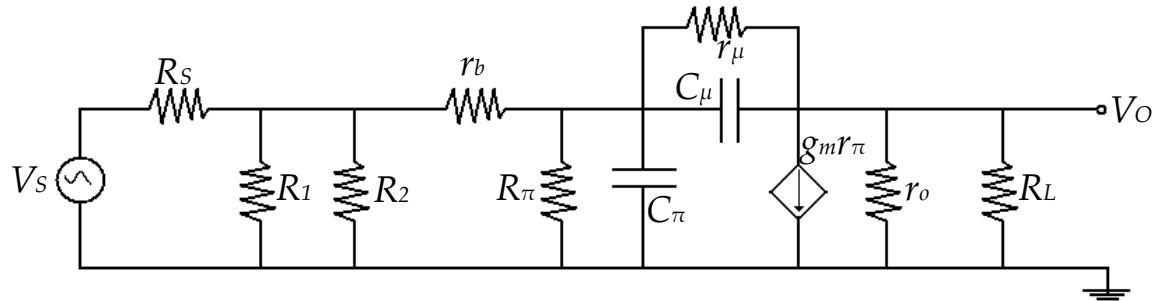
As an example, consider a typical “common-emitter” amplifier:



Firstly, we assume that C is very large, and can be short-circuited, and the DC voltage at Vcc is an AC earth.



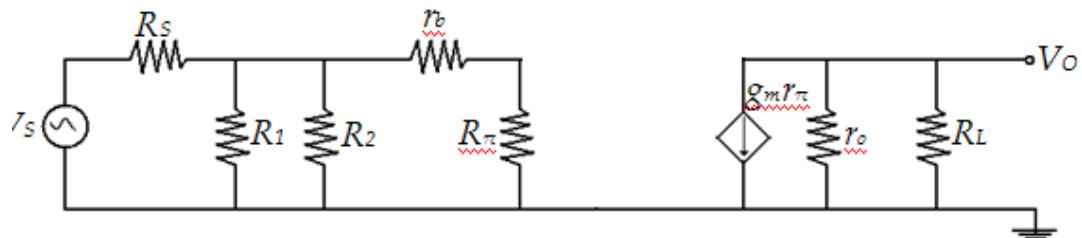
In step 2, we replace the transistor with the small-signal model.



### 3.1.6 The Common Emitter Amplifier

We will now look at a complete example of using the Hybrid- $\pi$  model by continuing with the Common-Emitter Amplifier from above.

From the AC equivalent circuit we found in the previous section, we can find the **mid-band voltage gain** for the circuit by realising that the small values of  $C_\mu$  and  $C_\pi$  mean that they need only be considered at higher frequencies (since  $Z_C = 1/\omega C$ ) and can be replaced by open circuits for mid-band and low-frequency calculations. For this problem, assume  $g_\mu = 0$  and  $r_\mu = \infty$ .



The first thing to do is find an expression for  $V_\pi$  in terms of  $V_s$ .

$$V_\pi = \frac{r_\pi}{r_\pi + r_b} \cdot \frac{(r_\pi + r_b) \parallel R_1 \parallel R_2}{(r_\pi + r_b) \parallel R_1 \parallel R_2 + R_S} \cdot V_s$$

On the output side of our circuit, the current source is feeding current to both  $R_L$  and  $r_o$ . This means that the output voltage can be written as:

$$V_o = -g_m V_\pi R_L \parallel r_o$$

We now possess the information needed in order to find the gain of the circuit for mid-band. The voltage gain is given by:

$$A_V = \frac{V_o}{V_s} = \frac{-\beta(R_L \parallel r_o)}{r_\pi + r_b} \cdot \frac{(r_\pi + r_b) \parallel R_1 \parallel R_2}{(r_\pi + r_b) \parallel R_1 \parallel R_2 + R_S} \quad [\text{Recall } \beta = g_m r_\pi]$$

Typically we can also neglect  $r_x$  and will also have  $R_s \ll r_\pi$  which means that the gain can be written:

$$A_V \approx -g_m (R_L \parallel r_o) \rightarrow -g_m R_L$$

By making  $R_s$  small, we have removed the dependence on the current gain  $\beta$ .

### What about the input and output impedances?

The **input impedance** is found by looking into the circuit from the node B. This can be seen to be  $r_x + r_\pi$ . Remember that the two halves of the circuit are essentially isolated from each other, so the input signal doesn't 'see'  $r_o$  or  $R_L$ .

The **output impedance** is found by looking into the circuit at node C with  $V_s$ , and hence  $V_\pi$  set to zero. This means the output resistance is  $R_L \parallel r_o$ .

---

## 3.2 MOSFET Small Signal Model

[See Sedra & Smith Chapter 4.6.]

### 3.2.1 Linearization and Graphical Analysis

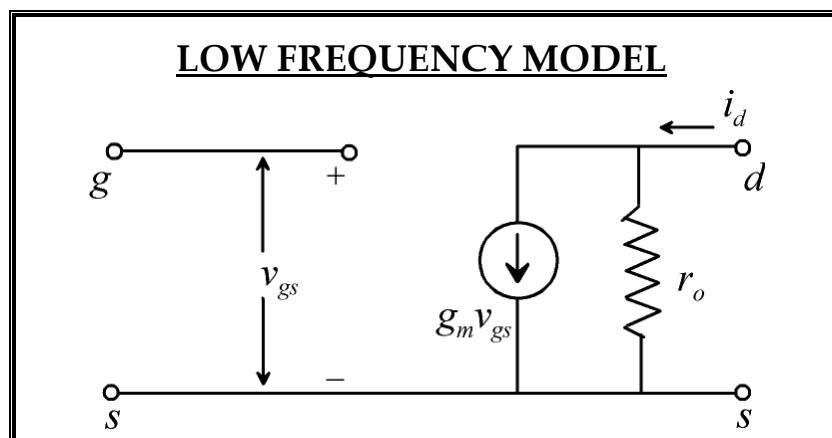
- Concerned with small signal variations about the operating points.

$$i_D = I_D + i_d$$

$$v_{DS} = V_{DS} + v_{ds}$$

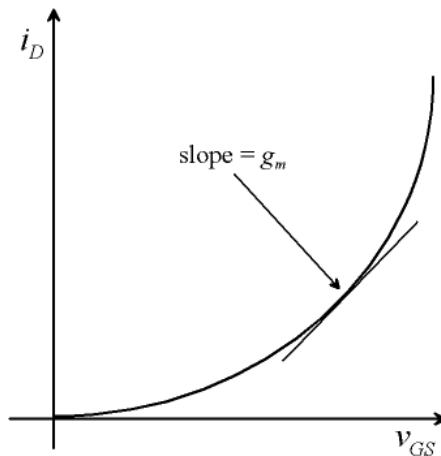
$$v_{GS} = V_{GS} + v_{gs}$$

- Interested in a relationship between  $i_d$ ,  $v_{gs}$  and  $v_{ds}$



This voltage-controlled current source  $g_m v_{gs}$  relates  $i_d$  to  $v_{gs}$  for the FET operating in the saturation region

- $g_m$  is given by the slope of the transfer characteristic at the operating point



### 3.2.2 Small Signal Model ( $g_m$ , $r_o$ )

$$g_m = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t) = \sqrt{2\mu_n C_{ox}} \sqrt{\frac{W}{L}} \sqrt{I_D}$$

Note:- 1.  $g_m$  depends on aspect ratio  $\left( \frac{W}{L} \right)$  - geometric  
 2.  $g_m$  depends on bias pt., ie.  $\propto$  to  $\sqrt{I_D}$

Typically  $\mu_n \approx 20 \mu A/V^2$

$$\text{For } I_D = I_m A, \quad \frac{W}{L} = 1, \quad \Rightarrow g_m = 0.2 mA/V$$

$$\frac{W}{L} = 100, \quad \Rightarrow g_m = 2 mA/V$$

Compare with BJT,  $I_c = 1mA \Rightarrow g_m \approx 40mA/V$

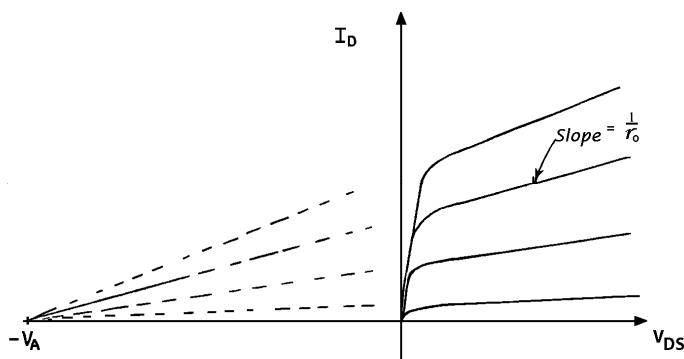
In spite of its low  $g_m$ , MOSFET have other advantages: high  $Z_{in}$ , small size low power dissipation & ease of fabrication.

Note:-  $g_m$  of BJT is geometry independent.

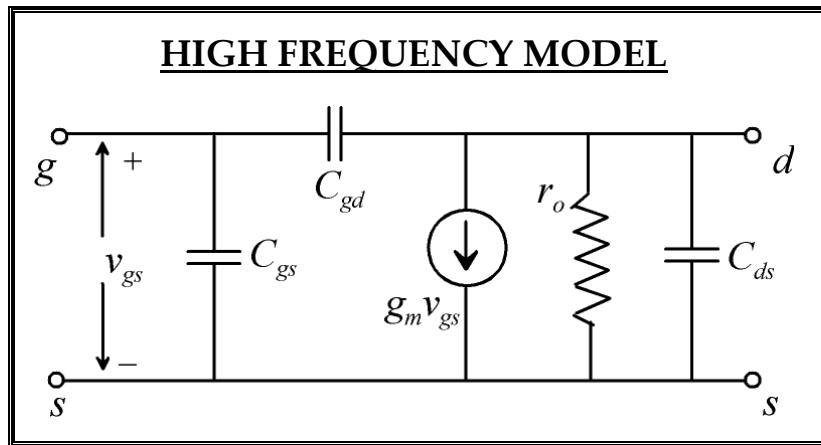
$r_o \equiv$  output resistance — slope of the output characteristic evaluated at the operating point — due to channel length modulation:

$$r_o = \frac{V_A}{I_D}$$

evaluated at the operating point typically  $r_o$  ranges from  $10k \rightarrow 100k\Omega$ .



**Note:**  $V_A$  has a similar effect on the output characteristic as for the Early Voltage for a BJT. It must be stressed that they are from very different effects.



$C_{gs} \equiv$  gate-source capacitance

$C_{gd} \equiv$  gate-drain capacitance

$C_{ds} =$  drain – substrate capacitance

Range: fraction of pF to 1 or 2 pF, depending on device size.

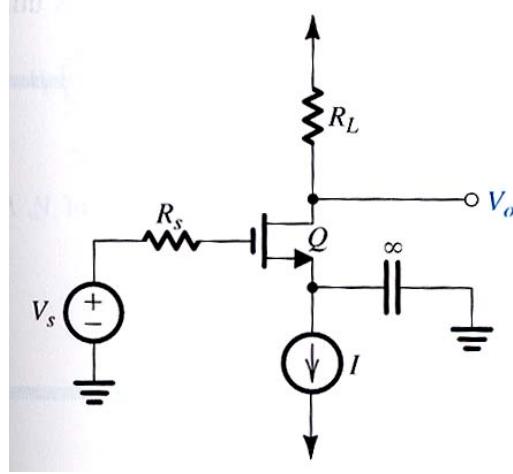
Note:  $C_{gd}$  contributes significantly to the Miller effect, resulting in reduction of gain at high frequencies — (covered later in the course).

### 3.2.3 Common-Source Amplifier

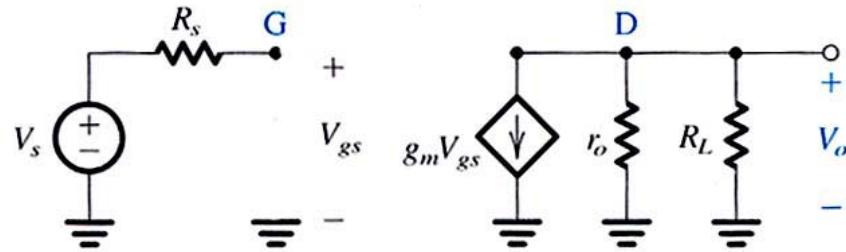
As for the case of the hybrid- $\pi$  model for the BJT the easiest way to gain an understanding of the use of the model just presented is to present an example. The example to be presented is the MOSFET analogue of the common emitter amplifier – the common source amplifier. Once again the model will be used to obtain an equivalent circuit and the mid-band voltage gain as well as the input and output impedances found.

#### EXAMPLE: The Common Source Amplifier

This is the FET equivalent of the BJT common emitter amplifier looked at earlier. We can find the mid-band gain and the input and output impedances by use of the low frequency equivalent circuit.



Using the low frequency model for the FET we can derive the equivalent circuit as:



To find the voltage gain of the circuit we proceed as for the common emitter circuit.

Firstly we can see that  $v_s = v_{gs}$ . So we just need to find the output voltage. The current source supplies current to both  $R_L$  and  $r_o$  and so the output voltage is given by:

$$v_o = -g_m v_{gs} (R_L // r_o)$$

This means the voltage gain will be:

$$A_v = -g_m (R_L // r_o)$$

What about the input and output impedances?

The input impedance for this circuit is infinite. No current is drawn through the gate and so the value of  $R_s$  is unimportant. This is obviously an approximation, but the input impedances of FETs are extremely high.

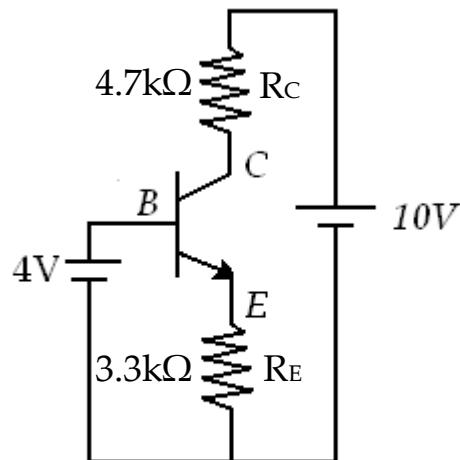
As for the output impedance if we look into the circuit from node D with  $v_s$  switched off the signal sees an impedance of  $R_L // r_o$ .

### 3.3 DC Biasing of Transistor Amplifiers

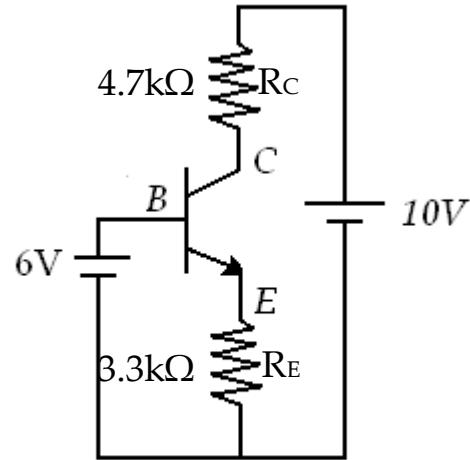
[See Sedra & Smith Section 5.4 and 4.3.]

#### 3.3.1 Basic DC Analysis of BJT Circuits

Consider the circuits shown below. Firstly we will examine the DC bias of (a).



(a)



(b)

To simplify our analysis, we will start by assuming that the transistor is in the active mode (i.e.  $V_{be} = 0.7V$ ).

We can first determine the emitter voltage to be 3.3V. The emitter current through  $R_E$  is thus 1mA. From the current relations that we have determined previously, we know that the collector current is:

$$I_C = \alpha I_E = \frac{\beta}{\beta + 1} I_E = 0.99 I_E$$

Thus,  $I_C = 0.99\text{mA}$ .

Finding the collector voltage to be 5.3V confirms that the base-collector junction is reversed bias, and the transistor is in the forward active mode.

Now we will consider (b), which is identical except for a higher base voltage. Again, if we assume active mode operation, we have:

$$V_B = 6 - 0.7 = 5.3V$$

$$I_E = \frac{5.3}{3.3} = 1.6\text{mA}$$

$$V_C = 10 - 4.7 \times I_C = 2.48 \text{ V}$$

Since our value for  $V_C$  is less than the base voltage, the transistor cannot be in the forward active mode. This transistor is in the *saturation mode*. In saturation, the normal current relations do not hold.

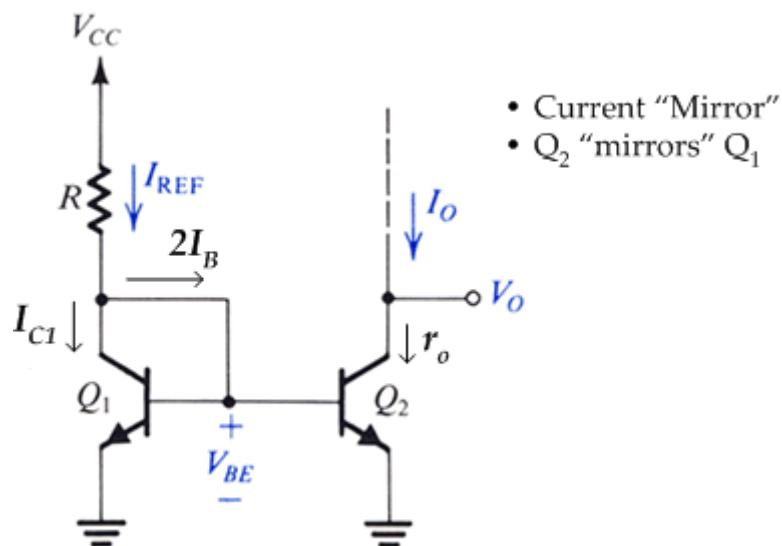
In practical transistor circuits, the base will not be connected directly to a voltage source, but instead will be biased via a resistance circuit such as a voltage divider. Normal circuit analysis can be used to find the base voltage in these cases.

### 3.3.2 Biasing of BJT Amplifier Circuits. Current Mirrors

The biasing of transistor amplifiers by the use of a number of resistors with large-value capacitors is unsuitable for integrated-circuit manufacture. This is because current technology doesn't allow the fabrication of large-value capacitors on ICs and the fabrication of resistors is uneconomical. However, ICs do provide a large number of transistors with matched characteristics.

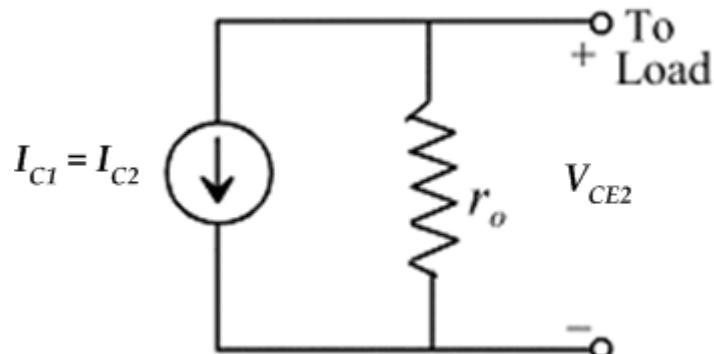
As we shall now see, transistors can be used to construct constant-current sources which can in turn be used to bias a number of amplifier circuits. Since the transistors are matched and on the same chip, the stages will track each other if there is a change in the temperature or even the power-supply voltage.

#### A Simple Current Source



Current sources or *mirrors* are designed to maintain  $I_C$  at a constant value even when  $V_{CE}$  changes; typical loads could be differential-amplifier stages, ECL gates (dealt with later on), etc.

The Norton-equivalent circuit of a current source



$r_o \equiv$  output resistance of the source, which is the output resistance seen at the collector of  $Q_2$ .

Now, it can be shown that the collector current is exponentially-dependent on the base-emitter voltage  $V_{BE}$ :

$$I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

where  $V_T = \frac{kT}{q} \equiv \frac{\text{Thermal voltage}}{\text{electronic charge}}$

and  $I_s \equiv$  the saturation current of the transistor, which depends on the doping concentration and mobility of minority carriers in the

base.

Since both transistors in a current source are fabricated on the same wafer, close to each other, the devices are well matched in  $\beta$ ,  $V_{BE}$  and  $I_S$ , if they are of identical geometry.

$$\therefore \beta_1 = \beta_2 = \beta$$

$$I_{C1} = I_{S1} \exp\left(\frac{V_{BE1}}{V_T}\right)$$

$$(I_{S1} = I_{S2})$$

$$I_{C2} = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right)$$

### Taking KVL in the Base Loop

$$V_{BE} = V_{BE1} = V_{BE2} \quad \& \quad \beta_1 = \beta_2 \quad \text{then} \quad I_B = I_{B1} = I_{B2}, I_C = I_{C1} = I_{C2}$$

i.e.  $I_B$  and  $I_C$  will be *identical* for  $Q_1$  and  $Q_2$

$$\therefore I_R = \frac{V_{CC} - V_{BE}}{R} = I_{C1} + 2I_B = \beta I_B + 2I_B$$

$$\therefore I_{C1} = I_{C2} = \frac{\beta}{\beta+2} \cdot I_R = \frac{\beta}{\beta+2} \cdot \left( \frac{V_{CC} - V_{BE}}{R} \right) = \left( \frac{1}{1 + \frac{2}{\beta}} \right) \cdot I_R$$

For  $\beta \gg 1$ ,  $I_{C1} \approx I_R$ . i.e.  $V_{CC}$  &  $R$  set the value  $I_{C2}$  and connection to  $Q_1$  mirrors  $I_{C2}$  on to  $I_{C1}$ .

If the effect of the Early Voltage ( $V_A$ ) is included, then we must write:

$$I_{C1} = I_{S1} \exp\left(\frac{V_{BE1}}{V_T}\right) \left( 1 + \frac{V_{CE1}}{V_A} \right)$$

$$I_{C2} = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right) \left( 1 + \frac{V_{CE2}}{V_A} \right)$$

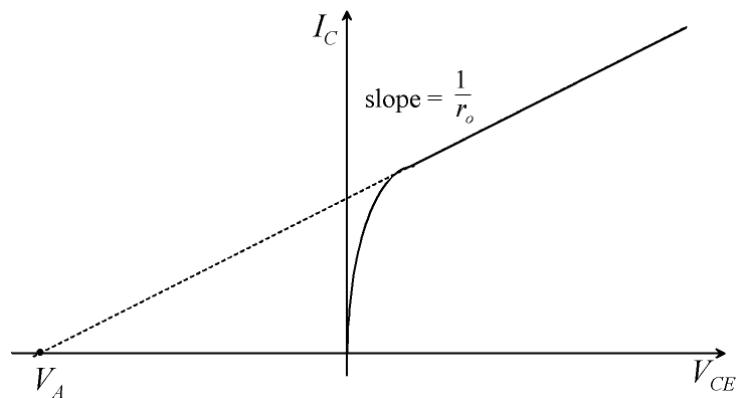
See Figure below.

Since  $V_{BE1} = V_{BE2} = V_{BE}$ ,  $I_{S1} = I_{S2}$ ,  $\beta_1 = \beta_2 = \beta$

$$I_{C2} = I_{C1} \left( \frac{1 + \frac{V_{CE2}}{V_A}}{1 + \frac{V_{CE1}}{V_A}} \right) \quad \text{note } V_{CE1} \approx 0.7 \text{ V - small compared to } V_A \approx 100 \text{ V}$$

$$\approx I_{C1} \left( 1 + \frac{V_{CE2}}{V_A} \right) = I_{C1} + \left( \frac{I_{C1}}{V_A} \right) \cdot V_{CE2} = I_{C1} + \frac{V_{CE2}}{r_o}$$

The output resistance of this simple current source is approximately given by  $r_o = \left( \frac{V_A}{I_C} \right)$ .



### 3.3.2 Basic DC Analysis of MOSFET Circuits

To analyze the behaviour of MOSFETs at DC, we first define the following current relations, based on the graphical analysis presented earlier.

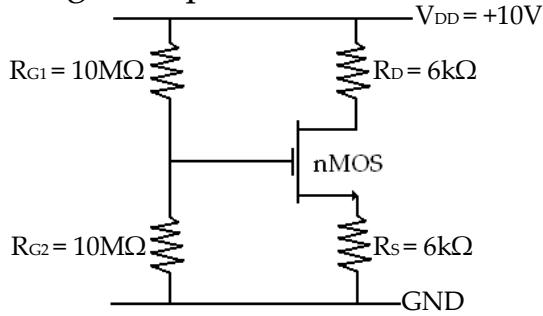
$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_t|)^2 \text{ for pMOS}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \text{ for nMOS}$$

To analysis the DC bias of a MOSFET circuit, we must determine the gate voltages, and hence the drain currents, similar to the approach taken with BJTs.

Sometimes it is useful to define the *overdrive voltage*  $V_{OV} = V_G - V_t$

Consider the following example:



Where the threshold voltage  $V_t = 1V$  and  $\mu_n C_{ox} \frac{W}{L} = 1mA/V^2$ .

Since the *gate current is zero*, we can determine the gate voltage by the simple voltage divider equation:

$$V_G = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}} = 10 \times \frac{10}{10 + 10} = 5V$$

We know that since the gate voltage is thus 5V and the transistor is turned on. We will first assume that the transistor is in the *saturation region*, similar to our approach with the BJT. If this turns out to be incorrect (i.e.  $V_D < V_G - V_t$ ) we will have to consider the *triode case*.

We can see from the circuit that the source voltage is related to the source-drain current by  $V_S = I_D R_S$ , so the gate-source voltage is:

$$V_{GS} = V_G - I_D R_S = 5 - 6I_D$$

Using the equation for the drain current above, we get:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (5 - 6I_D - V_t)^2$$

Solving the quadratic equation for  $I_D$  gives possible solutions of 0.89mA and 0.5mA. We can eliminate the first result as this would result in a source voltage of 5.34V, which would imply that the transistor is turned off.

So  $I_D = 0.5mA$ , thus  $V_S = 0.5 \times 6 = 3V$

$V_{GS} = 2V$  and  $V_D = 10 - 6 \times 0.5 = 7V$ .

Since  $V_D > V_G - V_t$ , the transistor is in saturation as we assumed.

### 3.3.4 Biasing of MOSFET Amplifiers. Current Mirrors

1. Using depletion mode MOSFET (with threshold voltage of  $V_{th}$ )

$$I_o = k(V_{ES} - V_{th})^2$$

Since the gate & source are connected

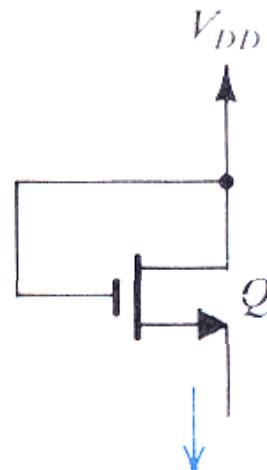
$$\therefore I_o = I_D = k(-V_{th})^2 = kV_{th}^2$$

If we include the channel length modulation effect in MOS, which is represented by the symbol  $\Lambda$  then

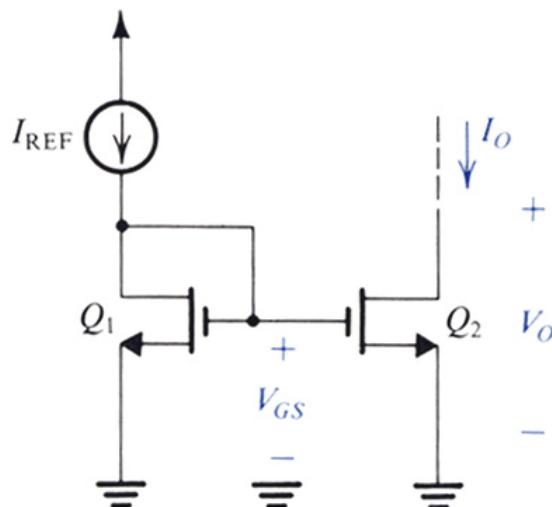
$$I_o = KV_{th}^2(H\Lambda V_{DS}) \text{ where } V_{DS} > |V_{th}|$$

Output resistance

1      1



### 2. Simple MOS current mirror



(gate current is ZERO) and all devices in saturation for  $Q_1$

$$I_o = I_{D1} = K_1(V_{GS1} - V_{th})^2(1 - \Lambda V_{DS1})$$

for  $Q_2$

$$I_{REF} = I_{D2} = K_2(V_{GS2} - V_t)^2(1 + \Lambda V_{DS2})$$

Since  $V_{GS1} = V_{GS2}$  threshold voltage  $V_{th}$  is matched

$$\therefore I_o = I_{REF} \cdot \frac{K_1}{K_2} \cdot \frac{(1 + \Lambda V_{DS1})}{(1 + \Lambda V_{DS2})}$$

$$\left. \begin{aligned} K_1 &= \frac{W_1}{L_1} \\ K_2 &= \frac{W_2}{L_2} \end{aligned} \right\} \text{aspect ratios of the two transistors.}$$

Usually  $\lambda$  is sufficiently small such that the  $I_o: I_{REF}$  is determined by the ratio of  $K_1: K_2$  this flexibility is at the disposal of the IC designer i.e. One can determine the desired current ratio by choosing the transistor sizes.

Again, the output resistance is given by:

$$R_o = r_d = \frac{1}{\lambda I_{D1}} = \frac{1}{\lambda I_o}$$

# **SECTION 4: FREQUENCY RESPONSE OF TRANSISTOR AMPLIFIERS**

## **4.1 Review of Bode Plots**

- 4.1.1 Amplitude & Phase Response. Decibel Scale**
- 4.1.2 Rules for Making Bode Plots. Amplifier Bandwidth**

## **4.2 Tools for Frequency Analysis**

- 4.2.1 Relationship Between Poles & Time Constants**
- 4.2.2 Dominant-Pole Approximation**
- 4.2.3 Miller's Theorem**

## **4.3 Low Frequency Analysis of Circuits**

- 4.3.1 Find the Small-Signal Circuit**
- 4.3.2 Finding  $f_L$  the Low Corner Frequency**

## **4.4 High Frequency Analysis of Circuits**

- 4.4.1 High-frequency Response of the Amplifiers**
- 4.4.2 Open-Circuit Time Constant Method**
- 4.4.3 High-frequency limit of BJT Hybrid- $\pi$  Model**
- 4.4.4 High Frequency Response of the Common-Emitter Amplifier**

## **4.5 Improving the Frequency Response**

- 4.5.1 Avoiding the Miller Effect**
- 4.5.2 The Cascode Configuration**
- 4.5.3 Common-Collector Common-Base Configuration**
- Common-Collector Common-Emitter Cascade**

### **Aims**

After this section the student should know:

- How to use and construct Bode plots for frequency analysis.
- The tools presented for frequency analysis including dominant pole approximation, Miller's Theorem as well as the relationship between poles and time constants. Should also know how to use these tools for analysis.
- The origin of the Miller effect as well as its impact on circuit performance and methods for overcoming it.

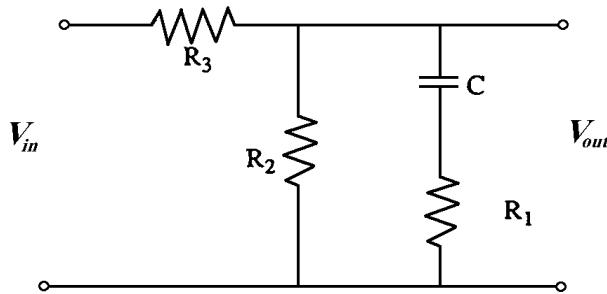
## 4.1 Review of Bode Plots

Most network functions that vary with frequency (such as input impedances, voltage gains, transfer functions, etc.) can be expressed in the general form:

$$G(j\omega) = \frac{A(1 + j\omega/\omega_0)(\ )(\ )}{(1 + j\omega/\omega_p)(\ )( )} \quad \dots(1)$$

where the bracketed numerator terms are the zeroes and the denominator terms are the poles of the functions. There are some other types of expressions encountered, but these will be commented on at a later stage.

As an illustration, consider the voltage transfer function of the network shown below:



$$\begin{aligned} G(j\omega) &= \frac{V_{out}}{V_{in}} \\ &= \frac{(R_1 + 1/j\omega C)\parallel R_2}{(R_1 + 1/j\omega C)\parallel R_2 + R_3} \end{aligned}$$

which reduces to

$$G(j\omega) = \frac{R_2 + (1 + j\omega CR_2)}{R_1 + R_3 + 1 + j\omega CR_T} \equiv \frac{A(1 + j\omega/\omega_0)}{(1 + j\omega/\omega_p)} \quad \dots(2)$$

with

$$R_T = \frac{(R_1 R_2 + R_2 R_3 + R_1 R_3)}{R_2 + R_3} = R_1 + \frac{R_2}{R_3}$$

In this case there is only one pole and one zero.

### 4.1.1 Amplitude & Phase Response

When plotting network functions against frequency, both the amplitude and phase responses are generally of interest. Therefore, from eqn. (1):

$$|G(j\omega)| = \frac{A\sqrt{1 + (\omega/\omega_0)^2}}{\sqrt{1 + (\omega/\omega_p)^2}} \dots \quad \dots(3)$$

and

$$\angle G(j\omega) = \tan^{-1} \frac{\omega}{\omega_0} + \dots - \tan^{-1} \frac{\omega}{\omega_p} \dots \quad \dots(4)$$

Consider first the problem of determining the magnitude response. By taking logarithms (base 10)

$$\log|G(j\omega)| = \log A + \log \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} + \dots - \log \sqrt{1 + \left(\frac{\omega}{\omega_p}\right)^2} - \dots$$

from which is seen that all the entries are additive and of the same form (apart from  $\log A$ ) with the zero contributions being positive and the pole contributions being negative.

The complete amplitude response can be constructed now, if the variation of each of the standard terms can be determined. Consider therefore

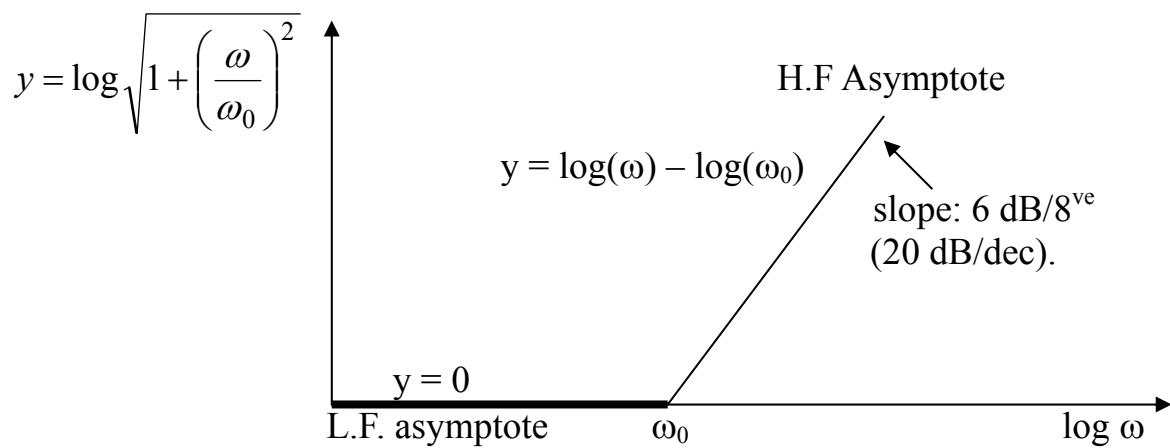
$$y = \log \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

$$\text{for } \omega \ll \omega_0, \quad y = \log 1 = 0. \quad \dots(5a)$$

$$\text{whereas for } \omega \gg \omega_0 \quad y = \log \frac{\omega}{\omega_0} = \log \omega - \log \omega_0 \quad \dots(5b)$$

Therefore, if the frequency axis is also scaled in logarithmic coordinates, the last expression is the equation of a straight line of unity slope and intercept with the frequency axis at ( $\log \omega_0$ ) – i.e.,  $\omega = \omega_0$ .

Equations (5a) and (5b) define two asymptotes for the frequency dependence of the general term under consideration. These are illustrated below.



The frequency  $\omega = \omega_0$  for obvious reasons, is referred to as the **CORNER FREQUENCY**. The sketch above is a good first-order approximation to the frequency dependence of the general zero term. To make it a better representation, we can now examine specific values of the term more closely. For example, at the corner frequency:

$$y = \log \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} = \frac{\log 2}{2} = \log \sqrt{2}$$

**It is useful at this stage if the ordinate scale is multiplied by 20 so that we plot vertically  $20 \log()$  and thus scale in decibels (dB). At the corner therefore:**

$$y = 20 \times \frac{\log 2}{2} \approx 3 \text{ dB}$$

– i.e., there is a 3 dB correction required.

## IMPORTANT: THE CORNER FREQUENCY = 3 dB FREQUENCY

Two other specific values worth noting are:

$$\text{at } \omega = 2\omega_0, \quad y = 20 \log \sqrt{5} \approx 7 \text{ dB}$$

$$\text{at } \omega = \frac{\omega_0}{2}, \quad y = 20 \log \sqrt{\frac{5}{4}} \approx 1 \text{ dB}.$$

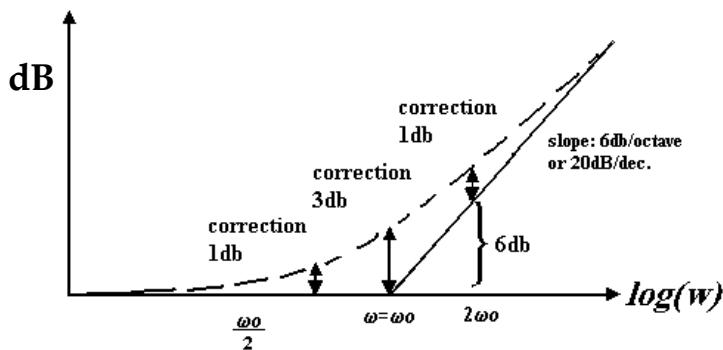
However, before making these corrections, it is instructive to consider the slope of the high-frequency asymptote in dB versus  $\log \omega$  coördinates.

From (5b), the equation of the high-frequency asymptote:

$$\text{at } \omega = \omega_0, \quad y = 0 \text{ dB}$$

$$\text{whereas at } \omega = 2\omega_0, \quad y = 20 \log 2 = 6 \text{ dB}.$$

Thus, the high frequency asymptote increases by 6 dB for every doubling in frequency – in other words, its slope is 6 dB/octave, which can also be shown to be 20 dB/decade. A more complete picture of the frequency dependence of the general zero term therefore can be sketched as below.



A very good freehand sketch is now possible, certainly accurate within  $\frac{1}{2}$  dB or so.

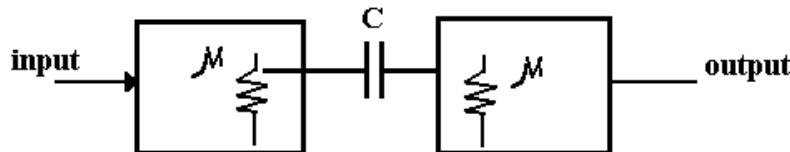
Terms which appear as poles in the function  $G(j\omega)$  will behave exactly as for the zero terms, except their plots will be multiplied by -1 and will thus be a mirror image of the zero plot across the  $\log \omega$  axis.

## 4.1.2 Some rules for making Bode Plots

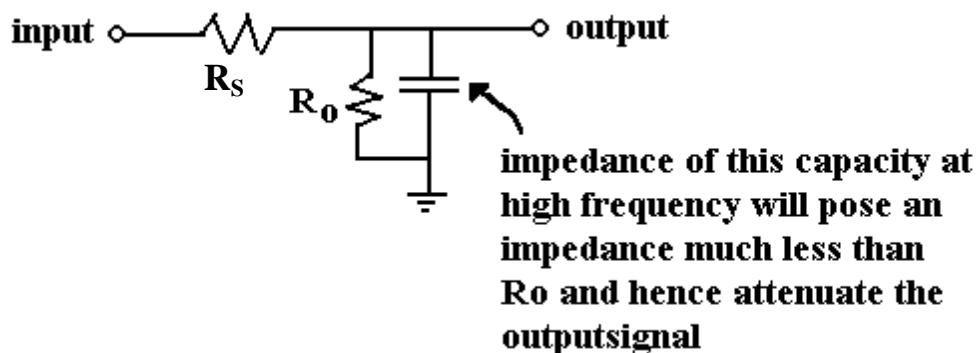
1. Identify the function of the capacitors (or even inductors) concerned. (Most important.)
  - Does the capacitor attenuate the signal flow from input to output or not?
  - Remember the magnitude of the impedance of the capacitor

$$|Z_C| = \frac{1}{\omega C} \begin{cases} 0 & \text{at high frequency} \\ \infty & \text{at low frequency} \end{cases}$$

- So, depending on how the capacitor is connected in the circuit, it will or will not attenuate the signal flow. E.g., coupling capacitors will allow high-frequency signals through and attenuate low-frequency signals (blocking d.c.).



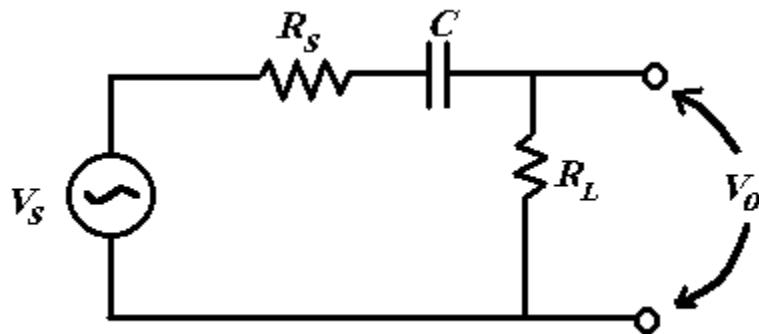
E.g., in general, shunting capacitors will tend to attenuate high frequency signals and not low frequency signals.



**CAUTION:** Watch out for the 'by-pass' capacitor!

2. Determine the resistance  $R_{\text{eq}}$  'seen' by each capacitor,  
[i.e.,  $R$  to ground with **independent** sources disabled].
3. Find the break-point or corner frequencies  $\omega_0 = \frac{1}{CR_{\text{eq}}}$ .
4. Sketch the graph of the magnitude versus frequency response.
5. Insert some gain values on the horizontal regions.  
(Calculate mid-band gain.)
6. If needed, sketch the phase response too!

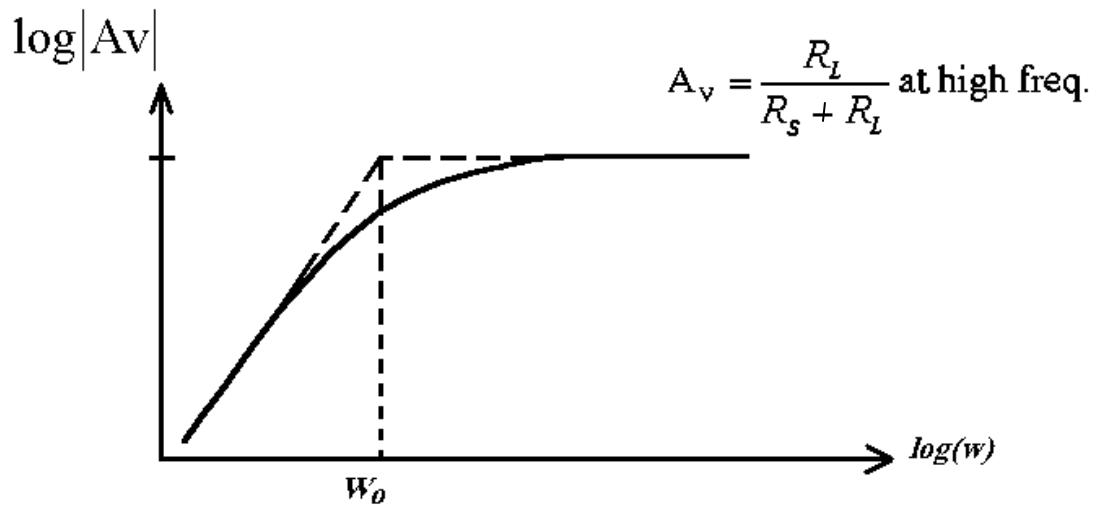
### Example 1



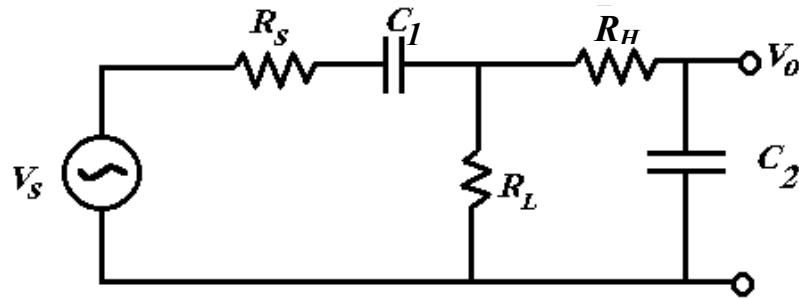
1. Capacitor  $C$  attenuates low-frequency signal, i.e., dc blocked.
2. Resistance seen by  $C$  with  $v_s$  sorted is  $R_s + R_L = R_{\text{eq}}$
3. Thus  $\omega_0 = \frac{1}{(R_s + R_L)C}$
4. At very high frequencies, impedance of  $C$  is very low (like a S/C), thus,

$$V_o = \left( \frac{R_L}{R_s + R_L} \right) V_s \rightarrow \text{gain} = \frac{R_L}{R_s + R_L}$$

Hence, the sketch would look something like this



## Example 2



1. Note that  $C_1$  will attenuate low-frequency signals and  $C_2$  will attenuate high-frequency signals.
2. Equivalent resistance seen by  $C_1$  is  $R_{eq1} = (R_s + R_L)$  [since at the frequency range of interest (lower end),  $C_2$  would look like an open circuit]. Equivalent resistance seen by  $C_2$  is  

$$R_{eq2} = R_H + R_S // R_L$$

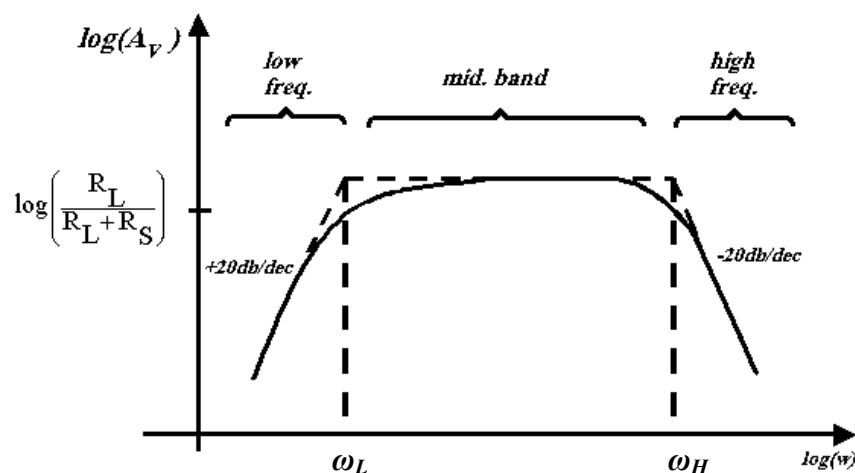
[since at the frequency range of interest (higher)  $C_1$  would look like a short circuit].
3. Corner frequencies are at

$$\omega_L = \frac{1}{C_1(R_s + R_L)}$$

$$\omega_H = \frac{1}{C_2(R_H + R_s // R_L)}$$

4. Make the following observations

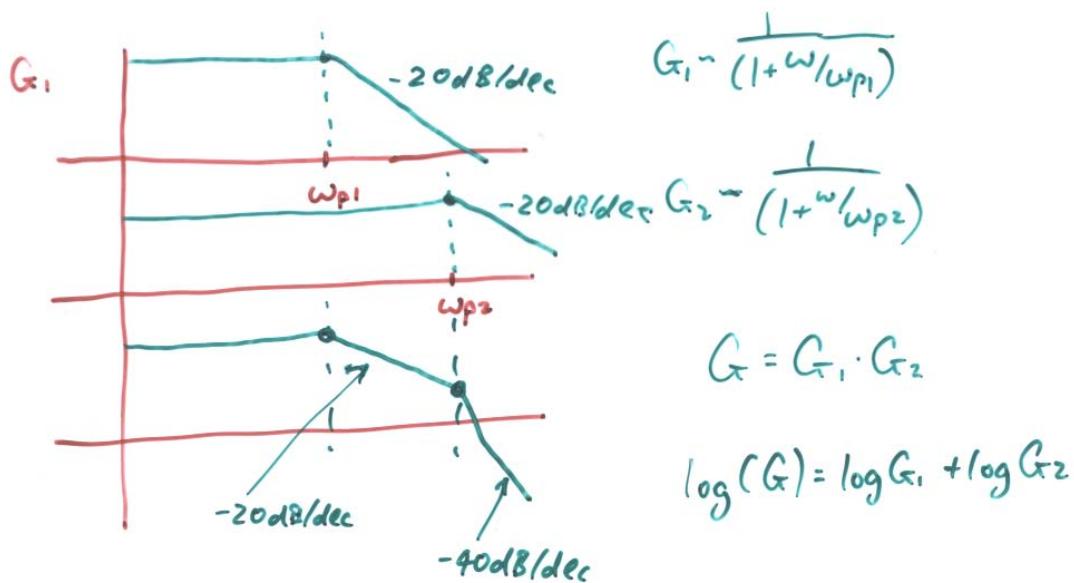
- at very low frequencies,  $C_1$  will attenuate all signals going to the output:  $V_o = 0$
- at very high frequencies,  $C_2$  will (shunt) attenuate all signals at the output:  $V_o \rightarrow 0$ .
- Somewhere in the mid-band frequency range where  $C_1$  still presents a very low impedance and  $C_2$  still presents a very high impedance, then  $A_V = \frac{V_o}{V_s} = \frac{R_L}{R_L + R_s}$  (assume no load at the output).



## 4.2 Tools for Frequency Analysis

The analysis techniques as well as the circuit models necessary for the analysis of the behaviour of transistor circuits as a function of frequency have been presented. We will now attempt to refine these tools and apply them to a series of important circuits. The analysis of these circuits will be used to highlight some important factors in determining the frequency response of a transistor circuit. Finally some methods for overcoming the limitations of transistor circuits will be presented.

With the frequency models for the BJTs and MOSFETs coupled with our circuit analysis techniques including Bode analysis, it would seem that we are able to work on any circuit we desire. This is true in essence; however, it should be pointed out that when we begin looking at the transfer function of an amplifier, it is rare that we will get a function that 'behaves nicely' and can be used easily to extract the frequency response. For this reason, we shall now see some approximation methods for determining the most important parameters of the frequency response.



### 4.2.1 Relationship Between Poles & Time Constants

1. For LOW-FREQUENCY amplifier circuits.

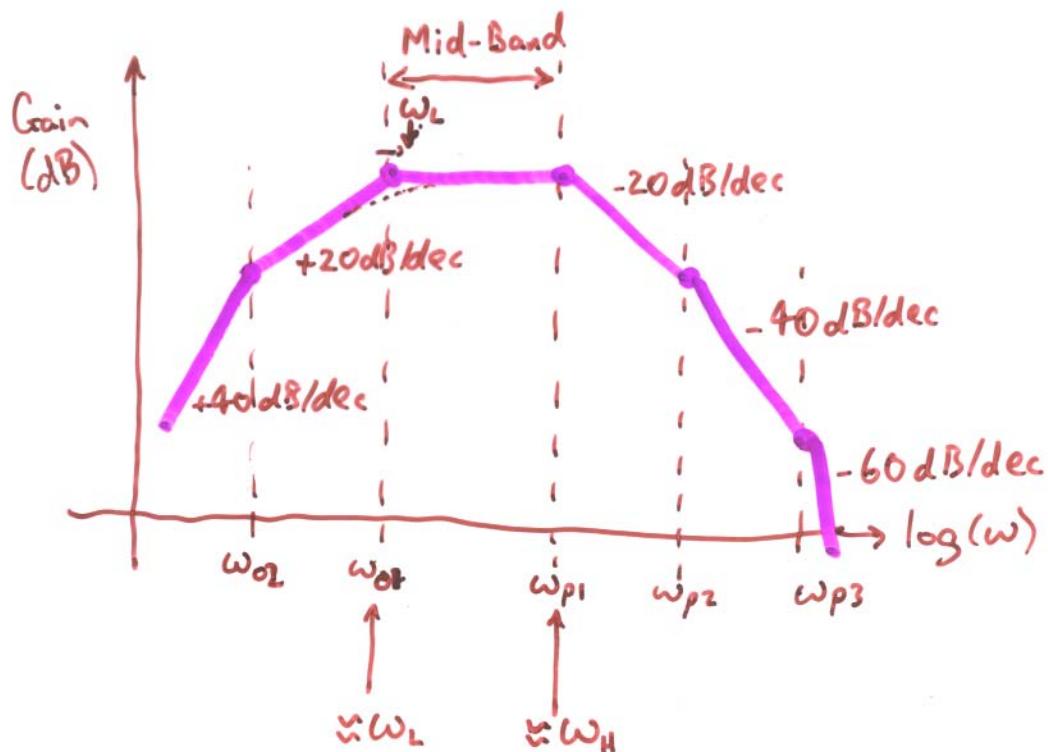
$$(P_1 + P_2 + P_3 \dots P_n) = \sum_{j=1}^n \frac{1}{\tau_{js}} \quad (\text{PT1})$$

where  $P_j \equiv j^{th}$  pole of the gain function  $\equiv \omega_{0j}$

$\tau_{js} = R_{js} C_j \equiv$  short-circuit time constant associated with  $C_j$

$R_{js} \equiv$  effective resistance in series with  $C_j$  under when  $C_{i \neq j}$  are short-circuited and the input source disabled

Hence, the sum of the poles equals the sum of the reciprocals of the short-circuit time constants. Each of the terms ( $\tau$ 's) is found for the specific capacitance in isolation, i.e., the other capacitances are short-circuited.



2. For HIGH-FREQUENCY amplifier circuits.

$$\left( \frac{1}{p_1} + \frac{1}{p_2} \dots \frac{1}{p_n} \right) = \sum_{j=1}^n \tau_{jo} \quad (\text{PT2})$$

where

$P_j \equiv j^{\text{th}}$  pole of the gain function  $\equiv \omega_{pj}$

$\tau_{jo} \equiv R_{jo} C_j \equiv$  open-circuit time constant associated with  $C_j$ .

$R_{jo} \equiv$  effective resistance in series with  $C_j$  under the condition  
that  $C_{i \neq j}$  are **open-circuited** and the input source disabled

Hence, **the sum of the reciprocals of the poles equals the sum of the open-circuit time constants.**

Once again, for each term, we are interested in the specific capacitance in isolation but this time, the other capacitors are open circuited.

In some cases our task can be simplified even further. In these cases, one pole will be the primary determinant of the corner frequency, with other terms having a minimal effect.

## 4.2.2 Dominant Pole Approximation

The dominant-pole approximation can be made if the highest-frequency pole is separated from the next pole or zero by at least two octaves (i.e., a factor of 4).

- For **LOW-FREQUENCY** analysis, if  $p_1$  is the dominant pole  $p_1 \gg p_2$  (poles widely separated)

Then,  $p_1 \approx \sum \frac{1}{\tau_{js}}$  and  $\omega_L \approx \sum \frac{1}{\tau_{js}}$

(DP1)

However, if the response is **not** dominated by a single pole, a good design procedure is to assume that the sum of the poles is  $\approx 1.15 \omega_L$ .

i.e.,  $1.15\omega_L \approx \sum \frac{1}{\tau_{js}}$

- For **HIGH-FREQUENCY** analysis, if  $p_1$  is the dominant pole, such that  $\frac{1}{p_1} \gg \frac{1}{p_2}$  then:

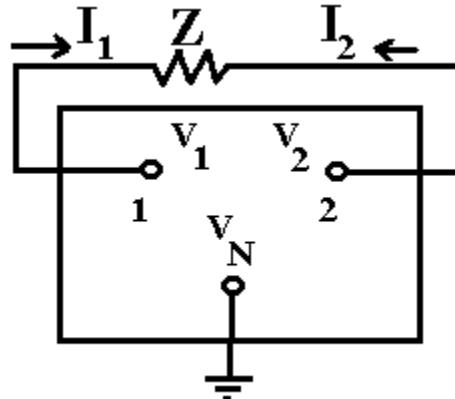
$$\frac{1}{\omega_H} \approx \sum \tau_{jo}$$
(DP2)

However, if the response is **not** dominated by a single pole, a good design procedure is to assume that:

$$\frac{1.15}{\omega_H} \approx \sum \tau_{jo}$$

### 4.2.3 Miller's Theorem

Consider an arbitrary circuit configuration of  $N$  distinct nodes where the node voltages are with reference to  $V_N = 0$  – ground.



Consider nodes 1 and 2 in with an impedance  $Z$  connected between them. We postulate that the voltage ratio (i.e., gain) between nodes 1 and 2 is

$$K = \frac{V_2}{V_1}$$

$$\therefore I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1(1 - K)}{Z} = \frac{V_1}{Z/(1-K)} = \frac{V_1}{Z_1} \quad (\text{M1})$$

$$\text{where } Z_1 = \frac{Z}{1 - K}$$

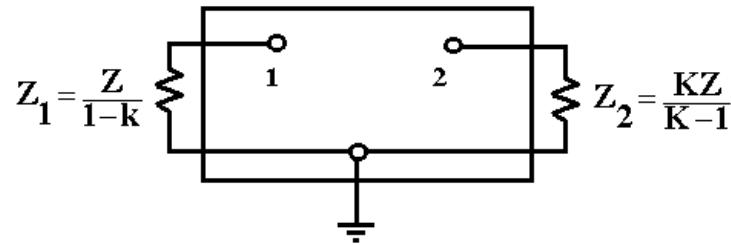
This means that the current drawn from node 1, (i.e.,  $I_1$ ) can be obtained by disconnecting  $Z$  from node 1 and placing an impedance  $Z_1$  between node 1 and  $V_N$ , i.e., ground.

Proceeding in a similar manner for  $I_2$  we find the following:

$$I_2 = \frac{V_2 - V_1}{Z} = \frac{V_2(1 - \frac{1}{K})}{Z} = \frac{V_2}{Z/(1 - \frac{1}{K})} \quad (\text{M2})$$

$$Z_2 = \frac{KZ}{K - 1}$$

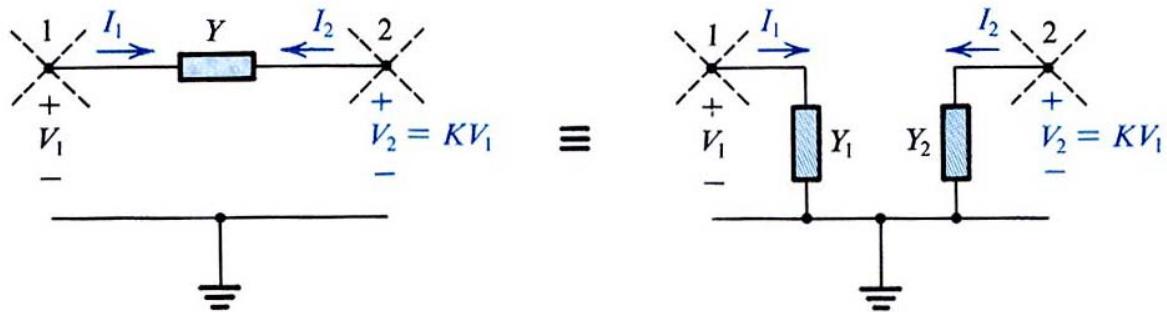
We can now replace the original circuit by the following:



**CAUTION:** Miller equivalent circuit is valid only as long as the conditions that existed in the network when  $K$  was determined are not changed, i.e., the Miller equivalent circuit cannot be used directly to determine output resistance and reverse transmission of the amplifier.

In practice, it is difficult to determine  $K$  independently and often the feed-through effects between input and output are neglected. For this reason the transfer function obtained from the exact analysis differs slightly from that of the Miller transformed circuit.

In terms of the circuits analysed in this subject, the Miller transformation can be summarised in the following:



A feedback element (typically a capacitor) is replaced by two elements in parallel with each other. In this case the  $Y$ 's in the circuits represent admittances but the circuit transformation is the same for impedances though the mathematical transformations are slightly different (remember  $Y=1/Z$ ).  $Y_1$  has the input voltage across it ( $V_1$ ) and  $Y_2$  has the amplified output voltage ( $V_2$ ) across it.

## 4.3 Low Frequency Analysis of Circuits

[See Sedra & Smith Section 7.3]

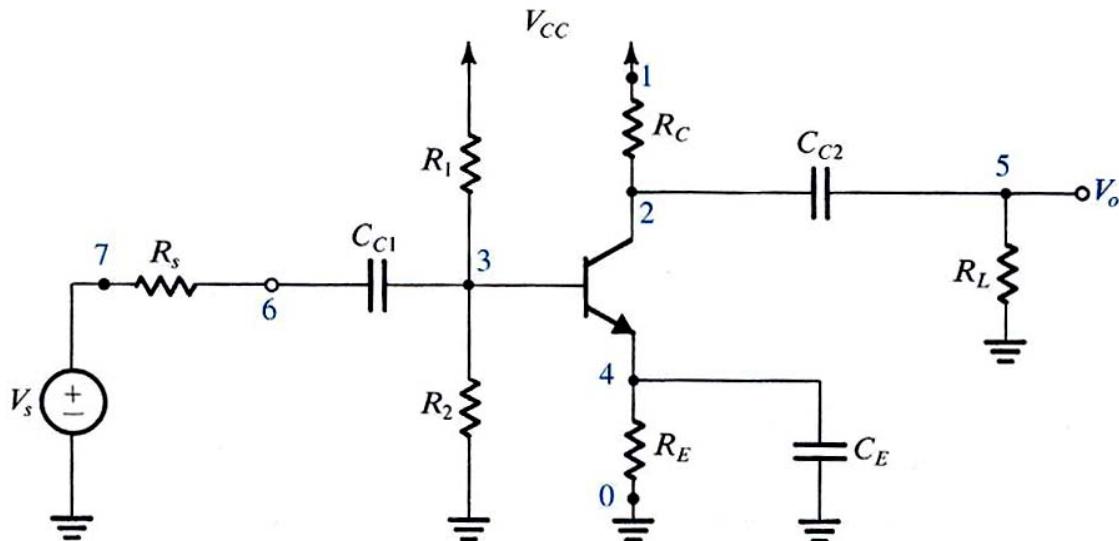
We have in fact already analysed a number of circuits for low frequencies. All of the calculations done thus far have assumed that all of the capacitances associated with the transistor can be neglected. By way of looking at the case of a common emitter amplifier, we will now see some key aspects of low-frequency behaviour, including the ability to select our low corner frequency value. It will be shown that **the poles in the amplifier transfer function are due to the capacitances introduced into the circuit by the designer.**

### 4.3.1 Find the Small Signal Circuit

Example: Low-Frequency Response of the CE Amplifier.

Consider the effect of

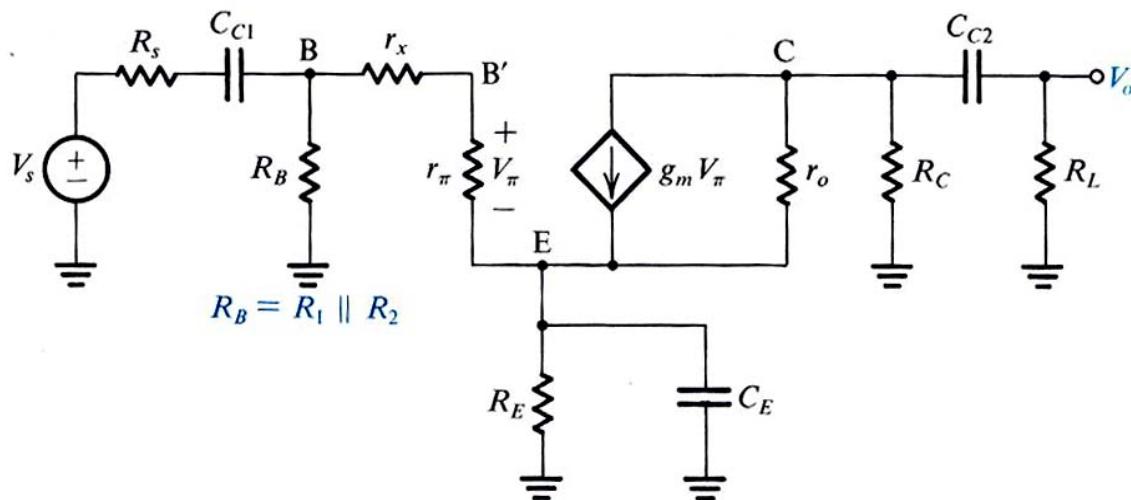
- $C_{C1}$  – input coupling capacitor
- $C_E$  – by-pass capacitor at the emitter.
- $C_{C2}$  – output coupling capacitor



Redraw the circuit as its small-signal equivalent.

[Note the following:

- 1) We have neglected  $r_\mu$  (i.e., assume  $r_\mu \rightarrow \infty$ ). Otherwise, the analysis is very complicated.
- 2) We have neglected  $C_\pi$  and  $C_\mu$ , since, at low frequencies, their impedance is very high.]



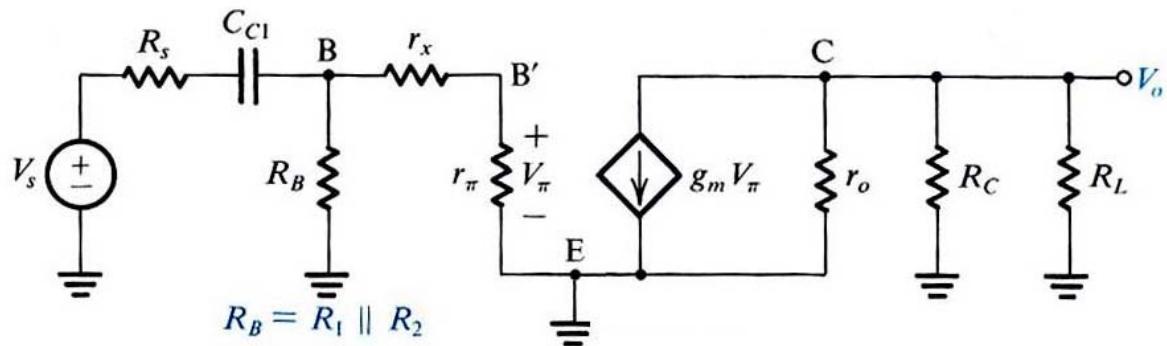
In this form, we can find a number of things, including the voltage gain, but in this case we will restrict ourselves to finding the lower corner frequency. Referring back to the relationship between the poles and time constants, and assuming a dominant pole, we see that for low frequency, **an estimate of  $f_L$  can be obtained by calculating the short-circuit time constant associated with each capacitor.**

### 4.3.2 Finding $f_L$ the Low Corner Frequency

Switch off the input voltage  $V_s$ .

Each capacitor in the circuit will produce a time constant term. Look at each capacitor in isolation with the other capacitors short-circuited.

1. Consider  $C_{C1}$ , with  $C_E$  and  $C_{C2}$  short-circuited. The equivalent resistance seen by  $C_{C1}$  is found by analysing the following circuit:



**Note:** This is just the small-signal model with two of the capacitors short-circuited.

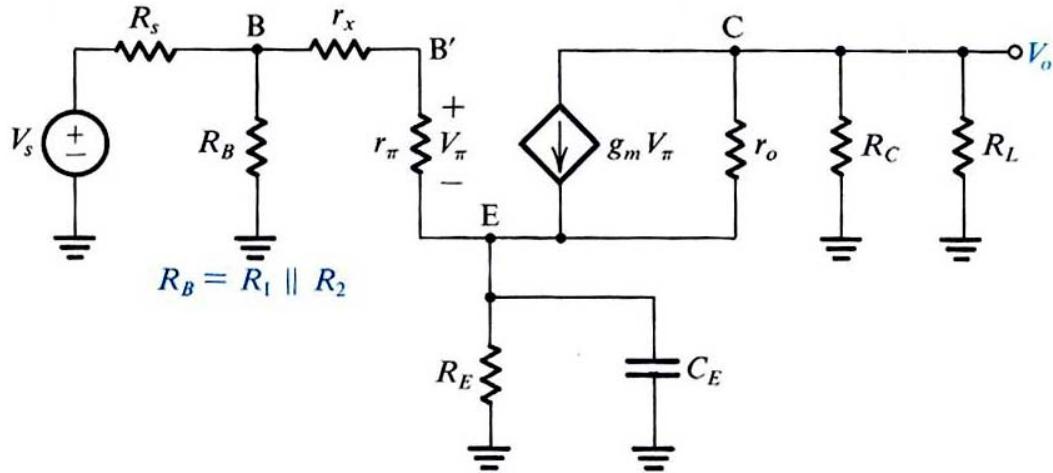
The capacitor  $C_{C1}$  doesn't 'see' the circuit to the right of the current source. So the resistance seen by  $C_{C1}$  will be a function of  $R_s$ ,  $R_B$ ,  $r_x$  and  $r_\pi$ .

Firstly we can see that to the right of  $C_{C1}$  that  $R_B$  is in parallel with  $r_x$  and  $r_\pi$ . These can be replaced by a resistor of value  $R_B // (r_x + r_\pi)$ . Finally, the source resistance and the parallel combination are both seen by  $C_{C1}$  as a series combination and so the total resistance seen by  $C_{C1}$  is given by:

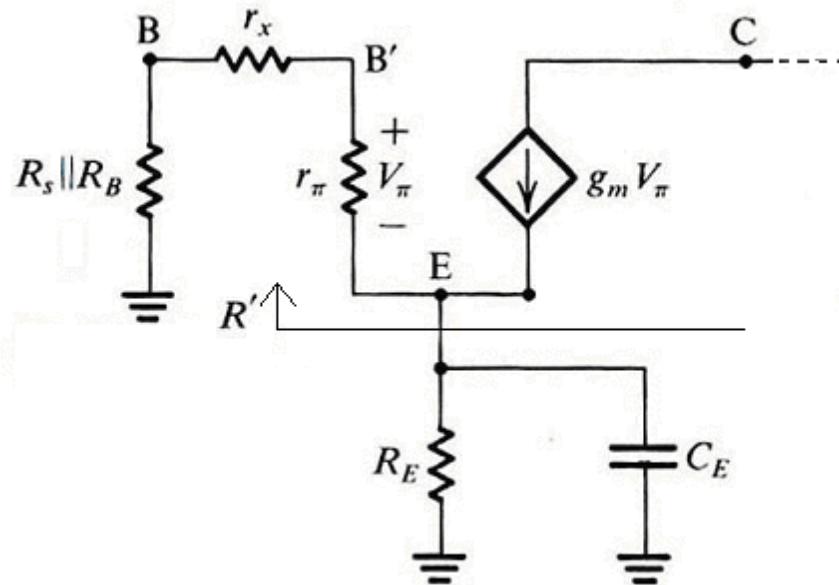
$$R_{C1} = R_s + [R_B // (r_x + r_\pi)]$$

$$\tau_{1S} = C_1 R_{C1}$$

2. Consider  $C_E$  with  $C_{C1}$  and  $C_{C2}$  **short-circuited**. The equivalent resistance seen by  $C_E$  is found by analysing the following circuit:



Assume, for the moment, that the value of  $r_0$  has become infinite to simplify matters (it has very little effect anyway). The circuit then becomes:



Find  $R'$ :

$$R' = \frac{V_E}{i_b + \beta i_b} = \frac{V_E}{i_b(1 + \beta)}$$

$$V_E = i_b [r_\pi + r_x + R_S // R_B]$$

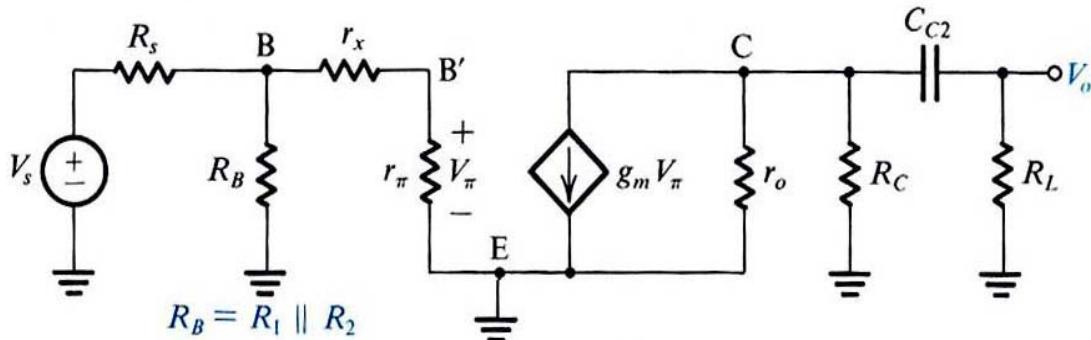
where  $i_b = V_\pi / r_\pi$

$$\therefore R' = \frac{r_\pi + r_x + R_S // R_B}{\beta + 1}$$

So we have two resistances in parallel to each other and the resistance seen by  $C_E$  is:

$$R'_E = R_E // \left[ \frac{r_\pi + r_x + (R_B // R_S)}{\beta + 1} \right] = R_E // R'$$

3. Consider  $C_{C2}$  with  $C_{C1}$  and  $C_E$  short-circuited. The equivalent resistance seen by  $C_{C2}$  is found by analysing the circuit below:



The capacitor effectively doesn't 'see' anything to the left of the current source and so we only need to consider  $R_C$ ,  $R_L$  and  $r_0$ .  $R_C$  and  $r_0$  are obviously in parallel, and  $R_L$  is effectively in series with both, so we have:

$$R_{C2} = R_L + (R_C // r_0)$$

## Estimate for $\omega_L$

We now have terms for each of the three capacitors. This means we can estimate the lower corner frequency for this circuit. Using the definition presented earlier (DP1) we have:

$$\omega_L = \frac{1}{C_{C1}R_{C1}} + \frac{1}{C_E R'_E} + \frac{1}{C_{C2}R_{C2}}$$

## Comments

We can see that the lower corner frequency is determined by capacitors **connected externally** to the transistor circuit. This means we can **design** for a specific value for  $\omega_L$  by choosing values for  $C_E$ ,  $C_{C1}$  and  $C_{C2}$ . When designing a circuit we make use of the fact that  $R'_E$  is the smallest resistance and select  $C_E$  so that the term due to it is the dominant pole. In a typical design  $C_E$  is selected so that we have  $1/C_E R'_E = 0.8\omega_L$  with the remaining 20% split evenly between the other two terms.

## 4.4 High-Frequency Analysis of Circuits

### 4.4.1 High-Frequency Response of Amplifiers

We have seen how we can design for the lower corner frequency of a circuit, since the corner is due to external capacitances. For higher frequencies, this is no longer the case and the behaviour of the transistor becomes paramount to the operation of the circuit (see aside). We will now see that, as will be shown, this is because **the poles in the amplifier transfer function are due to the internal capacitances of the transistor, which the designer has little control over.**

### 4.4.2 Open-Circuit Time Constant Method

To find the high-frequency breakpoint of an amplifier circuit, we will use the open-circuit time constant method.

Step 1: Redraw the circuit as its *AC equivalent*

Step 2: At high frequencies, large external (i.e. not in the transistor model) capacitors can be treated as *short circuits*.

Step 3: For *each capacitor* in the Hybrid- $\pi$  model, *open circuit* all other capacitors and find the equivalent resistance seen by this capacitor. You may need to apply Miller's Theorem at this stage.

Step 4: The high-frequency break point can be found from the as the inverse of the sum of the time constants:

$$\frac{1}{\omega_H} = \sum RC$$

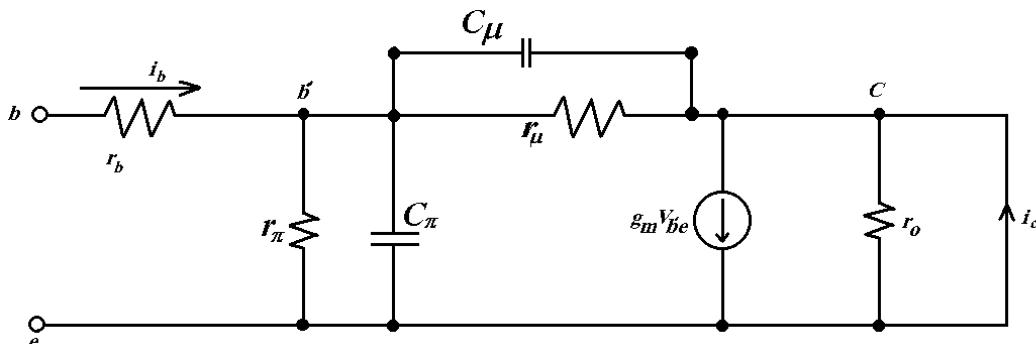
At the end of this section, we will present the high-frequency analysis of the common-emitter amplifier.

### 4.4.3 High Frequency Limit Of Hybrid- $\pi$ Model

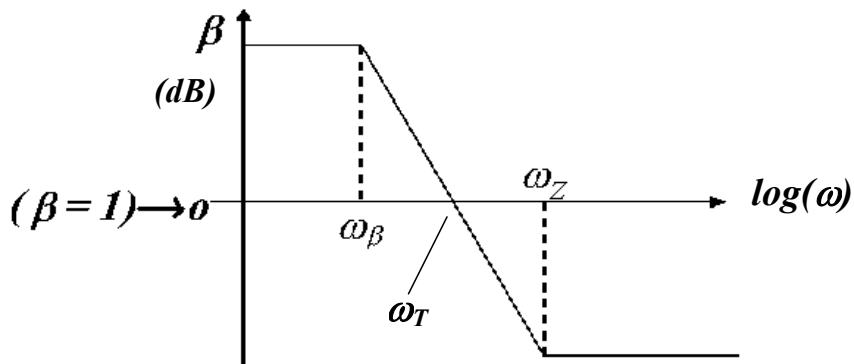
Consider a BJT operating at high frequency. The minority carriers in the base need time to diffuse from the emitter to the collector: the base transit time,  $\tau_t$ . The hybrid- $\pi$  model will work well for the case of  $\tau_t \ll 1/f$  where  $f$  is the frequency of the input signal.

A figure of merit is that we should have  $f$  such that  $f \leq 1/3f_T$  to ensure the hybrid- $\pi$  model works well.

$f_T$  is defined as the frequency at which the short-circuit current gain ( $\beta = h_{fe}$ ) of the transistor is unity. If we look at the hybrid- $\pi$  model again (see below), we see two capacitors in the circuit.



We would expect the response of the circuit to vary with frequency and this is the case. In fact the response of  $\beta = h_{fe} = \frac{i_c}{i_b} \Big|_{V_c=0}$  will look something like the graph below.



**Finding an expression for  $f_T$ .**

Let  $Z_\pi = r_\pi // \frac{1}{sC_\pi}$  and  $Z_\mu = r_\mu // \frac{1}{sC_\mu}$ . [note:  $s \equiv j\omega$ ]

So we will have:  $i_b = \frac{v_{b'e}}{Z_\pi // Z_\mu}$  and  $i_c = g_m v_{b'e} - \frac{v_{b'e}}{Z_\mu}$

It follows that  $h_{fe} = \frac{i_c}{i_b} = \frac{g_m - \frac{1}{Z_\mu}}{\frac{1}{Z_\pi} + \frac{1}{Z_\mu}}$ .

At high frequency, we can approximate  $\frac{1}{Z_\mu} \approx sC_\mu$  and  $\frac{1}{Z_\pi} = \frac{1}{r_\pi} + sC_\pi$

and so the expression for  $h_{fe}$  can be written as:

$$\begin{aligned} h_{fe} &= \frac{g_m - sC_\mu}{\frac{1}{r_\pi} + s(C_\pi + C_\mu)} \\ &= \frac{g_m r_\pi - s r_\pi C_\mu}{1 + s(C_\pi + C_\mu)r_\pi} \end{aligned}$$

which, since typically  $g_m \gg \omega C_\mu$ , gives:

$$\begin{aligned}
h_{fe}(j\omega) &= \frac{h_{fe}(0)}{1 + s(C_\pi + C_\mu)r_\pi} \\
&= \frac{h_{fe}(0)}{1 + j\omega(C_\pi + C_\mu)r_\pi} \\
&= \frac{h_{fe}(0)}{1 + j\omega/\omega_\beta}
\end{aligned}$$

where  $h_{fe}(0)$  is the low-frequency current gain (usually denoted by  $\beta_0$ ). This function has a single-pole response with a 3 dB frequency given by:

$$\omega_\beta = \frac{1}{(C_\mu + C_\pi)r_\pi}$$

It follows that the frequency at which  $h_{fe}$  drops to unity is given by:

$$\omega_T = h_{fe}(0)\omega_\beta = \frac{g_m}{C_\pi + C_\mu} \quad [\text{using } \frac{h_{fe}(0)}{r_\pi} = \frac{\beta}{r_\pi} = g_m]$$

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

Typically  $f_T$  is in the range of 100MHz to tens of GHz. In practice, both  $f_T$  and  $C_\mu$  are measured directly with  $C_\pi$  determined by using equation (F1).

Example:

$$\beta_{dc} = 100; C_\pi = 20 \text{ pF}, C_\mu = 2 \text{ pF}$$

For  $I_C = 0.2 \text{ mA}$ ,

$$r_\pi = \frac{\beta V_T}{I_C} = \frac{100 \times 25 \text{ mV}}{0.25 \text{ mA}} = 10 \text{ k}\Omega$$

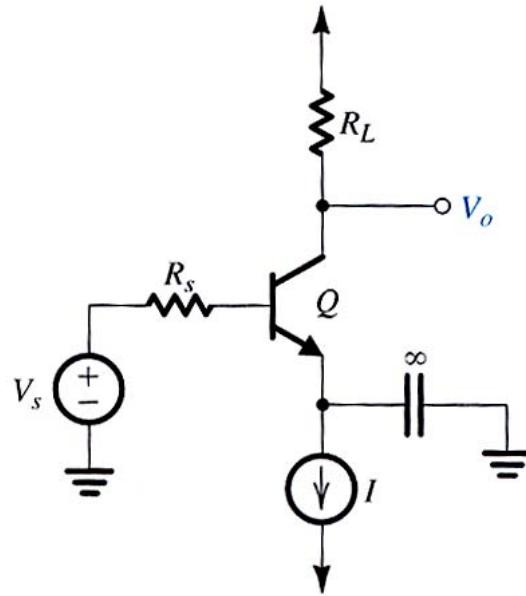
$$\text{So: } \omega_\beta = \frac{1}{22 \text{ pF} \times 10 \text{ k}\Omega} \approx 5 \times 10^6 \text{ rad/s} \quad \Rightarrow f_\beta = 1 \text{ MHz}$$

$$\text{So: } f_T = \beta_{DC} f_\beta \approx 100 \text{ MHz}.$$

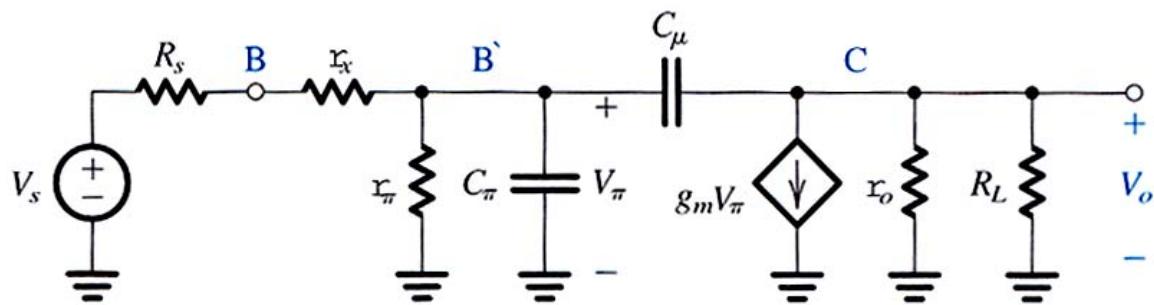
#### 4.4.4 High Frequency Response of the Common-Emitter Amplifier

The following is a simplified circuit diagram of a common-emitter amplifier, where  $V_s$  and  $R_s$  represent the Thévenin equivalent of the input circuit (recall the biasing circuit in the previous example). By the same token  $R_L$  represents the total resistance between the

collector and ground. The point is to try and highlight the transistor and its behaviour.



Using the hybrid- $\pi$  model for a BJT, we find the following small-signal equivalent circuit, (neglecting  $r_\mu$ , i.e., assume  $r_\mu \rightarrow \infty$ ):



We can now proceed as for the low-frequency case, only this time we would be open-circuiting capacitors apart from that of interest. For this case, however, we will use Miller's theorem to help gain some insight into the operation of the circuit.

Miller's theorem will be applied to the capacitor  $C_\mu$ . We assume that the current through  $C_\mu$  can be neglected since the value of  $C_\mu$  is so low. (At mid-band frequencies, we assume  $\frac{1}{\omega C_\mu} \rightarrow \infty$ .) This allows us

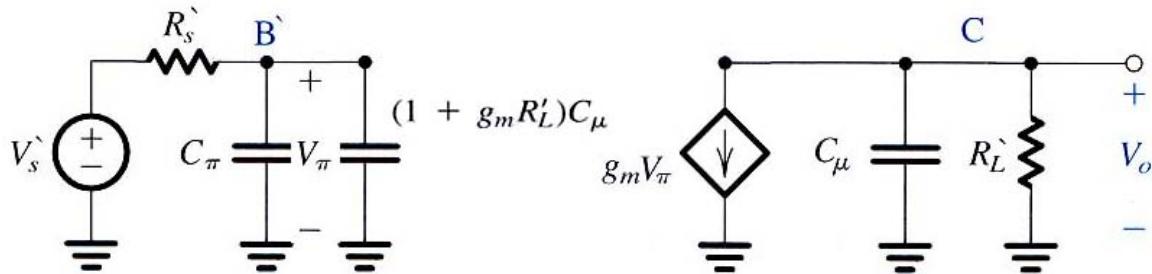
to easily calculate the gain (denoted  $K$  here), which we know from earlier to be  $K = \frac{v_C}{v_{B'}} = -g_m R'_L$ , where  $R'_L = R_L // r_0$ , since  $v_{B'} = V_\pi$  and  $v_C = -g_m V_\pi (R_L // r_0)$ .

So now we can replace  $C_\mu$  by two parallel capacitances with different respective values, using the Miller transformation, given by:

$$C_1 = C_\mu (1 + g_m R'_L)$$

$$C_2 = C_\mu \frac{(1 + g_m R'_L)}{g_m R'_L} \approx C_\mu$$

Inserting these into our small-signal equivalent circuit we end up with the following:



If we look at the input side of the circuit, we see that we have two capacitances in parallel, which means on the input side, we have a total capacitance given by:

$$C_T = C_\pi + (1 + g_m R'_L) C_\mu$$

On the output side we will have the capacitance  $C_\mu$ .

It is clear that the term due to the input side capacitance will be the dominant term in our calculation using equation (DP2). In this case the calculation of the higher corner frequency is straightforward.

$$\omega_H = \frac{1}{R'_s C_T}$$

where

$$R'_s = (R_s + r_x) // r_\pi$$

We could include the contribution of the output side capacitor but its effect would be minimal. (Applying the full open-circuit time constant method,  $\frac{1}{\omega_H} = R'_s C_T + R'_L C_\mu$ , in which the second term is small.)

---

Typically:  $C_\pi = 20 \text{ pF}$ ,  $C_\mu = 2 \text{ pF}$  and  $g_m R'_L = 500$ .

Then:  $C_T = 20 \text{ pF} + 1000 \text{ pF} = 1020 \text{ pF}$

## NOTES

This has shown us that the small capacitance  $C_\mu$  due to amplification gives rise to a substantial capacitance between the base and ground. This much larger capacitance will actually limit the high-frequency response of the circuit. **This multiplication of the effective value of the capacitance  $C_\mu$  is known as the MILLER EFFECT.**

**The Miller Effect will be the determining factor for high-frequency response in circuits that experience it.** Not all circuits do, however, and we will now look at a circuit that avoids the Miller effect – the common-base configuration.

One further note: the Miller transformation need not be used in order to simplify the analysis of a circuit. Most times, there will be little difference in calculations for the different approaches, but you must be careful not to make life more difficult than necessary by blindly applying a Miller transformation.

## 4.5 Improving the Frequency Response

We have just seen that the high-frequency response of an amplifier can be severely affected by the Miller effect – the multiplication of the capacitance  $C_\mu$ . We also saw that **not every circuit will suffer from the Miller Effect**. Unfortunately, high-gain amplifier circuits tend to suffer from the Miller effect and the question arises: can we get high gain from a circuit and minimise or even avoid the Miller effect?

Recall that the corner frequency,  $\omega_H$ , is determined by two things, namely:

1.  $C_\mu$  multiplication (the Miller effect) – signal feed through – observe that  $C_\mu$  is multiplied by  $(1 + |\text{gain}|)$   
For the CE case, this gain is  $\simeq |g_m R'_L|$ .
2. The resistance ‘seen’ by the capacitor  $(1 + |\text{gain}|)C_\mu$ .

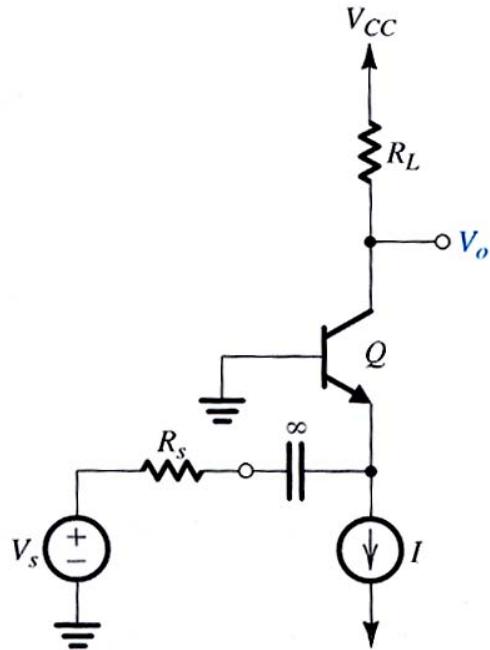
To improve on  $\omega_H$  we need to modify one of the terms or preferably both.

We must keep in mind that not all circuits suffer from the Miller effect and, in some cases, the Miller effect will decrease the effective capacitance (see the common collector, also called the emitter follower). The circuits now presented make use of these facts to provide excellent high-frequency response while maintaining a large mid-band gain.

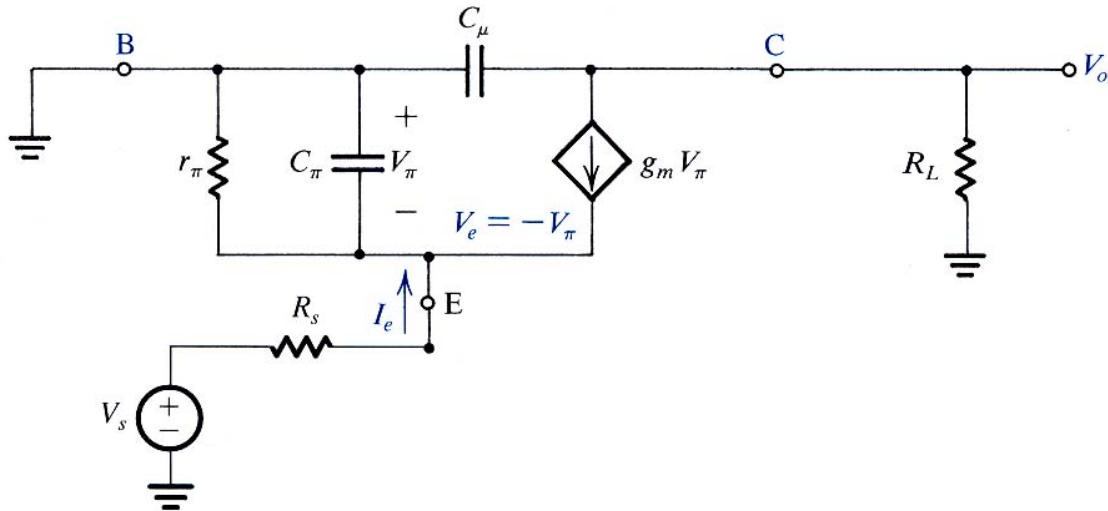
### 4.5.1 Avoiding the Miller Effect

#### The Common-Base Configuration

The common-base configuration is shown below. The circuit is somewhat simplified as for the case of the common emitter where  $V_s$  and  $R_s$  represent the Thévenin equivalent of the circuit feeding the amplifier. Again  $R_L$  represents the total resistance between the collector and signal ground.



For the small-signal equivalent circuit, we will neglect  $r_x$ ,  $r_\mu$  and  $r_0$  in order to observe the key feature of the circuit more readily. It is shown below:



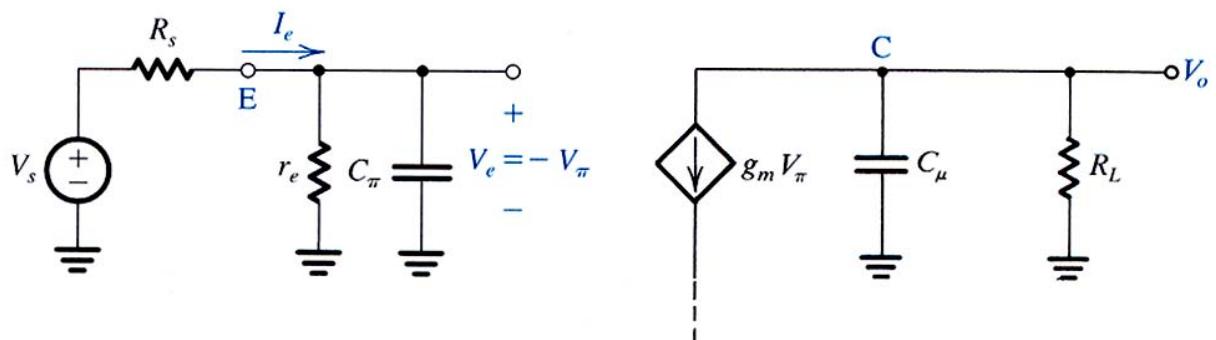
This can be modified by first observing that the voltage  $v_e$  at the emitter terminal (labelled E) is equal to  $-V_\pi$ . Further to this, we can write a node equation at E for the emitter current:

$$i_e = -V_\pi \left( \frac{1}{r_\pi} + sC_\pi \right) - g_m V_\pi = v_e \left( \frac{1}{r_\pi} + g_m + sC_\pi \right)$$

This means, looking into the emitter, we see an admittance given by:

$$\frac{i_e}{V_e} = \frac{1}{r_\pi} + g_m + sC_\pi = \frac{1}{r_e} + sC_\pi \quad [\text{We define: } \frac{1}{r_e} = \frac{1}{r_\pi} + g_m.]$$

From this, we can re-draw the equivalent circuit with the transistor replaced by the input admittance just found:

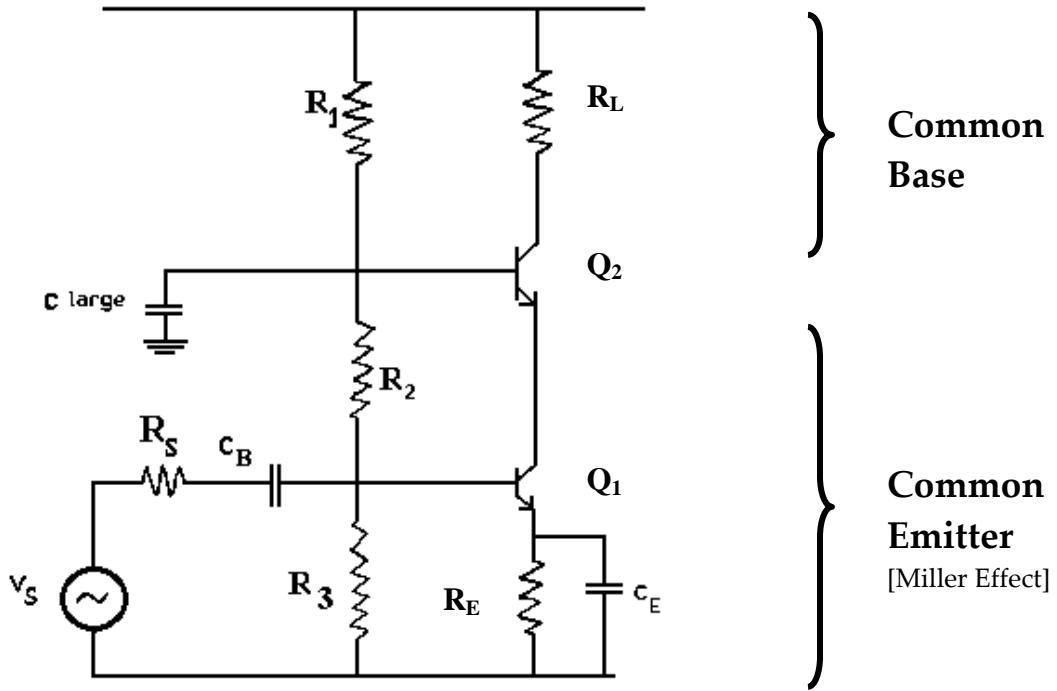


The most important aspect of this circuit is that there is **no feedback capacitor** as for the common-emitter circuit. This means that there is **no Miller effect** and we would expect the **higher corner frequency for the common-base circuit to be larger than that for a common-emitter circuit**.

## 4.5.2 The Cascode Configuration

Reduce the  $|gain|$  term by ensuring  $R'_L$  is low. This can be achieved by driving into the emitter of a common-base configuration.

**cascode configuration**



### Explanation:

The common-emitter stage sees the common-base stage as its load.

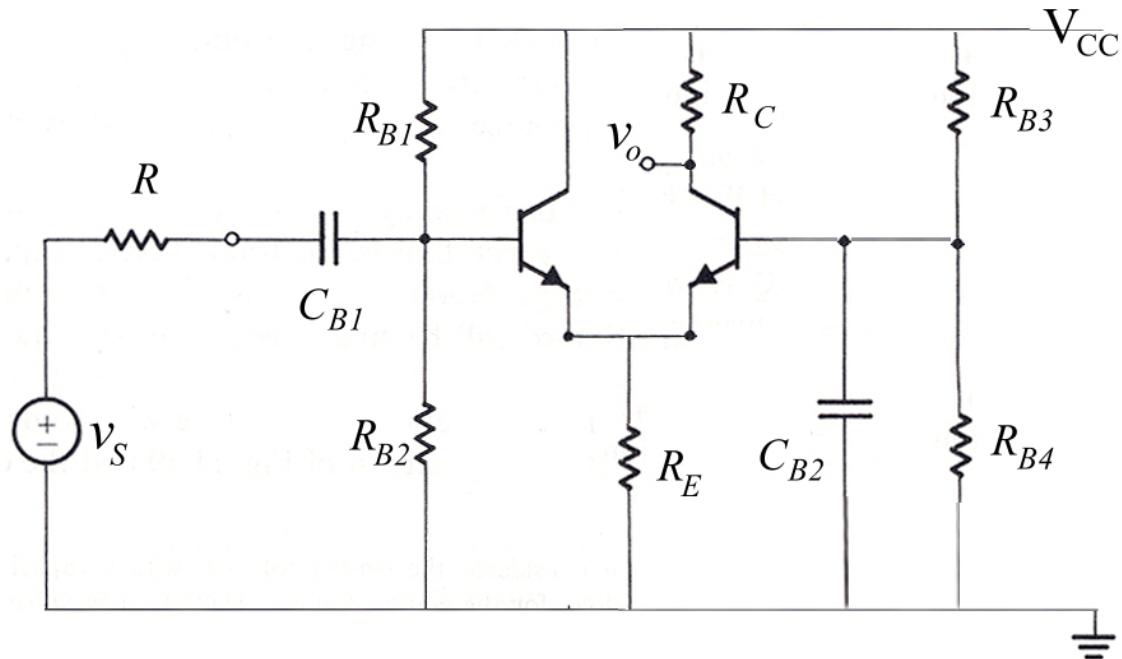
This load is equal to the output resistance of the common base stage which is equal to  $r_e$  – the emitter resistance typically  $\sim 25 \Omega$ , i.e., very low. This reduces the Miller effect since  $R'_L$  has been reduced. [Because  $r_e$  is small,  $r_e C_{Miller}$  is also small.]

Since the collector current through  $Q_2$  is approximately equal to that of  $Q_1$ , the mid-band gain doesn't suffer.

Another way to think of it is that  $Q_2$  is acting like a current buffer that passes on the signal current to the load while presenting a low load resistance to the amplifying transistor  $Q_1$ .

## 4.5.2 Common-Collector Common-Base Configuration, CC-CE Amplifier

'Long-Tailed Pair'



### Explanation

**Common Collector:** Low voltage gain.

Miller effect on  $C_\pi$  reduces the effective  $C_\pi$ .

$C_{\text{u}}$  is not multiplied.

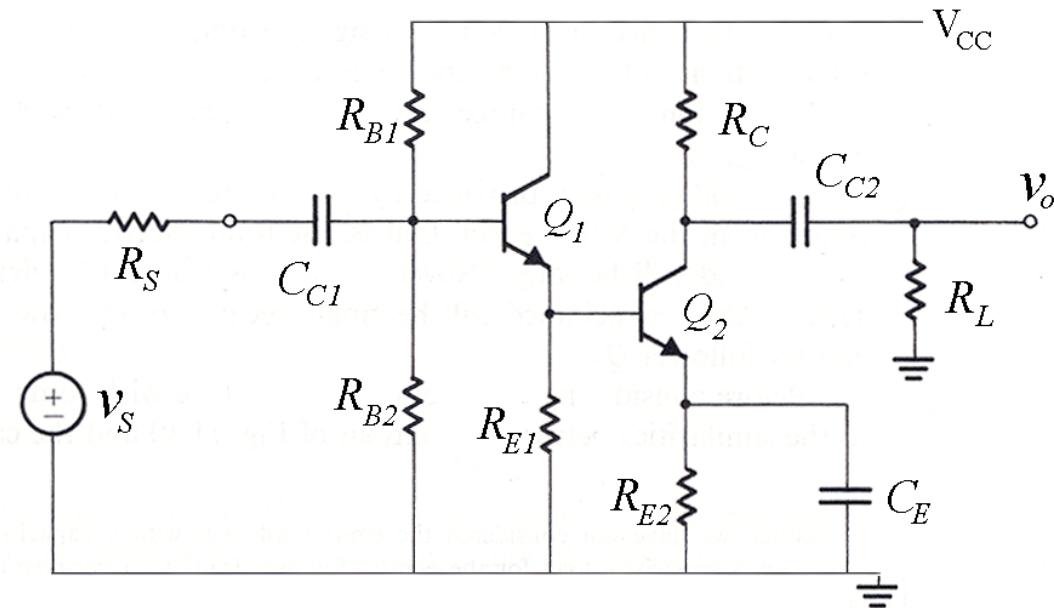
Provides current gain.

**Common Base:** Provides voltage gain.

### NOTE

This circuit is very similar to the differential amplifier presented earlier, though in this case a single ended input is provided. The bypass capacitor on the common-base side needs to be large to eliminate the effect of  $R_s$  in the base of Q<sub>2</sub> that has introduced a d.c. imbalance in the circuit.

## Common-Collector Common-Emitter Cascade



### Explanation

**Output resistance of C-C stage is very low** → looks like a signal source with very low output resistance.

The C-C stage doesn't suffer from the Miller effect.

The voltage gain is provided by the common-emitter stage, which does suffer from the Miller effect.

The multiplied capacitance of the common-emitter stage 'sees' a much smaller resistance due to the C-C stage → lower open circuit time constant → larger high corner frequency.

$$\frac{1}{\omega_H} = r_{cc} \times C_{\text{Miller}}$$

# **SECTION 5: FEEDBACK IN AMPLIFIERS**

## **5.1 The Feedback Concept**

## **5.2 The Four Basic Feedback Topologies**

- 5.2.1 Series-Shunt**
- 5.2.2 Shunt-Series**
- 5.2.3 Series-Series**
- 5.2.4 Shunt-Shunt**
- 5.2.5 Determining The Topology**

## **5.3 Properties of Negative Feedback**

- 5.3.1 Gain Desensitivity**
- 5.3.2 Reduction of Non-Linear Distortion & Noise**
- 5.3.3 Increase of Bandwidth**
- 5.3.4 Effect on Input Impedance**
- 5.3.5 Effect on Output Impedance**

## **5.4 Analysis of Feedback Amplifiers**

- 5.4.1 General Analysis Approach**
- 5.4.2 A Shunt-Shunt Case**
- 5.4.3 A Series-Series Case**
- 5.4.4 A Series-Shunt Case**
- 5.4.5 A Shunt-Series Case**
- 5.4.6 Hints & Summary**

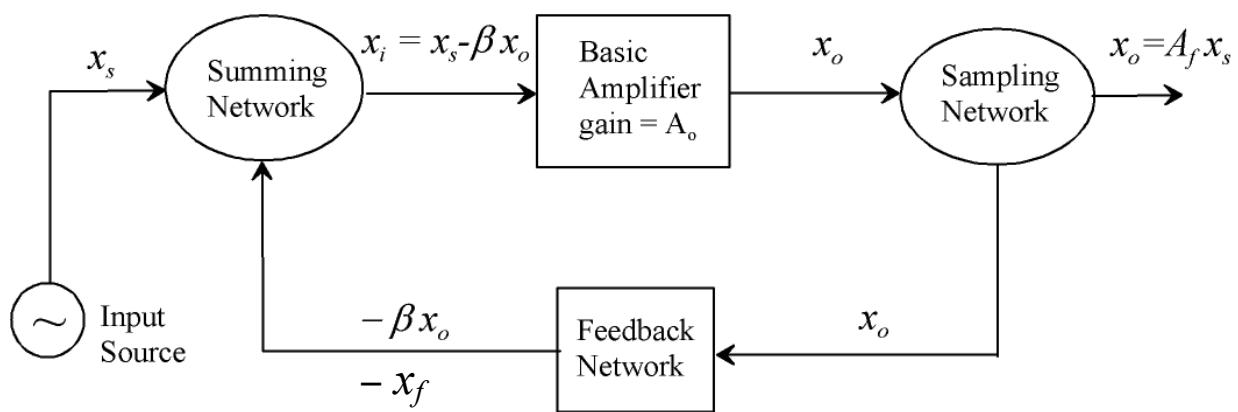
### **Aims**

After this section the student should know:

- the basic concept of feedback in circuit design;
- the effect of feedback on a circuit's performance;
- how to identify the feedback topology used in a feedback circuit; and
- how to analyse a circuit with feedback in order to obtain numerical and analytic values for key circuit parameters.

## 5.1 The Feedback Concept

When we refer to ‘feedback’, we mean any process where **a portion of the output is returned to the input to form part of the system excitation**. If appropriately applied, feedback can make a system self-regulating. The general idea of feedback is summed up in the signal-flow diagram below:



The signals  $x$ ,  $x_s$ ,  $x_o$  and  $x_i$  can be voltages or currents.  $A_o$  (open-loop gain) and  $\beta$  (feedback factor) are unilateral and  $\beta$  is independent of the source and load impedances.

Looking at the output from the open-loop amplifier we have:

$$x_o = A_o x_i$$

The sample of the output fed back to the input can be expressed as:

$$x_f = \beta x_o$$

If we take the feedback signal to be **subtracted from the input**, we will have, for the input signal:

$$x_i = x_s - x_f$$

This means that the output for the amplifier can now be expressed as:

$$\begin{aligned}x_i &= x_s - \beta x_o \\x_o &= A_o x_i = A_o(x_s - \beta x_o) = A_o x_s - \beta A_o x_o \\x_o(1 + \beta A_o) &= A_o x_s \\\Rightarrow x_o &= \frac{A_o}{(1 + \beta A_o)} \cdot x_s = A_f x_s\end{aligned}\tag{FB1}$$

It is also convenient to make the following definition:

$$T = A_o \beta\tag{FB2}$$

as the **loop gain** or **return ratio**.

The **closed-loop gain** is given by

$$A_f = \frac{A_o}{(1 + \beta A_o)}$$

## CAUTION

The sign of  $T$  is purely a convention; there are just as many instances where authors define  $T$  to be negative and the denominator of (FB1) to be  $1 - T$ . In this course, we will always **assume the positive convention**.

**NOTE:** for  $A_o \gg 1/\beta$ , we have  $A_f \approx 1/\beta$  – the **gain of the feedback amplifier is almost entirely determined by the feedback network**. Since the feedback network usually consists of passive components, i.e., resistors, etc., we can select our gain through the selection of components in the feedback network and be virtually independent of the basic amplifier.

There are two types of feedback possible:

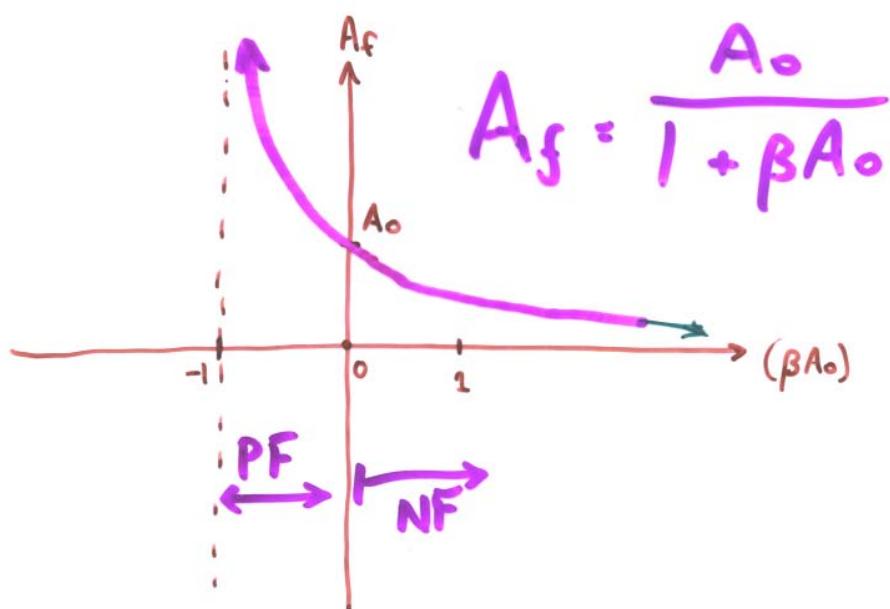
### Positive Feedback:

$A_o\beta < 0$ : this means that  $A_f > A$ , and, for the case of  $A_o\beta = -1$ , we will have  $A_f \rightarrow \infty$ . This will in fact lead to oscillations in the output of the circuit and stability problems – this will be looked at in further detail later.

### Negative Feedback:

$A_o\beta > 0$ : the system is stable provided there is enough of a phase margin. **When designing amplifiers negative feedback will always be used.**

**NOTE:** It may be tempting to think that positive feedback is useless. This is not the case, as will be seen in later sections dealing with circuits such as the Schmitt trigger.



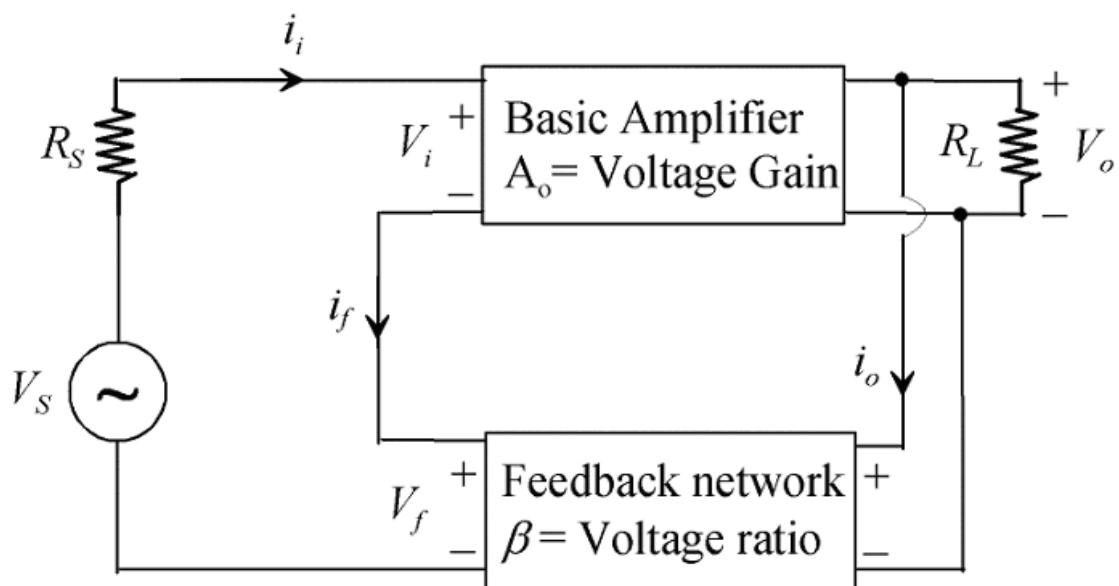
## 5.2 The Four Basic Feedback Topologies

### 5.2.1 Series-Shunt

#### [Voltage Sample – Voltage Sum]

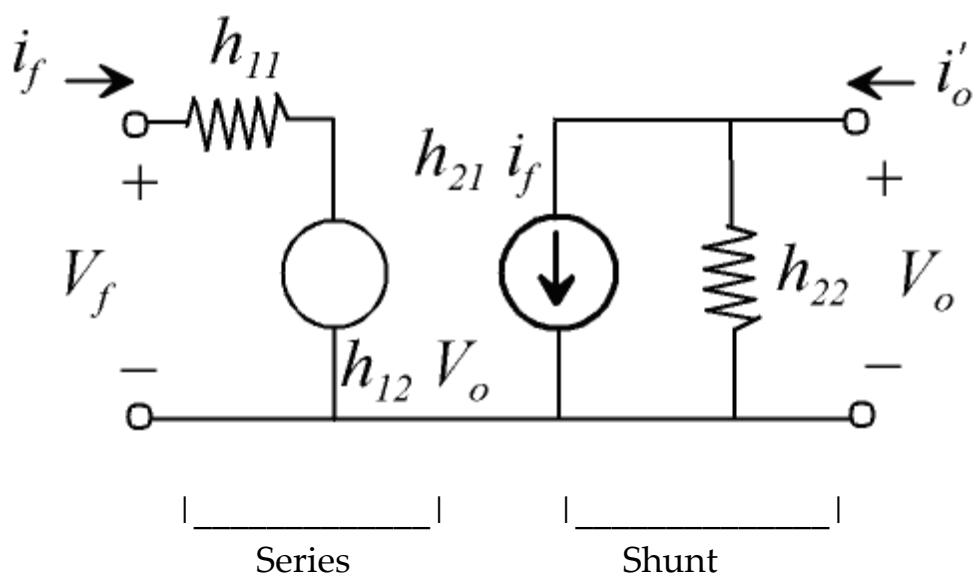
Assume that we have a **voltage amplifier** – voltage input with amplified voltage output. Since the output quantity is a voltage, it follows that any feedback network should **sample the output voltage**. It also follows that the feedback signal  $x_f$  should be a voltage that can be **added to the source voltage in series**.

This type of feedback topology – voltage sampling, series summing – is referred to as the **series-shunt configuration**. The series part refers to the input and shunt refers to the output. The feedback amplifier employing the series-shunt topology can be represented by the diagram below:



In this representation and for all subsequent, the basic amplifier is independent of all other elements of the circuit. The feedback network is an example of a two-port network. We can therefore use one of the two port network models to redraw the feedback network. In this case we have a **series network at port 1** and a **parallel network at port 2** – we will use the **h-parameter set**.

The feedback network is then recast as:



Note: 
$$h_{11} = \frac{v_f}{i_f} \Big|_{v_o=0}$$
      
$$h_{12} = \frac{v_f}{v_o} \Big|_{i_f=0} = \beta$$

$$h_{21} = \frac{i'_o}{i_f} \Big|_{v_o=0}$$
      
$$h_{22} = \frac{i'_o}{v_o} \Big|_{i_f=0}$$

$$h_{12} = \beta \equiv \text{feedback factor} \quad [v_f = \beta v_o]$$

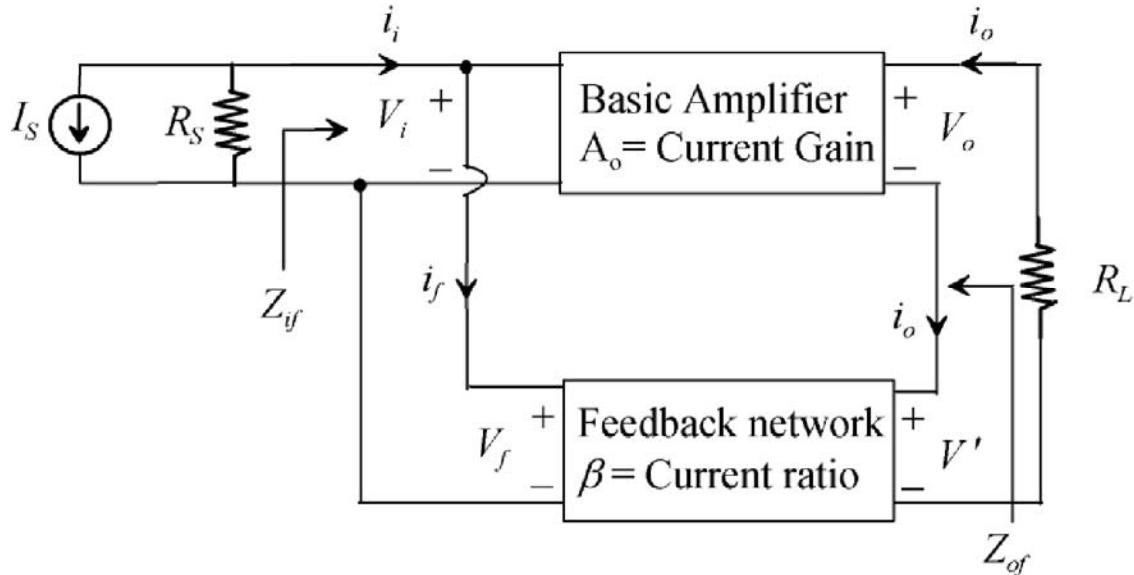
$h_{21}$  is a ‘feed-forward’ term, but we do not use it in this analysis.

## 5.2.2 The Shunt-Series Configuration

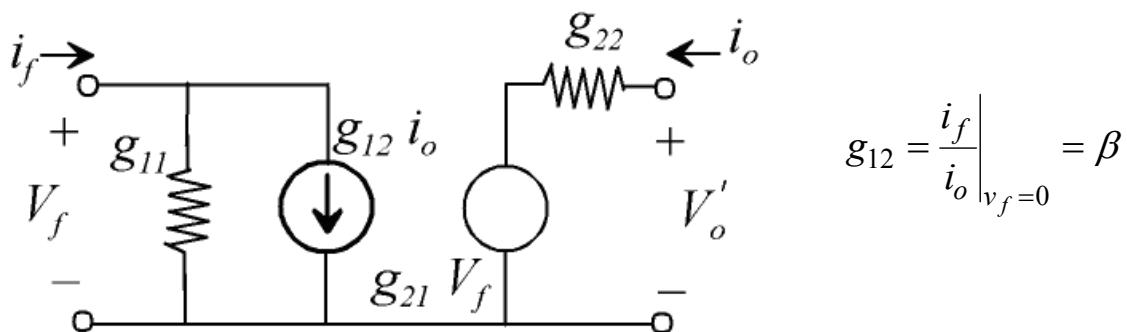
### [Current Sample – Current Sum]

Assume a current amplifier – current signal input with current signal output. In this case we want to sample the output current and so we have **current sampling**. The feedback signal needs to be a current and so it will be mixed in shunt with the input current, i.e., the **currents are summed** – we have current summing. In this case we have a **current sample–current sum topology** – this is referred to as a **Shunt-Series configuration**.

The Shunt-Series configuration is represented by the following diagram:



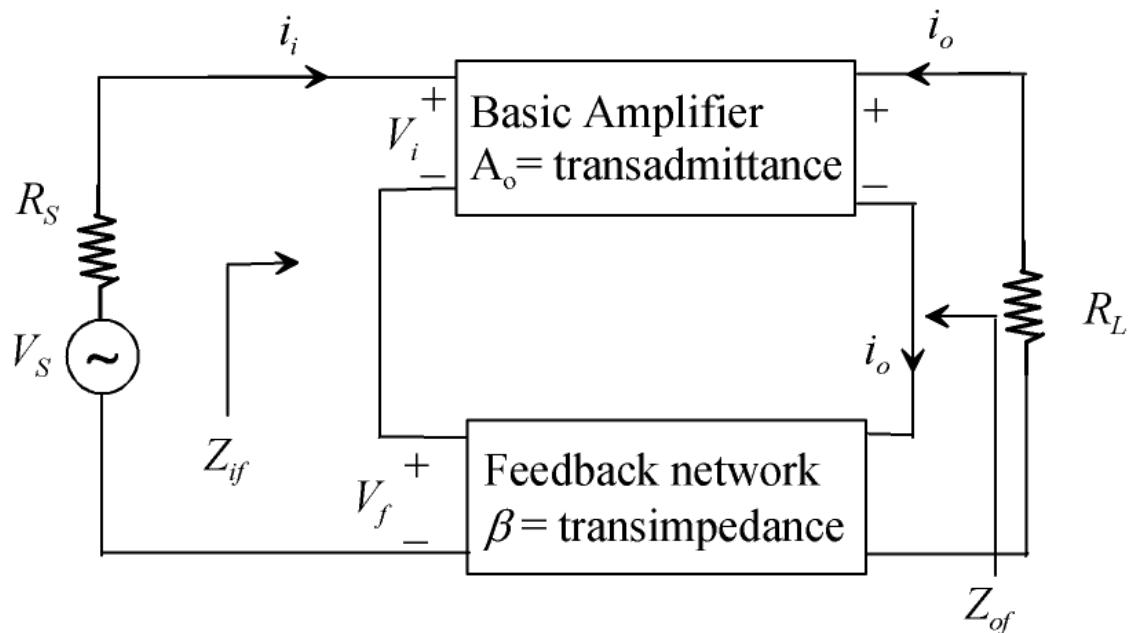
As for the Series-Shunt case the feedback network can be redrawn using two-port network parameters. In this case the ***g*-parameters** are used (parallel network at port 1, series network at port 2).



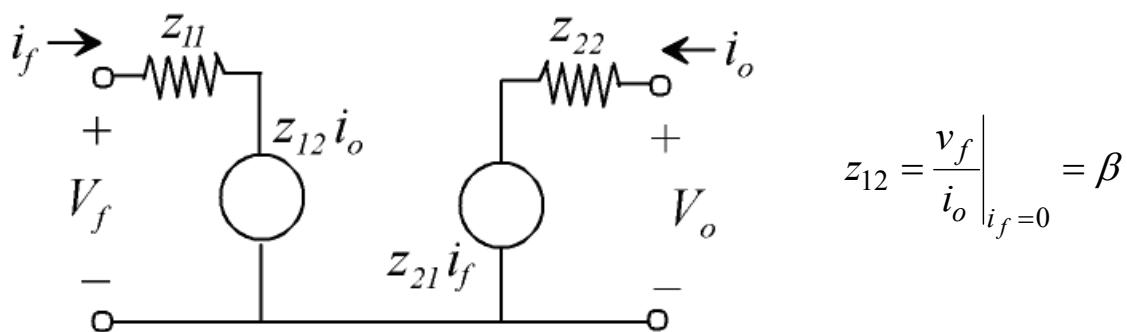
### 5.2.3 Series-Series Configuration

#### [Current Sample – Voltage Sum]

Assume a transconductance amplifier – voltage signal as input, a current signal as output. It follows that the appropriate feedback topology for this type of amplifier is **current sampling, voltage summing**. This type of topology is also referred to as the Series-Series configuration.



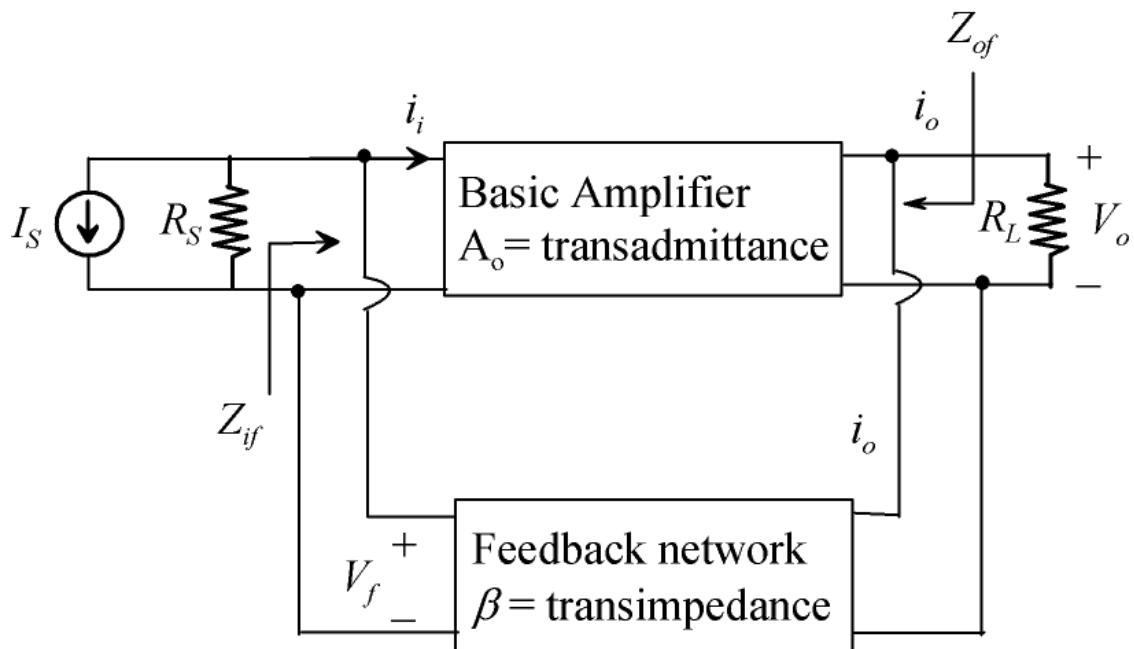
Since the feedback network has a series network at port 1 as well as at port 2 the appropriate two port parameters for the feedback network are the ***z*-parameters**.



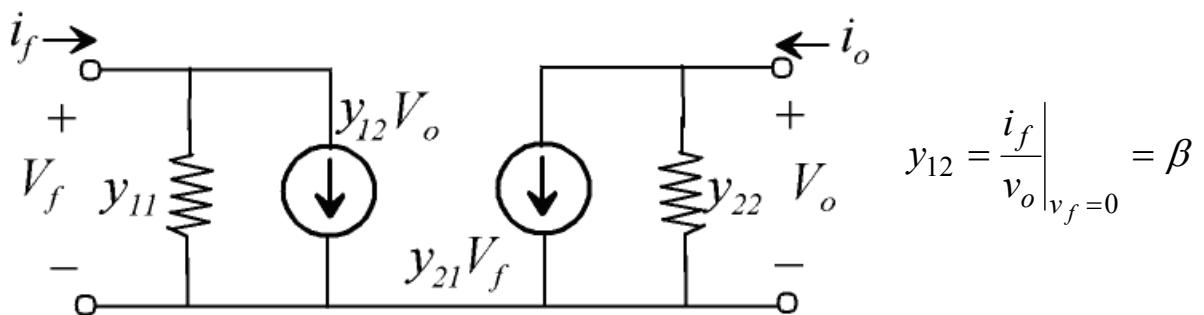
## 5.2.4 The Shunt-Shunt Configuration

### [Voltage Sample – Current Sum]

Assume a transresistance amplifier – current signal input, voltage signal output. It follows that the appropriate topology for such an amplifier is a **voltage sample, current sum configuration**. This is also referred to as the **Shunt-Shunt configuration**.



The feedback network is redrawn by using the **y-parameters** for two-port networks. This is because there is a parallel network at both port 1 and port 2 of the feedback network.



## 5.2.5 Determining the Feedback Topology

In the previous section, we found feedback topologies for amplifiers based upon the type of amplifier we had, i.e., voltage transconductance, etc. In general though, we want a method to determine the topology without prior knowledge of the operation of the amplifier. First, we make the following **assumptions**:

1. The **basic amplifier is unilateral** (it acts in only one direction), but its gain reflects the loading of the feedback network, and source and load resistances. The gain is that of the amplifier without feedback, i.e., open loop; we designate it  $A_{OL}$  in order to distinguish from the ideal situation.
2. The **feedback network is unilateral**. This can also be stated as assuming the feed-forward transmission through the  $\beta$  network is negligible in comparison to that through the amplifier.

**INPUT LOOP:** this is defined as **the mesh containing the applied signal source**.

If the **input signal is a voltage source**, the input loop will also contain either (a) the base-to-emitter region of the bjt or (b) the section between the two inputs of a differential or operational amplifier. If there is a circuit component in series with the voltage source, which is also connected to the output, the input connection is identified as **SERIES**.

If this is not true, replace the input voltage source with a current source. The input node is defined as either (a) the base of the first bjt or (b) the inverting terminal of a differential or operational amplifier. The current source sends a current to the input node and if a **connection between the input node and the output circuit exists, the configuration is identified as SHUNT**.

## **OUTPUT LOOP:**

Define  $V_o$  as the voltage across the load of the circuit (resistance  $R_L$ ) and  $I_o$  as the current flowing through  $R_L$ .

If the feedback signal becomes zero when  $v_o = 0$  the connection is sampling voltage - SHUNT.

If the feedback signal becomes zero when  $i_o = 0$  the connection is sampling current - SERIES.

## 5.3 Properties of Negative Feedback

### 5.3.1 Gain Desensitivity

We have already seen that the gain of the feedback circuit,  $A_f$ , will be smaller than the gain of the open loop amplifier (equation FB1). It also follows that changes in  $A_f$  will be related to changes in  $A \equiv A_o$  in the following way.

$$\begin{aligned}A_f &= \frac{A}{1 + \beta A} \\ \frac{dA_f}{dA} &= \frac{1}{1 + \beta A} + \frac{A}{(1 + \beta A)^2} (-\beta) = \frac{(1 + \beta A) - \beta A}{(1 + \beta A)^2} = \frac{1}{(1 + \beta A)^2} \\ dA_f &= \frac{dA}{(1 + \beta A)^2} \\ \therefore \frac{dA_f}{A_f} &= \frac{1}{(1 + \beta A)} \cdot \frac{dA}{A}\end{aligned}$$

This means that for negative feedback ( $\beta > 0$ ) the change in  $A_f$  will be less sensitive to changes in  $A$  by the factor  $(1 + \beta A)$ .

The reason that this property is important will now be shown for the cases of non-linear distortion and noise.

Example:

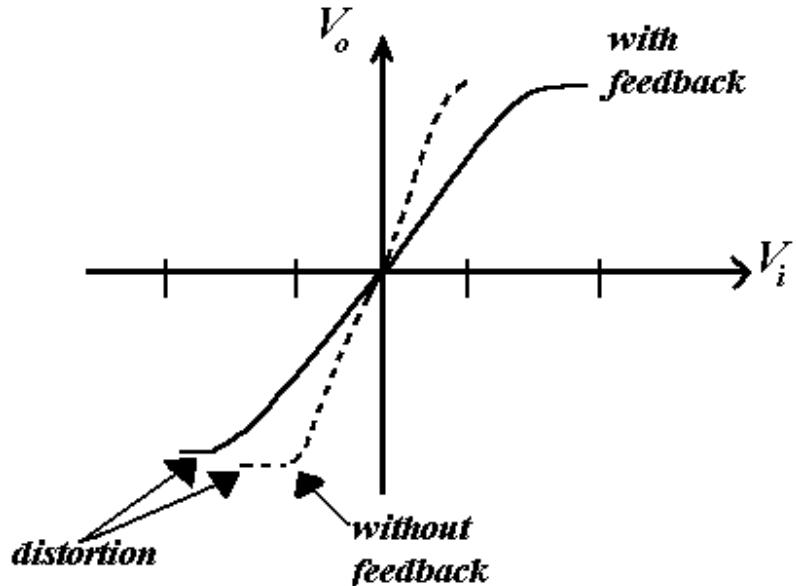
$$\begin{aligned}A &= 10^5, \quad \delta A = 10^2 \rightarrow \frac{dA}{A} = 10^{-3} \\ \beta &= 0.1 \rightarrow A_f = \frac{10^5}{1 + 10^4} \approx 10 = \frac{1}{\beta} \\ \frac{dA_f}{A_f} &= \frac{1}{(1 + 10^4)} \cdot \frac{dA}{A} = 10^{-4} \cdot 10^{-3} = 10^{-7} \\ A_f &= 10 \Rightarrow \delta A_f = 10^{-6}\end{aligned}$$

### 5.3.2 Reduction in Non-linear Distortion & Noise

#### Non-linear Distortion

If we look at the transfer characteristic of an amplifier, we will see that it is only piecewise linear, i.e., linear in certain regions but not in general. Since our analysis techniques rely on the linear response of an amplifier, we want to **maximise the range of inputs for which the amplifier behaves linearly**. The use of negative feedback achieves this objective.

We have just seen the gain with feedback,  $A_f$ , is desensitised to changes in  $A$ , the open-loop gain of the amplifier. Referring to the graph below, this means the slope of the transfer characteristic will be reduced by an amount determined by the return ratio. Since the onset of non-linearity will remain at the same output, **the input range for linear amplification has been extended**.



I.e., it keeps the amplifier away from saturation!

## Noise Reduction

Assume that an amplifier suffers from noise that is introduced at the input of the amplifier  $A_1$ . The signal-to-noise ratio for the amplifier  $A_1$  is taken to be:

$$S/N = V_s/V_n$$

If we can now precede the amplifier,  $A_1$ , by a 'clean' amplifier (one that doesn't suffer from the noise problem), called say  $A_2$ , and also include negative feedback around the whole circuit, the situation can be improved. The output voltage of such an arrangement, shown below, is:

$$V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta}$$

The signal-to-noise ratio for the total circuit is then given by:

$$S/N = \frac{V_s}{V_n} A_2 \quad (\text{FB3})$$

**Conclusion:** The signal-to-noise ratio has been improved markedly and the negative feedback allows the gain of the circuit to be kept constant.

### 5.3.3 Extension of Bandwidth

Consider amplifier that can be characterised with a single-pole function:

$$A(s) = \frac{A_o}{1 + s/\omega_H} \quad (\text{FB4})$$

$A_o$  is the mid-band gain and  $\omega_H$  is the high corner (3 dB) frequency. With feedback applied and a frequency-independent return ratio  $\beta$  we will have:

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

This can be recast using equation (FB4) as:

$$\begin{aligned} A_f(s) &= \frac{A_o / (1 + s/\omega_H)}{1 + \beta A_o / (1 + s/\omega_H)} \\ &= \frac{A_o}{(1 + s/\omega_H) + \beta A_o} = \frac{A_o}{(1 + \beta A_o) + \frac{s}{\omega_H}} \\ \Rightarrow A_f(s) &= \frac{A_o / (1 + \beta A_o)}{1 + \frac{s}{\omega_H (1 + \beta A_o)}} \end{aligned}$$

The high corner frequency for the amplifier with feedback is then given by:

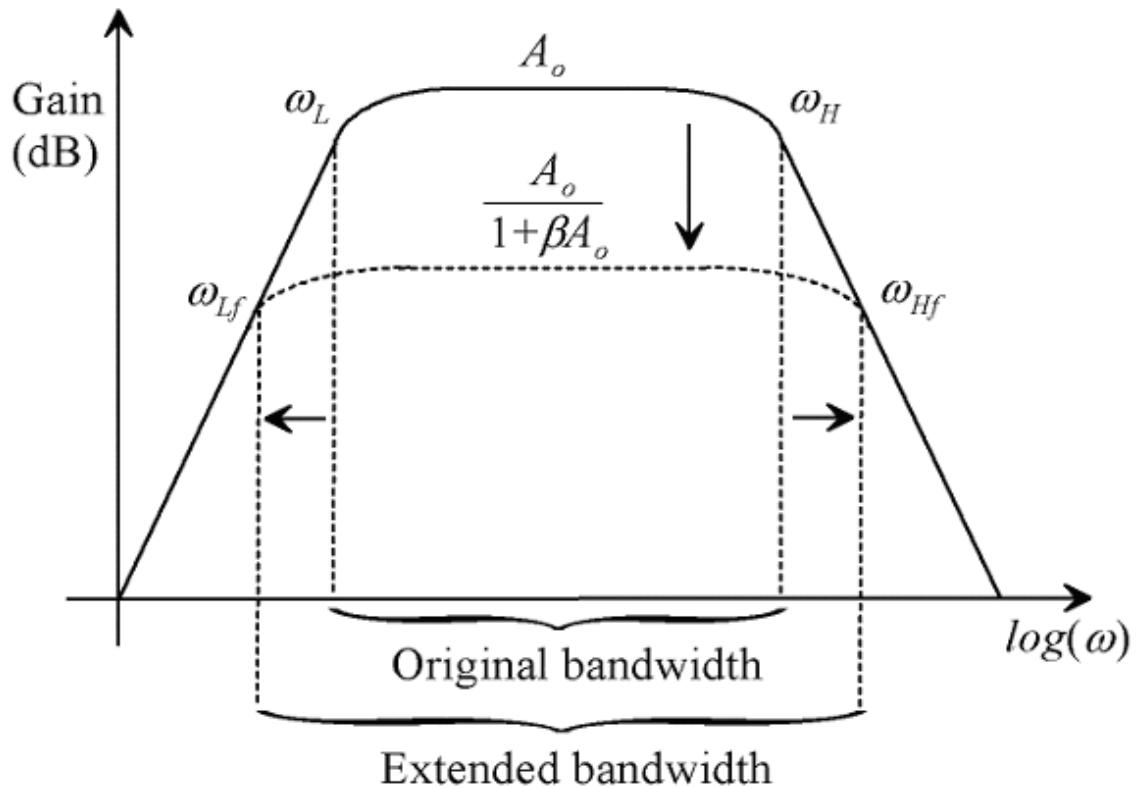
$$\omega_{fH} = (1 + \beta A_o) \omega_H$$

By a similar argument for the low corner frequency we find:

$$\omega_{fL} = \omega_L / (1 + \beta A_o)$$

where  $\omega_L$  is the low corner frequency of the amplifier without feedback.

**CONCLUSION:** The bandwidth of the amplifier ( $\omega_H - \omega_L$ ) has been increased by the feedback factor ( $1 + \beta A_o$ ).



### 5.3.4 Effect On Input Impedance

- Feedback signal is a voltage in series with input  
 $\Rightarrow$  input impedance is increased by the factor  $(1+\beta A)$ .

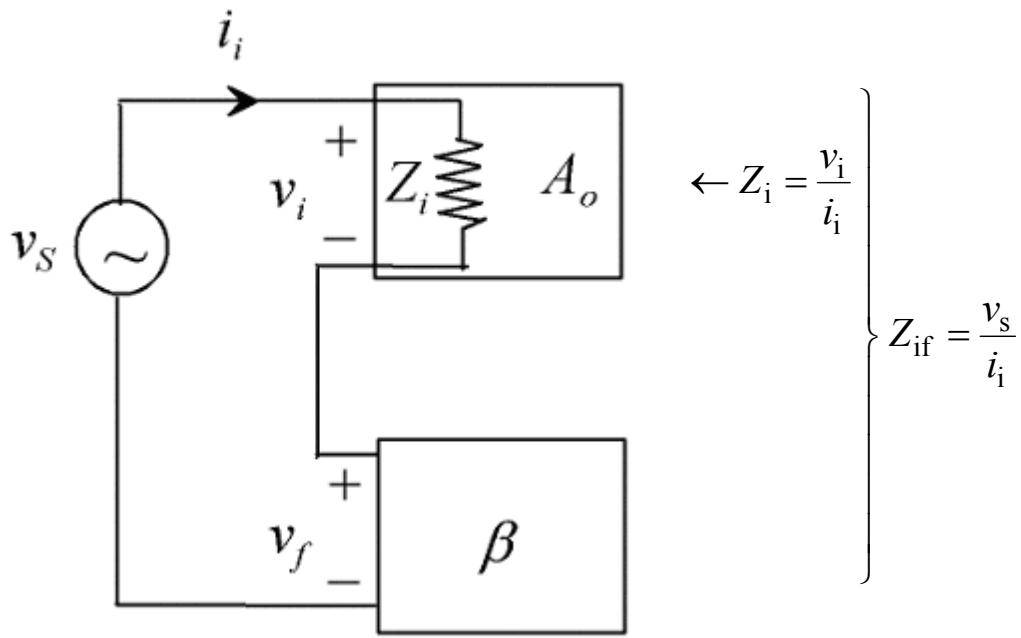


Figure I1: input impedance definition for series connection

*Proof*

Let the input be designated:

$$v_i = v_s - v_f, \quad v_f = \beta v_o, \quad v_o = A v_i \\ \therefore v_i = v_s - \beta A v_i \quad \Rightarrow \quad v_s = (1 + \beta A) v_i$$

Now if we denote  $Z_i$  as the input impedance without feedback and  $Z_{if}$  the input impedance with feedback, we have:

$$Z_{if} = \frac{v_s}{i_i} = \frac{(1 + \beta A) v_i}{i_i} = (1 + \beta A) Z_i \quad (\text{FB5})$$

2. Feedback signal is a current in shunt with input  $\Rightarrow$  the input impedance is decreased by the factor  $(1+\beta A)$ .

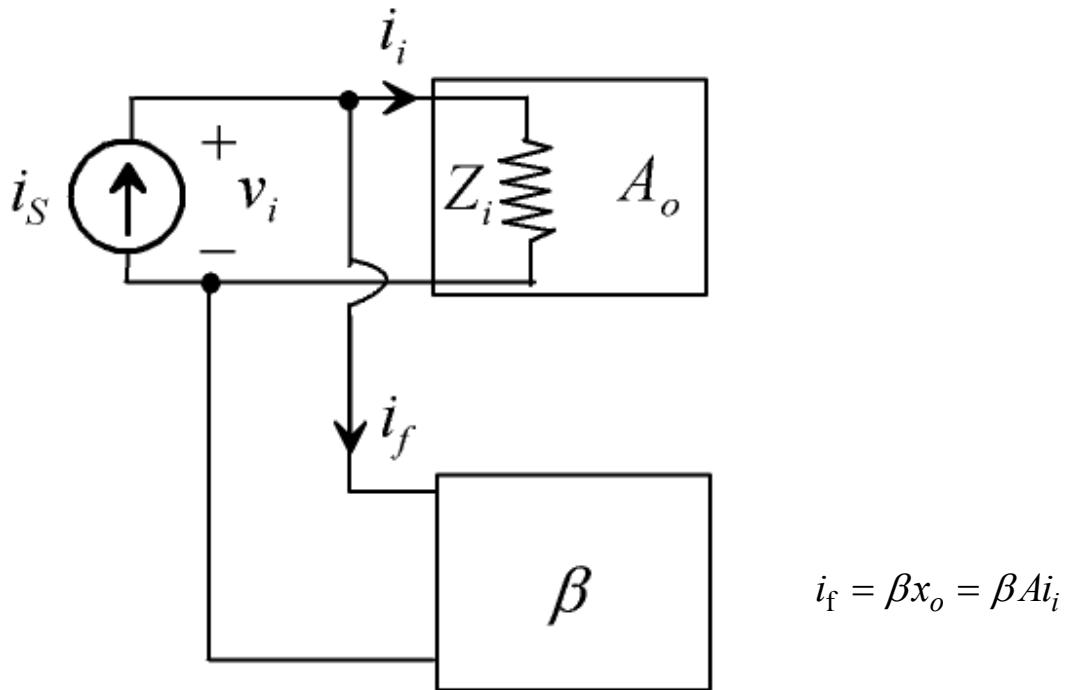


Figure I2: input impedance definition for shunt connection.

*Proof*

Let the input be designated:

$$i_i = i_s - i_f = i_s - \beta A i_i \Rightarrow i_s = i_i (1 + \beta A)$$

With similar notation to the previous proof, we will have for the input impedance:

$$Z_{if} = \frac{v_i}{i_s} = \frac{v_i}{(1 + \beta A)i_i} = \frac{Z_i}{(1 + \beta A)} \quad (\text{FB6})$$

### 5.3.5 Effect On Output Impedance

- Feedback configuration is a shunt connection (voltage sampling)  $\Rightarrow$  output impedance is reduced by the factor  $(1+\beta A)$ .

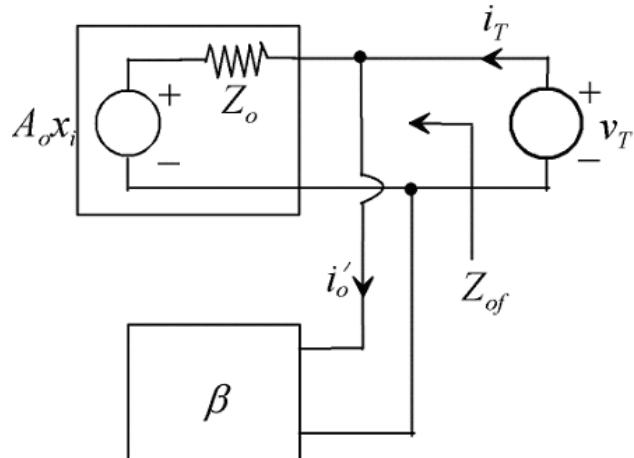


Figure O1: output impedance definition for shunt connection.

*Proof*

$x_i$  can be either  $v_i$  or  $i_i$ . N.b., the  **$Z_o$  of the basic amplifier includes the loading of the feedback network**. Since the feedback network is unilateral, we have either  $y_{21} = 0$  or  $h_{21} = 0$ . So  $i'_{of} = 0$ .

The output impedance is defined as:

$$Z_{of} = \left. \frac{v_T}{i_T} \right|_{\substack{\text{source set} \\ \text{to zero}}}$$

$$i_T = \frac{v_T - Ax_i}{Z_o}$$

When we have either  $v_s$  or  $i_s = 0$  (depending on whether source is a voltage or a current)  $\Rightarrow x_i = -x_f = -\beta v_T$ . [Note:  $x_i = x_s - x_f$ ]

$$\begin{aligned} i_T &= \frac{v_T(1 + \beta A)}{Z_o} \\ \therefore Z_{of} &= \frac{Z_o}{(1 + \beta A)} \end{aligned} \tag{FB7}$$

2. Feedback configuration is a series connection (current sampling)  $\Rightarrow$  output impedance is increased by the factor  $(1+\beta A)$ .

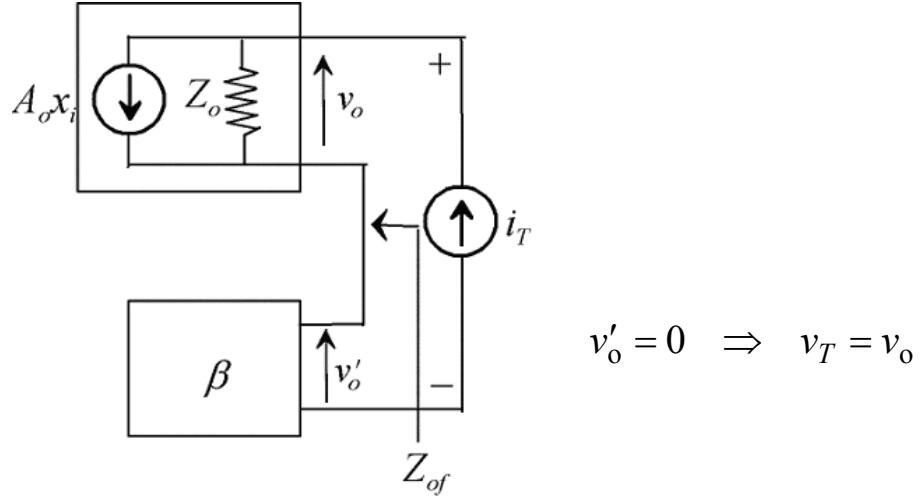


Figure O2: output impedance definition for series connection.

*Proof*

Since feedback network is unilateral, we have either  $z_{21}=0$  or  $g_{21}=0$ .  
 $\Rightarrow v'_o = 0$

$$i_T = Ax_i + \frac{v_T}{Z_o}$$

$$x_i = -x_f = -\beta i_T \Rightarrow i_T = -\beta A i_T + \frac{v_T}{Z_o} \Rightarrow (1 + \beta A) i_T = \frac{v_T}{Z_o}$$

If we then apply the definition of the output impedance from the previous part, we have:

$$Z_{of} = \frac{v_T}{i_T} = (1 + \beta A) Z_o \quad (\text{FB8})$$

## 5.4 Analysis of Feedback Amplifiers

### 5.4.1 General Analysis Approach

When we are performing **approximate analysis** on a feedback amplifier, the following assumptions are made:

1. The basic amplifier is unilateral (transmits only from input to output).
2. The feedback network is unilateral (transmits only from the output to the input). This implies that, depending on the topology,  $z_{21}$ ,  $g_{21}$ ,  $y_{21}$  or  $h_{21} = 0$ .
3. The gain of the basic amplifier includes the loading effect of the feedback network as well as the source and load impedances.

It is these assumptions that allow analysis.

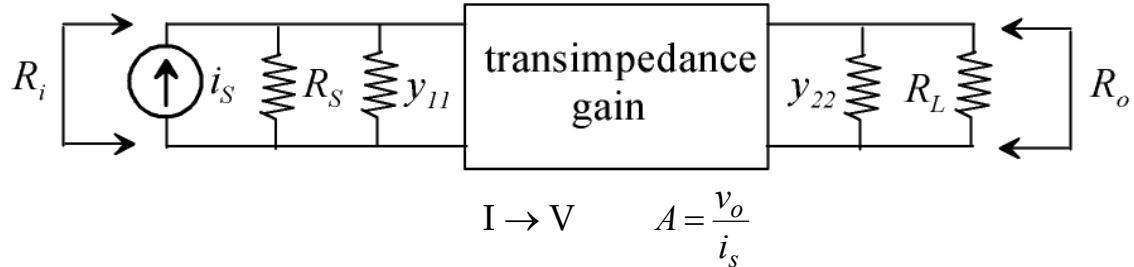
The following is a general plan for the analysis of a feedback amplifier. There will be occasions where there may be a slight variation in approach but, by following this plan, you can analyse any feedback amplifier circuit.

### General Approach

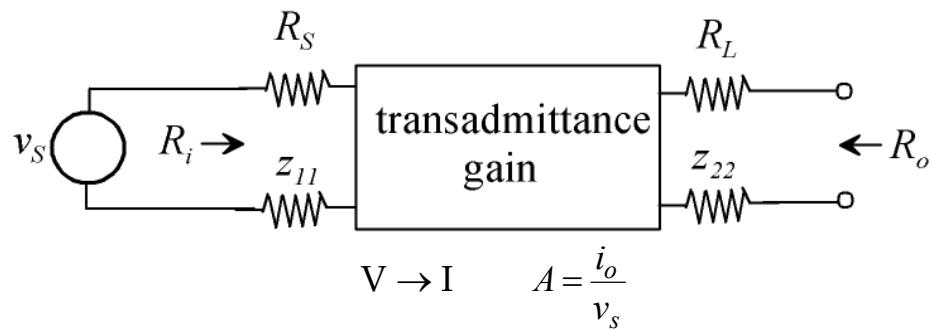
- I. **Identify the feedback topology.** The methods for the determination of the topology have been covered earlier.
- II. **Redraw the basic amplifier in a form suitable for small-signal analysis.** This consists of:
  - a) replacing active devices (i.e., transistors, op-amps, etc.) with the appropriate small-signal models, e.g., hybrid- $\pi$ ; and
  - b) including the loading effect of the feedback network on the input and output sections of the overall circuit.

## Examples

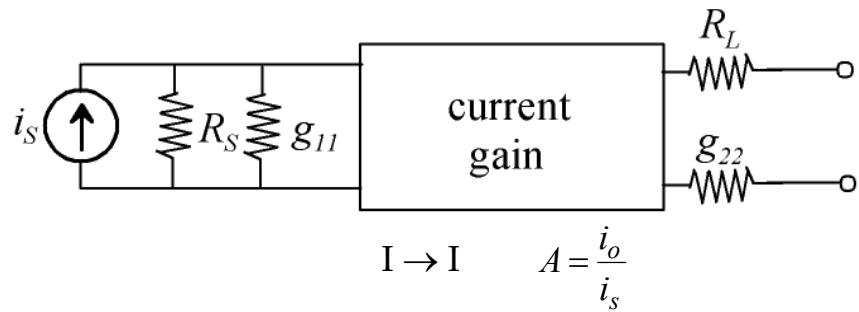
### A. Shunt-Shunt



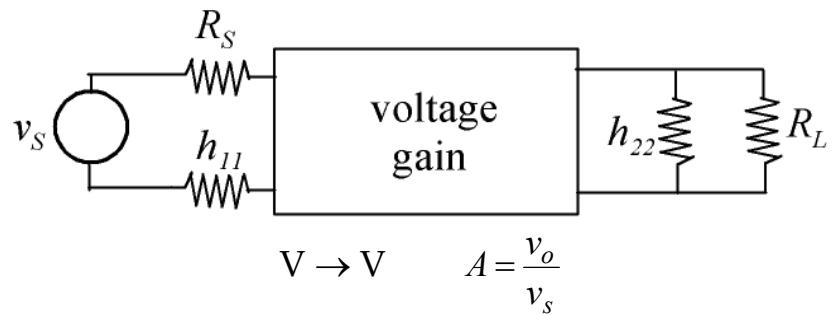
### B. Series-Series



### C. Shunt-Series



### D. Series-Shunt



The loading effects can be obtained by the following:

(i) input circuit

- voltage summing (series) – evaluate  $z_{11}$ ,  $h_{11}$  under the condition  $i_o = 0$ .
- current summing (shunt) – evaluate  $y_{11}$ ,  $g_{11}$  under the condition  $v_o = 0$ .

(ii) output circuit

- current sampling (series) – evaluate  $z_{22}$  and  $g_{22}$  under the condition  $v_i = 0$ .
- Voltage sampling (shunt) – evaluate  $h_{22}$  and  $y_{22}$  under the condition  $i_i = 0$ .

III. Identify  $x_o$  and  $x_f$  in order to evaluate the feedback factor:

$$\beta = \frac{x_f}{x_o}$$

which corresponds to one of  $y_{12}$ ,  $g_{12}$ ,  $z_{12}$ ,  $h_{12}$ .

IV. Evaluate the open loop gain  $A_{OL}$ . The form of  $A_{OL}$  will depend on the topology, i.e., whether it is a trans-impedance, voltage gain, etc. [N.B.: Calculations include loading from feedback network.]

V. Evaluate the input and output impedances of the basic amplifier with the loading effects of the feedback network included.

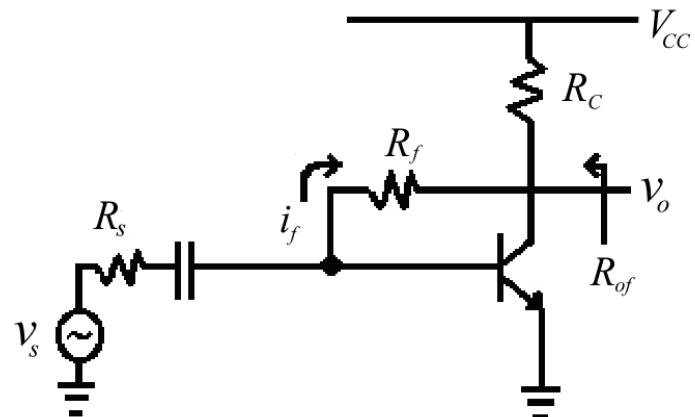
VI. Evaluate the following:

- Loop gain  $\beta A_{OL}$ .
- Closed loop gain  $A_f = \frac{A_{OL}}{1 + \beta A_{OL}}$
- Input and output impedances using equations FB5-8.

## 5.4.2 A Shunt-Shunt Case

[Voltage-Sample Current-Sum]

Collector-feedback bias circuit



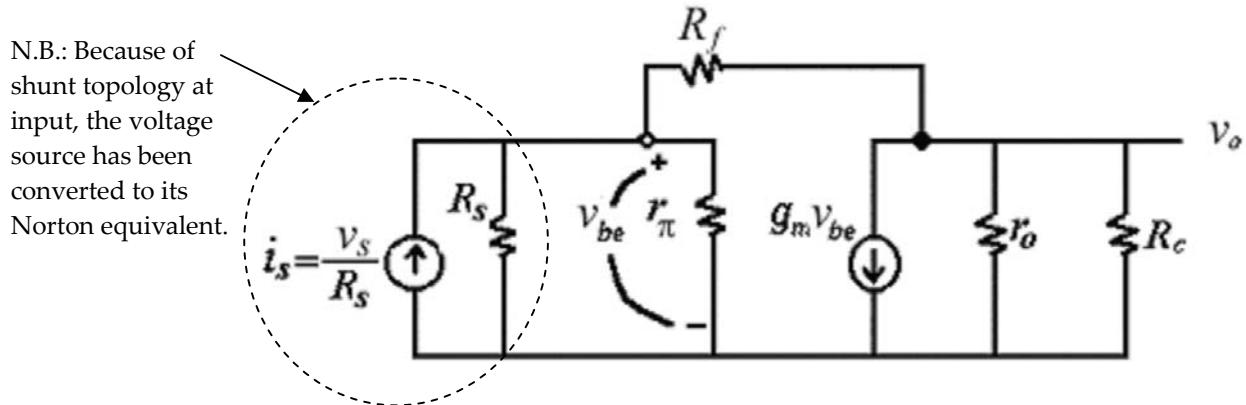
**Determine feedback topology:**

Output – set  $v_o=0$ . The feedback current if is disabled  
→ **voltage sample** (shunt)

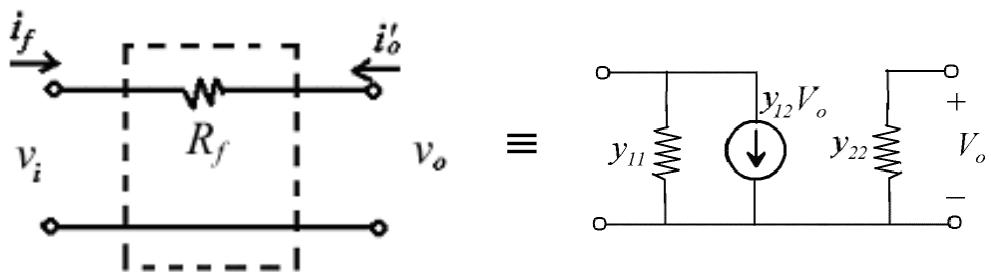
Input – current is being fed back to the input at a node  
→ **current sample** (shunt)

## SHUNT-SHUNT TOPOLOGY

Redraw circuit for small-signal analysis.



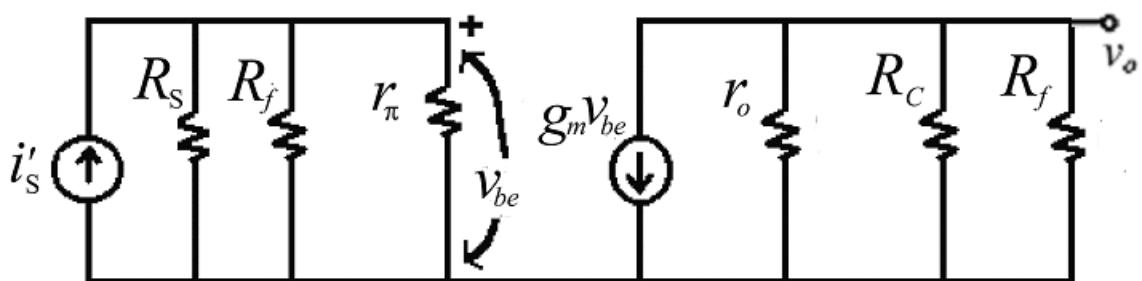
Consider the loading effect of  $R_f$  on the basic circuit next.



We make use of the **y-parameters** in this case:

$$y_{11} = \left. \frac{i_f}{v_i} \right|_{v_o=0} = \frac{1}{R_f} \quad y_{22} = \left. \frac{i'_o}{v_o} \right|_{v_i=0} = \frac{1}{R_f}$$

The circuit can now be re-drawn in the following manner:



Find the **feedback factor**:

$$\beta = y_{12} = \left. \frac{i_f}{v_o} \right|_{v_i=0} = -\frac{1}{R_f}$$

Now the open-loop gain: in this case we are after a **trans-impedance**, since the input is a current and the output a voltage.

$$A_{OL} = \frac{v_o}{i'_s}$$

If we define:  $R_i = R_s // R_f // r_\pi$  and  $R_o = R_C // R_f // r_o$

We will have:  $v_{be} = i_s' R_i$  and  $v_0 = -g_m v_{be} R_o$

Allowing the **open-loop gain** to be expressed as:

$$A_{OL} = \frac{v_o}{i'_s} = \frac{-g_m v_{be} R_o}{v_{be}/R_i} = -g_m R_i R_o$$

We can now find the closed loop expressions for this circuit. First, the **closed-loop gain**:

$$A_f = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{-g_m R_i R_o R_f}{R_f + g_m R_i R_o}$$

Note:  $A_f \rightarrow -R_f = \frac{1}{\beta}$  for  $|A_{OL}| \rightarrow \infty$

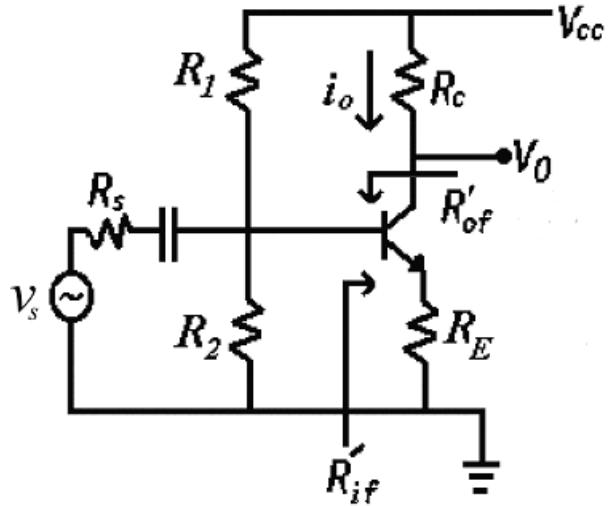
Now the **closed-loop input and output impedances**:

$$R_{if} = \frac{R_i}{1 + \beta A_{OL}} = \frac{R_i}{\left(1 + \frac{g_m R_i R_o}{R_f}\right)}$$

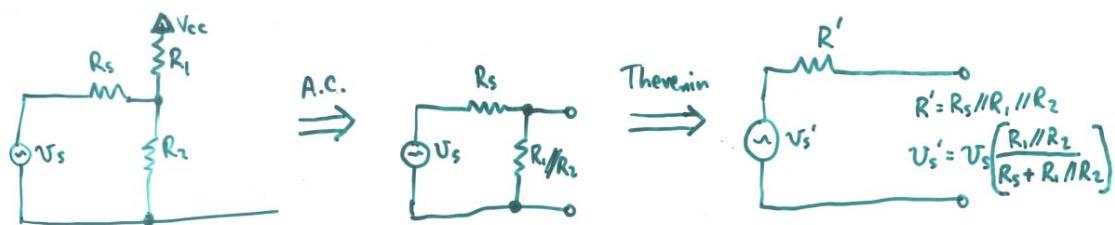
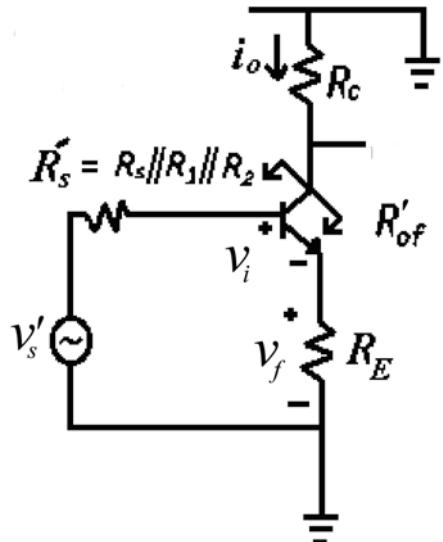
$$R_{of} = \frac{R_o}{1 + \beta A_{OL}} = \frac{R_o}{\left(1 + \frac{g_m R_i R_o}{R_f}\right)}$$

### 5.4.3 A Series-Series Case

'Common-Emitter' Amplifier with Emitter Resistor.



The first thing to do is to simplify the circuit slightly in order to make analysis more straightforward.



## Identify the Topology

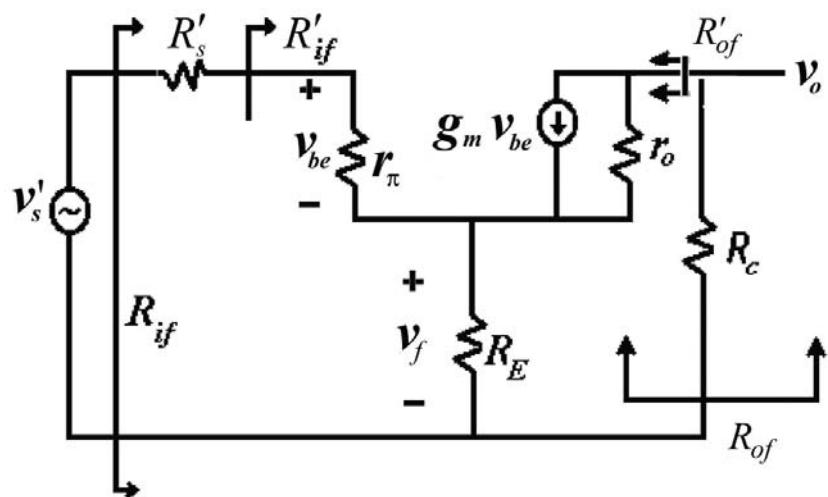
Input circuit –  $v_f$  has been included in series with  $v_s$  and  $v_i$ . This means we have a **series connection**.

Output circuit – set  $v_o = 0$ . In this case  $v_f$  is unaffected.

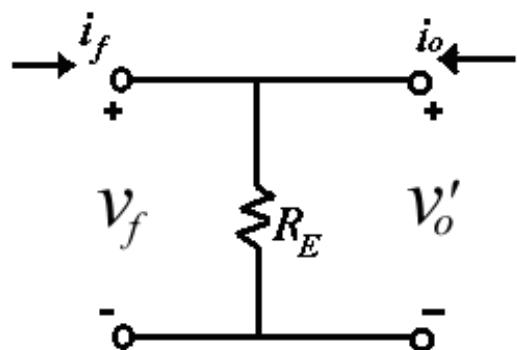
Set  $i_o = 0$ . In this case  $v_f = 0$ . We have a **series connection**.

### SERIES-SERIES TOPOLOGY

Draw the equivalent circuit for small signal analysis.



$R_E$  is now identified as the feedback element.

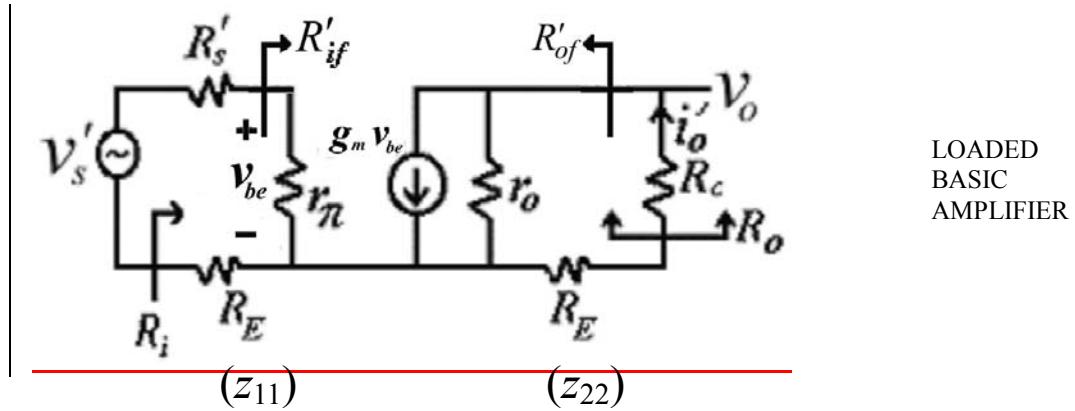


Since topology is series-series we use the z-parameters:

$$z_{11} = \left. \frac{v_f}{i_f} \right|_{i_o=0} = R_E \quad z_{22} = \left. \frac{v'_o}{i_o} \right|_{i_f=0} = R_E$$

$$\beta = z_{12} = \left. \frac{v_f}{i_o} \right|_{i_f=0} = R_E$$

Include the loading effect of the feedback network into the basic circuit to calculate open loop parameters.



Since topology is series-series, **the gain will be a trans-admittance**.

Compute:  $A_{OL} = \frac{i'_o}{v'_s}$

[NB: The input signal ( $v_s$  or  $i_s$ ) used in the generalised feedback analysis (to calculate  $A_{OL}$ ,  $A_f$ , etc.) **must** be the Thévenin  $v_s$  or the Norton  $i_s$ .]

Input loop:  $v_{be} = \frac{r_\pi}{R'_s + R_E + r_\pi} \cdot v'_s$

 $i'_o = \frac{r_o}{r_o + R_C + R_E} \cdot g_m v_{be} \quad [\text{NB: if } r_o \rightarrow \infty, i'_o = g_m v_{be}]$ 
 $\therefore \frac{i'_o}{v_i} = A_{OL} = \frac{g_m r_o}{(r_o + R_C + R_E)} \cdot \frac{r_\pi}{R'_s + R_E + r_\pi}$

Typically we will have  $r_o \gg R_C + R_E$  and so:

$$A_{OL} = \frac{g_m r_\pi}{R'_S + R_E + r_\pi}$$

By inspection we find the **open-loop input and output impedances** to be:

$$\begin{aligned} R_i &= R'_S + R_E + r_\pi \\ R_o &= R_C + R_E + r_o \end{aligned}$$

[N.B.: This shows why we can't assume  $r_o \rightarrow \infty$ . Otherwise,  $R_o \rightarrow \infty$ .]

Notice the definition of the output impedance (see diagram). This illustrates that the impedance found by feedback analysis often does not correspond to the impedance we are after. As we will see, an adjustment must be made to correct this. We are taking  $R_C$  in this case to be the load of the circuit. If unsure of the definitions of  $R_i$  and  $R_o$ , look at examples II A-D.

We have the open loop parameters now to find those for the closed loop. First find the **feedback factor**, this is just  $z_{12}$  which was earlier found to be:

$$\beta = z_{12} = R_E$$

This means that the **closed-loop gain** will be:

$$A_f = \frac{i_o}{v'_s} = \frac{A_{OL}}{I + \beta A_{OL}} = \frac{h_{fe} \left( \frac{r_o}{r_o + R'_S + R_E} \right)}{R'_S + r_\pi + \left( 1 + h_{fe} \cdot \frac{r_o}{r_o + R_C + R_E} \right)}$$

where  $g_m r_\pi = h_{fe}$

Again if we have  $r_o \gg R_C + R_E$

This can be simplified:

$$A_f = \frac{h_{fe}}{R'_S + r_\pi + (1 + h_{fe})R_E} \approx \frac{1}{R_E}$$

The **closed-loop input impedance** is found to be:

$$R_{if} = (1 + \beta A_{OL})R_i = R'_S + r_\pi + (1 + h_{fe})R_E$$

This however has included the source resistance, which we should subtract to get the input impedance of the amplifier.

$$\begin{aligned} R'_{if} &= R_{if} - R'_S \\ &= r_\pi + (1 + h_{fe})R_e \end{aligned}$$

The **closed-loop output impedance** is found:

$$\begin{aligned} R_{of} &= (1 + \beta A_{OL})R_o \\ &= R_C + R_E + r_o + (1 + h_{fe})R_E \end{aligned}$$

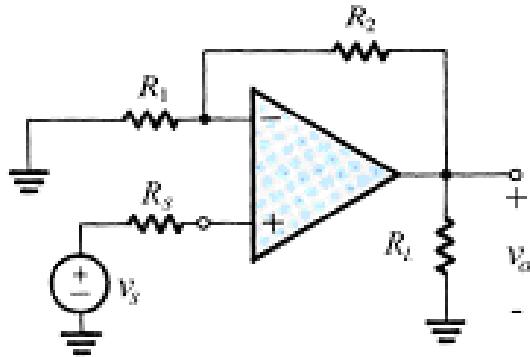
This, however, has included the effect of  $R_C$  which needs to be removed.

$$R'_{of} = R_{of} - R_C$$

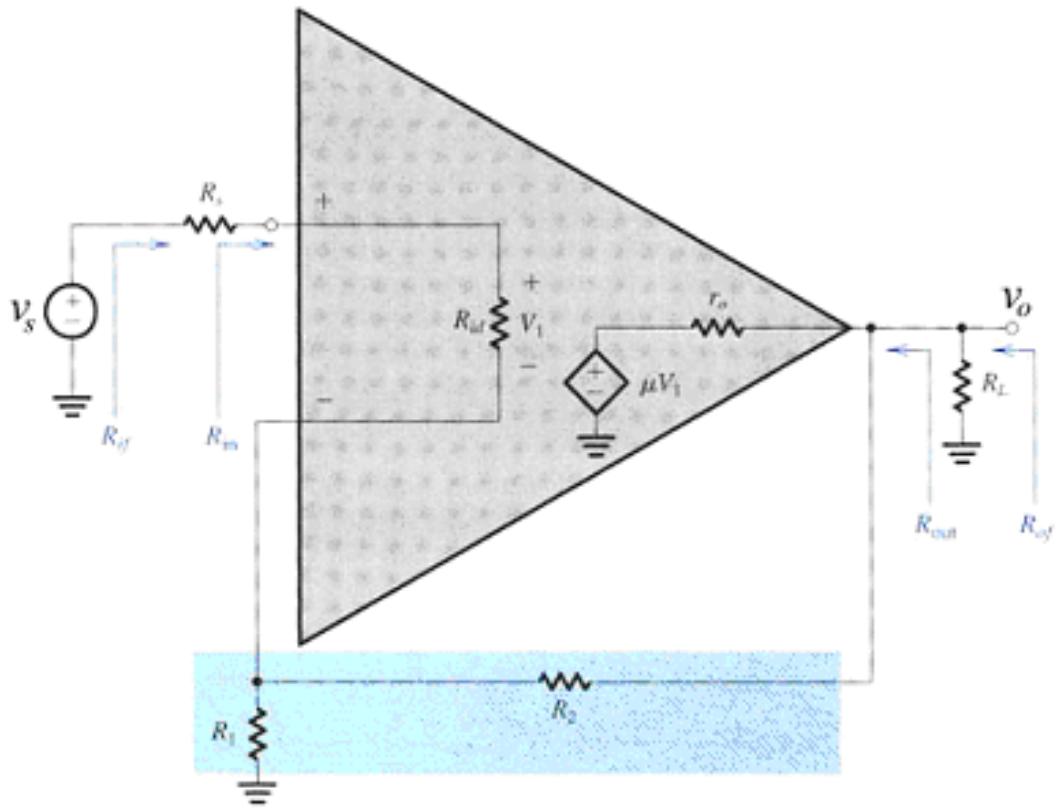
**NOTE:** Q. Should the input and output impedances from the previous example of the shunt-shunt topology be adjusted in a similar manner?

### 5.4.4 A Series-Shunt Case

Non-inverting op-amp circuit.



In determining the topology of the circuit, we shall be better served by looking at the equivalent circuit with the op-amp replaced by its circuit model.

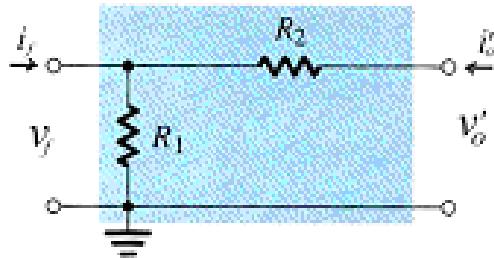


Input – we see that  $R_1$  and  $R_2$  are in series with the source voltage and is also connected to the output voltage of the op-amp  
 $\Rightarrow$  **voltage summing** – SERIES.

Output – set  $v_o = 0$ . The feedback signal through  $R_2$  becomes zero  
 $\Rightarrow$  **voltage sampling** – SHUNT.

### SERIES-SHUNT TOPOLOGY

In order to determine the loading effect of the feedback network on the basic circuit we need to use the ***h*-parameters**. The feedback network consists of  $R_1$  and  $R_2$  and is shown below.



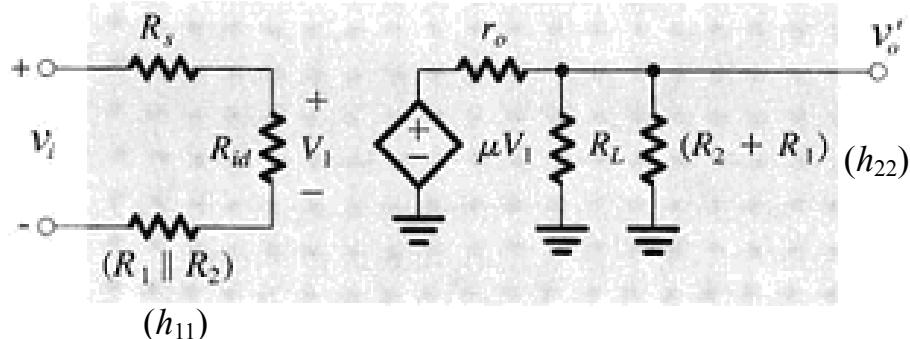
$$h_{11} = \left. \frac{v_f}{i_f} \right|_{v_o' = 0} = R_1 \| R_2$$

$$h_{22} = \left. \frac{i_o'}{v_o'} \right|_{i_f = 0} = R_1 + R_2$$

While we are at it we may as well find the feedback factor:

$$\beta = h_{12} = \left. \frac{v_f}{v_o'} \right|_{i_f = 0} = \frac{R_1}{R_1 + R_2}$$

The basic circuit can now be drawn with the loading effect of the feedback network included.



The gain of this circuit is now found.

$$V_1 = v_s \cdot \frac{R_{id}}{R_S + R_{id} + (R_1 \parallel R_2)}$$

$$v'_o = \mu V_1 \cdot \frac{R_L \parallel (R_1 + R_2)}{R_L \parallel (R_1 + R_2) + r_o}$$

(Remember  $\mu$  is dimensionless.)

So for the open loop gain we have:

$$A_{OL} = \frac{v'_o}{v_s} = \mu \cdot \frac{R_L \parallel (R_1 + R_2)}{R_L \parallel (R_1 + R_2) + r_o} \cdot \frac{R_{id}}{R_S + R_{id} + (R_1 \parallel R_2)}$$

N.B.:  $A_{OL} \rightarrow \mu$   
for  $r_o$  small  
and  $R_{id}$  large.

From the circuit we can also easily find the input and output impedances.

$$R_i = R_S + R_{id} + R_1 \parallel R_2$$

$$R_o = r_o \parallel R_L \parallel (R_1 + R_2)$$

We already have found the expression for the feedback factor and the only thing that remains is to find the expressions for the closed-loop gain and closed-loop input and output impedances. These expressions will be large and messy, but the important thing is they can be found.

[N.B.: If we assume  $A_{OL} = \mu$ , then:  $A_f = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{\mu}{1 + \beta\mu} \rightarrow \frac{1}{\beta} = \frac{R_1 + R_2}{R_1}$  for  $\mu$  large.]

We must remember that  $R_S$  is due to the signal source attached to the circuit and so the input resistance of the circuit is  $R_{if}$  less  $R_S$ .

$$R'_{if} \equiv R_{in} = R_{if} - R_S$$

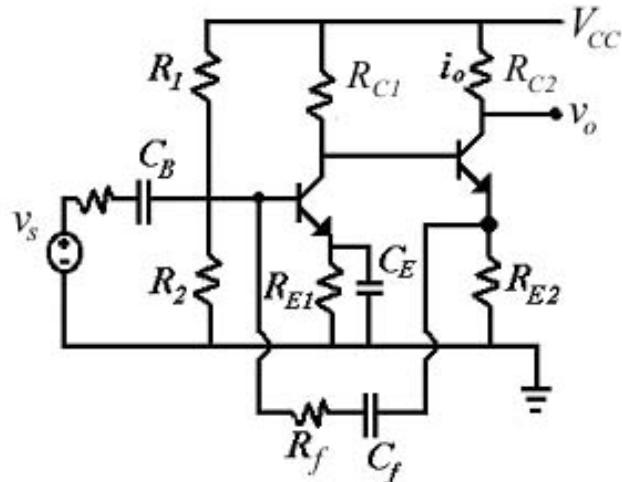
A similar situation exists for the output resistance. The output resistance of the circuit ( $R_{out}$ ) **is not** equal to  $R_{of}$ . In this case we have the load resistance  $R_L$  in parallel to the circuit's output resistance  $R_{of}$ . It follows that:

$$R_{of} = R_{out} \parallel R_L$$

So we can find  $R_{out}$ .

### 5.4.5 A Shunt-Series Case

Shunt-series pair.



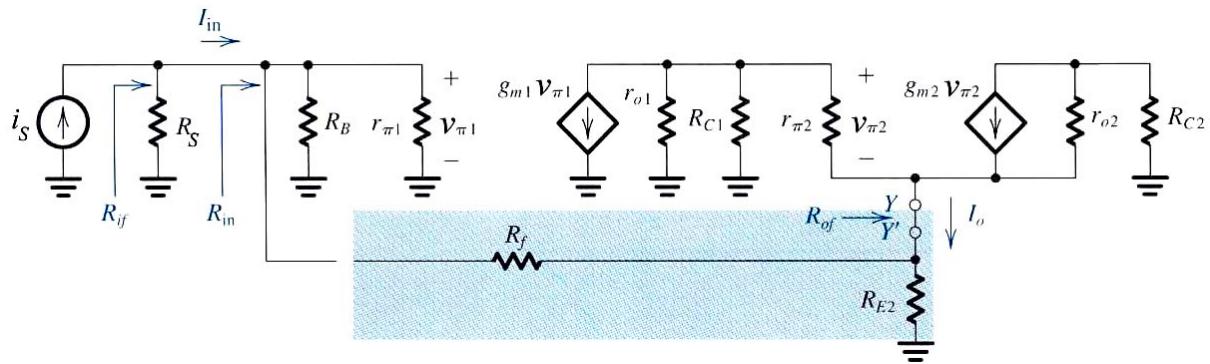
Determine the topology (assuming you can't read the above). Note firstly that the capacitors will be short-circuited for mid-band analysis.

Input – there is no element in series with the voltage source in the input loop and connected to the output. Replace by a current source,  $R_f$  is connected to the input node of the first transistor and the output circuit. Input is **current summing – SHUNT**.

Output – set  $v_o=0$ . A current will still flow through  $R_f$ . Set  $i_o=0$ . No current can flow through  $R_E$  or through  $R_f$ . The output has **current sampling - SERIES**.

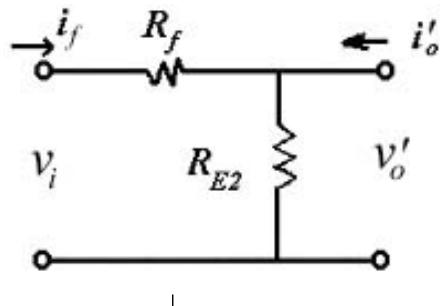
## SHUNT-SERIES TOPOLOGY

Re-draw for small-signal analysis



Where  $i_s = v_s/R_s$  and  $R_B = R_1 // R_2$ .

Now find the loading effect of the feedback network. In this case we use the **g-parameters**. The feedback network is shown below.



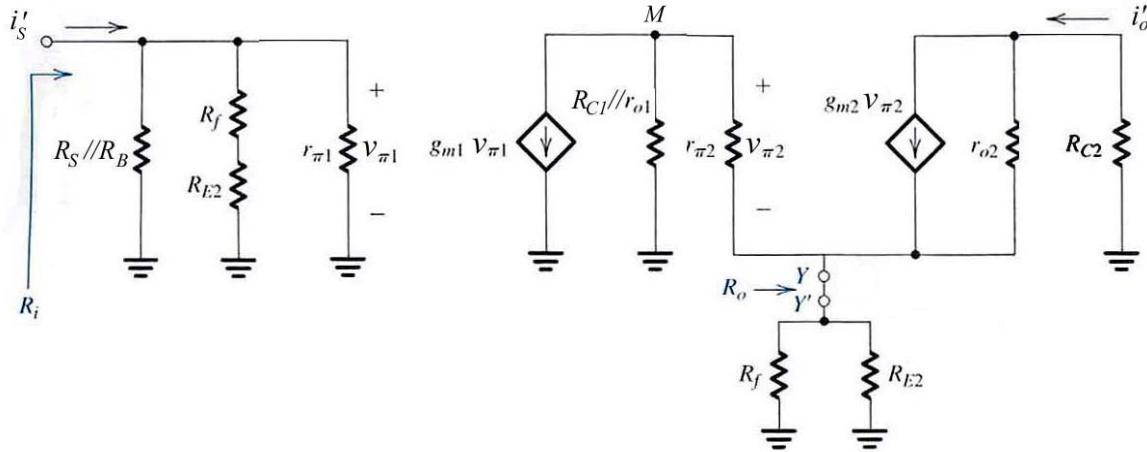
$$g_{11} = \left. \frac{i_f}{v_i} \right|_{i'_o=0} = \frac{1}{R_f + R_{E2}}$$

$$g_{22} = \left. \frac{v'_o}{i'_o} \right|_{v_i=0} = R_f \| R_{E2}$$

We'll calculate the feedback factor as well:

$$\beta = g_{12} = \left. \frac{i_f}{i'_o} \right|_{v_i=0} = -\frac{R_{E2}}{R_f + R_{E2}}$$

We can now draw the basic circuit for open loop analysis.



We can use this to find the open-loop gain, etc. In this case, the amplification is current gain and so we are trying to find:

$$A_{OL} = \frac{i'_o}{i'_s}$$

Look first at the input loop:

$$v_{pi1} = i'_s [r_{pi1} \| R_S \| R_B \| (R_f + R_{E2})] = i'_s R_i.$$

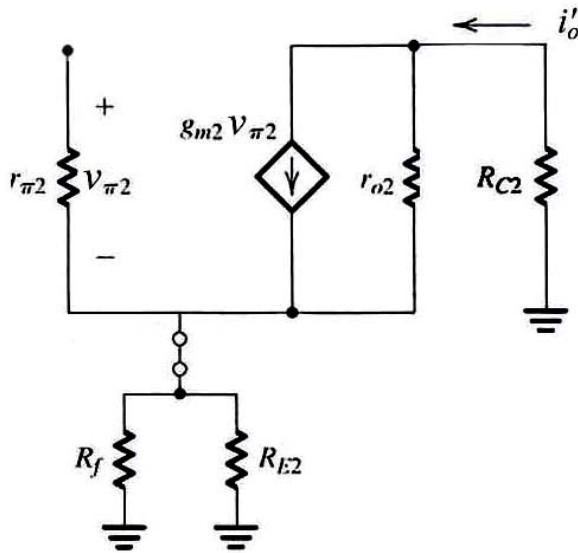
It should be noted that **the open loop input impedance is  $R_i$** .

Now look at the output loop. First find the voltage at the point marked  $M$ .

$$v_M = -g_{m1}v_{pi1} \{ r_{o1} \| R_{C1} \| [r_{\pi2} + (1 + g_{m2}r_{\pi2})(R_{E2} \| R_f)] \} = -g_{m1}v_{pi1}R_A$$

By voltage division we find:

$$v_{\pi2} = -g_{m1}v_{pi1}R_A \cdot \frac{r_{\pi2}}{r_{\pi2} + (1 + g_{m2}v_{\pi2})(R_{E2} \| R_f)}$$



Look at the output loop and sum the voltages around the loop.

$$i'_o R_{C2} + (i'_o - g_{m2}r_{\pi2})r_{o2} + \left( i'_o + \frac{v_{\pi2}}{r_{\pi2}} \right) (R_E \| R_f) = 0$$

$$i'_o = g_{m2}v_{\pi2} \cdot \frac{r_{o2} - \frac{R_E \| R_f}{g_{m2}r_{\pi2}}}{r_{o2} + R_{C2} + (R_E \| R_f)} \approx g_{m2}v_{\pi2}$$

This is because typically we have  $r_{o2} \gg R_f, R_{C2}, R_{E2}$ . We can now write an expression for the **open-loop gain**.

$$A_{OL} = -g_{m1}g_{m2}R_i R_A \cdot \frac{r_{\pi2}}{r_{\pi2} + (1 + \beta_2)(R_E \| R_f)}$$

As mentioned earlier, the open loop input impedance is equal to  $R_i$ , defined previously. It remains to **find the output impedance**.

Find the resistance seen by a **test signal applied to the output terminal with  $i'_s = 0$** . This implies that  $v_{\pi1} = 0$  and only the circuit to the right of the first current source need be considered. The circuit to be analysed is shown below.

$$v_T = i_T R_{C2} + (i_T - g_{m2} v_{\pi2}) r_{o2} + i_T [R_f \| R_{E2} \|(r_{\pi2} + r_{o1} \| R_{C1})]$$

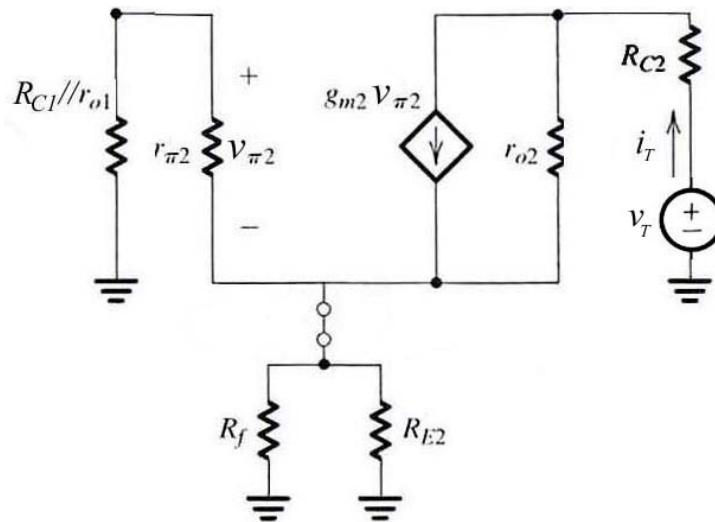
$$v_{\pi2} = - \frac{r_{\pi2}}{r_{\pi2} + r_{o1} \| R_{C1}} \cdot [R_f \| R_{E2} \|(r_{\pi2} + r_{o1} \| R_{C1})]$$

$$R_o = \frac{v_T}{i_T} = R_{C2} + r_{o2} + \left\{ 1 + \frac{g_{m2} r_{o2} r_{\pi2}}{r_{\pi2} + (r_{o1} \| R_{C1})} \right\} [R_f \| R_{E2} \|(r_{\pi2} + r_{o1} \| R_{C1})]$$

We won't find the closed-loop expressions in all their glory but remark on how to calculate them. Since the topology is shunt-series the expressions used are:

$$A_f = \frac{A_{OL}}{1 + \beta A_{OL}}$$

$$R_{if} = \frac{R_i}{1 + \beta A_{OL}}, R_{of} = R_o (1 + \beta A_{OL})$$



Circuit for finding the open loop  $R_o$

For the **input resistance**, the input is current summing and we have a current source as the applied signal. In order to remove the effect of the source resistance we note that:

$$R_{if} = R'_{if} \| R_S$$

where  $R'_{if}$  is the input impedance of the amplifier.

The output is current sampling so in this case the load  $R_{C2}$  is series connected and so the **output impedance** is:

$$R'_{\text{of}} = R_{\text{of}} - R_{C2}$$

### 5.4.6 Hints & Summary

The following are hints for determining the feedback topology of a feedback circuit with transistor/s present. They are included only as a guide and do not constitute a solution – you must justify all answers in an exam/assignment.

- Locate the feedback element – it is typically a resistor, sometimes with a capacitor in series (why?). It is usually imaginatively named as  $R_f$ .
- Locate where the **input** end of the element is. If it is **connected to the emitter/source** then it is probably **SERIES**. If it is **connected to the base/gate** then it is probably **SHUNT**.
- Locate the **output** end of the element. If it is **connected to the emitter/source** of the output transistor then it is probably **SERIES**. If it is **connected to the collector/drain** then it is probably **SHUNT**.

**Important:** check by the method outlined in Section 4.2.5.

On the following page is a summary of the effect of feedback on the properties of a circuit. Note that the feedback always improves the performance of the circuit.

## Summary of Feedback Amplifier Properties

<u>Topology</u>	<u>Amplifier Type</u>	<u>Sum Signal (i/p)</u>	<u>Sample Signal (o/p)</u>	<u><math>Z_{if}</math></u>	<u><math>Z_{of}</math></u>
Shunt-Shunt	current-voltage	current	voltage	Low $Z_{if} = Z_i/(1+\beta A_o)$	Low
Shunt-Series	current-current	current	current	Low $Z_{of} = Z_o(1+\beta A_o)$	High
Series-Series	voltage-current	voltage	current	High $Z_{if} = Z_i(1+\beta A_o)$	High
Series-Shunt	voltage-voltage	voltage	voltage	High $Z_{of} = Z_o/(1+\beta A_o)$	Low

---

- If Amplifying  $I$ , want low  $Z_i$   
 $V$ , want high  $Z_i$
- If output is  $I$ , want high  $Z_o$  – see current source  
 $V$ , want low  $Z_o$  – see voltage source

# **SECTION 6: FEEDBACK STABILITY & COMPENSATION**

## **6.1 Introduction**

## **6.2 Effect of Feedback on Amplifier Poles**

- 6.2.1 Single Pole System**
- 6.2.2 Two Pole System**
- 6.2.3 Three Pole System**

## **6.3 Stability Criteria**

- 6.3.1 Nyquist Criterion**
- 6.3.2 The Gain & Phase Margins**

## **6.4 Frequency Compensation**

- 6.4.1 Dominant Pole Compensation**
- 6.4.2 Compensation**
- 6.4.3 Gain-Bandwidth Product**
- 6.4.4 Slew Rate**

### **Aims:**

After this section the student should know:

- The origin of frequency instability in circuits.
- The role of feedback in the frequency stability of circuits.
- The meaning and importance of the gain and phase margins.
- Common methods of frequency compensation and their principle of operation.

## 6.1 Introduction

In the previous section, negative feedback was used to improve the performance of amplifier circuits. But what happens if the feedback ceases to be negative and becomes positive?

Imagine some transient disturbance to the circuit, say  $X_o$ : if the feedback is negative the amplified output will quickly die away after the initial pulse. If, however, the feedback is positive some of the amplified output is fed back to the input. If this portion of the signal,  $TX_o = -\beta AX_o$ , is equal to  $X_o$  then the output has regenerated itself – not a good thing! Another way to look at it is if  $T = -1$ , the amplifier oscillates.

This raises one important aspect of the behaviour of feedback circuits that was not covered earlier and that is **stability**. What do we mean by stability?

For our example above, this means that if a transient disturbance of finite duration is applied, the output dies out when the amplifier is stable. If the amplifier is unstable, the output persists indefinitely or increases until non-linearities limit the output.

Mathematically, *a system is stable if and only if all bounded input signals produce bounded output signals*.

The question remains; why would the feedback go from being negative to being positive? The answer lies in the phase difference between input and output. As has already been seen, the presence of capacitors in a circuit has an influence on the phase-shift produced by a circuit. Imagine a circuit where the output is  $180^\circ$  out of phase with the input, i.e., the feedback is negative (convince yourself of this). If the presence of capacitors sees the phase of the output shift by another  $180^\circ$ , then the feedback signal is  $360^\circ$  out of phase with the input – it is now in phase and we have positive feedback.

The issue of keeping a circuit stable can be summarised:

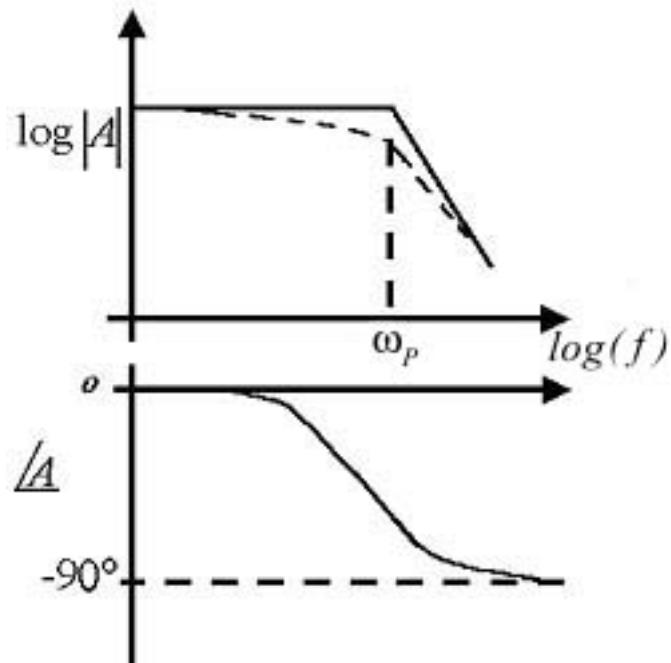
**AIM:** To keep the feedback negative over the frequency range where the loop gain  $\geq 1$

**PROBLEM:** Phase shifts in practical amplifier.

## 6.2 Effect of Feedback on Amplifier Poles

### 6.2.1 Single pole system:

$$A_0(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_p}}$$
$$\Rightarrow A_f(\omega) = \frac{A_0 / (1 - \beta A_0)}{1 + \frac{j\omega}{(1 - \beta A_0)\omega_0}}$$



This amplifier is **unconditionally stable** since the phase shift is at most 90°.

## 6.2.2 Two pole system

$$A_0(\omega) = \frac{A_0}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)}$$

$$A_f(s) = \frac{A_0/(1+\beta A_0)}{1 + \frac{s}{1+\beta A_0} \left( \frac{1}{\omega_1} + \frac{1}{\omega_2} \right) + \left( \frac{s^2}{(1+\beta A_0)\omega_1\omega_2} \right)}$$

$$= \frac{A_{f0}}{1 + \left( \frac{s}{\omega_0} \right) \left( \frac{1}{Q} \right) + \left( \frac{s}{\omega_0} \right)^2}$$

where  $\omega_0 = \sqrt{\omega_1\omega_2(1+\beta A_0)}$ ;  $Q \equiv \frac{\omega_0}{\omega_1 + \omega_2}$

Poles of  $A_f(s)$  are given by:

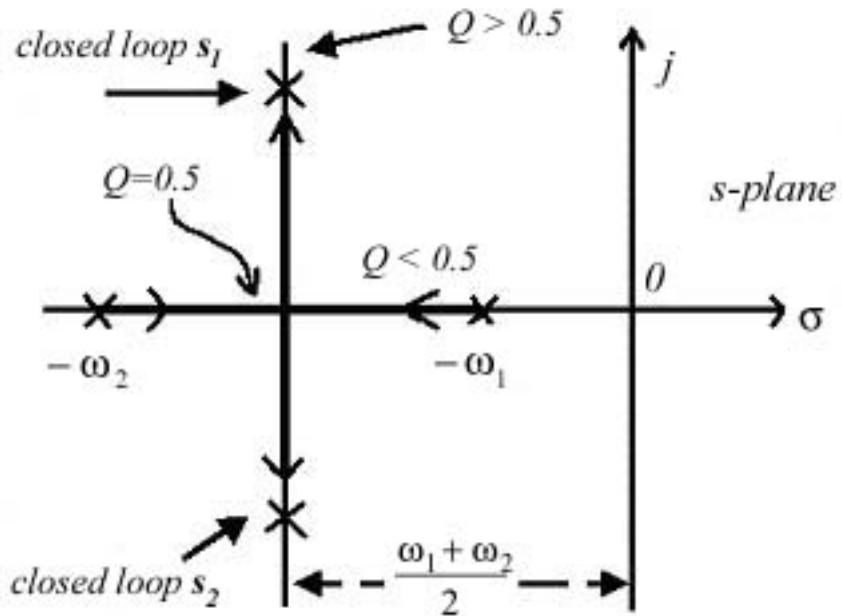
$$\frac{s}{\omega_0} = -\frac{1}{2Q} \pm \frac{1}{2Q} \sqrt{1 - 4Q^2}$$

$$\Rightarrow s = -\frac{\omega_1 + \omega_2}{2} \pm \frac{\omega_1 + \omega_2}{2} \sqrt{1 - 4Q^2}$$

note:

(i) if  $\beta \Rightarrow 0$ ,  $s \rightarrow \omega_1$  and  $\omega_2$  i.e., no feedback

(ii) As  $|\beta A_0|$  is increased, the root-locus plot of the poles is shown below.



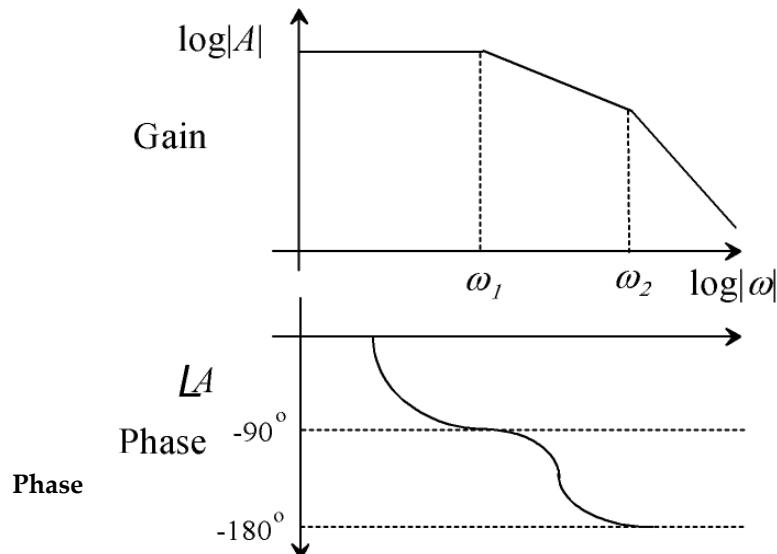
Frequency response:

$$\text{Let } K = \frac{1}{2Q}, \text{ then}$$

$$\left| \frac{A_f}{A_{f0}} \right| = \frac{1}{\sqrt{\left( 1 - \left( \frac{\omega}{\omega_0} \right)^2 \right)^2 + 4K^2 \left( \frac{\omega}{\omega_0} \right)^2}}$$

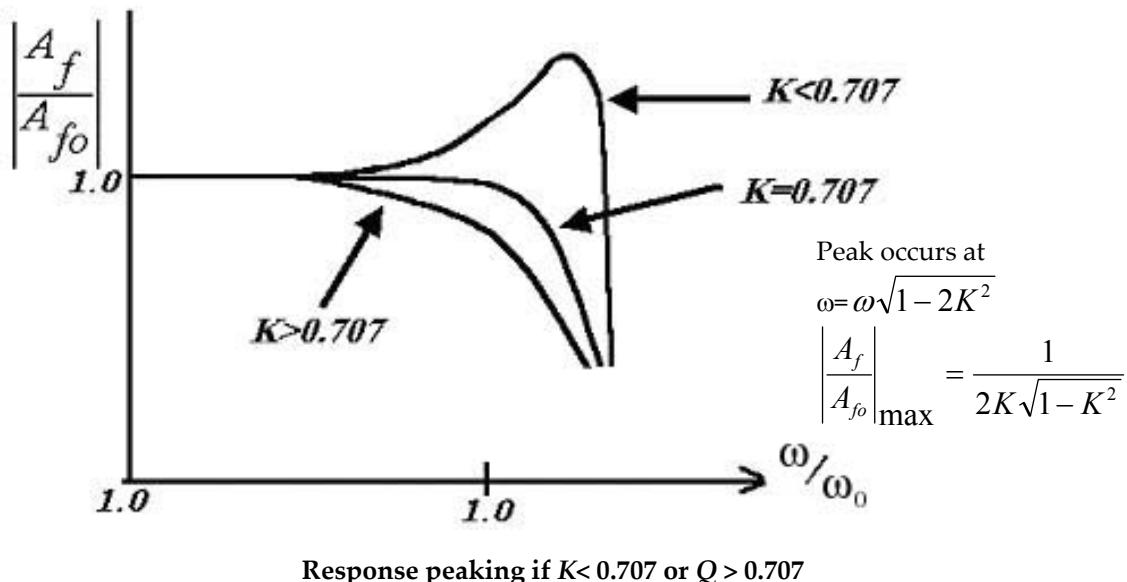
$$\angle \frac{A_f}{A_{f0}} = -\tan^{-1} \left[ \frac{2K \left( \frac{\omega}{\omega_0} \right)}{1 - \left( \frac{\omega}{\omega_0} \right)^2} \right]$$

**Regardless of how much negative feedback is employed, a two-pole amplifier remains stable – poles remain in the left-hand side of the s-plane.** If  $\beta A_o$  is too large, response of the amplifier may be unsatisfactory.



The phase shift tends asymptotically towards  $-180^\circ$ . Thus, in the limit of infinite  $\omega$  the feedback will be positive, but this is not damaging since the gain will be zero then.

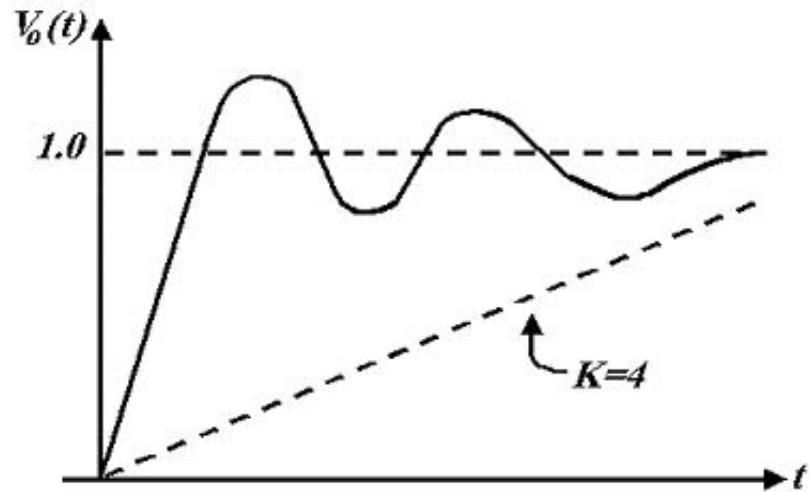
However, a high enough loop gain can give a **resonance**:



$$\begin{aligned}
 A_f(\omega) &= \frac{A_0(\omega)}{1 + \beta A_0(\omega)} = \frac{A_0}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right) - \beta A_0} \\
 &= \frac{A_0 \omega_1 \omega_2}{(j\omega)^2 + j\omega(\omega_1 + \omega_2) + \omega_1 \omega_2 (1 - \beta A_0)}
 \end{aligned}$$

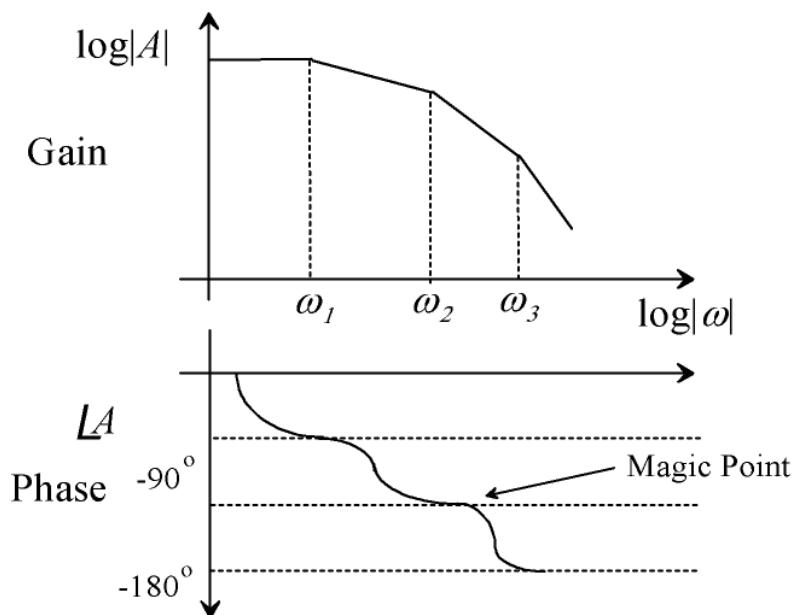
with  $s = j\omega$ , we have the standard response of a damped tuned circuit to a transient input.

## Step Response



Step response of a two-pole feedback amplifier for  $K = 0.3$ .

### 6.2.3 Three Pole System

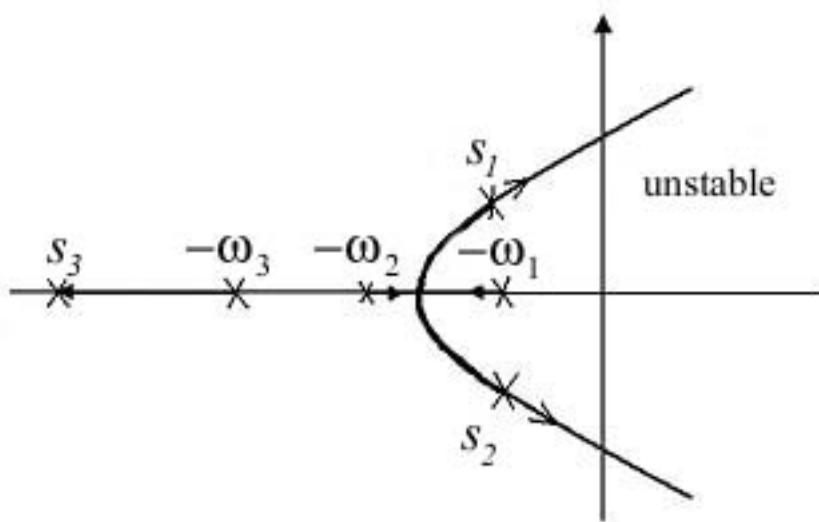


**Magic point!** Here the phase of the signals is opposite to that in the mid band region. Hence the feedback is no longer negative.

Positive feedback can give not only a **poor transient response** (as with 2 poles) but also actual **oscillations**.

$$A_f(s) = \frac{A_{f0}}{1 + \frac{s}{1-\beta A_0} \left( \frac{1}{\omega_1} + \frac{1}{\omega_2} + \frac{1}{\omega_3} \right) + \frac{s^2}{1-\beta A_0} \left( \frac{1}{\omega_1 \omega_2} + \frac{1}{\omega_1 \omega_3} + \frac{1}{\omega_2 \omega_3} \right) + \frac{s^3}{(1-\beta A_0) \omega_1 \omega_2 \omega_3}}$$

Root locus plot of poles as  $\beta A_o \rightarrow \infty$ .



Note: increasing  $\beta A_o$ , 2 of the poles into the right half plane causing the amplifier to be **unstable**.

## 6.3 Stability Criteria

Negative feedback  $\rightarrow T > 0$

Positive feedback  $\rightarrow T < 0$

If  $T = -1 \Rightarrow A_f \rightarrow \infty$  the **amplifier oscillates.**

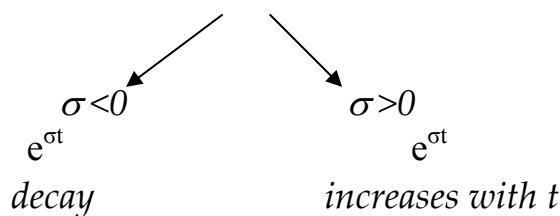
Feedback in amplifiers is almost always negative.

In designing a feedback amplifier, it must be ascertained that the circuit is **stable at all frequencies.**

The system is **stable** if a **transient disturbance of finite duration results in a response which dies out.**

Stability depends on the location of the poles of the transfer function of the circuit. I.e.. **the poles must reside on the open left half of the complex-frequency s-plane.**

$$s = \sigma + j\omega$$



Consider the closed loop gain:

$$A_F(s) = \frac{A_0(s)}{1 + T(s)}$$

where we assume that the feedback factor  $\beta$  is independent of frequency.

The poles of  $A_0(s)$  are the same as those of  $T(s)$ , if the feedback network is frequency independent.

The poles of  $A_0(s)$  that are not common to  $T(s)$  and the zeros of  $1 + T(s)$ .

For the closed loop amplifier to be stable, all the poles of  $A_f(s)$  must reside on the left hand side of the s-plane.

Assuming that the open loop amplifier is stable, (i.e., poles of  $A_0(s)$  are on the LHS of the s-plane) the “zeros of  $1 + T(s)$  must reside on the LHS of the s-plane” for  $A_f(s)$  to be stable.

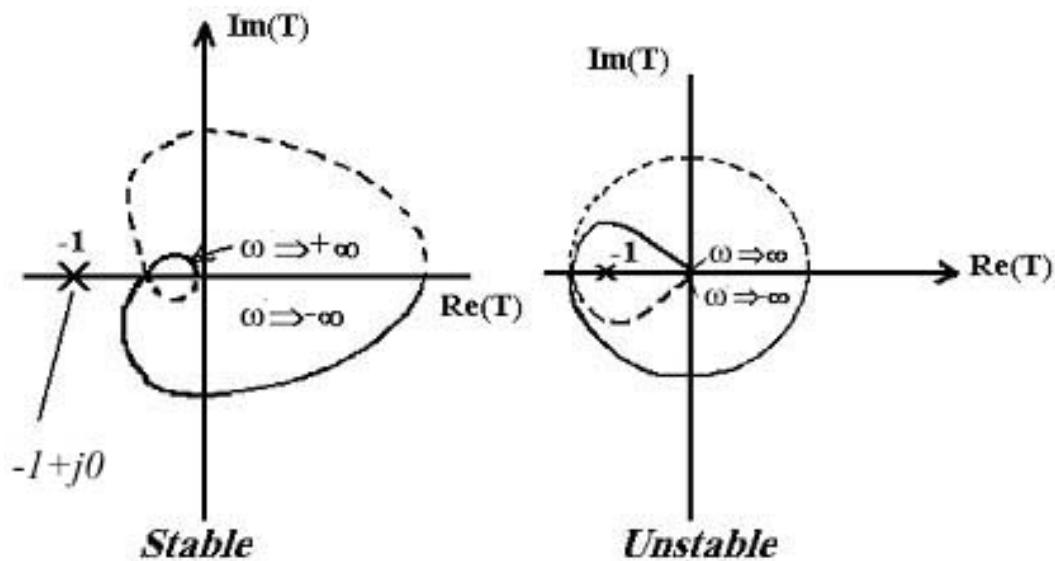
### 6.3.1 Nyquist Criterion

Nyquist plot is a graphical construction of:

$$T(s) = T(j\omega) = |T(j\omega)| \angle \theta(j\omega)$$

in polar co-ordinates.

Note: because the coefficient of  $T$  are real,  $T(-j\omega) = t^\Phi(j\omega)$

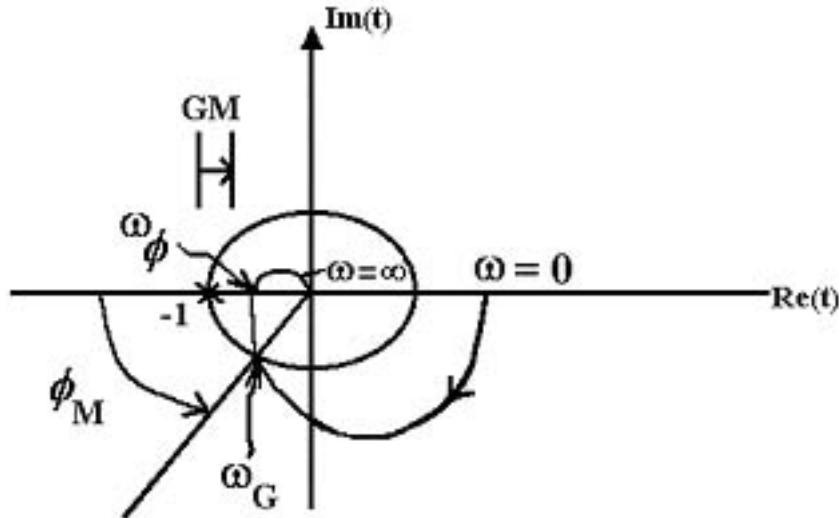


$A_f(s)$  is stable if the Nyquist plot does **not** encircle the point  $(-1, 0)$ , i.e. the radius vector from  $(-1 + j0)$  to the Nyquist plot does not rotate by  $360^\circ$ , then **no** encirclement occurs.

The Nyquist criterion states that the **number of clockwise encirclements of  $(-1 + j0)$  equals the difference between the number of zeros and the number of poles of  $F(s) = 1 + T(s)$ .**

### 6.3.2 The Gain & Phase Margins

Draw a unit circle corresponding to  $|T(j\omega)| = 1$  on the Nyquist plot.



- 1)  $\omega_G \equiv$  frequency at which the Nyquist plot intersect the unit circle.

gain cross over angular frequency where:

$$|T| < 1 \text{ when } \omega > \omega_G$$

$$|T| > 1 \text{ when } \omega < \omega_G$$

Phase margin  $\phi_M$  is defined as:

$$\phi_M = \angle T(j\omega_G) + 180^\circ$$

For the stable system, illustrated above,  $\phi_M > 0$

For an unstable system  $\phi_M < 0$

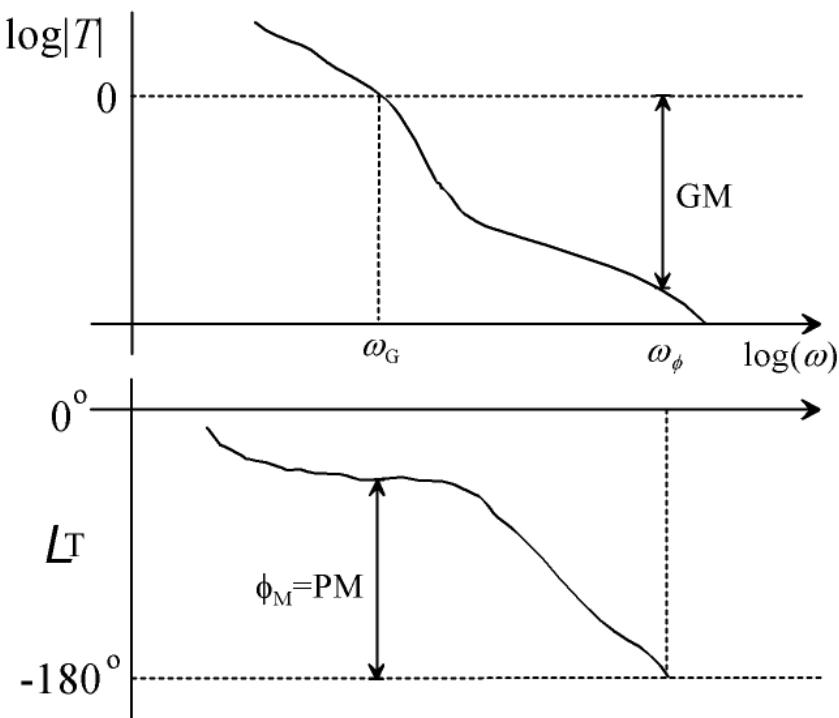
- 2)  $\omega_\phi \equiv$  phase crossover frequency, where at that frequency, the Nyquist plot crosses the negative real axis where  $\angle T(j\omega_\phi) = -180^\circ$ .

$$GM = -20 \log |T(j\omega_\phi)|$$

For a stable system  $|T(j\omega)| < 1 \rightarrow$  hence  $GM > 0$

(for an unstable system,  $GM < 0$ )

## Bode Diagram Representation



Phase margin  $\phi_M$  indicates how far  $\angle T$  is away from  $-180^\circ$  when  $|T|=1$ .

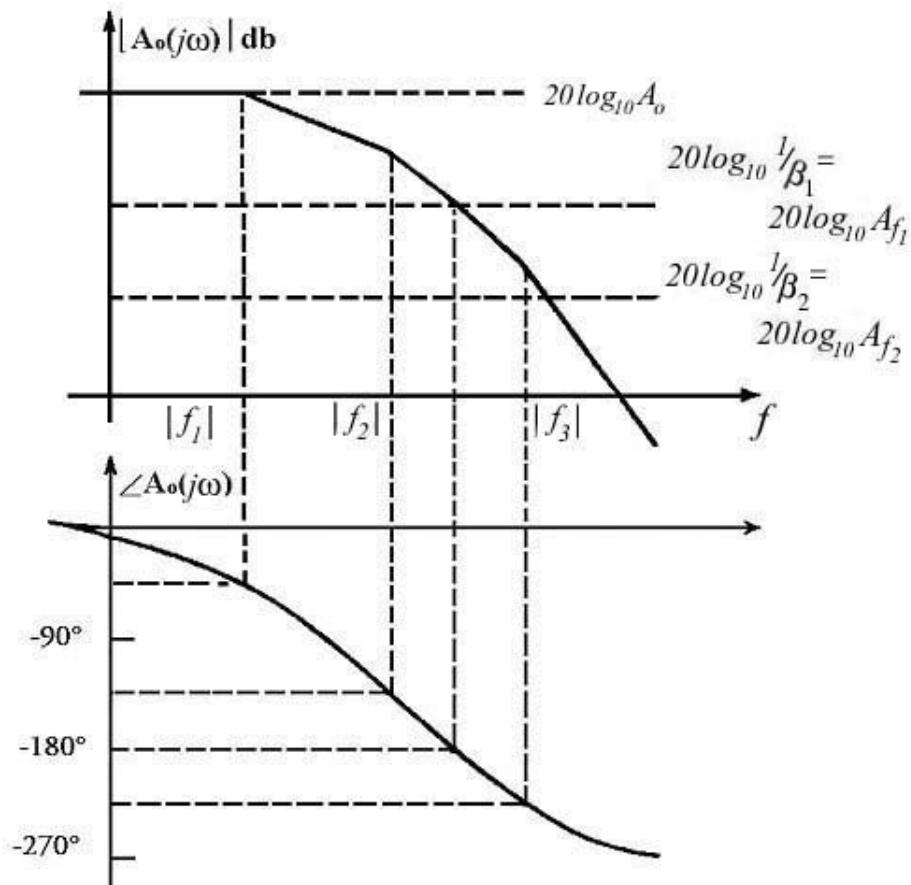
Gain margin  $GM$  indicates how far  $|T|$  is below 1 when  $\angle T = -180^\circ$ .

For good stability  $\omega_G < \omega_\phi$

## 6.4 Frequency Compensation

The purpose of compensation is to reshape the magnitude and phase response  $T(s)$  in such a way that  $|T| < 1$  when  $\angle T = 180^\circ$ .

Consider an amplifier whose gain phase relationship corresponds to that below:



Assume the open loop gain is large enough so that  $A_f = 1/\beta$ .

Choose  $\beta_1$  such that the phase margin is zero. Now increase the amount of feedback to  $\beta_2$ . The phase margin will now be negative and the circuit will oscillate.

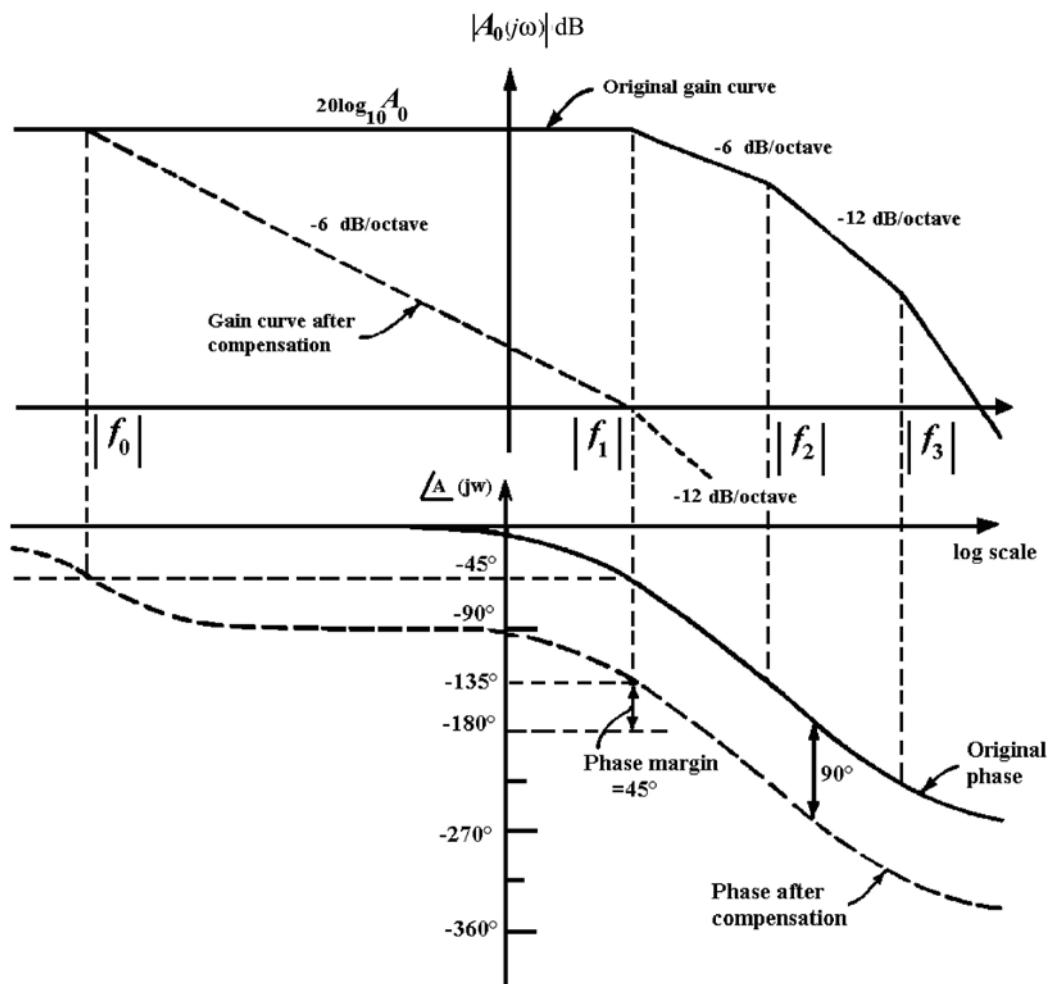
If we are going to use this amplifier in a feedback loop with a loop gain  $> \beta_1$  we must make the phase margin greater –we must compensate the amplifier.

### 6.4.1 Dominant Pole Compensation

Sometimes referred to as 'narrow banding'.

A dominant pole is deliberately introduced into the open-loop amplifier to force the phase margin to be  $< -180^\circ$  when the loop gain is 1.

Consider the case for unity gain feedback ( $\beta = 1$ ). In this case, the loop gain curve is identical to the open-loop gain curve of the amplifier.



To compensate the amplifier we introduce a new dominant pole at a frequency  $f_D$  (assume that in the process of doing so, it does not alter  $f_1, f_2$  and  $f_3$ - not always the case).

If  $f_D$  is chosen so that  $A_0(j\omega)$  is unity at frequency  $f_1$ , then the loop gain  $T$  is also unity at  $f_1$  for the assumed case of unity feedback with  $\beta = 1$ .

Note that the phase margin is  $45^\circ$  and the amplifier is stable, whereas the original amplifier (without compensation) would have been unstable.

### **drawbacks of dominant pole compensation**

1. Significant reduction in the unity-gain bandwidth from  $>f_3$  to  $f_1$ .
2. With feedback applied, the loop gain now begins to decrease at a frequency  $f_0$  and all the benefits of feedback diminishes as the loop gain increases.

Example: Feedback employing shunt-topology we have

$Z = \frac{Z_0}{1 + T(jw)}$  this will increase with frequency and so can appear inductive.

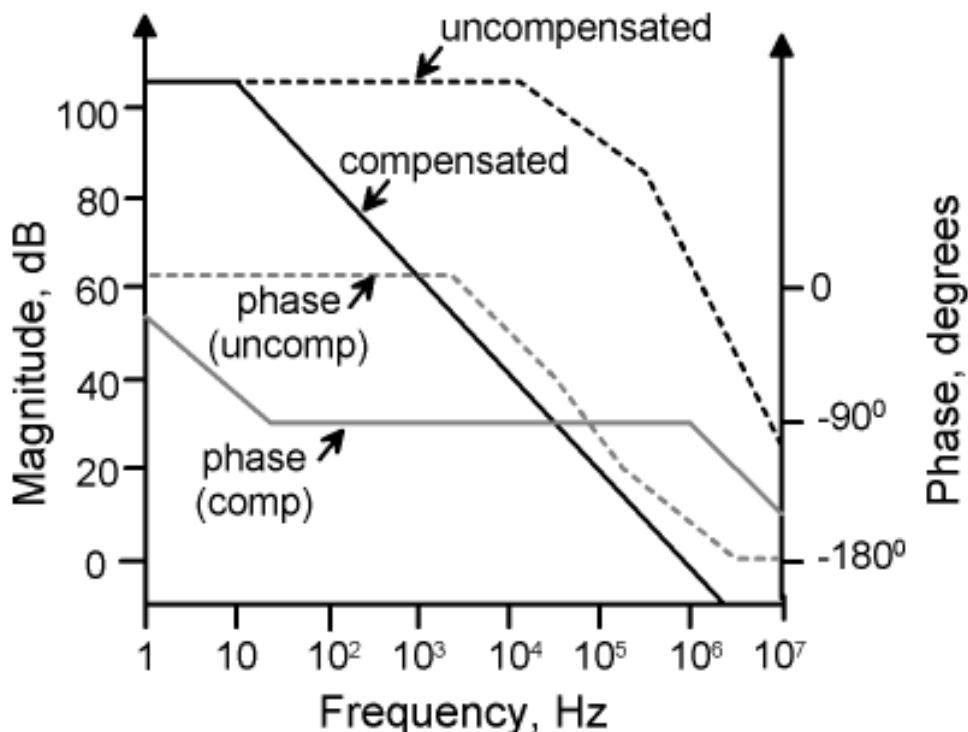
## 6.4.2 Compensation

To ensure stable operation most op-amps have internal compensation.

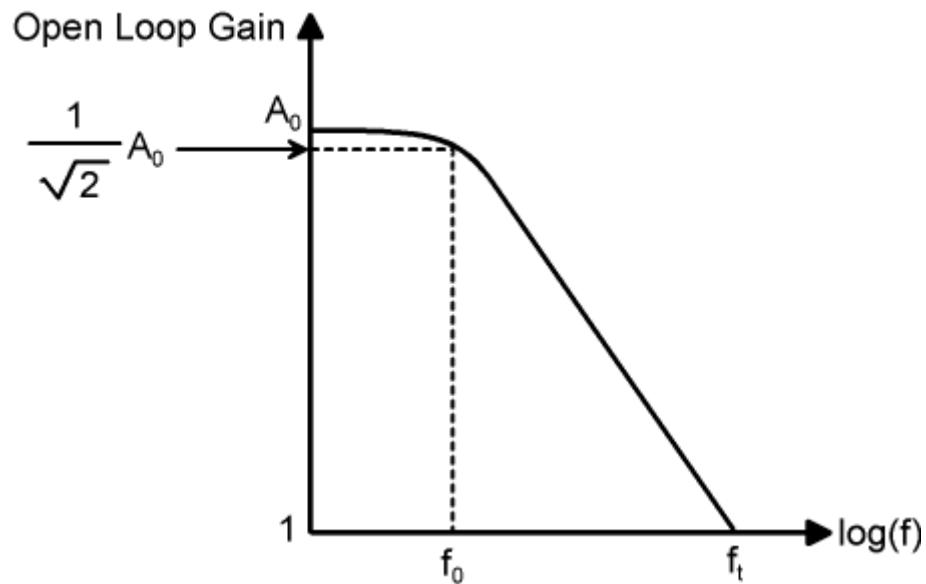
It causes the open loop gain to **roll-off at 20 dB/dec**, with a much lower corner frequency, over several decades – such that the **non-dominant pole is shifted far away**.

It also causes a **phase margin of 90%** to be achieved.

See the schematic of 741. The capacitor across the gain stage employs **Miller-effect compensation**.



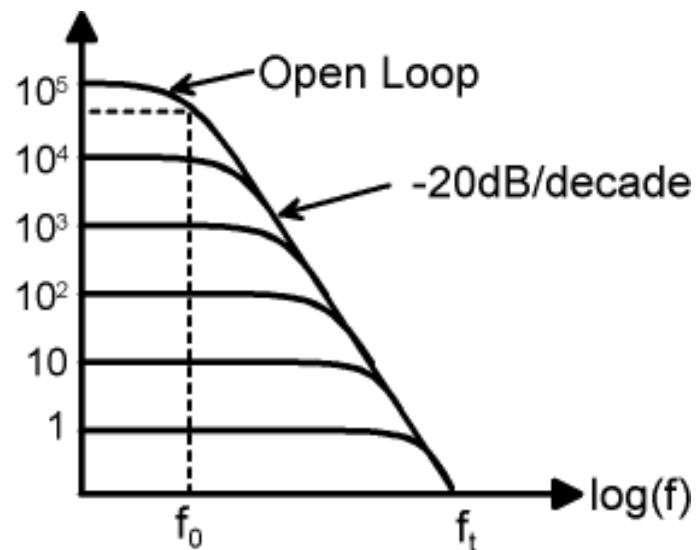
### 6.4.3 Gain Bandwidth Product



When the amplifier gain falls to 1, at frequency,  $f_t$ , it equals the product of the cut-off frequency,  $f_o$ , and the low frequency gain  $A_0$ :

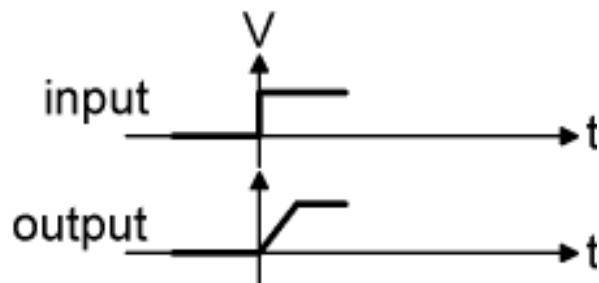
$$f_t = A_o f_o$$

Closed loop bandwidth is given approximately by  $BW_{CL} = f_t \beta$  where  $\beta$  is the feedback ratio.



#### 6.4.4 Slew Rate

The time rate of change of the closed-loop amplifier output voltage under large-signal conditions – the maximum possible rate at which an amplifier output voltage can change, in V/sec



For a sinusoidal input  $V_{in} = K \sin(\omega t)$ , the maximum rate of change of input signal is  $K\omega$  V/sec.

If  $S$  is the specified slew rate

$$\text{Then } K\omega < S \rightarrow \omega < \frac{S}{K}$$

$$\text{maximum frequency is: } f_s = \frac{S}{2\pi K}$$

The cause of slew-rate limitation is the presence of the compensation capacitor.

# **SECTION 7: Non-Linear Circuits**

## **7.1 Oscillator Circuits**

### **7.1.1 Introduction – Conditions for Oscillation**

### **7.1.2 Op-Based Oscillator: The Wein Bridge Oscillator**

## **7.2 Schmitt Trigger**

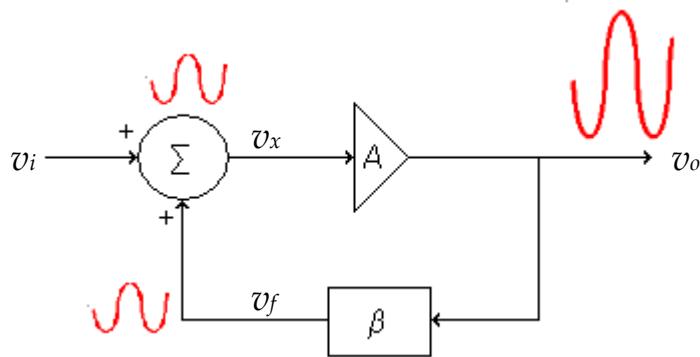
### **Aims**

After this section the student should know:

- Basic conditions for oscillator circuits
- Principles of the Wein-Bridge Oscillator
- Behaviour and analysis of the Schmitt trigger Bistable circuit

## 7.1 Oscillator Circuits

### 7.1.1 Introduction – Conditions for Oscillation



Recall that Loop  
Gain:  $T = -\beta A_o$

Consider the case where  $v_i = 0$  then

$$v_x = v_f = \beta v_o = \beta A_o v_x$$

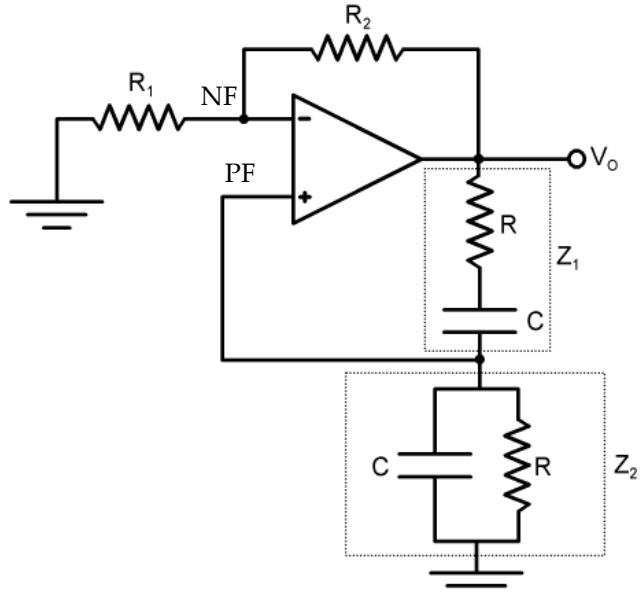
Thus  $v_x = (\beta A_o) v_x$

This equation has two solutions

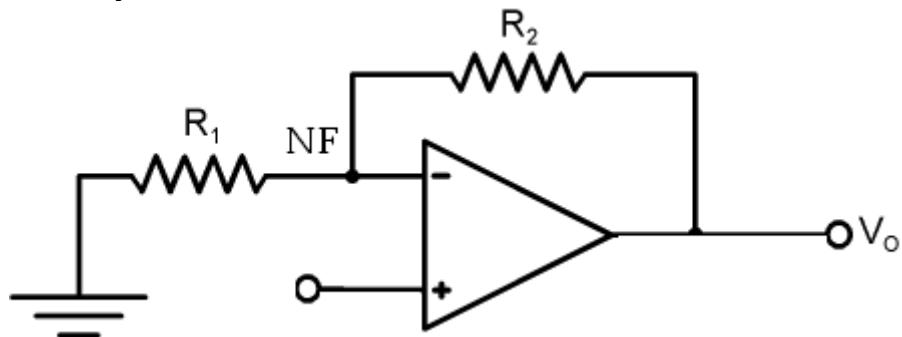
- 1) Trivial Solution:  $v_x = 0$
- 2)  $\beta A_o = 1$  (i.e.  $T = -1$ );  $v_x$  is undefined and the oscillations are self sustaining.

This is the **Barkhausen Criterion**:  $T(j\omega) = -1$ . When the Barkhausen criterion is satisfied, self sustaining

### 7.1.2 The Wein-Bridge Oscillator



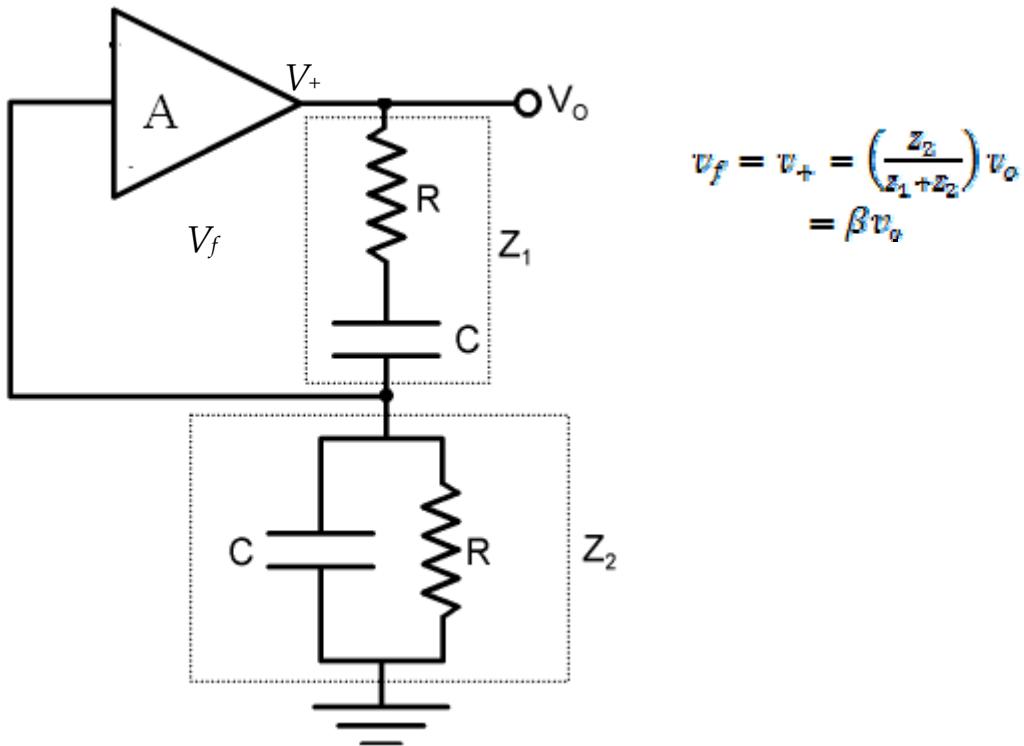
Consider first the non-inverting amplifier component (negative feedback only).



The gain of this amplifier is:

$$A = \frac{v_o}{v_+} = \frac{R_1 + R_2}{R_1} = \left(1 + \frac{R_2}{R_1}\right)$$

Now consider the positive feedback signal provided by the RC network.



So the loop gain is

$T \equiv -\beta A_o = -\left(1 + \frac{R_2}{R_1}\right)\left(\frac{Z_2}{Z_1 + Z_2}\right)$ , by the Barkhausen criterion, we require  $T = -1$ .

Loop gain is given by

$$T = -\left(1 + \frac{R_2}{R_1}\right) \frac{Z_2}{Z_1 + Z_2}$$

where  $Z_2 = R \parallel \frac{1}{j\omega C}$  and  $Z_1 = R + \frac{1}{j\omega C}$

Now

$$\begin{aligned}\frac{Z_2}{Z_1 + Z_2} &= \frac{\frac{R}{(1+j\omega RC)}}{R + \frac{1}{j\omega C} + \frac{R}{1+j\omega RC}} \\ &= \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)} \\ \therefore T &= \frac{-\left(1 + \frac{R_2}{R_1}\right)}{3 + j\left(\omega_o RC - \frac{1}{\omega_o RC}\right)} = -1\end{aligned}$$

For  $T$  to be real.

$$\omega_o RC - \frac{1}{\omega_o RC} = 0 \rightarrow \omega_o = \frac{1}{RC}$$

$$\text{and } 1 + \frac{R_2}{R_1} = 3 \Rightarrow \frac{R_2}{R_1} = 2$$

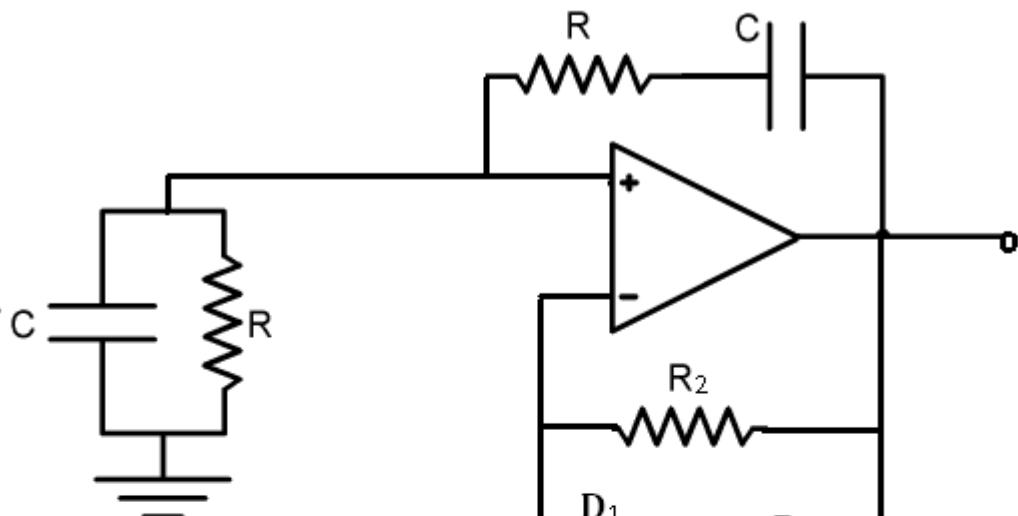
$$\text{In practice: Set } 1 + \frac{R_2}{R_1} \cong 3.1$$

$C$  — 2 gauged capacitors for varying frequency.

$R$  — Range setting.

Max. frequency of oscillation limited by slew rate of op-amp.

## Amplitude Stabilization Schemes



If  $|T| \geq 1$ , oscillations increase

- Saturation
- Non-linearity
- Distortion (harmonics)

Need to *stabilise* amplitude below saturation

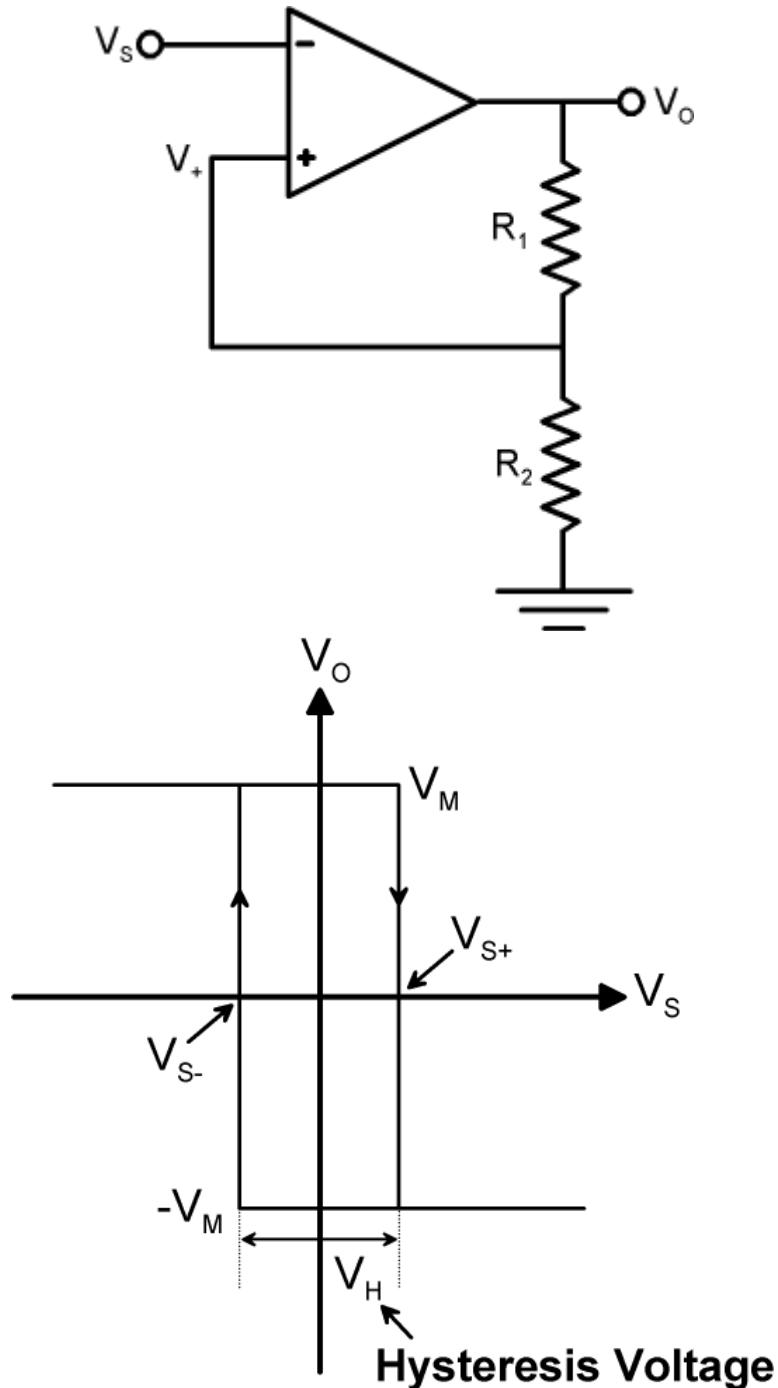
$$\text{During oscillation: } v_+ = \frac{1}{3}v_o = v_-.$$

Consider  $v_o$  going through the +ve cycle. Diode  $D_1$  will not conduct by diode  $D_2$  will conduct under certain conditions. When  $D_2$  conducts,  $R_A$  is shunted across  $R_2$  which reduces the gain of amplifier and limits the output voltage.

## 7.2 The Schmitt Trigger (Bistable)

(Inverting)

Uses positive feedback around op-amp or comparator



## Analysis

$$v_+ = \frac{R_2}{R_1 + R_2} v_o$$

(i) If  $v_s < v_+ \rightarrow v_o = +V_m \Rightarrow v_+ = \frac{R_2}{R_1 + R_2} V_m$

As  $v_s$  increases, nothing happens until it passes  $\frac{R_2}{R_1 + R_2} V_m$ ,

denote by  $V_{S+}$ , when  $v_s$  exceeds  $V_{S+}$ ,  $v_+$  becomes  $-\frac{R_2}{R_1 + R_2} V_m$ .

(ii) consider the situation when  $v_s > v_+$  and decreasing then  $v_o = -V_m$

$$v_+ = -\frac{R_2}{R_1 + R_2} V_m$$

when  $v_s$  crosses  $v_+ = V_{S-} = -\frac{R_2}{R_1 + R_2} V_m$

$v_o$  changes to  $+V_m$ .

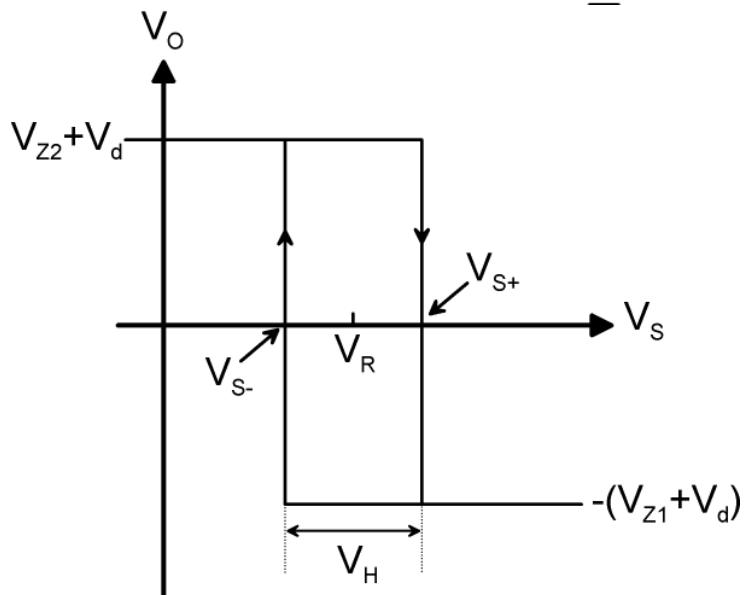
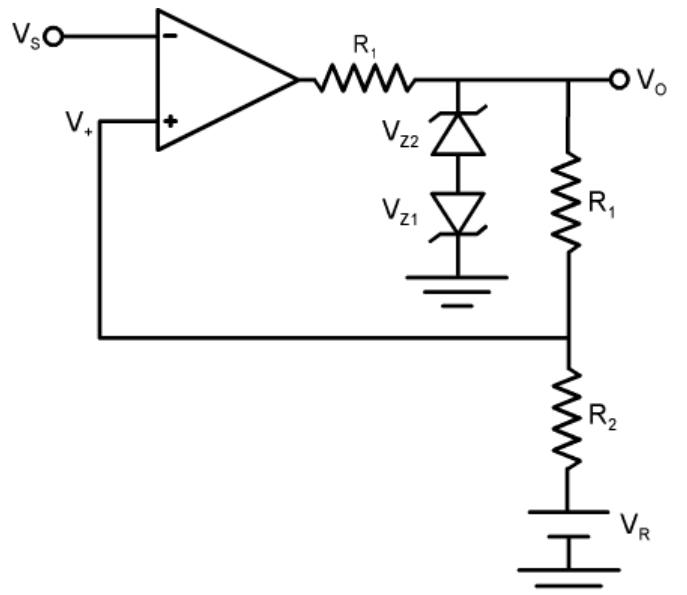
### Summary:

1.  $V_{S-} < v_s < V_{S+} \rightarrow 2$  possible stable states.
2. Hysteresis voltage  $= V_{S+} - V_{S-} = V_H$

$$V_H = \frac{2R_2}{R_1 + R_2} V_m$$

### Modifications:

- a) Clamping  $v_o$ , such that  $V_m$  is less than the rail voltages.
- b) Non-zero centre for hysteresis loop.



$$V_{S+} = V_R + \frac{R_2}{R_1 + R_2} (V_{Z2} + V_d - V_R) = V_R + \frac{R_2}{R_1 + R_2} (V_{Z2} + V_d)$$

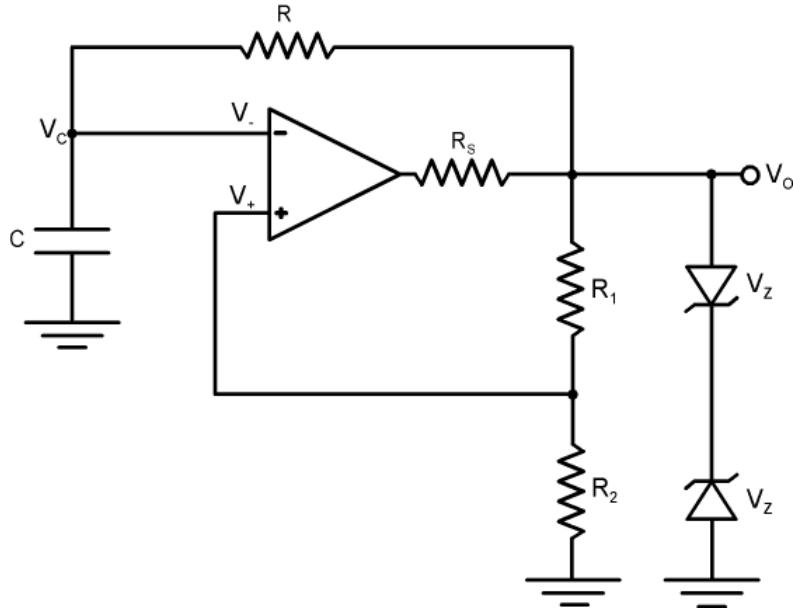
$$V_{S-} = V_R - \frac{R_2}{R_1 + R_2} (|V_{Z1}| + |V_d| + V_R) = (\frac{R_1}{R_1 + R_2}) V_R - \frac{R_2}{R_1 + R_2} (|V_{Z1}| + |V_d|)$$

### Questions:

- (a) How do you obtain a non-inverting Schmitt trigger?  
A. Interchange the role of  $v_s$  and  $V_R$ .
- (b) How to eliminate comparator “chattering”?  
A. Choose hysteresis voltage  $V_H >$  max noise voltage.

## Square-Wave Generator

(astable multivibrator)



Replace external signal to a Schmitt Trigger by an R-C circuit.

$$v_C = v_-$$

$$v_+ = \beta v_o = \frac{R_2}{R_1 + R_2} v_o$$

and  $v_o = \pm V_m$  depending on the sign of  $v_C - v_+$ .

Consider the case where

$$v_C < v_+ = \beta v_o = \beta V_m$$

capacitor charges exponentially toward  $V_m$ .

The threshold point is at  $v_C = \beta V_m$  at which the comparator output  $v_o$  changes to  $-V_m$ .

Suppose at  $t = 0$  while  $v_C = \beta V_m$ , the capacitor charges according to the equation:

$$v_C(t) = V_m \left[ 1 - (1 + \beta) \exp\left(-t/RC\right) \right]$$

at  $v_C(T_1) = \beta V_m$

$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right) = RC \ln\left(1 + \frac{2R_2}{R_1}\right)$$

when  $v_C$  reaches  $+V_m$  the comparator output  $v_o$  switches to  $-V_m$  and  $C$  will discharge towards  $-V_m$  but the threshold point is now  $-\beta V_m$ .

The capacitor equation is then:

$$v_C(t) = (1 + \beta)V_m \exp(-t/RC) - V_m$$

By inspection (symmetry):  $T_2 = T_1 = T$

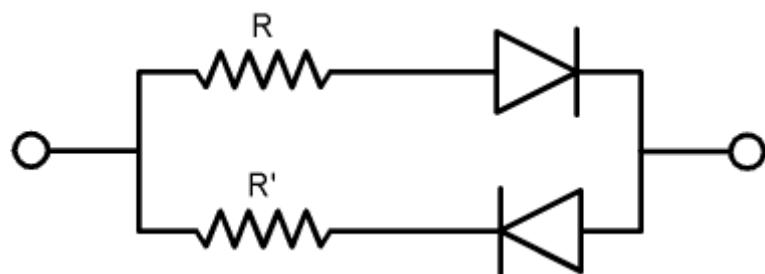
$$\therefore \text{Period } T = 2RC \ln\left(1 + \frac{2R_2}{R_1}\right) \text{ — independent of } V_m.$$

If Zener diodes do not have the same  $V_z$ , then  $v_o$  is unsymmetrical.

**Frequency range: ~10 Hz → 10 kHz**

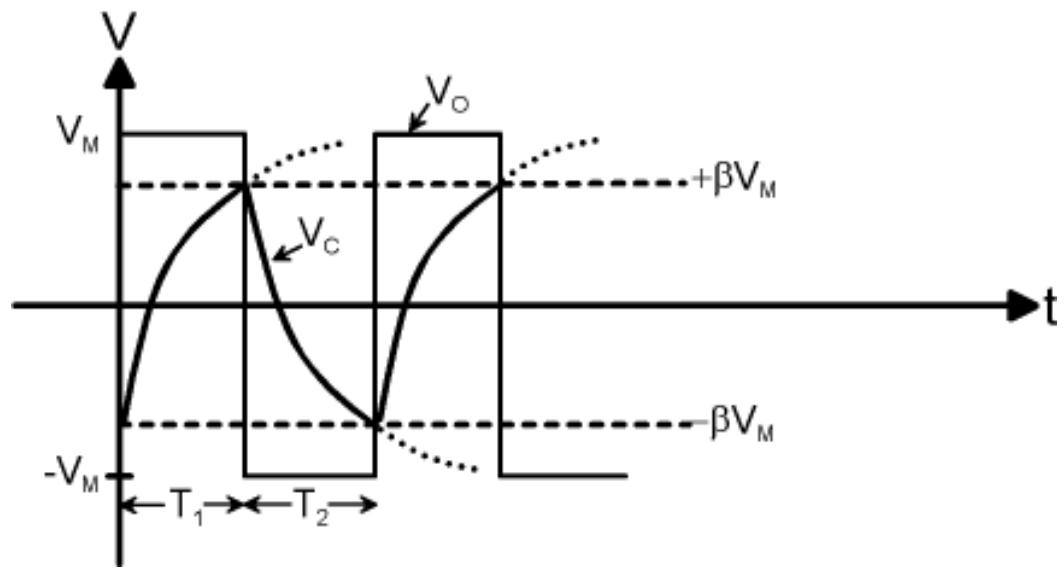
Slew rate of op-amp is limiting the slope of output waveform at higher frequencies.

To make the output non-symmetrical ( $T_1 \neq T_2$ ) we can replace  $R$  in the circuit with the following:



Now we will have:

$$T_1 = R'C \ln\left(1 + \frac{2R_2}{R_1}\right) \text{ and } T_2 = RC \ln\left(1 + \frac{2R_2}{R_1}\right)$$



## **SECTION 8: DIGITAL-ANALOGUE INTERFACE**

### **8.1 Digital-to-Analogue Conversion**

- 8.1.1 Basic Concepts**
- 8.1.2 Binary Weighted DAC**
- 8.1.3 R-2R Ladder**

### **8.2 Analogue-to-Digital Conversion**

- 8.2.1 Successive Approximation ADC**
- 8.2.2 Dual-Slope ADC**
- 8.2.3 Flash ADC**

### **8.3 Specifications ofr ADCs and DACs**

- 8.3.1 Errors in DAC**
- 8.3.2 Errors in ADC**

#### **Aims**

After this section the student should know:

- common methods for Analogue-to-Digital and Digital-to-Analogue Conversion (adc and dac)
- how to obtain simple parameters and characteristics from the circuits presented
- the role and origin of errors in adc and dac operations

## 8.1 Digital-to-Analogue Conversion

### 8.1.1 Basic Concepts

Convert a binary digital word to an analogue voltage or current

$$V_o = (a_0 \cdot 2^0 + a_1 \cdot 2^1 + a_2 \cdot 2^2 + \dots + a_{n-1} \cdot 2^{n-1}) \cdot k \cdot V_R, \quad a_i = 1 \setminus 0 \text{ for } i = 0 \dots n-1.$$
$$= \left( \frac{a_0}{2^{n-1}} + \frac{a_1}{2^{n-2}} + \dots + a_{n-1} \right) \cdot 2^{n-1} \cdot k \cdot V_R \quad (\text{DA-1})$$

where  $V_R$  is a reference voltage and  $k$  is a proportionality factor determined by the system parameters.

$a_{n-1}$  – most significant bit (MSB) weighted by  $2^{n-1} \cdot k \cdot V_R$

$a_o$  – least significant bit (LSB) weighted by  $2^0 \cdot k \cdot V_R$

e.g., for a 3-bit word

$$V_o = (a_0 + 2a_1 + 4a_2) \cdot k \cdot V_R$$

If  $a_0 = 0, a_1 = 1, a_2 = 1$

$$V_o = 6 k \cdot V_R$$

If  $a_0 = 1, a_1 = 0, a_2 = 1$

$$V_o = 5 k \cdot V_R$$

Output is an analogue voltage proportional to  $k \cdot V_R$ .

## Definitions

$$V_o = \left( a_{n-1} + \frac{a_{n-2}}{2} + \dots + \frac{a_0}{2^{n-1}} \right)$$

MSB                                    LSB  
↓                                        ↓

$$= 2 \cdot \left( \frac{a_{n-1}}{2} + \frac{a_{n-2}}{2^2} + \dots + \frac{a_0}{2^n} \right) V *$$

$$V_{o(LSB)} = 2 \cdot \left( \frac{1}{2^n} \right) V * = \frac{1}{2^{n-1}} V *$$

$$V_{o(MSB)} = V * = 2^{n-1} V_{o(LSB)}$$

Maximum output voltage occurs when digital input is (11111....1)

$$V_{o(MAX)} = \left( 1 + \frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{2^{n-1}} \right) V *$$

This is a geometric series:

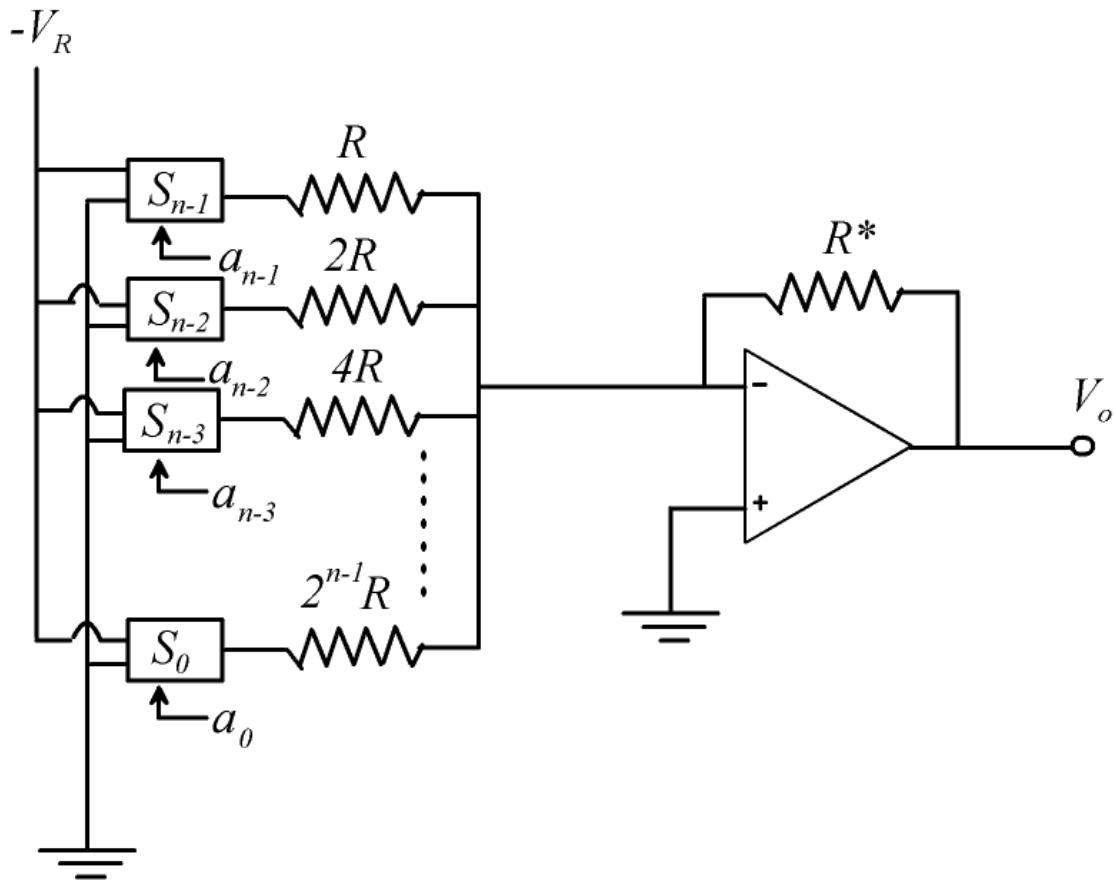
$$V_{o(MAX)} = \frac{\left( 1 - \frac{1}{2^n} \right)}{\left( 1 - \frac{1}{2} \right)} V *$$

$$= 2V_{o(MSB)} - V_{o(LSB)}$$

Nominal Full Scale output voltage is by definition:

$$V_{o(FS)} = 2V_{o(MSB)} = 2^n V_{o(LSB)}$$

## 8.1.2 Binary-Weighted Digital-to-Analogue Converter



The switches  $S_n$  are electric switches which can be controlled by bits of the binary word.

When  $a_{n-1} = 1 \rightarrow$  switch  $S_{n-1}$  connects  $R$  to  $-V_R$ .

When  $a_{n-1} = 0 \rightarrow$  switch  $S_{n-1}$  connects  $R$  to ground.

Op-amp is wired as a summing current to voltage converter.

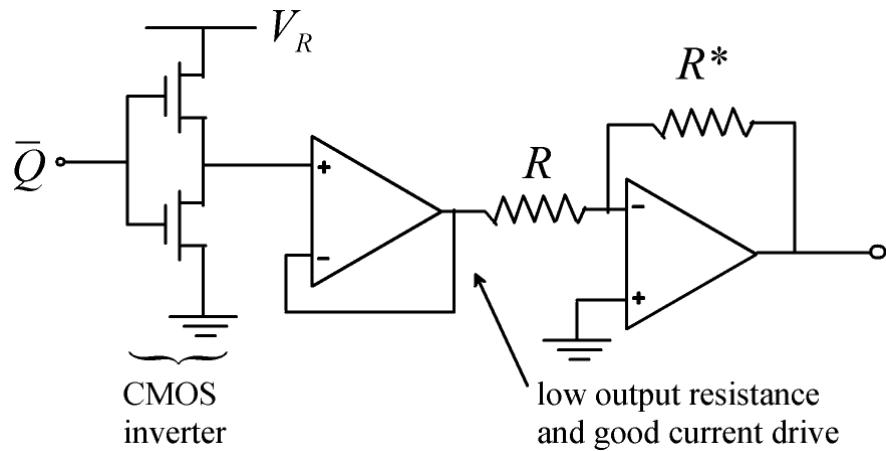
$$V_o = \left( a_{n-1} \cdot \frac{R^*}{R} + a_{n-2} \cdot \frac{R^*}{2R} + a_{n-3} \cdot \frac{R^*}{4R} + \dots + a_0 \cdot \frac{R^*}{2^{n-1}R} \right) V_R$$

$$= \left( a_{n-1} + \frac{a_{n-2}}{2} + \frac{a_{n-3}}{2^2} + \dots + \frac{a_0}{2^{n-1}} \right) \frac{R^*}{R} V_R$$

$V_o$  is proportional to the digital word.

---

## A possible switch design



Let,  $a_n = Q \rightarrow a_n = 1 \rightarrow \bar{Q} = 0$

Output of CMOS inverter is high, i.e.,  $= V_R$

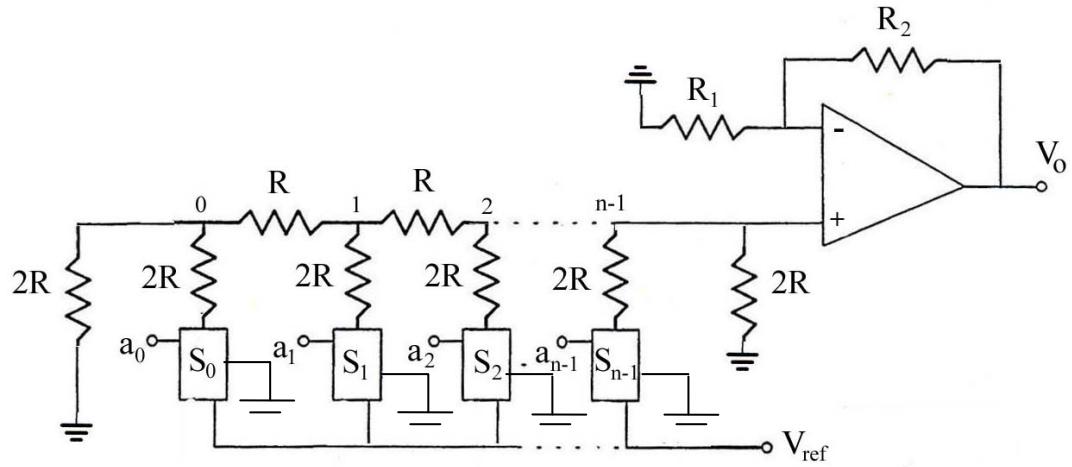
Hence:  $\rightarrow$  buffer output is  $V_R$

---

Disadvantages of this dac:

1. Very difficult to fabricate such resistor ratios over a wide range, e.g. 12 bit, and maintain the stability.
2. If  $R = 1 \text{ k}\Omega$  then  $2^{12-1}R = 2.048 \text{ M}\Omega$ . Impractical to make such large resistors values. But if we start with  $R = \text{a couple of } \Omega\text{'s}$  then we would reach values comparable to the switch output resistances.
3. This approach cannot really be used where more than 4-bits are required.

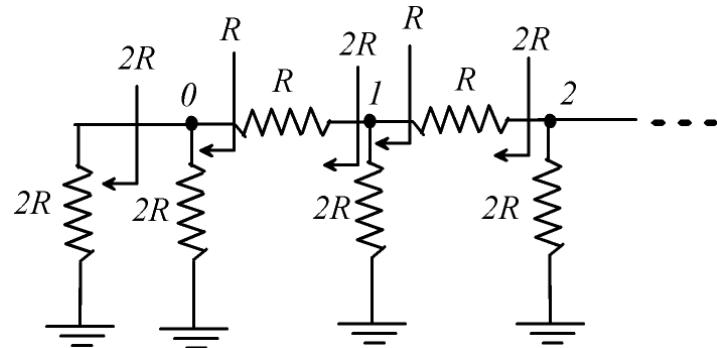
### 8.1.3 R-2R Ladder DAC



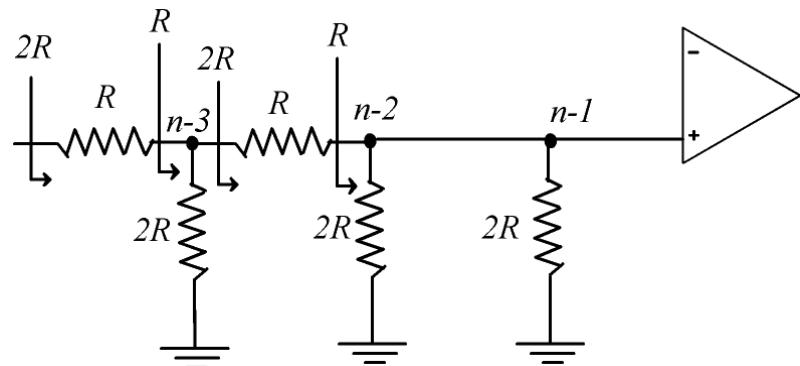
Based on current-splitting principle.

Observe that the resistance seen to the left or right or towards the switch of each node ( $0 \rightarrow n-1$ ) is always  $2R$ .

Consider the following: look to the left of node 2



Consider look to the right



Suppose  $V_R$  is applied to the MSB by making  $a_{n-1} = 1$  and  $a_0 \rightarrow a_{n-2} = 0$ , i.e., switch  $S_{n-1}$  closed to  $V_R$  and the others to ground.

The voltage at node  $n-1$ :

$$V_+ = V_{n-1} = \frac{2R//2R}{2R + 2R//2R} \cdot V_R$$

$$\therefore V_o = \left( \frac{V_R}{3} \right) \left( \frac{R_1 + R_2}{R_1} \right) = V^*$$

Now consider  $a_{n-2} = 1$ ,  $a_{n-1} = 0$  and  $a_0 = \dots = a_{n-3} = 0$ .

Voltage at node  $n-2$ :  $V_{n-2} = \frac{2R//2R}{2R + 2R//2R} \cdot V_R$

$$\text{But } V_+ = V_{n-1} = \frac{1}{2} V_{n-2} = \frac{1}{2} \left( \frac{V_R}{3} \right)$$

$$V_o = \frac{1}{2} V^*$$

again, try out  $a_{n-3} = 1$  and all other bits 0

$$\text{Voltage at node } n-3: V_{n-3} = \frac{V_R}{3}$$

$$\text{But } V_+ = V_{n-1} = \frac{1}{4} \left( \frac{V_R}{3} \right)$$

$$V_o = \frac{1}{4} V^*$$

$$\text{In general, } V_o = \left( a_{n-1} + \frac{a_{n-2}}{2} + \frac{a_{n-3}}{2^2} + \dots + \frac{a_0}{2^{n-1}} \right) V^*$$

in a form similar to equation (DA-1)

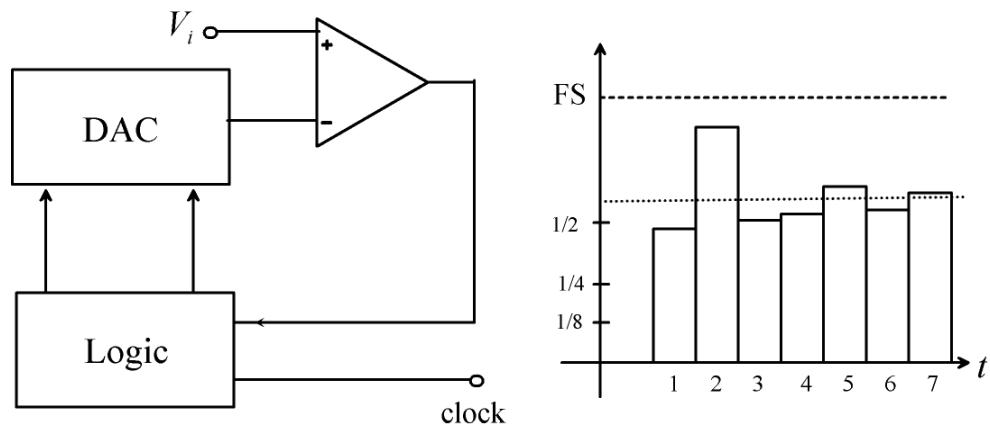
However, there is a slight problem with this circuit arrangement: variable propagation delay time due to stray-capacitance from each node to the ground - depends on which switch closes, e.g., when  $S_o$  closes, it takes a longer time for the output  $V_o$  to settle down than when  $S_{n-1}$  closes.

## 8.2 Analogue-To-Digital Conversion

Data from the physical system ('real world') always appear in analogue form → continuous voltage or current, e.g. thermocouple voltage, strain gauge bridge output.

Analogue-to-Digital Converters (ADCs) provide a means of converting such analogue signals into digital form for display purposes, storage in memory or additional digital processing.

### 8.2.1 Successive Approximation ADC



Successive approximation is a comparison method, in which  $V_i$  is compared to  $V_{DAC}$ .

Sign of the error signal  $V_i - V_{DAC}$  sets successive bits of the digital input to the DAC.

Bits are set and tested in turn, starting with the most significant bit:

$$\equiv \frac{1}{2} \text{ full scale.}$$

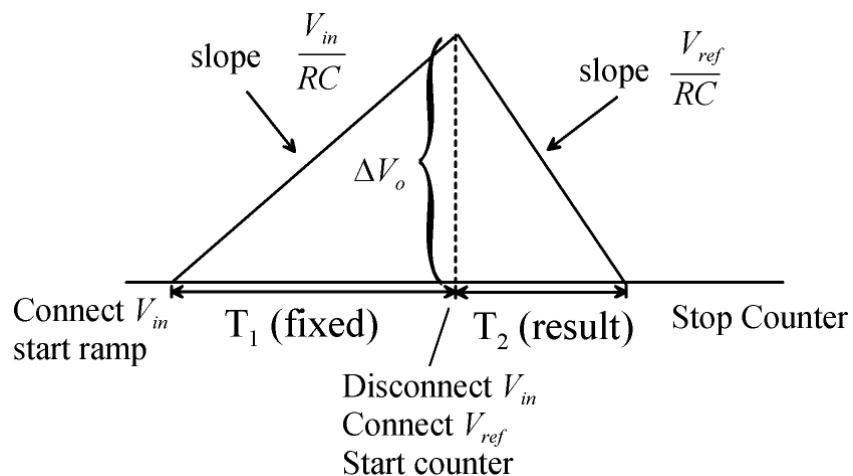
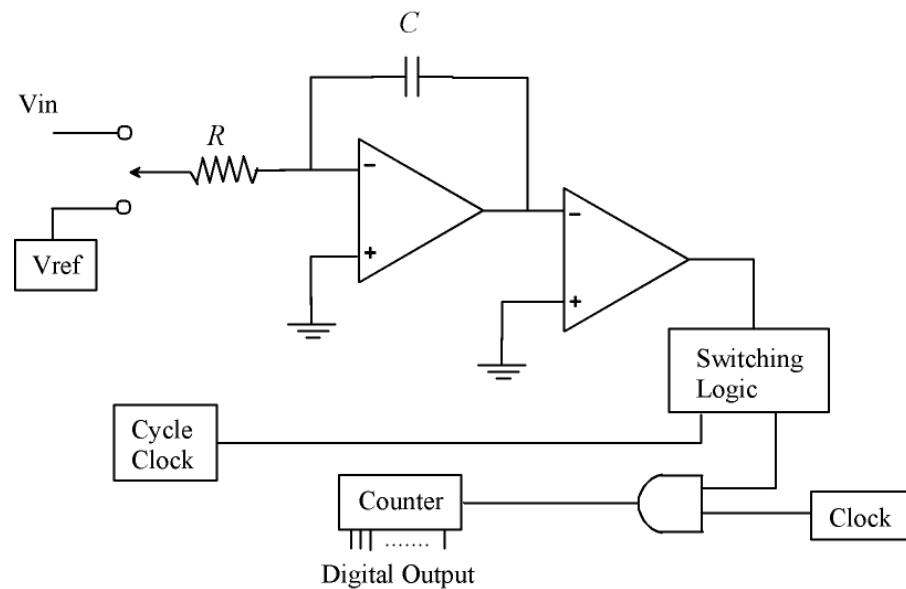
The Logic block must perform the following function:

- When the Encode or Convert signal is set, the MSB of the DAC is set.
- if  $V_i > \frac{1}{2}FS$  the sign of the comparator voltage results in the MSB being "kept"
- In the next clock cycle, the next MSB is set and this new approximation is compared to  $V_i$  – note  $V_i < \frac{3}{4}FS$  too large,

resulting in an opposite sign in the comparator output – hence the bit is “turned off”

- Continue with the next MSB etc, etc, until all bits are tried.
- At the end of the last test, a status line will indicate conversion complete.
- Successive approximation method is fast -  $n$  clock cycles only - for  $n$  bit result.
- Lacking in noise immunity especially in high resolution ADC

## 8.2.2 Dual Slope ADC



Circuit consists of an analogue integrator whose output voltage is the time integral of the input voltage  $V_{in}$

Assume that a constant  $V_{in}$  is applied,  $V_o$  will change at a rate given by

$$\frac{dV_o}{dt} = \frac{V_{in}}{RC}$$

At the start of the cycle, switch connects  $V_{in}$  to the integrator and  $V_o$  ramps upwards (depending on the sign of  $V$  for a fixed interval  $T_1$  (sampling period)

At  $T_1$  the cycle clock switches over  $V_{ref}$  to the integrator where  $V_{ref}$  is of the opposite polarity and initiates the counter. Integrator ramps downwards until  $V_o$  makes a zero crossing. The time taken to do this is  $T_2$  at which time the counter stops.

Obviously, the duration  $T_2$  depends on the magnitude of  $V_{in}$  for a fixed  $V_{ref}$

$$\text{Hence, } \Delta V_o = T_1 \left( \frac{V_{in}}{RC} \right) = T_2 \left( \frac{V_{ref}}{RC} \right)$$

If the clock period is  $T = \frac{1}{f}$

Then in the interval  $T_2$ , the number of accumulated pulses is  $n_2$ : ( $T_2 = n_2 T$ )

Also, for the fixed interval:  $T_1 = n_1 T$

$$\therefore V_{in} = n_2 \left( \frac{V_{ref}}{n_1} \right) \propto n_2$$

Counter reading is proportional to the analogue input  $V_{in}$

Note that this relationship is independent of  $f$  – clock frequency

However, accuracy depends on  $V_{ref}$  though the precision depends on  $f$  and  $T$ ,

Noise rejection:

A dual slope ADC has inherently good noise rejection.

Noise which goes through several cycles during the sampling period  $T_1$  makes positive and negative contributions to the integral which tends to average out.

$$\text{Ave. noise} = \frac{1}{T} \int_{-T/2}^{T/2} \cos\left(\frac{2\pi k}{T} t\right) dt = \frac{\sin(k\pi)}{k\pi}$$

where  $f_{noise} = \frac{k}{T}$        $\Rightarrow$       decreases as  $f_{noise}$  increases.

Noise components whose periods are integral multiples of the sampling time  $T_1$  are totally rejected. Hence for 50 Hz rejection, choose  $T_1 = 20$  ms.

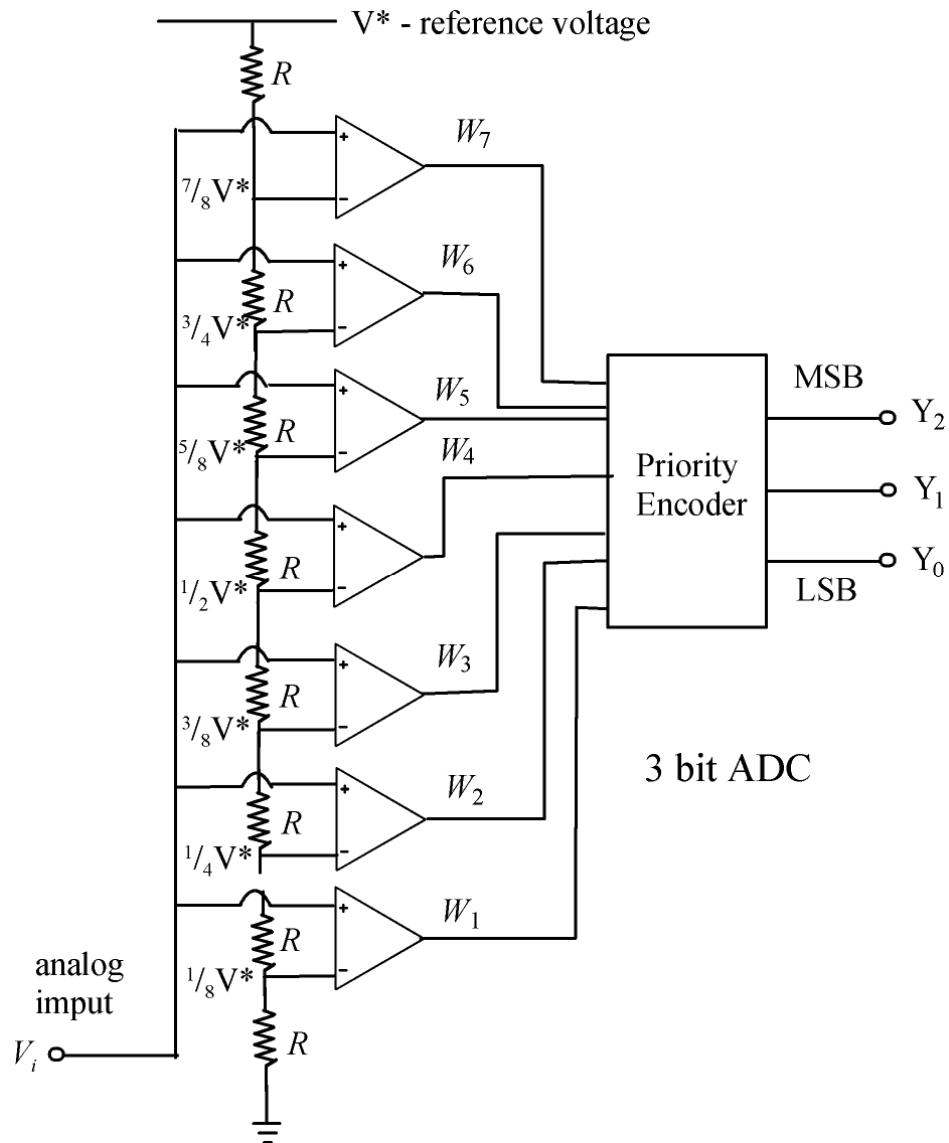
The throughput rate of dual slope converters is limited to somewhat less than  $\frac{1}{2T_1}$  conversions per second.

Too slow for fast data acquisition  
Used in Digital Volt Meter (DVM)

## ADC Comparison

	Dual	Successive
	<u>Slope</u>	<u>Approx</u>
Speed	Low	High
Resolution	High 3→6 digits >10 bit	Medium 8-12 bits
Accuracy	Excellent	Good
Noise Immunity	Excellent	None
Typical Application	DVM	Digital Signal Processing

### 8.2.3 Flash ADC



Fastest of all ADC converters

Analogue input  $V_i$  is applied simultaneously to all comparators  
Threshold voltage of each comparator is evenly spaced.

If  $V_i$  is greater than the threshold voltage, the comparator output will be high.

Eg If  $\frac{1}{4}V^* < V_i < \frac{3}{8}V^*$  then  $W_1 = 1, W_2 = 1$

And  $W_3 \rightarrow W_7 = 0$

### 3 bit Priority encoder truth table

$W_7$	$W_6$	$W_5$	$W_4$	$W_3$	$W_2$	$W_1$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	.	0	1
							.	.	
							.	.	
							.	.	
							.	.	
1	1	1	1	1	1	1	1	1	1

Conversion time is limited by the speed of the comparator and the priority encoder  $\sim 20\text{ns}$

Disadvantages: complexity of hardware: N bit ADC requires  $2^{N-1}$  comparators.

i.e. the no. of comparators double for each additional bit.

→ complexity of priority encoder also increases

All parallel flash AD converters tend to have fair random linearity errors. Related to the offset – voltage matching of comparators and tolerance of the resistors in the voltage divider.

Codes can be missed if adjacent comparators have offset voltages of opposite polarity and sufficient magnitude.

Because the input is connected to a large no, of comparators the i/p capacitance is high – must be driven by an analogue buffer which is stable when driving large capacitive loads.

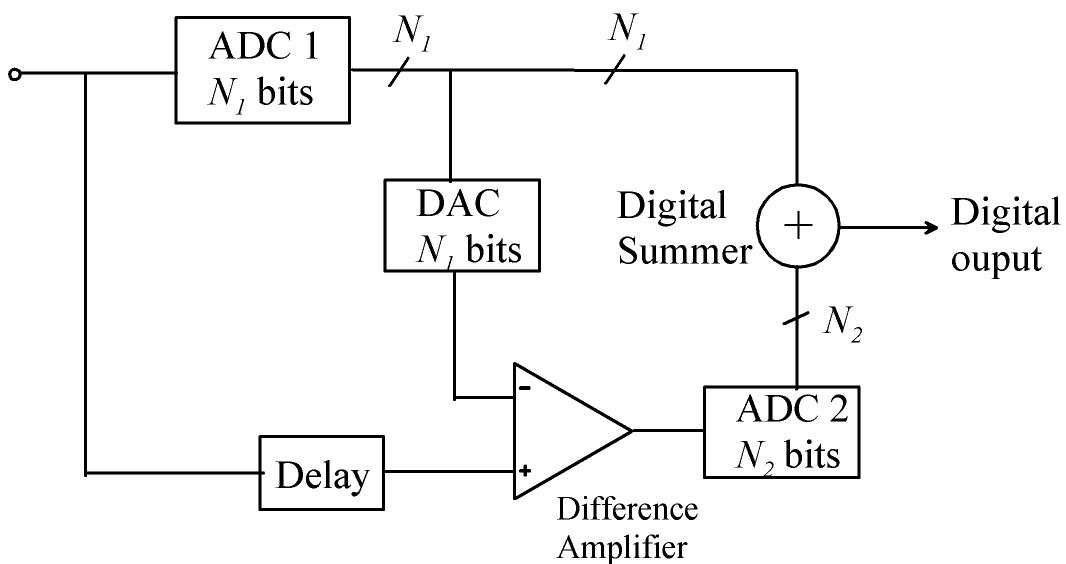
## Subranging Flash ADC

Typical Flash ADC resolve  $\sim 6$  bits

$$\text{N}^{\circ} \text{ of comparators} = 2^N - 1$$

9 bit resolution requires 511 comparators!

Question: how can we increase the resolution?



1<sup>st</sup> ADC produces a  $N_1$  bit digital code that is supplied to the output as the  $N_1$  MSB of the digit output code.

This digital output is also applied to a DAC which produces an analogue voltage corresponding to the  $N_1$  MSB.

The analogue output from the DAC is subtracted from the analogue input in the difference amplifier to produce an error (difference) voltage.

This difference voltage is converted by ADC into  $N_2$  bits. This constitutes the  $N_2$  LSB of the digital output code.

Hence, the full complement of digital output is  $N_1+N_2$  bits.

4 bit Flash ADC  $\rightarrow$  produce 8 bit digital output.

Problem:

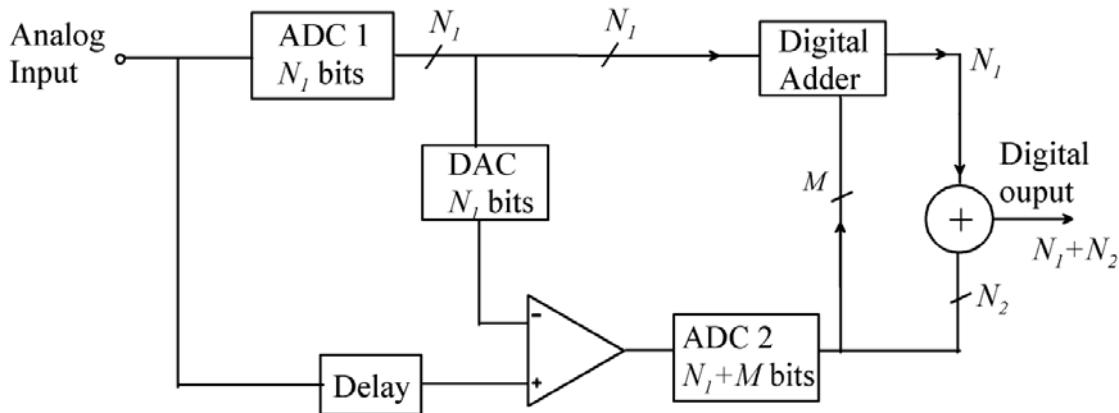
- (a) For 8 bit accuracy, the accuracy of each ADC must be such that the conversion error in each be  $< V_{FS} / 2^8$

ADC2 – no problem, since this corresponds to a maximum error of  $\frac{1}{2^4}$  of its F.S. Voltage.

ADC1- must have an error not exceeding  $\frac{1}{2^8} V_{FS} \rightarrow$  difficult to achieve.

- (b) Delay in ADC2 conversion, due to delays in ADC1, DAC, difference amplifier – significant problem for a rapidly changing input voltage (Track threshold function)

## Digitally Correcting Subranging (DCS) Flash ADC



The difference voltage supplied to the ADC 2 may fall outside its FS conversion range.

Increase the no. of bits from  $N_2$  to  $N_2 + M$  for ADC 2

The  $N_2$  LSBs of ADC 2 still becomes the  $N_2$  LSB of the total digital output code

The  $M$  MSBs of ADC<sub>2</sub> are combined with the  $N_1$  bits of ADC 1, to produce  $N_1$  MSBs of the total digital output code (digital correcting subranging)

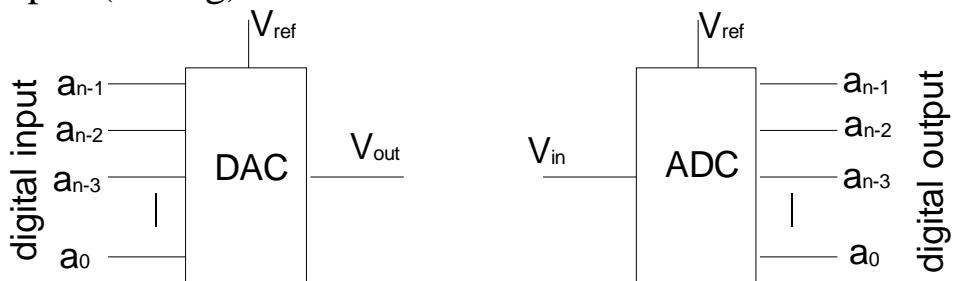
If no errors were made in ADC 1 or DAC then  $M$  MSBs of ADC 2 will be zero and no correction will be made to output of ADC.

If there is error from ADC 1, the  $M$  bits generated from ADC 2 will correct the  $N_1$  bits from ADC 1

Timing is of extreme importance – as each element in the conversion process must settle to its optimal point before the required stroke signal is applied.

### 8.3. Specifications of ADCs and DACs

- Popular D-A applications: CD/DVD players - where the digital information stored in the disc is converted to music via a high precision DAC; ADCs that involve the use of DACs (eg. Successive Approximation type)
- What defines the performance of the DAC?
- Popular A-D applications: data acquisition for signal processing
- What defines the performance of the ADC? - what's the difference from DAC specifications? - subtle
- DAC converts a discrete digital code to a specific analog representation: a fixed number of inputs(digital) and outputs(analog).



- ADC input is an analog signal with an infinite number(range) of values, which is then quantised into an N-bit digital word.
- Note: DACs and ADCs can use either voltage or current as it analog signal. For this discussion, we assume the signal is a voltage.

## DAC

- Output of a **N** bit DAC is given as follows:

$$V_{out} = \frac{D}{2^N} V_{ref}$$

where  $D$  is the digital input word ( $a_{n-1}, a_{n-2}, \dots, a_0$ ).

$2^N$  is the number of input combinations.

- **Eg.1** For a N=5 bit resolution converter,  $V_{ref} = 3\text{volts}$  and a digital word  $D = (10100) = 20_{10}$

$$V_{out} = \frac{20_{10}}{2^5} V_{ref} = 1.875\text{v}$$

- Plot of  $V_{out}$  versus the input word D would give the transfer curve as shown in figure DA1

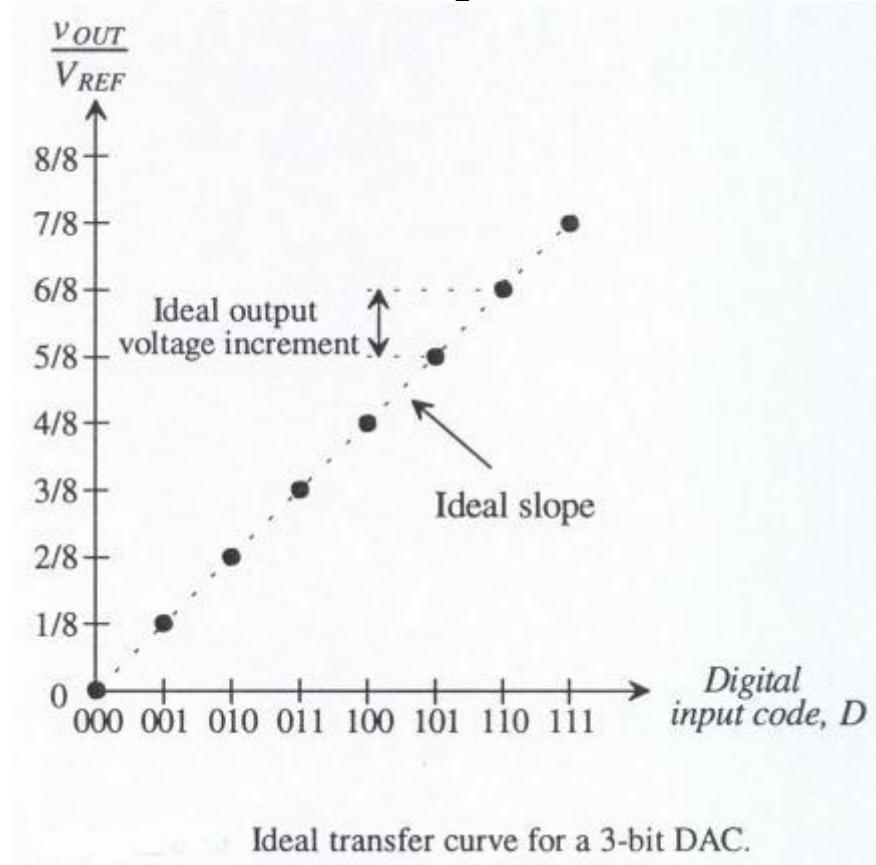


Figure DA1

### Comments:

- Transfer curve is not continuous since the input signal is digital signal (inherently discrete) - hence output can have only fixed number of values as determined by the digital word input.
- For the N=3 bit DAC example in figure DA1, the max. output voltage  $V_{out(max)} = 7/8 V_{ref}$ .

**General comments:** The max. analog output voltage that can be generated is known as the **FULL-SCALE VOLTAGE**  $V_{FS}$ .  
For a N-bit DAC, it is :

$$V_{FS} = \frac{2^N - 1}{2^N} V_{ref}$$

The **least significant bit**  $a_0$  (LSB) defines the smallest possible change in the analog output voltage :

$$1 \text{ LSB is defined as} = \frac{V_{ref}}{2^N}$$

Hence for the example of a 5 bit DAC with  $V_{ref} = 3$  volts,  
 $1 \text{ LSB} = 93.75\text{mV}$ .

Obviously, as the number of bit increases (for better resolution), the analog value of 1 LSB decreases.

The **most significant bit**  $a_{N-1}$  (MSB) will contribute a change of  $\frac{1}{2} V_{ref}$ .

**Resolution** of the DAC is the smallest change in analog output voltage (or current) w.r.t. to  $V_{ref}$  (or  $I_{ref}$ ) that the DAC can generate.

**Dynamic range(DR)** of a DAC is defined as the largest output signal over the smallest output signal - related to the resolution of the converter

$$DR = 20 \log \left( \frac{2^N - 1}{1} \right) \text{ dB}$$

For a 16-bit DAC,  $DR = 96.33 \text{ dB}$ .

**Eg.2** What resolution of a DAC is required to produce an output change of 0.6 mV increments with a 3 volt reference voltage

DAC must resolve  $\frac{0.6mV}{3V} = 0.0002$  or 0.02%

Accuracy required will be  $\frac{1}{2^N} = 0.0002$

$$\therefore N = \log_2 \left( \frac{3V}{0.6mV} \right) = 12.29 \text{ bits}$$

which means we have to have at least N=13bit DAC to meet the resolution requirements.

**Eg.3** For a 3-bit, 8-bit and 16 bit DAC, find their corresponding values for 1 LSB, % accuracy and  $V_{FS}$ , for a  $V_{ref}$  of 5 volts.

Resolution	Input combinations	1 LSB	% accuracy	$V_{FS}$
3	8	0.625V	12.5	4.375V
8	256	18.5mV	0.391	4.985V
16	65,536	76.29μV	0.00153	4.9999V

Note:

- Accuracy doubles for each LSB increase in resolution
- $V_{out(max)}$  approaches  $V_{ref}$  at high resolutions.

### 8.3.1. Errors in DAC

The accuracy of a DAC is described by three fundamental types of errors.

- 1) OFFSET ERRORS
- 2) GAIN ERRORS
- 3) (INTEGRAL) NON-LINEARITY ERRORS

Non-Linearity errors are the most important because they cannot be conveniently compensated. Gain and offset errors can be adjusted or compensated for.

## OFFSET ERROR

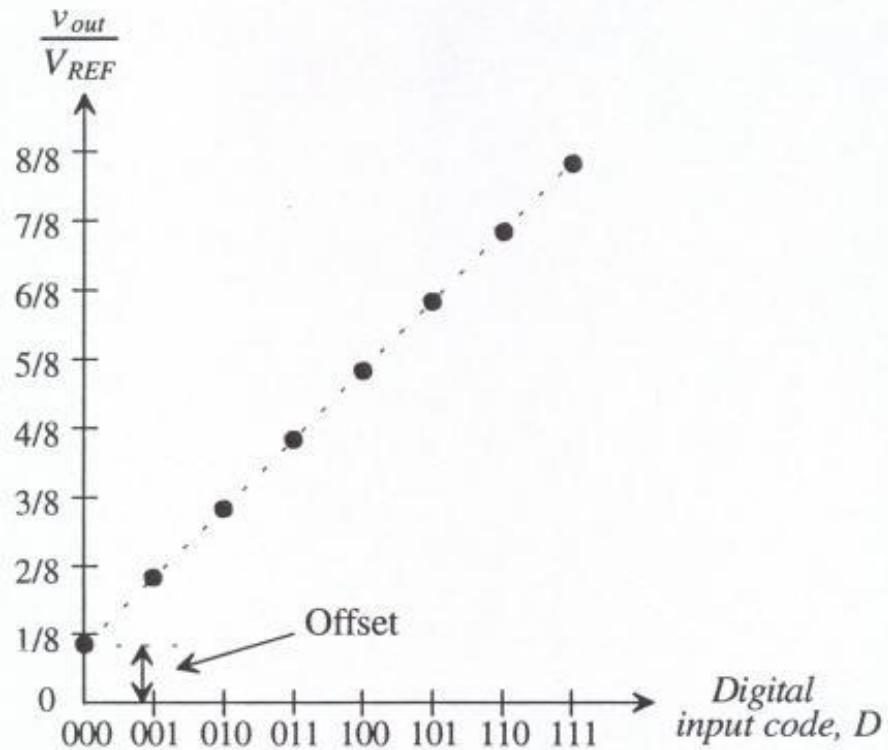


Illustration of offset error for a 3-bit DAC.

Figure DA2

- Analog output should be ZERO for digital input of  $D= (00..0)$
- But if not, offset voltage exist, resulting in a shift of the transfer curve as shown in figure DA2.

## GAIN ERROR

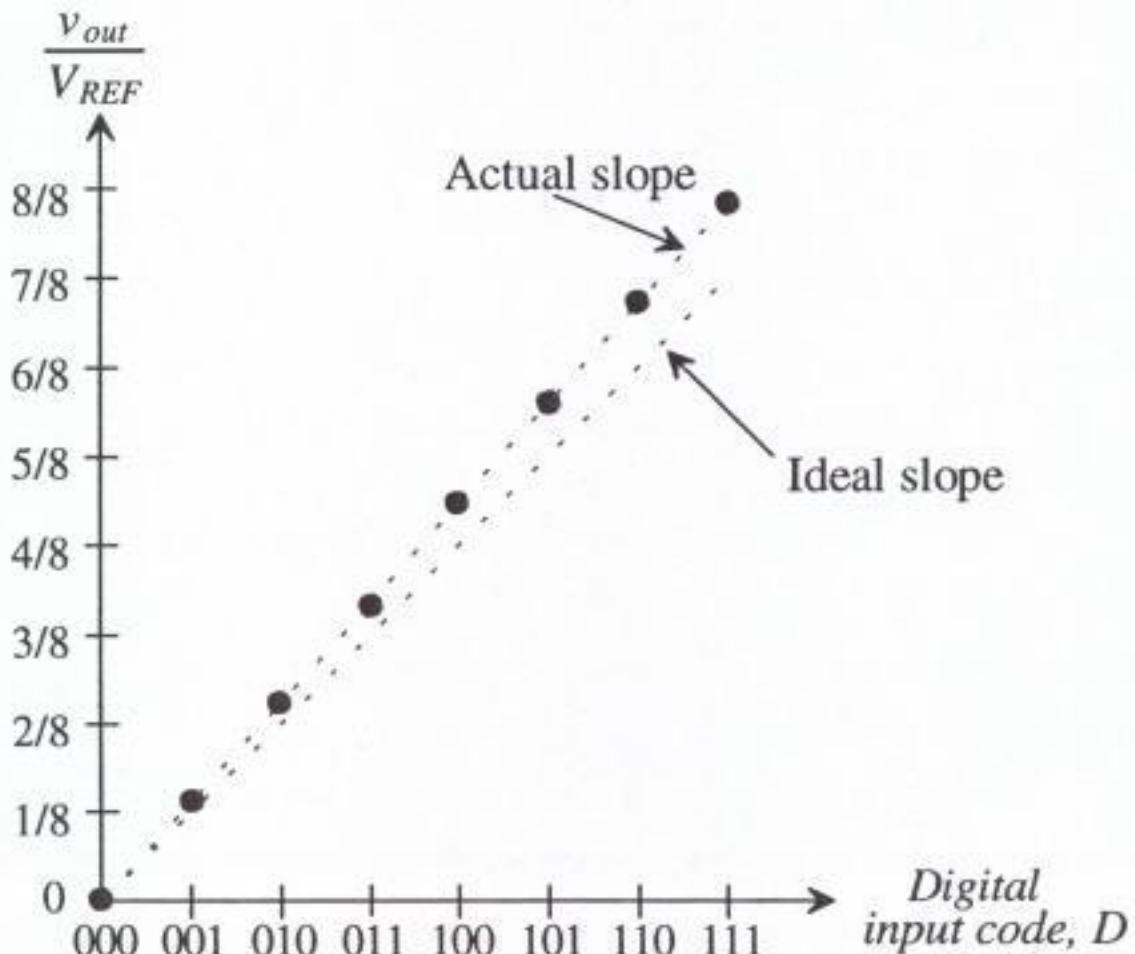


Illustration of gain error for a 3-bit DAC.

Figure DA3

- Slope of the best-fit line through the transfer curve is different from the slope of best-fit line for the ideal case
- Gain error = Ideal slope - Actual slope

## DIFFERENTIAL NON-LINEARITY (DNL) ERROR

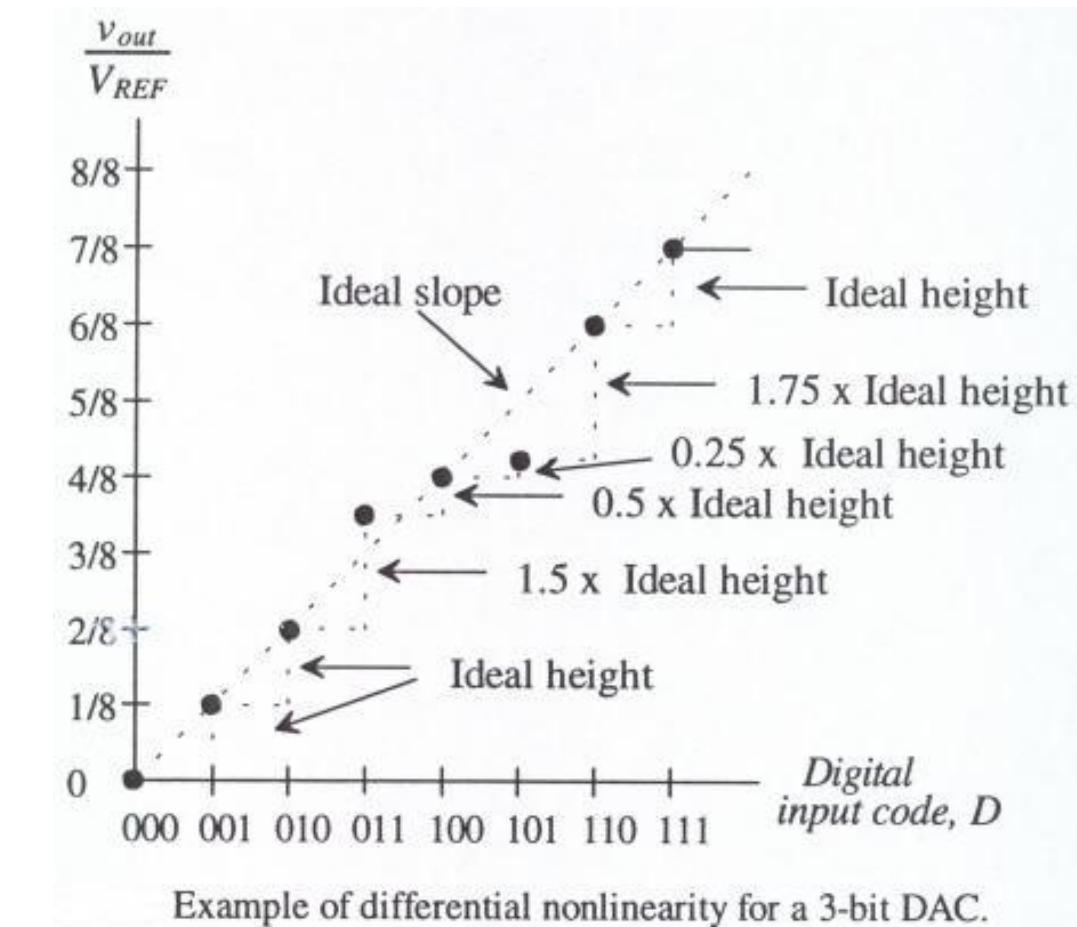
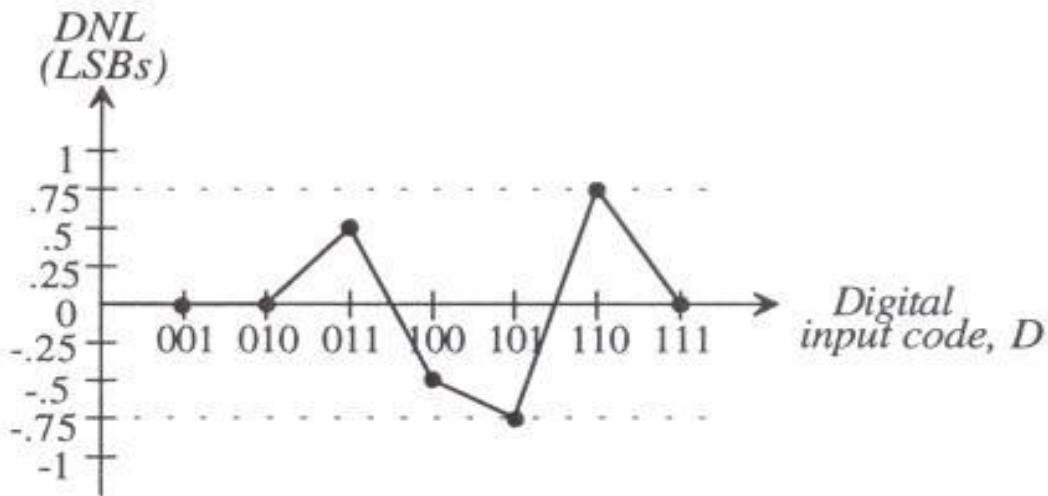


FIGURE DA4



DNL curve for the nonideal 3-bit DAC.

Figure DA5

**Definition:**

The difference between the actual analog increments and their ideal values is known as the DNL error:

**DNL<sub>n</sub> = Actual increment height of transition n – Ideal increment height**  
(where the height is expressed as fractions of LSB)

Eg.  $DNL_3 = 1.5 \text{ LSB} - 1 \text{ LSB} = 0.5 \text{ LSB}$

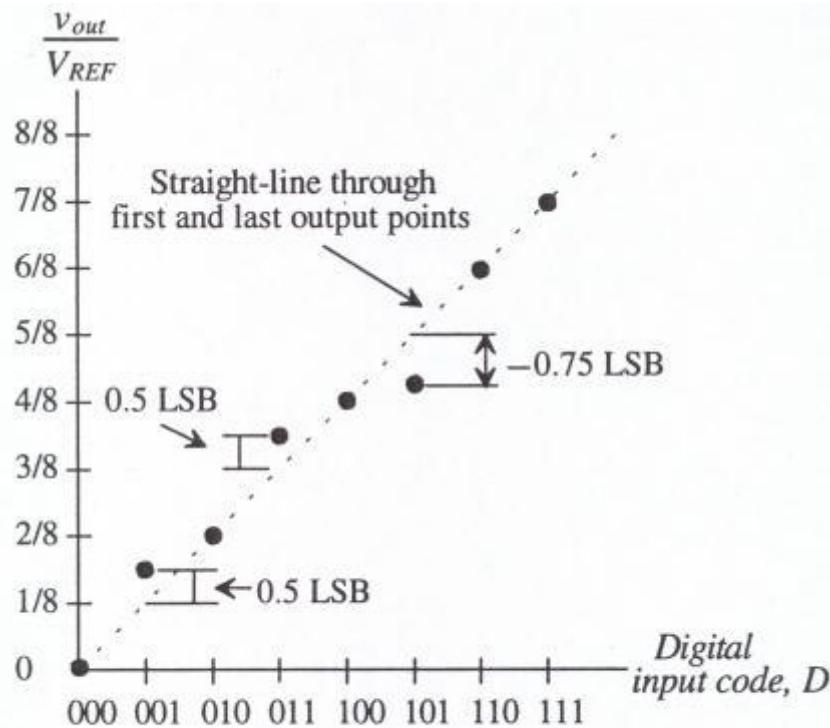
$$DNL_5 = 0.25 \text{ LSB} - 1 \text{ LSB} = -0.75 \text{ LSB}$$

$$DNL_7 = 1 \text{ LSB} - 1 \text{ LSB} = 0 \text{ LSB}$$

in this example the worst case DNL is  $\pm 0.75 \text{ LSB}$ .

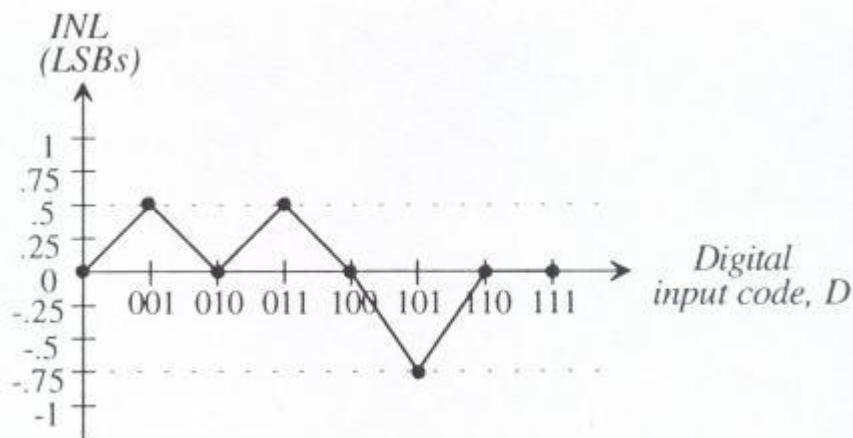
- DNL is a measure of how well the DAC can produce analog LSB multiples at the output - an indication of the **monotonicity** of the DAC.
- DACs with DNL of less than -1 LSB is considered to be **non-monotonic**. [this is not a desirable outcome for DACs]
- Typically, DACs will have less than  $\pm 0.5 \text{ LSB}$  of DNL if it is to be N-bit accurate. i.e. if a 6-bit DAC has 0.75 LSB of DNL, the DAC has a resolution of 5-bits only.
- Overall DNL performance is determined by its worst-case DNL as seen in the DNL plot in figure DA5.

## INTEGRAL NON-LINEARTIY (DNL) ERROR



Example of integral nonlinearity for a DAC.

Figure DA6



INL curve for the nonideal 3-bit DAC.

Figure DA7

**Definition:**

- INL is defined as the difference between the DAC output values and a reference straight line drawn through the first and the last output values - it defines the overall linearity of the transfer curve.
- **INL<sub>n</sub> = Output value for input code n - Output value of the reference line at point**

Eg:

$$\text{INL}_2 = \text{INL}_4 = \text{INL}_6 = \text{INL}_7 = 0$$

{in this example of Figure DA6, it so happens the reference line coincides with the ideal transfer curve, which is not always the case}

$$\text{INL}_1 = \text{INL}_3 = 0.5 \text{ LSB}$$

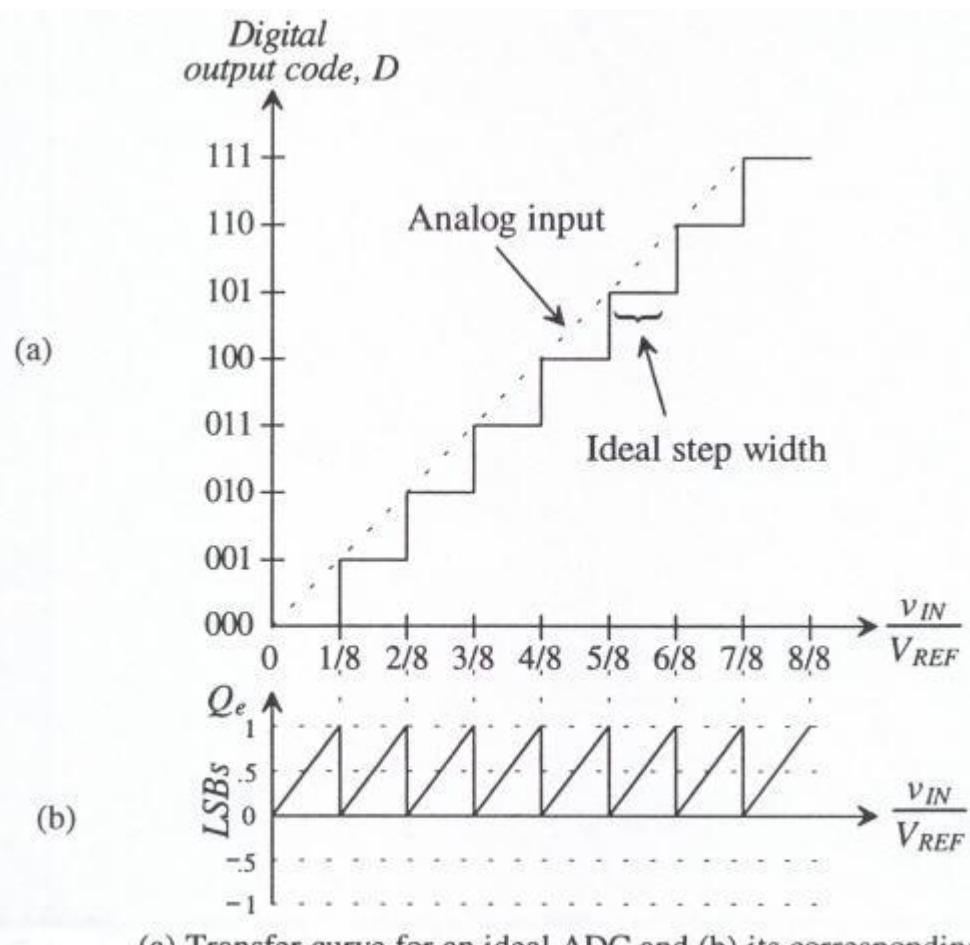
$$\text{INL}_5 = -0.75 \text{ LSB}$$

- Usually, the INL of a DAC is taken as the worst case INL : for the case in figure DA6,7 the worst case INL is +0.5LSB and -0.75LSB.

# ADC

- In contrast to DACs, ADCs involve analog inputs with an infinite number of values, which has to be quantised into a N-bit digital word.
- For a 16 bit ADC with  $V_{ref} = 5V$ , it has to be able to resolve changes in the analog signal of  $76.294\mu V$ .
- Remember, the ADC has a finite number of discrete outputs determined by the number of bits N. - it has to “quantise” the infinite-valued analog signal into many segments:

$$\text{Number of quantisation levels} = 2^N$$



(a) Transfer curve for an ideal ADC and (b) its corresponding quantization error.

Figure AD1

Note:(with reference to fig.DA1 for a 3bit ADC)

- The  $2^N$  quantisation levels corresponding to the digital codes from 0 – 7.
- Max output of ADC is (111) corresponding to the value for which  $\frac{V_{in}}{V_{ref}} \geq \frac{7}{8}$
- Figure DA1(b) shows the error caused by the quantisation.
- In general, 1 LSB =  $1/2^N$

### Quantisation Error $Q_e$

Quantisation error is defined as the difference between the actual analog input and the value of the output staircase given in volts:

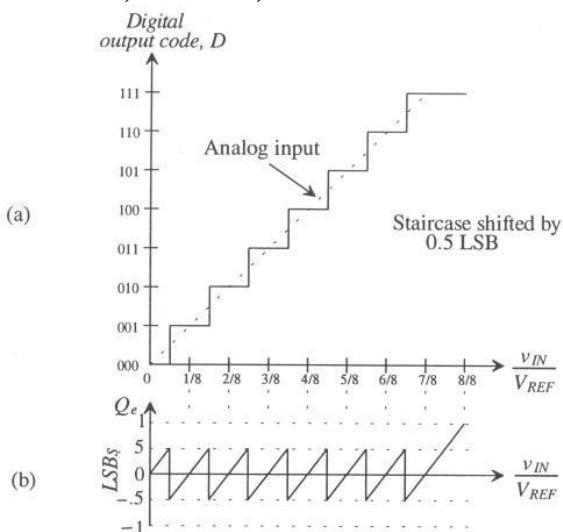
$$Q_e = V_{in} - V_{staircase}$$

and  $V_{staircase} = D \cdot \frac{V_{ref}}{2^N} = D \cdot V_{LSB}$

where D is the value of the digital word  $(a_{n-1} a_{n-2} \dots a_0)$

Figure DA1(b) shows the sawtooth waveform centred around  $1/2$  LSB.

Figure DA2 shows the transfer curve centred around 0 LSB by shifting the transfer curve of DA1 by  $1/2$  LSB to the left. - then the quantisation error, at best, for an ideal ADC is  $\pm 1/2$  LSB.



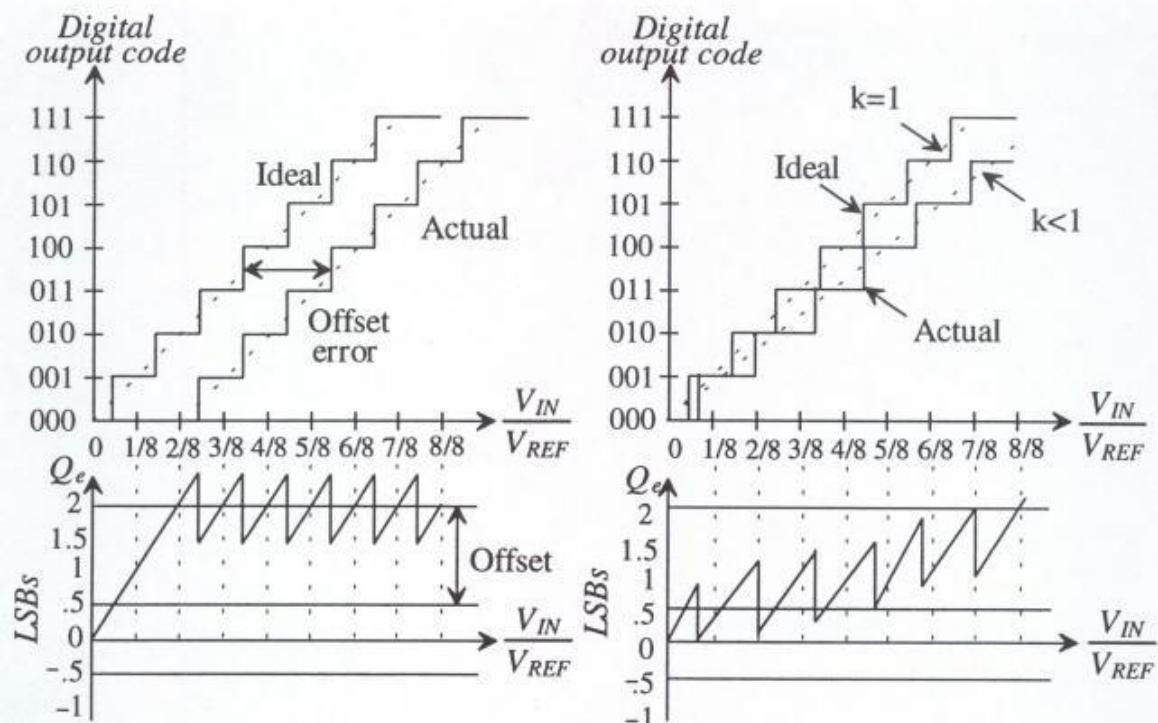
(a) Transfer curve for an ideal 3-bit ADC with (b) quantization error centered about zero.

Figure AD2

*Implications:*

- The first code transition occurs when  $\frac{V_{in}}{V_{ref}} \geq \frac{1}{16}$ .
- Range of  $\frac{V_{in}}{V_{ref}}$  to (000) is half as wide as the ideal step width.
- Last code transition occurs when  $\frac{V_{in}}{V_{ref}} \geq \frac{13}{16}$ , such that this last code transition is 1.5 times larger than the ideal width and that the quantisation error extends up to 1 LSB  
- but, range of ADC is considered out of range when  $\frac{V_{in}}{V_{ref}} \geq \frac{15}{16}$

### Gain and Offset Error



Transfer curve illustrating (a) offset error and (b) gain error.

(a)

(b)

Figure AD3

*Offset error:* occurs when there is a difference between the value of the first code transition and the ideal value of  $\frac{1}{2}$  LSB. Such an error can be compensated for and the transfer curve moves back to the ideal as can be seen in figure AD3(a)

*Gain error:* is the difference in the slope of the straight line drawn through the transfer characteristic and the slope of 1 of an ideal ADC as shown in figure AD3(b)

### Differential Non-linearity Error

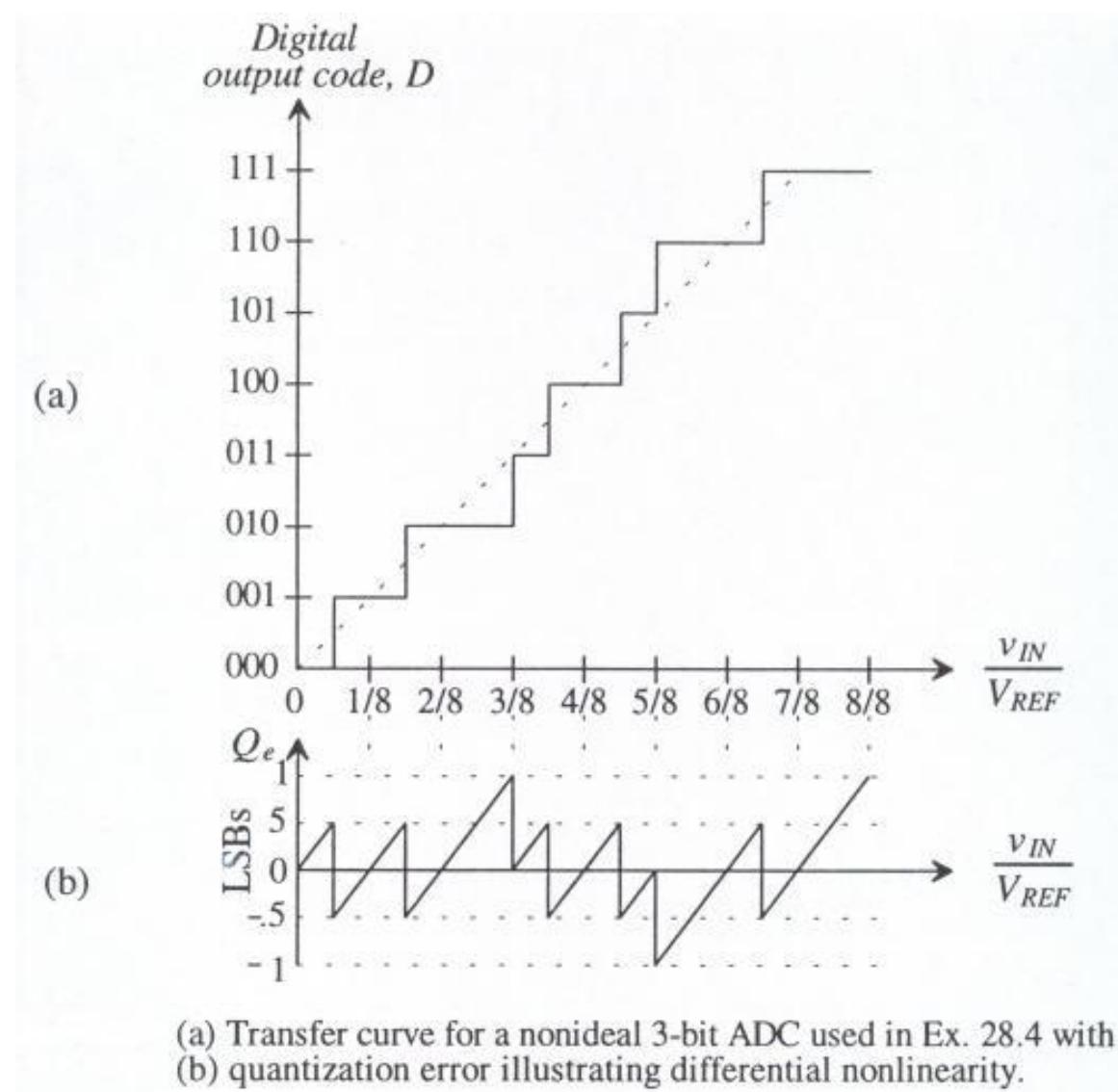


Figure AD4

- Just like in DACs, the ADC Differential Non-Linearity Error is the difference between the actual code width of a non-ideal converter and the ideal case.
- $DNL = \text{Actual step width} - \text{Ideal step width}$   
where the stepwidth are expressed in LSBs.
- In general the step width

$$V_{\text{stepwidth}} = \frac{1}{2^N} V_{ref} = 1 \text{ LSB}$$

For a 3 bit case with  $V_{ref} = 5V$ ,  $V_{\text{stepwidth}} = 0.625V$ .

- Referring to figure AD4:
  - Since the ideal stepwidth of the (000) transition is  $\frac{1}{2}$  LSB, the  $DNL_0 = 0$
  - Also note that the step width of (001) and (011) are equal to 1LSB, therefore  $DNL_1 = DNL_4 = 0$  LSB
  - For the rest , convince yourselves that
 
$$DNL_2 = 1.5 \text{ LSB} - 1 \text{ LSB} = 0.5 \text{ LSB}$$

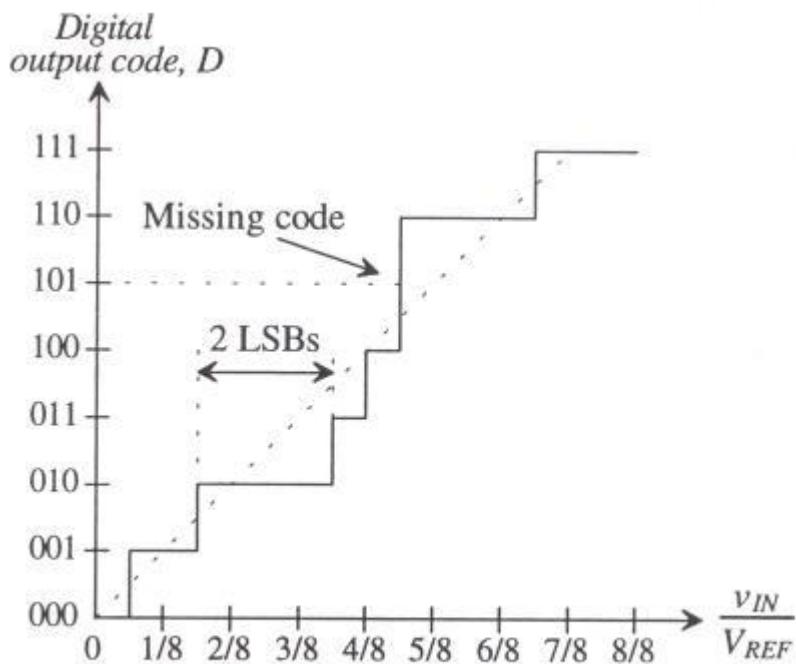
$$DNL_3 = 0.5 \text{ LSB} - 1 \text{ LSB} = -0.5 \text{ LSB}$$

$$DNL_5 = -0.5 \text{ LSB}$$

$$DNL_6 = 0.5 \text{ LSB}$$

$$DNL_7 = 0 \text{ LSB} \text{ (since the ideal stepwidth here is } 1.5 \text{ LSB at the code transition)}$$
- Overall DNL error for the converter of figure AD4 is  $\pm \frac{1}{2}$  LSB.
- As DNL error increases in either direction, the quantisation error worsens. Ideally , we like to have each ‘tooth’ in  $Q_e$  to be the same.

- ***Missing Codes:***



Transfer curve for a nonideal 3-bit ADC with a missing code.

Figure AD5

- Consider the case when  $DNL = -1 \text{ LSB}!!.$
- Refering to figure AD5, look at the step width corresponding to (101) - its completely missing!!  
This has a  $DNL = -1 \text{ LSB}$
- In general, whenever a ADC has a  $DNL \leq -1 \text{ LSB}$ , there will be a missing code.
- Note: step (010) has 2 LSBs the corresponding  $DNL_2 = +1 \text{ LSB}.$
- Note: however there is no missing code at (011), since the step width of code (011) is dependent on the (100) transition.
- In general,  $DNL \geq +1 \text{ LSB}$  is not guaranteed to have a missing code, but it could.

## Integral Non-Linearity Error

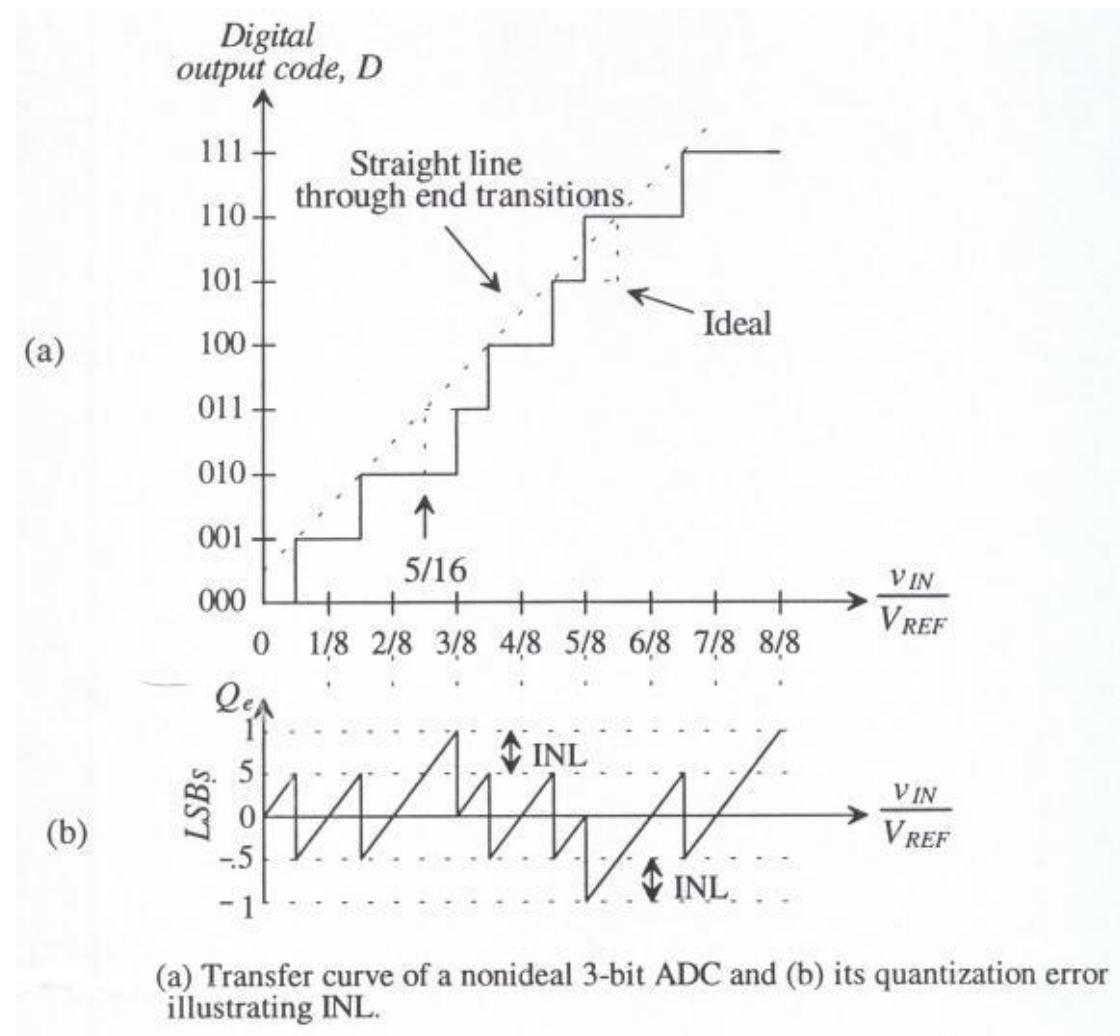


Figure DA6

**INL:** like in DNL, is defined as the difference between the data converter code transition points and the straight line with all other error set to zero. That straight line is the “best-fit” line drawn through the end points of the first and last code transition.

- Consider figure DA6:
  - Convince yourselves that  
 $INL_0 = INL_1 = INL_2 = INL_4 = INL_5 = INL_7 = 0 \text{ LSB}$
  - $INL_3 = \frac{3}{8} - \frac{5}{16} = \frac{1}{16} = 0.5 \text{ LSB}$

- Show that  $\text{INL}_6 = -0.5\text{LSB}$
  - Overall INL for an ADC is the max value of INL corresponding to  $\pm 0.5$  LSB
- 
- **Note:**
    - Quantization plot (fig. DA6(b)) gives an indication of the INL performance.
    - INL is the magnitude of the quantization error which lies outside the  $\pm \frac{1}{2}$  LSB band of  $Q_e$ .
    - $Q_e = 1$  LSB  $\rightarrow$   $\text{INL} = 0.5$  LSB
    - $Q_e = -1$  LSB  $\rightarrow$   $\text{INL} = -0.5$  LSB

## General procedure for amplifier analysis

Amplifier analysis has three main steps

Step 1: Find the DC currents and voltages in the amplifier. These voltages and currents are normally referred as biasing values (also known as quiescent values or in relation to transistor output and input characteristics). In order to find the biasing values, one needs to draw DC equivalent circuit for the amplifier. DC equivalent circuit for an amplifier can be obtained by:

- (i) Opening all external capacitors;
- (ii) Disable all AC signals (disable voltage sources by shorting and current sources by opening);
- (iii) For BJT, assume V<sub>BEQ</sub>, base to emitter voltage, of all transistors is about 0.7V if this quiescent value is not given and further assume all transistors are in forward active region (that is  $I_c = \beta I_b$  or  $I_E = (1 + \beta)I_b$ ).  $\beta$  should be given or obtained from the transistor data sheet; You may have base current which is small. This may be neglected in some cases (you need to be careful as it may not be negligible when compared to other currents flowing into the base node). The best way to go about is to find a Thevenin equivalent circuit looking away from the base of the transistor into the biasing voltage or current;
- (iv) For MOSFETs, there is no gate current,  $I_G = 0$ ;  $V_{GS}$  (Gate-Source voltage) and  $I_{DS}$  (Drain-source current (also called drain current,  $I_D$ )) are related by  $I_D = (\frac{1}{2})K_n(W/L)(V_{GS} - V_t)^2$ . This is the direct consequence of the transistors are operating in saturation region. Note that  $V_t$  is a threshold voltage and characteristic of transistor and should be given.
- (v) Apply the circuit analysis techniques (KVL and KCL) to calculate DC voltages and currents in the DC equivalent circuit.

Step 2: Calculate small signal model parameters:  $g_m$ ,  $r_\pi$  and  $r_o$  for BJTs and  $g_m$  and  $r_o$  for MOSFETS. Note that those parameters are DC values dependent (bias dependent or quiescent value dependent). To calculate  $g_m$ ,  $r_\pi$  and  $r_o$  for BJTs, use the following formulas

$$g_m = \frac{I_{CQ}}{V_T}$$

where  $V_T$  is thermal voltage and 26mV at room temperature (Note that it is different from  $V_t$ , threshold voltage for MOSFETs)

$$r_\pi = \frac{\beta}{g_m} \quad \text{and}$$

$$r_o = \frac{V_{CEQ} + V_A}{I_{CQ}}$$

where  $V_A$  is early voltage and often significantly larger than  $V_{CEQ}$

(2)

To calculate and  $g_m$  and  $r_o$  for MOSFETs, use the following formula

$$g_m = K_n \left( \frac{W}{L} \right) (V_{GS} - V_t) \quad \text{and} \quad r_o = \frac{V_D + V_A}{I_{DQ}} = \frac{1}{\lambda I_D}$$

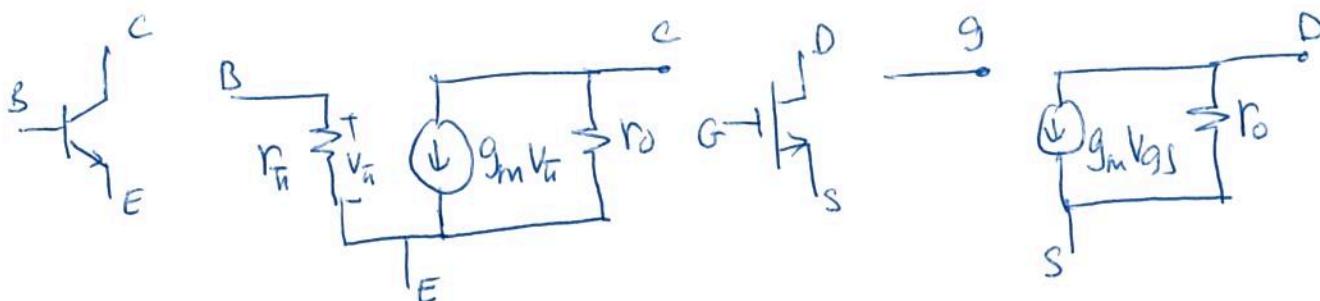
Where  $\lambda$  is modulation factor and characteristic of MOSFET transistor.

Step 3: Draw AC equivalent circuit ( small signal model) of the transistor suitable for low frequency analysis, mid-band frequency analysis and high frequency analysis. Steps in drawing AC equivalent circuit are

- **Low-frequency analysis**

Disable all DC voltage and current sources (Short all DC voltages and open all DC currents). Terminal connected to DC power supply are now at ground.

Replace BJTs and MOSFETs with their equivalent small signal model. At low frequency, the internal capacitors have very large impedances and therefore appear open.



Redraw the circuit with all grounds facing the same direction and isolating all grounds from each other. This should give you somewhat simpler circuit to analyse.

Apply short circuit time constant method to estimate the lower cut-off frequency as follows

$$f_L = \frac{1}{2\pi} \sum_{i=1}^N \frac{1}{\tau_{s/ci}}$$

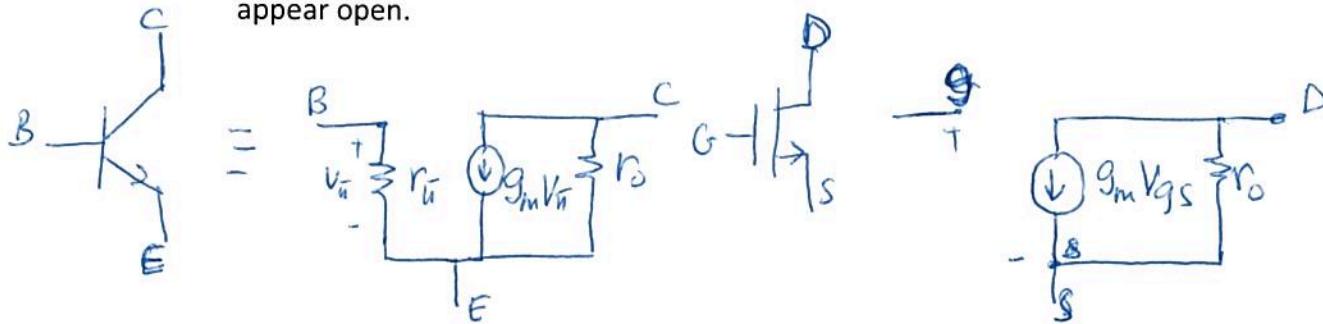
Where  $\tau_{s/ci} = C_i R_{th}$   $R_{th}$  is the Thevenin resistance that  $C_i$  will see across its terminals when all other capacitors are short circuited.  $C_i$  is the  $i^{th}$  external capacitor.

- **Midband frequency analysis**

Disable all DC voltage and current sources (Short all DC voltages and open all DC currents). Terminal connected to DC power supply are now at ground.

Short circuit all external capacitors.

Replace BJTs and MOSFETs with their equivalent small signal model. At midband frequency, the internal capacitors have very large impedances and therefore appear open.



Redraw the circuit with all grounds facing the same direction and isolating all grounds from each other. This should give you somewhat simpler circuit to analyse.

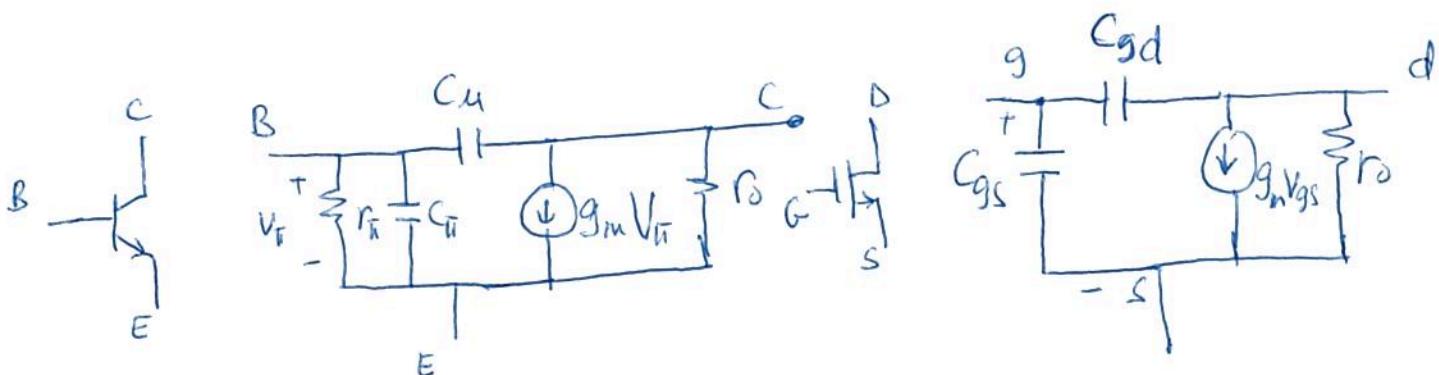
Calculate voltage gain, input and output impedance using the circuit analysis techniques. You will need to practice with this one....

- **High frequency analysis**

Disable all DC voltage and current sources (Short all DC voltages and open all DC currents). Terminal connected to DC power supply are now at ground.

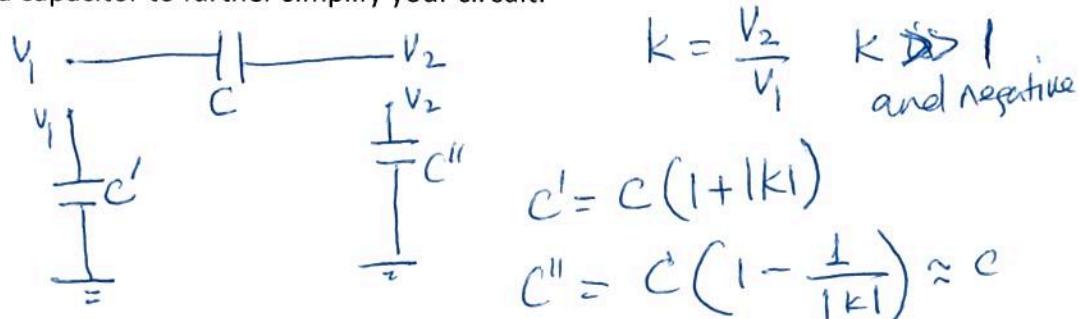
Short circuit all external capacitors

Replace BJTs and MOSFETs with their equivalent small signal model. At high frequency, the internal capacitors become visible and will be included in the small signal model.



Redraw the circuit with all grounds facing the same direction and isolating all grounds from each other. This should give you somewhat simpler circuit to analyse.

You may apply Miller's theorem when there is voltage amplification across the terminals of a capacitor to further simplify your circuit.



Add capacitors in parallel and replace them with one effective capacitor whenever possible.

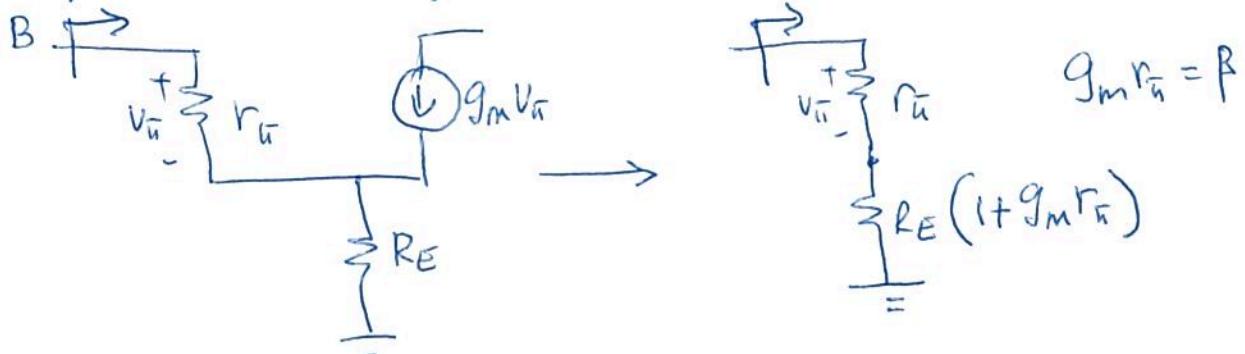
Apply open circuit time constant method to estimate the higher cut-off frequency as follows

$$f_L = \frac{1}{2\pi} \frac{1}{\sum_{i=1}^n \tau_{o/ci}}$$

Where  $\tau_{o/ci} = C_i R_{th}$   $R_{th}$  is the Thevenin resistance that  $C_i$  will see across its terminals when all other capacitors are open circuited.  $C_i$  is internal capacitor.

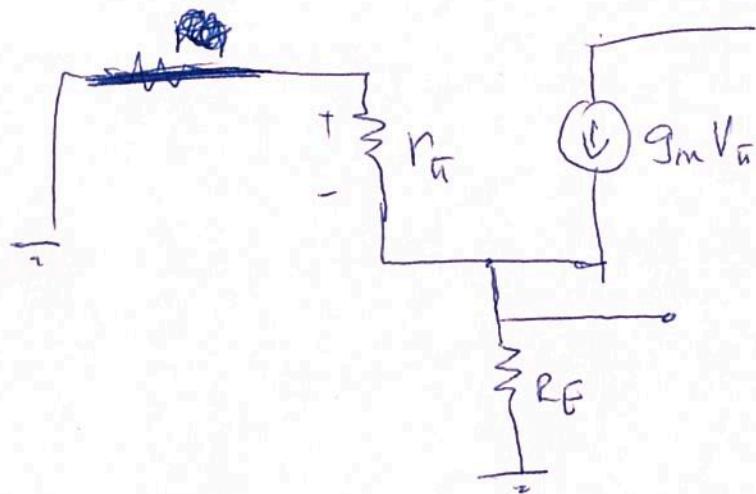
Helpful directions in calculating Thevenin resistances, input and output impedances

Refer resistance from Emitter to base

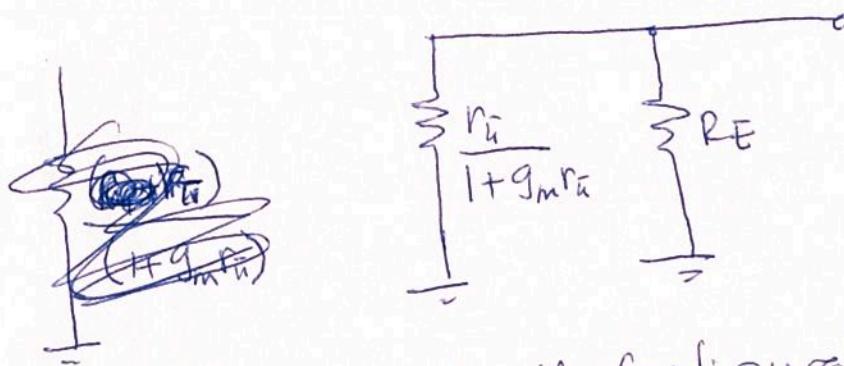


Refer resistance from base to emitter

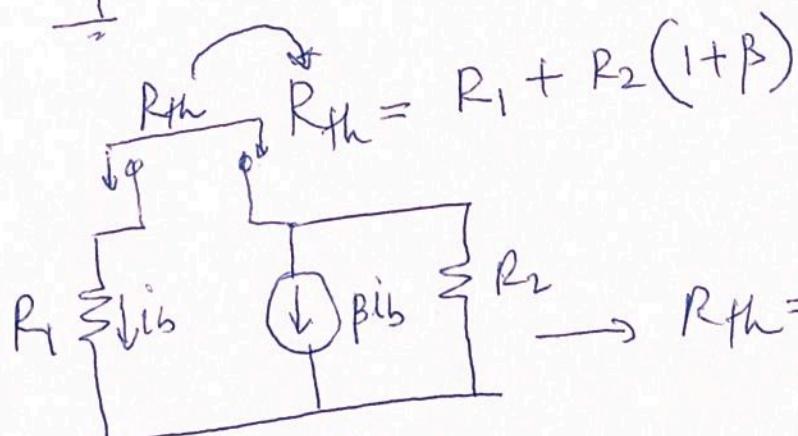
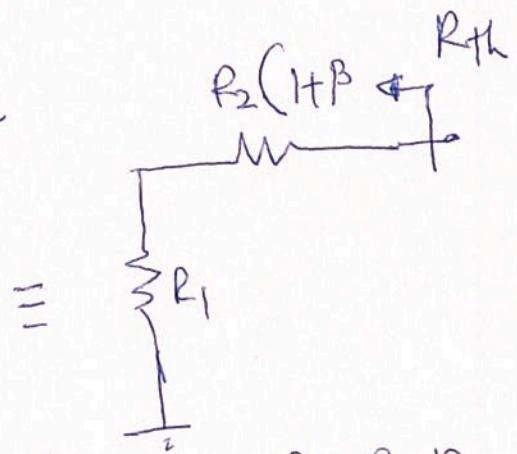
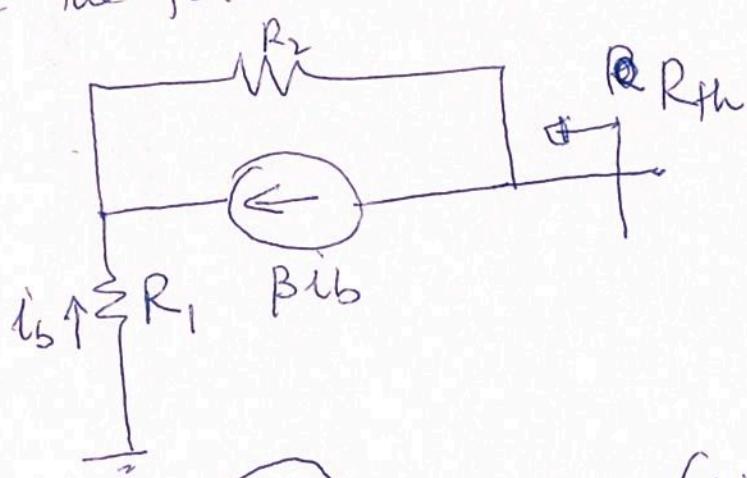
(5)



$\equiv$



Note the following circuit configuration



$$\beta = g_m R_h$$

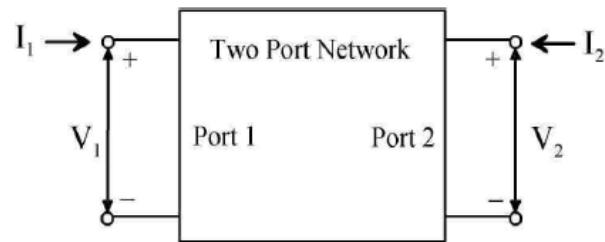
$$R_{th} = R_1 + R_2 (\beta + 1)$$



---

## INFORMATION SHEET

### Two-Port Network Parameters




---

#### **Admittance Parameters**

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$


---

#### **Impedance Parameters**

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$


---

#### **Hybrid Parameters**

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$


---

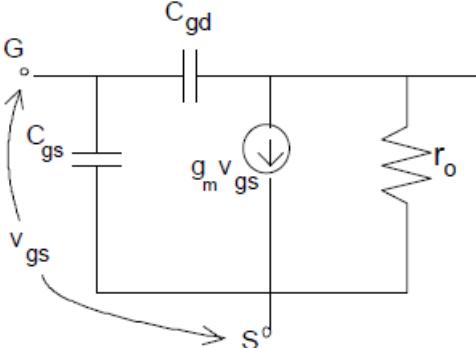
#### **g – Parameters**

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

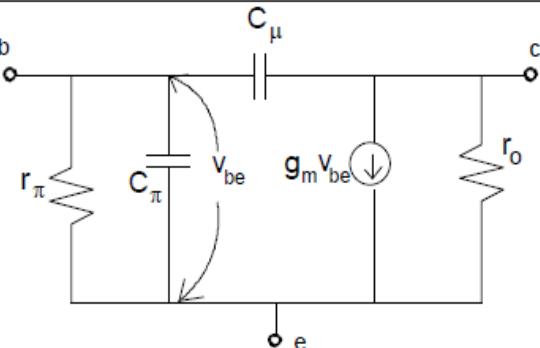

---

## Transistor models and parameters

### Mosfet (n-channel enhancement mode)

$I_d = \frac{1}{2} K_n \frac{W}{L} (V_{gs} - V_t)^2$ where $K_n = 250 \mu A/V^2$ $V_t = 0.6 \text{ volt}$ $r_0 = 100K\Omega$ $C_{gs} = 3.5 \text{ pF}, C_{gd} = 0.1 \text{ pF}$	 Small signal model
--	--

### Bipolar Junction transistor (BJT)

$I_c = I_s \left( e^{\frac{v_{be}}{V_T}} - 1 \right)$ where the thermal voltage at room temperature is $V_T = 26 mV$ Early voltage $V_A = 250V$ $\beta = 100$ $f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ $C_\mu = 0.2 pF$ $f_T = 2 GHz$ $r_o = V_A/I_C$	 Hybrid-pi model ( $r_\mu$ assumed to be very large)
---	---