1. Description

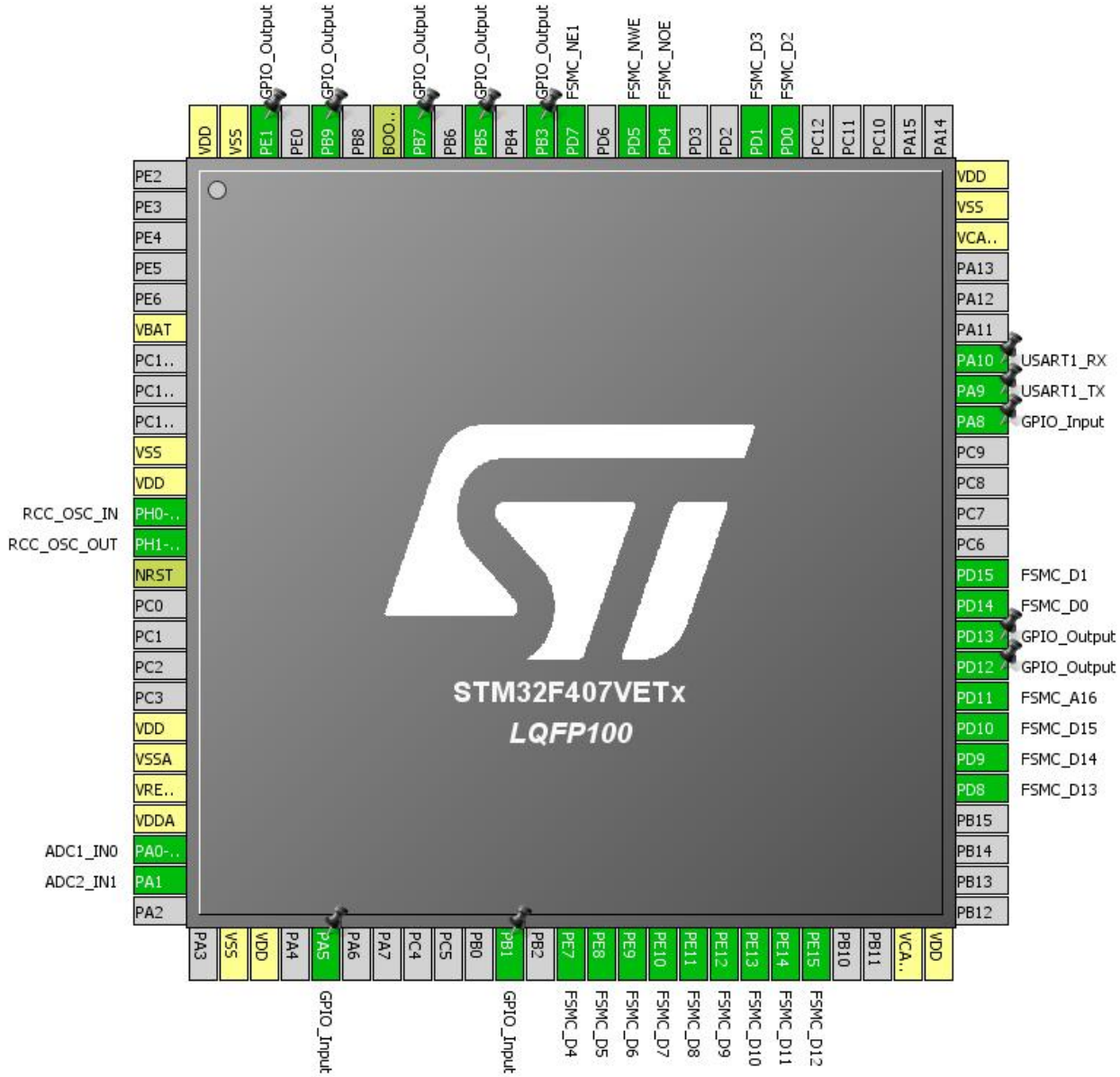
1.1. Project

Project Name	ADC
Board Name	ADC
Generated with:	STM32CubeMX 4.20.1
Date	05/11/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



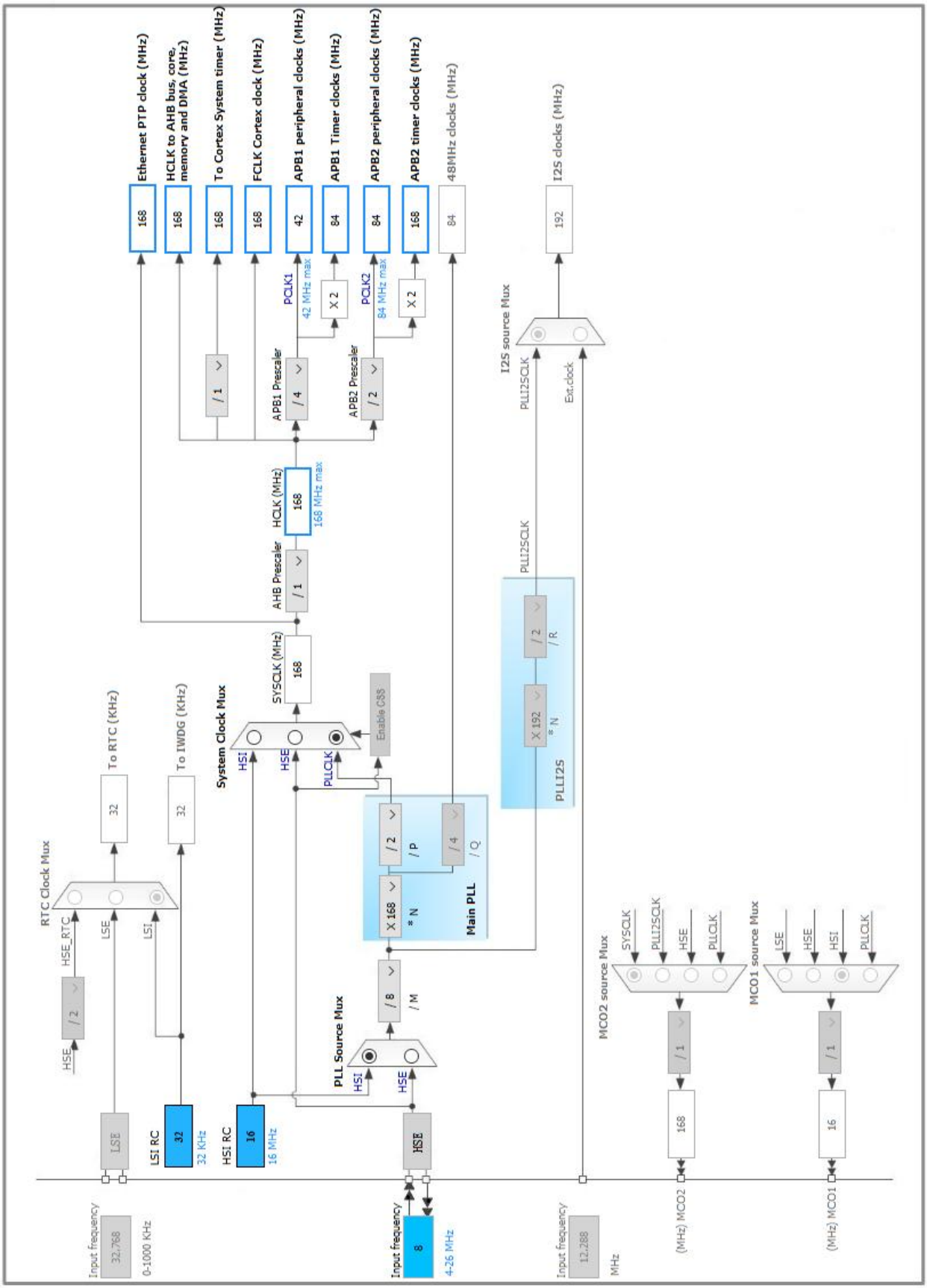
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	
24	PA1	I/O	ADC2_IN1	
27	VSS	Power		
28	VDD	Power		
30	PA5 *	I/O	GPIO_Input	
36	PB1 *	I/O	GPIO_Input	
38	PE7	I/O	FSMC_D4	
39	PE8	I/O	FSMC_D5	
40	PE9	I/O	FSMC_D6	
41	PE10	I/O	FSMC_D7	
42	PE11	I/O	FSMC_D8	
43	PE12	I/O	FSMC_D9	
44	PE13	I/O	FSMC_D10	
45	PE14	I/O	FSMC_D11	
46	PE15	I/O	FSMC_D12	
49	VCAP_1	Power		
50	VDD	Power		
55	PD8	I/O	FSMC_D13	
56	PD9	I/O	FSMC_D14	
57	PD10	I/O	FSMC_D15	
58	PD11	I/O	FSMC_A16	
59	PD12 *	I/O	GPIO_Output	
60	PD13 *	I/O	GPIO_Output	
61	PD14	I/O	FSMC_D0	
62	PD15	I/O	FSMC_D1	
67	PA8 *	I/O	GPIO_Input	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
81	PD0	I/O	FSMC_D2	
82	PD1	I/O	FSMC_D3	
85	PD4	I/O	FSMC_NOE	
86	PD5	I/O	FSMC_NWE	
88	PD7	I/O	FSMC_NE1	
89	PB3 *	I/O	GPIO_Output	
91	PB5 *	I/O	GPIO_Output	
93	PB7 *	I/O	GPIO_Output	
94	BOOT0	Boot		
96	PB9 *	I/O	GPIO_Output	
98	PE1 *	I/O	GPIO_Output	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN1

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: set

Memory type: LCD Interface

LCD Register Select: A16

Data: 16 bits

5.3.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled
Extended mode	**Enabled ***

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15

Data setup time in HCLK clock cycles	**60 ***
Bus turn around time in HCLK clock cycles	15
Access mode	A

NOR/PSRAM timing for write accesses:

Extended address setup time	**3 ***
Extended data setup time	**2 ***
Extended bus turn around time	15
Extended access mode	A

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.5. SYS

Timebase Source: SysTick

5.6. USART1

Mode: Asynchronous

5.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA1	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	
FSMC	PE7	FSMC_D4	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE8	FSMC_D5	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE9	FSMC_D6	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE10	FSMC_D7	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE11	FSMC_D8	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE12	FSMC_D9	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE13	FSMC_D10	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE14	FSMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FSMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FSMC_D13	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD9	FSMC_D14	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD10	FSMC_D15	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD11	FSMC_A16	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD14	FSMC_D0	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD15	FSMC_D1	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD0	FSMC_D2	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD1	FSMC_D3	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD4	FSMC_NOE	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD5	FSMC_NWE	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD7	FSMC_NE1	Alternate Function Push Pull	**Pull-up ***	Very High	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
GPIO	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
USART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	022152_Rev7

7.2. Parameter Selection

Temperature	25
Vdd	3.3

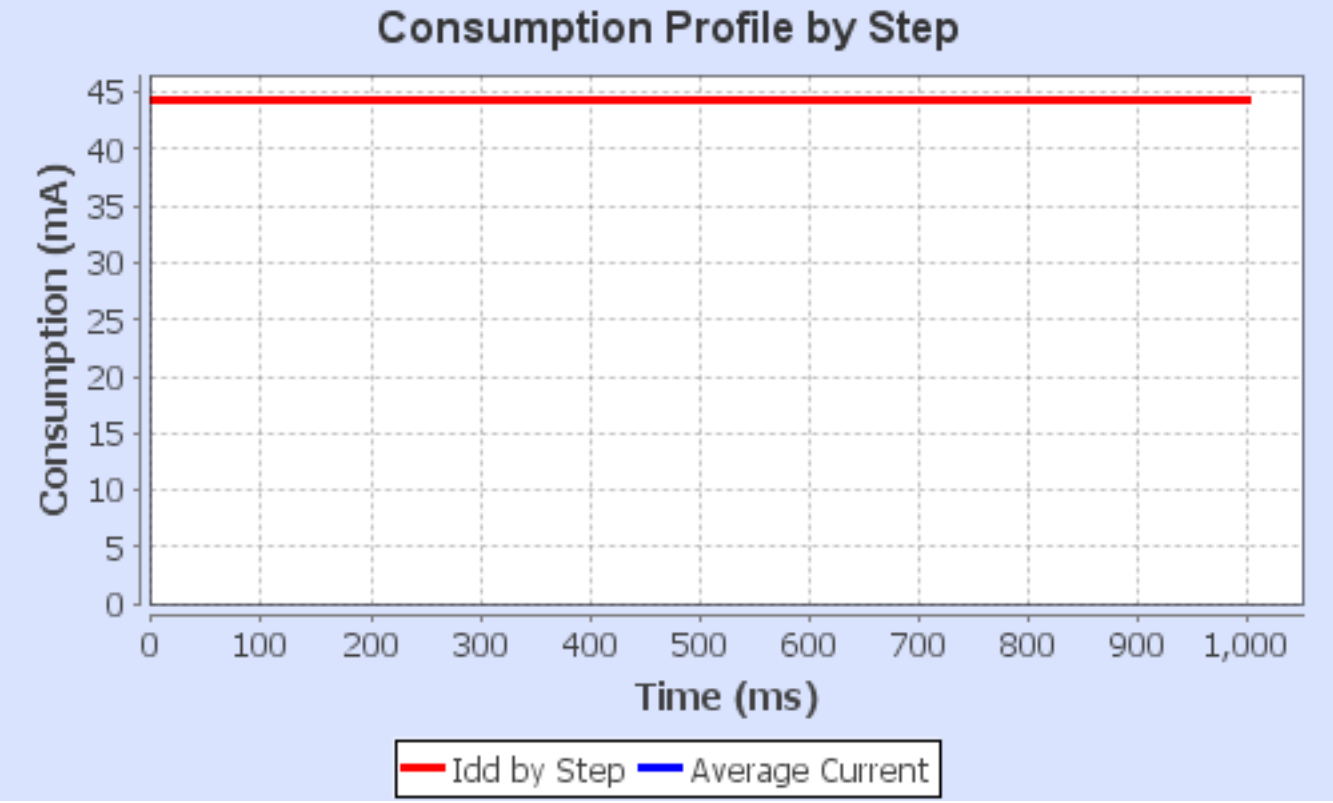
7.3. Sequence

Step	Step1
Mode	RUN
Vdd	3.3
Voltage Source	Battery
Range	Scale1-High
Fetch Type	RAM/FLASH/ART
Clock Configuration	HSE PLL
Clock Source Frequency	4.0 MHz
CPU Frequency	168.0 MHz
Peripherals	FSMC GPIOA GPIOB GPIOD GPIOE GPIOH
Additional Cons.	0 mA
Average Current	44.27 mA
Duration	1 s
DMIPS	210.0
Ta Max	98.72
Category	In DS Table

7.4. RESULTS

Sequence Time	1 s	Average Current	44.27 mA
Battery Life	0	Average DMIPS	210.0 DMIPS

7.5. Chart



8. Software Project

8.1. Project Settings

Name	Value
Project Name	ADC
Project Folder	E:\stm32f4\STM32F4\ADC\ADC
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No