Emerging NVM: A Survey on Architectural Integration and Research Challenges

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There has been a surge of interest in Non-Volatile Memory (NVM) in recent years. With many advantages, such as density and power consumption, NVM is carving out a place in the memory hierarchy and may eventually change our view of computer architecture. Many NVMs have emerged, such as Magnetoresistive random access memory (MRAM), Phase Change random access memory (PCM), Resistive random access memory (ReRAM), and Ferroelectric random access memory (FeRAM), each with its own peculiar properties and specific challenges. The scientific community has carried out a substantial amount of work on integrating those technologies in the memory hierarchy. As many companies are announcing the imminent mass production of NVMs, we think that it is time to have a step back and discuss the body of literature related to NVM integration. This article surveys state-of-the-art work on integrating NVM into the memory hierarchy. Specially, we introduce the four types of NVM, namely, MRAM, PCM, ReRAM, and FeRAM, and investigate different ways of integrating them into the memory hierarchy from the horizontal or vertical perspectives. Here, horizontal integration means that the new memory is placed at the same level as an existing one, while vertical integration means that the new memory is interleaved between two existing levels. In addition, we describe challenges and opportunities with each NVM technique.

CCS Concepts: • **Information systems → Storage class memory**; **Phase change memory**; **Hierarchical storage management**; • **Hardware → Non-volatile memory**; **Memory and dense storage**; • **Software and its engineering → Memory management**;

Additional Key Words and Phrases: Non-volatile memory, MRAM, PCM, FeRAM, ReRAM, storage, main memory

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1 INTRODUCTION

Volume, performance, energy efficiency, and scalability are key factors that designers of memory hierarchies have to deal with to satisfy the ever-increasing need for current data intensive applications.

Volume. The amount of digital data produced today, in different forms, is growing exponentially (Ranganathan 2011; Winter 2008). While for transistor integration, Moore's law gives an impressive example of increasing process, the amount of data being produced is growing at a much faster rate. In a recent study, EMC forecasted growth by a factor of 44 in the amount of digital data created per year from 2009 to 2020. This is mainly due to the growth in the number of devices (and sensors within devices) that generates data—around 11 billion devices are connected to the Internet to date. In fact, applications are becoming more and more data-intensive with the increasing popularity of social networking, video playbacks, and transaction processing, and large memory volumes are needed to store and process the data generated from those activities.

Performance. Efficiently processing the data that are generated has become a major economic and social issue. Better analyzing of data means better results, processes, and decisions. It can help in efforts to generate new ideas and solutions, or in attempts to more accurately predict future events (weather forecasts, disease propagation, etc.). Much effort has been expended to provide more processing power for both the online and offline manipulation of these large amounts of data (Mutlu 2015). However, this is putting a great deal of pressure on the memory hierarchy to bridge the historical gap with the processing elements from the performance point of view.

Energy. In addition to performance and capacity, energy efficiency is a critical metric to consider when designing memory systems. Indeed, one of the most challenging technological innovations for the Exascale computing systems planned for 2020 is the management and optimization of power consumption (Kogge et al. 2008). Data centers in the U.S. consume more than 1.5% of the energy generated in the country, and this ratio is projected to increase annually by 18% (Zhang et al. 2010). A large proportion of this energy is due to memory systems. The energy consumption of storage systems is estimated to comprise between 20% and 40% of the total energy consumption of a typical data center (Carter and Rajamani 2010). Other studies gave different numbers, for instance, a dynamic random access memory (DRAM) main memory subsystem consumes between 30% and 50% of an HPC (High Performance Computing) node, even though this ratio depends on the capacity and configuration of the DRAM (Vetter and Mittal 2015).

Scalability. DRAM technology has undergone impressive improvements in terms of size, capacity, and performance; however, many studies predict that DRAM scaling trends will hit a plateau the next 5 to 10 years. DRAM cells need to be large enough for reliable sensing, but this goes against the trend of shrinking feature sizes. As a consequence, high-density DRAMs impose an exponential cost penalty (e.g., in 2008, using 1 DIMM 8GB cost 212$/GB while 2 × 4GB DIMMS cost 50$/GB, and 4 × 2GB DIMMS cost 15$/GB (Mogul et al. 2009)). DRAM cells also need to be periodically refreshed, thus consuming power even when no read/write operations are performed; such power consumption has been proven to be between 19% and 31% of peak power (Mogul et al. 2009). Other problems related to disturbance issues and reliability for features that are very reduced in size pose great difficulties for future DRAM designs (Yoongu et al. 2014; Vetter and Mittal 2015). Therefore, it is becoming more and more difficult to increase the scaling of charge-based technologies such as DRAM, as well as flash memories (Mutlu 2015).

In this context, emerging non-volatile solid-state memories (NVMs) promise to revolutionize the memory hierarchy. They can provide very high density, almost zero static power consumption, and high endurance. Many emerging NVM technologies are being extensively studied, such as Phase Change Memory (called PRAM or PCM), Resistive Memory (ReRAM), Spin Torque Transfer

Memory (STT-RAM), and Ferroelectric memories (FeRAM). Several companies have announced the imminent mass production of such technologies.

The most popular established NVM is NAND flash memory. It took advantage of the surge in the use of smartphones at the beginning of the 2000s and is now ubiquitous in many applicative domains such as embedded systems and high performance computing. It has become an indispensable technology to partly bridge the gap between DRAM and storage performance.

As with flash memory a decade ago, NVMs are attracting a great deal of interest and much work is being conducted on the issue of how different technologies can be integrated in the memory hierarchy. The numerous announcements from different companies seeking to mass produce NVMs justifies the need to take a step back to discuss and classify the options for integration that have been investigated in state-of-the-art work.

The objective of this survey is threefold: (1) To shed some light on the characteristics of NVMs; (2) To classify state-of-the-art work according to architectural integration options—more precisely, horizontal, or vertical integration. Horizontal integration means that the NVM is put at the same level as an existing memory technology (e.g., in cache with SRAM), while vertical integration means that the new memory is interleaved between two existing levels (e.g., between DRAM and traditional storage devices); (3) To discuss the main challenges involved in making those NVMs ready for use.

There are other recent surveys about emerging NVMs. In Yu and Chen (2016), the authors present a mainly technological and low-level description of different types of NVM. Some other very interesting surveys such as that by Mittal et al. (2015b) are more about a specific level of the memory hierarchy (in this case, about cache), or about the software optimizations that were employed (Mittal and Vetter 2016). Other surveys such as that by Xia et al. (2015) are exhaustive and related to one technology (here, PCM). Different from and complementary to previous surveys, ours focuses on architectural integration issues for four NVM technologies: PCM, MRAM, FeRAM, and ReRAM.[1]

The remainder of the article is organized as follows: Section 2 lays the ground for a discussion of NVM integration. Sections 3, 4, 5, and 6 discuss PCM, MRAM, FeRAM, and ReRAM technologies, respectively. In each section, we define one of these technologies and discuss options for its integration. We will highlight the main issues discussed in some representative research work.

2 BACKGROUND

In this section, we first introduce the memory hierarchy and discuss about integration options. Then, we present the example of flash memory integration, which is considered as the last major disruptive memory technology. We end up this section by introducing NVM properties and integration options.

2.1 Overview on Memory Hierarchy

Memories are a key component of computer systems, and both their function and integration into systems have evolved considerably over time. In effect, a large set of devices and technologies have been developed.

The design of modern computers introduced the first division in the management of memory hierarchy management: a fast memory that supports the high-speed movement of data, which is indispensable for running applications and is called primary or main memory; and a memory used for mass storage. The latter supplies the former, thanks to a lower cost data storage property,

[1] Note that in this survey, Domain Wall Memory (DMW) will not be investigated, and we suggest readers to consult the interesting survey in Mittal (2016).

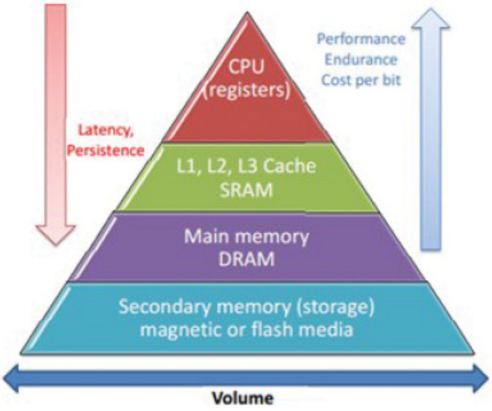


Fig. 1. The memory hierarchy pyramid.

which is called secondary memory or storage memory. This hardware classification of memories has translated into different management policies at the operating system level, as different services manage those memories. Indeed, a specific service manages the primary memory and shares this resource among different application processes, while the storage system is managed as a peripheral, more precisely, as a block device.

The position of a given memory technology in the memory hierarchy pyramid (see Figure 1) reflects the distance to the main processing unit. The better its performance in terms of bandwidth and endurance, the closer it is architected with respect to the processing unit; the poorer its performance, the farther it is architected with respect to the processing unit.

From an architectural point of view, one might think about inserting a given NVM technology in any location within the memory hierarchy pyramid solely according to its characteristics in terms of technology process, bandwidth, and endurance. From a quantitative point of view, the integration would depend on some cost considerations. Generally speaking, the greater the performance of a given memory technology, the higher the cost and the closer to the CPU it is integrated. For instance, an example of integration is under the form of a cache level. SRAM caches are memories that are closer to the CPU.

However, the situation is different from both the applicative and operating system points of view. For instance, from the operating systems perspective, even though many memory components are integrated in a computer, it is mainly the following three that are recognized:

(1) The cache system, which can be activated or deactivated, but for which no explicit management is provided, as the CPU cache is managed by a specific hardware component.
(2) The main memory, which is byte addressable and is managed as a resource with a dedicated service in the operating system. With regard to the latter, the system relies on some hardware components to accelerate its management (for instance, the Translation Lookaside Buffer, TLB).
(3) Finally, the storage system, whether it be a traditional magnetic disk or a flash-based storage drive (Solid State Drive, or SSD). The storage device is a block-addressed device managed as a peripheral from the operating system perspective.

From the architectural point of view, the integration of NVM can be performed **vertically** or **horizontally**.

Vertical integration means that the integrated NVM will shift a given memory technology down in the memory hierarchy and replace it. In this case, the used access method is the same as the one of the replaced memory technology. For instance, in case DRAM is replaced, the NVM is accessed with the same way as DRAM is (from an application level).

Horizontal integration means supplementing a given memory technology in the hierarchy (Vetter and Mittal 2015). In horizontal integration, the newly integrated NVM is interfaced in the same way as the existing memory at the same level. For instance, in case of a horizontal integration within the main memory, some specific application programming interfaces are needed so an application can take benefit of memory heterogeneity. Some standardization organisms such as SNIA already began working on the question throughout the "NVM Programming Model (NPM)" (SNIA 2015). This document claims that this kind of new architecture needs some specific API, but the standard POSIX API is supported as well. This means that a system needs to provide two APIs, one allowing the programmer to be aware of the presence of NVM while the other (standard POSIX) hides the memory heterogeneity.

Whether the integration is horizontal or vertical, hardware (controller) and/or software (operating system and/or applications) components must be aware of the new memory stack for performance optimization reasons.

To fully integrate NVMs, one must consider hardware integration and software integration. The former answers the question about the horizontal or vertical integration and how NVM should interface with the rest of the system, while the latter is related to the system and to application upgrades to make full profit of the additional memory technology.

2.2 Flash Memory, a Pioneer NVM

Flash memory has been a disruptive technology as it has allowed discussions to be raised about the standard storage integration on operating systems, namely the block I/O layer (Bjørling et al. 2013; Ouyang et al. 2011).

Flash memory displays high density, consumes little power when idle, and provides faster access time than HDD, especially for random reads. But to be efficiently integrated in a given storage system, one must take into consideration its peculiarities: read/write performance asymmetry, a limited lifetime, write/erase operations granularity asymmetry, and so on.

2.1.1 Flash Memory Integration. Flash memory can be integrated into storage servers in three ways (Roberts et al. 2009; Boukhobza 2013): (1) as an extension of the memory system (horizontal integration), (2) as a storage accelerator where flash is managed as a cache storing frequently accessed code and data and so reducing the number of I/Os to HDD (vertical integration), or (3) as an alternative storage device where flash SSDs are used as a replacement or to complement HDDs (horizontal integration again). Of the above three options, two are horizontal integrations but are placed at two different levels: main or secondary memory. From the applicative point of view, in the case where flash is integrated with DRAM, the integration is transparent to the applications as the flash memory is managed through dedicated hardware to supplement DRAM (e.g., NVDIMM (Huang and Jiang 2014; Chen et al. 2016)). In the second case of horizontal integration, the flash memory is revealed to the rest of the system through a traditional storage system interface and is thus accessed like an HDD through standard file system interfaces. Flash memory has also been integrated through a PCIe interface, allowing more room for performance enhancement by making use of internal parallelism that can be achieved with multi-channel and other multi-die, and plane parallelism. This integration through PCIe can be storage stack compliant and thus seen as a storage device, or non-compliant and thus needing some specific driver and software tools to be accessed by applications. The objective of the latter is to get rid of traditional storage stack latencies through specialized software.

Because of cost considerations (flash is roughly one order of magnitude more expensive than HDDs), flash-based storage systems will not replace disk systems in the medium term (Gurumurthi 2009). Thus, disk storage systems are not about to disappear from the memory hierarchy.

2.1.2 Flash Memory Properties and Management. As compared to traditional magnetic storage systems, NAND flash memories have some peculiar characteristics that have pushed the scientific community to design specific solutions for their integration (both horizontal and vertical). Here is a set of flash memory characteristics taken from (Boukhobza 2013; Boukhobza and Olivier 2017):

—**Random reads**: Flash memories are entirely electronic-based components with no moving mechanical parts. Contrary to HDDs, read access latency no longer depends on the physical location of data, so random reads perform as well as sequential ones. This makes flash memories more efficient and predictable for read operations as compared to traditional HDDs. The poor performance of HDDs in cases of random access has led to the implementation of many mechanisms at the operating system level to try to minimize this performance gap: I/O scheduler, page cache, and others. At the user layer, many applications also suppose an underlying HDD and thus try to maximize sequential requests while minimizing random ones such as database management systems (e.g., sorting algorithms), and big data applications (e.g., MapReduce). In the case of flash memory integration, those mechanisms were revisited to take full advantage of flash memory performance and the scientific community has made significant contributions toward this end.

—**I/O performance asymmetry**: Another specificity of flash memories is that, unlike HDDs, reads are generally much faster than writes. This is mainly due to the electrical properties of the basic flash memory cell; it takes more time to program the cell to reach a stable state than simply to read it. Many flash-specific buffer system mechanisms have been designed to absorb write operations and so increase the performance.

—**Sequential writes in a block**: To avoid write errors (due to some electrical disturbance properties), writes must be performed sequentially within one block, especially for MLC (Multi Level Cell) technology. Error correction codes (ECC) are implemented in hardware to cope with such errors.

—**Low power consumption**: Even though the power consumption of flash-based storage systems depends on its internal architecture and on the applied workload (Park et al. 2011), it remains more energy efficient than HDDs. As the roadmap of high performance computing integrates more and more constraints on energy efficiency, such a storage system technology will be more sought after than ever.

—**I/O interface**: To ease the adoption of flash memory, the integration of SSD as a replacement technology relies on the use of I/O interfaces similar to HDDs. This characteristic can be considered an advantage from the point of view of the user, as no modifications to the operating system are required (with the exception of drivers). However, this may give the illusion that one must deal with flash memories in the same way as with HDDs, which is far from true.

—**Shock resistance**: This characteristic is yet another consequence of the absence of mechanical parts.

A given set of constraints must be dealt with when designing flash-based solutions. These constraints can be summarized as follows:

—**Erase-before-write limitation:** This is one of the most critical constraints on flash memories. One cannot directly overwrite data. This constraint means that if the data of a given page need to be modified in-place, then the whole block should first be erased (see the previous constraint). This is time consuming; thus, data are generally updated out of place (after invalidating the old data) via a **mapping scheme**. This mapping scheme has a strong impact on the performance of the SSD. In addition to the mapping scheme, a flash memory controller must implement a **garbage collector** to recycle previously invalidated data.

- **Write/Erase granularity asymmetry**: Writes are performed on pages, while erase operations are realized on blocks. Flash memory blocks are composed of a given number of pages of a size between 2 and 8 KB (powers of 2).
- **Limited number of Erase/Write cycles**: The average number of write/erase (W/E) cycles is approximately 10^5 for a single level cell (SLC), 10^4 for a multi-level cell (MLC), and 5000 for a triple level cell (TLC). After the maximum number of erase cycles is reached, a given memory cell may no longer retain data. Due to this constraint on endurance, flash memory controllers implement **wear leveling techniques** to balance the wear out of the flash memory blocks.

Therefore, to be integrated with a traditional storage interface (just like an HDD), a flash memory controller should implement at least the three abovementioned services: a mapping scheme, a garbage collector, and a wear leveler. Those mechanisms have a very strong impact on performance.

2.3 NVM, Why and How?

From the architectural and system points of view, a new NVM can be inserted in the memory hierarchy in one of the three main subclasses of memory: processor caches, main memory, or storage systems. NVMs can be vertically or horizontally integrated.

2.2.1 As a Storage System. From the storage system point of view, NVM can be integrated horizontally. Therefore, similar to the flash memory, some constraint management mechanisms should be implemented and abstracted to higher levels so the new NVM-based storage system can be integrated in the traditional storage software stack. NVM can also be integrated vertically such as PCIe-based flash devices. Another possibility is to have some hybrid devices such as HDDs integrate flash memories, but this time with NVM technologies other than flash.

2.2.2 As a Main Memory. As many NVM technologies have very appealing performance characteristics (see Table 1), they can be integrated into a higher level in the memory hierarchy than the storage system. NVMs have some peculiar characteristics, such as a read performance that is higher than the write performance, an endurance that varies according to the technology and that is more impacted by write operations than by read operations, and the fact that most NVMs use only power when accessed. All of these characteristics must be dealt with and some new services must be included when integrating NVM as DRAM or next to DRAM to have some hybrid main memory.

Again, NVM can be integrated vertically with DRAM or horizontally (Li et al. 2012). In the first case, DRAM can be regarded as a cache for the NVM to reduce the access latency to the primary memory. NVM can also be integrated horizontally on the same bus as the memory. Data placement issues could be managed by hardware and thus abstracted to the operating system, or managed by the operating system and abstracted to the application. Finally, some interface could be made available to the application by the operating system, to facilitate decisions on placements at the applicative layer. In such cases, operating system support is a critical issue when dealing with memory heterogeneity.

Table 1. Characteristics of NVMs According to State-of-the-art Studies[2] (Vetter and Mittal 2015; Mittal et al. 2015b; Xia et al. 2015; Wang et al. 2014a; Suresh et al. 2014; Baek et al. 2013; Meena et al. 2014)

	SRAM	DRAM	HDD	NAND flash	STT-RAM	ReRAM	PCM	FeRAM
Cell size (F^2)	120–200	60–100	N/A	4–6	6–50	4–10	4–12	6–40
Write Endurance	10^{16}	$>10^{15}$	$>10^{15}$ (pb: mechanical parts)	10^4–10^5	10^{12}–10^{15}	10^8–10^{11}	10^8–10^9	10^{14}–10^{15}
Read Latency	~0.2–2ns	~10ns	3–5ms	15–35μs	2–35ns	~10ns	20–60ns	20–80ns
Write Latency	~0.2–2ns	~10ns	3–5ms	200–500μs	3–50ns	~50ns	20–150ns	50–75ns
Leakage Power	High	Medium	(Mechanical parts)	Low	Low	Low	Low	Low
Dynamic Energy (R/W)	Low	Medium	(Mechanical parts)	Low	Low/High	Low/High	Medium/ High	Low/High
Maturity	Mature	Mature	Mature	Mature	Test chips	Test chips	Test chips	Manufactured

2.2.3 As a Processor Cache. From the CPU cache perspective, the first-level cache is generally accessed at a high frequency, so very low latency and high endurance is required. This is hard to achieve with most NVMs, even if some of them can be considered candidates for such integration. On the other hand, last-level caches are designed more to reduce off-chip data movements and thus must have high density (to achieve large capacity). NVMs integrated in CPU caches are intended more for use in the last-level cache than in other levels of cache (Mittal et al. 2015b). However, even in this case, NVMs will absorb very large amounts of write operations, so issues of wear must be mitigated. In addition, the compatibility of the technology with the fabrication process is also a very important issue.

Table 2 summarizes state-of-the-art work on the NVM integration with regard to the memory hierarchy. As previously discussed, NVM can be integrated horizontally with some other technology; in this case some data migration mechanisms need to be provided whether at the hardware, operating system, or applicative level. NVM can be integrated vertically by shifting another memory down, or it can replace an existing memory technology. In Table 2, in the case of the processor cache, the line "replacement" lists studies where all of the levels of cache have been replaced by an NVM.

It should be noted in Table 2 that the most studied options are the vertical integration of MRAM in processor caches and the horizontal integration of PCM in main memory, with those two technologies being the most investigated in state-of-the-art work.

Note that for many studies related to PCM (or ReRAM), the proposed mechanisms can also work for ReRAM (or PCM).

In the rest of the article, we will investigate each of the following NVMs: PCM, MRAM, FeRAM, and ReRAM, and their integration.

3 PCM

As one can observe in Table 1, phase change memory (PCM), also called phase change random access memory (PRAM), has small-sized cells and excellent scalability within the CMOS fabrication process, relatively fast random access, a moderate write throughput, a good retention time, very

[2] The values are not strict values, but give an overall idea of the characteristics.

Table 2. Classification of State-of-the-art Studies about NVM Integration

		MRAM	ReRAM	PCM	FeRAM
Cache (different levels)	Horizontal	(Oboril et al. 2015; Li et al. 2012; Syu et al. 2013; Li et al. 2014; Wu et al. 2009; Jadidi et al. 2011; Li et al. 2011; Wang et al. 2014 ; Komalan et al. 2014; Cheng et al. 2016)	(Wang et al. 2014a; Komalan et al. 2013; Mittal and Vetter 2015)	(Wu et al. 2009; Joo et al. 2010)	
	Vertical	(Oboril et al. 2015; Senni et al. 2014; Sun et al. 2009; Wu et al. 2009; Samavatian et al. 2014; Smullen et al. 2011; Jog et al. 2012; Zhou et al. 2009b; Goswami et al. 2013; Yazdanshenas et al. 2014; Ahn et al. 2012; Rasquinha et al. 2010; Park et al. 2012; Chen et al. 2013; Kwon et al. 2014; Jokar et al. 2016; Senni et al. 2015; Cheng et al. 2016)	(Dong et al. 2013; Wang et al. 2013; Jokar et al. 2016)	(Wu et al. 2009)	
	Replacement	(Oboril et al. 2015; Smullen et al. 2011; Sun et al. 2011; Guo et al. 2010; Goswami et al. 2013; Wang et al. 2015)	(Dong et al. 2013)		
Main Memory	Horizontal	(Yang et al. 2013; Suresh et al. 2014; Wei et al. 2015)	(Hassan et al. 2015; Wei et al. 2015)	(Dhiman et al. 2009; Park et al. 2010; Bock et al. 2011; Suresh et al. 2014; Zhou et al. 2009a; Sun et al. 2015; Wei et al. 2015; Lee et al. 2014; Salkhordeh and Asadi 2016; Wei et al. 2015; Kannan et al. 2016; Dulloor et al. 2016; Wu et al. 2016 ; Li et al. 2012 ; Oikawa 2014; Gao et al. 2015)	(Doh et al. 2007; Suresh et al. 2014)
	Vertical	(Suresh et al. 2014)		(Qureshi and Srinivasan 2009; Suresh et al. 2014; Awad et al. 2016; Wu et al. 2016)	(Suresh et al. 2014; Jung et al. 2010)
	Replacement	(Kultursay et al. 2013; Wang et al. 2014; Jin et al. 2014)	(Xu et al. 2013 ; Xu et al. 2015)	(Lee et al. 2009; Chen et al. 2012; Park et al. 2015)	(Baek et al. 2013)
Storage	Horizontal	(Lee et al. 2014)	(Tanakamaru et al. 2014; Sun et al. 2014; Fujii et al. 2012)	(Sun et al. 2010; Caulfield et al. 2010; Park et al. 2010)	(Yoon et al. 2008)
	Vertical	(Kang et al. 2015)		(Liu et al. 2011 ; Kang et al. 2015)	
	Replacement	(Lee et al. 2014)	(Jung et al. 2013)	(Akel et al. 2011; Kim et al. 2014)	(Baek et al. 2013)

good endurance as compared to NAND flash, and erase-less programming (no need for an erase operation to update data) (Qureshi et al. 2011).

3.1 Basic Concepts

3.1.1 PCM Technology. PCM uses a chalcogenide alloy to implement a memory cell. A PCM cell usually uses a thin layer of chalcogenide such as Ge2Sb2Te5 (GST) (Xue et al. 2011) and two

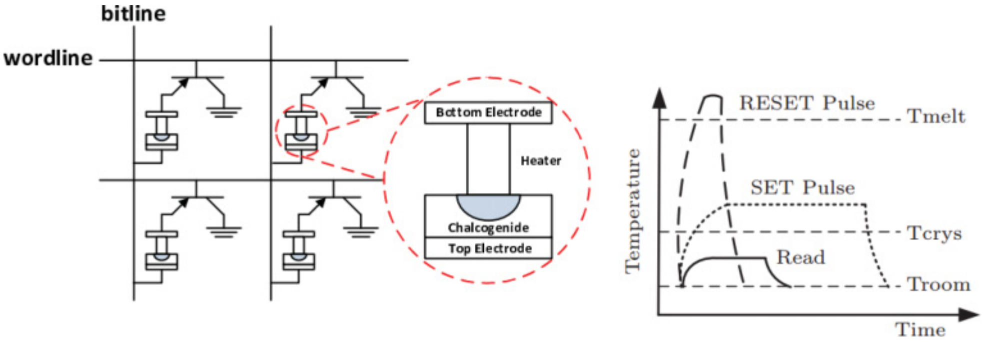


Fig. 2. PCM cell array (Xue et al. 2011) and RESET/SET temperatures (Xia et al. 2015).

electrodes that wrap the chalcogenide on both sides, in addition to a heater (see Figure 2). PCM is a resistive NVM that utilizes different resistances to represent bit information.

This chalcogenide material is subject to rapid amorphous-to-crystalline phase-change process that is electrically initiated.

The phase is dependent upon the heat produced by an electrical current pulse. A short but high voltage pulse results in an amorphous state (RESET, bit to 0), where the GST is heated above the melting temperature (T_{melt} in Figure 2). On the other hand, a long pulse with a low voltage results in a crystalline state (SET, bit to 1). Here the GST is heated above the crystallization temperature (T_{crys}) but below the melting temperature (see Figure 2). The write performance is thus determined by the longer operation that is the SET. Once a phase has been established, it may be read without disturbing this phase; the ratio between the resistance of the material in a SET and a RESET phase is between 10^2 and 10^4 (Kim 2008).

Thanks to a large difference between the two state resistance values, it is possible to store multiple bits (Multi-Level Cells) by making use of intermediate resistive values, thus increasing the storage density of PCM. Several state-of-the-art studies reported 3 bits per cell density (Wu et al. 2015). However, due to material composition fluctuation, the storage of the intermediate values needs an iterative Program-and-Verify process that is based on few SET operations until the target resistance value is reached (Jiang 2014).

3.1.2 Write Endurance. The main issue with PCM is the write endurance, as a PCM cell can only sustain a limited number of write operations (generally 10^8). This is mainly due to repeated heat stress applied on phase change material. Indeed, thermal expansion and contraction degrades the electrode-storage contact, which leads to a decrease in the reliability of writing currents in the cell. However, the endurance of PCM is better than that of flash memory (around 10^5 cycles), but worse than that of DRAM (10^{15}). This property is crucial when deciding on the integration of such a technology into the memory hierarchy.

Another issue regarding the write endurance of PCM is related to the RESET optimal current. State-of-the-art studies have confirmed that using current values above the optimal value leads to quick degradation of the memory cell, thus decreasing its endurance. As mentioned in Xue et al. (2011) and Kim and Ahn (2005), a twofold increase in the write energy leads to an approximately 50-fold decrease in the endurance.

3.2 Integration Options

The write characteristics of PCM narrow the scope of its use in different levels of the memory hierarchy. The write endurance and high write latency are the main issues, as they do not allow,

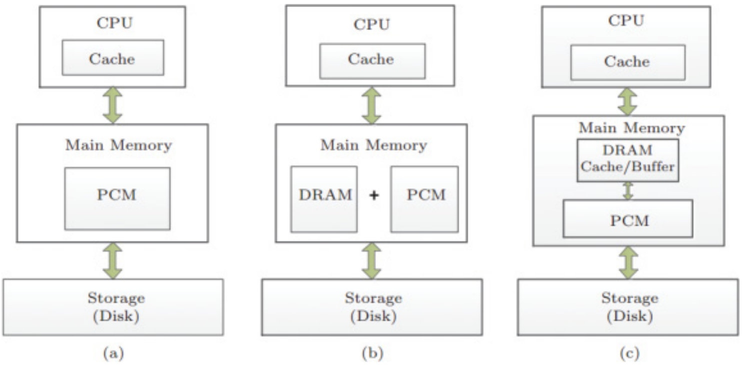


Fig. 3. Three PCM integration options (Xia et al. 2015).

for instance, for an integration in the first levels of the processor cache as the write traffic is very heavy (Mittal et al. 2015b). In state-of-the-art work, the main integration possibilities are as a main memory or as a storage system. In both cases, the PCM can be integrated vertically or horizontally.

3.2.1 PCM in Main Memory. There are three integration possibilities for PCM as a main memory: (1) as a replacement of the DRAM, (2) horizontally at the same level as the DRAM, (3) vertically with the DRAM.

Figure 3 shows the different integration options. When the DRAM and PCM are placed at the same level, the placement of data according to the access pattern is achieved by the application (for instance, through a specific API such as in Kannan et al. (2016)), at the operating system level (Lee et al. 2014; Salkhordeh and Asadi 2016; Wei et al. 2015), or at the memory controller level (Dhiman et al. 2009; Qureshi and Srinivasan 2009; Lee et al. 2009). In fact, the main objectives would be to hide the high latency of the write operations by moving write intensive workloads/data on DRAM and to rely on the non-volatility of PCM to save energy (Dhiman et al. 2009; Sun et al. 2015). In Wei et al. (2015), for instance, the authors use the NVM space to store file system meta data. Their system, called FSMAC, decouples the data and meta data I/O flow from the file system level and up to the hardware, which allows for a high-performance gain. PCM is also used in main memory for checkpointing (Oikawa 2014; Gao et al. 2015) and fault tolerance issues (Li et al. 2012).

In the case where DRAM is integrated as a cache for PCM, its objective is to absorb write operations to reduce the overall write latency and to address the problem of the write endurance of the PCM. Indeed, some experimental results (Qureshi and Srinivasan 2009) have shown that, with regard to memory, given a small DRAM buffer (3% of the PCM) a threefold improvement in speed can be achieved, as well as a three-fold extension in lifetime. Of course, performance depends on the write patterns. (Awad et al. 2016) emphasized the high impact of operating system mechanisms such as page prefetching and page replacement policies, on such PCM integration. Employing both horizontal and vertical integration, (Wu et al. 2016) used a small portion of DRAM to accelerate access to the NVM, while placing another portion horizontally in PCM.

Park et al. (2015) chose option (a) of Figure 3; they replaced the DRAM with PCM while trying to optimize the use of row buffers for an LPDDR2 interface integration.

3.2.2 PCM in Storage Systems. As compared to NAND flash memory, PCM has the ability to perform byte-wise random access and direct in-place updates; this makes it a serious competitor to flash memories.

PCM-based storage systems have already been prototyped. For instance, Onyx (Akel et al. 2011) is a PCM-based storage array interfaced in PCIe that has been proven to have better performance than state-of-the-art SSDs for some specific workload patterns (irregular and read dominated).

Many studies have focused on the vertical integration of PCM within storage systems. For instance, in Sun et al. (2010), PCM was used and integrated in solid state storage with flash memory to absorb log updates, similar to a cache. The objectives were (1) to relieve the flash memory from bursts of updates, which decreases performance and affects endurance; (2) to improve performance, as PCM allows in-place updates; and (3) to save energy, as PCM is more energy efficient than DRAM. Other studies used the same principle of using PCM inside SSDs to supplement or replace DRAM (Liu et al. 2011) with the objective of optimizing performance and avoiding loss of data from the SSD cache due to power failures, with the help of PCM non-volatility.

According to state-of-the-art studies and prototypes, PCM-based storage systems show great promise, as they can drastically reduce latencies and increase the bandwidth of storage systems for high performance I/O intensive computing (Caulfield et al. 2010).

How to architect this type of NVM to take full advantage of its performance is a critical issue. Many of the prototype storage systems are based on PCIe, and the authors claim that this interface can be a bottleneck as it can limit the achievable performance (in terms of latency, for instance).

From an operating system perspective, many layers of the storage system software stack were devised with HDD in mind, so some micro seconds of latency can be tolerated. This is no longer the case, and efforts need to be expended to adapt the storage software stack to the new coming NVMs (Lee et al. 2014). Many questions need to be answered, such as what to abstract to the OS from the underlying hybrid architecture, how to interface the different storage systems, and which protocol/mechanisms should be used. Towards that end, some propositions have been made, for instance, in Park et al. (2010) the authors proposed two possible integrations of PCM in the Linux operating system:

1. Having both DRAM and PCM in main memory and performing data placement according to the I/O type. This would allow large amounts of energy to be saved as compared to full DRAM implementation. Page placement is performed according to the segmentation of the executed processes.
2. As complementary storage with traditional storage systems. Here, data placement is based on putting small-sized random accessed data in the PCM.

This study presents a concrete solution on how to interface hybrid memory systems on Linux.

3.3 Open Research Questions

Xia et al. (2015) observed that many optimization issues have been discussed in the literature, with the aim of making this technology viable in different systems. The main issues deal with optimizing the write latency so PCM can be used in place of DRAM, optimizing the endurance, and saving energy.

3.3.1 Optimizing the Write Latency. As the write latency is due to some physical properties of the phase change material, the optimizations should be performed at other levels.

Indeed, the first optimization technique consists of optimizing the write command latency. Many options are possible such as: (1) Reducing the write bits: this solution consists of writing only modified bits (Zhou et al. 2009a; Yang et al. 2007; Dong et al. 2015); (2) increasing the level of parallelism of the writing bits by making better use of the SET and RESET operation properties (Yue et al. 2013a; Du et al. 2013); (3) hiding the write latency for read operation optimization: this is achieved, for instance, by pausing long write operations when a read operation arrives, and then resuming the write once the read is achieved (Qureshi et al. 2010).

3.3.2 Optimizing the Endurance. One of the main issues regarding PCM as a DRAM replacement is the write endurance, which is due to the continuous heating of the phase change material. Many techniques have been proposed to cope with this problem.

Solutions for optimizing the endurance can be grouped into three subclasses: (1) Improving the endurance by acting on the electrical characteristics, such as by targeting an optimal RESET current because over-programming, has a very bad impact on endurance. For instance, in Jiang et al. (2012) the authors proposed an elastic RESET, which reduces the RESET current, thus positively impacting the memory lifetime. (2) The second option consists of minimizing the number of write operations; this can be achieved by inserting a DRAM buffer that absorbs frequent writes. Other solutions were proposed, such as avoiding the writing of unmodified memory bits (Lee et al. 2009; Zhou et al. 2009a; Yang et al. 2007) or even avoiding the writing of useless data from the cache (Bock et al. 2011). Other techniques were also explored, such as data compression (Sun et al. 2011). (3) Finally, global PCM endurance can be improved through wear leveling techniques. There are two main classes of wear leveler: wear levelers that rely on memory block states, for example, switching hot (frequently updated) and cold data (Zhou et al. 2009a; Yun et al. 2012); and wear levelers that randomly swap data independently from their access pattern, for example, those that do so periodically, such as in Zhou et al. 2009a; Qureshi and Srinivasan (2009).

3.3.3 Write Disturbance. PCM is subject to write disturbance when the inter-cell distance is too small. The high temperature produced by a RESET operation can lead to a phase change in adjacent cells by thermal conduction. This may induce parasitic SET operations (Russo et al. 2008). This effect could limit the technology scaling under 20 nm. The state-of-the-art solutions include imposing a minimal inter-cell space, and designing write strategies and data coding techniques to avoid write disturbance (Jiang et al. 2014; Wang et al. 2015b; Wang et al. 2015c).

3.3.4 Energy Saving. One of the key arguments in favor of NVMs as a replacement or complement to DRAM concerns their energy behavior. Indeed, the static energy is negligible. Unfortunately, PCM demonstrates very high write energy (higher than DRAM). Many techniques have been proposed to address this problem.

There are two main ways of reducing the energy consumption of write operations: (1) reducing the number of writes and (2) reducing the energy consumption of write operations. The techniques cited previously and which consist of avoiding the updating of all bits, avoiding unnecessary writes, and so on, not only reduce write latency, but also the energy consumption of write operations. As for the second class of solutions, they mainly consist of exploiting the write asymmetry (SET and RESET) (Xu et al. 2009; Mirhoseini et al. 2012; Chen et al. 2012; Yue et al. Zhu 2013b) to reduce energy, as the RESET operation consumes more energy than the SET operation (Xia et al. 2015).

In MLC PCM, writing of a cell line begins with a RESET operation followed by a variable number of SET operations. This number depends on the values to store (P&V process). In Jiang (2014), the authors propose to schedule RESET operations among different cells at different times to reduce the size of charge pumps that supply the RESET operation energy. By reducing their sizes, the wasted power can be reduced. This optimization relies on the fact that the number of SET operations to perform might be different according to the target value. As a consequence, some RESET operations can be easily shifted in time with no impact on the cell line write operation duration.

3.4 PCM Maturity and the State of the Market

Many companies have put a great deal of effort into making PCM available in the market. In August 2004, Nanochip licensed PCM technology for use in MEMS (Micro-Electric-Mechanical-Systems) probe storage devices. In September 2006, Samsung announced a prototype device with 512Mb size using diode switches. The fairly high density is notable. The prototype featured a cell size of only 46.7nm, smaller than commercial flash devices available at that time. In comparison, the only MRAM and FeRAM devices being produced at the time were about 4Mb in size. The high density of Samsung's prototype PCM device suggested that PCM could be a viable competitor to flash, not limited to niche roles as other devices have been (Athmanathan et al. 2016).

Samsung's announcement was followed by announcements from Intel and STMicroelectronics, who demonstrated their own PCM devices in 2006 (at the Intel Developer Forum). They came up with a 128Mb device that STMicroelectronics began manufacturing as a proof-of-concept. In February 2008, Intel and STMicroelectronics revealed the first multi-level (MLC) PCM array prototype. The prototype had two logical bits stored in each physical cell; in effect, 256Mb of memory were stored in a 128Mb physical array. This means that instead of the normal two states, fully amorphous and fully crystalline, an additional two distinct intermediate states represent different degrees of partial crystallization, allowing for twice as many bits to be stored in the same physical area.

In June 2011, IBM announced that they had created a stable, reliable, multi-bit PCM with high performance and stability. Also in February 2008, Intel and STMicroelectronics shipped prototype samples of their first PCM product—a 90nm, 128Mb product that they called Alverstone.

In April 2010, Numonyx announced the Omneo line of 128Mbit NOR-compatible phase-change memories, while Samsung announced that a 512Mb PCM in a multi-chip package (MCP) would be used in mobile handsets shipped by the fall of 2010. In July 2012, Micron announced the availability of PCM for mobile devices, the first PCM solution in production. However, Micron withdrew all PCM parts from the market in January 2014. In 2016, IBM demonstrated that they could store two bits per cell, and were on their way to achieving three bits per cell (Athmanathan et al. 2016).

4 MRAM

One of the more mature and promising NVMs is Magnetic or Magnetoresistive RAM (MRAM), which has the following very attractive properties: high density, fast read, low leakage, and high endurance (see Table 1 for the STT-RAM variant of MRAM).

4.1 Basic Concepts

4.1.1 MRAM Technology. MRAM are based on the magnetic properties of a special material. Contrary to standard DRAM technologies, the information carrier is the Magnetic Tunnel Junction (MTJ) instead of electrical charges. Magnetic orientation can be controlled and sensed using electrical signals (Kultursay et al. 2013).

The MTJ implements the storage function. It consists of two ferromagnetic layers separated by an oxide (tunnel) barrier layer. One of the ferromagnetic layers has a fixed direction of magnetization and is called the *reference (or pinned) layer*, while the other has a variable direction and is called the *free layer*.

The MTJ shows a low resistance when the two layers have the same direction of magnetization; this is called the parallel state and represents the logical 0 (see Figure 4). When magnetization directions are opposite to one another, we call this an anti-parallel state in which the resistance is higher than the parallel state. This represents a logical 1.

In Spin Torque Transfer RAM (STT-RAM), that is widely studied and our focus in this article, the magnetization direction of the free layer changes according to the voltage that is applied

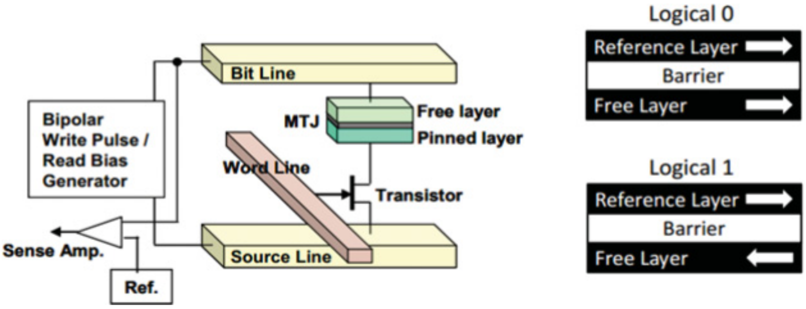


Fig. 4. An STT-RAM memory cell (Xue et al. 2011) and operations (Kultursay et al. 2013).

between the source line (SL) and the bit line (BL). Therefore, when a high positive voltage difference is applied between SL and BL, a logical 0 is written, while if a high negative voltage difference is applied, then a logical 1 is written. To ensure a status reversal, the issued current must be maintained for a given duration of time called the *write pulse width* (between 2ns and 12ns) and its amplitude should be equal to a *threshold current* (between 100μa and 1000μa).

STT-RAM differs from the original MRAM cell in how it sets the orientation of the MTJ: in previous MRAM technology the orientation is set using an external magnetic field, while in STT-RAM a current of polarized electrons is used.

For a read operation to occur, a very small voltage is applied between SL and BL, which causes a current to flow through the MTJ. The value of this current is relative to the resistance of the MTJ, which depends on the magnetization. This current is compared with a reference current, and then the value 0 or 1 is read from the MRAM cell.

Another promising type of MRAM technology is the SOT-RAM (Spin Orbit Torque RAM) (Oboril et al. 2015). The junction here uses perpendicular magnetization and an additional terminal is added to separate the path of read and write operations. This implementation allows for a better optimization of the two (read and write) paths, as they have different physical requirements.

4.1.2 MRAM Endurance. For STT-RAM, a 10^{15} endurance value, in write cycles, has been estimated. However, in some other studies the best endurance test yielded a value of less than 4×10^{12} (Mittal et al. 2015b; Huai 2008).

In fact, MRAM suffers mainly from two sources of unreliability: (1) MTJ cells are subject to thermal instability, which could lead to data loss. The probability of failure depends on the implementation of the junction, the temperature, the vulnerability time (which is the time between the write and the last reading of data), and the number of memory cells. The thermal instability increases as the scale of technology decreases. (2) The high write current stresses the memory cells and degrades the junction, and then limits their integrity over the time. This problem impacts STT-RAMs, where the write current is high.

In addition, as the read operation needs a flow of current, this can also induce a change in the magnetization, called read disturb. As the write current is proportional to the MJT area, the shrinking of the feature size causes the reduction of the write current, whereas the read current must remain sufficient to drive the sense amplifiers (Wang et al. 2015a). As a consequence, the read disturbance rate increases with the memory density. STT-RAMs are also more sensible to such an effect than SOT-RAMs, as the write and read paths are the same.

4.2 Integration Options

As one can see in Table 1, the write endurance of STT-MRAM is approximately the same as that of DRAM and SRAM. This makes it a good candidate for integration at those levels of the memory hierarchy. However, the endurance is far from the ideal value of 10^{15}. Nevertheless, as we will see in the next sections, some efforts have been made to increase the endurance by, for instance, compromising on the retention time.

From a performance point of view, even though the read performance of STT-RAM is comparable to that of SRAM and in some cases better than that of DRAM, it is lagging in terms of write latency and energy.

Most state-of-the-art work integrated STT-MRAM at the primary memory or cache memory level, whether when complementing a given level of the hierarchy or replacing it.

4.2.1 MRAM in On-Chip Cache. STT-MRAM has been integrated in mainly two ways in on-chip caches in state-of-the-art work: (1) in all levels of the cache hierarchy, as in Li et al. (2012), Komalan et al. (2014), and Senni et al. (2015), or (2) in the last levels of cache (LLC), as in Syu et al. (2013), Cheng et al. (2016). The idea behind the second set of solutions is that the large write latencies of STT-RAM cannot be tolerated in first-level cache, because this level is accessed very frequently.

MRAM in all levels of cache. Many studies have proposed using STT-MRAM in all levels of cache. In Senni et al. (2014), the authors highlighted the gain that one can expect in terms of static energy from replacing SRAM caches on L1 and L2 with STT-RAM. The study shows that while the performance is comparable for the tested workloads, STT-RAM drastically decreases the static energy while consuming more dynamic energy. The same conclusions were drawn in Komalan et al. (2014), in which an L1 instruction cache was replaced by STT-RAM by extending the miss status holding registers to cope with the write latency of the NVM.

Multi-level caches offer abilities for mitigating read disturbance issues. For an STT-RAM integration as L2 cache, in Wang et al. (2015), a Read-And-Restore strategy is proposed, by which after the processing of a L1 miss, a restore buffer refreshes the source L2 block in background. Based on the observation that read disturbance happens when the read current is in an opposite direction than the write current, they also establish a two-read sequence, which makes it possible to detect disturbed memory cells, thereby only refreshing these ones. These two techniques optimize the performance and reduce energy overhead due to the read disturbance management.

The authors of Li et al. (2014) envisioned a horizontal integration of STT-RAM with SRAM on a one-level cache system. In such hybrid caches (Sun et al. 2009; Wu et al. 2009; Jadidi et al. 2011; Li et al. 2011), the system migrates data from the two technologies according to the access pattern mainly to mitigate the high write operation latency. The authors of Li et al. (2014) presented a compiler-assisted approach to minimizing the migration overhead. In Wang et al. (2015), the authors proposed a full design of STT-RAM integration as a scratchpad memory for real-time applications.

As previously stated, the very promising SOT-RAM technology drastically reduces the access time and energy consumption. It has even been used in L1 hybrid caches. In Oboril et al. (2015), the authors studied many configurations with SRAM, SOT-RAM, and STT-RAM. The main metrics for evaluation were the area, the execution time, and the energy. The study ended with some interesting conclusions, such as that the SOT-RAM can be the best choice for the first level of cache for low power devices, but that for small memory blocks, SRAM is still the best solution in terms of area and performance. They were even many cases for which hybrid configurations such as SOT-RAM for L1 instruction caches and SRAM for L1 data caches, with SOT-RAM for L2 caches, was the optimal solution.

MRAM in Last-Level Cache (LLC). The main technology used in studies introducing MRAM in LLC is the STT-RAM.

In Wu et al. (2009), the authors presented a very interesting study on exploring the architecture of cache when integrating some NVMs, such as MRAM and PCM, with some new technologies with volatile memories such as eDRAM (embedded DRAM). In this study, the authors evaluated many different architectures split into two types of hybrid caches namely: inter-cache level hybrid cache architectures (LHCA) and intra-cache or region-based hybrid cache architecture (RHCA). In the former, each level consists strictly of one memory technology (vertical integration), while in the latter each level may consist of regions with different technologies (horizontal integration). The study showed that LHCA can provide a 7% improvement in IPC (instructions per cycle) over a three-level SRAM cache, while RHCA can provide a 12% IPC improvement with the same area constraints.

Concerning horizontal integration, in which two memory technologies can be integrated for a given level of cache, the system should apply some adaptive data placement mechanism to take full advantage of each integrated technology. For instance, in Wang et al. (2014), the system tries to reduce writes on STT-RAM by detecting the access pattern on the LLC.

Following the idea of partitioning a given level of cache, in Samavatian et al. (2014) the authors partitioned the L2 cache into two regions of STT-RAM by tuning the retention. They used a low retention partition to absorb frequently written data and a high retention region for less frequently written and very frequently read data. Decreasing the retention allows the write energy and the area of the STT-RAM cell to decrease.

4.2.2 MRAM in Main Memory. Even though most state-of-the-art work on integrating MRAM has focused on on-chip cache subsystems, some studies have explored integrating MRAM as a DRAM replacement or complement.

In Kultursay et al. (2013), the authors studied the complete replacement of the main memory by STT-RAM. In fact, as previously underlined, DRAM is limited by two main factors: scalability and power consumption due to power leakage. The authors first compared DRAM with non-optimized STT-RAM technology. They showed that a simple replacement of DRAM by STT-RAM does not lead to good performance; rather, the STT-RAM main memory behaved very badly because of its write operation latency and energy consumption. The authors then performed some optimizations on STT-RAM. One optimization involved using its property of a decoupled structure of sense amplifiers and row buffers. This allows it to perform selective and partial writes on the memory cell, thereby reducing the number of write operations, thus the latency and energy. Another optimization consisted of bypassing the row buffer for the write operations, as it was observed that the number of hits on write operations is much lower than on read operations. The results of such optimizations on a given number of workloads and a multicore processor showed that an STT-RAM memory, while achieving a performance comparable to that of DRAM, drastically reduces the amount of energy that is consumed (by about 60%).

Another approach studied in Yang et al. (2013) consists of integrating STT-RAM horizontally with DRAM while implementing a scheme to direct write-intensive data to DRAM. The main objective in integrating both memory technologies in a main memory is to reduce energy consumption levels.

Even though previous studies showed good results from integrating STT-RAM in main memory, as noted in Wang et al. (2014), the internal structure of the MRAM chip is not compatible with current DRAM interfaces. Therefore, to address this issue, the authors proposed some techniques to make the design of LPDDR3 compatible with MRAM architecture.

Other concerns were noted in Jin et al. (2014), relating to the area, power, and latency of STT-RAM memories. The authors draw the attention of the reader to the size of an STT-RAM cell, which might present a serious obstacle to attaining a DRAM-like density. In addition, the write power of STT-MRAM is reportedly too large for many application domains. The authors propose modifications to some critical parameters, such as the thermal stability factor, critical current, and retention time to mitigate the STT-RAM's cell energy and latency properties to make it more suitable as a replacement for DRAM.

4.2.3 MRAM in Storage Systems. There are several studies in integrating MRAM in storage system devices. Lee et al. investigated both PCM and STT-RAM integration in storage systems (Lee et al. 2014). This interesting study emphasizes the effect of the kernel I/O software stack by integrating these NVMs. In addition, they compared and analyzed the efficiency of kernel mechanisms (such as read-ahead) and access methods (such as direct and synchronous I/Os) with NVM based storage systems. In Kang et al. (2015), the authors propose a vertical integration of NVM in the storage system. The study focused on PCM but their techniques can work on STT-RAM as well. The idea is to use retention relaxation when NVM is used as a cache in storage systems to decrease the latency, since most data in a cache are evicted within a short time period after they have been entered into the cache.

4.3 Open Research Questions

In many studies on using STT-RAM in a given cache level, the authors tried to improve its performance or to adapt to the constraints of the MRAM through a given set of optimizations. These are summarized in Mittal et al. (2015b):

4.3.1 Relaxing Non-volatility. Relaxing the non-volatility of STT-RAM (Smullen et al. 2011; Jog et al. 2012; Sun et al. 2011; Guo et al. 2010): the idea here is to use different regions (horizontal integration) or levels (vertical integration) of STT-RAM with different retention periods, thus resulting in different write latencies and energy consumption properties.

4.3.2 Minimizing or Avoiding Writes. Minimizing or avoiding writes (Joo et al. 2010; Bishnoi et al. 2014; Zhou et al. 2009b; Goswami et al. 2013; Yazdanshenas et al. 2014; Ahn et al. 2012; Sun et al. 2009; Rasquinha et al. 2010; Jung et al. 2013; Park et al. 2012; Cheng et al. 2016): the main objective of this optimization is to reduce the number of bits updated on the STT-RAM. This can be achieved with different techniques: for instance reading the data before writing it and writing only the different bits, using caches to perform comparisons before updating, coding data to decrease bit modifications, and so on.

4.3.3 Improving the Memory Lifetime. Improving the memory lifetime by using wear-leveling: for flash memories, wear leveling techniques could be used to increase the memory lifetime while coping with the temporal and spatial locality of workloads (Mittal 2013; Chen et al. 2013; Wang et al. 2014a; Jokar et al. 2016).

4.3.4 Addressing 0/1 Asymmetry. As the time required to perform a 1 to 0 transition is larger than that required to perform a 0 to1 transition due to the asymmetry of the switching time of the MTJ, presetting all cells to 0 before an operation allows the effective write latency to be reduced (Kwon et al. 2014).

4.4 MRAM Maturity and the State of the Market

Companies have been developing MRAM for many years. In 2003, a 128Kbit MRAM chip manufactured with a 180nm lithographic process was introduced. The next year, a 16Mbit prototype was unveiled by Infinenon. In 2005, Honeywell posted a data sheet for a 1Mbit Rad-hard MRAM using a 150nm lithographic process, followed by a MRAM memory cell running at 2GHz. Sony announced the first lab-produced STT- MRAM that utilizes a spin-polarized current through the tunneling magneto resistance layer to write data. This method consumes less power and is more scalable than a conventional MRAM. That same year, Freescale Semiconductor Inc. demonstrated

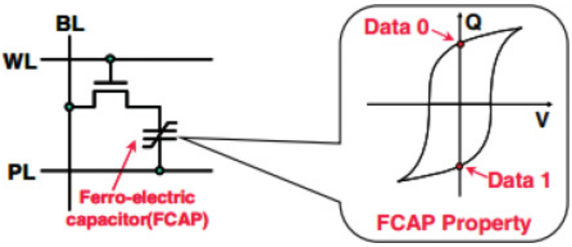


Fig. 5. A FeRAM memory cell.

an MRAM that uses a magnesium oxide barrier and improved bit resistance during the write cycle, thereby reducing the required write current.

Toshiba and NEC announced a 16Mbit MRAM chip with a new *power-forking* design in 2006. It achieved a transfer rate of 200MB/s, with a 34ns cycle time, the best performance of any MRAM chip. Hitachi and Tohoku University demonstrated a 32Mbit STT-RAM in 2009, and then announced a multi-level MRAM in 2010. In November 2012, Everspin debuted a 64Mb STT-MRAM (Everspin 2015).

5 FERAM

Ferroelectric RAM (FeRAM or FRAM) is an NVM that has made it to the stage of mass production earlier than other NVMs (apart from flash memory). Indeed, FeRAM is used in many products today, mainly in the embedded domain (Fujisaki 2013), for example, in automobile equipment such as data recorders and wireless cards, and promises to be a good candidate for the non-volatile storage for wearable electronics (Venkatesh and Singh 2015).

FeRAM exhibits some very attractive properties that made it one of the strongest early candidates (Burr et al. 2008) for the NVM of the future, namely, low latency (as low as that of DRAM), reported to be 20ns (Burr et al. 2008), low power consumption, an erase-less write operation, and the possibility of a straightforward CMOS integration (Kato et al. 2005).

5.1 Basic Concepts

The unit cell of FeRAM resembles that of DRAM in that it consists of one transistor and one Ferro-electric capacitor (FCAP), also known as a 1T1C structure (Kryder et al. 2009; Kanaya et al. 2004). Ferro-electric material is formed of $Pb(Zr_x, Ti_{1-x})O_3$ (PZT or lead zirconate titanate), between two metallic electrodes. FCAP is characterized by two remnant reversible polarization states. The charge of the FCAP retains its polarity without the need for power, thanks to the property of hysteresis that the ferroelectric material exhibits in comparison to the dielectric material in DRAM. This explains its non-volatility. In addition, FeRAM does not require refreshing operations; consequently, it consumes less power than DRAM.

The write operation is achieved by forcing a pulse through the plate line (PL) of the FCAP for a 0, and through the bitline (BL) for a 1 (see Figure 5). Contrary to NAND flash memory, FeRAM does not need asymmetric voltage and/or special high voltage for write operations. For FeRAM, the voltage used is the same as that for Vcc, and can be very small.

As stated earlier, FeRAM was seen as one of the first mature NVMs to replace and/or complement DRAM and storage system technologies. However, after many years of studies on the technology, FeRAM cells still seem difficult to make scalable. In fact, their size remains significantly larger than DRAM cells for gigabit-scale integration. As a consequence, as will be seen in the next section, most recent work on FRAM integration address the issue of whether FeRAM can be used in embedded systems (they are already deployed in MCUs) or in a limited quantity in hybrid systems, or as small volume caches.

5.2 Integration Options

Many different figures on performance have been given in state-of-the-art studies concerning the performance of FeRAM. However, many agree that its read and write operations are more or less symmetric. Unlike MRAM and PCM, FeRAM does not show a strong asymmetry between read and write operations. The performance of FeRAM approaches that of DRAM, but still seems to lag behind. In contrast, it is better than DRAM in terms of power consumption. Concerning endurance, values between 10^{12} and 10^{15} have been reported.

The integration of FeRAM can be discussed from different points of view:

- From an endurance point of view, FeRAM could replace DRAM or storage system technologies such as flash memory.
- From a performance point of view, FeRAM could complement DRAM and replace storage system technologies.
- From a density point of view, FeRAM cannot yet replace either DRAM or storage systems technologies, because its scalability to the gigabit remains an open question. As high density cannot be proven for FeRAM, its price is still very high compared to flash memories, even though some applications in the embedded domain are driving the technology.

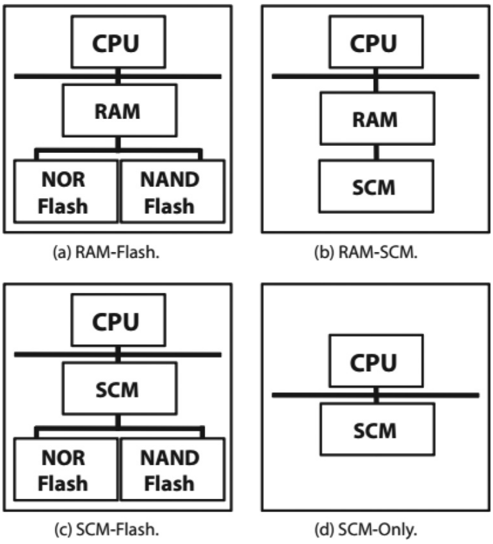
Nevertheless, FeRAM has been studied in state-of-the-art work, indeed, as the physics behind FeRAM have been well mastered, its performance can easily be improved if some new materials with better scalability are discovered.

Some FeRAM integration propositions exist in state-of-the-art studies. To the best of our knowledge, in all studies it was integrated between DRAM and the storage system. The integration was either horizontal, for schemes replacing or complementing DRAM and the storage system with FeRAM; or vertical, involving the insertion of FeRAM between the DRAM and the storage system, generally as a metadata cache (Doh et al. 2007; Yoon et al. 2008).

5.2.1 FeRAM in Main Memory. We did not find an exhaustive set of state-of-the-art work on the use of FeRAM as a primary memory replacement or complement. This is probably due to the drop in performance that can result when integrated in such a way.

Two main studies have been identified. In Suresh et al. (2014), the authors evaluated many different NVM technologies, among which is FeRAM. It has been investigated as a replacement for DRAM and also as a complementary memory to form a hybrid main memory. The performance of FeRAM was tested and compared with that of other NVMs, namely STT-RAM and PCM. Simulations showed that as FeRAM alone can degrade the performance as compared to DRAM, but in some cases, it can lead to small improvements in energy consumption. However, a hybrid memory with DRAM and FeRAM showed better energy efficiency for workloads showing large static energy, even as it degraded performance. As compared to other NVMs, FeRAM was the poorer performer in this study.

Another interesting study on the integration of NVMs (called Storage Class Memory – SCM in this study) was conducted (Baek et al. 2013). In this study, several architectures were tested against different workloads (see Figure 6). This included classical DRAM + flash memory as a storage system, DRAM + SCM, only SCM, and SCM + flash. A FeRAM prototype of 32MB was used as the SCM. The first observation of the study was that SCM + flash gave the worst performance in most cases. This simply means that a straightforward replacement of DRAM by FeRAM is probably not a good idea because of the high latencies of FeRAM (as compared to DRAM). On the other



(a) RAM-Flash. (b) RAM-SCM. (c) SCM-Flash. (d) SCM-Only.

Fig. 6. Tested memory hierarchies in Baek et al. (2013).

hand, the SCM only configuration produced some good results depending on the workload. The authors went further by proposing some optimizations of the SCM only configuration. The idea was to perform in-place updates of files and meta-data rather than having multiple copies as is the case in memory/storage traditional systems. The authors proposed a unified file/data management system referred to as object management. Bridges were built between traditional file and memory API, with the SCM manager implementing object management. With this new architecture, the authors demonstrated some significant performance enhancements over an SCM that simply reuses traditional operating system memory and a storage stack.

The authors of previous studies clearly mentioned that FeRAM performance lags behind that of DRAM, even if the energy consumption properties of FeRAM are superior. However, if it is to be used in high performance computing, then FeRAM needs to demonstrate scalability, which it is far from being able to do.

5.2.2 FeRAM in Storage Systems. From a storage system perspective, FeRAM was mainly integrated horizontally in state-of-the-art studies, except in Chameleon (Yoon et al. 2008), where it was integrated both horizontally and vertically, and in Baek et al. (2013), where the authors mainly focused on replacing the primary storage system with FeRAM, with or without DRAM.

As noted above, FeRAM has been used sparingly because of integration and scalability issues. With the exception of Baek et al. (2013), most state-of-the-art studies used FeRAM mainly to optimize data access to file systems (Jung et al. 2010; Doh et al. 2007) or FTL (Yoon et al. 2008) metadata.

In Chameleon (Yoon et al. 2008), the idea is to store (1) FTL metadata such as mapping tables in FeRAM, and (2) to use a FeRAM block and page buffer to accelerate access to the underlying flash memory. In Doh et al. (2007), the main idea is to store flash file system (MiNV) metadata into FeRAM rather than storing the data into flash and copying them to DRAM at mount time. A very good performance has been observed on the tested workloads.

In FRASH (Jung et al. 2010), the authors tried to bring persistence to memory data structures, so it would be possible to accelerate some operations, for instance, mount time, and to offer faster access to file system data structures by storing them in NVM (FeRAM). For the first objective, the goal was to overcome the volatility of DRAM and to avoid costly mount time data structures by storing those data structures in FeRAM. For the second objective, FRASH stores some storage system structures, such as page metadata, in the FeRAM. FRASH proved to have good performance in comparison to classical flash file systems such as YAFFS or other SCM integration solutions.

5.3 FeRAM Maturity and the State of the Market

Many companies are offering FeRAM-based products. Among these are Ramtron, which has a large spectrum of products; Texas instruments with FeRAM-based MCUs; and Toshiba, which introduced a 128MB FeRAM in a 130nm technology in 2009 (Shiga et al. 2009).

Much of the current FeRAM technology was developed by Ramtron, a fabless semiconductor company. One major licensee is Fujitsu, which operates what is probably the largest semiconductor foundry production line with FeRAM capability. Since 1999 Fujitsu has been using this line to produce standalone FeRAMs, as well as specialized chips (e.g., chips for smart cards) with embedded FeRAMs. Fujitsu produced devices for Ramtron until 2010. Since 2010 Ramtron's fabricators have been Texas Instruments (TI) and IBM. Since at least 2001 TI has collaborated with Ramtron to develop FeRAM test chips in a modified 130nm process. In the fall of 2005, Ramtron reported that they were evaluating prototype samples of an 8Mbit FeRAM manufactured using TI's FeRAM process. Fujitsu and Seiko-Epson were collaborating in 2005 to develop a 180nm FeRAM process. In 2012, Ramtron was acquired by Cypress Semiconductor.

FeRAM research projects have also been reported at Samsung, Matsushita, Oki, Toshiba, Infineon, Hynix, Symetrix, Cambridge University, the University of Toronto, and the Interuniversity Microelectronics Centre (IMEC, Belgium).

Since 2016, TI's latest MSP430 microcontrollers have been utilizing FeRAM for code and data with a unified memory approach (Wong 2016).

6 RERAM

The basic idea behind Resistive RAM (ReRAM) is that they are memories that store their logical state under the form of a resistive state (Sandhu 2013). Thanks to its characteristics, ReRAM is supposed to integrate many application domains such as consumer electronics, personal computers, medical applications, space, and automotive applications (Meena et al. 2014). Indeed, ReRAM is compatible with conventional semi-conductor fabrication processes. ReRAM is a very promising technology as it has a lower power consumption than PCM and a higher density than MRAM (see Table 1). ReRAM has demonstrated good stability at fabrication technologies of 10nm (Akinaga and Shima 2010). From an endurance point of view, it is between one and five orders of magnitude better than flash memory (see Table 1). From the scalability and fabrication points of view, ReRAM could be considered a serious candidate for universal memory; however, its endurance remains limited and it cannot be a replacement for SRAM or DRAM. Nevertheless, it is currently very extensively studied and many scientific obstacles could be resolved in the coming years.

6.1 Basic Concepts

ReRAM belongs to the class of memristor devices. A *memristor* is a two-terminal resistor device with varying resistance. The resistance value changes according to the magnitude and polarity of the voltage that is applied, and the duration for which the voltage is applied (William 2008). The main characteristic of a memristor is that the resistance value does not change when the power is turned off; this provides it with its property of non-volatility.

The concept of memristor was invented by Leon Chua in 1971 (Chua 1971). It has been called the fourth fundamental building block of electronics (along with resistors, capacitors, and inductors). In 2008, it was demonstrated by a team of researchers from HP labs (Sturkov et al. 2008): "Memristor

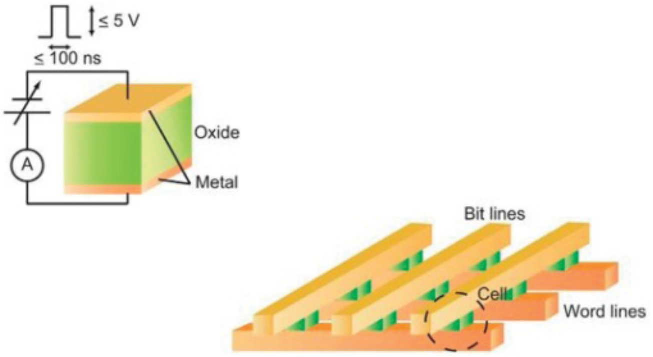


Fig. 7. ReRAM cells[3]

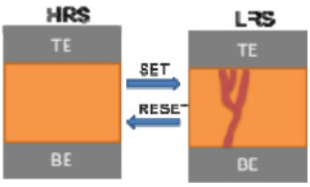


Fig. 8. ReRAM cells and filament formation in Oxide-based RAM (Clermidy et al. 2014).

is a contraction of memory resistor, because that is exactly its function. . . the ability to indefinitely store resistance values means that a memristor can be used as a nonvolatile memory" (William 2008).

In a memristor, a low resistance value is considered as a logical 1 while a high resistance value is considered as a logical 0. To read a memory cell value, the sensing logic compares the current flowing through the selected memristor cell with the one flowing through a reference resistor with the same voltage applied on both.

A ReRAM cell is a two-terminal Metal-Insulator-Metal (MIM) device composed of an insulating or resistive material, which is an oxide, sandwiched between two electrode metal conductors (see Figure 7).

The basic principle behind ReRAM is the formation (Low Resistive State) and disruption (High Resistive State) of a conductive filament, the objective of which is to shunt the top and bottom electrodes (M) through the resistive oxide layer (see Figure 8).

ReRAMs can be classified into the following two types according to their switching behavior: (1) unipolar devices, where the switching direction depends on the amplitude of the applied voltage (Kryder et al. 2009; Sandhu 2013; William 2008), and (2) bipolar devices, where the switching direction depends on the voltage polarity. In bipolar devices, the switching mechanism is based on the creation of oxygen vacancies, which form an electric path between the top and bottom electrodes. TiO_x material has been widely used as top and bottom electrode material (Choi et al. 2005; Fujimoto et al. 2006; Hosoi et al. 2006). Many other materials have been used in state-of-the-art-work, such as ZrOx (Lee et al. 2006) and NiO (Gibbons and Beadle 1964).

[3] Source: http://www.dobreprogramy.pl/Crossbar-pokazal-terabajtowy-czip-pamieci-ReRAM-niebawemzapomnimy-o-flashu,News,45456.html.

Conductive Bridge RAM (CBRAM), another promising technology, is a solid-electrolyte (SE) memory in which the SE material is sandwiched between an inert electrode (cathode) and an oxidizable electrode (anode).

6.2 Integration Options

Due to its integration capabilities and performance, ReRAM has been considered in many studies as a potential replacement and/or as complementary memory in the memory hierarchy. The endurance of ReRAM was reported to be between 10^{10} and 10^{12} (Sheu et al. 2011; Kim et al. 2011; Eshraghian et al. 2011), meaning that it would be difficult to integrate in cache levels without specific optimizations. ReRAM has been investigated for both horizontal and vertical integrations.

6.2.1 ReRAM in Cache Memory. The endurance of ReRAM could pose an obstacle to its integration in low memory levels such as caches, and this possibility has been investigated in many studies.

In Dong et al. (2013), the authors studied many NVMs with a focus on a ReRAM case study. Different models were proposed, allowing for a design space exploration for the integration of ReRAM and other NVMs. Those models were implemented through a simulator called NVSim (Dong et al. 2012). The authors of Dong et al. (2012) compared differences in performance when ReRAM was integrated vertically in the cache (traditional SRAM) stack. Many scenarios were tested: putting ReRAM in all traditional cache levels, then in the two higher levels (L2 and L3), and then only in the higher level (L3). In each case the authors noted an energy gain and a degradation in performance (ReRAM is comparable to SRAM in read performance but significantly slower in write performance). One would need to compromise on the chosen architecture in accordance with the energy/performance tradeoff needed for the application. In a previous study, the authors relied on wear leveling techniques to partly cope with endurance issues (Schechter et al. 2010; Wang et al. 2013). In Mittal and Vetter (2015a), the authors presented a horizontal integration of ReRAM in the L2 cache together with SRAM in a system called AYUSH. To cope with the ReRAM endurance issue, frequently reused data are stored in the SRAM.

ReRAM was also introduced in the memory hierarchy for more specific application domains. In Komalan et al. (2013), it was integrated in the L0 (loop buffer (Uh et al. 1999)) and/or L1 cache level for ultra-low power embedded instruction memories dedicated to low-power wireless/multimedia applications with specific read-dominant workloads (loop dominated code). ReRAM has also shown good performance when integrated into FPGAs as a replacement for SRAM to improve problems such as leakages of power and rapid power on/off operations (Clermidy et al. 2014).

6.2.2 ReRAM in Main Memory. As for PCM, ReRAM has been integrated in main memory to complement DRAM. For instance, in Hassan et al. (2015), the authors considered ReRAM in a horizontal scheme with DRAM. They proposed a data placement and migration strategy at the applicative level and validated it on key value data stores.

In Xu et al. (2015), an 8Gb ReRAM chip is modelled based on cell array structures without selection transistor (0T1R). The chip is compatible with the DDR3 interface and constrained by the same power and area budget as a DRAM of the same capacity. The authors have optimized the write latency by means of microarchitectural level enhancements and data encoding. Their simulations show less than 10% of performance degradations with respect to a main memory system using DRAM chips.

6.2.3 ReRAM in Storage Systems. Many researchers found that the ReRAM endurance cannot fit in a low-level memory hierarchy; consequently, ReRAM has been regarded as future replacement or complement for flash memory.

In Tanakamaru et al. (2014), the authors studied a hybrid storage system composed of a small volume of ReRAM and a large volume of flash memory. The integration of ReRAM was horizontal, with the objective being to store mirroring information and parity and error records, as ReRAM is non-volatile, page rewritable, and has better performance and endurance than flash. The objective of the proposed Unified Solid State Storage system (USSS), which implements reverse mirroring, shift mirroring, error reduction synthesis, and page-RAID, was to improve the acceptable raw bit error rate (ABER) of the memory.

In Jung et al. (2013), the authors highlighted the main issues in designing a large-scale crossbar ReRAM, such as write disturbance and read sensing margin (Jung et al. 2013). The authors argued that without taking this issue into consideration, the sensing margin would be unacceptable for a large-scale ReRAM. The authors proposed some microarchitectural solutions based on a new access strategy to deal with this issue. They also proposed a macroarchitecture design and evaluated the performance of an 8GB ReRAM as compared to two flash memory configurations (integration as a replacement of flash memory). The proposed architecture gave up to eight times better bandwidth and between 66% and 88% shorter latency.

Other studies used ReRAM horizontally integrated in a solid-state device to absorb some specific patterns and relieve flash memory from intensive and random fragmented data updates. In Sun et al. (2014) and Fujii et al. (2012), the authors proposed a horizontal integration of ReRAM together with NAND flash memory; the idea was to use ReRAM for highly written and random data to optimize the overall performance.

6.3 Open Research Issues

Open research issues and challenges related to ReRAM have been discussed in Xue et al. (2011) and (Yang and Williams 2013) and are summarized in this section.

6.3.1 The Switching Endurance. The switching endurance is related to the number of cycles that the device can be switched ON and OFF reversibly before its performance degrades to a non-tolerable threshold. The endurance values reported in the literature are far from the limit of metal oxide memristive devices. The key element resides in the choice of the switching material. Many switching materials have been investigated, such as Pt/TaO$_x$/Ta, TiO$_x$, HfOx (Yee et al. 2010), and WOx (Chien 2010). Some showed an endurance of close to 10 billion switching cycles, which is still far from the looked-for universal memory endurance of about 10^{15}–10^{16}.

6.3.2 The Device Yield. To make ReRAM viable for manufacturing, the device yield should be enhanced, as it has been reported as being low (Yang et al. 2010). One of the key parameters in determining this yield is the control of the switching channels inside the device (Yang and Williams 2013). Some state-of-the-art solutions have improved the yield through seeding nanoscale switching centers (Yang et al. 2010).

6.3.3 The Operation Energy. Even though the energy required to switch the ReRAM cell is very small compared to other NVMs such as flash and PCM, it is still very important to lower its value to increase the memory density. The energy required for switching is larger than that required for reading. There are two main solutions to lowering the energy consumed in switching: (1) lowering the junction size, or (2) optimizing the switching material (Miao et al. 2011).

6.3.4 Electroforming Process. Electroforming is the application of high voltage or a current, which needs to be performed at one time to enable the switching of the resistive memory cell. This process produces a reduction in electronic conductivity (Xue et al. 2011; Yang et al. 2009). After this, the device operates with widely varying properties according to the material that is used. It is very important to limit this variance in computing circuit applications (Yang et al. 2009).

6.3.5 Sneak Path and Nonlinearity. The sneak path is an unexpected path in the crossbar structure, which may lead to write and read failures (Jung et al. 2013). It occurs due to the absence of a transistor or any access device on the ReRAM crossbar structure. Preventing sneak paths is a necessary property for achieving a large-scale ReRAM memory (Chen et al. 2011a, 2011b). To solve the issue of sneak paths without introducing an access device, a highly nonlinear current-voltage relation for the ON state is required (Yang and Williams 2013). In fact, the higher the non-linearity, the better the memory cell as the sneak current is significantly reduced (Niu et al. 2012), and the better the scaling of the write current and the energy consumption. As discussed in Jung et al. (2013), state-of-the-art sneak path solutions may introduce some other issues such as write disturbances and a read sensing margin that can prevent ReRAM from scaling and thus from becoming a candidate for replacing storage systems.

To perform design space exploration of ReRAM, many tools were developed such as NVSim (Dong et al. 2012), and models were built to study and optimize many parameters such as area, latency, energy (Xu et al. 2011), and reliability (Xu et al. 2014), or to study trade-offs to achieving a multi-level cell ReRAM (Xu et al. 2013).

6.4 ReRAM Maturity and the State of the Market

The ReRAM is still under development, and some prototypes have been provided by the Rambus Company and the Crossbar Company. In February 2012, Rambus bought a ReRAM company called Unity Semiconductor, and Panasonic launched a ReRAM evaluation kit in May 2012. The evaluation kit is based on a tantalum oxide 1T1R memory cell architecture. In 2013, Crossbar introduced a ReRAM prototype in the form of a chip about the size of a postage stamp that can store 1 TB of data. In August 2013, the Crossbar Company claimed that large-scale production of their ReRAM chips was scheduled for 2015. This same year, Intel and Micron introduced a so-called 3D Xpoint memory bearing similarities with ReRAM and that was being developed by Crossbar.

In 2016, Western Digital announced at the Flash Memory Summit that it intends to use 3D Resistive RAM (ReRAM) as storage class memory (SCM) for its future special-purpose ultra-fast SSDs (Shikov 2016).

7 CONCLUSION

In this article, we have introduced four very promising NVM technologies: PCM, MRAM, FeRAM, and ReRAM, each of which has its pros and cons. Those NVMs are in different stages of development, with some are already being manufactured (such as FeRAM in some MCUs) and others still in the prototype phase. Those NVMs have been discussed in state-of-the-art studies and integrated according to many factors such as endurance, write latency, energy, and process fabrication compatibility.

Two main ways of integrating NVMs have been proposed: horizontal or vertical. Horizontal integration consists of complementing the existing level of memory in the memory hierarchy pyramid, thereby providing at least two options for storing data (with generally no redundancy). Data placement in this case obeys some pattern-related properties based mainly on two characteristics: types of operation and access patterns. In vertical integration an additional level is inserted into the memory hierarchy. The inserted level acts as a cache or a buffer to cope with the performance gap between two memory technologies.

From the applicative or even the operating system points of view, there are mainly two options for the integration. First, it is possible to hide the introduced memory from the operating system and/or the application, just as if there were different levels of cache memory, where the operating system knows about the existence of a cache, but does not know how many levels there are, nor does it have the ability to manage the cache, as this managing is done in the hardware. The second option consists of making the newly integrated memory visible to the operating system and eventually to the applications, so it is possible to choose the memory in which to store data.

NVM brings new research opportunities for optimizing computing systems. It should be an interesting direction to continuously exploit specific characteristics of NVM. For instance, compared with DRAM, all NVM techniques have superior static power but with worse write performance and endurance. Therefore, more effective hardware/software techniques need to be developed to utilize these features. Moreover, integrating NVM into the memory/storage systems may introduce new heterogeneous traffics. For instance, I/O traffics can be passed to the memory system (Chen et. al. 2016). It will be a challenge to develop effective architectural techniques to handle such heterogeneity with small modification to existing systems. Finally, with NVM integration, it is possible to build a uniform memory/storage system. It should be interesting to investigate how to fully exploit this uniform memory/storage system at the software level.

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