

MTE421 Project 2

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Introduction

In this project, I'm designing a single-ended differential amplifier circuit made up of 6 MOSFETs as its main components. The load of the differential amplifier will be a PMOS current mirror, and the tail current will be provided through an NMOS current mirror. The circuit aims to achieve DC gain of 15V/V and gain bandwidth product of at least 10MHz at -3dB point. Lastly, all MOSFETs are assumed to operate in saturation mode in this project.

Paper Design

Small Signal Analysis :

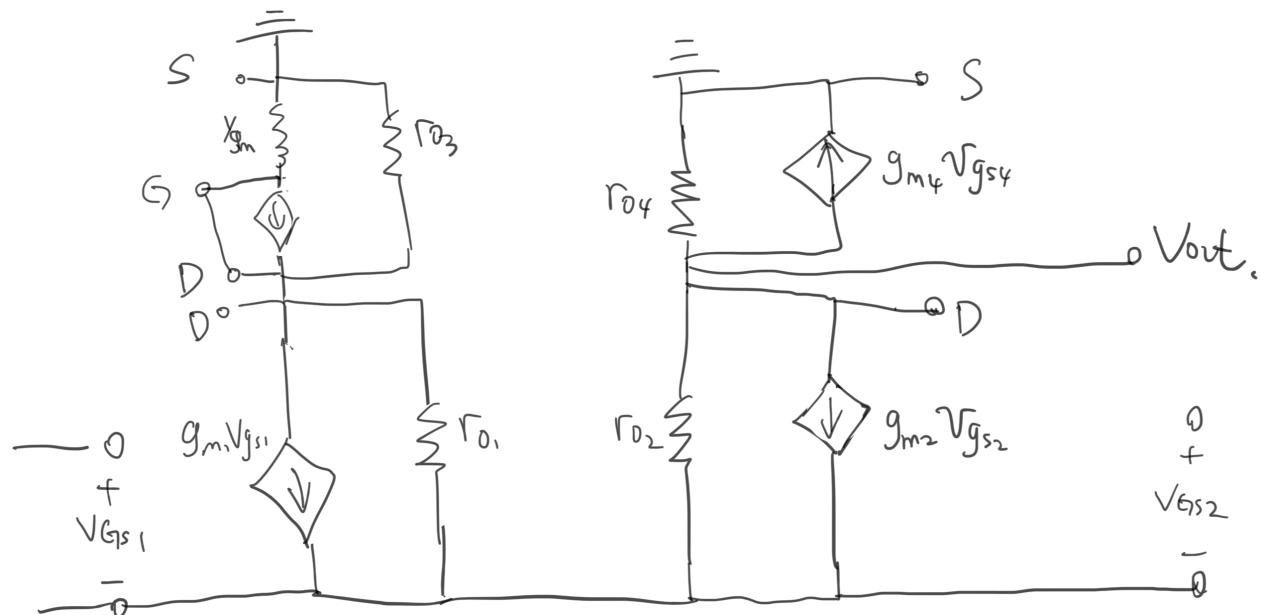


Figure 1: Small Signal Analysis of the Differential Amplifier Circuit

As we assumed all MOSFETs are operating in the saturation region, M5 can be treated as an ideal current source. In the world of small signal analysis, a DC current source is treated as an open circuit due to zero current change over time.

Therefore, the small signal analysis circuit is reduced to the differential pair MOSFETs M1 & M2, and the PMOS current mirror MOSFET pair M3 & M4.

PMOS M3 has its gate and drain terminal shorted together, which reduces its small signal model to just its intrinsic small signal resistance in parallel with its output resistance, $\frac{1}{g_{m3}} \parallel r_{o3}$. g_{m3} is very large, resulting in $\frac{1}{g_{m3}}$ to be very small,

which reduces the whole small signal model of M3 to be $\frac{1}{g_{m3}}$.

The differential gain $A_d \equiv \frac{v_o}{v_{id}}$, can also be analyzed using the two-port network

model. Its equation can be expressed as the product of overall transconductance of the circuit G_m and the output resistance R_o .

First, we short the output to ground to find G_m , which is the relationship between input voltage and output current. The drain of M2 (i.e. output node) is shorted to ground. The common source of M1 and M2 needs to have a voltage smaller or equal to 0V to maintain current flow through M2. Therefore, a virtual ground is developed at the common source of M1 and M2. The small signal circuit becomes

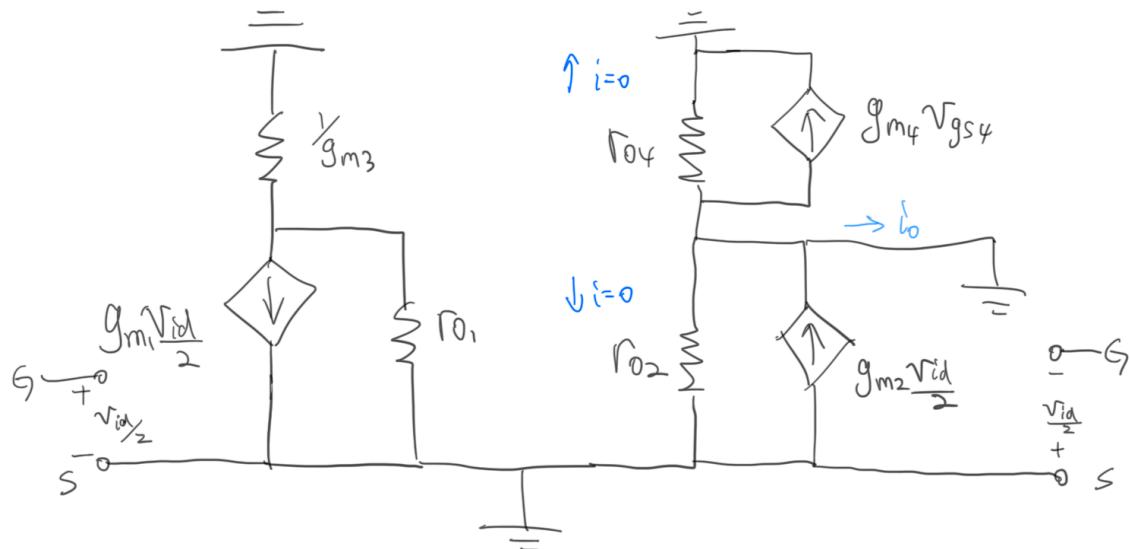


Figure 2: Small Signal Analysis of the Differential Amplifier Circuit to find Circuit G_m

After some calculations, we obtained the differential amplifier's transconductance G_m to be either MOSFET M1 or M2's transconductance.

$$i_o = -g_{m2}v_{gs2} - g_{m4}v_{gs4}$$

$$v_{gs2} = -\frac{v_{id}}{2}.$$

$$\therefore i_o = g_{m2}\frac{v_{id}}{2} - g_{m4}v_{gs4}$$

from PMOS current mirror:

$$v_{gs4} = v_{gs3} = v_{ds3} = -i_{ds3} \cdot r_3 = -i_{ds1} \cdot r_3$$

$$v_{gs4} = -g_{m1}v_{gs1} \cdot \frac{1}{g_{m3}} = -\frac{g_{m1}}{g_{m3}} \left(\frac{v_{id}}{2} \right)$$

PMOS current mirror MOSFET pair has $g_{m3} \approx g_{m4}$

Difff pair has $g_{m1} \approx g_{m2}$.

$$v_{gs4} = -\frac{g_{m2}}{g_{m4}} \left(\frac{v_{id}}{2} \right)$$

$$i_o = g_{m2} \frac{v_{id}}{2} - \left(g_{m4} \cdot \frac{g_{m2}}{g_{m4}} \frac{v_{id}}{2} \right)$$

$$i_o = g_{m2} \frac{v_{id}}{2} + g_{m2} \frac{v_{id}}{2} = g_{m1} v_{id},$$

$$G_m \equiv \frac{i_o}{v_{id}} = g_{m1} = g_{m2}.$$

Figure 3: Calculation Steps to find differential amplifier circuit's G_m

Moving on to finding the output resistance R_o , we set both input voltage sources to 0 to eliminate any contributions from them such that we can focus on the intrinsic behaviors of the circuit. Connecting a voltage source at the single ended output, the ratio between the voltage and the current flowing out of it is defined as the output resistance R_o , of the overall differential amplifier circuit.

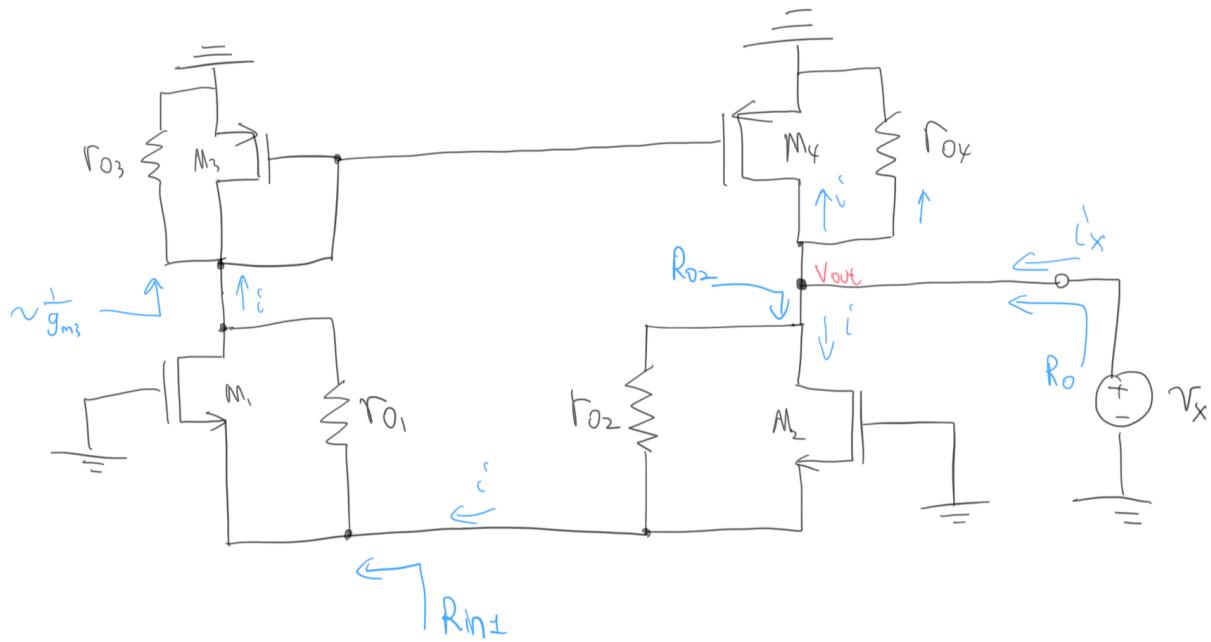
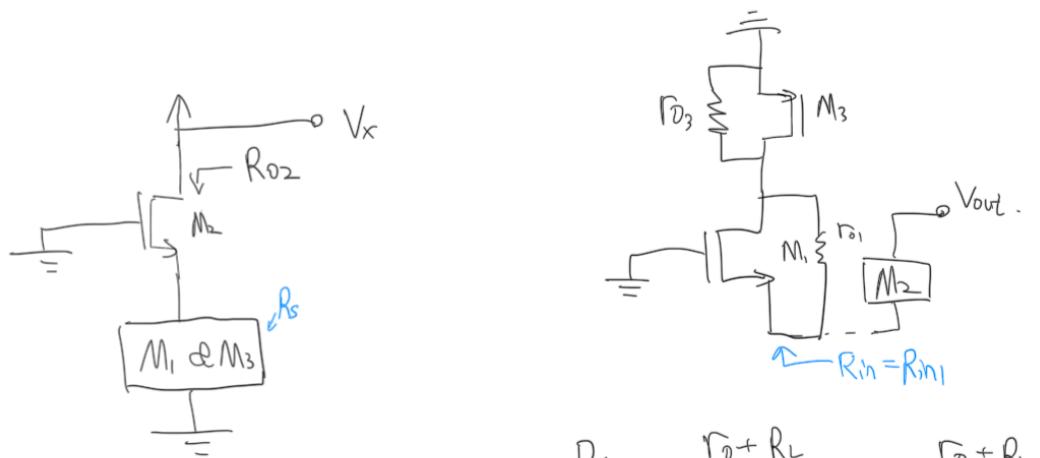


Figure 4: Small Signal Analysis of the Differential Amplifier Circuit to find Circuit R_o

If we follow the current flowing downwards through M2 and label it as i , there is only a path for it to flow through M2, followed by M1 & M3, all the way to the ground on the top left. Applying Ohm's Law, it can be observed that $i = \frac{v_x}{R_{o2}}$,

where R_{o2} is the resistance seen into the drain of M2. Both MOSFET M1 and M2 has their gate connected to the ground. Analyzing them with the common gate amplifier model, we get $R_{o2} \approx 2r_{o2}$.



$$R_o = R_o + R_s + g_m R_o R_s$$

$$R_{o2} = R_{o2} + R_{in_1} + g_{m2} R_{o2} R_{in_1}$$

$$R_{o2} = R_{o2} + \frac{1}{g_{m1}} + g_{m2} R_{o2} \frac{1}{g_{m1}}$$

$$\therefore g_{m1} \approx g_{m2}$$

$$\therefore R_{o2} \approx \frac{1}{g_{m1}} + R_{o2} + R_{o2}$$

$$R_{o2} \approx 2R_{o2}$$

$$\begin{aligned}
 R_{in} &= \frac{R_o + R_L}{g_m R_o + 1} \approx \frac{R_o + R_L}{g_m R_o} \\
 R_{in_1} &= \frac{R_{o1} + \frac{1}{g_{m3}} \parallel R_{o3}}{g_{m1} R_{o1}} \\
 &\approx \frac{R_{o1} + \frac{1}{g_{m3}}}{g_{m1} R_{o1}} \\
 &= \frac{1}{g_{m1}} + \frac{\frac{1}{g_{m3}}}{g_{m1} R_{o1}} \approx 0
 \end{aligned}$$

Figure 5: Partial Analysis of the Differential Amplifier Circuit to find Circuit R_o

Returning to the output node and applying KCL, current i_x coming out of v_x can flow into 3 different directions. The current flowing into M4 is the same as the current flowing into M3 by the nature of the current mirror circuit, and thus equal to i . The current flowing through the output resistance of M4, can be expressed using the Ohm's Law, as $\frac{v_x}{r_{o4}}$.

$$\begin{aligned}
i_x &= i + i + \frac{\sqrt{x}}{r_{o4}} \\
&= 2 \frac{\sqrt{x}}{r_{o2}} + \frac{\sqrt{x}}{r_{o4}} \\
&\approx 2 \frac{\sqrt{x}}{2r_{o2}} + \frac{\sqrt{x}}{r_{o4}} \\
&= \frac{\sqrt{x}}{r_{o2} \parallel r_{o4}} \\
R_o &\equiv \frac{\sqrt{x}}{i_x} = r_{o2} \parallel r_{o4}
\end{aligned}$$

Figure 6: Calculation Steps to find circuit's R_o

Now, we have derived both short-circuit transconductance $G_m = g_{m1}$ and output resistance $R_o = r_{o2} \parallel r_{o4}$. We want to find a reference current such that the gain G_m and R_o of the differential amplifier circuit yield a gain that is above 15V/V.

Going back to the basics of an MOSFET, it can be found that $g_m \propto \sqrt{I_d}$, $r_o \propto \frac{1}{I_d}$ and $r_o \propto L$.

$$g_m \equiv \frac{\partial I_d}{\partial V_{GS}}$$

$$I_d = \frac{1}{2} \mu_n C_{ox} V_{ov}^2 = \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_{th})^2$$

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

$$V_{ov} \propto \sqrt{I_d} \Rightarrow g_m \propto \sqrt{I_d}$$

$$r_o = \frac{1}{\lambda I_d} \Rightarrow r_o \propto \frac{1}{I_d}$$

$$\because \lambda \propto \frac{1}{L} \text{ and } r_o = \frac{1}{\lambda I_d}$$

$$\therefore r_o \propto L$$

Figure 7: Relationships between MOSFET g_m & r_o and Design Parameters

As values of g_m and r_o cannot be directly calculated by solving the system of equations, we will pick a random I_D by manipulating the and see if it meets the design criteria in the Cadence simulation. The NMOS and PMOS parameters are extracted after simulating the whole differential and confirming all design criteria are met.

Table 1: MOSFET design parameters

Parameter	M1 & M2	M3 & M4 (PMOS)	M5	M6
$ V_t $	0.342 V	0.3 V	0.343 V	0.342 V
I_d	2.2593 μ A	2.2593 μ A	4.52 μ A	1 μ A
g_m	26.45 μ A / V	25.43 μ A / V	60.56 μ A / V	15.25 μ A / V
r_o	2.50 M Ω	2.53 M Ω	/	/

The differential input voltage range is essentially limited by the supply voltage of 1V, which means the maximum single-ended output voltage is 1V. Assuming the gain is 15V/V, the corresponding differential input voltage range would be $V_{diff} \in [0, \frac{V_{DD}}{A_v}]$, plugging in the numbers gives us $V_{diff} \in [0V, 0.067V]$. This value translates to a valid input range of $V_{id} \in [V_{CM} - \frac{V_{diff}}{2}, V_{CM} + \frac{V_{diff}}{2}]$, plugging in the numbers gives us $V_{id} \in [0.524V, 0.590V]$.

Simulation

The simulation begins with an AC sweep of frequency. There are 3 parameters carefully measured to make sure the design criteria are met.

1. DC gain is above 15 V/V at low frequency
2. -3 dB point frequency must be above 10 MHz
3. All MOSFETs are operating in the saturation region, i.e. $V_{GS} > |V_t|$ (Assuming $|V_t|$ is at most 0.48V based on Project 1 parameters)

After fine-tuning the MOSFET width and length, and adjusting the common mode input voltage, I obtained the differential amplifier circuit that met all the design criteria. The design parameters are summarized in the table below and other circuit parameters are shown in Figure 8.

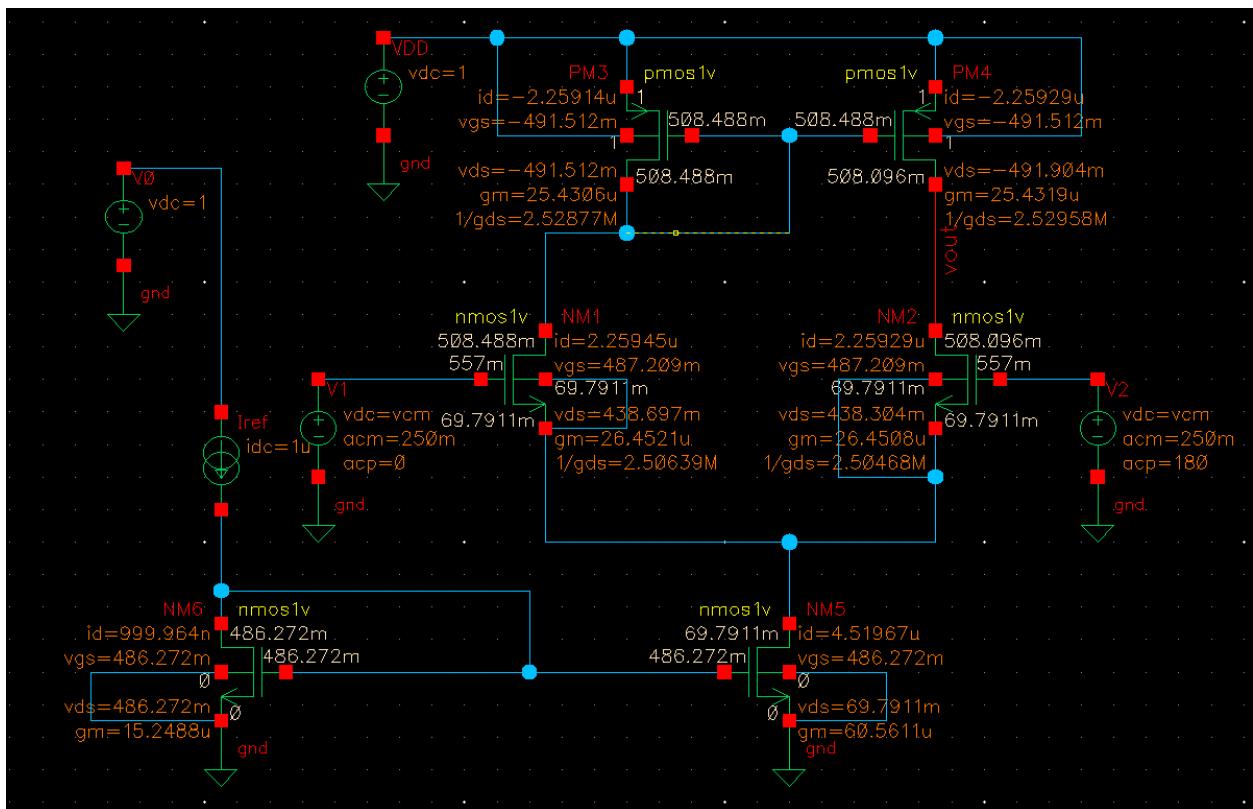


Figure 8: Designed Differential Amplifier Circuit in Cadence

Table 2: MOSFET design parameters

Name	Value
Common Mode Voltage	557mV
M1 width	3μ
M1 length	5μ
M2 width	3μ
M2 length	5μ
M3 width	1.8μ
M3 length	3.2μ
M4 width	1.8μ
M4 length	3.2μ
M5 width	2.25μ
M5 lenth	500n

Name	Value
M6 width	130n
M6 length	130n

Voltage Transfer Characteristic:

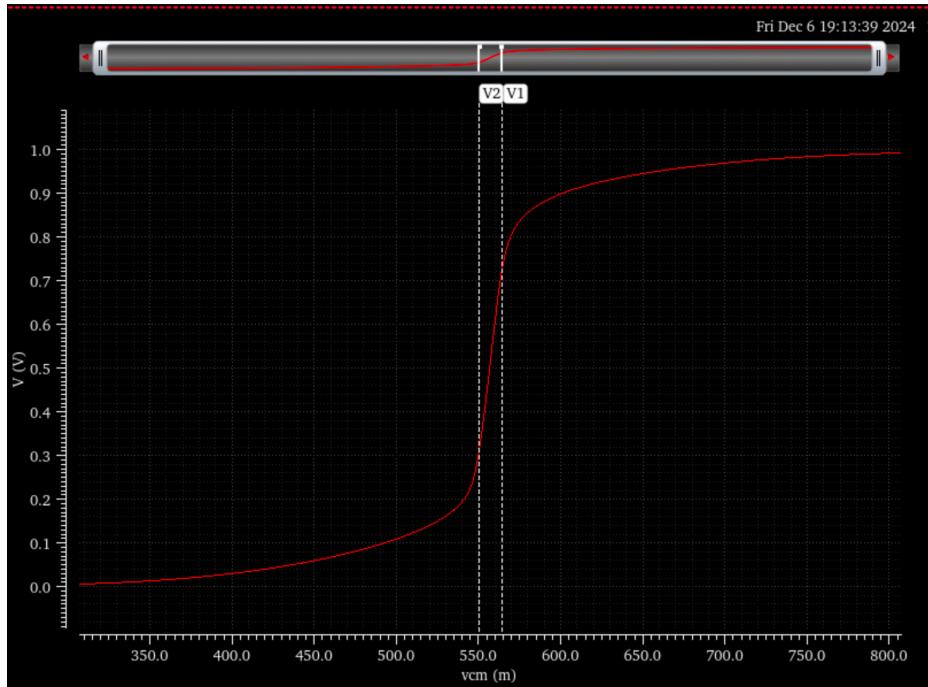


Figure 9: VTC simulation result V_{out} V.S. V_{in+}

After subtracting the common mode voltage from the x-axis, we get a plot showing the relationship between the single-ended output voltage and the differential input voltage at DC:

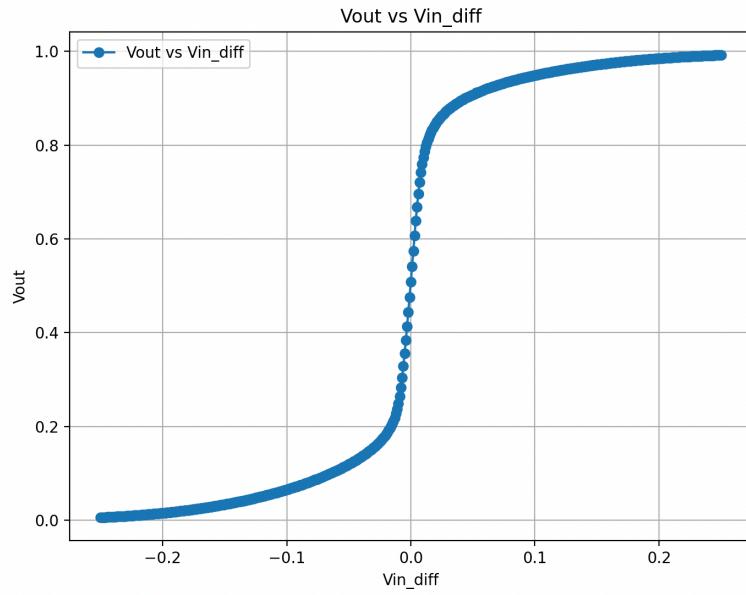


Figure 10: VTC Characteristic after Removing Input Offset Voltage

Frequency Response:

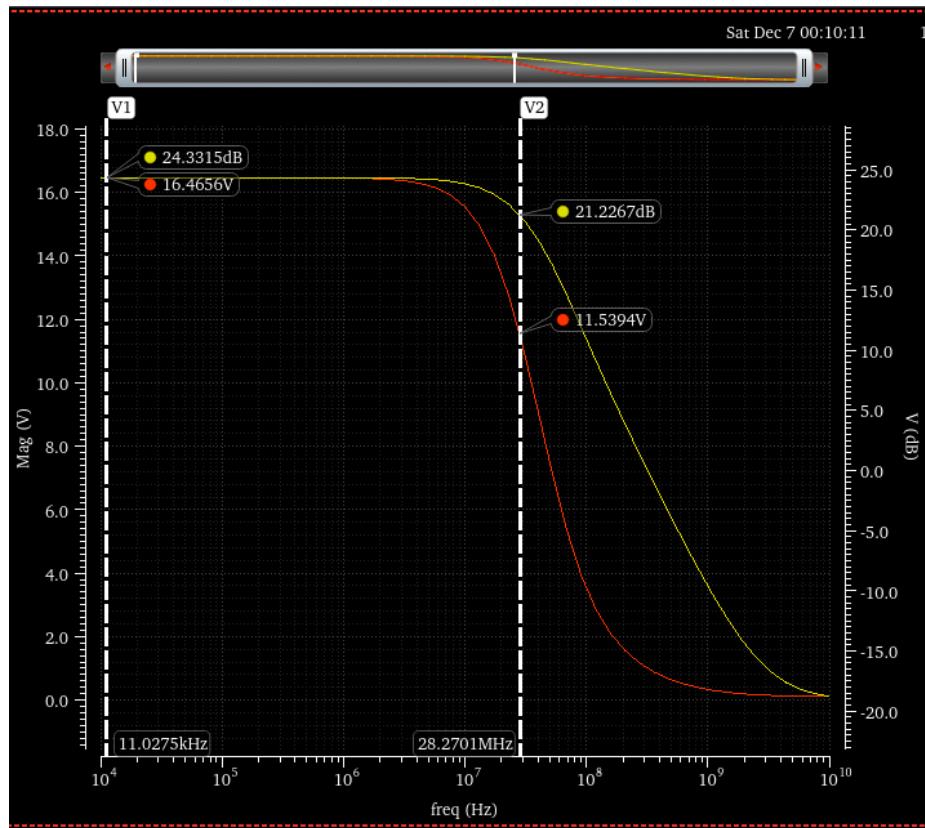


Figure 11: Frequency Response from AC Sweep Simulation Result

Common Mode Rejection:

The plot of common mode gain is shown below.

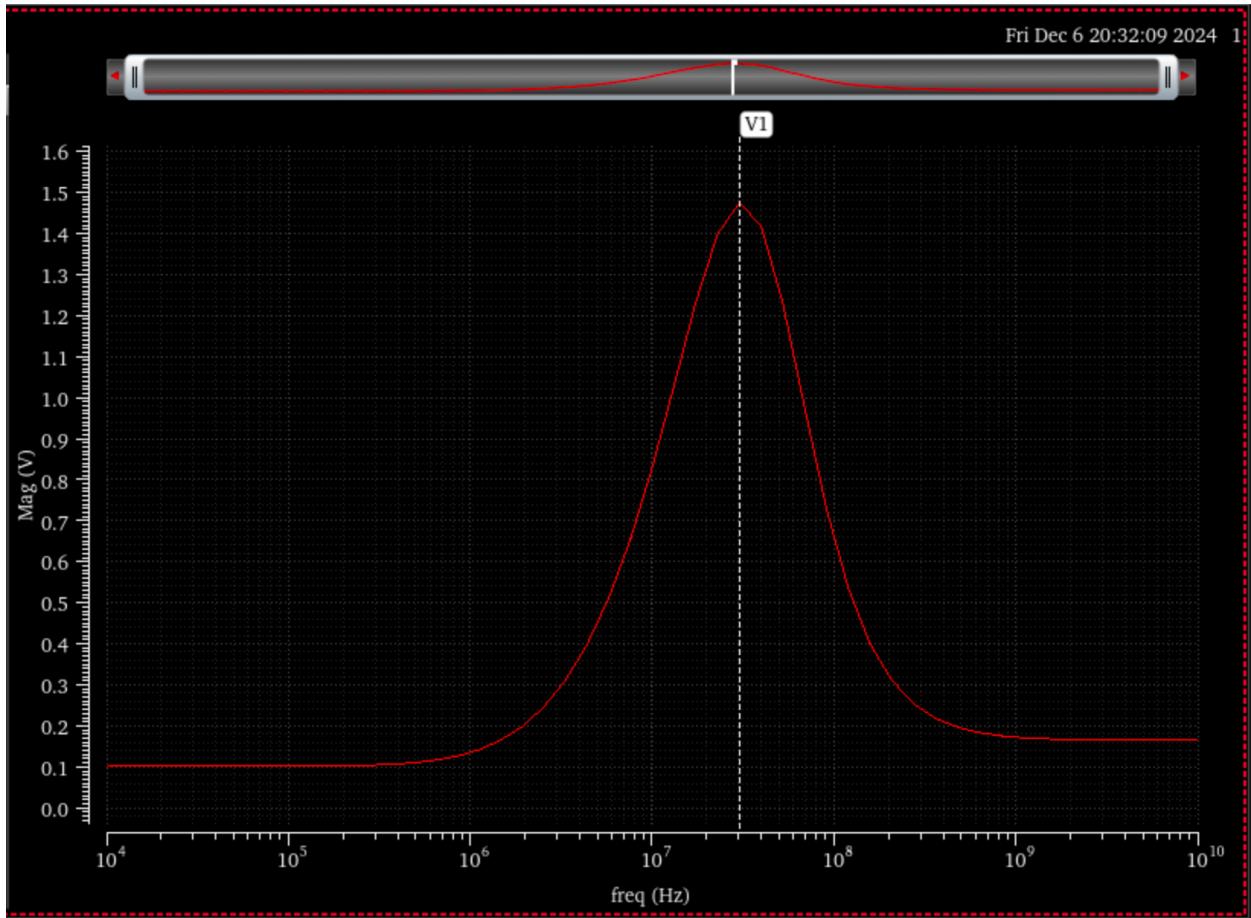


Figure 12: Frequency Response from AC Sweep Simulation with no phase shift at both inputs

Discussion

Voltage Transfer Characteristic:

The common mode voltage is chosen at 0.557V. Around the linear region of it, we calculate the DC gain by finding the slope, $A_d = \frac{\Delta V_o}{\Delta V_{id}} = 30.58$.

Frequency Response:

Gain at DC is around 16.47V/V and it's above the 15V/V design criteria. The DC gain in decibel is 24.3315dB, the -3dB gain is labeled around 21.2267dB at 28.27MHz. This yields a gain bandwidth product of $21.2267 \times 28.27 \times 10^6 = 600$ MHz, well above the 10MHz design criteria.

Common Mode Rejection:

The common mode gain plot is displaying a peak at around 30.2MHz while being small around very low and very high frequencies. Exporting both the common mode gain data and the differential gain data from the frequency response, we found that our designed differential amplifier circuit has a CMRR of around 162dB at low frequency and rolls off after the frequency exceeds around 200kHz.

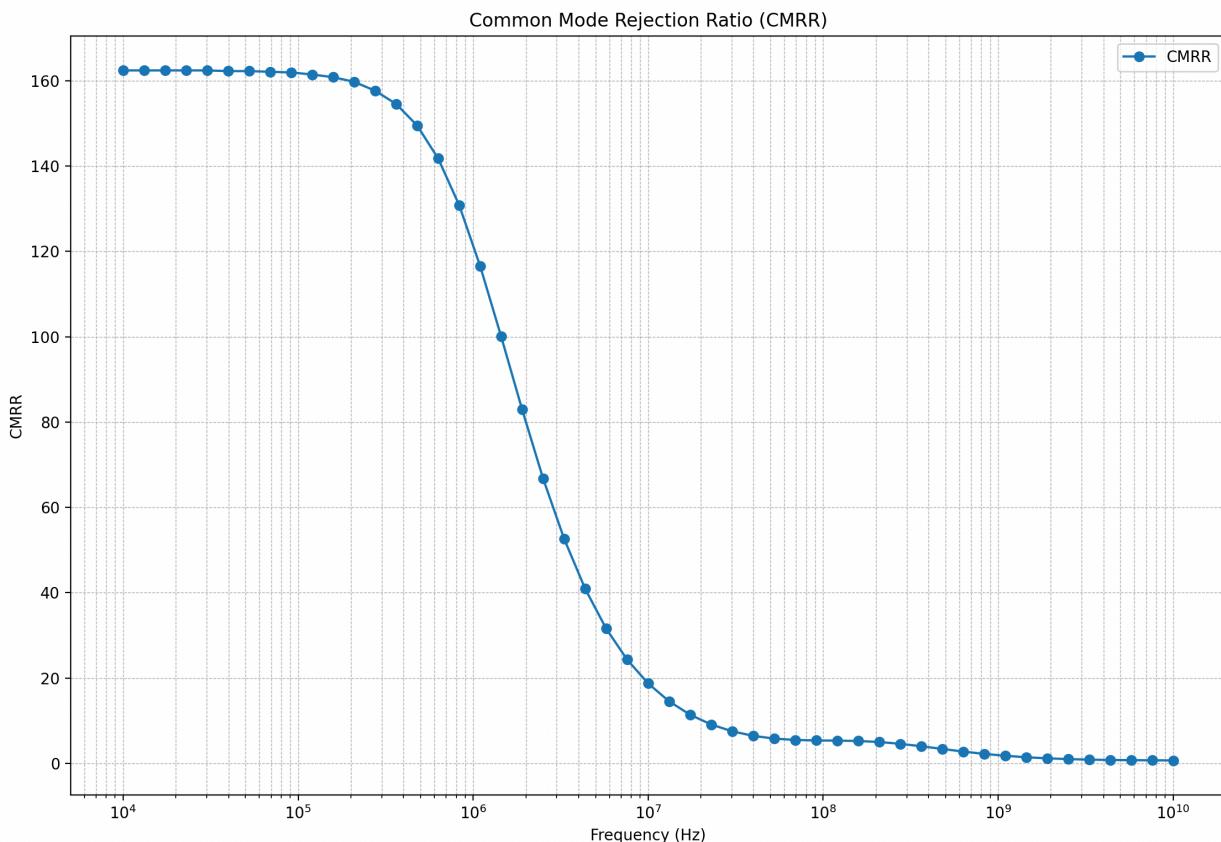


Figure 13: Common Mode Rejection Ratio from 10kHz to 10GHz