

# MTE421 Project 1

Common Source Amplifier with a PMOS current mirror active load

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## Introduction

This project aims to familiarize myself with the Cadence software, including but not limited to schematic capture and analog design simulations. The project starts off by extracting key parameters from both an N-Channel MOSFET (NMOS) and a P-Channel MOSFET (PMOS). Then I will perform a small signal analysis of the common source amplifier circuit with the PMOS current mirror as its load. A maximum bias current will then be calculated using the 5 V/V minimum gain requirement. Lastly, the paper designed circuit will be transferred into Cadence and multiple simulations will be run to analyze this circuit. Based on the simulations, this project will report the relationship between the circuit's intrinsic gain and current density across different biasing current, length and width of the MOSFETs.

## Parameter Extraction

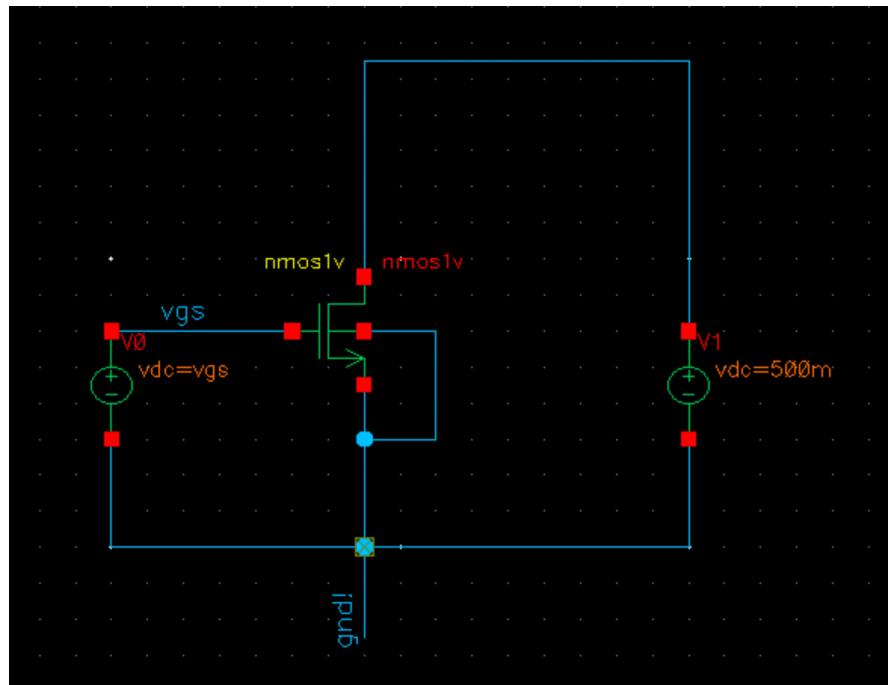


Figure 1: NMOS Parameter Extraction Circuit

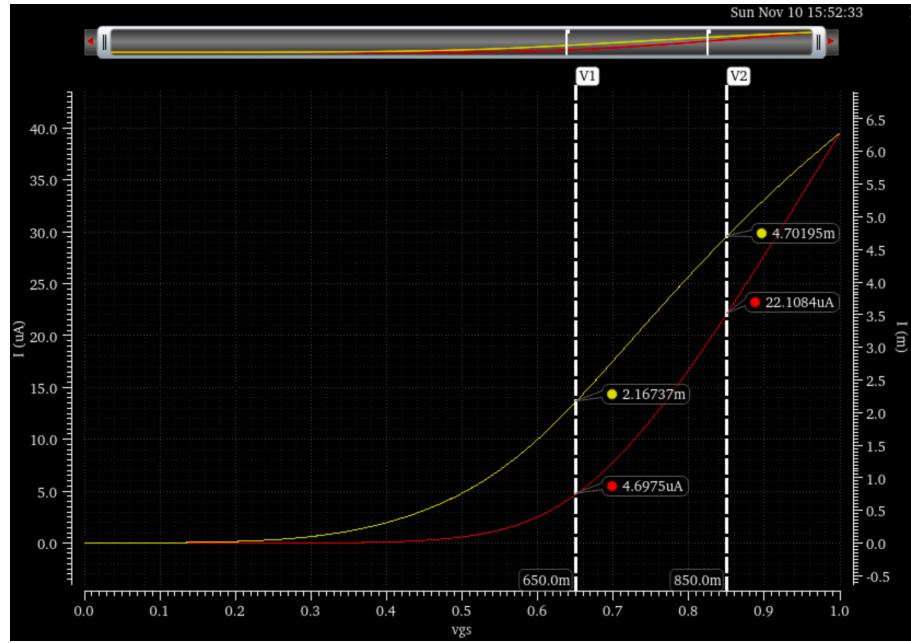
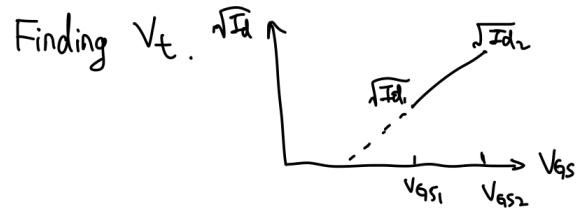


Figure 2: Plot of NMOS  $I_D$  (Red) and  $\sqrt{I_D}$  (Yellow)

The process started from building the circuit schematic and sweeping the  $V_{GS}$  to generate a plot showing  $I_D$  v.s.  $V_{GS}$ .



$$\sqrt{I_d} = \underbrace{\sqrt{\frac{k_n}{2}}}_{\text{slope}} (V_{GS} - V_t)$$

$$\sqrt{I_d} = 0 \Rightarrow V_{GS_1} - V_t = \frac{\sqrt{I_{d_1}}}{\text{slope}} \Rightarrow V_t = V_{GS_1} - \frac{\sqrt{I_{d_1}}}{\text{slope}}$$

$$\text{slope} = \frac{4.70195 - 2.16737}{850 - 650} = 0.01267$$

$$V_t = V_{GS_1} - \frac{\sqrt{I_{d_1}}}{\text{slope}} = 650 - \frac{2.16737}{0.01267} = \boxed{480 \text{ mV}}$$

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2$$

$$4.6975 \mu A = \frac{\mu_n C_{ox}}{2} \cdot \frac{120}{45} (0.65 - 0.48)^2$$

$$\mu_n C_{ox} = 121.91 \frac{\mu A}{V^2}$$

Figure 3: Calculation Steps to find NMOS  $V_t$  and  $\mu_n C_{ox}$

By assuming the NMOS is in the saturation region, its drain current  $I_D$  can be expressed as:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

Taking the square root on both side, I can obtain a linear relationship between  $\sqrt{I_D}$  and  $V_{GS}$ . By extrapolating the linear part of  $\sqrt{I_D}$ , the root of it yields  $V_t$  as  $\sqrt{I_D} = 0$  has to have  $V_t = V_{GS}$ . Given  $V_t$ ,  $\mu_n C_{ox}$  can be calculated using the original  $I_D$  equation at a DC operating point.

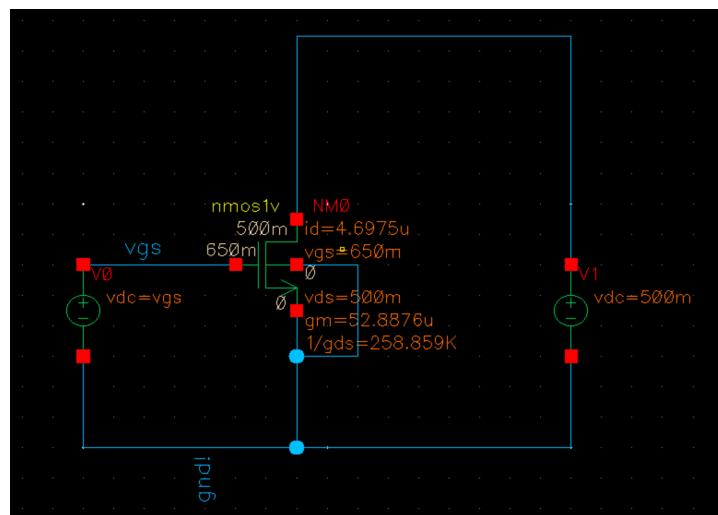
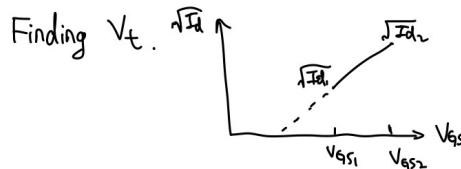
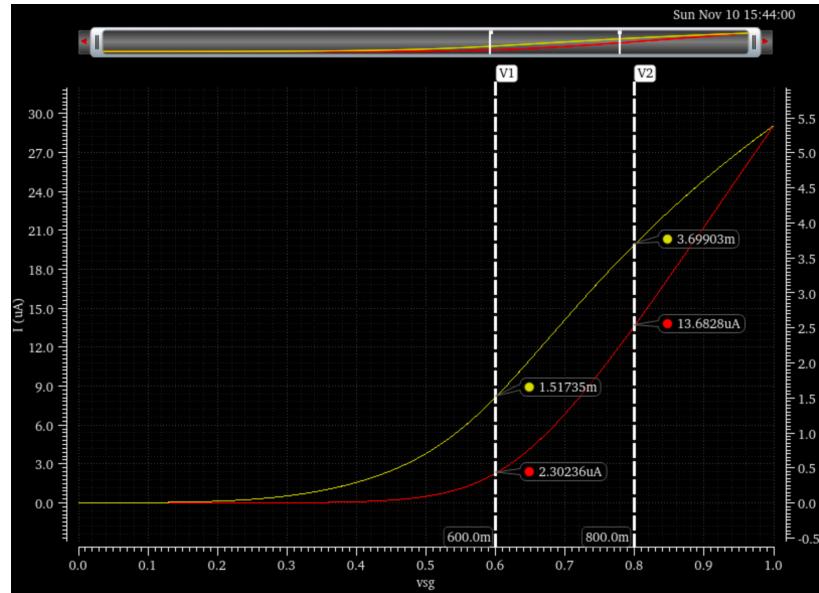


Figure 4: Other NMOS Parameters Calculated by Cadence

At the same point, Cadence also calculated other important parameters such as transconductance  $g_m$  and output resistance  $r_o$  (expressed as  $1/gds$  in Figure 4) which will be used in paper design to meet the amplifier gain requirement.



$$\sqrt{I_d} = \underbrace{\frac{k_n}{2}}_{\text{slope}} (V_{gs} - V_t)$$

$$\sqrt{I_d} = 0 \Rightarrow V_{gs} - V_t = \frac{\sqrt{I_d}}{\text{slope}} \Rightarrow V_t = V_{gs1} - \frac{\sqrt{I_{d1}}}{\text{slope}}$$

$$\text{slope} = \frac{3.69903 - 1.51735}{800 - 600} = 0.01091$$

$$V_t = V_{gs-v_1} - \frac{\sqrt{I_{d-v_1}}}{\text{slope}} = 600 - \frac{1.51735}{0.01091} = \boxed{46 \text{ mV}}$$

$$I_d = \frac{M_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_t)^2$$

$$2.30236 \mu\text{A} = \frac{M_n C_{ox}}{2} \cdot \frac{120}{45} (0.6 - 0.461)^2$$

$$\mu_n C_{ox} = 89.373 \frac{\mu\text{A}}{\text{V}^2}$$

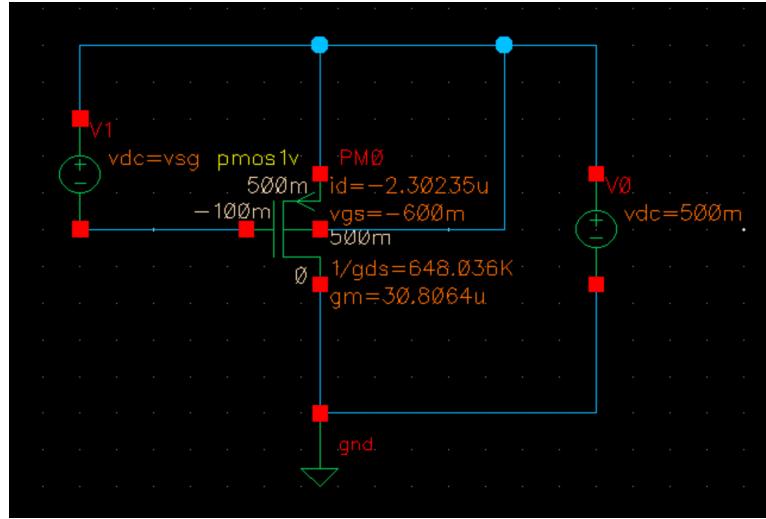


Figure 5: PMOS Parameterization Steps

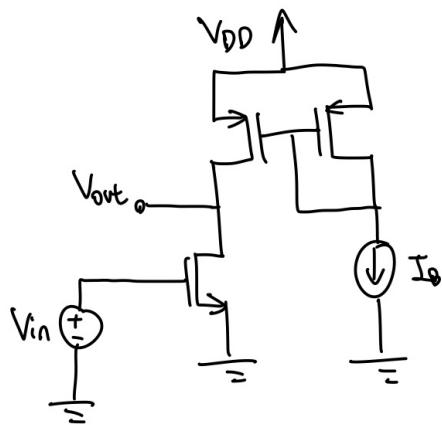
Table 1: NMOS & PMOS design parameters

Parameter	NMOS	PMOS
$ V_t $	0.48 V	0.461 V
$\mu_n C_{ox}$	$121.91 \mu\text{A/V}^2$	$89.373 \mu\text{A / V}^2$
$I_d$	$4.6975 \mu\text{A}$	$2.30235 \mu\text{A}$
$g_m$	$52.8876 \mu\text{A / V}$	$30.8064 \mu\text{A / V}$
$r_o$	$258.859 \text{k}\Omega$	$648.036 \text{k}\Omega$

## Paper Design

With all design parameters available, I moved on to design the common source amplifier circuit on paper. The design started off with a basic NMOS common source amplifier with its input connected to its gate and output to its drain. The load is replaced by a PMOS current mirror circuit to meet the project requirement. Next step was to perform a small signal analysis of the circuit and calculate the bias current. Lastly, I calculated the theoretical gain of the circuit to make sure that its gain meets the 5 V/V requirement.

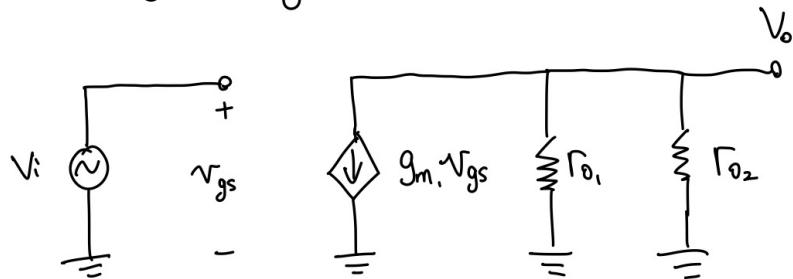
# C.S. Amp Circuit Design.



$$V_{DD} = 1V, A_V = 5\%$$

$$I_B = ?$$

Small Signal Analysis



$$V_o = -g_m V_{gs} (R_{o1} \parallel R_{o2})$$

$$= -g_m V_{in} (R_{o1} \parallel R_{o2})$$

$$\frac{V_o}{V_{in}} = A_v = -g_m (R_{o1} \parallel R_{o2})$$

$$\frac{V_{out}}{V_{in}} = A_v = g_m (R_{o1} \parallel R_{o2}) > 5$$

$$52.8876 \times 10^{-3} \left( \frac{R_{o1} R_{o2}}{R_{o1} + R_{o2}} \right) > 5$$

$$\frac{r_{o_1} r_{o_2}}{r_{o_1} + r_{o_2}} > 94.54$$

$$r_{o_1} r_{o_2} > 94.54 r_{o_1} + 94.54 r_{o_2}$$

$$r_{o_1} r_{o_2} - 94.54 r_{o_2} > 94.54 r_{o_1}$$

$$r_{o_2} > \frac{94.54 r_{o_1}}{r_{o_1} - 94.54}$$

$$r_{o_2} > 148.933 \text{ k}\Omega .$$

Find PMOS channel length modulation parameter  $\lambda$  from existing parameters

$$R_{o\text{-pmos}} = \frac{1}{\lambda I_D} \quad @ I_D = 2.30235 \mu\text{A} .$$

$$648.036 = \frac{1}{\lambda 2.30235 \times 10^{-3}}$$

$$\lambda = 0.67024$$

Find bias current using  $\lambda$ .

$$r_{o_2} > 148.933 \text{ k}\Omega .$$

$$\Rightarrow \frac{1}{\lambda I_D} > 148.933 \text{ k}\Omega$$

$$I_D < 0.01 \text{ mA} .$$

$$\Rightarrow I_B < 0.01 \text{ mA} .$$

Figure 6: Paper Design Steps

## Simulation

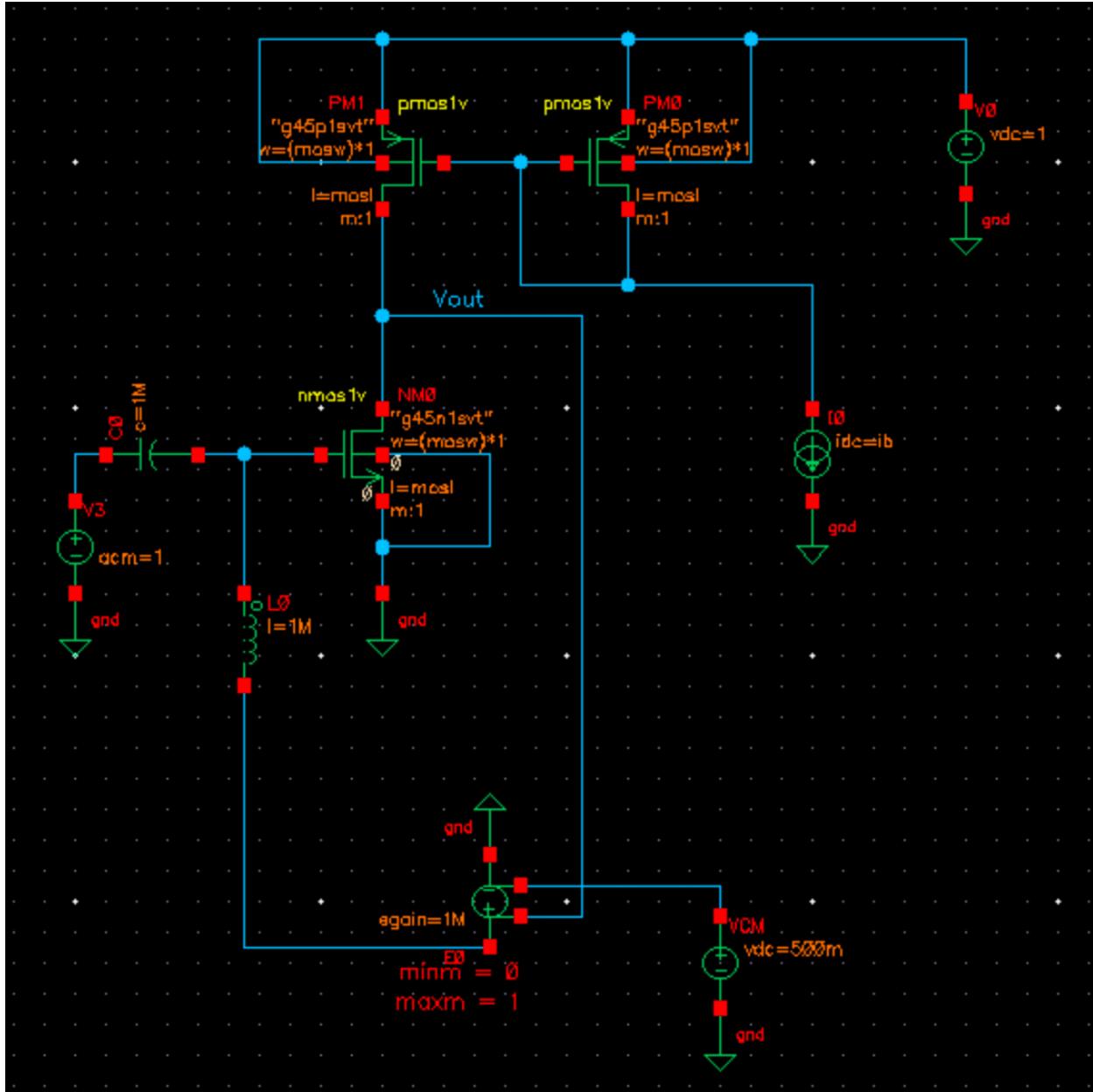


Figure 7: Common Source Amplifier Circuit Implementation in Cadence

The designed circuit was then implemented in Cadence with two modifications at the input. The error amplifier serves as a DC offset to the input AC signal, and the inductor and the capacitor block AC from the input voltage source and DC from error amplifier output respectively.

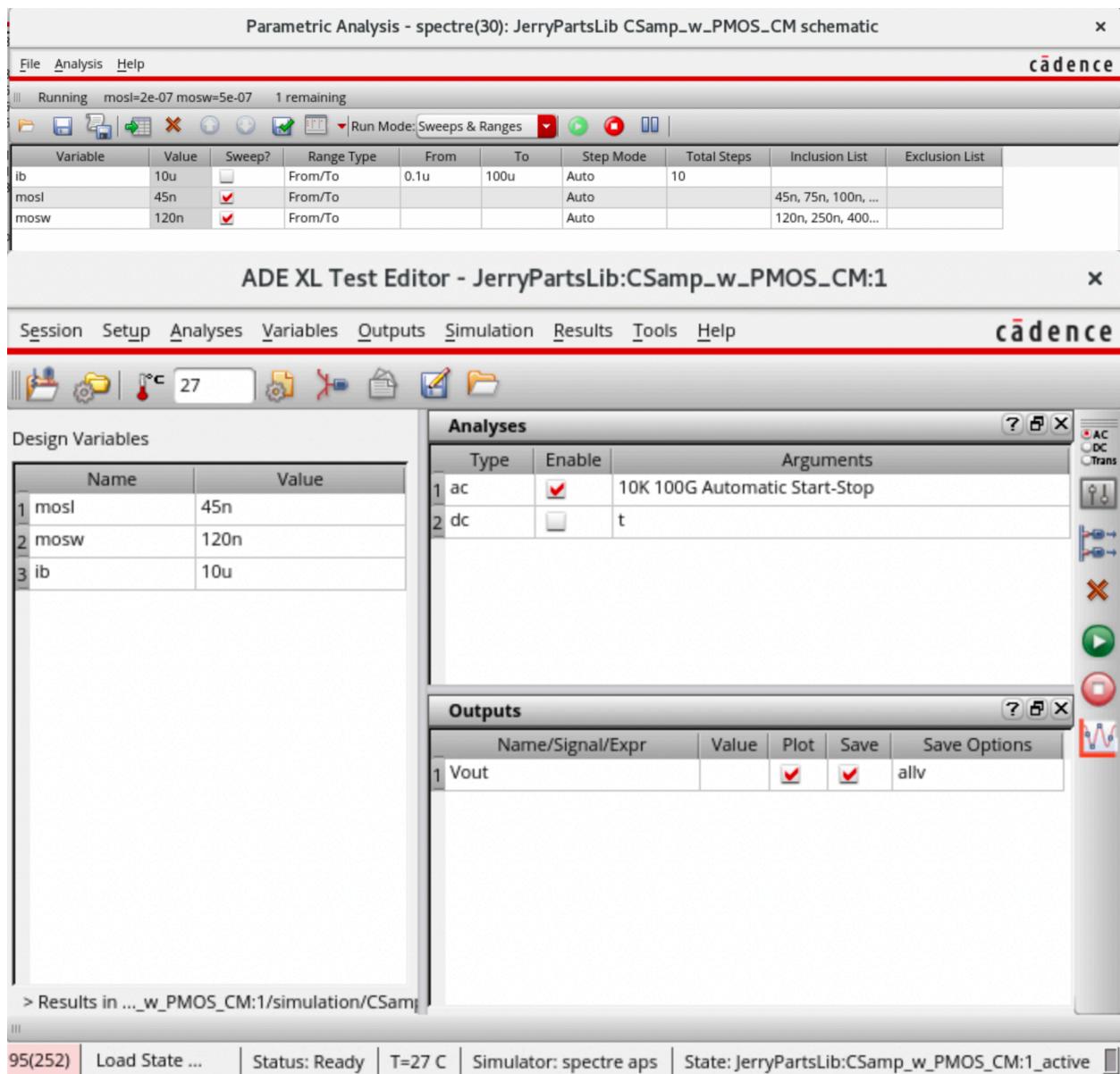


Figure 8: Simulation Settings

Next, I set up an AC sweep from 10 kHz to 100 GHz to observe the amplifier's gain with different parameters. Lastly, I configured parameterization analysis to plot 10 different contours of bias current from 0.1  $\mu$ A to 100  $\mu$ A, MOSFET width of [45 nm, 75 nm, 100 nm, 150 nm, 200 nm] and MOSFET length of [120 nm, 250 nm, 400 nm, 500 nm, 600 nm]. The default bias current is set to 10  $\mu$ A as calculated from the paper design. The default width and length of the MOSFET is set to 120 nm and 45 nm respectively. The parameters are chosen to ensure the simulation covers a wide range of cases, allowing me to draw conclusions about the relationships between various parameters and the gain of the amplifier circuit.

In the discussion section, I will analyze the relationship between bias current and the amplifier's gain, as well as between MOSFET area and the amplifier's gain.

## Discussion

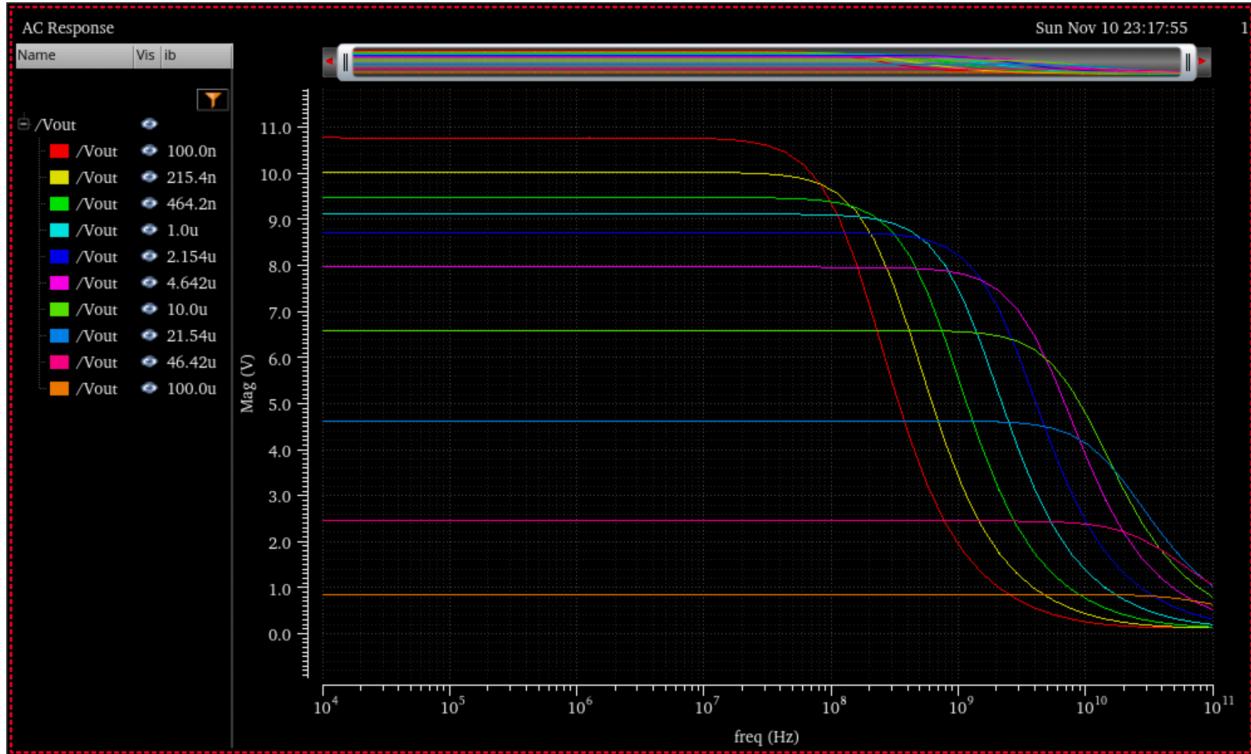


Figure 9: Contours of Different Bias Current against Amplifier Gain

Running the simulation of various bias current, it is observed that decreasing the bias current would increase the amplifier's gain. In the designed circuit, the bias current is the same as the drain current flowing through the NMOS amplifier. From the output resistance equation,  $r_o = \frac{1}{\lambda I_D}$ , it can be observed that decreasing  $I_D$

would increase  $r_o$ , which in turn would increase the intrinsic gain of the amplifier given that  $A_v = g_m r_o$ .

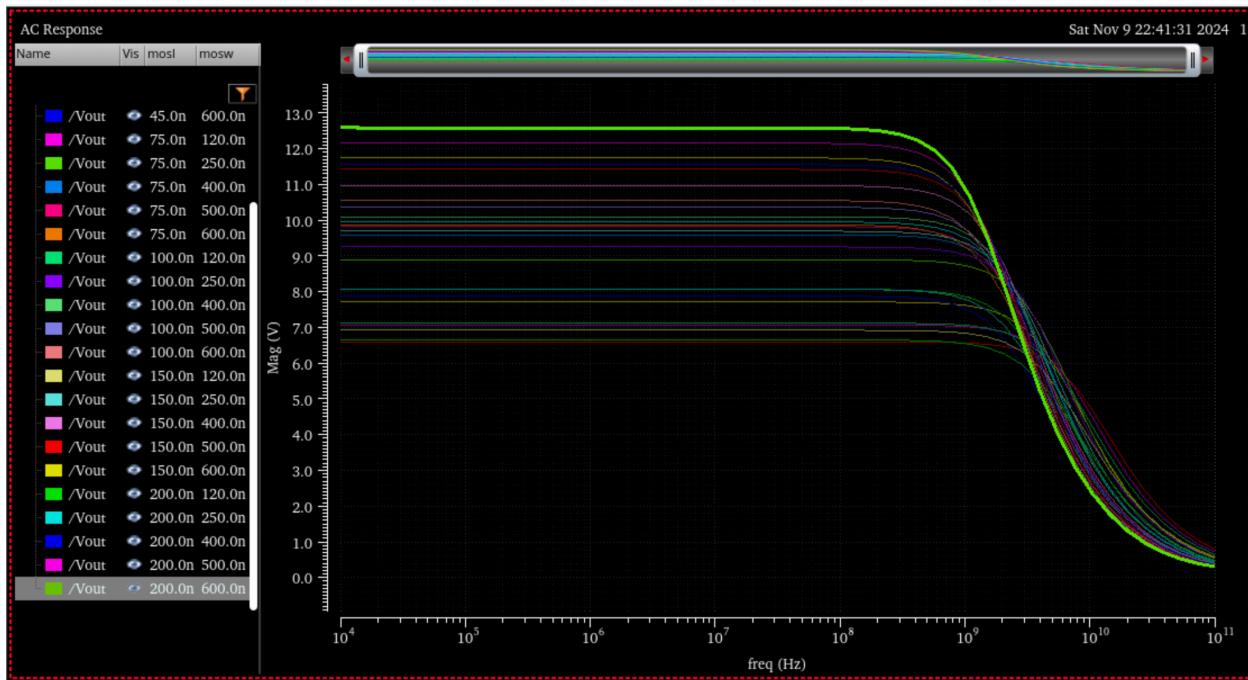


Figure 10: Contours of Different MOSFET Dimensions against Amplifier Gain

Running the simulation again with various MOSFET width and length settings, I observed that increasing the MOSFET dimensions generally leads to a higher amplifier gain. The highlighted green line in Figure 10 has the largest MOSFET dimension and it provides the largest gain. However, increasing MOSFET area doesn't always lead to a higher amplifier gain.

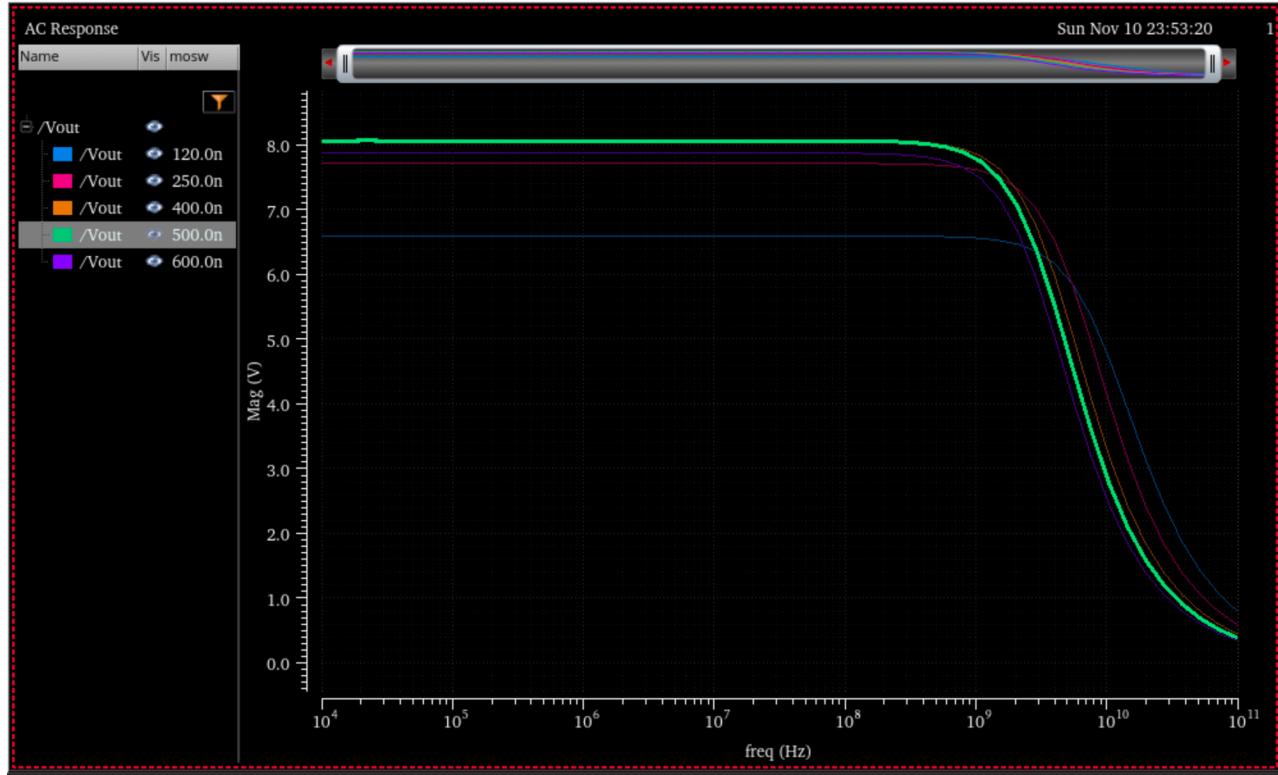


Figure 11: Contours of Different MOSFET Width against Amplifier Gain

After running another simulation where only the MOSFET width is changing from 120 nm to 600 nm, the gain at MOSFET width of 600 nm is smaller than the gain at MOSFET width of 500 nm. The MOSFET dimension is universal to both the NMOS in the common source amplifier circuit and the PMOS in the current mirror circuit. Both PMOS and NMOS contribute to the output resistance of the common source amplifier. Increasing the width while fixing the length may result in a larger enough delta between the PMOS  $r_o$  and the NMOS  $r_o$  such that the combined parallel output resistance is smaller. This observation will need to be further investigated to arrive at a concrete conclusion.

Decreasing the bias current and increasing the MOSFET dimension both decrease the current density which can be expressed as  $\frac{I_D}{wl}$ . Overall, from the 2 parametric simulations, I arrived to a conclusion that decreasing the current density leads to an increase in the amplifier's intrinsic gain. However, in some cases, increasing the MOSFET width in specific ranges may decrease the gain.