COA Final Project

Logism Evaluation Documentation

Delali

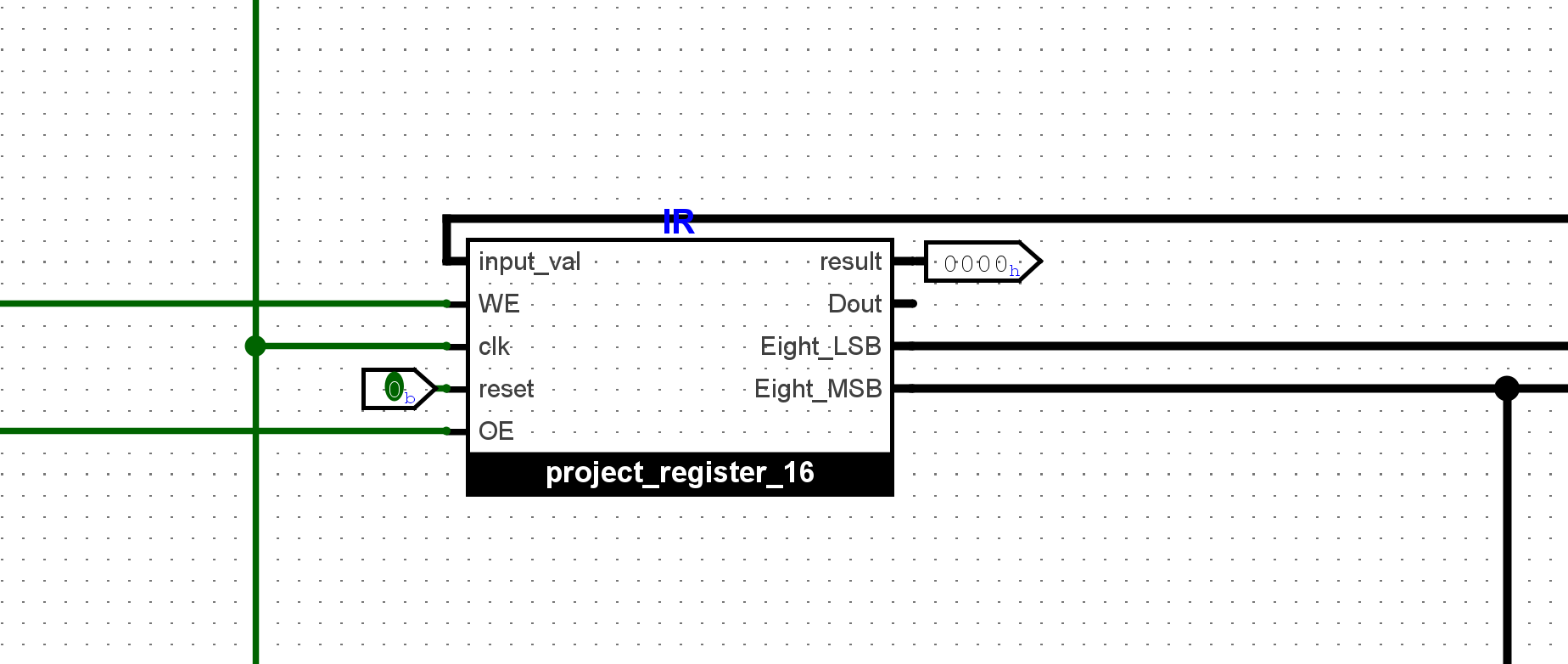
Hutton

Victor

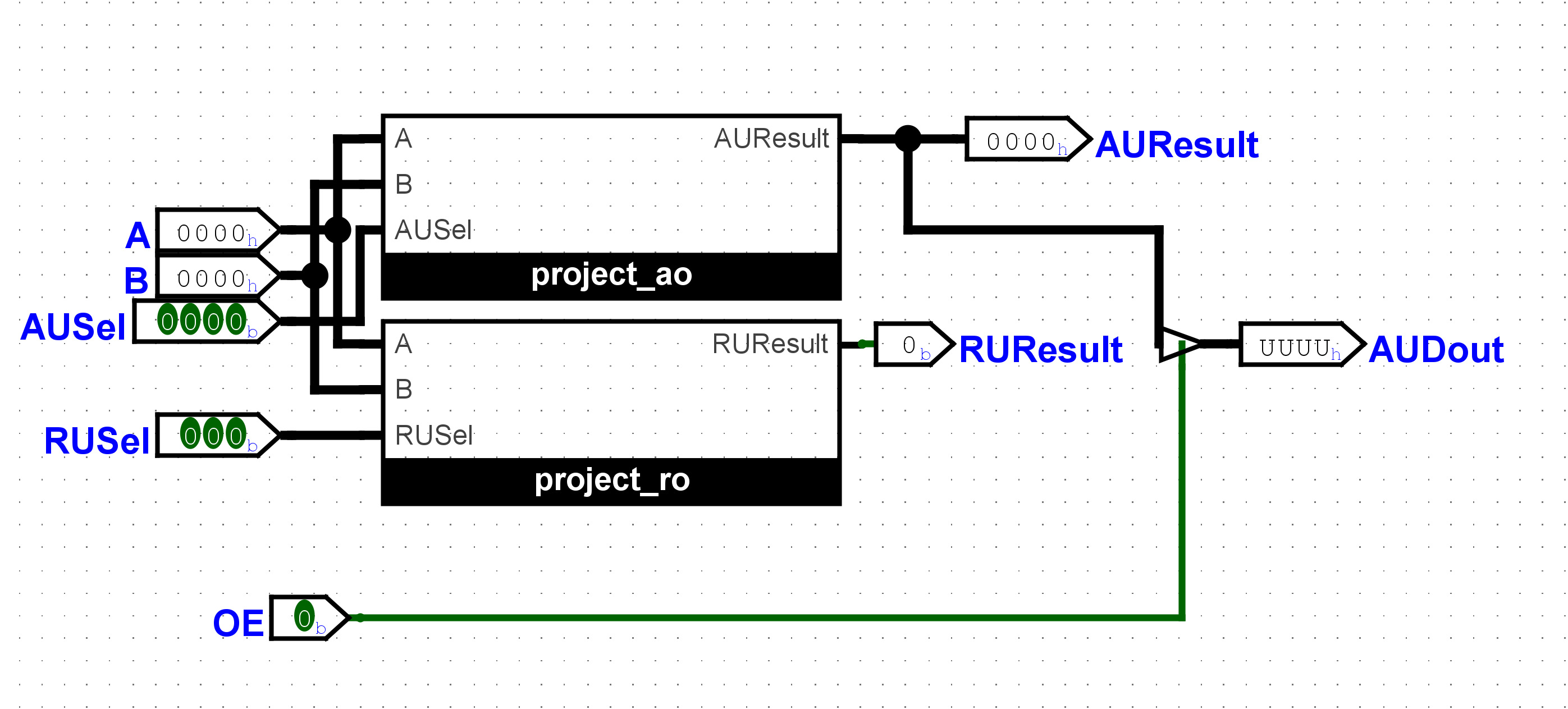
5th August 2024

1. CPU Design Architecture

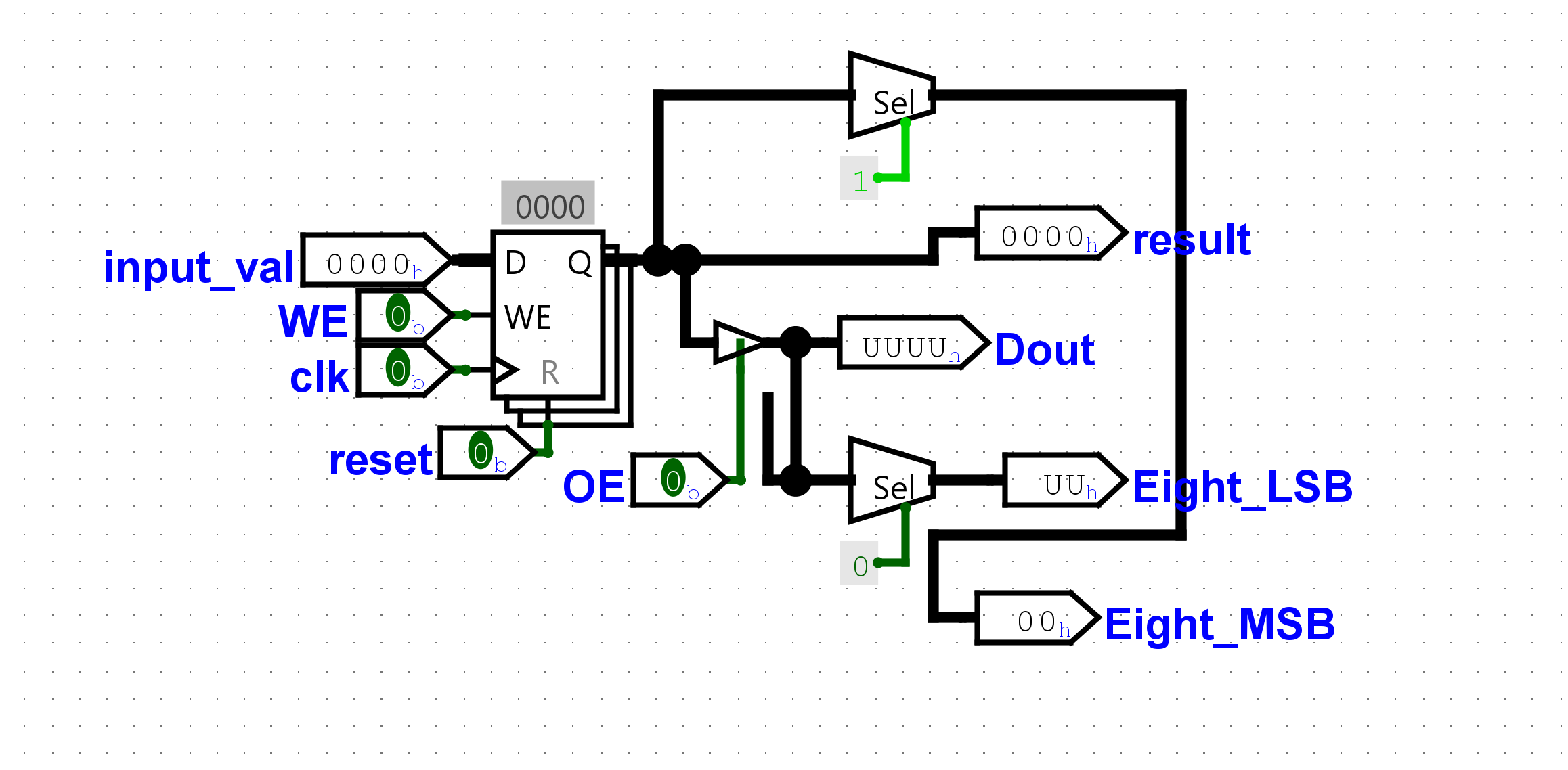
Instruction Register (IR) 16 bits



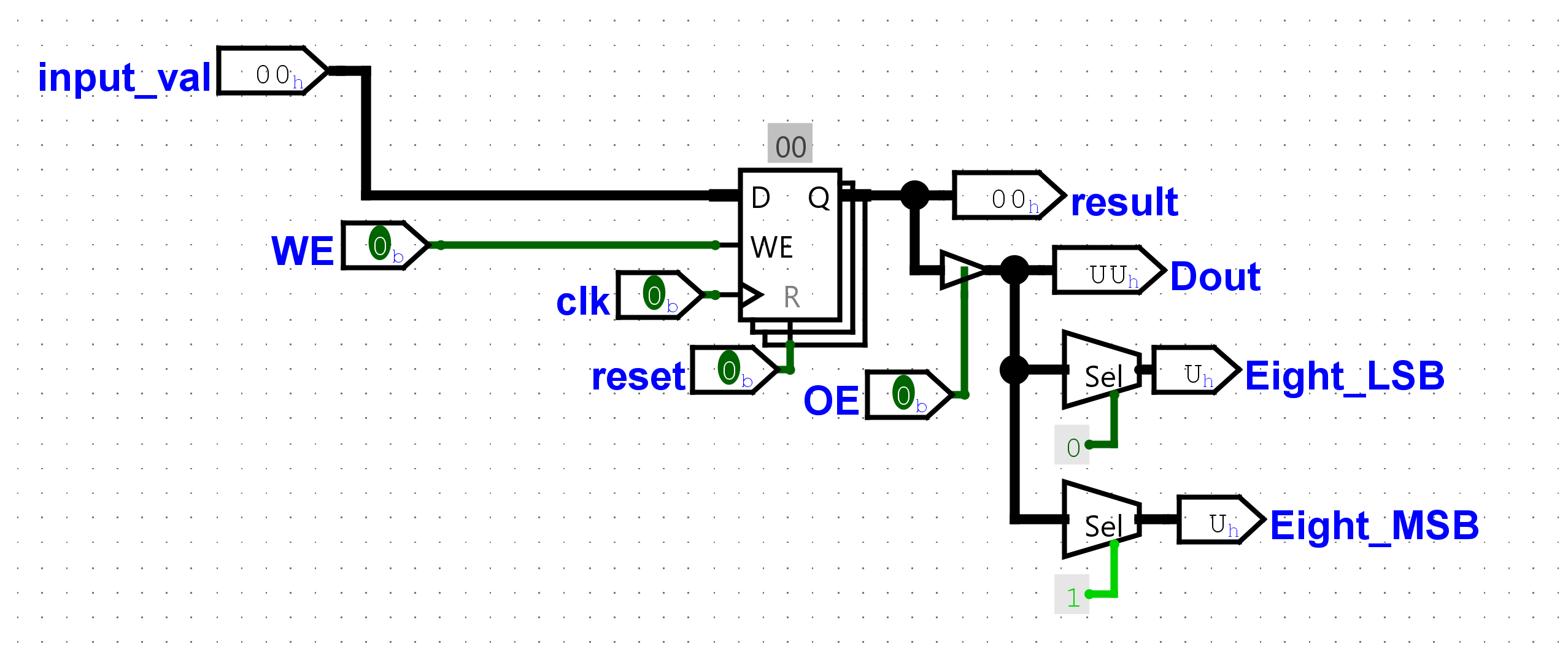
Arithmetic Logic Unit (ALU) 16 bits



16-bit-Register (Output Register, RegA, RegB, MBR)



8-bit-Register (MAR)



1. Datapath Design

|  |  |  |
| --- | --- | --- |
| 1. **Memory Address** | **Content** | **Hex** |
| 0000 | **00000000 00001010** | 000A |
| 0001 | 00000001 00001101 | 010D |
| 0010 | 00000010 00000000 | 0200 |
| 0011 | 00000011 00001100 | 030C |
| 0100 | 00000000 00000000 | 0000 |
| 0101 | 00000000 00000000 | 0000 |
| 0110 | 00000000 00000000 | 0000 |
| 0111 | 00000000 00000000 | 0000 |
| 1000 | 00000000 00000000 | 0000 |
| 1001 | 00000000 00000000 | 0000 |
| 1010 | 00000000 00001010 | 000A |
| 1011 | 00000000 00000000 | 0000 |
| 1100 | 00000000 00000000 | 0000 |
| 1101 | 00000000 00001111 | 000F |
| 1110 | 00000000 00000000 | 0000 |
| 1111 | 00000000 00000000 | 0000 |

1. Control Unit Design

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1. Simulation and Testing

