ArmCortexA9 Main Board

Table of Content

Revision History

Rev. Code	Date	Description
A	10/15/2014	Release to Prototype Phase

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

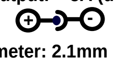
3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

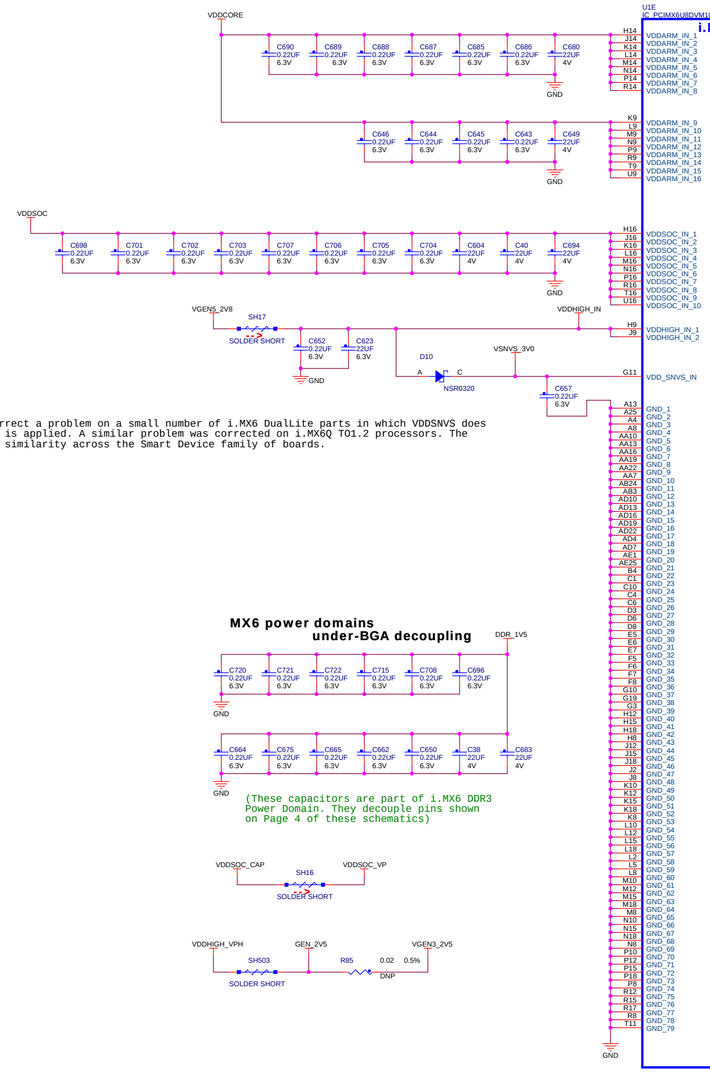
AC ADAPTER SPECIFICATIONS

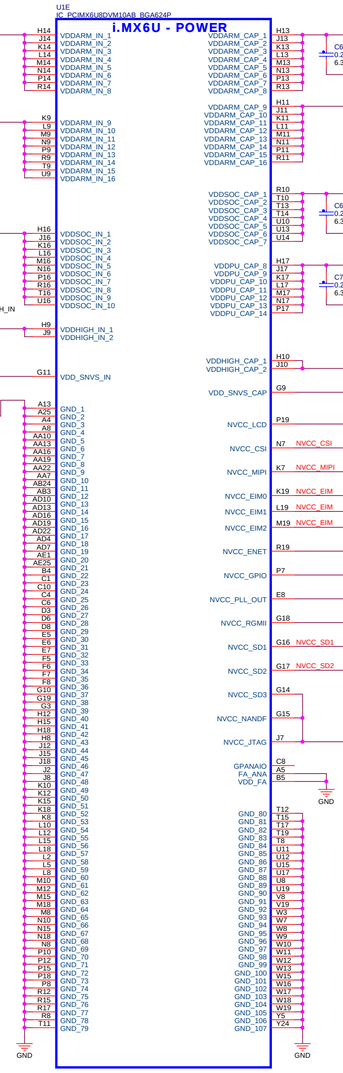
DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity: 
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

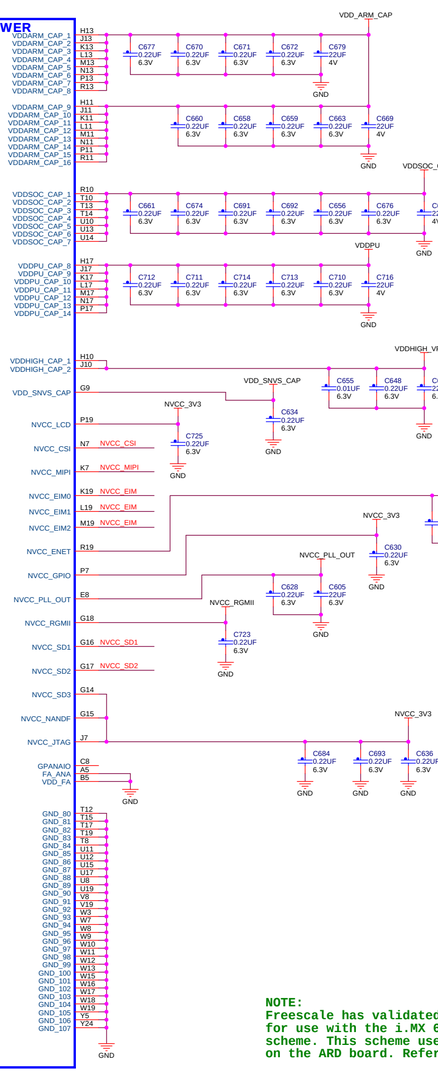
Multimedia Application Division, Wireless & Mobile System Group

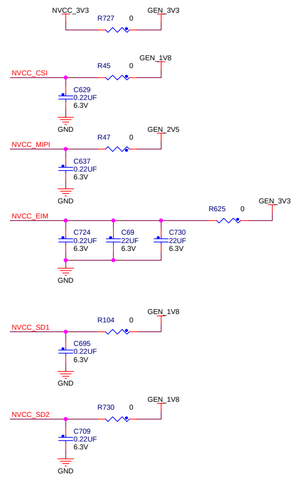
 ICAP Classification: FCP: ____ FIUO: ____ PUBI: __X__

Designer: Mark Middleton	Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**		
Drawn by: Mark Middleton	Page Title: **TITLE PAGE**		
Approved: <Approver>	Size D	Document Number SOURCE:SCH-27417 PDF:SPF-27417	Rev C3
	Date: Saturday, October 18, 2014	Sheet 1 of 25	









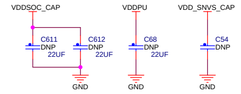
NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and Duallite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

Extra Bulk Capacitors



NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

freescale

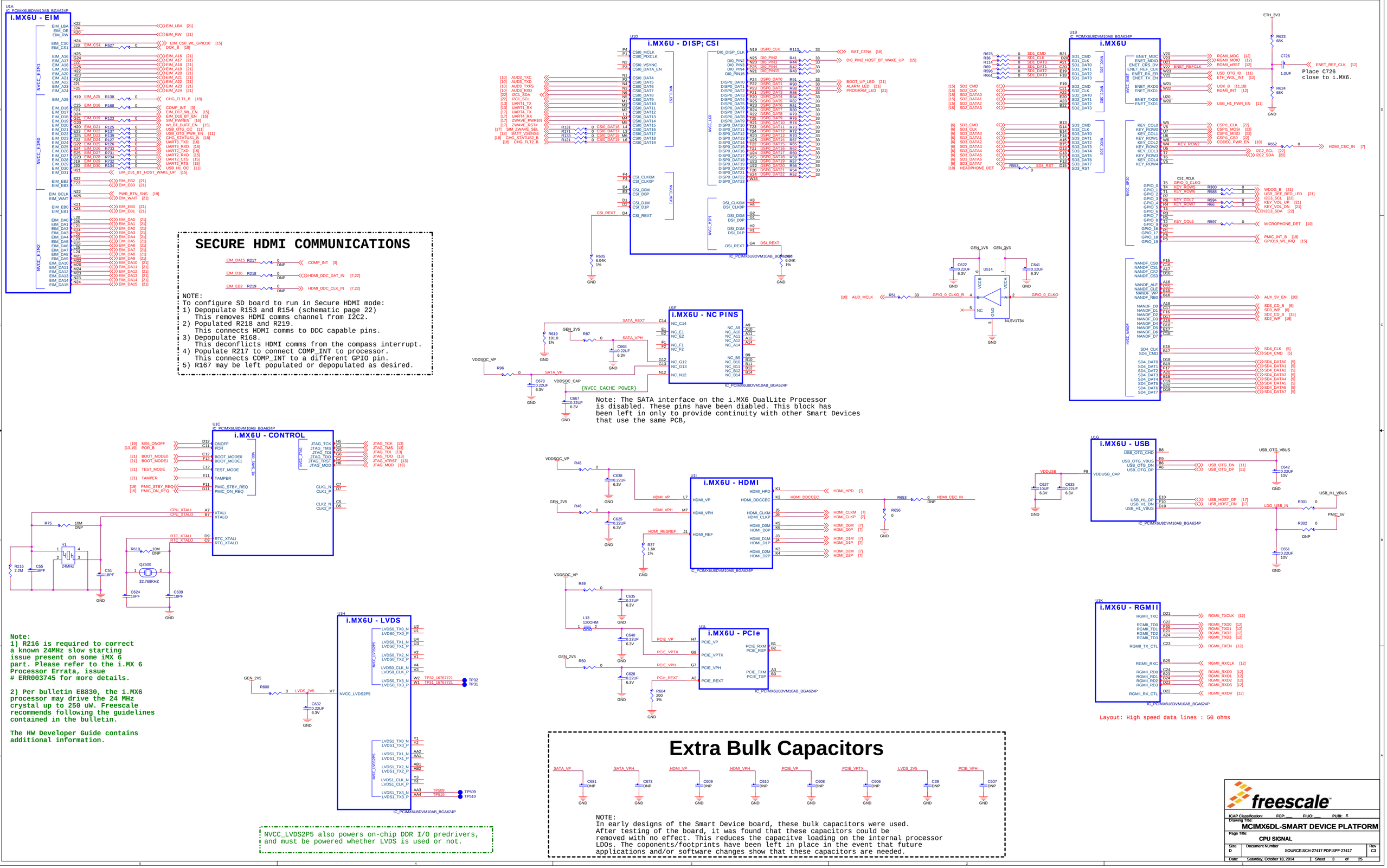
ICAP Classification: FCP: FIUO: PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: CPU POWER

Size	Document Number	Rev
D	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 2 of 25


U1A
IC_PCIMX6U8DVM10AB_BGA624P
i.MX6U - EIM
EIM_LBA K22 EIM_LBA [21]
EIM_OE J24
EIM_RW K20 EIM_RW [21]
EIM_CS0 H24
EIM_CS1 J23 EIM_CS1 R627 0 EIM_CS0_WL_GPIO10 [15]
DOK_B [18]
EIM_A16 H25 EIM_A16 [21]
EIM_A17 G24 EIM_A17 [21]
EIM_A18 J22 EIM_A18 [21]
EIM_A19 G25 EIM_A19 [21]
EIM_A20 H22 EIM_A20 [21]
EIM_A21 H23 EIM_A21 [21]
EIM_A22 F24 EIM_A22 [21]
EIM_A23 J21 EIM_A23 [21]
EIM_A24 F25 EIM_A24 [21]
EIM_A25 H19 EIM_A25 R138 0 CHG_FLT1_B [18]
EIM_D16 C25 EIM_D16 R168 0 COMP_INT [3]
EIM_D17 F21 EIM_D17_WL_EN [15]
EIM_D18 D24 EIM_D18_BT_EN [15]
EIM_D19 G21 EIM_D19 R123 0 SIM_PWREN [16]
EIM_D20 C20 WL_BT_BUFF_EN [15]
EIM_D21 H20 EIM_D21 R125 0 USB_OTG_OC [11]
EIM_D22 E23 EIM_D22 R137 0 USB_OTG_PWR_EN [11]
EIM_D23 D25 EIM_D23 R139 0 CHG_STATUS1_B [18]
EIM_D24 F22 EIM_D24 R127 0 UART3_TXD [16]
EIM_D25 G22 EIM_D25 R126 0 UART3_RXD [16]
EIM_D26 E24 EIM_D26 R733 0 UART2_TXD [15]
EIM_D27 E25 EIM_D27 R731 0 UART2_RXD [15]
EIM_D28 G23 EIM_D28 R734 0 UART2_CTS [15]
EIM_D29 J19 EIM_D29 R732 0 UART2_RTS [15]
EIM_D30 J20 EIM_D30 R134 0 USB_H1_OC [11]
EIM_D31 H21 EIM_D31_BT_HOST_WAKE_UP [15]
EIM_EB2 E22 EIM_EB2 [21]
EIM_EB3 F23 EIM_EB3 [21]
EIM_BCLK N22 PWR_BTN_SNS [19]
EIM_WAIT M25 EIM_WAIT [21]
EIM_EB0 K21 EIM_EB0 [21]
EIM_EB1 K23 EIM_EB1 [21]
EIM_DA0 L20 EIM_DA0 [21]
EIM_DA1 L21 EIM_DA1 [21]
EIM_DA2 K24 EIM_DA2 [21]
EIM_DA3 L22 EIM_DA3 [21]
EIM_DA4 L23 EIM_DA4 [21]
EIM_DA5 K25 EIM_DA5 [21]
EIM_DA6 L25 EIM_DA6 [21]
EIM_DA7 L24 EIM_DA7 [21]
EIM_DA8 M21 EIM_DA8 [21]
EIM_DA9 M22 EIM_DA9 [21]
EIM_DA10 M20 EIM_DA10 [21]
EIM_DA11 M24 EIM_DA11 [21]
EIM_DA12 M23 EIM_DA12 [21]
EIM_DA13 N23 EIM_DA13 [21]
EIM_DA14 N24 EIM_DA14 [21]
EIM_DA15 P24 EIM_DA15 [21]
NVCC_EIM1
NVCC_EIM0
NVCC_EIM2
SECURE HDMI COMMUNICATIONS
EIM_DA15 R217 0 DNP COMP_INT [3]
EIM_D16 R218 0 DNP HDMI_DDC_DAT_IN [7,22]
EIM_EB2 R219 0 DNP HDMI_DDC_CLK_IN [7,22]
NOTE:
To configure SD board to run in Secure HDMI mode:
1) Depopulate R153 and R154 (schematic page 22)
This removes HDMI comms channel from I2C2.
2) Populated R218 and R219.
This connects HDMI comms to DDC capable pins.
3) Depopulate R168.
This deconflicts HDMI comms from the compass interrupt.
4) Populate R217 to connect COMP_INT to processor.
This connects COMP_INT to a different GPIO pin.
5) R167 may be left populated or depopulated as desired.
U1D
i.MX6U - DISP; CSI
CSI0_MCLK P4
CSI0_PIXCLK P1
CSI0_VSYNC N2
CSI0_DATA_EN P3
CSI0_DAT4 N1
CSI0_DAT5 P2
CSI0_DAT6 N4
CSI0_DAT7 P3
CSI0_DAT8 N5
CSI0_DAT9 M1
CSI0_DAT10 M3
CSI0_DAT11 M2
CSI0_DAT12 L1
CSI0_DAT13 M4
CSI0_DAT14 M5
CSI0_DAT15 L5
CSI0_DAT16 L4
CSI0_DAT17 L3
CSI0_DAT18 M6
CSI0_DAT19 L6
[10] AUD3_TXC
[10] AUD3_TXD
[10] AUD3_TXFS
[10] AUD3_RXD
[22] I2C1_SDA
[22] I2C1_SCL
[13] UART1_TX
[13] UART1_RX
[17] UART4_TX
[17] UART4_RX
[17] ZWAVE_PWREN
[17] ZWAVE_RST#
[17] SIM_ZWAVE_SEL
[18] BATT_VSENSE
[18] CHG_STATUS2_B
[18] CHG_FLT2_B
R131 0 CSI0_DAT16
R171 0 CSI0_DAT17
R133 0 CSI0_DAT18
R121 0 CSI0_DAT19
NVCC_CSI
CSI_CLK0M F4
CSI_CLK0P F3
CSI_D0M E4
CSI_D0P E3
CSI_D1M D1
CSI_D1P D2
CSI_REXT D4
R605 6.04K 1%
NVCC_CSI1
NVCC_REF1
NVCC_REF2
DI0_DISP_CLK N19 DSP0_CLK R113 33 BAT_CEN# [18]
DI0_PIN2 N25 DI0_PIN2 R41 33 DI0_PIN2_HOST_BT_WAKE_UP [15]
DI0_PIN3 N20 DI0_PIN3 R44 33
DI0_PIN4 P25 DI0_PIN4 R42 33
DI0_PIN15 N21 DI0_PIN15 R40 33
DISP0_DAT0 P24 DSP0_DAT0 R91 33 BOOT_UP_LED [21]
DISP0_DAT1 P22 DSP0_DAT1 R90 33 ALARM_LED [21]
DISP0_DAT2 P23 DSP0_DAT2 R88 33 PROGRAM_LED [21]
DISP0_DAT3 R84 33
DISP0_DAT4 P20 DSP0_DAT4 R84 33
DISP0_DAT5 R25 DSP0_DAT5 R82 33
DISP0_DAT6 R23 DSP0_DAT6 R81 33
DISP0_DAT7 R24 DSP0_DAT7 R80 33
DISP0_DAT8 R22 DSP0_DAT8 R78 33
DISP0_DAT9 T25 DSP0_DAT9 R76 33
DISP0_DAT10 R21 DSP0_DAT10 R74 33
DISP0_DAT11 T23 DSP0_DAT11 R73 33
DISP0_DAT12 T24 DSP0_DAT12 R72 33
DISP0_DAT13 R20 DSP0_DAT13 R70 33
DISP0_DAT14 U25 DSP0_DAT14 R69 33
DISP0_DAT15 T22 DSP0_DAT15 R66 33
DISP0_DAT16 T21 DSP0_DAT16 R60 33
DISP0_DAT17 V25 DSP0_DAT17 R60 33
DISP0_DAT18 U24 DSP0_DAT18 R59 33
DISP0_DAT19 U23 DSP0_DAT19 R57 33
DISP0_DAT20 U22 DSP0_DAT20 R56 33
DISP0_DAT21 T20 DSP0_DAT21 R55 33
DISP0_DAT22 V24 DSP0_DAT22 R53 33
DISP0_DAT23 W24
NVCC_LCD
DSI_CLK0M H3
DSI_CLK0P H4
DSI_D0M G2
DSI_D0P G1
DSI_D1M H2
DSI_D1P H1
DSI_REXT G4 DSI_REXT
R606 6.04K 1%
NVCC_MIPI
IC_PCIMX6U8DVM10AB_BGA624P
U1B
i.MX6U
SD1_CMD B21 SD1_CMD
SD1_CLK D20 SD1_CLK
SD1_DAT0 A21 SD1_DAT0
SD1_DAT1 C20 SD1_DAT1
SD1_DAT2 E19 SD1_DAT2
SD1_DAT3 F18 SD1_DAT3
R676 0 SD1_CMD
R36 0 SD1_CLK
R114 0 SD1_DAT0
R69 0 SD1_DAT1
R596 0 SD1_DAT2
R661 0 SD1_DAT3
NVCC_SD1
SD2_CMD F19 SD2_CMD
SD2_CLK C21 SD2_CLK
SD2_DAT0 E20 SD2_DAT0
SD2_DAT1 A23 SD2_DAT1
SD2_DAT2 B22 SD2_DAT2
SD2_DAT3 SD2_DAT3
[15] SD2_CMD
[15] SD2_CLK
[15] SD2_DAT0
[15] SD2_DAT1
[15] SD2_DAT2
[15] SD2_DAT3
NVCC_SD2
SD3_CMD B13 SD3_CMD
SD3_CLK D14 SD3_CLK
SD3_DAT0 E14 SD3_DAT0
SD3_DAT1 A15 SD3_DAT1
SD3_DAT2 B15 SD3_DAT2
SD3_DAT3 D13 SD3_DAT3
SD3_DAT4 C13 SD3_DAT4
SD3_DAT5 E13 SD3_DAT5
SD3_DAT6 F13 SD3_DAT6
SD3_DAT7 D15 SD3_DAT7
SD3_RST SD3_RST
[6] SD3_CMD
[6] SD3_CLK
[6] SD3_DAT0
[6] SD3_DAT1
[6] SD3_DAT2
[6] SD3_DAT3
[6] SD3_DAT4
[6] SD3_DAT5
[6] SD3_DAT6
[6] SD3_DAT7
[10] HEADPHONE_DET
R553 0 SD3_RST
NVCC_SD3
ENET_MDC V20 RGMII_MDC [12]
ENET_MDIO V23 RGMII_MDIO [12]
ENET_CRS_DV V21 RGMII_nRST [12]
ENET_REF_CLK V22 ENET_REFCLK
ENET_RX_ER W23 USB_OTG_ID [11]
ENET_TX_EN V21 ETH_WOL_INT [12]
ENET_RXD0 W21 UOK_B [11,18]
ENET_RXD1 W22 RGMII_INT [12]
ENET_TXD0 U20
ENET_TXD1 W20 USB_H1_PWR_EN [11]
NVCC_ENET
ETH_3V3
R623 68K
C726 1.0UF
R624 68K
GND
Place C726 close to i.MX6.
KEY_COL0 V5 CSPI1_CLK [22]
KEY_ROW0 V6 CSPI1_MOSI [22]
KEY_COL1 U6 CSPI1_MISO [22]
KEY_ROW1 V4 CSPI1_CS0 [22]
KEY_COL2 W4 KEY_ROW2 CODEC_PWR_EN [10]
KEY_ROW2 U5 I2C2_SCL [22]
KEY_COL3 T7 I2C2_SDA [22]
KEY_ROW3 T6
KEY_COL4 U7
KEY_ROW4 T5
R652 0 HDMI_CEC_IN [7]
CSI_MCLK
GPIO_0 T5 GPIO_0_CLKO
GPIO_1 T4 KEY_ROW5 R300 0 WDOG_B [21]
GPIO_2 T1 KEY_ROW6 R588 0 USR_DEF_RED_LED [21]
GPIO_3 R7 I2C3_SCL [22]
GPIO_4 R6 KEY_COL7 R594 0 KEY_VOL_UP [21]
GPIO_5 R4 KEY_ROW7 R66 0 KEY_VOL_DN [21]
GPIO_6 T3 I2C3_SDA [22]
GPIO_7 R3
GPIO_8 R5
GPIO_9 T2 KEY_COL6 R597 0 MICROPHONE_DET [10]
GPIO_16 R2
GPIO_17 R1
GPIO_18 P6 PMIC_INT_B [19]
GPIO_19 P5 GPIO19_WL_IRQ [15]
NVCC_GPIO
NANDF_CS0 F15
NANDF_CS1 C16
NANDF_CS2 E17
NANDF_CS3 D16
NANDF_ALE A16
NANDF_CLE C15
NANDF_WP E15
NANDF_RB0 B16 AUX_5V_EN [20]
NANDF_D0 A18 SD3_CD_B [6]
NANDF_D1 C17 SD3_WP [6]
NANDF_D2 F16 SD2_CD_B [15]
NANDF_D3 D17 SD2_WP [15]
NANDF_D4 A19
NANDF_D5 B18
NANDF_D6 E17
NANDF_D7 C18
SD4_CLK E16 SD4_CLK [5]
SD4_CMD B17 SD4_CMD [5]
SD4_DAT0 D18 SD4_DAT0 [5]
SD4_DAT1 B19 SD4_DAT1 [5]
SD4_DAT2 F17 SD4_DAT2 [5]
SD4_DAT3 A20 SD4_DAT3 [5]
SD4_DAT4 E18 SD4_DAT4 [5]
SD4_DAT5 C19 SD4_DAT5 [5]
SD4_DAT6 B20 SD4_DAT6 [5]
SD4_DAT7 D19 SD4_DAT7 [5]
NVCC_NAND
GEN_1V8
GEN_3V3
C622 0.22UF 6.3V
C641 0.22UF 6.3V
U514
VCCB
VCCA
GND
NC
NLSV1T34
[10] AUD_MCLK
R51 33 GPIO_0_CLKO_R
GPIO_0_CLKO
U1E
i.MX6U - NC PINS
NC_C14 C14
NC_E1 E1
NC_E2 E2
NC_F1 F1
NC_F2 F2
NC_G12 G12
NC_G13 G13
NC_N12 N12
NC_A9 A9
NC_A10 A10
NC_A11 A11
NC_A12 A12
NC_A14 A14
NC_B9 B9
NC_B10 B10
NC_B11 B11
NC_B12 B12
NC_B14 B14
SATA_REXT
R619 191.0 1%
GEN_2V5
R87 0
SATA_VPH
C668 0.22UF 6.3V
VDDSOC_VP
R96 0
SATA_VP
C678 0.22UF 6.3V
VDDSOC_CAP
{NVCC_CACHE_POWER}
C667 0.22UF 6.3V
Note: The SATA interface on the i.MX6 Duallite Processor is disabled. These pins have been diabled. This block has been left in only to provide continuity with other Smart Devices that use the same PCB,
U1C
i.MX6U - CONTROL
ONOFF D12
POR C11
BOOT_MODE0 C12
BOOT_MODE1 F12
TEST_MODE E12
TAMPER E11
PMIC_STBY_REQ F11
PMIC_ON_REQ D11
[19] MX6_ONOFF
[13,19] POR_B
[21] BOOT_MODE0
[21] BOOT_MODE1
[21] TEST_MODE
[21] TAMPER
[19] PMIC_STBY_REQ
[19] PMIC_ON_REQ
VDD_SNVS_CAP
JTAG_TCK H5 JTAG_TCK [13]
JTAG_TMS C3 JTAG_TMS [13]
JTAG_TDI G5 JTAG_TDI [13]
JTAG_TDO G6 JTAG_TDO [13]
JTAG_TRST C2 JTAG_nTRST [13]
JTAG_MOD H6 JTAG_MOD [13]
NVCC_JTAG
CLK1_N C7
CLK1_P D7
CLK2_N C5
CLK2_P D5
CPU_XTALI A7
CPU_XTALO B7
RTC_XTALI D9
RTC_XTALO C9
R75 10M DNP
Y1 24MHz
R216 2.2M
C55 18PF
C51 18PF
R610 10M DNP
QZ500 32.768KHZ
C624 18PF
C639 18PF
GND
U1F
i.MX6U - HDMI
HDMI_VP L7
HDMI_VPH M7
HDMI_REF J1
HDMI_RESREF
HDMI_HPD K1 HDMI_HPD [7]
HDMI_DDCCEC K2 HDMI_DDCCEC
HDMI_CLKM J5 HDMI_CLKM [7]
HDMI_CLKP J6 HDMI_CLKP [7]
HDMI_D0M K5 HDMI_D0M [7]
HDMI_D0P K6 HDMI_D0P [7]
HDMI_D1M J3 HDMI_D1M [7]
HDMI_D1P J4 HDMI_D1P [7]
HDMI_D2M K3 HDMI_D2M [7]
HDMI_D2P K4 HDMI_D2P [7]
R653 0 DNP HDMI_CEC_IN
R656 0
R48 0
C638 0.22UF 6.3V
R46 0
C625 0.22UF 6.3V
R37 1.6K 1%
U1G
i.MX6U - USB
USB_OTG_CHD B8
USB_OTG_VBUS E9
USB_OTG_DN B6 USB_OTG_DN [11]
USB_OTG_DP A6 USB_OTG_DP [11]
USB_H1_DP E10 USB_HOST_DP [17]
USB_H1_DN F10 USB_HOST_DN [17]
USB_H1_VBUS D10
VDDUSB_CAP F9
VDDUSB
C627 10UF 6.3V
C633 0.22UF 6.3V
USB_OTG_VBUS
C642 0.22UF 10V
USB_H1_VBUS
LDO_USB_IN
R301 0
PMIC_5V
R302 0 DNP
C651 0.22UF 10V
VDDSOC_VP
R49 0
C635 0.22UF 6.3V
L13 120OHM
C640 0.22UF 6.3V
GEN_2V5
R50 0
C626 0.22UF 6.3V
R604 200 1%
U1H
i.MX6U - LVDS
LVDS0_TX0_N U2
LVDS0_TX0_P U1
LVDS0_TX1_N U4
LVDS0_TX1_P U3
LVDS0_TX2_N V2
LVDS0_TX2_P V1
LVDS0_CLK_N V4
LVDS0_CLK_P V3
LVDS0_TX3_N W2 TP32_16767721 TP32
LVDS0_TX3_P W1 TP31_16767721 TP31
LVDS1_TX0_N Y1
LVDS1_TX0_P Y2
LVDS1_TX1_N AA2
LVDS1_TX1_P AA1
LVDS1_TX2_N AB1
LVDS1_TX2_P AB2
LVDS1_CLK_N Y3
LVDS1_CLK_P Y4
LVDS1_TX3_N AA3 TP509 TP509
LVDS1_TX3_P AA4 TP510 TP510
NVCC_LVDS2P5
R600 0 LVDS_2V5
C632 0.22UF 6.3V
U1I
i.MX6U - PCIe
PCIE_VP H7
PCIE_VPTX G8
PCIE_VPH G7
PCIE_REXT A2
PCIE_RXM B1
PCIE_RXP B2
PCIE_TXM A3
PCIE_TXP B3
U1K
i.MX6U - RGMII
RGMII_TXC D21 RGMII_TXCLK [12]
RGMII_TD0 C22 RGMII_TXD0 [12]
RGMII_TD1 F20 RGMII_TXD1 [12]
RGMII_TD2 E21 RGMII_TXD2 [12]
RGMII_TD3 A24 RGMII_TXD3 [12]
RGMII_TX_CTL C23 RGMII_TXEN [12]
RGMII_RXC B25 RGMII_RXCLK [12]
RGMII_RD0 C24 RGMII_RXD0 [12]
RGMII_RD1 B23 RGMII_RXD1 [12]
RGMII_RD2 B24 RGMII_RXD2 [12]
RGMII_RD3 D23 RGMII_RXD3 [12]
RGMII_RX_CTL D22 RGMII_RXDV [12]
Layout: High speed data lines : 50 ohms
Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.
The HW Developer Guide contains additional information.
NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.
Extra Bulk Capacitors
SATA_VP C681 DNP
SATA_VPH C673 DNP
HDMI_VP C609 DNP
HDMI_VPH C610 DNP
PCIE_VP C608 DNP
PCIE_VPTX C606 DNP
LVDS_2V5 C39 DNP
PCIE_VPH C607 DNP
NOTE:
In early designs of the Smart Device board, these bulk capacitors were used.
After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.
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ICAP Classification: FCP:___ FIUO:___ PUBI: X
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM
Page Title: CPU SIGNAL
Size D
Document Number SOURCE:SCH-27417 PDF:SPF-27417
Rev C3
Date: Saturday, October 18, 2014
Sheet 3 of 25

Clock terminators: Place at end of route at each DDR pair

DRAM_SDCLK0 — R118 200 1% — DRAM_SDCLK0_B

DRAM_SDCLK1 — R43 200 1% — DRAM_SDCLK1_B

GND probe pads: TP17, TP16 (GND, GND)

U1J
IC_PCIMX6U8DVM10AB_BGA624P

i.MX6U - DDR

DRAM_D[63:0]

DRAM_A[15:0]

U3 — 2G_DDR3_SDRAM_128MX16 — Top right

DDR_1V5

MT41K128M16JT

U5 — 2G_DDR3_SDRAM_128MX16 — Bottom under U3

DDR_1V5

MT41K128M16JT

Note 1

R89 240 — GND

R599 240 — GND

DDR_VREF

C653 0.22UF 16V — GND

C47 0.22UF 16V — GND

C717 0.22UF 16V — GND

C618 0.22UF 16V — GND

R635 10.0K 1% — GND

R602 10.0K — GND

SH21 DDR_SDCLK0 — DRAM_SDCLK0

SH20 DDR_SDCLK0_B — DRAM_SDCLK0_B

0

Clock access points

SH18 DDR_SDCLK1 — DRAM_SDCLK1

SH19 DDR_SDCLK1_B — DRAM_SDCLK1_B

0 GND probe pad

TP15

0

C621 0.1UF 16V — GND

R107 240 1%

R18

R119 240 — GND

C72 0.22UF 16V — GND

C56 0.22UF 16V — GND

U2 — 2G_DDR3_SDRAM_128MX16 — Top left

DDR_1V5

MT41K128M16JT

U4 — 2G_DDR3_SDRAM_128MX16 — Bottom under U2

DDR_1V5

MT41K128M16JT

R99 240 — GND

C734 0.22UF 16V — GND

1 GByte DDR3

T-point routing
Components allow pin to pin route length matching

C647 C613 C614 C666 C76 C48 0.22UF 16V (6.3V) — GND

C619 C728 C617 C616 C615 C620 0.22UF 6.3V / 16V — GND

C736 C735 C733 C732 C731 C718 0.22UF 16V — GND

C75 C64 C737 C57 C58 C59 C67 0.22UF 16V — GND

C70 C71 C73 C74 C79 C78 C49 0.22UF 16V / 22UF 6.3V — GND

C37 C53 C44 C46 C36 C35 0.22UF 16V / 22UF 6.3V — GND

C727 C45 C42 C41 C52 C43 C77 0.22UF 6.3V / 16V / 22UF 6.3V — GND

NOTE 1:

Using bit swapping for DATA bus to allow easy pcb routing.

When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

NOTE 2:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

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ICAP Classification:	FCP: ___	FIUO: ___	PUBI: X

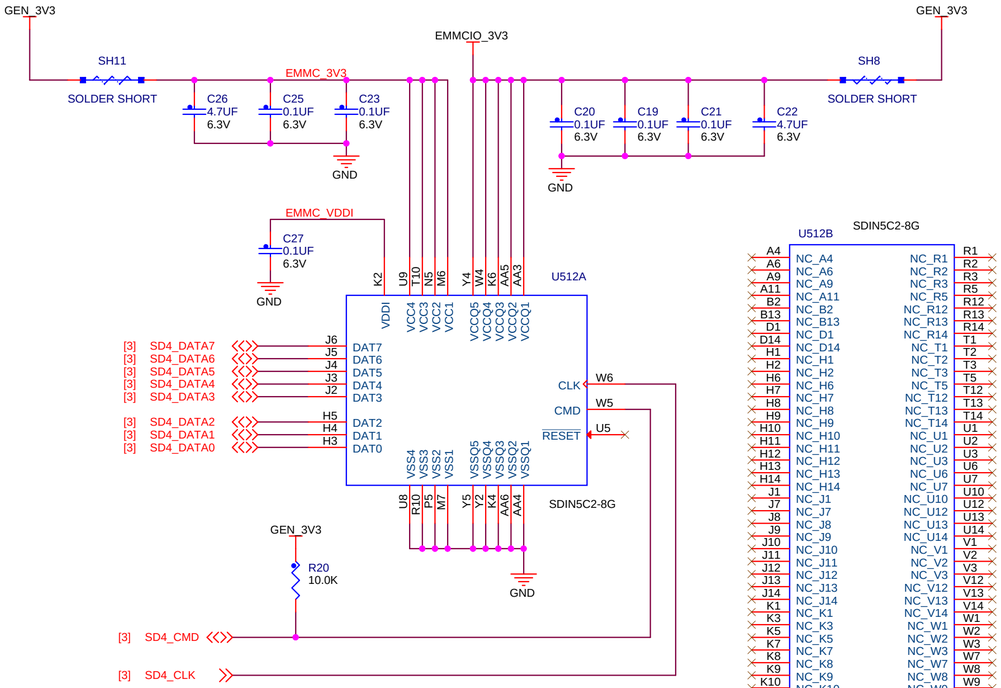
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **DDR3 MEMORY**

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

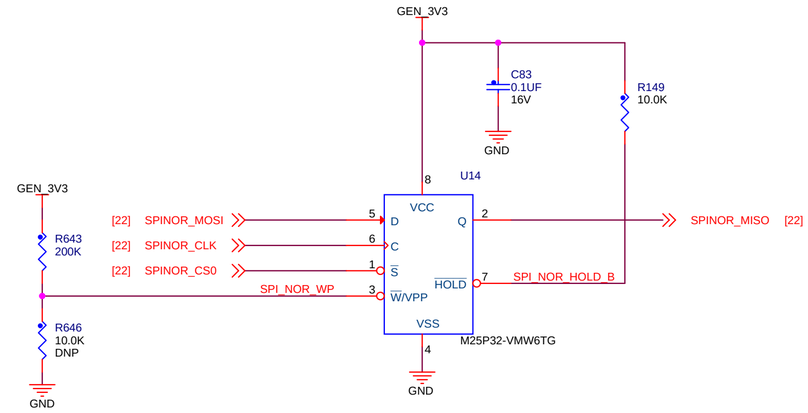
Date: Saturday, October 18, 2014 — Sheet 4 of 25

8GB eMMC MEMORY



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

4MB SPI NOR FLASH



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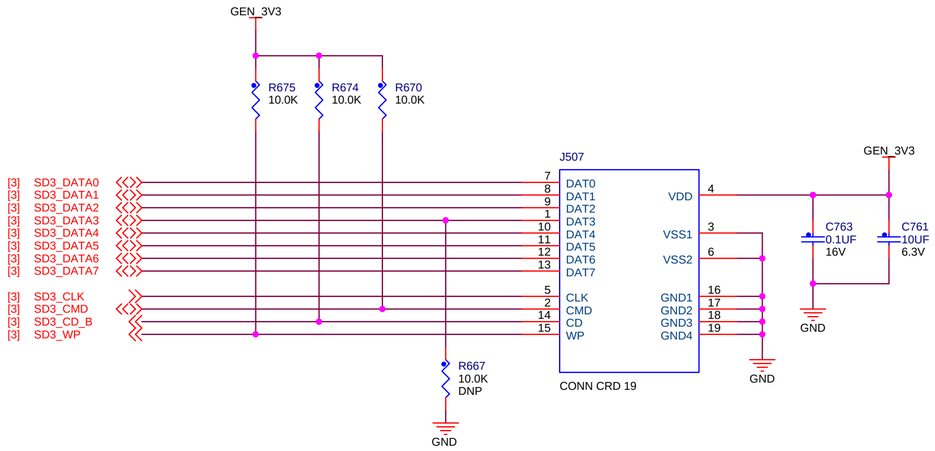
ICAP Classification:	FCP:___ FIUO:___ PUBI: X	
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM	
Page Title:	eMMC, SPI NOR FLASH	
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417	Rev C3
Date: Saturday, October 18, 2014	Sheet 5 of 25	

SD CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

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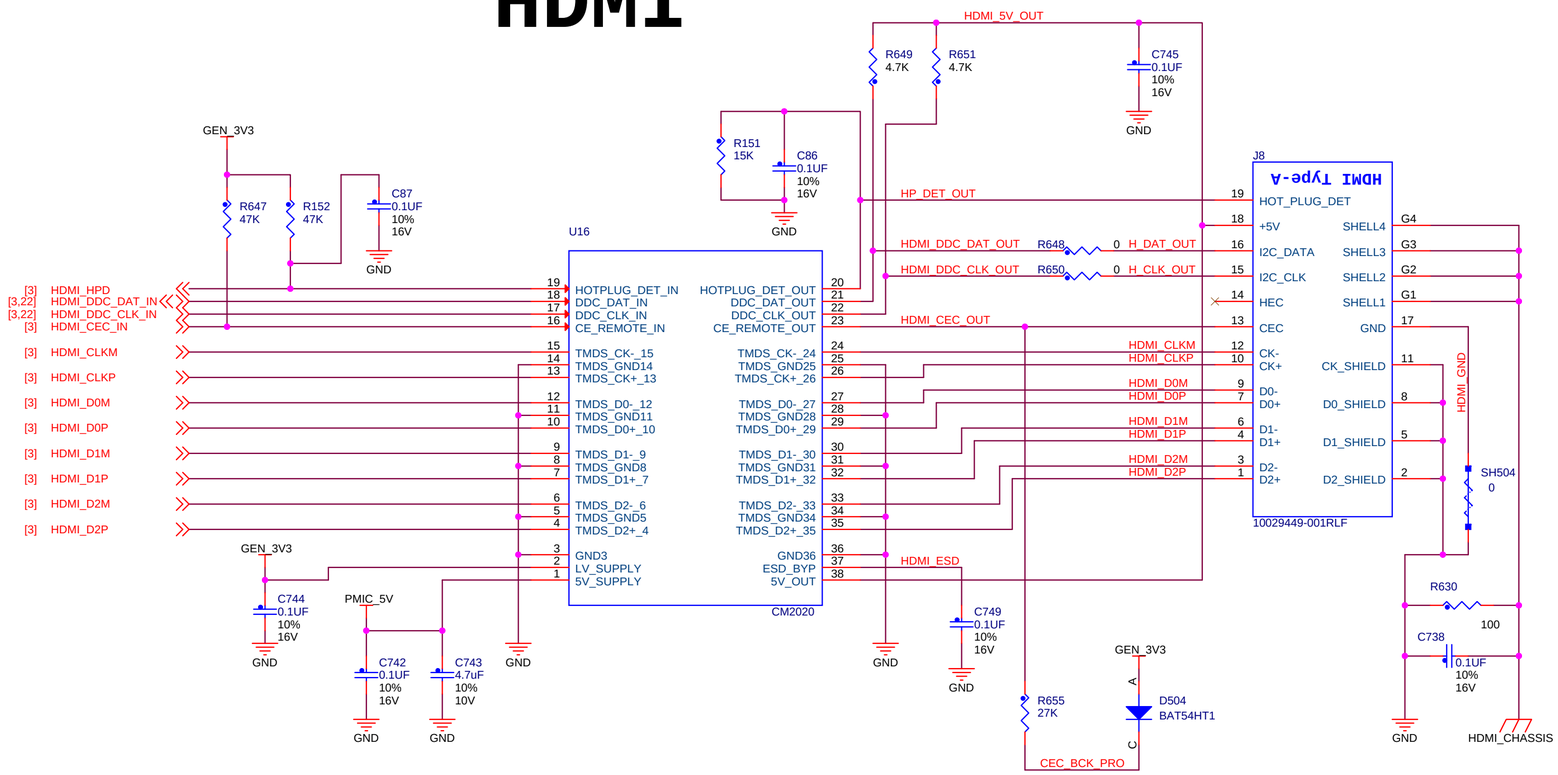
ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

Page Title:
SD CARD, SATA

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3
Date: Saturday, October 18, 2014	Sheet 6 of 25	

HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz
to read EDID values due to HDMI standards.
I2C2 bus speed should be limited to 100 kHz whenever
Hot Plug Detect is high.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

Page Title:
HDMI

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 7 of 25

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:

MCIMX6DL-SMART DEVICE PLATFORM

Page Title:

CAMERA, EXP PORT

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 8 of 25

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ICAP Classification: FCP:___ FIUO:___ PUBI:X

Drawing Title:

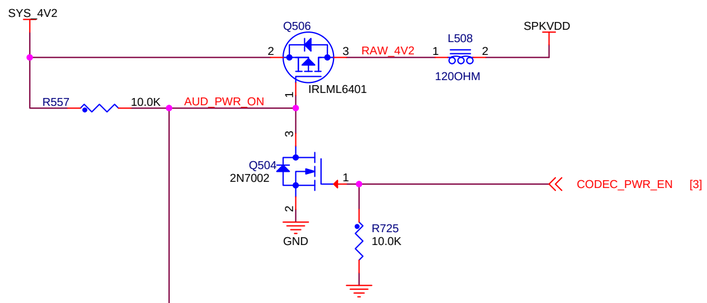
MCIMX6DL-SMART DEVICE PLATFORM

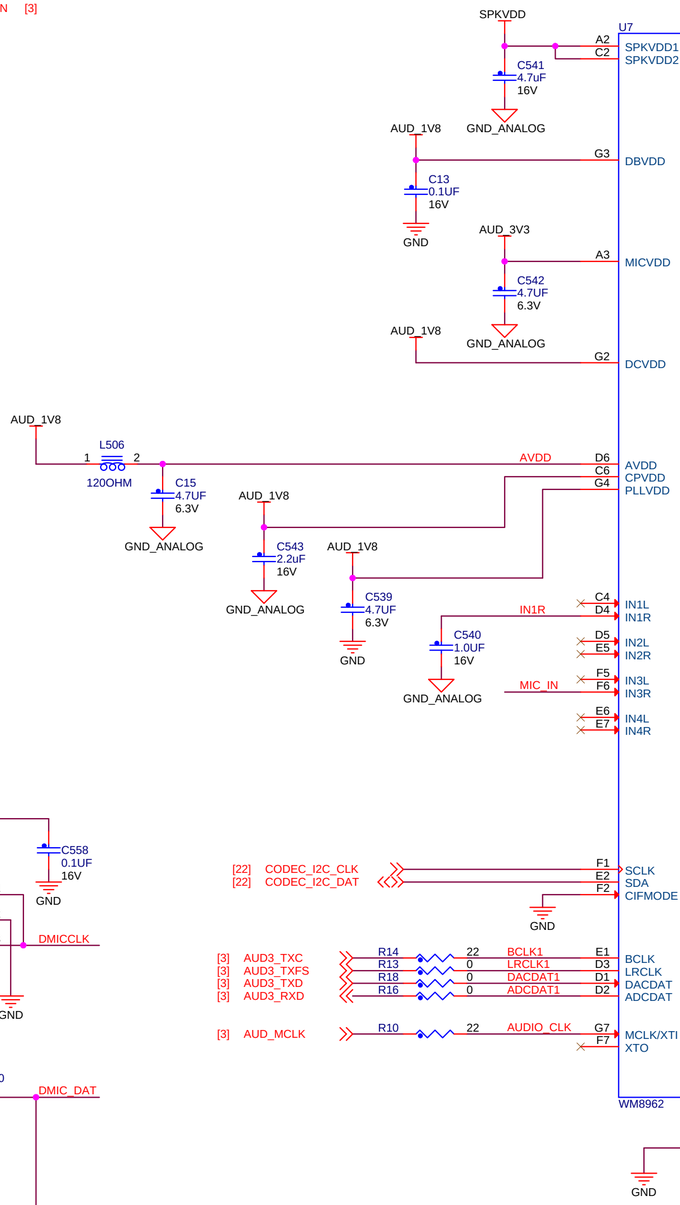
Page Title:

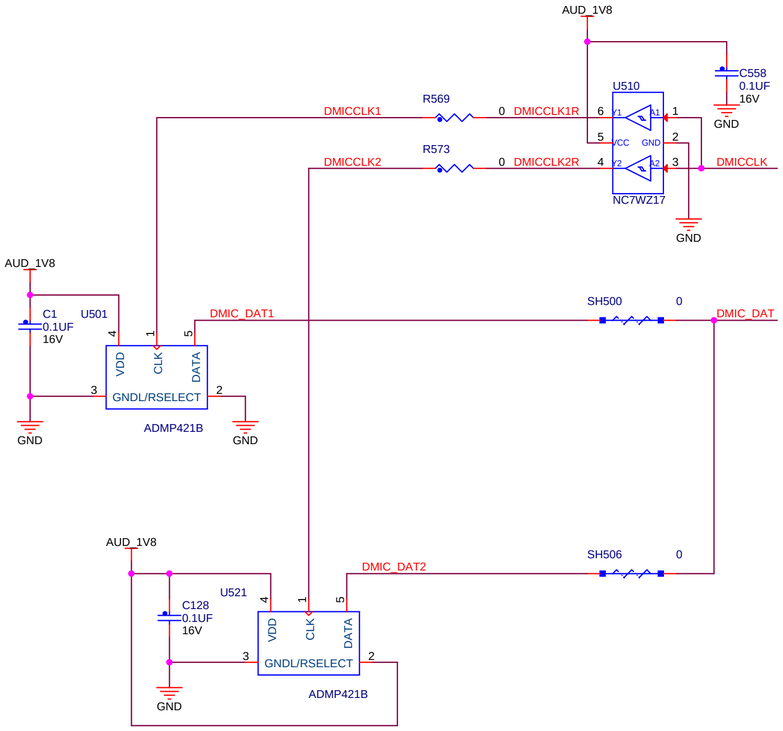
EPDC EXP PORTS

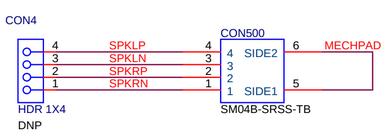
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 9 of 25









NOTE:
On Rev B4 boards, buffers U500 and U520 are removed, and a wire is added by hand connecting pins 2 and 4 together. On Rev C boards, the layout will be modified to remove the hand rework.

NOTE:
MECHPAD trace is for mechanical hold down tabs only. There is no shield ground on this plastic connector.

place as close as possible to AGND ball

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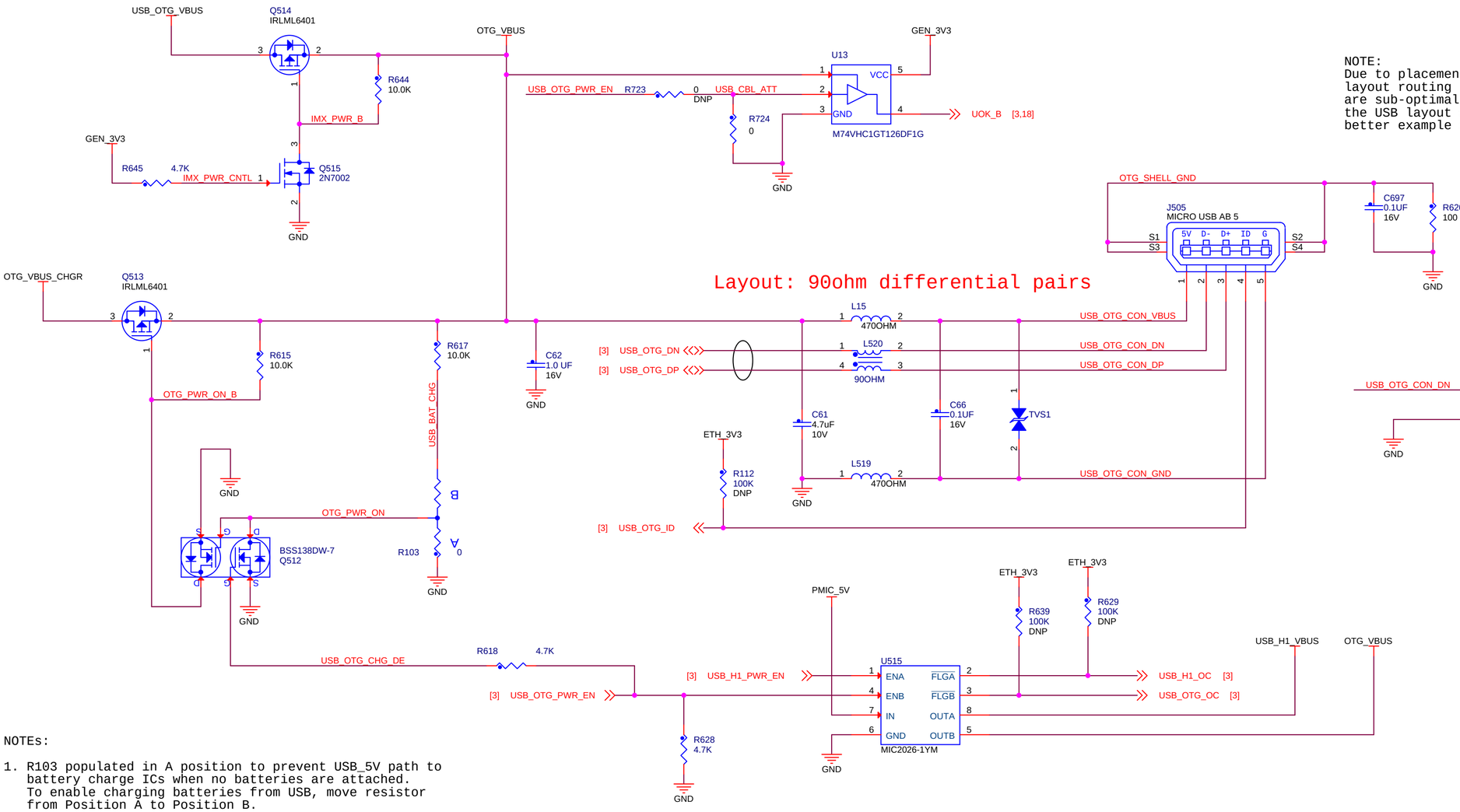
ICAP Classification:	FCP:___	FIUO:___	PUBI: X

Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **AUDIO**

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3
Date: Saturday, October 18, 2014	Sheet 10 of 25	



Layout: 90ohm differential pairs

NOTE:
Due to placement requirements on the SABRE SD board set, layout routing for the USB_OTG_DP and USB_OTG_DN traces are sub-optimal. It is recommended that customers consider using the USB layout on the Freescale i.MX6 SABRE AI board as a better example of proper USB trace routing.

Cut Trace on Rev B1 Boards

NOTEs:

1. R103 populated in A position to prevent USB_5V path to battery charge ICs when no batteries are attached. To enable charging batteries from USB, move resistor from Position A to Position B.

TRUTH TABLE
OTG_VBUS INPUT TO BATTERY CHARGERS

USB_OTG _PWR_EN	OTG_PWR _ON	OTG_PWR _ON_B	OTG_VBUS _CHGR
LOW	HIGH	LOW	POWERED
HIGH	LOW	HIGH	NOT POWERED

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: USB

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 11 of 25

To Processor I/O supply

Alternate power source for processor I/O

NOTE:
Solder short normally connects NVCC_RGMII to ETH_VDDIO.
To connect NVCC_RGMII to VGEN1_1V5, cut the trace between pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.

Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.

Layout: 100 ohm differential pairs

EMI Filter Reserved
470pF are for LED

NOTE:
Place R626 close to Ethernet PHY.

Place LED D11 near LED for pins 11 - 12 of RJ-45 connector. Orange LED indicates 1000 speed.

Power-on Strapping Pins

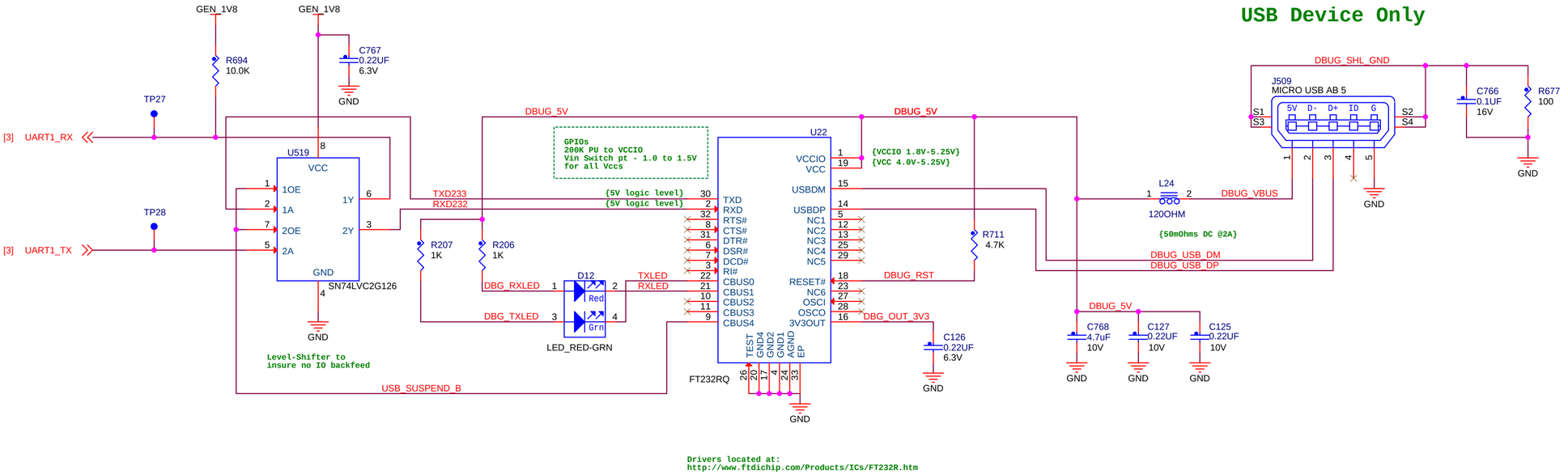
MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

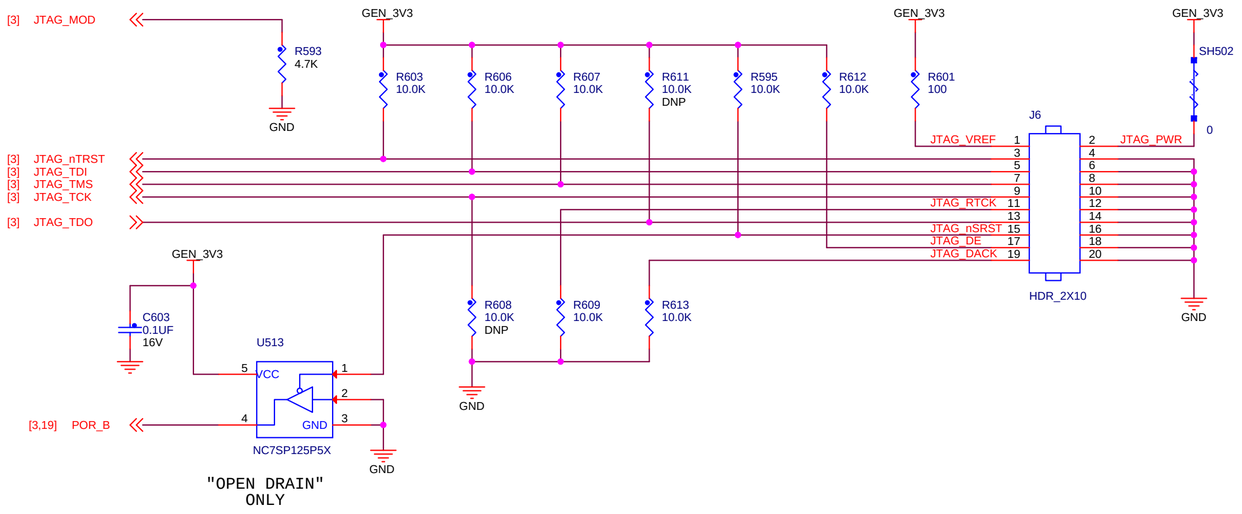
ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X	
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM	
Page Title:	ETHERNET	
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417	Rev C3
Date: Saturday, October 18, 2014	Sheet 12 of 25	

DEBUG UART TO USB CONVERSION

Library Revision - A



JTAG



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Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417		Rev: C3
Date: Saturday, October 18, 2014		Sheet 13 of 25	

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:

MCIMX6DL-SMART DEVICE PLATFORM

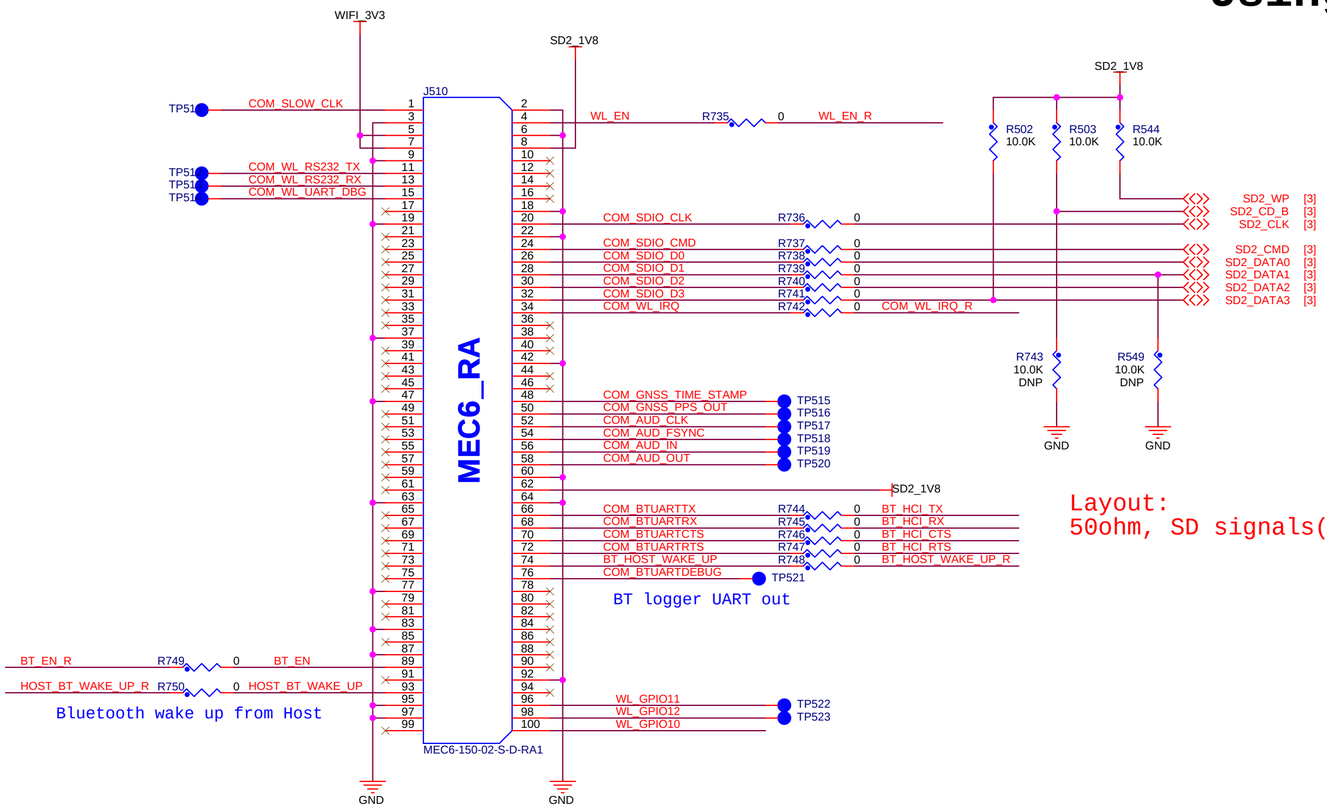
Page Title:

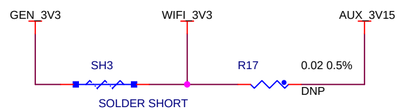
SENSORS

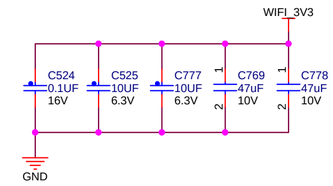
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

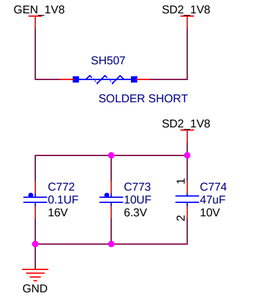
Date: Saturday, October 18, 2014 Sheet 14 of 25

WIFI + BLUETOOTH CONNECTOR
Using module WL1835MODCOM8B

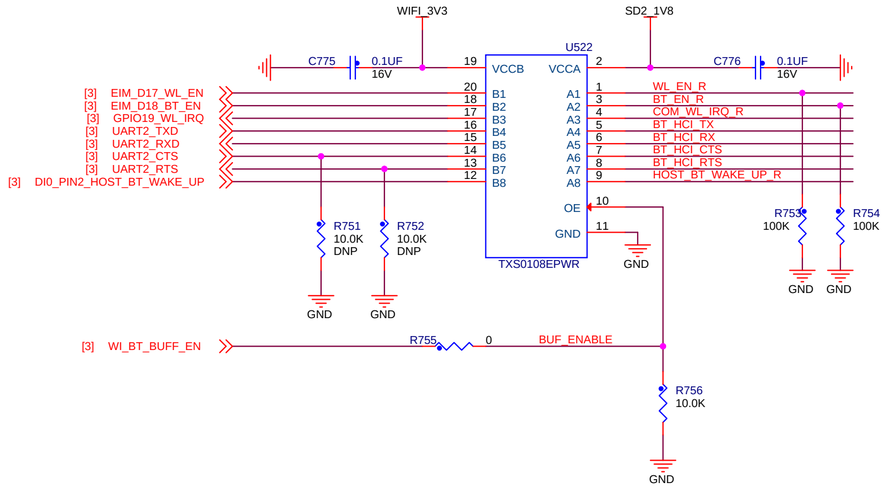


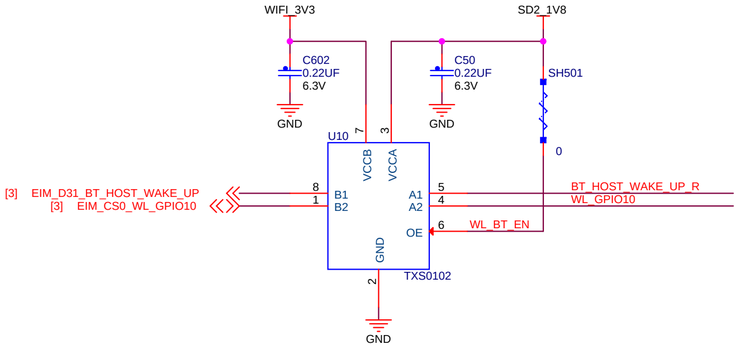






BUFFER_1





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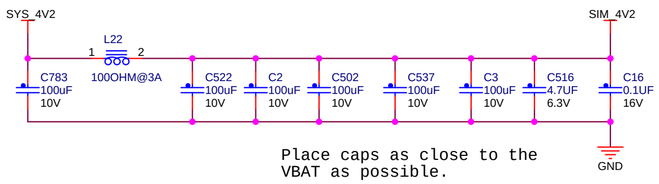
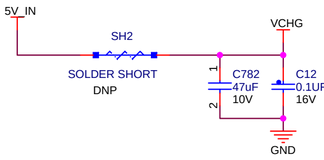
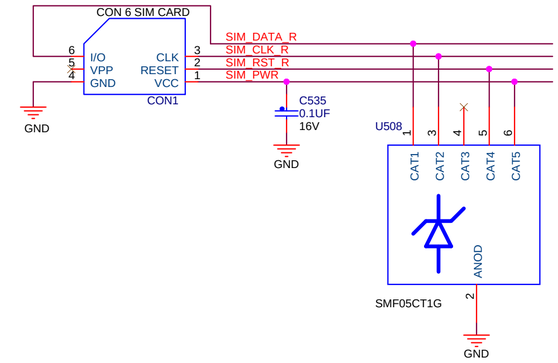
Page Title: AUX SDIO CONN, CAN		
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417	Rev C3
Date: Saturday, October 18, 2014	Sheet 15 of 25	

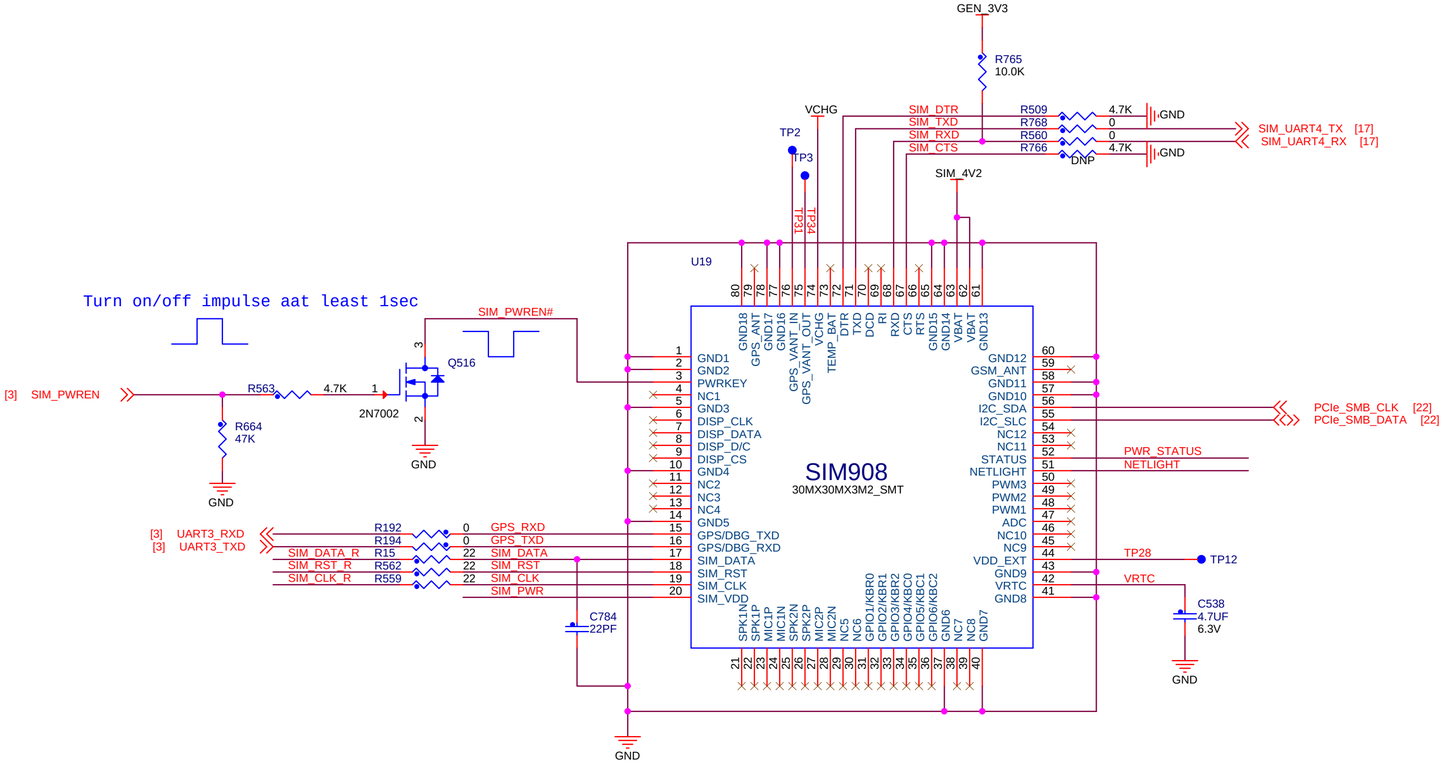
GSM, GPS

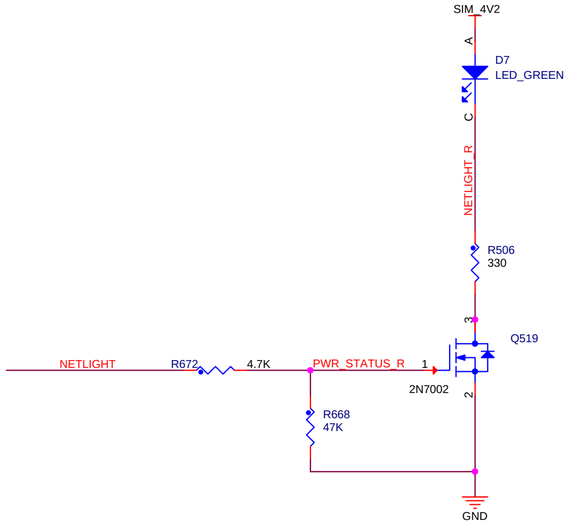


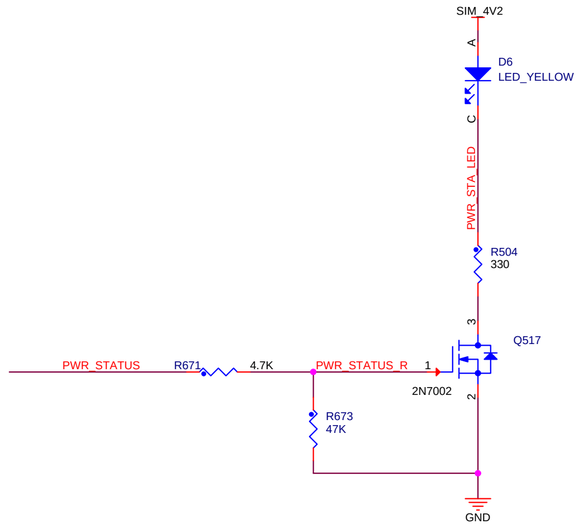
Place caps as close to the VBAT as possible.











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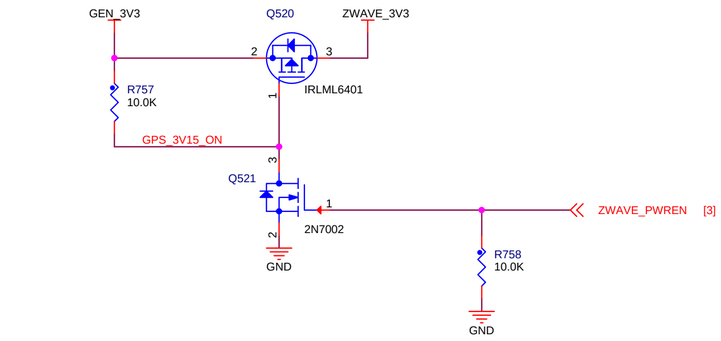
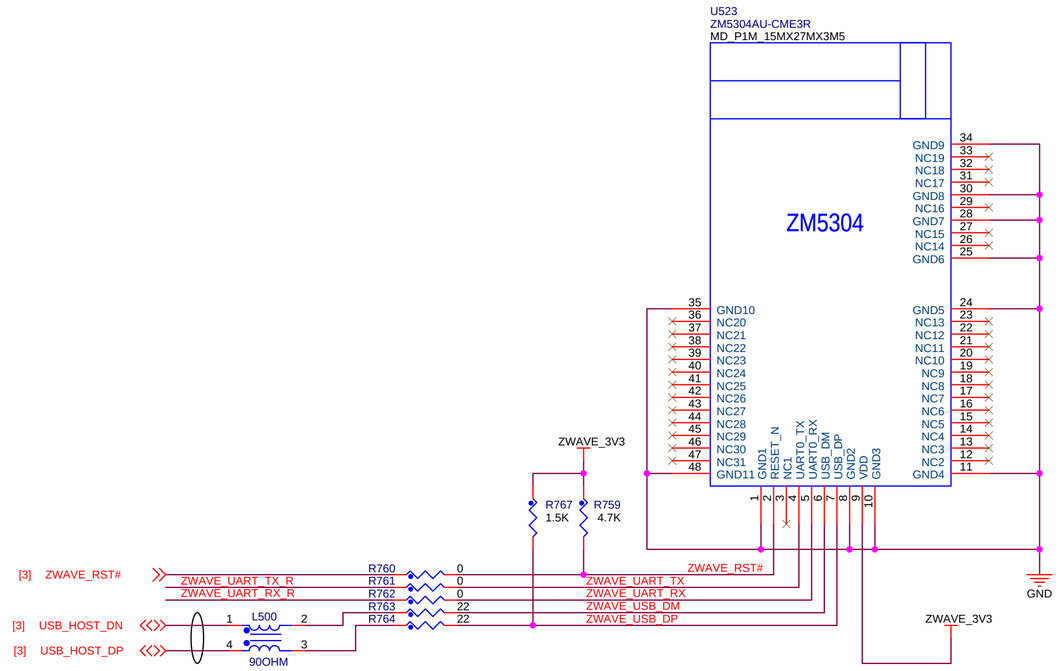
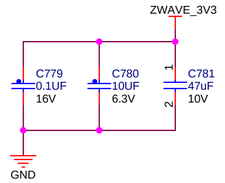
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM			
Page Title: GSM,GPS MODULE			
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417		Rev C3
Date: Saturday, October 18, 2014		Sheet 16 of 25	







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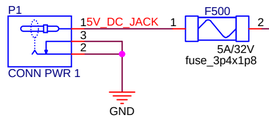
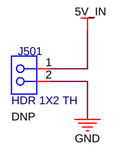
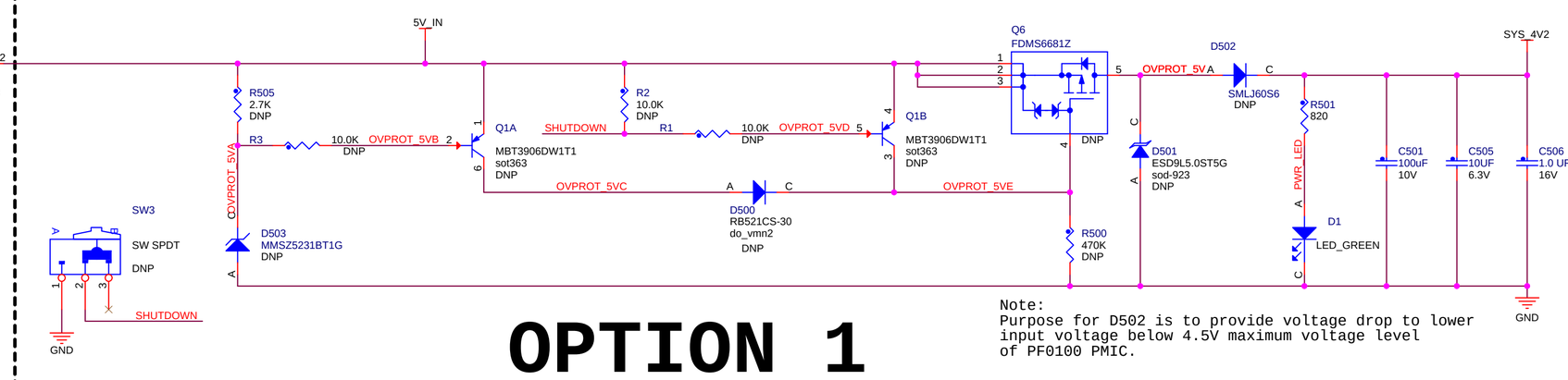
Page Title: Z-WAVE MODULE			
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417		Rev C3
Date: Saturday, October 18, 2014	Sheet 17 of 25		

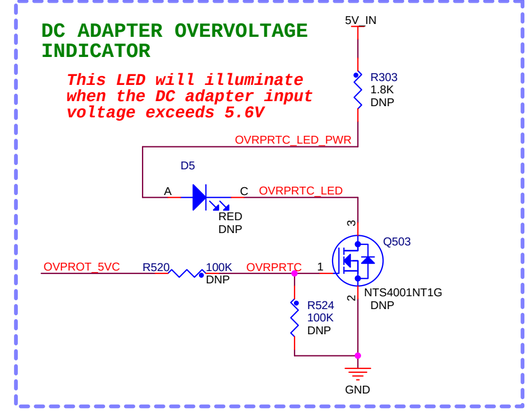
OVER VOLTAGE PROTECTION

External Power 5 Vdc





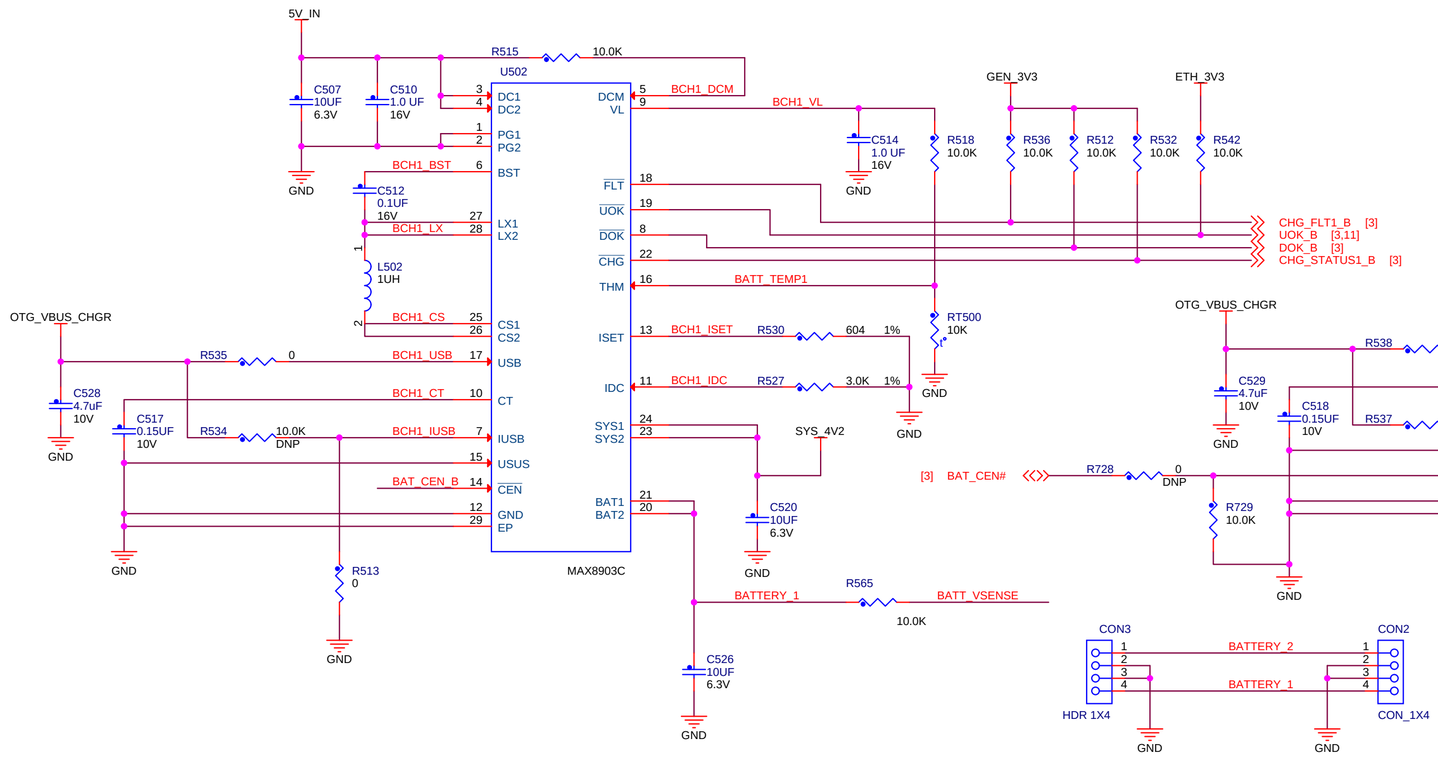


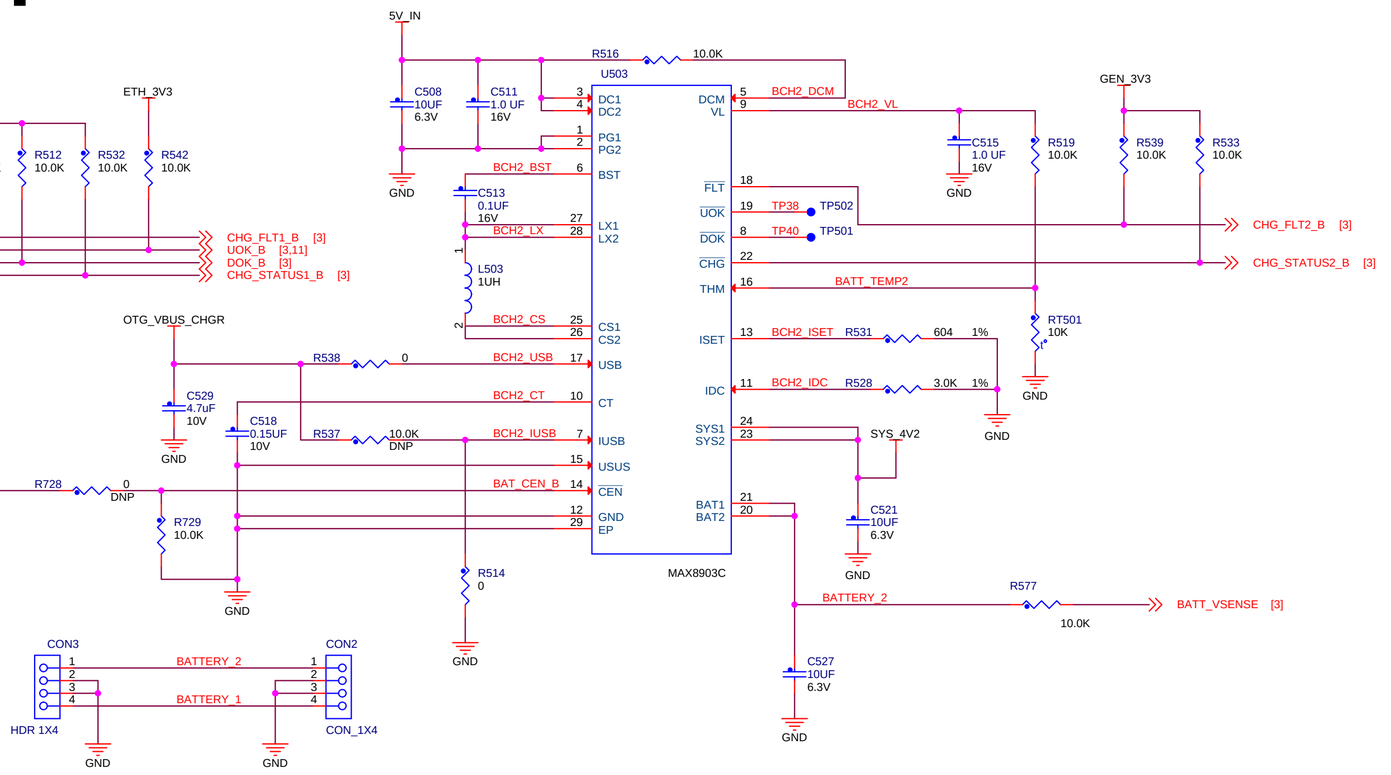


Note:
Purpose for D502 is to provide voltage drop to lower input voltage below 4.5V maximum voltage level of PF0100 PMIC.

OPTION 1

BATTERY 1 CHARGE CIRCUIT





OPTION 2

NOTE:
Battery posts are meant for two, single cell 3.7 Li-ION batteries to be added in parallel.

Note: Populate either
Option #1 for the Smart Device Board, or
Option #2 for the Smart Device Platform

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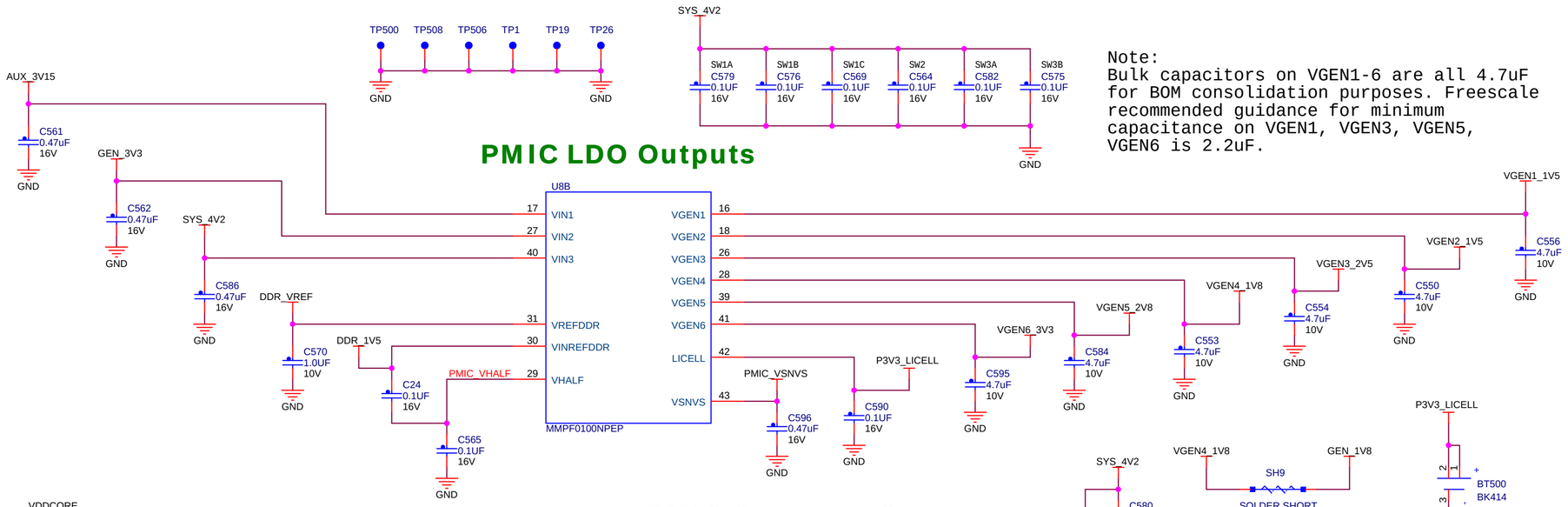
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **BATTERY CHARGER**

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

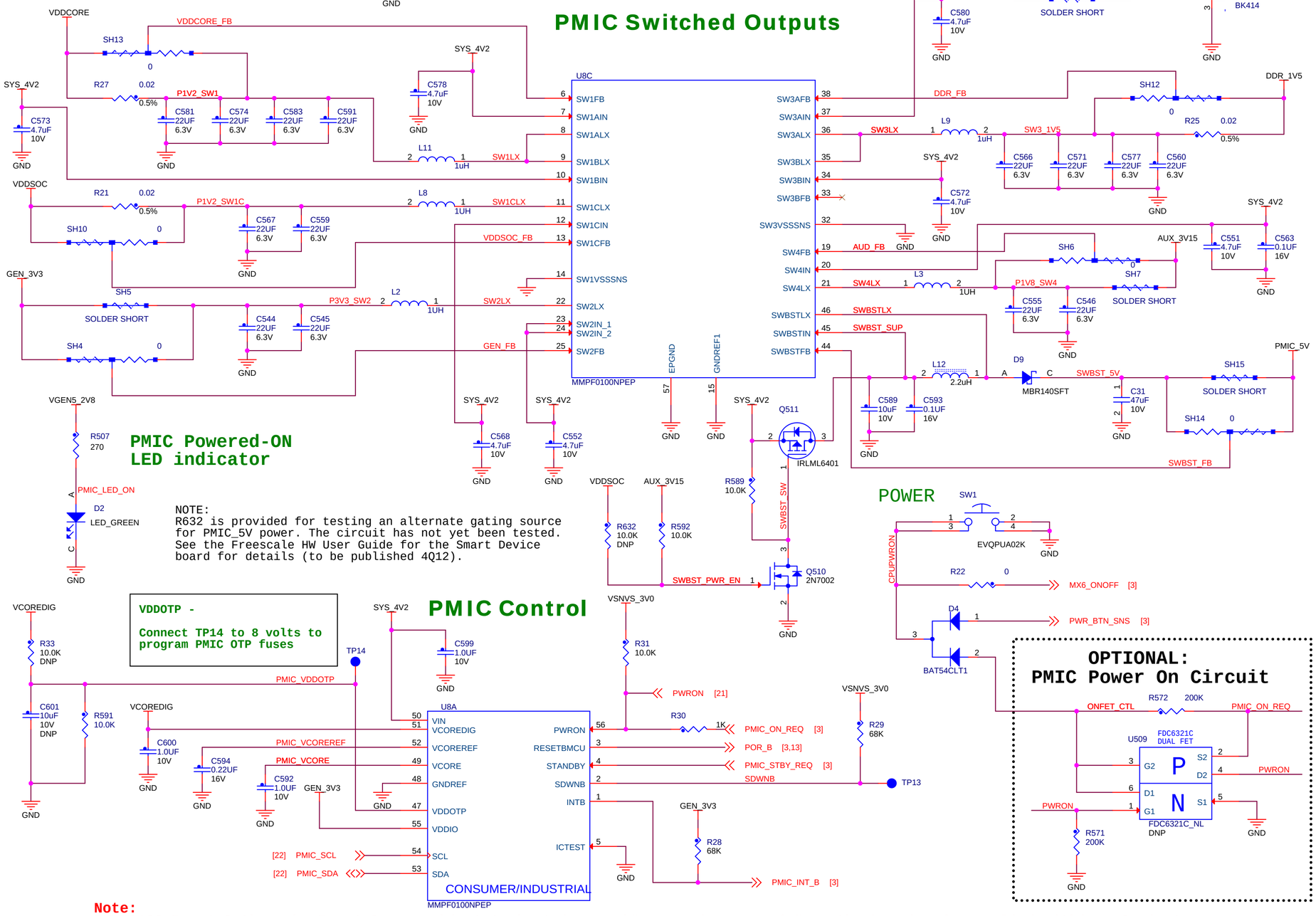
Date: Saturday, October 18, 2014 Sheet 18 of 25

PMIC LDO Outputs



Note:
Bulk capacitors on VGEN1-6 are all 4.7uF for BOM consolidation purposes. Freescale recommended guidance for minimum capacitance on VGEN1, VGEN3, VGEN5, VGEN6 is 2.2uF.

PMIC Switched Outputs



PMIC Powered-ON LED indicator

NOTE:
R632 is provided for testing an alternate gating source for PMIC_5V power. The circuit has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

PMIC Control

VDDOTP -

Connect TP14 to 8 volts to program PMIC OTP fuses

POWER

OPTIONAL: PMIC Power On Circuit

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Note:
PMPF0100 Pass1.0 through Pass1.2 are subject to boot issues if power is removed from the board and reapplied within ~ 2 minutes.
PMPF0100 Pass2.0 will correct this issue. For more details, see the PMPF0100 ERRATA, Issue #ER19

Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A	1.375	1	2155	1001	
SW1B					
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A	1.5	3	1500	760	
SW3B					
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:				4454	

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
		HDMI			
	AUX_5V	SATA	MAX8815	1000	
		LVDS0			
		CAN			
3.3	GEN_3V3	EMMC	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
		SENSORS			
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
		TOUCH			
		GPS			
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
		ACC			
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS	PF0100 VGEN1	100	
		mPCIe			
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

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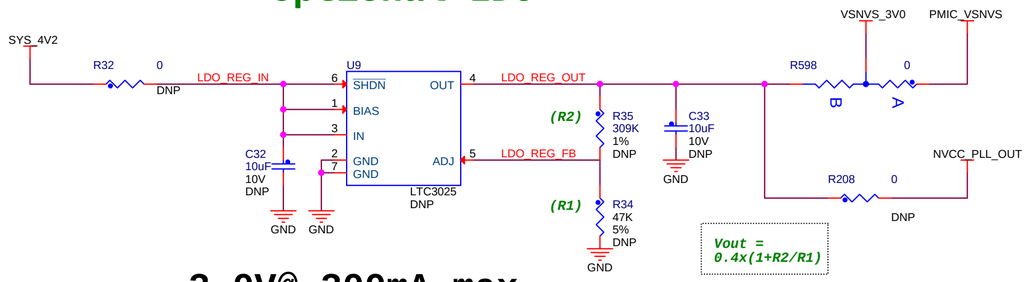
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **PF0100 PMIC**

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 19 of 25

Optional LDO



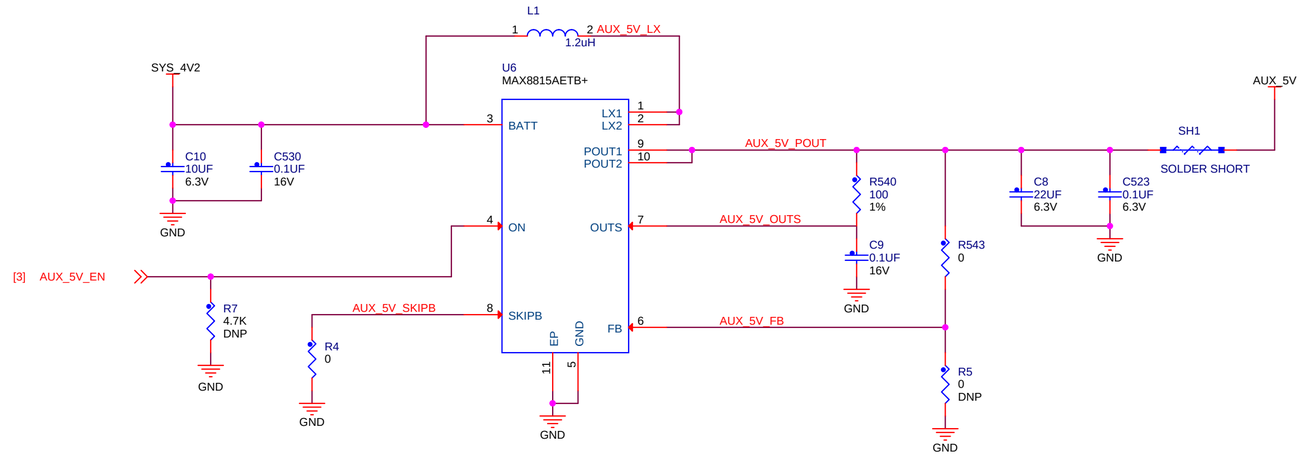
3.0V@ 300mA max

NOTE FOR VDDHIGH_IN LOADING ON VGEN5:
VDDHIGH was placed on VGEN5 early in the design as a compromise solution for a board designed primarily for software development. Validation of the i.MX6 processor has shown that operations at elevated temperatures may cause VDDHIGH_IN to require much more current than VGEN5 can supply. It is recommended for robust designs potentially operating at more extreme temperatures for VDDHIGH to be supplied from a power rail that can supply 250 mA or more.
This allows for datasheet maximum of 125 mA for internal VDDHIGH_IN loads plus 125 mA for external PHY IO loads.

The optional LDO U9 shown on this page could be reconfigured to supply both VDDHIGH_IN and VDD_SNVS_IN loads to meet the additional current requirments

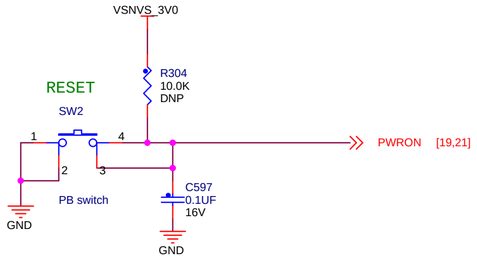
U9 is no longer required for PF0100 VSNVS issue, but may be desired for NVCC_PLL_VOUT.
It is being left in a depopulated condition. If the LDO is needed, R34 and R35 should be populated as follows:
For VSNVS (3.0V): R34 = 47K, R35 = 309K
For NVCC_PLL_OUT (1.1V): R34 = 47K, R35 = 82.5K

5.0V@1A DC2DC

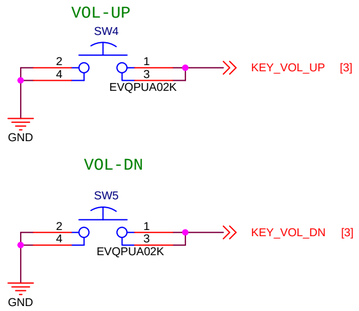


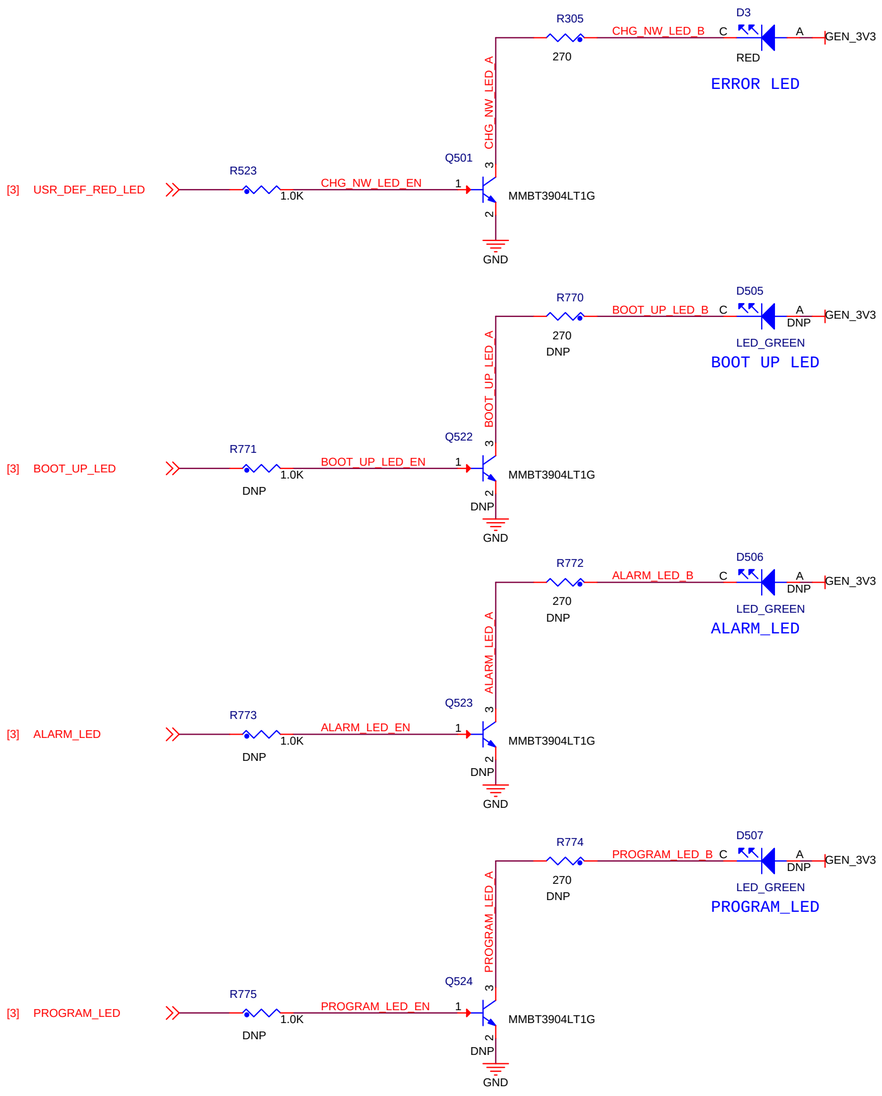
ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X	
Drawing Title:	**MCIMX6DL-SMART DEVICE PLATFORM**	
Page Title:	**AUX VOLT REG**	
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417	Rev C3
Date: Saturday, October 18, 2014	Sheet 20 of 25	

U/I KEY

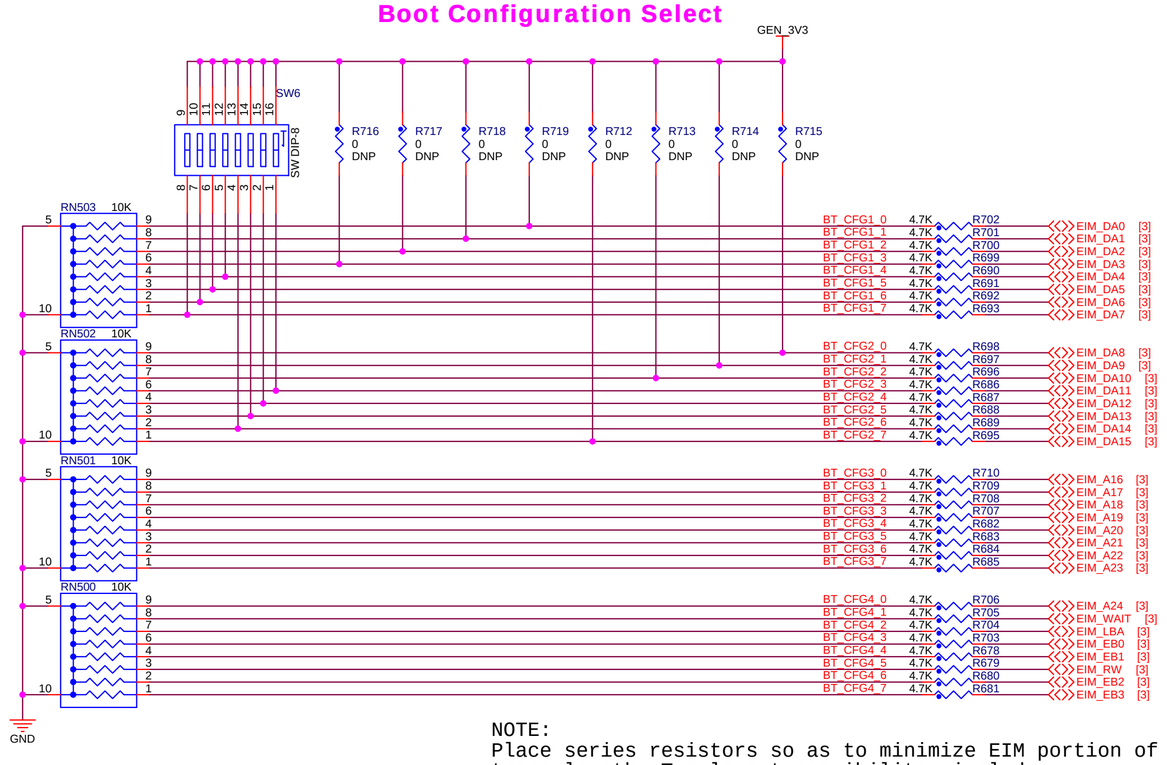


NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.





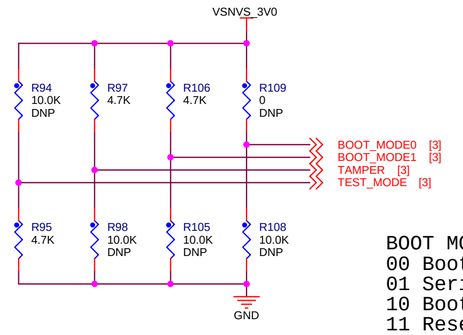
Boot Configuration Select



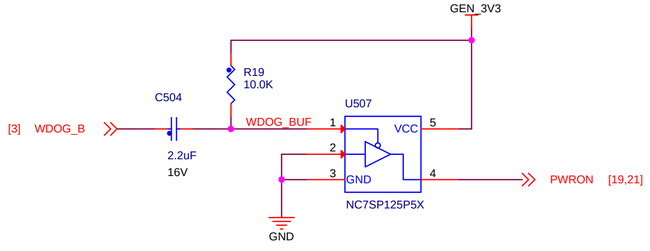
NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0



BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved



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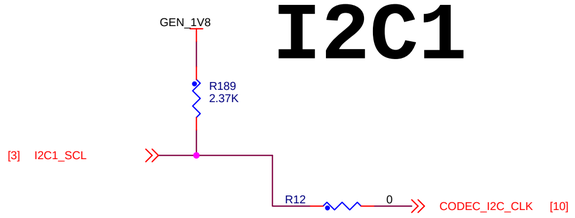
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **BOOT SELECT**

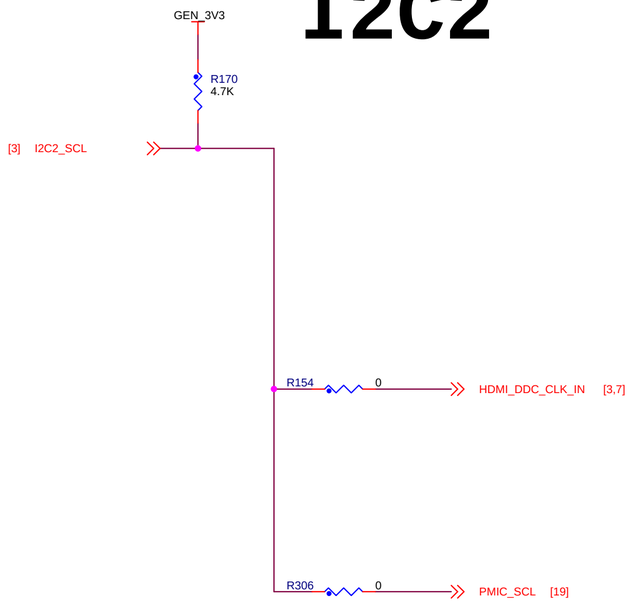
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 21 of 25

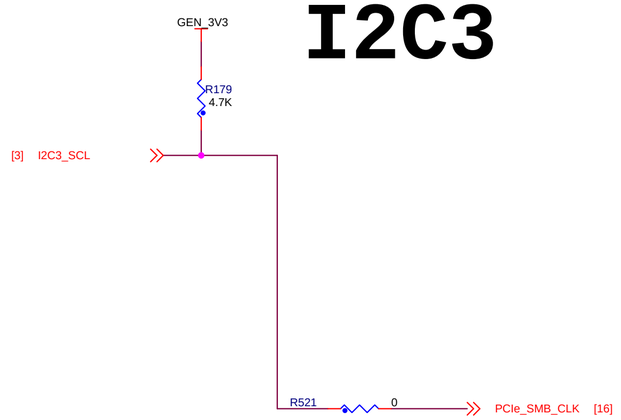
I2C1

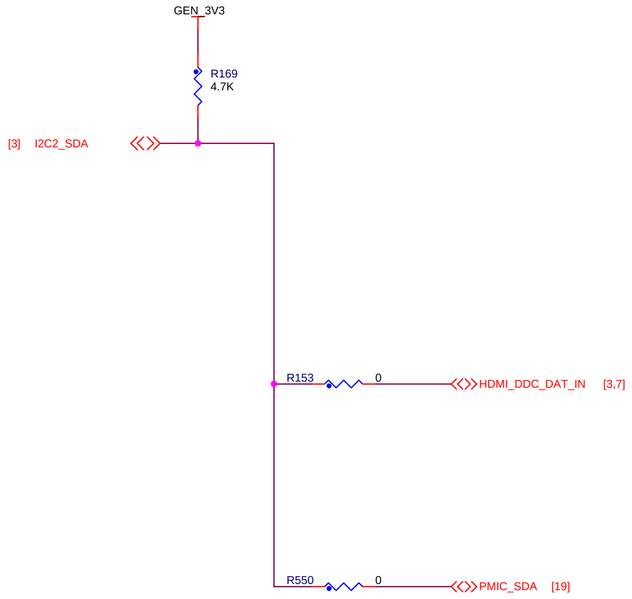


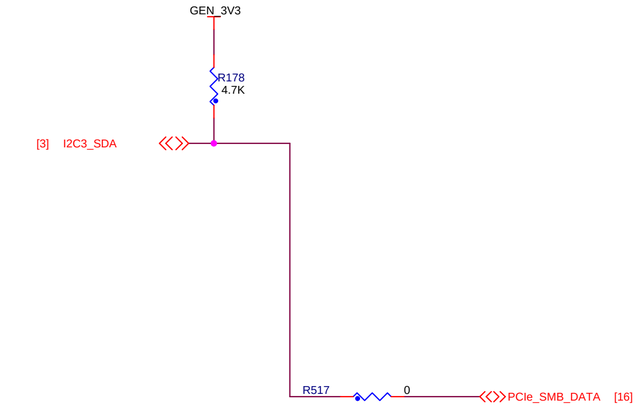
I2C2



I2C3

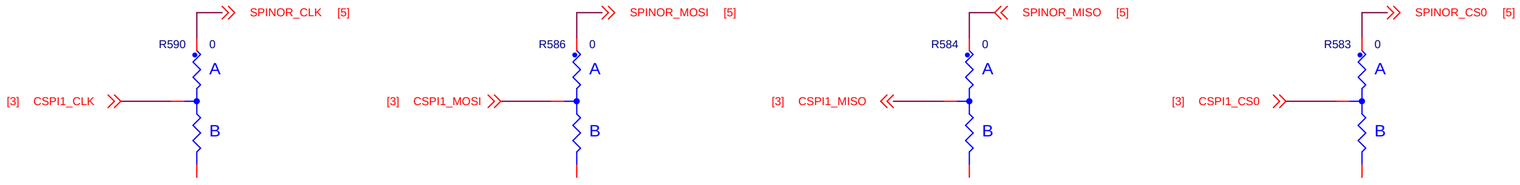






NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.

CSPI1



NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

Page Title:
COMM CHANNEL STEERING

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 22 of 25

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:

MCIMX6DL-SMART DEVICE PLATFORM

Page Title:

BUILD OPTON TABLES

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 23 of 25

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:

MCIMX6DL-SMART DEVICE PLATFORM

Page Title:

PIN MUX TABLE

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 24 of 25

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:

MCIMX6DL-SMART DEVICE PLATFORM

Page Title:

TEMPORARY DEVIATIONS

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C3

Date: Saturday, October 18, 2014 Sheet 25 of 25