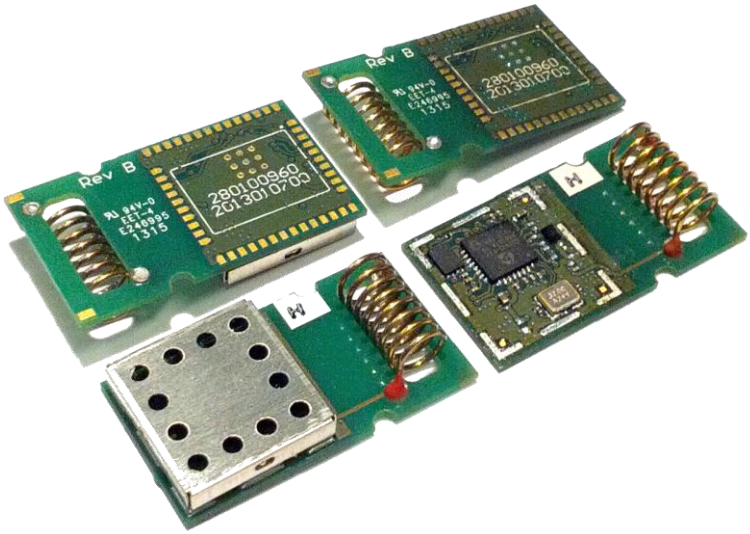
DATASHEET: ZM5304

FULLY INTEGRATED Z-WAVE® WIRELESS MODEM WITH ON-BOARD ANTENNA



The Sigma Designs ZM5304 Modem is a fully integrated Z-Wave modem module in a small 27mm x 15.2mm x 5.5mm form factor. It is an ideal solution for home control applications such as access control, appliance control, AV control, building automation, energy management, lighting, security, and sensor networks in the "Internet of Things".

A baseband controller, sub-1 GHz radio transceiver, crystal, decoupling, SAW filter, matching, and the antenna is included to provide a complete Z-Wave solution to an application executing in an external host microcontroller. The ZM5304 Modem is certified with the FCC modular transmitter approval, ready to be used in any product without additional testing and license costs.

The ZM5304 Modem is based on an 8-bit 8051 CPU core, which is optimized to handle the data and link management requirements of a Z-Wave node. The UART0 or USB interface can be used to access the Z-Wave stack available in the on-chip Flash memory, or to easily upgrade the modem firmware.

FCC ID	D87-ZM5304-U

Features

- Complete Z-Wave stack available over UART or USB
- Firmware upgradeable via UART or USB
- 32kB of byte addressable NVM memory
- Fully Integrated crystal, EEPROM, SAW filter, matching circuit, and antenna
- No external components required
- FCC modular transmitter approval
- ITU G.9959 compliant

Modem

- UART speed up to 230.4kbps
- USB 2.0 full speed
- Z-Wave serial API accessed over UART or USB
- ADC for internal battery monitoring
- Hardware AES-128 security engine
- Power-On-Reset / Brown-out Detector
- Supply voltage range from 2.3V to 3.6V for optional battery operation
- TX mode current typ. 36mA @ 0dBm
- RX mode current typ. 33mA
- Normal mode current typ. 15mA
- Sleep mode current typ. 2µA
- Less than 1ms cold start-up time

Radio Transceiver

- Receiver sensitivity with SAW filter down to -103dBm @ 9.6kbps
- Transmit power with SAW filter up to +4dBm
- Z-Wave 9.6/40/100kbps data rates
- Supports all Z-Wave sub-1 GHz frequency bands (865.2MHz to 926.3MHz)
- Supports multi-channel frequency agility and listen before talk
- Regulatory Compliance
  ACMA: AS/NZS 4268
  CE: EN 300 220/489
  FCC: CFR 47 Part 15
  IC: RSS-GEN/210
  MIC: ARIB STD-T108

1 CONTENT

2 OVERVIEW

The ZM5304 Modem is a fully integrated module with an on-board antenna that allows the establishment of a Z-Wave network with minimum risk. The SD3503 modem chip is used with an external NVM (EEPROM), 32MHz crystal, power supply decoupling, SAW filter, matching circuit, and a helical antenna. Figure 2.1 shows the main blocks of the ZM5304 Modem, while Figure 2.2 illustrates the firmware stack of an example application.

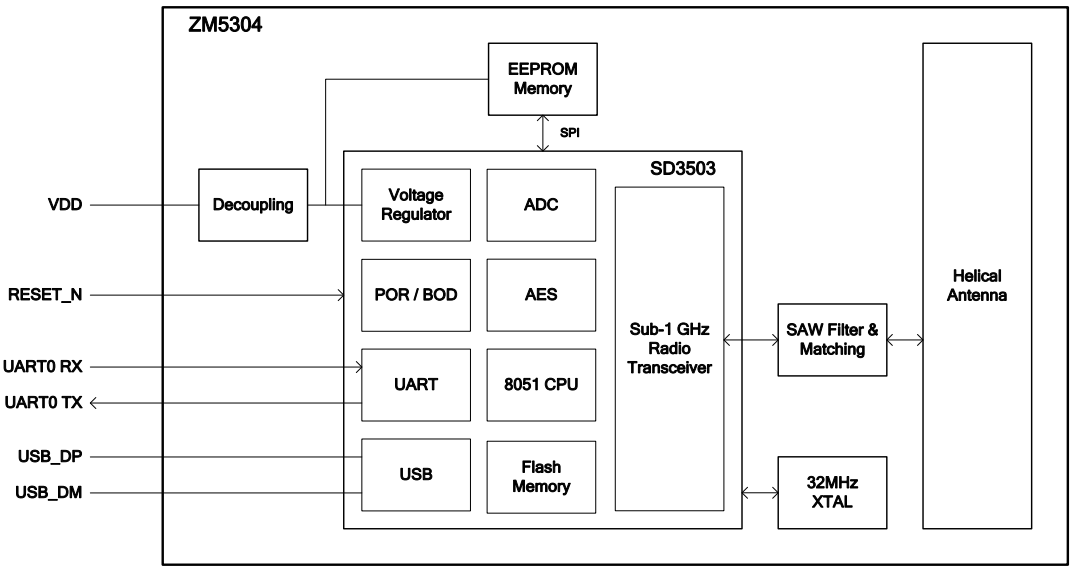


Figure 2.1: Functional block diagram

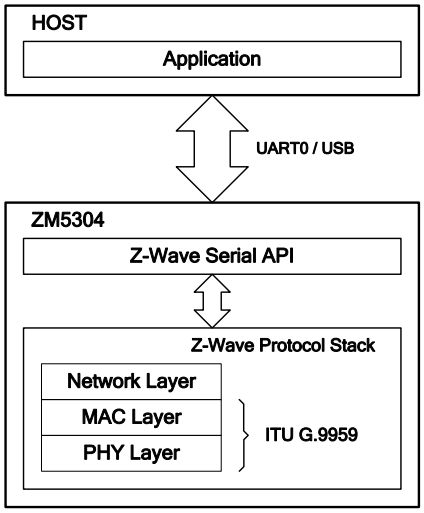


Figure 2.2: Firmware stack

2.1 PERIPHERALS

2.1.1 ADVANCED ENCRYPTION STANDARD SECURITY PROCESSOR

The Z-Wave protocol specifies the use of Advanced Encryption Standard (AES) 128-bit block encryption for secure applications. The built-in Security Processor is a hardware accelerator that encrypts and decrypts data at a rate of 1 byte per 1.5µs. It encodes

the frame payload and the message authentication code to ensure privacy and authenticity of messages. The processor supports Output FeedBack (OFB), Cipher-Block Chaining (CBC), and Electronic CodeBook (ECB) modes to target variable length messages. Payload data is streamed in OFB mode, and authentication data is processed in CBC mode as required by the Z-Wave protocol. The processor implements two efficient access methods: Direct Memory Access (DMA) and streaming through Special Function Register (SFR) ports. The processor functionality is exposed via the Z-Wave API for application use.

2.1.2 ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) is capable of sampling an input voltage source and returns an 8- or 12-bit unsigned representation of the input scaled relative to the selected reference voltage. It can be configured to implement a battery monitor, as described by the formula below.

$$ADC_{OUT} = \frac{V_{BG}}{V_{DD}} \times 2^{Number\ of\ bits}$$

The ADC is capable of operating rail to rail, where the built-in Band-gap V_{BG} = 1.25V and V_{DD} is the supply voltage. When the supply voltage crosses a predefined lower or upper voltage threshold, an interrupt can be triggered.

2.1.3 BROWN-OUT DETECTOR / POWER-ON-RESET

When a cold start-up occurs, an internal Power-On-Reset (POR) circuit ensures that code execution does not begin unless the supply voltage is sufficient. After which, an internal Brown-Out Detector (BOD) circuit guarantees that faulty code execution does not occur by entering the reset state, if the supply voltage drops below the minimum operating level. These guarantees apply equally in both the active and sleep modes.

2.1.4 CRYSTAL DRIVER AND SYSTEM CLOCK

The system clock and RF frequencies are derived from an external 32MHz crystal (XTAL) which is factory trimmed to guarantee initial frequency precision.

2.1.5 UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER

The Universal Asynchronous Receiver / Transmitter (UART) is a hardware block operating independently of the 8051 CPU. It offers full-duplex data exchange, up to 230.4kbps, with an external host microcontroller requiring an industry standard NRZ asynchronous serial data format. The UART0 interface is available over pin 4 and pin 5 (refer section 4). A data byte is shifted as a start bit, 8 data bits (lsb first), and a stop bit, respectively, with no parity and hardware handshaking. Figure 2.3 shows the waveform of a single serial byte. UART0 is compliant with RS-232 when an external level converter is used.

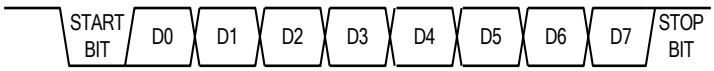


Figure 2.3: UART0 waveform

2.1.6 UNIVERSAL SERIAL BUS

A Universal Serial Bus (USB) 2.0 full speed interface is available over pin 6 and pin 7 (refer section 4). The Communication Device Class / Abstract Control Mode (CDC/ACM) provides an emulated virtual COM port to a host. This makes it easy to migrate from legacy RS-232 communication to USB communication. Figure 2.4 shows the two termination resistors necessary to maintain signal integrity of the differential pair and a single pull-up resistor on USB_DP, which indicates a full speed device to the host.

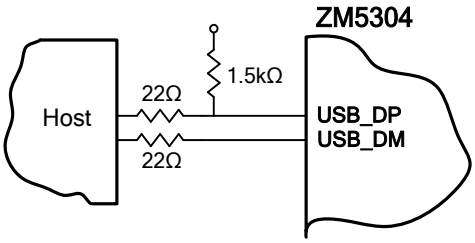


Figure 2.4: USB interface

The controller supports USB suspend mode and remote wake-up. During suspend mode, except for the crystal oscillator clocking at a slower rate and the active USB controller, the entire CPU is powered off. The USB controller uses the DMA for fast data transfer and automatic data retransmissions/CRC to maintain data integrity.

2.1.7 WATCHDOG

The watchdog helps prevents the CPU from entering a deadlock state. A timer that is enabled by default achieves this by triggering a reset event in case it overflows. The timer overflows in 1 second, therefore it is essential that the software clear the timer periodically. The watchdog is disabled when the chip is in power down mode, and automatically restarts with a cleared timer when waking up to the active mode.

2.1.8 WIRELESS TRANSCEIVER

The wireless transceiver is a sub-1 GHz ISM narrowband FSK radio, a modem, and a baseband controller. This architecture provides an all-digital direct synthesis transmitter and a low IF digital receiver. The Z-Wave protocol currently utilizes 2-key FSK/GFSK modulation schemes at 9.6/40/100 kbps data rates throughout a span of carrier frequencies from 865.2MHz to 926.3MHz.

The output power of the transmitter is configurable in the range -26dBm to +4dBm (V_{DD} = +2.3V to +3.6V, T_A = -10°C to +85°C).

2.2 MEMORY MAP

An application executing on an external host microcontroller can access the higher address space of the integrated EEPROM via the serial API. As shown in Figure 2.5, the protocol data is stored in the lower address space. A serial API function returns the size of the application data space. [1][2]

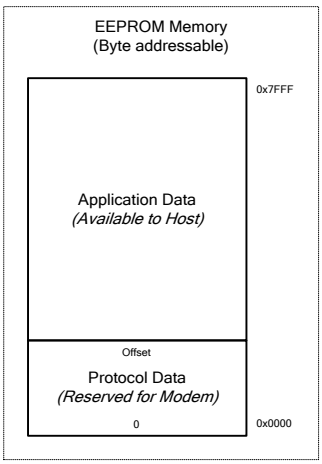


Figure 2.5: EEPROM memory map

2.3 MODULE PROGRAMMING

The firmware of the ZM5304 Modem can be upgraded either via UART0 or USB interface. [3] In-System Programming is the default mode delivered from the factory.

2.3.1 ENTERING IN-SYSTEM PROGRAMMING MODE

The module can be placed into the UART0 In-System Programming (ISP) mode by asserting the active low RESET_N signal for 5.2ms. The programming unit of the module then waits for the “Interface Enable” serial command before activating the ISP mode over UART0.

2.3.2 ENTERING AUTO PROGRAMMING MODE

Alternatively, the module can be placed into the Auto Programming Mode (APM) by calling a serial API function. The programming unit of the module will enter APM immediately after a hardware or software reset. Once the module is in APM, the firmware can be written to the internal flash using either the UART0 or USB interface.

2.4 POWER SUPPLY REGULATOR

While the supply to the digital I/O circuits is unregulated, on-chip low-dropout regulators derive all the 1.5 V and 2.5 V internal supplies required by the Micro-Controller Unit (MCU) core logic, non-volatile data registers, flash, and the analogue circuitry.

3 TYPICAL APPLICATION

An illustration of two application examples using the ZM5304 Modem implementation follows. The host application located on an external microcontroller accesses the Z-Wave stack via the serial API. Figure 3.1 depicts the scenario when UART0 is used as the primary interface to the ZM5304 Modem, while Figure 3.2 shows the scenario when the USB[1] is used. In the latter scenario, UART0 must be routed out to test points in order to program the initial firmware during production. It is strongly recommended that the power supply is decoupled sufficiently.

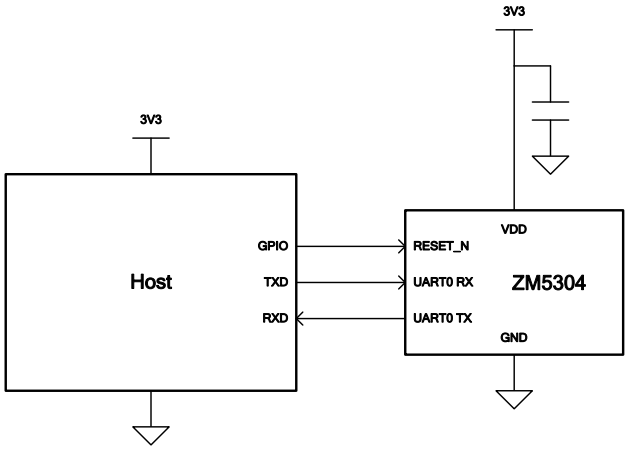


Figure 3.1: Example of a host microcontroller based application using UART0

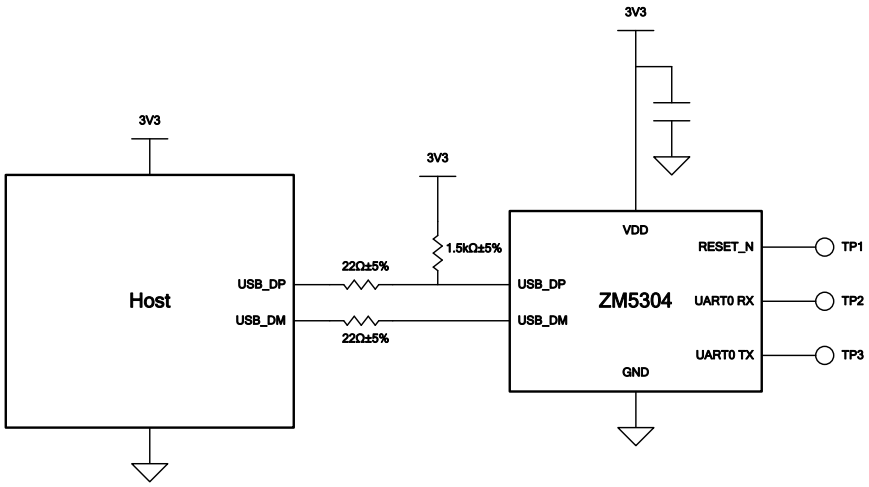


Figure 3.2: Example of a host microcontroller based application using the USB

[1] Firmware upgrades can be performed only when the ZM5304 Modem is placed in APM.

4 PIN CONFIGURATION

The layout of the pins on the ZM5304 Modem is shown in Figure 4.1.

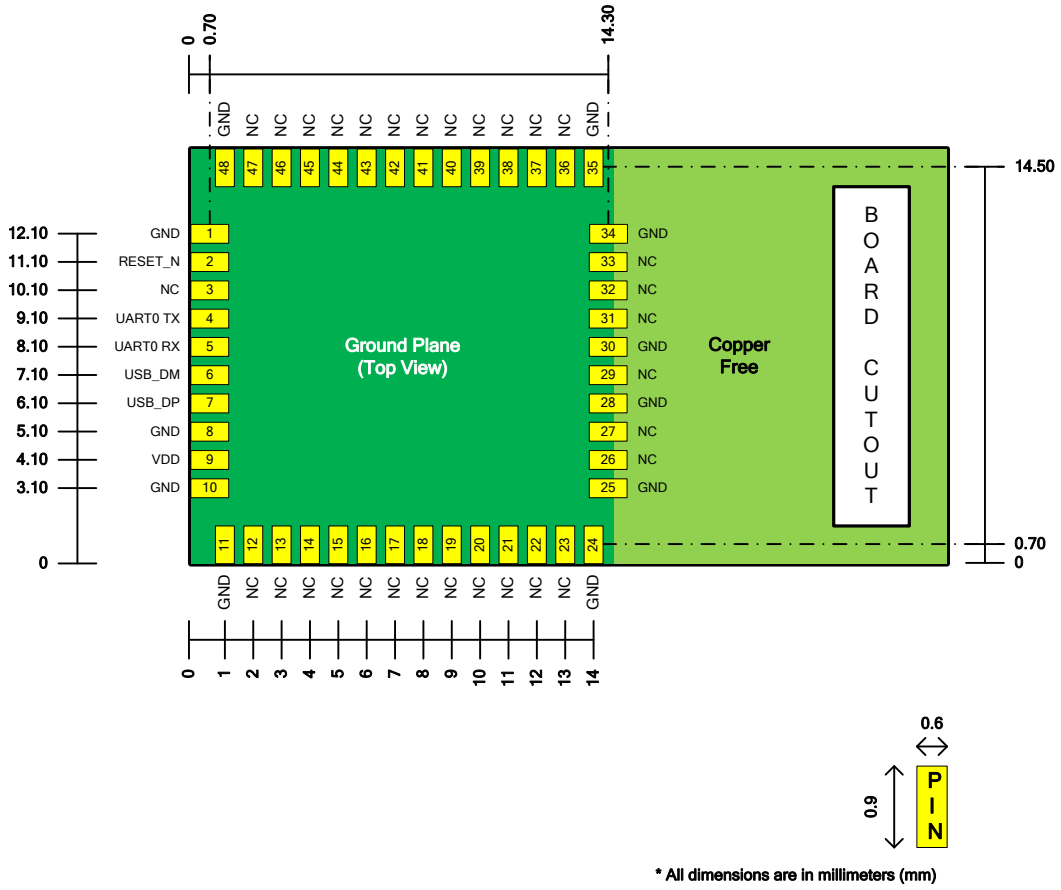


Figure 4.1: Pin layout (top view)

4.1 PIN FUNCTIONALITY

Table 4.1: Power, ground, and no connect signals

Pin Name	Pin Location	Type[2]	Function
V_{DD}	9	S	Module power supply.
GND	1, 8, 10, 11, 24, 25, 28, 30, 34, 35, 48	S	Ground. Must be connected to the ground plane.
NC	3, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 26, 27, 29, 31, 32, 33, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47	-	Placement pins for mechanical stability. Leave unconnected.

[2] I = Input, O = Output, D+ = Differential Plus, D- = Differential Minus, S = Supply

Table 4.2: Module control signals

Pin Name	Pin Location	Type	Function
RESET_N	2	I	Active low signal that places the module in a reset state.

Table 4.3: UART0 interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
UART0 RX	5	I	Waits for the "Interface Enable" serial command after 5.2ms. Enters UART0 ISP mode after command is received from the host.	Receive data from host serial port.
UART0 TX	4	O	Serial data transmit when in UART0 ISP mode, high impedance with internal pull-up otherwise.	Transmit data to host serial port.

Table 4.4: USB interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
USB_DP	7	D+	ISP when in APM mode, high impedance with internal pull-up otherwise.	USB 2.0 full-speed positive differential signal.
USB_DM	6	D-	ISP when in APM mode, high impedance with internal pull-up otherwise.	USB 2.0 full-speed negative differential signal.

5 ELECTRICAL CHARACTERISTICS

This section describes the electrical parameters of the ZM5304 Modem module.

5.1 TEST CONDITIONS

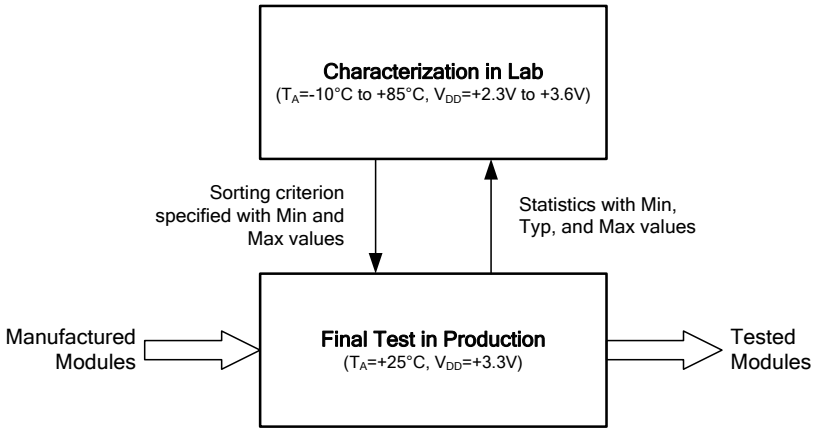


Figure 5.1: Testing flow

The following conditions apply for characterization in the lab, unless otherwise noted.

1. Ambient temperature T_A = -10°C to +85°C
2. Supply voltage V_{DD} = +2.3V to +3.6V
3. All tests are carried out on the ZDB5304 Z-Wave Development Board. [4]
4. Total radiated power is measured for 868.4, 908.4, and 921.4MHz

The following conditions apply for the final test in production, unless otherwise noted.

1. Ambient temperature T_A = +25°C
2. Supply voltage V_{DD} = +3.3V
3. Near-field radiated transmission power is measured for 868.4, 908.4, and 921.4MHz
4. Near-field radiated receiver sensitivity is measured for 868.4, 908.4, and 921.4MHz

5.1.1 TYPICAL VALUES

Unless otherwise specified, typical data refer to the mean of a data set measured at an ambient temperature of T_A=25°C and supply voltage of V_{DD}=+3.3V.

5.1.2 MINIMUM AND MAXIMUM VALUES

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by a final test in production on 100% of the devices at an ambient temperature of T_A=25°C and supply voltage of V_{DD}=+3.3V.

For data based on measurements, the minimum and maximum values represent the mean value plus or minus three times the standard deviation (μ±3σ).

5.2 ABSOLUTE MAXIMUM RATINGS

The absolute ratings specify the limits beyond which the module may not be functional. Exposure to absolute maximum conditions for extended periods may cause permanent damage to the module.

Table 5.1: Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}	Main supply voltage	-0.3	+3.6	V
V_{IN}	Voltage applied on any I/O pin	-0.3	+3.6	V
I_{IN}	Current limit when over driving the input ($V_{IN} > V_{DD}$)	-	+20.0	mA
ESD_{HBM}	JEDEC JESD22-A114F Human Body Model	-	+2000.0	V
ESD_{MM}	JEDEC JESD22-A115C Machine Model	-	+200.0	V
ESD_{CDM}	JEDEC JESD22-C101E Field-Induced Charged-Device Model	-	+500.0	V

Table 5.2: Current characteristics

Symbol	Description	Min	Max	Unit
I_{VDD}	Current into VDD power supply pin	-	+120	mA
I_{GND}	Sum of the current out of all GND ground pins	-120	-	mA

Table 5.3: Thermal characteristics

Symbol	Description	Min	Max	Unit
T_J	Junction temperature	-55	+125	°C

5.3 GENERAL OPERATING RATINGS

The operating ratings indicate the conditions where the module is guaranteed to be functional.

Table 5.4: Recommended operating conditions

Symbol	Description	Min	Typ	Max	Unit
V_{DD}	Standard operating supply voltage	+2.3	+3.3	+3.6	V
V_{DD_USB}	Standard operating supply voltage when USB PHY is used	+3.0	+3.3	+3.6	V
f_{SYS}	Internal clock frequency	-	32.0	-	MHz
T_A	Ambient operating temperature	-10.0	+25.0	+85.0	°C

5.4 CURRENT CONSUMPTION

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.5: Current consumption in active modes

Symbol	Description	Min	Typ	Max	Unit
I_{DD_ACTIVE}	MCU running at 32MHz	-	14.8	15.8	mA
I_{DD_RX}	MCU and radio receiver active	-	32.7	35.0	mA
$I_{DD\_TX\_01}$	MCU and radio transmitter active, RFPOW=01	-	27.7	TBD	mA
$I_{DD\_TX\_63}$	MCU and radio transmitter active, RFPOW=63	-	42.7	TBD	mA

Table 5.6: Current consumption in power saving modes

Symbol	Description	Min	Typ	Max	Unit
I_{DD_SLEEP}	Module in sleep state	-	1.7	3.7	µA
I_{USB_SLEEP}	USB suspend mode with state persistency, and system clock	-	2.0	2.3	mA

Table 5.7: Current consumption during programming

Symbol	Description	Min	Typ	Max	Unit
$I_{DD\_PGM\_UART0}$	Programming via UART0	-	15	-	mA
$I_{DD\_PGM\_USB}$	Programming via USB	-	15	-	mA

5.5 SYSTEM TIMING

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.8: Transition between operating modes

Symbol	Description	Min	Typ	Max	Unit
t_{ACTIVE_SLEEP}	Transition time from the active state to the sleep state	-	-	125	ns
t_{SLEEP_ACTIVE}	Transition time from the sleep state to the active state ready to execute code	-	-	160	µs

Table 5.9: System start-up time

Symbol	Description	Min	Typ	Max	Unit
V_{POR}	Power-on-Reset (POR) threshold on rising supply voltage at which the reset signal is deasserted	-	-	+2.3	V
t_{RESET_ACTIVE}	Transition time from the reset state to the active state ready to execute code with a power rise time not exceeding 10µs	-	-	1.0	ms

Table 5.10: Reset timing requirements

Symbol	Description	Min	Typ	Max	Unit
t_{RST_PULSE}	Duration to assert RESET_N to guarantee a full system reset	20	-	-	ns

Table 5.11: Programming time

Symbol	Description	Min	Typ	Max	Unit
t_{ERASE_FULL}	Time taken to erase the entire flash memory	-	-	44.1	ms
$t_{PGM\_FULL\_UART0}$	Time taken to program the entire flash memory over UART0 including a full erase	-	-	16.2	s
$t_{PGM\_FULL\_USB}$	Time taken to program the entire flash memory over USB including a full erase	-	-	TBD	s

5.6 NON-VOLATILE MEMORY RELIABILITY

Qualified for an ambient temperature of TA=+25°C and a supply voltage of VDD=+3.3V. The on-chip memory is based on SuperFlash® technology.

Table 5.12: On-chip flash

Symbol	Description	Min	Typ	Max	Unit
END_{FLASH}	Endurance, erase cycles before failure	10000	-	-	cycles
$RET_{FLASH-LT}$	Data retention	100	-	-	years
$RET_{FLASH-HT}$	Data retention *(Qualified for a junction temperature of T_J=-10°C to +85°C)*	10	-	-	years

Table 5.13: On-chip high endurance NVM

Symbol	Description	Min	Typ	Max	Unit
END_{NVM}	Endurance, erase cycles before failure	100000	-	-	cycles
RET_{NVM-LT}	Data retention	100	-	-	years
RET_{NVM-HT}	Data retention *(Qualified for a junction temperature of T_J=-10°C to +85°C)*	10	-	-	years

Table 5.14: EEPROM

Symbol	Description	Min	Typ	Max	Unit
END_{EEPROM}	Endurance, erase cycles before failure	1Mil	-	-	cycles
RET_{EEPROM}	Data retention	100	-	-	years

5.7 ANALOG-TO-DIGITAL CONVERTER

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.15: 12-bit ADC characteristics

Symbol	Description	Min	Max	Unit
V_{BG}	Internal reference voltage	+1.20	+1.30	V
DNL_{ADC}	Differential non-linearity	-1.00	+1.00	LSB
ACC_{8b}	Accuracy when sampling 20ksps with 8-bit resolution	-2.00	2.00	LSB
ACC_{12b}	Accuracy when sampling 10ksps with 12-bit resolution	-5.00	5.00	LSB
f_{S-8b}	8-bit sampling rate	-	0.02	Msps
f_{S-12b}	12-bit sampling rate	-	0.01	Msps

5.8 DC CHARACTERISTICS

Measured at an ambient temperature of TA=-10°C to +85°C.

Table 5.16: Digital input characteristics, supply voltage of V_{DD}=+2.3V to +3.0V

Symbol	Description	Min	Max	Unit
V_{IH}	Logical 1 input voltage high level	+1.85	-	V
V_{IL}	Logical 0 input voltage low level	-	+0.75	V
V_{IF}	Falling input trigger threshold	+0.75	+1.05	V
V_{IR}	Rising edge trigger threshold	+1.35	+1.85	V
V_{HYS}	Schmitt trigger voltage hysteresis	+0.55	+0.85	V
I_{IH}	Logical 1 input high level current leakage	-	+7.00	µA
I_{IL-NPU}	Logical 0 input low level current leakage *(no internal pull-up resistor)*	-7.00	-	µA
I_{IL-PU}	Logical 0 input low level current leakage *(with internal pull-up resistor)*	+35.00	+90.00	µA
PU_{IN}	Internal pull-up resistance *(T_A=+25°C)*	20.00	30.00	kΩ
C_{IN}	Pin input capacitance	-	15.00	pF

Table 5.17: Digital output characteristics, supply voltage of V_{DD}=+2.3V to +3.0V

Symbol	Description	Min	Max	Unit
V_{OH}	Logical 1 output voltage high level	+1.9	-	V
V_{OL}	Logical 0 output voltage low level	-	+0.4	V
I_{OH-LP}	Logical 1 output high level current sourcing	-	+6.0	mA
I_{OL-LP}	Logical 0 output low level current sinking	-6.0	-	mA

Table 5.18: Digital input characteristics, supply voltage of V_{DD}=+3.0V to +3.6V

Symbol	Description	Min	Max	Unit
V_{IH}	Logical 1 input voltage high level	+2.10	-	V
V_{IL}	Logical 0 input voltage low level	-	+0.90	V
V_{IF}	Falling input trigger threshold	+0.90	+1.30	V
V_{IR}	Rising edge trigger threshold	+1.60	+2.10	V
V_{HYS}	Schmitt trigger voltage hysteresis	+0.65	+0.95	V
I_{IH}	Logical 1 input high level current leakage	-	+10.00	µA
I_{IL-NPU}	Logical 0 input low level current leakage *(no internal pull-up resistor)*	-10.00	-	µA
I_{IL-PU}	Logical 0 input low level current leakage *(with internal pull-up resistor)*	+40.00	+120.00	µA
PU_{IN}	Internal pull-up resistance *(T_A=+25°C)*	15.00	20.00	kΩ
C_{IN}	Pin input capacitance	-	15.00	pF

Table 5.19: Digital output characteristics, supply voltage of V_{DD}=+3.0V to +3.6V

Symbol	Description	Min	Max	Unit
V_{OH}	Logical 1 output voltage high level	+2.4	-	V
V_{OL}	Logical 0 output voltage low level	-	+0.4	V
I_{OH-LP}	Logical 1 output high level current sourcing	-	+8.0	mA
I_{OL-LP}	Logical 0 output low level current sinking	-8.0	-	mA

5.9 RF CHARACTERISTICS

5.9.1 TRANSCEIVER

The radio transceiver of the ZM5304 is based on the SD3503 modem chip and an external SAW filter. Refer to [5] for measurements on the conducted performance of the SD3503. Although the crystal is factory calibrated, it is mandatory to calibrate the transmitter in production. Refer to [6] for more information.

5.9.2 ANTENNA

The radiation measurements for the ZM5304 were performed on the ZDP03A Z-Wave Development Platform. [7] The orientation of the ZM5304 during the measurements is shown in Figure 5.2.

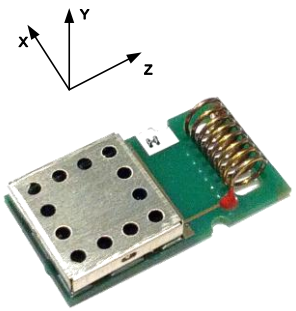


Figure 5.2: Measurement orientation

5.9.2.1 REGION E

Table 5.20: Region E performance

Symbol	Description	Min	Typ	Max	Unit
f_C	Carrier frequency	-	868.40	-	MHz
TRP	Total radiated power	-	-3.05	-	dBm
ε_R	Radiation efficiency	-	-7.05	-	dB
D	Directivity	-	3.47	-	dBi
G	Peak gain	-	-3.58	-	dBi

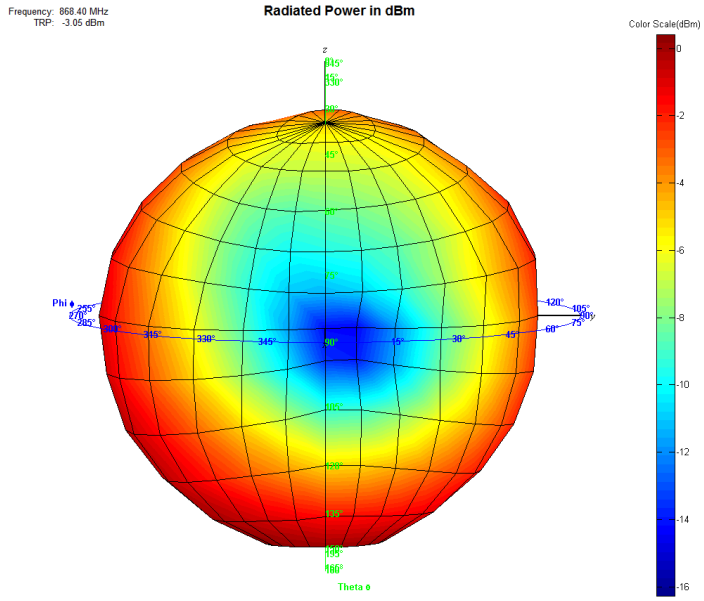


Figure 5.3: YZ plane (X front view)

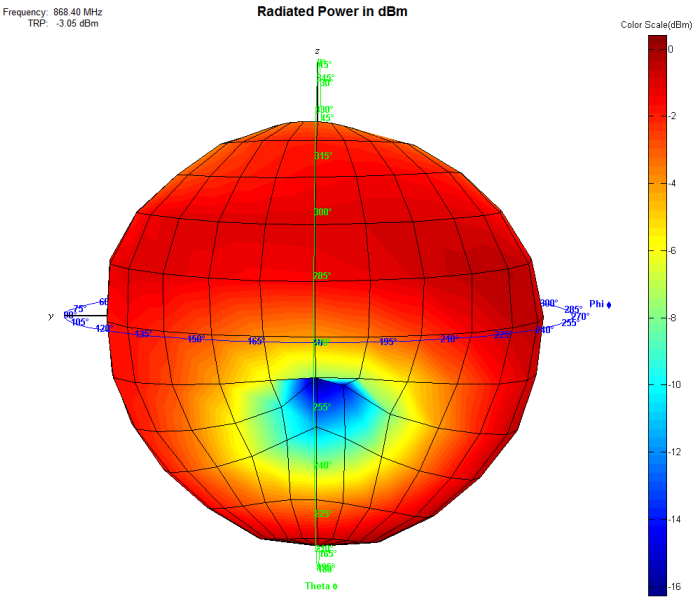


Figure 5.4: YZ plane (X back view)

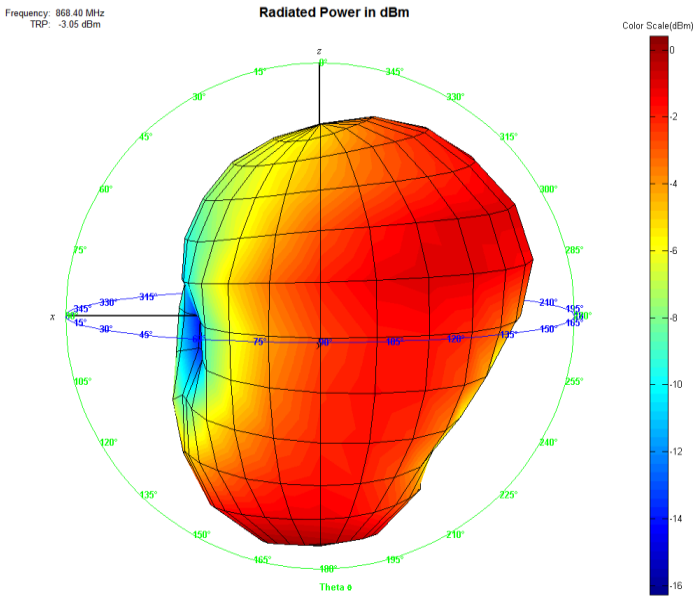


Figure 5.5: XZ plane (Y front view)

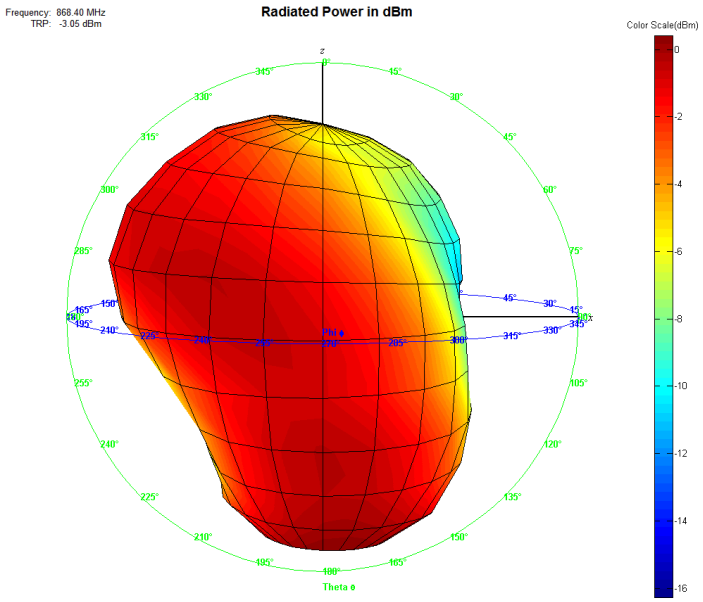


Figure 5.6: XZ plane (Y back view)

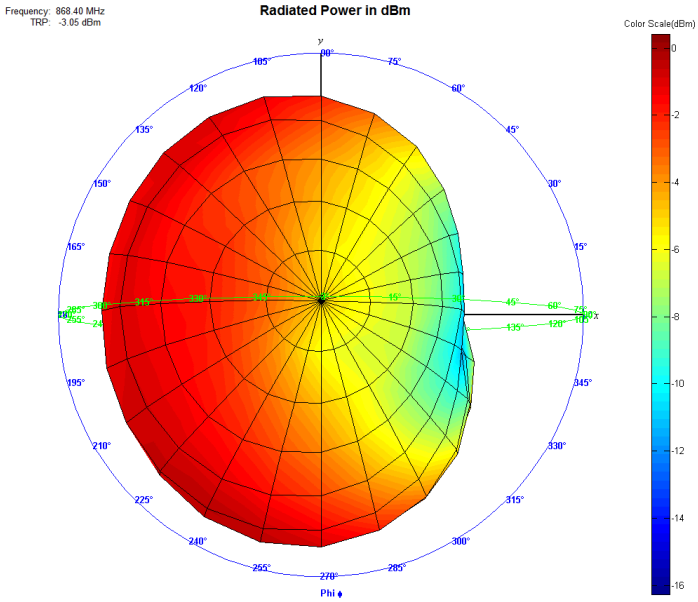


Figure 5.7: XY plane, (Z front view)

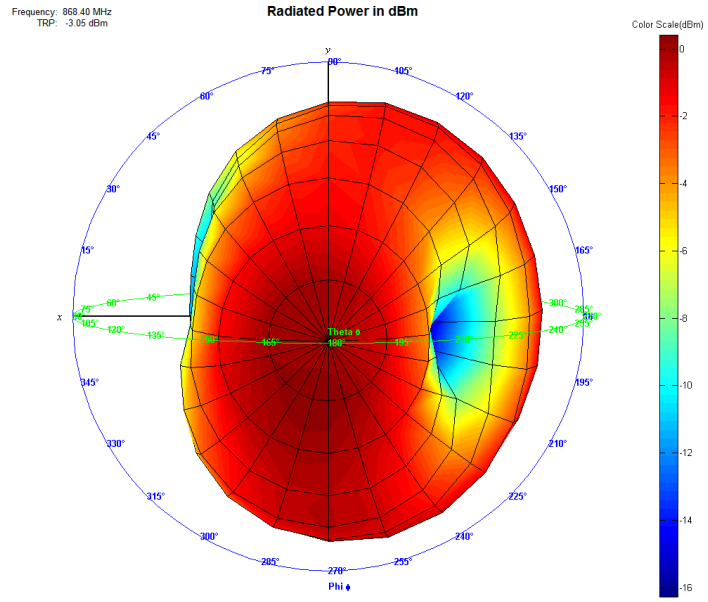


Figure 5.8: XY plane, (Z back view)

5.9.2.2 REGION U

Table 5.21: Region U performance

Symbol	Description	Min	Typ	Max	Unit
f_C	Carrier frequency	-	908.40	-	MHz
TRP	Total radiated power	-	-3.95	-	dBm
ε_R	Radiation efficiency	-	-7.95	-	dB
D	Directivity	-	4.21	-	dBi
G	Peak gain	-	-3.74	-	dBi

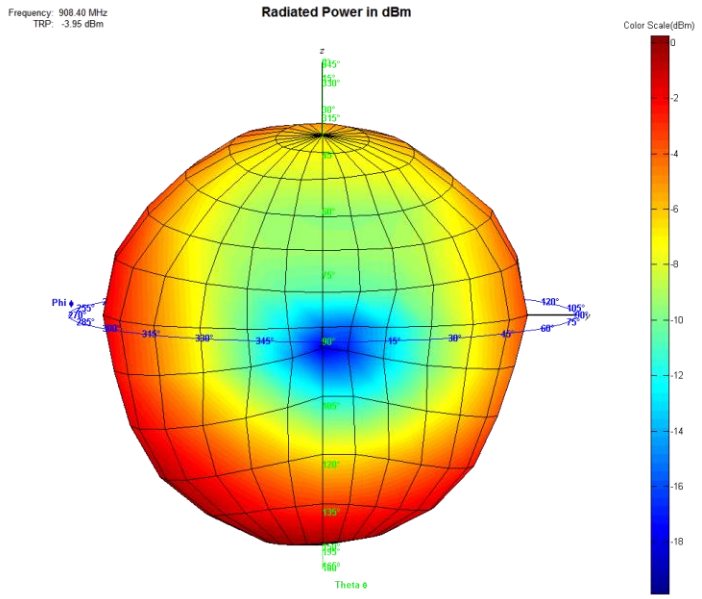


Figure 5.9: YZ plane (X front view)

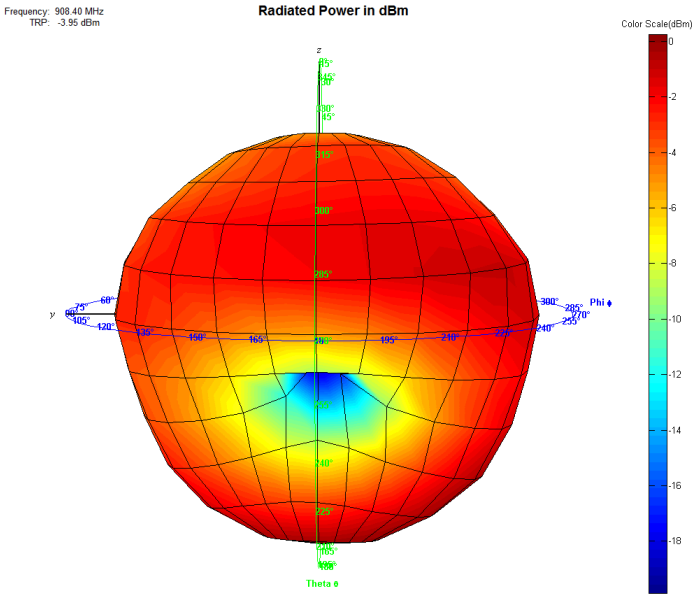


Figure 5.10: YZ plane (X back view)

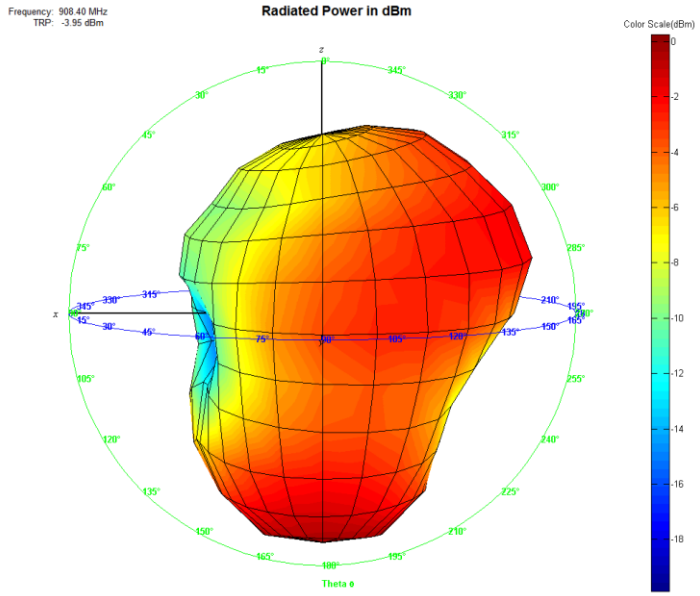


Figure 5.11: XZ plane (Y front view)

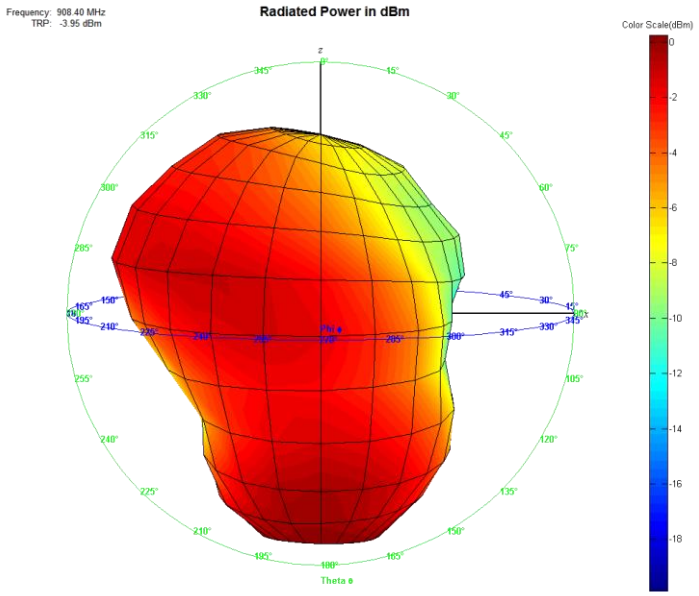


Figure 5.12: XZ plane (Y back view)

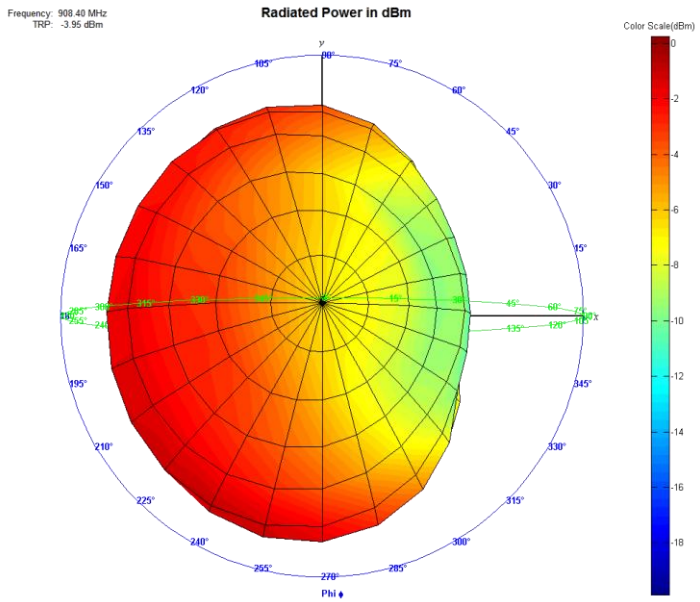


Figure 5.13: XY plane (Z front view)

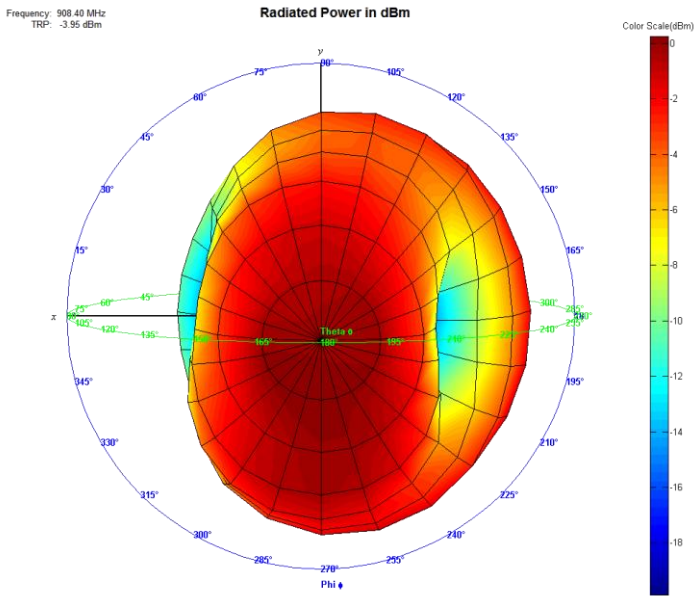


Figure 5.14: XY plane (Z back view)

5.9.2.3 REGION H

Table 5.22: Region H performance

Symbol	Description	Min	Typ	Max	Unit
f_C	Carrier frequency	-	921.40	-	MHz
TRP	Total radiated power	-	-7.73	-	dBm
ε_R	Radiation efficiency	-	-11.73	-	dB
D	Directivity	-	4.26	-	dBi
G	Peak gain	-	-7.47	-	dBi

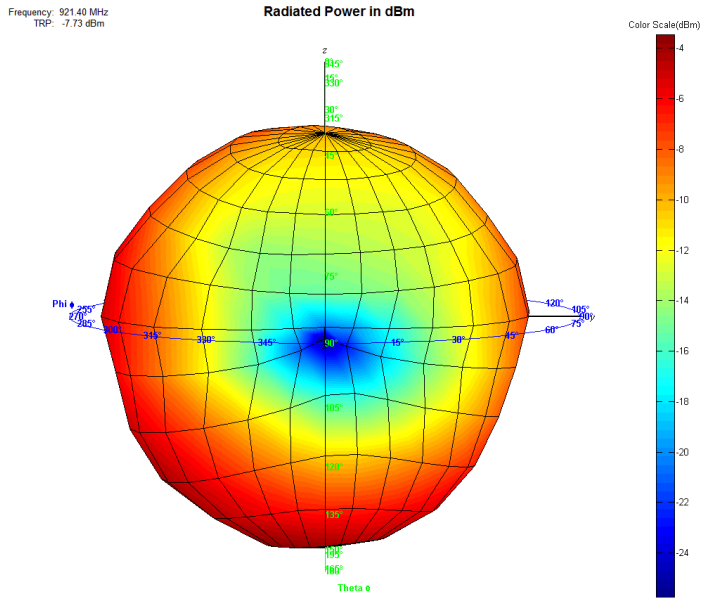


Figure 5.15: YZ plane (X front view)

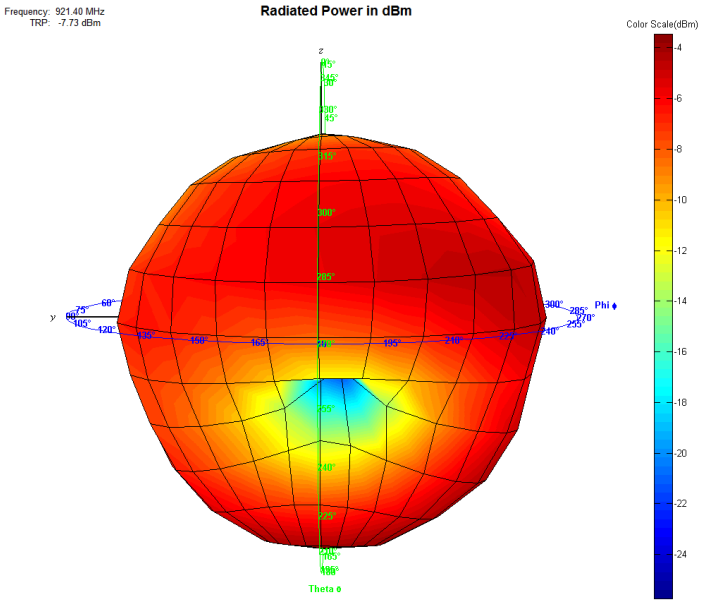


Figure 5.16: YZ plane (X back view)

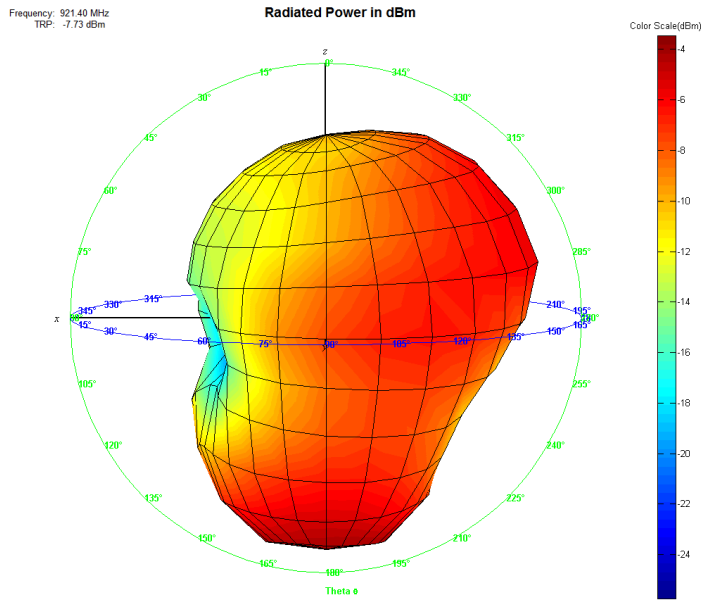


Figure 5.17: XZ plane (Y front view)

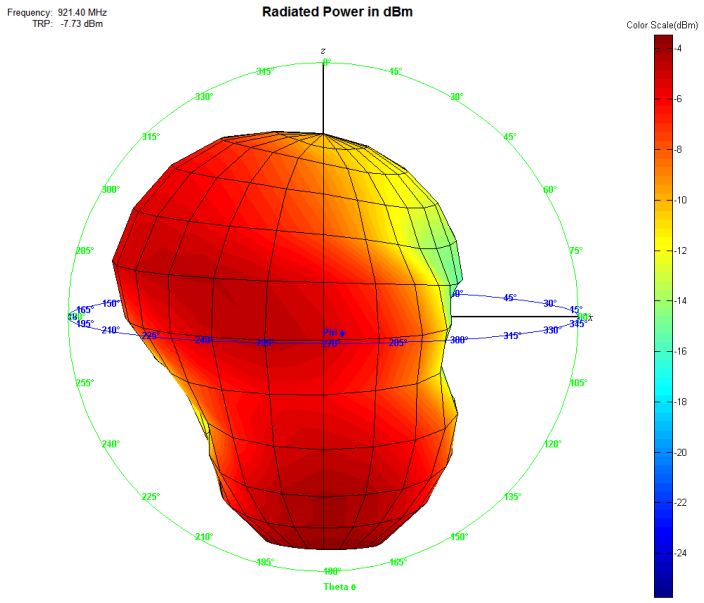


Figure 5.18: XZ plane (Y back view)

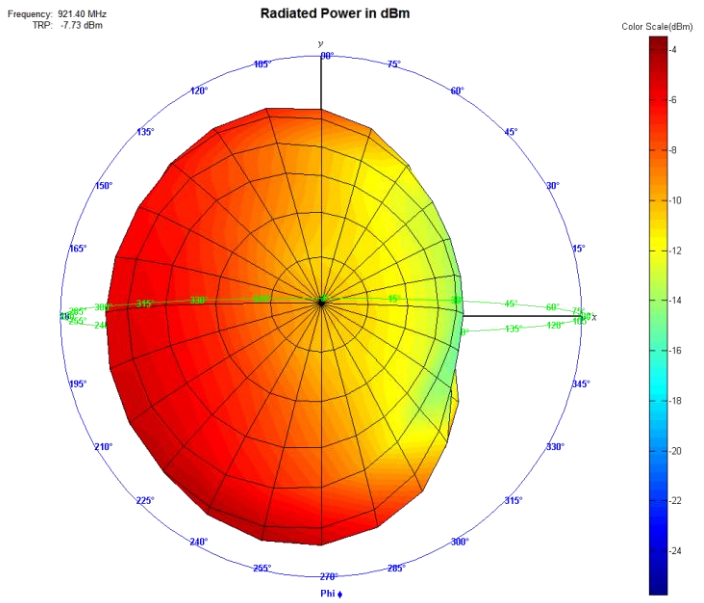


Figure 5.19: XY plane (Z front view)

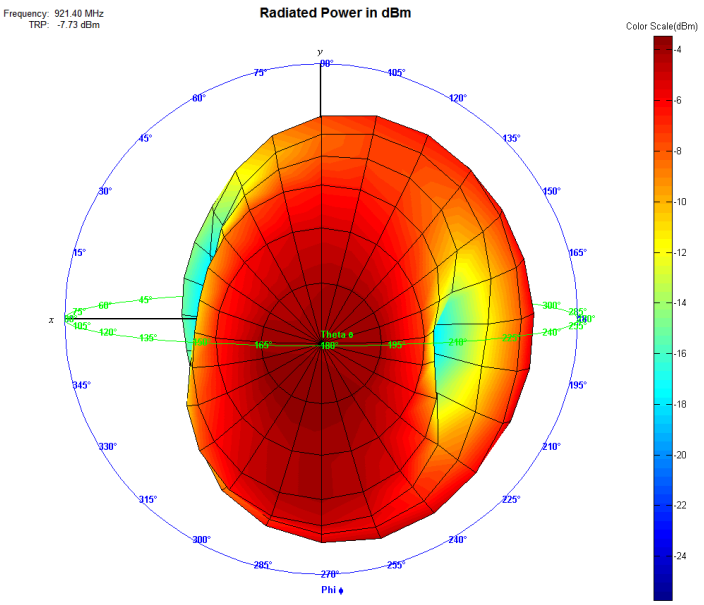


Figure 5.20: XY plane (Z back view)

5.9.3 REGULATORY COMPLIANCE

The ZM5304 has been tested on the ZDP03A Z-Wave Development Platform to be compliant with the following regulatory standards.

- **ACMA COMPLIANCE**
  - AS/NZS 4268
  - CISPR 22
- **CE COMPLIANCE**
  - EN 300 220-1/2
  - EN 301 489-1/3
  - EN 55022
  - EN 60950-1
  - EN 61000-4-2/3
  - EN 62479
- **FCC COMPLIANCE**
  - FCC CFR 47 Part 15 Subpart C §15.212
- **IC COMPLIANCE**
  - RSS-GEN
  - RSS-210
  - ANSI C63.10
- **MIC COMPLIANCE**
  - ARIB STD-T108

6 Z-WAVE FREQUENCIES

Table 6.1: Z-Wave RF specification

Data rate	9.6kbps	40kbps	100kbps	
Modulation	Frequency Shift Keying (FSK)	FSK	Gaussian Frequency Shift Keying (GFSK)	
Frequency deviation	f_C±20kHz	f_C±20kHz	f_C±29.3kHz	
Coding	Manchester encoded	Non-return to Zero (NRZ)	NRZ	
United Arab Emirates	868.42 MHz	868.40 MHz	869.85 MHz	E
Australia	921.42 MHz	921.40 MHz	919.80 MHz	H
Brazil	921.42 MHz	921.40 MHz	919.80 MHz	H
Canada	908.42 MHz	908.40 MHz	916.00 MHz	U
Chile	908.42 MHz	908.40 MHz	916.00 MHz	U
China	868.42 MHz	868.40 MHz	869.85 MHz	E
European Union	868.42 MHz	868.40 MHz	869.85 MHz	E
Hong Kong	919.82 MHz	919.80 MHz	919.80 MHz	H
Israel	916.02 MHz	916.00 MHz	-	U
India	865.20 MHz	865.20 MHz	865.20 MHz	E
Japan	-	-	922.50 MHz	H
	-	-	923.90 MHz	H
	-	-	926.30 MHz	H
Korea	-	-	919.70 MHz	H
	-	-	921.70 MHz	H
	-	-	923.10 MHz	H
Mexico	908.42 MHz	908.40 MHz	916.00 MHz	U
Malaysia	868.12 MHz	868.10 MHz	868.10 MHz	E
New Zealand	921.42 MHz	921.40 MHz	919.80 MHz	H
Russia	869.02 MHz	869.00 MHz	-	E
Singapore	868.42 MHz	868.40 MHz	869.85 MHz	E
Taiwan	-	-	922.50 MHz	H
	-	-	923.90 MHz	H
	-	-	926.30 MHz	H
United States	908.42 MHz	908.40 MHz	916.00 MHz	U
South Africa	868.42 MHz	868.40 MHz	869.85 MHz	E

7 MODULE INFORMATION

7.1 MODULE MARKING

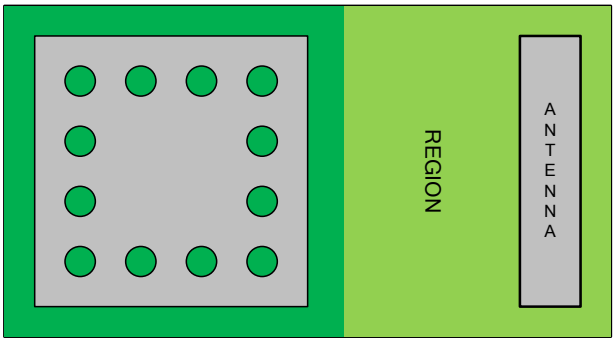


Figure 7.1: Marking placement

Table 7.1: Marking description

REGION	E FCC ID: D87-ZM5304-U H

NB: The shield is only mounted on the U regional module.

7.2 MODULE DIMENSIONS

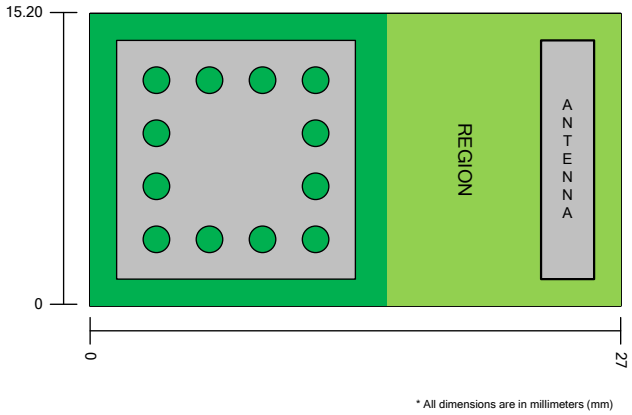


Figure 7.2: Top view of module

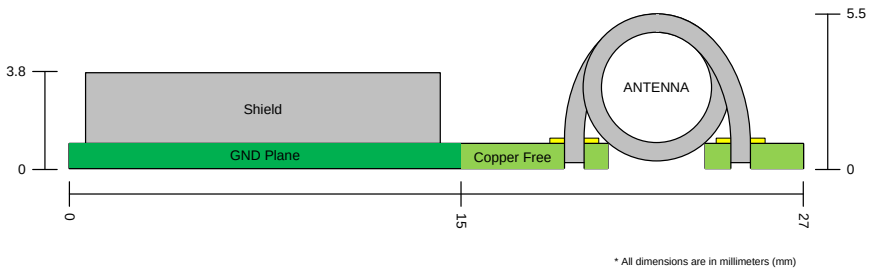


Figure 7.3: Side view of module

8 PCB MOUNTING AND SOLDERING

8.1 PCB MOUNTING PATTERN

The land pattern is required to include two drilled holes of 70 mil (=1.8mm) at the positions indicated, to ensure clearance to antenna structures.

The recommended land pattern includes a layout of 48 pads of size 1.70 mm x 0.65 mm positioned as indicated in the figure.

All coordinates are relative to the centre of pad 11.

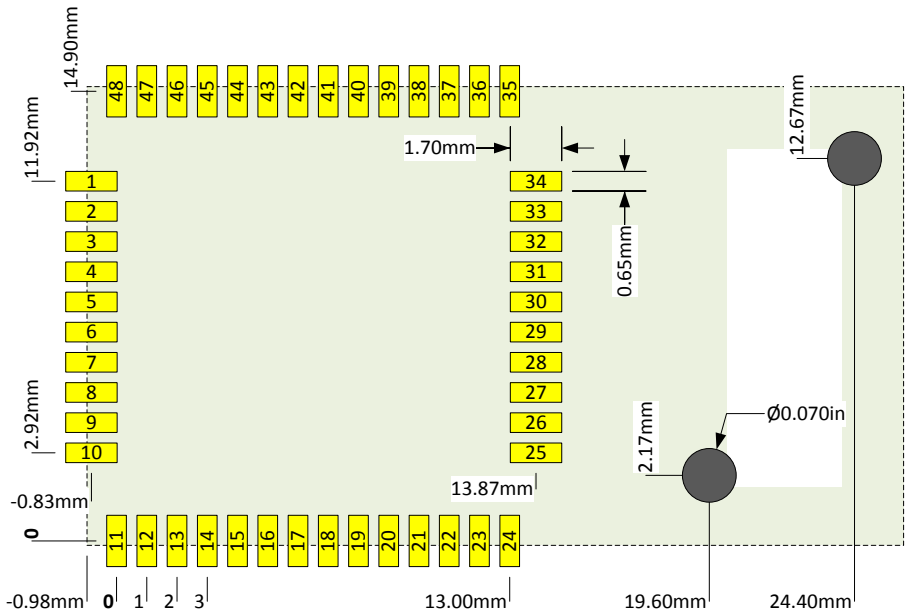


Figure 8.1: Top view of land pattern

8.2 RECOMMENDED PLACEMENT ON PCB

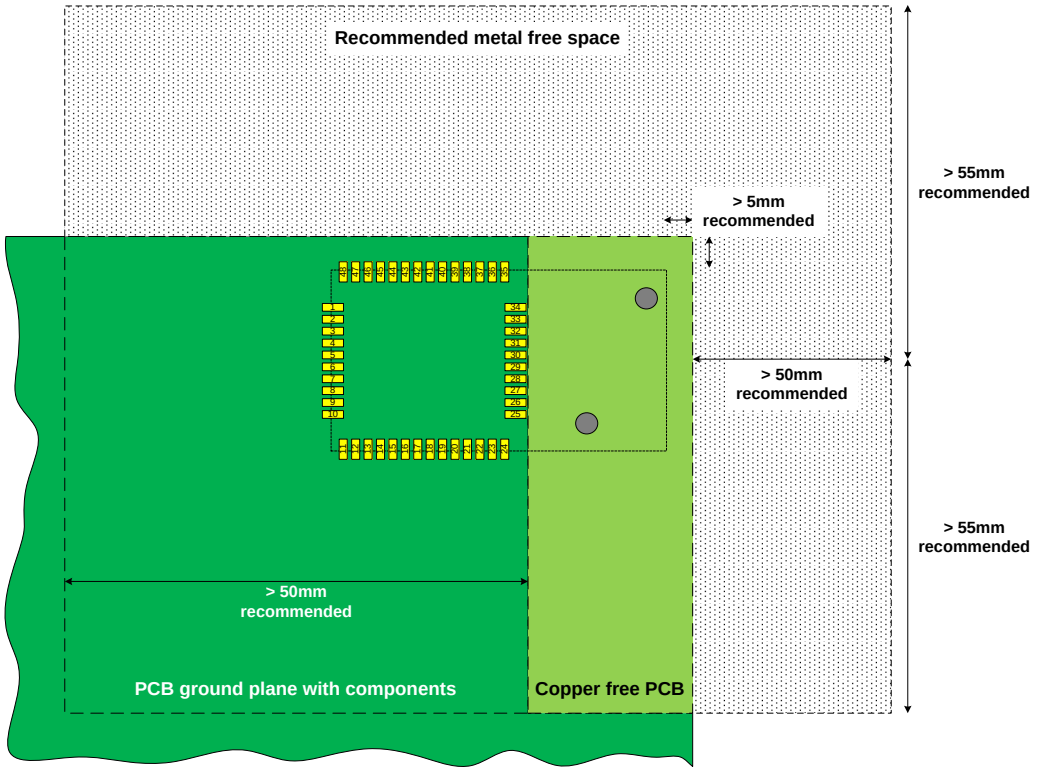


Figure 8.2: Top view of recommended placement of module on PCB

8.3 SOLDERING INFORMATION

The soldering details to properly solder the ZM5202 module on standard PCBs are described below. The information provided is intended only as a guideline and Sigma Designs is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020D.1 for more information.

Table 8.1: Soldering details

PCB solder mask expansion from landing pad edge	0.1 mm
PCB paste mask expansion from landing pad edge	0.0 mm
PCB process	Pb-free (Lead free for RoHS[3] compliance)
PCB finish	Defined by the manufacturing facility (EMS) or customer
Stencil aperture	Defined by the manufacturing facility (EMS) or customer
Stencil thickness	Defined by the manufacturing facility (EMS) or customer
Solder paste used	Defined by the manufacturing facility (EMS) or customer
Flux cleaning process	Defined by the manufacturing facility (EMS) or customer

[3] RoHS = Restriction of Hazardous Substances Directive, EU

Table 8.2: Typical reflow profile

Symbol	Description	Min	Max	Unit
T_L to T_P	Ramp-up rate	-	3	°C/s
T_S	Preheat temperature	150	200	°C
t_S	Preheat time	60	120	s
T_L	Heating temperature	215	220	°C
t_L	Heating time	60	150	s
T_P	Peak temperature	-	260	°C
t_P	Time within 5°C of actual peak temperature	28	32	s
T_P to T_L	Ramp-down rate	-	6	°C/s
t	Time 25°C to peak temperature	-	8	min

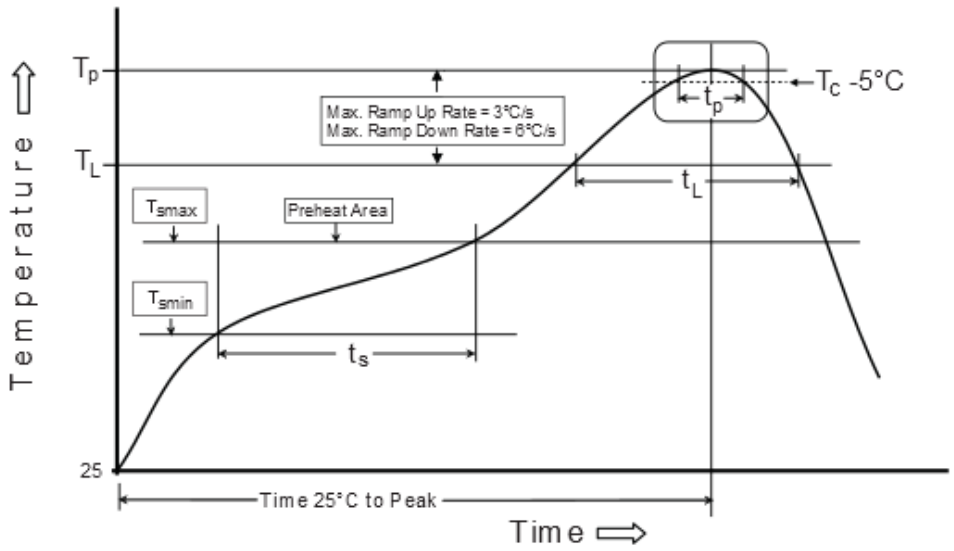


Figure 8.3: Typical reflow profile

9 ORDERING INFORMATION

Table 9.1: Ordering codes

Orderable Device	Status	Package Type	Pins	Minimum Order Quantity	Description
ZM5304AE-CME3R	ACTIVE	SOM	48	500 pcs.	ZM5304 Modem Module, No Shield, RevA, 868MHz Band, Tape and Reel
ZM5304AU-CME3R	ACTIVE	SOM	48	500 pcs.	ZM5304 Modem Module, With Shield, RevA, 908MHz Band, Tape and Reel
ZM5304AH-CME3R	ACTIVE	SOM	48	500 pcs.	ZM5304 Modem Module, No Shield, RevA, 921MHz Band, Tape and Reel

9.1 TAPE AND REEL INFORMATION

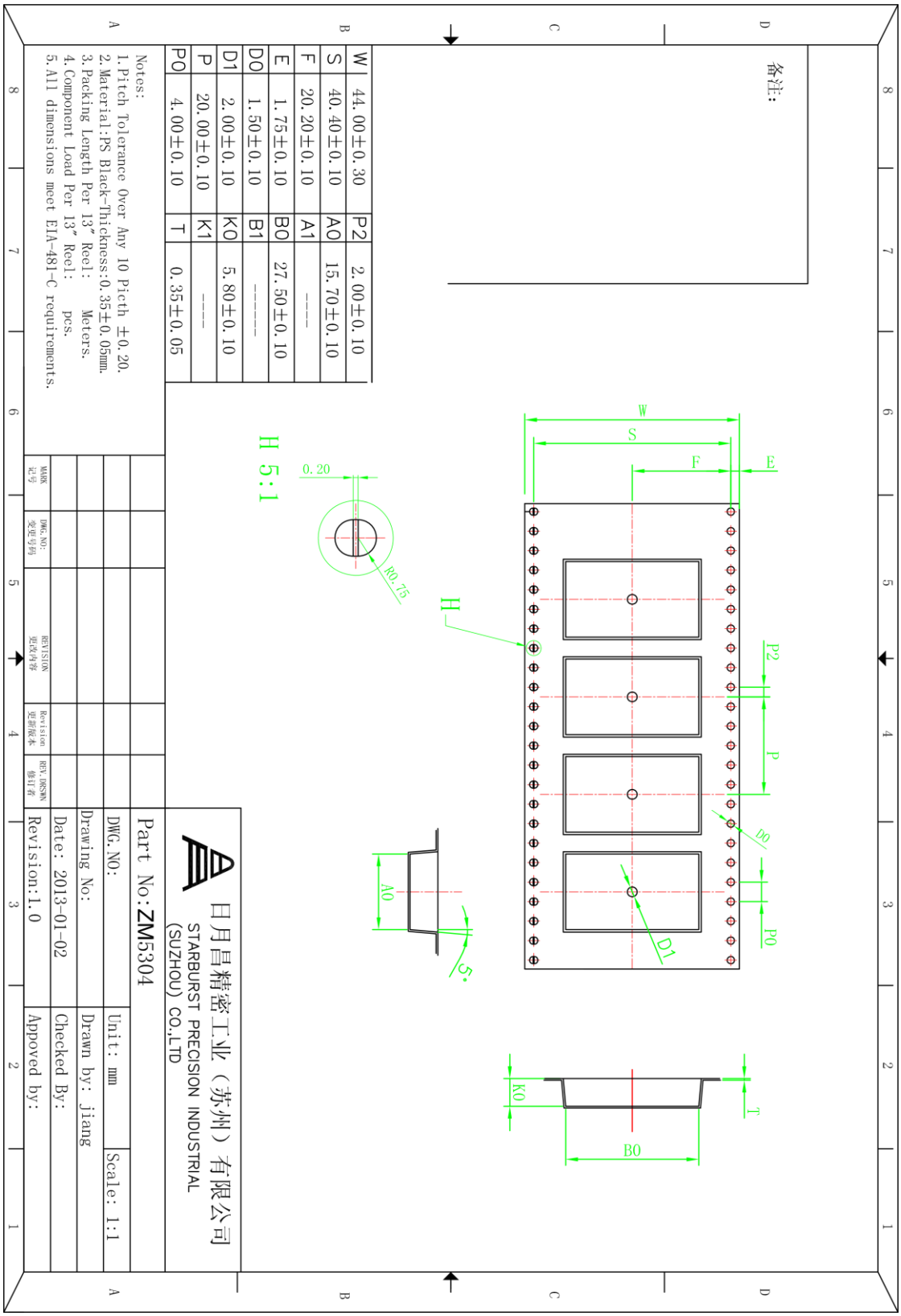


Figure 9.1: Tape information

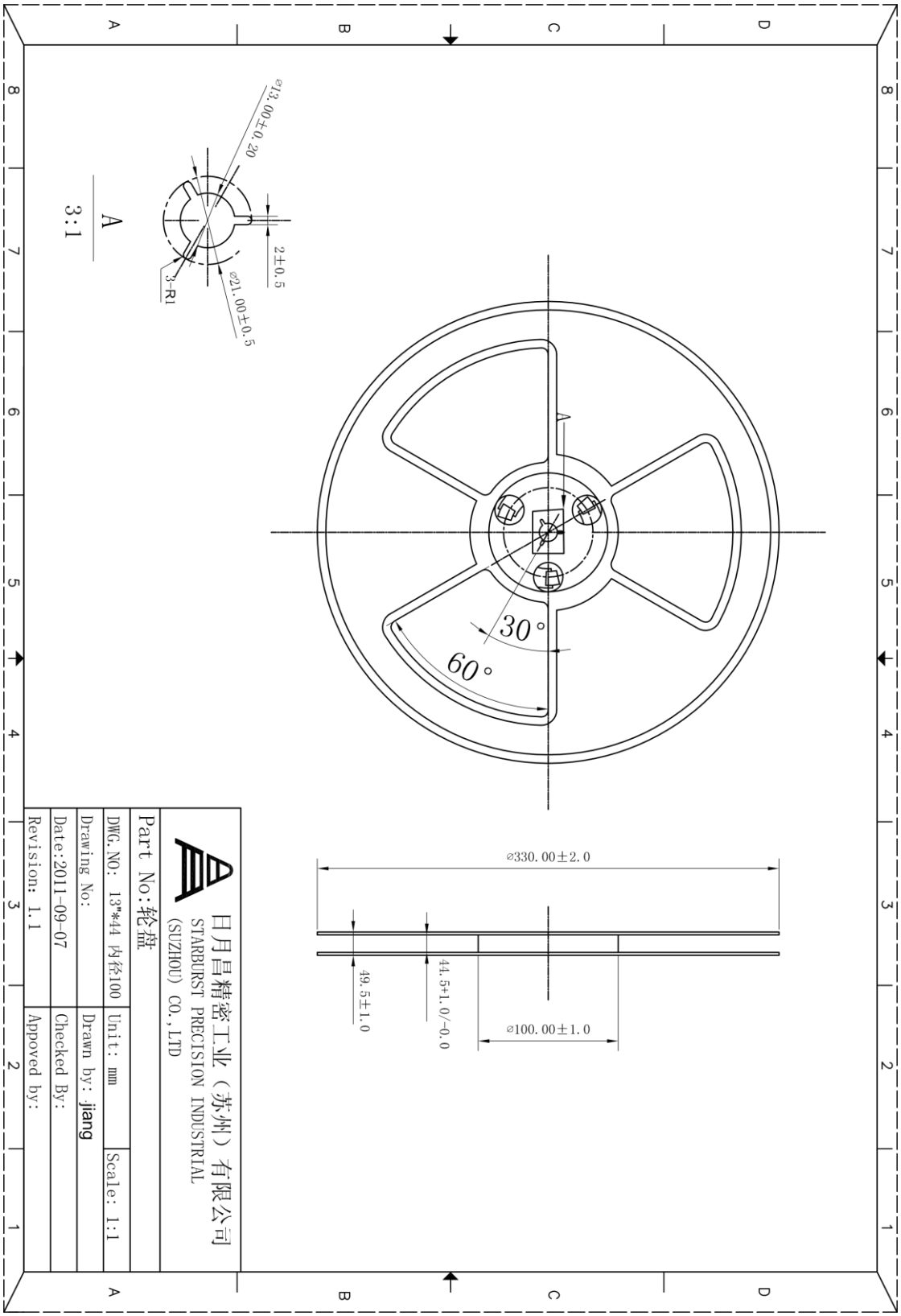


Figure 9.2: Reel information

10 ABBREVIATIONS

Abbreviation	Description
2FSK	2-key Frequency Shift Keying
2GFSK	2-key Gaussian Frequency Shift Keying
ACM	Abstract Control Model
ACMA	Australian Communications and Media Authority
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
API	Application Programming Interface
APM	Auto Programming Mode
AV	Audio Video
BOD	Brown-Out Detector
CBC	Cipher-Block Chaining
CDC	Communications Device Class
CE	Conformité Européenne
COM	Communication
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
D	Differential
D-	Differential Minus
D+	Differential Plus
DC	Direct Current
DMA	Direct Memory Access
ECB	Electronic CodeBook
EMS	Electronic Manufacturing Services
FCC	Federal Communications Commission
FER	Frame Error Rate
FLiRS	Frequently Listening Routing Slave
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose Input Output
I	Input
I/O	Input / Output
IC	Integrated Circuit
IF	Intermediate Frequency
IPC	Interconnecting and Packaging Circuits
IRAM	Indirectly addressable Random Access Memory
ISM	Industrial, Scientific, and Medical
ISP	In-System Programming
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
lsb	Least Significant Bit
LSB	Least Significant Byte
MCU	Micro-Controller Unit
MIC	Ministry of Internal affairs and Communications, Japan
msb	Most Significant Bit
MSB	Most Significant Byte
NRZ	Non-Return-to-Zero
NVM	Non-Volatile Memory
NVR	Non-Volatile Registers
O	Output
OEM	Original Equipment Manufacturer
OFB	Output FeedBack

Abbreviation	Description
Pb	Lead
PCB	Printed Circuit Board
POR	Power-On Reset
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RS-232	Recommended Standard 232
RX	Receive
S	Supply
SAW	Surface Acoustic Wave
SFR	Special Function Register
SOM	System-in-Module
SRAM	Static Random Access Memory
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
XRAM	External Random Access Memory
XTAL	Crystal

11 REVISION HISTORY

Date	Version	Affected	Revision
2014/04/11	7	§2.3.1	Mandatory mounting holes added to the PCB mounting pattern. Drawing and text is updated.
2013/12/12	6A	§2.3.1	Increased RESET_N low period
2013/11/13	5A	§Cover, §2.1.2, Figure 2.4, Figure 2.5, Figure 3.2, §5.1, §5.4, Table 5.13, §5.9.1, §5.9.2, §5.9.3	Updated with measurement values Changed to a battery monitor implementation Added resistor values Removed size of application area Added UART0 and RESET_N as test points Updated test conditions Removed graph and updated current consumption values Added NVM performance data Replaced transmitter and receiver with a reference to SD3503 Added radiated measurements of the antennas Updated the standards list
2013/08/28	4B	§5.9, §11	Added transmitter and receiver bandwidth to Tables 5.19 and 5.21 Updated 4A revision description
2013/08/26	4A	§Cover, §2, §3, §4, §5.2, §5.8, §6, §7, §10	Clarified cover page summary to reflect controller based applications Added FCC ID to cover page Changed TXD and RXD to UART0 TX and UART0 RX in Figure 2.1, Figure 3.1, and Figure 4.1 Renamed ‘pad’ to ‘pin’ throughout document except §8.3 Added pin dimensions to Figure 4.1 Fixed Korea Z-Wave frequency Changed the location of the FCC ID label in Figure 7.1 and Figure 7.2 Updated Figure 7.3 to thru-hole antenna Added table of abbreviations
2013/07/02	3A	§1, §2, §5	Removed remnants of WUT
2013/07/02	2B	§2.1.8, §10	Removed invalid references to the WUT and added the date to the references
2013/07/01	2A	§2.1, §2.3, §7.2, §6	Added dimensions of shield Changed the low operating voltage from 2.5V to 2.3V Added AES, ADC, XTAL driver, BOD, RST controller, WUT, Watchdog, and RF transceiver sections to the peripheral descriptions Changed “Firmware Upgrade” to “Module Programming” and added default programming mode Changed the module width to 15.05mm Removed the frequency from the module marking and added region data to the frequency table
2013/06/03	1F	§5.5	Added transition time values Removed empty page
2013/05/31	1E	§All	Updated IO characteristics and added USB termination resistor values
2013/05/30	1D	§All	Added missing receiver graphs and proposed changes
2013/05/27	1C	§All	Updated layout with feedback from the technical writer, and data from the latest corner tests
2013/02/22	1A	§All	Preliminary draft released
2013/02/18	1A	§All	Initial draft

12 REFERENCES

[1] INS12350, Instruction, “Serial API Host Application Programming Guide”
[2] INS12308, Instruction, “Z-Wave 500 Series Application Programmers Guide”
[3] INS11681, Instruction, “500 Series Z-Wave Single Chip Programming Mode”
[4] DSH12468, Datasheet, “ZDB5304 Z-Wave Development Board”
[5] DSH12469, Datasheet, “SD3503”
[6] INS12213, Instruction, “500 Series Hardware Integration Guide”
[7] DSH11243, Datasheet, “ZDP03A, Z-Wave Development Platform”

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