CMPEN 431 - HW 2 - Quang Nguyen

Thursday, September 17, 2015 7:41 PM

#1

A) @ 4 ps per bit, an add would take 64 ps = T_{add}

Using RCA, it would take at least 1.024 ns

B) @ 4 ps per bit, an add would take 0.16 ps = T_{add}

Using CLA, it would take at least 0.256 ns

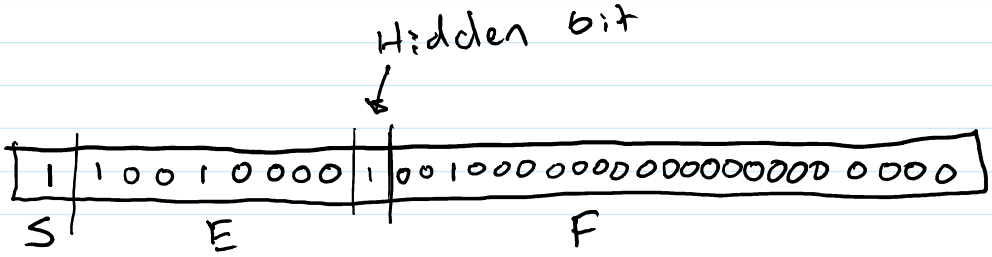
#2

A) -2.25 X 2^{+16}

$0.25 = \frac{1}{4} = \frac{1}{2^2} = 0.01 \quad therefore \quad 2.25\ x\ 2^{+16} \rightarrow 10.01_2 x\ 2^{16}$

$normalize(10.01_2 x\ 2^{16}) = 1.001\ x\ 2^{17}$

$Fractional = 0.001_2 \qquad Exponential = 17 + 127 = 144$

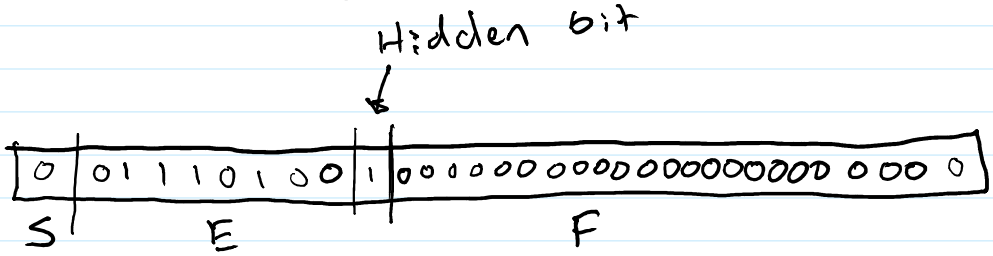


B) 0.50 X 2^{-10}

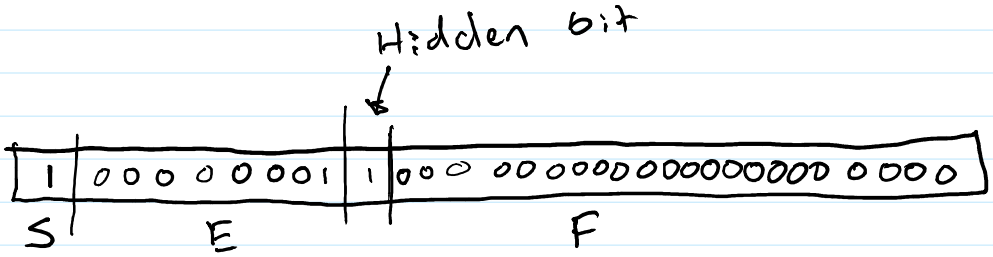
$0.5_{10} = \frac{1}{2_{10}} = \frac{1}{2^1_{10}} = 0.1_2$

$normalize(0.1_2\ x\ 2^{10}) = 1.0\ x\ 2^{-11}$

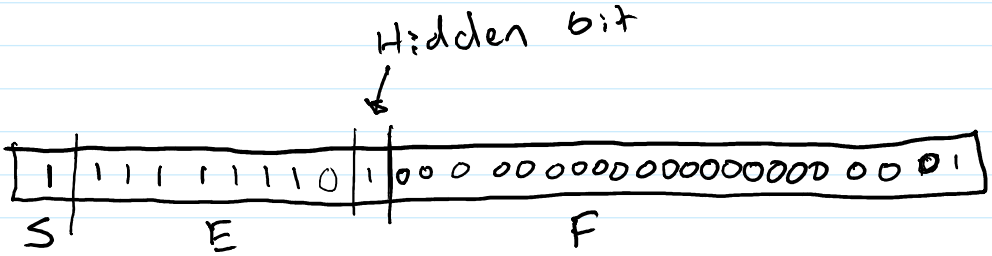
$Fractional = 1.0000_2 \qquad Exponential = -11 + 127 = 116$



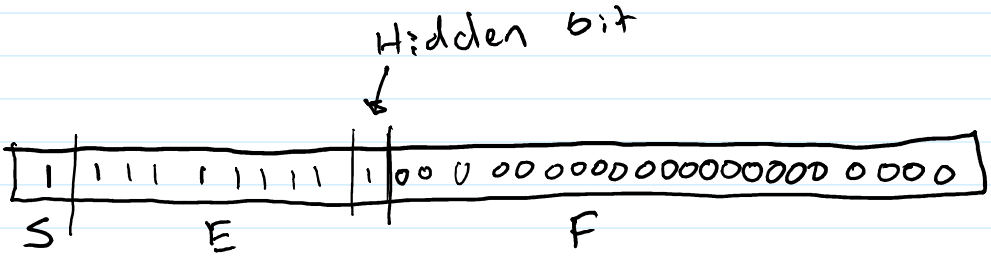
C) The smallest negative number



D) The largest negative number

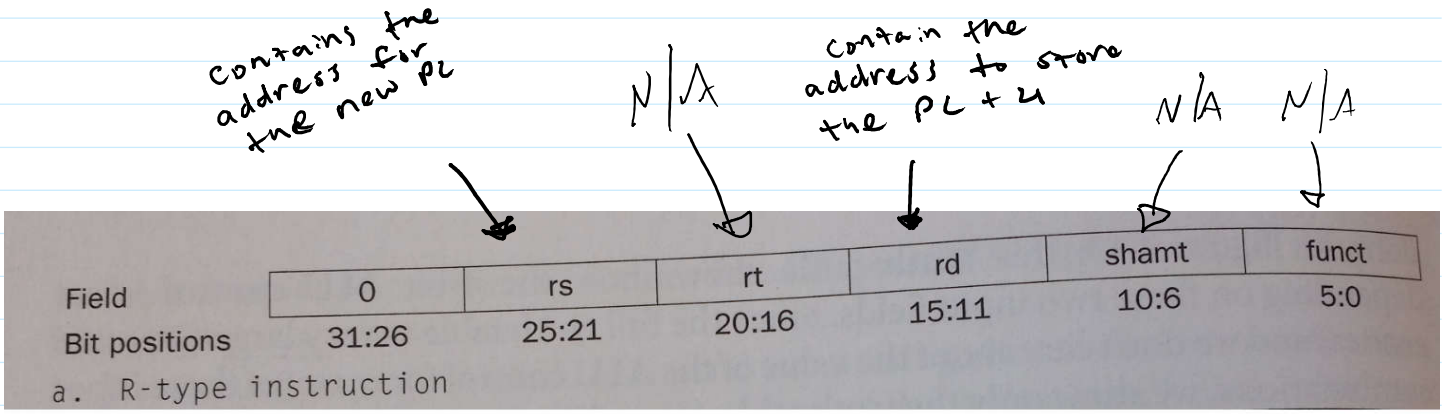


D) +∞



#3

An additional JAR bit needs to be added to the control unit inorder to make the JAR instruction possible.



#4

A)

```
LW    $4, -100($3)
NOP                    <- Load-use data hazard
NOP
SW    $2, 8($4)
ADD   $2, $4, $4
```

B)

```
LW    $4, -100($3)     <- Load use data hazard
NOP
SW    $2, 8($4)
ADD   $2, $4, $4
```

#5

A) 2 stalls would occur
B) 1 stall would occur

#6

Set 1: cache 2 lat = 5. Clock = 1 GHz		bzip2	hmmer	mcf	sjeng	milc	equake
	# of instructions	2500000	2500000	2500000	2500000	2500000	2500000
	CPI	4.0102	2.3681	2.568	2.8592	2.5335	2.7813
	II1 cache miss rate	0.0002	0.0002	0.0412	0.0001	0.0031	0.0595
	D11 cache miss rate	0.4186	0.0832	0.0874	0.0798	0.12	0.0209
	UL2 cache miss rate	0.2959	0.1677	0.158	0.2538	0.25	0.0139
Int Mean	**2.889691006**	**Float Mean**	**2.65451004**	**Performance (int)**	173.0288806	**Performance (int)**	188.3586773
Set 1: cache 2 lat = 10. Clock = 1.5 GHz		bzip2	hmmer	mcf	sjeng	milc	equake
	# of instructions	2500000	2500000	2500000	2500000	2500000	2500000
	CPI	4.3233	2.4082	2.7908	2.8963	2.5474	3.125
	I11 cache miss rate	0.0002	0.0002	0.0411	0.0001	0.0031	0.0595
	D11 cache miss rate	0.4186	0.0833	0.0874	0.0798	0.12	0.0209
	UL2 cache miss rate	0.2959	0.1676	0.158	0.2538	0.25	0.0139
Int Mean	**3.028796159**	**Float Mean**	**2.821457956**	**Performance (int)**	247.6231349	**Performance (int)**	265.8200163
Set 1: cache 2 lat = 15. Clock = 2 GHz		bzip2	hmmer	mcf	sjeng	milc	equake
	# of instructions	2500000	2500000	2500000		2500000	2500000
	CPI	4.6364	2.4488	3.0137	2.9339	2.5613	3.4694
	I11 cache miss rate	0.0002	0.0002	0.0411	0.0001	0.0031	0.0595
	D11 cache miss rate	0.4183	0.0834	0.0874	0.0798	0.12	0.0209
	UL2 cache miss rate	0.2959	0.1675	0.158	0.2538	0.25	0.0139
	Mean	2.349518537	1.933220036	2.030571963	2.055874485	1.969727431	2.108634142
Int Mean	**3.165336493**	**Float Mean**	**2.980968671**	**Performance (int)**	315.9221783	**Performance (int)**	335.4614255

Conclusion: Whenever a designer increase the clock rate, this often introduces latency to the system. This latency is often acceptable as the increase in the clock rate will provide an overall performance increase. Also, changing the L2 cache Latency has little to no effect on the caches miss rate.

For both interger and floating point benchmarks, set 3 has the best performance