CSE 577 - Homework# 2 Report

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The goal of the improved design is to optimize on the power consumption of the design. The was done by decreasing the amount of states in the design's state machine. Be reducing the number of sequential circuits needed, it was predicted that the overall power consumption would decrease.

As expected, reducing the number of states did indeed decrease the total power consumption. Not surprisingly, this optimization also decrease the total area and timing of the design. The decreased in power was due to the fact that the few combination gates, that replaced the flip flops needed for the additional states, consumed less power. This makes sense since the flip flops are just multiple combination gates combined together. By the same reasoning, this improvement also decreased the total area and timing of the of design.

	Original	Optimized
Total Area	263.188920	255.662470
Slack (MET)	0.17	0.10
Total Power (μW)	14.6083	13.9345

Table 1: Result of optimized design