Homework 3 - Due Febuary 11, 2016

1 Problem Statement

FPGA design flow using Xilinx Vivado tools

2 Tasks

- Go over the tutorial on Vivado (uploaded on ANGEL)
- Using Vivado 2014.4, synthesize provided HDL, run place-and-route and generate a bitstream. Your design should use the maximum possible frequency to drive the counter, while meeting a worst negative slack (WNS) of **atleast** $1ns$. Use **only** one of the four clocks ($100MHz$, $200MHz$, $400MHz$, $600MHz$) provided to you. Report both the maximum frequency and the corresponding WNS obtained.

3 Notes

Steps to launch Vivado *(Assume you have physical/remote access to IST 218)*

- Run the following command on your terminal

  ```
  $ source /home/software/vivado-2014.4/Vivado/2014.4/settings64.csh
  ```

- Check if *vivado* points to the correct version

  ```
  $ which vivado
  ```

- You should see the below path

  ```
  $ /home/software/vivado-2014.4/Vivado/2014.4/bin/vivado
  ```

- Launch Vivado and the GUI should get invoked

  ```
  $ vivado &
  ```