# CSE 577 - Final Project: Phase 1, Part 3

Quang Nguyen, Shenbo Li

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## 1 Objective

The objective for this part of the project is to evaluate the performance and cost of the design from part 1 and 2. Table 1 depicts cost associated with each of the components in the FPGA.

| Component Type | Cost |
|---|---|
| LUT | 2 units |
| Registers | 1 unit |
| BRAM | 8 units |
| DSP | 8 units |

Table 1: Cost table for components of the FPGA

Performance in this design is expressed in term of frame per second (FPS). A single frame is composed of 1920 x 1080 pixels and the design must have a minimum throughput of 30 FPS.

# 2 Results

## 2.1 Reports

The design was synthesized using the Vivado software. The following files are the reports for the power, timing, and utilization for a single fully-pipelined design.

- power.rpt
- timing.rpt
- utilization.rpt

## 2.2 Cost Analysis for Single Fully-Pipelined Design

Cost analysis was perform by using the data from the utilization report and Table 1. Table 2 shows the result of the cost analysis.

Table 2: Cost Analysis on one fully-pipelined design

| Component Type | Cost (units) | # Used | Total Cost (units) |
|---|---|---|---|
| LUT | 2 | 428 | 856 |
| Registers | 1 | 1054 | 1054 |
| BRAM | 8 | 0 | 0 |
| DSP | 8 | 44 | 352 |
| | | | **2262** |

## 2.3 Performance Analysis for Single Fully-Pipelined Design

The design was synthesized using the 600 MHz clock as the clock source. The following data was gathered from the timing report.

- Slack (MET) for max delay paths = 0.190 ns.

- Slack (MET) for min delay paths = 0.107 ns.

At 600 MHz per second, the design will have a throughput of 289.35185 FPS.

## 2.4 Optimization

Based on the data from the utilization report, we can see that that the FPGA have enough resources for us to duplicate our pipelined design several more times. Table 3 shows the resource utilization.

Table 3: Resource utilization for single fully-pipelined design

| Component Type | Utilization % |
|---|---|
| LUT | 0.09 |
| Registers | 0.12 |
| BRAM | 0 |
| DSP | 1.22 |

We know that a single word has has 4 pixels so, at best, we can duplicate our design 4 times and have the design process all 4 of these pixels in parallel. Table 4 shows the cost and performance for duplicating the design.

Table 4: Cost and performance for duplicating the design

| | Cost (units) | Performance (FPS) |
|---|---|---|
| 1 Pipeline | 2262 | 289 |
| 2 Pipeline | 4524 | 579 |
| 3 Pipeline | 6786 | 868 |
| 4 Pipeline | 9048 | 1157 |

We can safely eliminate the option of duplicating the pipeline 3 times since this would cause a misalignment in the data word. This effectively leaves us with 2 options: 2 pipeline or 4 pipeline.

We think it is best to duplicate the pipeline for time since this will allow the design to maximize the utilization of each of the data word that the FPGA is bring in. Table 5 shows our final design decision.

Table 5: Final Design

| | Cost (units) | Performance (FPS) |
|---|---|---|
| 4 Pipeline | 9048 | 1157 |

# 3 Conclusion

After synthesizing our design and looking at the reports that Vivado generated, we have decided that it is reasonable to duplicate our design 4 times to maximize the utilization of each of the data word that the FPGA is bringing in. Table 3 shows that the FPGA has more than enough resources to accommodate this duplication. Table 5 shows the final performance and cost of our design.