CSE 577 – Hw5

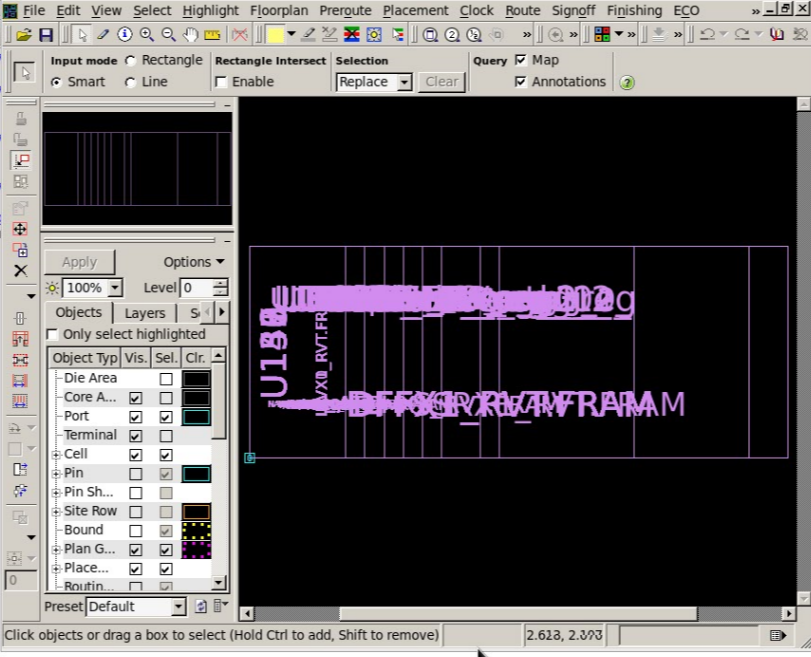
Below are the steps that were taken to complete the project

# Library\_setup

The library\_setup.tcl file was sourced to link all the library to the project.

# Read\_design

The read\_design file was then source to read the synthesized netlist. Once the design was read, the script also setup VDD and VSS for the project.

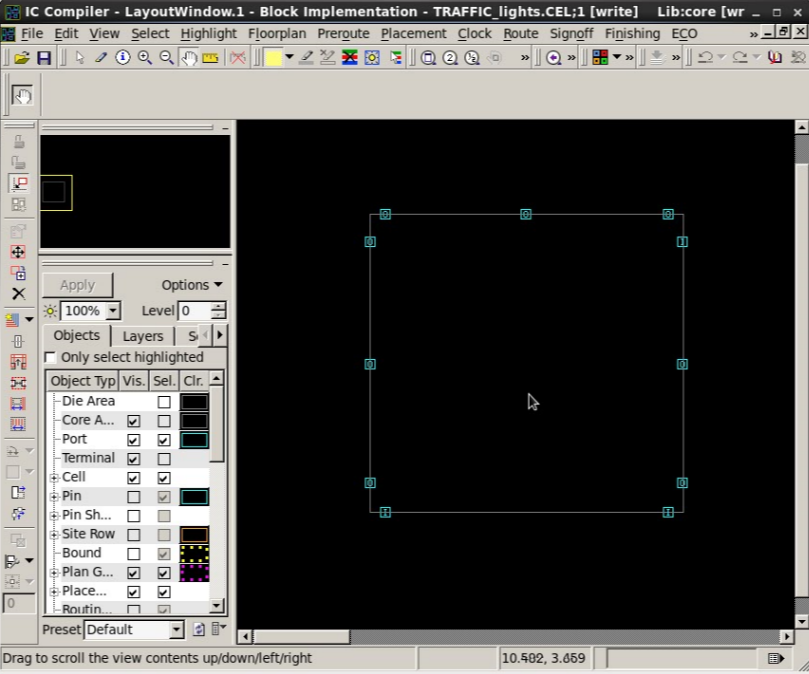


Snapshot of loaded design

# Floorplan1

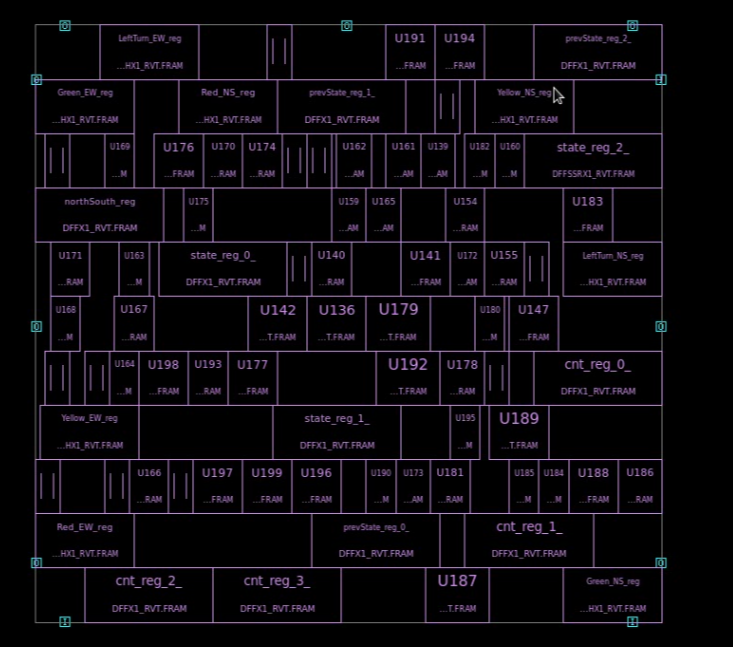
Each line of this script was ran separately. Below were the finding from each of the line.

* create\_floorplan -control\_type aspect\_ratio -core\_utilization 0.63
  + This command creates the size of the core and ensure that the core has a utilization of 1.5
    - Once this command was ran, the cell utilization was set to 66.3565 %. .



Floor plan with inputs and outputs

* Commands to ensure that properties such as cell density and such are kept
  + set\_app\_var physopt\_hard\_keepout\_distance 5
  + set\_route\_zrt\_global\_options -effort low -timing\_driven false -crosstalk\_driven false
  + set\_app\_var placer\_max\_cell\_density\_threshold 0.6
  + set\_app\_var placer\_reduce\_high\_density\_regions true
* create\_fp\_placement -timing\_driven
  + This command places all the components onto the core. Their placement is based on their timing, meaning the shortest distance that the wire have to travel.

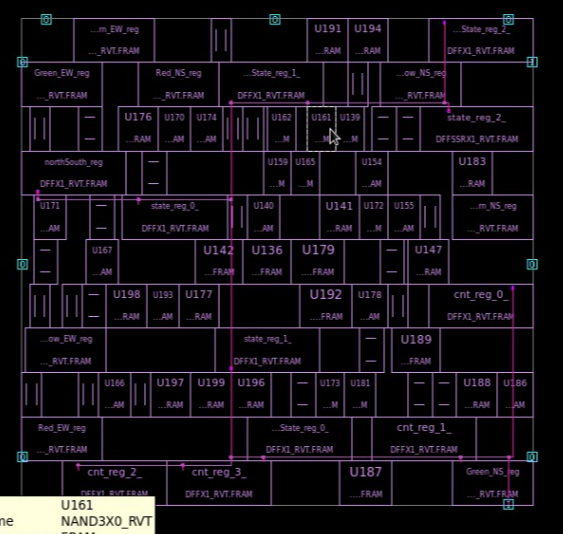


All standard cells are placed inside the core

# Place\_route

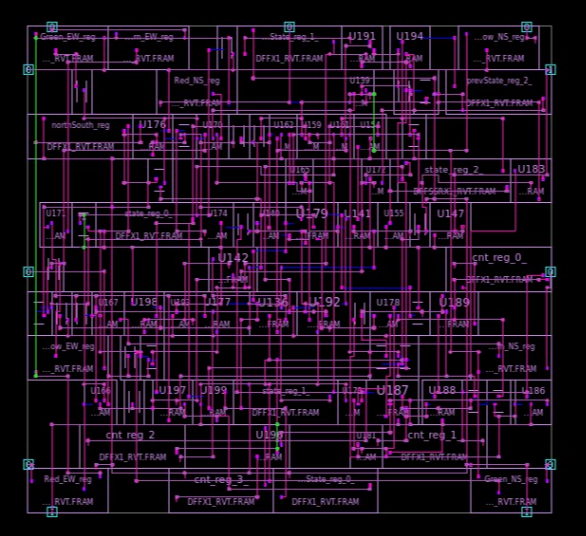
Each line of this script was ran separately. Below were the finding from each of the line.

* source ../inputs/clock\_uncertainity.tcl
  + This command just simply input the uncertainty of our clock
* Psynopt
  + This command performs incremental preroute optimization on the current design.
* Route\_zrt\_group –nets {clk}
  + This command generates the clock routing for the design



Design with clock tree

* route\_opt
  + This command does all the routing and optimization for the design



All signals routed

* source generate\_report.tcl
  + This script just simply output all the reports to their proper files.

# Conclusion

The optimization done in the ICC stage did indeed improve the design. Below is the chart that compares the reports from the synthesis and the ICC stage. It is evident that the design from the ICC stage is better.

|  |  |  |
| --- | --- | --- |
|  | **Synthesis Stage** | **ICC Stage** |
| **Total Area** | 272.705662 | 270.174529 |
| **Total Power** | 12.5001 | 9.6052 |
| **Slack (MET)** | 0.06 | 1.04 |