MENTOR-MENTEE SYSTEM TRAINING GUIDANCE

07 MAY 2018

CONTENTS

1. PURPOSE

- To accelerate improving new engineers' skill systematically

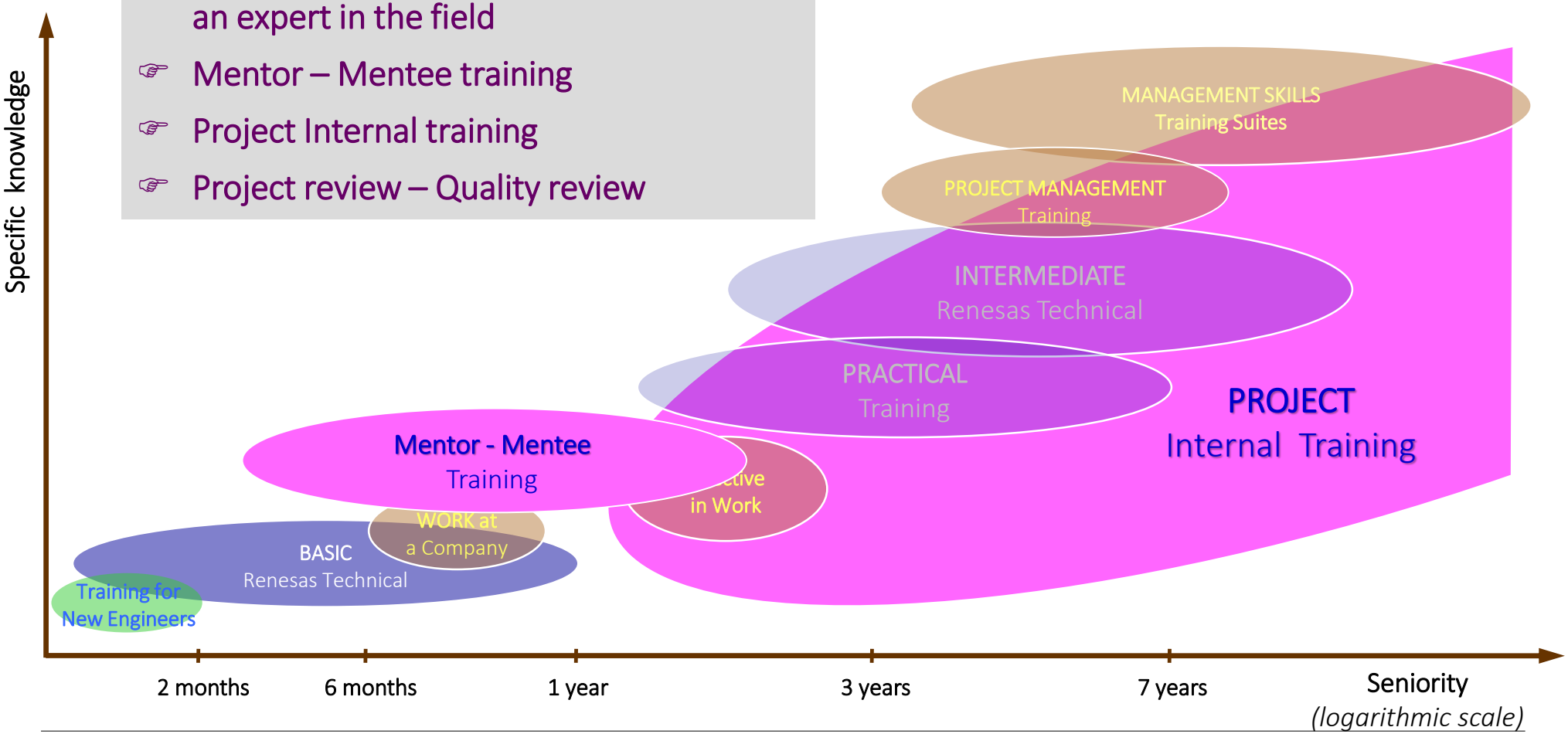
- To develop new engineers in both technical and soft skills.

- To improve mentor's soft skill (finding fact, evaluating, visualizing problems, consensus building, coaching …)

TRAINING SYSTEM AT RVC

Structured On-the-Job Training

- The most important condition to become an expert in the field
- Mentor – Mentee training
- Project Internal training
- Project review – Quality review

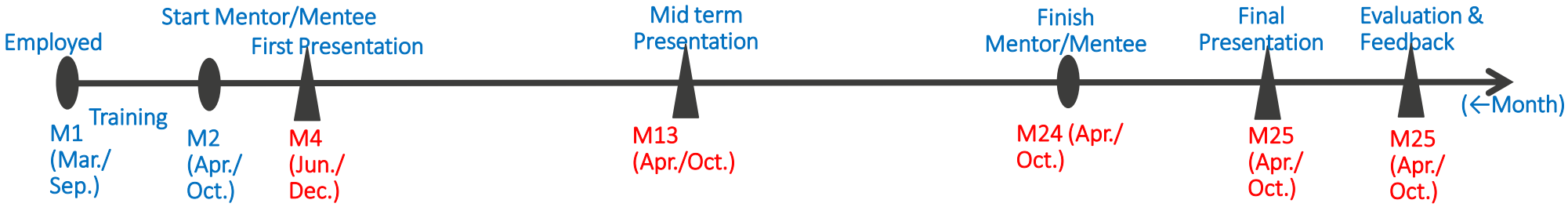


2. ROLE & RESPONSIBILITY

PIC	Role	Responsibility
HR	Organizer	- Organize the plan and follow up MMS for all fresh engineers systematically. - Collect the suggestion and feedback from Mentors and Mentees and Engineering Division to improve this system. - Collect and record the result from MMS for MBO and appraisal and evaluation the improve in quality of engineers. - Evaluate and feedback to managers for improvement
Department/ Section/Group (Senior Manager/ Manager/ Assistant Manager)	Evaluator Host in presentation days	- Define the overall standard and target for each Department/ Section/Group - Approve the MM program - Evaluate the result of MMS on each stage. - Apply result of MMS for MBO/Appraisal - Verify and modify the content of MMS to be suitable with the development of company. - Improve MMS
Mentor	Instructor	- Define target and detail training content for Mentee in line with the overall standard and target of department/section/group - Follow up and coach Mentee during MMS - Report, evaluate the Mentee & program monthly or quarterly to supervisors - Improve MMS
Mentee	PIC	- Discuss with Mentor to define target for MMS - Follow the training plan - Report the result to Mentor monthly or quarterly - Give feedback to improve MMS

3. PLAN SCHEDULE

< Standard Cycle Schedule >



Note:

1. *If Mentee is assigned into new group during MMS, the Group Leader should assign new Mentor and review training program immediately to catch up with new business requirement.*
2. *Mentors should have the high technical skills and good attitude.*

   Mentees cannot be assigned as Mentors if they have not completed their Mentor-Mentee training, except for special cases approved by the company.
3. *In case the Mentor resigns, the Assistant Manager should assign new Mentor immediately to ensure the quality of MMS and the current Mentor has to transfer all information of MMS to the new Mentor before last working day.*
4. *If Mentee has submitted resignation letter, the MMS will be closed automatically*

PRESENTATION SCHEDULE

1. First Presentation (at 4th month from joining RVC)

   (1) After group assignment, Eng. Div. decides assignment of Mentors and communicate overall standard and target for each Department/Section/Group to Mentors.

   (2) HR announces presentation schedule to related persons (Assistant Managers and above and Mentors, Mentees) and gives guidance to Mentor, Mentee.

   (3) Mentor & Mentee decide target and training program in line with overall standard and target for the Department/Section/Group, make presentation and upload to DMS as HR guidance.

   (4) Mentee gives presentation.

   (5) Assistant Manager and above gives feedback to Mentor and Mentee.

2. Mid term Presentation (before 13th month from joining RVC)

   (1) HR announces presentation schedule to related persons.

   (2) Mentee makes presentation and upload to DMS as HR guidance

   (3) Assistant Manager evaluates performance of Mentor and Mentee for Manager to review and send to HR before the presentation.

   (4) Mentee gives presentation and Mentor gives comments.

   (5) Assistant Manager and above gives feedback to Mentor and Mentee.

3. Final Presentation (before 25th month from joining RVC)

   (1) HR announces presentation schedule to related persons.

   (2) Mentee makes presentation and upload to DMS as HR guidance

   (3) Assistant Manager evaluates performance of Mentor and Mentee for Manager to review and send to HR before the presentation.

   (4) Mentee gives presentation and Mentor gives comments.

   (5) Assistant Manager and above gives feedback to Mentor and Mentee.

(Note: Standard duration is 10 min. for presentation and 5 min. for Q&A. However, it can be altered depending on number of Mentees.)

PRESENTATION REQUIREMENT

1. First Presentation (at 4th month from joining RVC)

- Set target and estimate achievement in advance
- Make plan both PJ and training schedule
- Analyze difficulties and solutions

2. Mid term Presentation (before 13th month from joining RVC)

- Report the result compare with original target
- Activities and achievement
- Next plan
- Difficulties and solutions if any
- Feedback for improvement if any

3. Final Presentation (before 25th month from joining RVC)

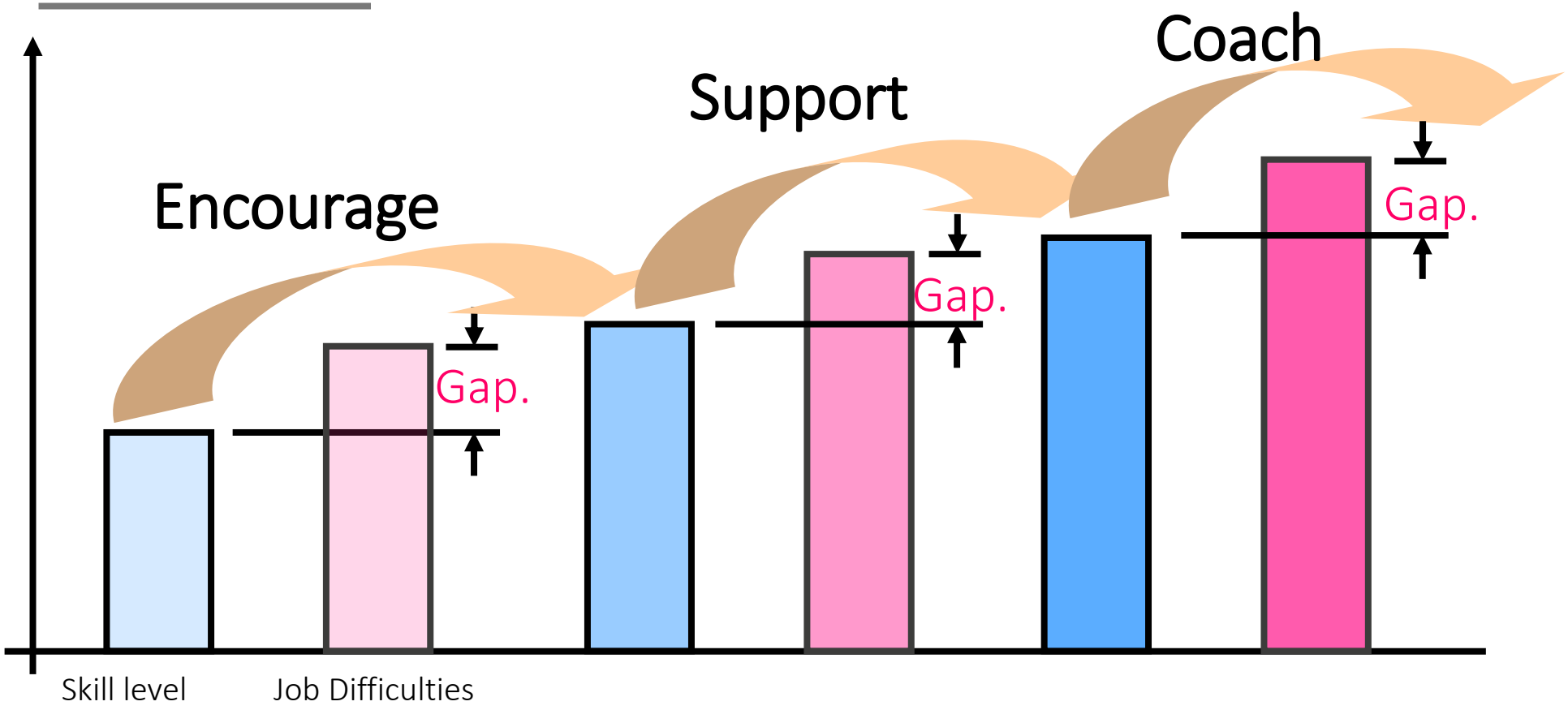
- Report MM target and result
- Activities and achievement
- Difficulties and solutions
- Feedback for improvement if any
- Next plan after MMS

PRESENTATION PROCEDURE

In a mentor-mentee presentation meeting:

- Host: Assistant Manager and above
- Time for presenting: 15 minutes per person including presenting and QA.
- Mentor needs to give the comment (from 30 seconds to 1 minute) about target of Mentee.
- Assistant Manager and above give feedback to Mentor and Mentee

4. Training Cycle



- Overcoming this gap makes engineers more capable, skillful and productive.

Training Cycle

Job Assignment

proper job to your mentee
with appropriate difficulties.

Higher job Assignment

to your mentee with more difficulties.

Encourage, Support and Coach

your mentee to achieve the task.

Evaluate, Analyze and Recognize

your mentee's achievement
and capability.

Only the high level job assignment
makes engineers be skillful.

Require and Gain

Phase	Requirement	Need to do	You can gain
<Planning Phase> Job assignment	• With proper difficulties. • "Proper" means that mentee can overcome within PJ schedule with your coaching.	• To find facts (mentee's level, job level) • To manage both PJ and training schedule. • To set target and estimate achievement in advance.	• Finding fact • Schedule management • Making accurate estimation • Sharing target
<Doing Phase> Encourage, Support, Coach, Suggest	• A piece of instructive advice. • Don't give solutions. • Give the chance of "aha!-moment"	• Let mentee think about and find solutions by himself, at least let him propose options. • To point out and reinforce his weak-point.	• Effective coaching • Visualizing problems
<Checking Phase> Evaluate mentee's ability	• Fair and accurate evaluation based on achievement. • Proper feed back	• To find facts and compare estimation (expectation) and result (improvement).	• Evaluating • Giving feed back logically
<Action Phase> Higher job assignment	• With proper difficulties. • "Proper" means "more challenging" than before.	• To explain evaluation result and make next plan on common ground with mentee. • To build consensus with mentee.	• Making common ground • Building consensus • Accountability

DEFINITION OF TARGETED ENGINEER BY ENGINEERING DIVISION

Experience	Over all Image of Character	Technical Ability	Management Ability	Communication Ability	TOEIC
1 Year Later	Can do basic work under supervisor's instruction	It should be defined by Department as following pages	Can keep assigned schedule	Can report his problem to supervisor	-
2 Year Later	Can do feedback by looking at result of work		Can keep schedule and raise alarm if necessary	Can report work status in his team	-
3 Year Later	Can instruct younger engineers in his responsible segment		Can estimate schedule, and can make action to keep schedule	Can report problem in group, and can negotiate with group member	650

Expected Level of engineers

FRONTEND

2-Year old engineers are expected to obtain skills below at level where he/she can complete task without help.

Category	Frontend Design	
	Functional Design	Functional Verification
Execution of Design & Verification	to create RTL level functional description and module connection with HDL	to list verification items based on product specifications and chip specifications
	to describe timing constraints for chip and/or module levels	to create test patterns covering verification items using HDL and assertions
	to check RTL description using RTL checker and modify if errors are found	to conduct verification by using logic simulator with test patterns, judge results and modify input data if necessary
	to conduct synthesis with associated tool and retry synthesis with alteration of synthesis options and/or modification of RTL/SDC to meet specified criteria	to conduct verification coverage collection
Evaluation of Design & Verification result	to check assignment proceeds as scheduled	to check assignment proceeds as scheduled
	to check design met given specification and modify it if necessary	to judge verification items are covered by test cases and evaluate coverage result
	to summarize design information and constraints and provide them to DFT and layout designer	to summarize verification results and report

Remarks : Individual targeted skill should be defined by Mentor/Mentee and MBO

RENESAS

Expected Level of engineers

BACKEND

2-Year old engineers are expected to obtain skills below at level where he/she can complete task without help.

Category	Backend Design	
	Layout Design & STA	DFT
Execution of Design & Verification	to create floor-plan considering signal timing, chip size, wiring density, power constraints and hard-macro constraints	to insert Mux SCAN chain, logic BIST, memory BIST, boundary and IDDQ test scan into netlist with associated tool
	to perform PPA (Performance/Power/Area) optimization as to specification.	to check logic equivalence between before and after of DFT insertion with associated tool and provide feedback if necessary
	to create chip layout based including power/ground network, CTS, Place & Route, considering timing, area, leakage, wiring congestion, … as specification	to create test patterns for SCAN and functional tests with associated tool and provide feedback if failure detection rate does not meet criteria
	to carry out signal routing improvement according to satisfy the timing and physical verification rules	to create patterns for defective memory replacement and conduct verifying memory rescue patterns
	To design Timing constraint for DFT circuit To perform accuracy check of timing constraint. To do timing closure	To insert Test point to achieve Functional safety coverage. To design and apply test policy to achieve test time, chipsize, power consumption.
Evaluation of Design & Verification result	to check assignment progress as scheduled	to check assignment proceeds as scheduled
	to verify if the chip-implementation follow to the guidelines and specifications	to verify design and tests are met to test strategy of product
	to summarize layout results and report	to summarize DFT results and report

Remarks : Individual targeted skill should be defined by Mentor/Mentee and MBO

RENESAS

Expected Level of engineers

Software

MINIMUM SKILL/ROLE (TWO YEARS LATER)

Skill Role	Verification/Failure analysis	Programming	MCU architecture	Operating System	Development Process	QC in software	Project Management
Software design engineer (Function/Detail spec) role level 2	Can do feedback by looking at result of work	Can do feedback by looking at result of work	Can understand architecture of objective MCU of assigned product	Can understand objective OS of assigned product	Can do feedback by looking at result of work	Can do basic work under supervisor's instruction	Can do basic work under supervisor's instruction
Coding engineer (Software) role level 2	Can do feedback by looking at result of work	Can do feedback by looking at result of work	Can understand architecture of objective MCU of assigned product	Can understand objective OS of assigned product	Can do feedback by looking at result of work	–	–
Verification/ System testing engineer role level 2	Can do feedback by looking at result of work	–	Can understand architecture of objective MCU of assigned product	Can understand objective OS of assigned product	Can do feedback by looking at result of work	–	–

Remarks : Individual targeted skill should be defined by Mentor/Mentee and MBO

5. EVALUATION METHOD

< Evaluation Format >

- Assistant manager evaluates and Manager examines the result.
- Evaluation point is described in the same way as appraisal (5 = Top <-> 1= Bottom: by absolute evaluation, not relative evaluation)

Role		Evaluation item	Criteria to evaluate
Mentee	A	Technical skill	Acquired designated technical skill, knowledge required by the standard definition of mentee to perform the expected job level.
	B	Communication ability and team work	Acquired proper communication skill to report to supervisor for feed back and alarm for problem solving, and have team work attitude for cooperation with colleagues.
	C	Motivation	Maintained high motivation with commitment to achieve mission and keen enthusiasm for challenging spirit for better result.
	D	Customer satisfaction	Maintained attitude to mind customer satisfaction and improvement of quality of work and productivity
	E	Education and Training	Attended designated training curriculum and performed qualification in result of training to obtain knowledge.
Mentor	A	Communication	Maintained enough frequent opportunity of contact and monitored situation of mentee's progress regularly and carefully.
	B	Coaching	Whether listened sincerely issues of mentee and provided proper suggestion timely to let him discover solution by himself.
	C	Technical development	Whether provide enough and timely technical advice and monitor progress of mentee's technical improvement.

EVALUATION FORM

MENTEE																MENTOR									
No.	Code	FN	GN	Department	Group	Evaluation (5: Top -> 1: Bottom)							Email	MMS schedule			Code	FN	GN	Group	Evaluation (5: Top -> 1: Bottom)				
						A	B	C	D	E	Overall	Comments		Date	Time	Venue					A	B	C	Overall	Comments

RENESAS DESIGN VIETNAM

GUIDELINE OF TARGET SKILL LEVEL

For Frontend Design 1 Department (FED1)

Skill item		Level	
Functional design		2.7	Average
	To create functional/logic specifications for chip design	2	
	To create module design specifications	3	
	To create LSI functional description at behavior level	3	
	To create RTL description	3	
	To create top level netlist	3	
	To create timing budget	3	
	To determine strategies of evaluation and testing	2	
Functional verification		2.8	Average
	To determine verification strategy (verification policy)	2	
	To check specification	3	
	To create verification item list (checklist)	3	
	To create test patterns for functional verification	3	
	To conduct functional verification of RTL	3	
	To evaluate functional verification result	3	
Logic design		2.7	Average
	To conduct logic synthesis, optimize netlist and do formal verif	3	
	To determine checker strategy	2	
	To analyze and fix checker error (HLDRC, DFTcheck)	3	
	To analyze and fix checker error (STAcheck)	3	
	To create SDC (Synopsys Design Constraint)	2	
	To analyze timing report and optimize timing	3	

GUIDELINE OF TARGET SKILL LEVEL

For Frontend Design 2 Department (FED2)

Skill item		Level
Functional verification (Main role)		2.5
	Determine verification strategy	2
	Check specification	2
	Create verification item list (checklist)	2
	Create test patterns for functional verification	3
	Conduct functional verification of RTL	3
	Evaluate functional verification result	3
Functional design (Sub-role)		2
	Create module design specifications	2
	Create LSI RTL description	2
	Create top level netlist	2
	Create timing budget	2

GUIDELINE OF TARGET SKILL LEVEL
FOR BACKEND SECTION

Skill			1st year	2nd year	Note
Main skill	PnR IP full flow	Synthesis, DCG	1	2	At least level 2
		Placement	2	3	
		CTS	2	3	
		PostCTS	2	3	
		Routing & postRoute	2	3	
		Static Timing Analysis	2	3	At least level 2
		Physical Verification	2	3	At least level 2
Soft skill	Scripting (Csh, awk, tcl, Perl, …)		2	3	
	Documentation		2	3	
	Communication		2	3	
	English TOEIC		550+	650+	Not mandatory
	Training new members		1	2	

GUIDELINE OF TARGET SKILL LEVEL

FOR MIDDLEEND (DFT)

ME standard skill target

Created by: TrucNguyen

Revision: 2015 Jul/29

Standard skill map for DFT engineer

			Target for Mentor-Mentee				
			1-year		2-year		
No.	Field	Skill	MB Eng	SCAN Eng	MB Eng	SCAN Eng	Note
1	BSD	Can do BSD insertion				2	Can choose BSD or SDC
2		Can do BSD verification & make tester pattern				2	
3	MBIST	Can do MBIST insertion	2		3		
4		Can do MBIST verification	2		3		
5		Can make MBIST tester pattern	2		3		
6		Can make special pattern (AC-merge, FBM,...)	2		3		
7		Can ROMBIST insertion & verification (for flash memory)	2		3		
8		Can do RAM grouping considering routing, timing, power, test-time.	2		3		
9		Do & optimize fusebit assignment to get best RAM-repair efficiency	2		3		
10	SCAN	Can do SCAN/LBIST insertion		2		3	
11		Can do DFT/SCAN grouping considering routing, timing, power, test-time.		2		3	
12		Can do SCAN/LBIST verification & make tester pattern		2		3	
13		Can analyze coverage result & give solution to improve it (such as: TPI analysis & decide TPI insertion configuration)		2		3	
14		Can generate IDDQ pattern (bridge fault, stuck at fault) & obtain coverage		2		3	
15		Can obtain toggle rate of Burn-in pattern.		2		3	
16		Can generate path-delay pattern (to check critical path)		2		3	
17	SDC	Make DFT mode SDC			2		Can choose BSD or SDC
18		Can make judgement for timing path in DFT mode			2		
19		Can do accuracy check (GCA, warning, Error judgement)			2		
20	General	Can make DFT strategy (method, flow, circuit structure, circuit configuration,...) considering test time, test cost, area overhead, and routing/timing effect based on design feature & direction.			2	2	
21		Can make DFT clean netlist (if necessary)	2	2	2	2	
22		Can do Test-cost estimation & test-cost calculation.				2	
23		Can do Formal verification (build env, check result, failure debug)	2	2	2	2	
24		Can do Synthesis considering power, area, timing.	2	2	2	2	
25		Can do SDF simulation			2	2	
	Prj/Task Management	Can keep assigned schedule, and rise alarm if necessary	2	2	3	3	
26		Can make project plan (scope, target, schedule, input-output, resource)					
27		Can define input/output criteria for each design phase	2	2	2	2	
28		Can do risk assessment(identify the risk & make countermeasure, ex. method: DRBFM,...)		2	2	2	
29		Can monitor & control project work	2	2	2	2	
30		Can follow design procedure (make/apply checklist, do review, get approve before releasing) to guarantee output quality	2	2	3	3	
31		Can make detail project schedule, including discuss schedule with related groups					
32		Can do project Lesson Learn & PDCA	2	2	2	2	
33	Others	Can check wire congestion (using Amateras)	2	2	3	3	
34		Can make plan to proceed the task (what to do, target, milestone, how to do)	2	2	2	2	
35		Can make the report (prj report, weekly report,...)	2	2	3	3	
36		Can make the document	2	2	3	3	
37		Can do QC issue analysis (include PDCA)	2	2	2	2	
38		Can use scripting lanquage (TCL, SCH, PERL, AWK, SED,...)	2	2	3	3	

GUIDELINE OF TARGET SKILL LEVEL
FOR MIDDLEEND (STA)

ME standard skill target

Created by: TrucNguyen
Revision: 2015 Jul/15

Standard skill map for STA engineer

			Target for Mentor-Mentee		
No.	Field	Skill	1-year	2-year	Note
1	Technical	Build & control STA env	2	2	
2		Do timing analysis (identify problem, make countermeasure)	2	2	
3		Make DFT mode SDC (from spec)			One of USER or DFT SDC is OK.
4		Make User mode SDC (from spec + individual constraints)		2	
5		Do timing closure (setup & hold)	2	3	
6		Conduct Kobetsu/AC timing check & closure	2	2	
7		Contact SDC accuracy check (GCA, warning, Error)	2	3	
8	Prj/Task Management	Can keep assigned schedule, and rise alarm if necessary	2	3	
		Can make project plan (scope, target, schedule, input-output, resource)			
9		Can define input/output criteria for each design phase	2	2	
10		Can do risk assessment(identify the risk & make countermeasure, ex. method: DRBFM,…)		2	
11		Can monitor & control project work	2	2	
12		Can follow design procedure (make/apply checklist, do review, get approve before releasing) to guarantee output quality	2	3	
13		Can make detail project schedule, including discuss schedule with related groups			
14		Can do project Lesson Learn & PDCA	2	2	
15	Others	Can make plan to proceed the task (what to do, target, milestone, how to do)	2	3	
16		Can make the report (prj report, weekly report,…)	2	2	
17		Can make the document	2	3	
18		Can do QC issue analysis (include PDCA)	2	3	
19		Can use scripting lanquage (TCL, SCH, PERL, AWK, SED,…)	2	2	

GUIDELINE OF TARGET SKILL LEVEL
FOR MCU SOFTWARE SOLUTION

Role ID	Role name	Skill group ID	Skill group	Skill ID	Skill name	Skill detail explanation	Keyword	Input	Output	Tool
R140	Engineer for software design (functional and detailed design)									
R140		G505	Software architecture design	S01944	Design software architecture	Decide the structure of software according to given software requirement definitions.		Software basic specification	Functional specification	
R140		G506	Software detailed design	S01945	Make a detailed software design	Conduct a detailed software design according to given software structure definitions.		Functional specification	Detailed specification	
R141	Coding engineer (software)									
R141		G507	Software coding	S01946	Perform software coding	1. Have sufficient knowledge of programming languages and create a program based on the detailed design document. 2. Conduct a code review of created code.		Detailed specifications, coding rules, etc.	Source code	Coding guide
R141		G508	Development environment	S01947	Have knowledge of the development environment and create code	Have knowledge of the development environment (compiler, debugger) and target environment (OS, middleware, applications, etc.) and create source code with these environments in mind.		Development environment, tool specifications	Source code	
R141		G509	Readability	S01948	Make an easy-to-read code	Have knowledge of the techniques for improving the source code readability and perform coding		Coding guide	Source code	Coding guide
R141		G510	Software development methodology	S01949	Make structured analysis/design and object-oriented design	Make structured analysis/design (programming) and object-oriented design (programming) as an application of the software development methodology.		Programming technology books	Source code	
R142	Engineer for test/system validation (software)									
R142		G511	Test item extraction	S01950	Extract test items	1. Extract test items from various specifications and design specifications. 2. Round up and integrate the extracted test items into test specifications.		Basic specification, functional specification, detailed specification	Test specification	
R142		G512	Testing	S01951	Conduct tests and round up the results	1. Conduct tests according to the test specifications. 2. Round up the results of the tests and make a report.		Test specification	Bug report, Fault report, test result summary table	
R142		G513	Failure analysis	S01952	Failure analysis	1. Locate the cause of any trouble and make analysis of its influences and other side effects. 2. Take countermeasures against similar problems.		Bug report, test result summary table	Failure-analysis report	
R142		G514	Test environment construction	S01953	Have knowledge of the development environment and conduct tests and evaluations	Have knowledge of the development environment (compiler, debugger) and target environment (OS, middleware, applications, etc.) and conduct tests and evaluations.		Development environment, tool specification	Bug report, Fault report, test result summary table	
R142		G515	Validity verification	S01954	Validity verification	Create system verification specifications from the use cases as viewed from the user application side and from the view point of uses such as high load environment, and conduct tests.		Requests by customers, basic specification	Bug report, Fault report, test result summary table	

GUIDELINE OF TARGET SKILL LEVEL
FOR SOC SOFTWARE SOLUTION

Details of technical requirements

Main role	Expected role level	Skills	Expected skill level
Engineer for SW design	2	Software architecture design	2
		Software detailed design	2
Coding engineer	2	Software coding	2
		Development environment	2
		Readability	2
		Software development methodology	2
Engineer for test/system verification	2	Test item extraction	2
		Testing	3
		Failure analysis	2
		Test environment construction	3
		Validity verification	N/A

THANK YOU!