Bài Thi Cuối Kỳ Môn Kiến Trúc Máy Tính và Hợp Ngữ

Kiến trúc máy tính _ hợp ngữ (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

Thi Online KTMT&HN nhóm lẻ

Started on	Friday, 31 May 2019, 1:11 PM
State	Finished
Completed on	Friday, 31 May 2019, 2:21 PM
Time taken	1 hour 9 mins

Question 1
Complete
Marked out of 0.50

In multiplication instruction, the upper half of the result is nonzero implies which state of Carry flag and Overflow flag?

Select one or more:

- [ ] OF=1
- [ ] CF=1
- [x] OF=0
- [x] CF=0

Question 2
Complete
Marked out of 1.00

Which is correct about dual-layer DVD?

Select one:

- ( ) the same as double-sided DVD
- ( ) contains layers on both sides of the disk for writing data to
- (•) contains two layers on a single side for writing data to
- ( ) DVD drives has double laser head for reading from or writing to this disk

Question 3
Complete
Marked out of 1.00

For better speed, in CPU design, engineers make use of the following techniques:

Select one or more:

- [x] Pipelining
- [x] Branch prediction
- [ ] Faster CPU internal bus
- [x] Speculative execution

Question 4

Complete

Marked out of 1.00

Consider the following assembly instruction sequence

```
        XOR BX, BX
        CMP DL, 5
        JLE   a_label
        CMP DL,17h
        JGE  a_label
        MOV BX, 10h
a_label:
        INC BX
```

watch point:

...

Choose correct value of BX register at watch point for different value of DL?

DL=0Ah 01h

DL=0FFh 11h

DL=10 01h

DL=17h 11h

Question 5

Complete

Marked out of 1.00

Consider a 16-bit microprocessor, with a 16-bit external data bus, driven by an 10-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain?

Select one:

- 4 MB/s
- 1 MB/s
- 5 MB/s
- 10 MB/s

Question 6

Complete

Marked out of 1.00

Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system:

rotational delay: time for the sector in the request track to reach the head

seek time: time for the head to settle at the request track

access time: access time + settle time

Question 7

Complete

Marked out of 0.50

Which are the correct actions for LODSW string operation if DF is reset (=0)

Select one or more:

- decrease DI by 2
- Load 16-bit value at memory location pointed by ES:[DI] into AX
- Load 16-bit value at memory location pointed by DS:[SI] into AX
- increase SI by 2

Question 8

Complete

Marked out of 1.00

In computer organization, the CPU transfer rate is much higher than that of memory. It is easy to match performance of these components by:

Select one:

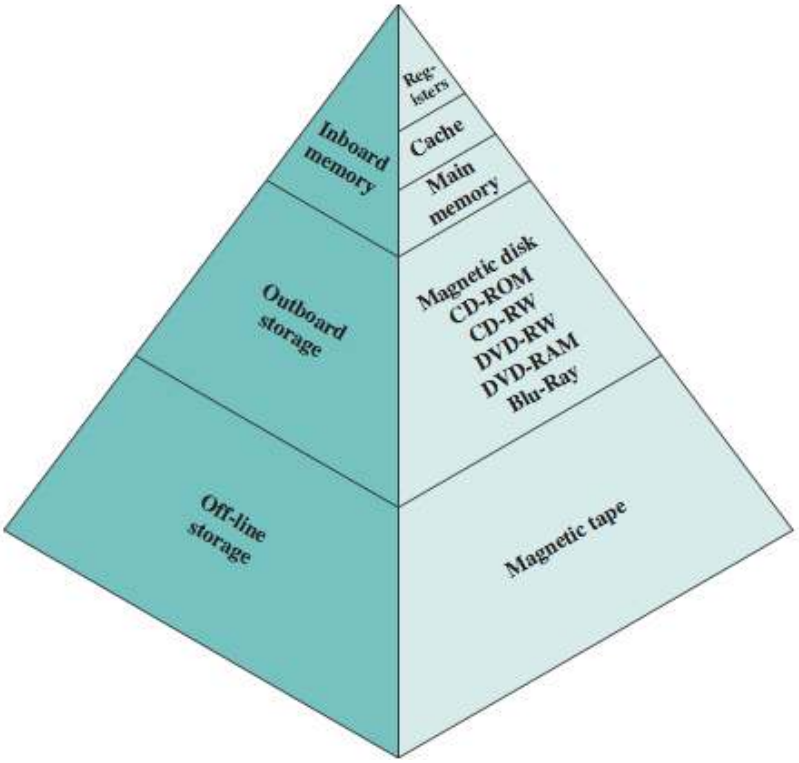
- increase the bus speed
- producing faster memory module
- Introducing cache memory
- increase I/O speed

Question 9

Complete

Marked out of 1.00

For memory hierarchy below, which relationship hold when moving downward



Select one or more:

- Decreasing cost per bit
- the processor accesses more often
- Increasing access time
- Decreasing frequency of access by the processor
- Increasing capacity

Question 10

Complete

Marked out of 0.50

Which of the following instructions are not valid?

Select one or more:

- MOV DS, B800h
- MOV AX, SI
- MOV AX, [BP+2]
- MOV SP, SS:[SI+2]

Question 11
Complete
Marked out of 0.50

Sign-extend number 1011 0101 (8-bit binary) to 16-bit

Answer: 1111 1111 1011 0101

Question 12
Complete
Marked out of 1.00

The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left

Temporal locality — the tendency for a processor to access memory locations that have been used recently

Spatial locality — the tendency of execution to involve a number of memory locations that are clustered

tendency to use large cache and prefetch mechanism

Question 13
Complete
Marked out of 1.00

Which ones are not correct for static RAM?

Select one or more:

- [x] faster than dynamic RAM because they are made from capacitor
- [ ] Cheaper than dynamic RAM because simpler chip controller
- [x] Cost per bit is higher than dynamic RAM
- [ ] Cost per bit is lower than dynamic RAM

Question 14
Complete
Marked out of 1.00

Which of the following instructions are not legal addressing?

Select one or more:

- [ ] MOV AX, [DI]
- [ ] MOV CX, [SI]
- [x] MOV AX, [BX+SP]
- [x] MOV AX, [SP+1]

Question 15
Complete
Marked out of 1.00

Structural components of computer include:

Select one or more:

- [x] I/O
- [ ] DMA
- [x] System interconnection
- [ ] Interrupt
- [x] Central processing unit
- [x] Memory

Question 16
Complete
Marked out of 1.00

A memory chip has 12 address pins, determine the maximum memory words of this chip?

Select one:
- 4096
- 2048
- 2048K
- 4000

Question 17
Complete
Marked out of 1.00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity

Answer: 262144 KB

Question 18
Complete
Marked out of 1.00

Choose correct features for SRAM and DRAM

SRAM: Faster access time, cost more per bit, smaller size

DRAM: Slower access time, cheaper cost per bit, can manufacture with larger size

Question 19
Complete
Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

```
MOV AX,0020
MOV CX,0010
MUL  CL
```

watch point:

DX: 0000

AX = 0200

CX = 0010

Question 20
Complete
Marked out of 1.00

Which statements are correct for HDDs?

Select one or more:
- a. Bits are store randomly on disk surfaces
- b. Head, Track, Cylinder are key parameters for access data on hard disk
- c. Bits are stored on tracks
- d. Head, Track, Sector are key parameters for access data on hard disk

Question 21

Complete

Marked out of 0.50

Which are the correct inputs for XLAT instruction

Select one or more:

- [ ] look-up index must be loaded into DL
- [ ] DS:[BX] pointed to look-up table
- [x] look-up index must be loaded into AL
- [ ] DS:[SI] pointed to look-up table

Question 22

Complete

Marked out of 1.00

What is the correct value of SI, AL (in hex) at watch point:

```
01:             MOV SI, 300h
02:             MOV AL, 10h
03:             MOV CX, 7
04: Loop_label:
05:             MOV [SI], AL
06:             ADD AL,10h
07:             INC  SI
08:             LOOP Loop_label
```

watch point:

SI 307h

AL = 80h

Question 23

Complete

Marked out of 1.00

To evaluate processor performance, the following indicators and formulas are used:

Cycles per instruction $$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Time to execute a program $$T = I_c \times CPI \times \tau$$

Or $$T = I_c \times [p + (m \times k)] \times \tau$$

In which:
p: the number of processor cycles needed to decode and execute the instruction
m: the number of memory references needed
k: the ratio between memory cycle time and processor cycle time
τ: cycle time = *1/f*

Which of the following system attributes affects cycle time τ

Select one or more:

- [x] Instruction set architecture
- [x] Cache and memory hierarchy
- [ ] Compiler technology
- [ ] Processor implementation

Question 24
Complete
Marked out of 0.50

To encrypt a byte value, use _____ instruction.

Select one:
- XOR
- AND
- NOT
- OR

Question 25
Complete
Marked out of 0.50

In multiplication instruction, when the source operand is 8 bit, _____ will be multiplied with source.

Select one:
- AX
- AL
- Whatever general purpose register
- BX

Question 26
Complete
Marked out of 1.50

A system programmer needs to compute 449/2+358/4 (decimal). Instruct him to code in debug (number must be in hex) with the least number of instruction counts.

Step 1: MOV AX,166
Step 2: MOV CL,2
Step 3: SHR AX,CL
Step 4: MOV BX,AX
Step 5: MOV AX,01BC
Step 6: ADD AX,BX

Question 27
Complete
Marked out of 1.00

Convert 0.1015625 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa)

Answer: 3DD00000

Question 28
Complete
Marked out of 0.50

The instruction that loads the AH register with the lower byte of the flag register is

Select one:
- LAHF
- PUSHF
- AH
- SAHF

Question 29
Complete
Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL, 0F
ADD AL, F1

watch point:

Zero flag (OF) = set

Carry flag (CF) = set

Question 30
Complete
Marked out of 1.50

Which are correct about 32 bit index registers of IA-32 processors:

Select one or more:

- [x] ESI: 32 bit pointer to source memory in data movement instructions
- [ ] ESH,EDH: 16 bit pointers to higher memory above 1M
- [x] SI: 16 bit pointer to source memory in data movement instructions
- [x] EDI: 32 bit pointer to destination memory in data movement instructions
- [x] DI: 16 bit pointer to destination memory in data movement instructions

Question 31
Complete
Marked out of 1.00

Select the correct sequence of instructions to compute -1024/128 (all values are in hex).

Step 1: MOV AX,FC00

Step 2: MOV CX,80

Step 3: CWD

Step 4: IDIV CX

Question 32
Complete
Marked out of 1.50

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate MIPS rate for this program

Given:

$$\text{MIPS rate} = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Answer: 25.80645161

Question 33
Complete
Marked out of 1.20

What is the correct sequence of instruction cycle?

Step 6 Store result
Step 4 Fetch operand
Step 1 Execution
Step 5 Calculate operand address
Step 2 Fetch opcode
Step 3 Decode

Question 34
Complete
Marked out of 1.00

Convert the 32-bit floating point number C4361000 (in hex) to decimal.

Answer: -728.25

Question 35
Complete
Marked out of 0.50

Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit).

Answer: E9

Question 36
Complete
Marked out of 0.50

8088 is 16 bit processor, the maximum addressable memory is:

Select one:
- 640M
- 640K
- 1024K
- 64M

Question 37
Complete
Marked out of 0.50

Write mask byte (in hex) to set bit 6th, 4th of a byte value with OR instruction (LSB is the 1st bit).

Answer: 28

Question 38
Complete
Marked out of 0.50

the instruction, CMP to compare source and destination operands by _____

Select one:
- subtracting
- adding
- dividing
- comparing

Question 39

Complete

Marked out of 1.00

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate the execution time for this program.

Given:

$$T = I_c \times CPI \times \tau$$

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Answer: 0.003875

Question 40

Complete

Marked out of 1.00

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction **MOV AX, [1D4B]** executed

Answer: 5A2D

Question 41

Complete

Marked out of 1.00

Select correct level for contemporary computer multilevel machine

Level 3: Operating system level

Level 5: High level programming language

Level 6: Applications

Level 1: Microarchitecture level

Layer 4: Assembly Language level

Level 2: Instruction set level

Level 0: Digital logic level

Question 42

Complete

Marked out of 1.00

the memory stack area of a program shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of **PUSH SI**

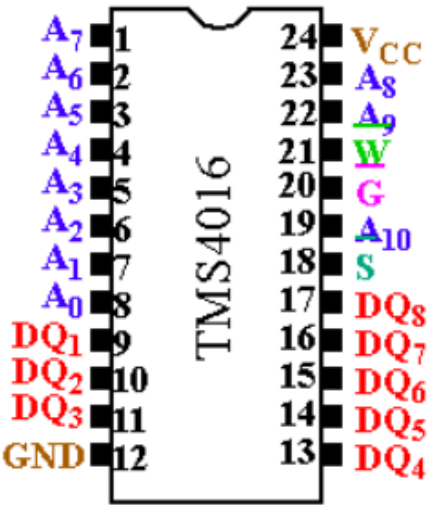
Answer: 1D48

Question 43

Complete

Marked out of 1.00

Choose the correct structure of memory chip as shown below



Note:

DQ: Data pinout

Select one:

- DRAM 2Kx8-bit
- SRAM 1Kx16-bit
- SRAM 2Kx8-bit
- DRAM 1Kx16-bit

Question 44

Complete

Marked out of 1.00

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number 68 (in hex) to decimal.

Answer: 12.0

Question 45

Complete

Marked out of 2.00

Choose correct RAID volume definitions for a request 2T storage.

RAID 0 - Striped volume	2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails
RAID5 Volume	At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time
RAID 1 - Mirror volume	2 x 2T HDDs are needed, no data lost when the primary storage fails
Spanned Volume	2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails

◄ Announcements

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Thi Kiến Trúc Máy Tính và Hợp Ngữ

Computer Architecture and Assembly language (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

THI Kiến trúc máy tính và hợp ngữ (lớp CHẴN)

Started on	Monday, 30 December 2019, 1:10 PM
State	Finished
Completed on	Monday, 30 December 2019, 2:20 PM
Time taken	1 hour 10 mins

Question 1

Complete

Marked out of 1.00

Which ones are not correct for static RAM?

Select one or more:

- [x] Cheaper than dynamic RAM because simpler chip controller
- [x] Cost per bit is higher than dynamic RAM
- [ ] Cost per bit is lower than dynamic RAM
- [x] faster than dynamic RAM because they are made from capacitor

Question 2

Complete

Marked out of 1.00

Match the correct definition of flag bits in PSW.

indicates the result of an arithmetic or comparison operation	CF
contains the carry from bit 3 to bit 4 following an arithmetic operation	AF
indicates the overflow of leftmost bit of data after an arithmetic operation	OF
shows the sign of the result of an arithmetic operation	SF

Question 3

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

```
MOV AX,0020
MOV CX,0010
MUL  CL
```

watch point:

AX = 020F

CX = 0010

DX 00FF

Question 4

Complete

Marked out of 1.00

To evaluate processor performance, the following indicators and formulas are used:

Cycles per instruction $$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Time to execute a program $$T = I_c \times CPI \times \tau$$

Or $$T = I_c \times [p + (m \times k)] \times \tau$$

In which:
p: the number of processor cycles needed to decode and execute the instruction
m: the number of memory references needed
k: the ratio between memory cycle time and processor cycle time
τ: cycle time = *1/f*

Which of the following system attributes contribute to p (the processor cycles needed to decode and execute the instruction)

Select one or more:

- [ ] Processor implementation
- [ ] Compiler technology
- [ ] Cache and memory hierarchy
- [x] Instruction set architecture

Question 5

Complete

Marked out of 1.50

A system programmer needs to compute 163250 % 32767 + 257 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?

Step 1: MOV EAX,27BD2

Step 2 MOV BX,7FFC

Step 3: DIV BX

Step 4: ADD EAX,101

Result:
EAX = 20000

EDX = 7DB2

Question 6

Not answered

Marked out of 1.00

Convert the 32-bit floating point number 3E580000 (in hex) to decimal.

Answer:

Question 7

Complete

Marked out of 1.00

Major structural components of the CPU include:

Select one or more:

- [ ] Instruction Pointer (PC)
- [x] Arithmetic and Logic Unit
- [ ] Interconnections
- [x] Registers
- [ ] Instruction Register
- [x] Control Unit

Question 8

Not answered

Marked out of 1.00

Convert the 32-bit floating point number 44363800 (in hex) to decimal.

Answer:

Question 9

Complete

Marked out of 0.50

Which are the correct inputs for XLAT instruction

Select one or more:

- [ ] look-up index must be loaded into DL
- [ ] DS:[SI] pointed to look-up table
- [x] DS:[BX] pointed to look-up table
- [x] look-up index must be loaded into AL

Question 10

Complete

Marked out of 1.50

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate MIPS rate for this program

Given:

$$\text{MIPS rate} = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Answer: 8545.994

Question 11

Complete

Marked out of 1.00

Select correct match for register values at watch points:

MOV AX, 4FCA

ADD AX, DDA9

watch point #1:

ADD AH, F3

watch point #2:

.....

watch point #2: AH = 30

watch point #1: AL = 83

Question 12

Complete

Marked out of 1.00

Which statement is correct about interrupt vector table?

Select one or more:

- [x] Store in the beginning area of the main memory
- [ ] Store in the ending area of 1024K of the main memory
- [ ] Take up 1024 bytes in the main memory
- [ ] Store on disk

Question 13

Complete

Marked out of 1.50

A system programmer needs to divide -6247 by 300 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?

Step 1: MOV AX,E799

Step 2: CDW

Step 3: MOV BX,012C

Step 4: IDIV BX

Result:

AX = FFEC

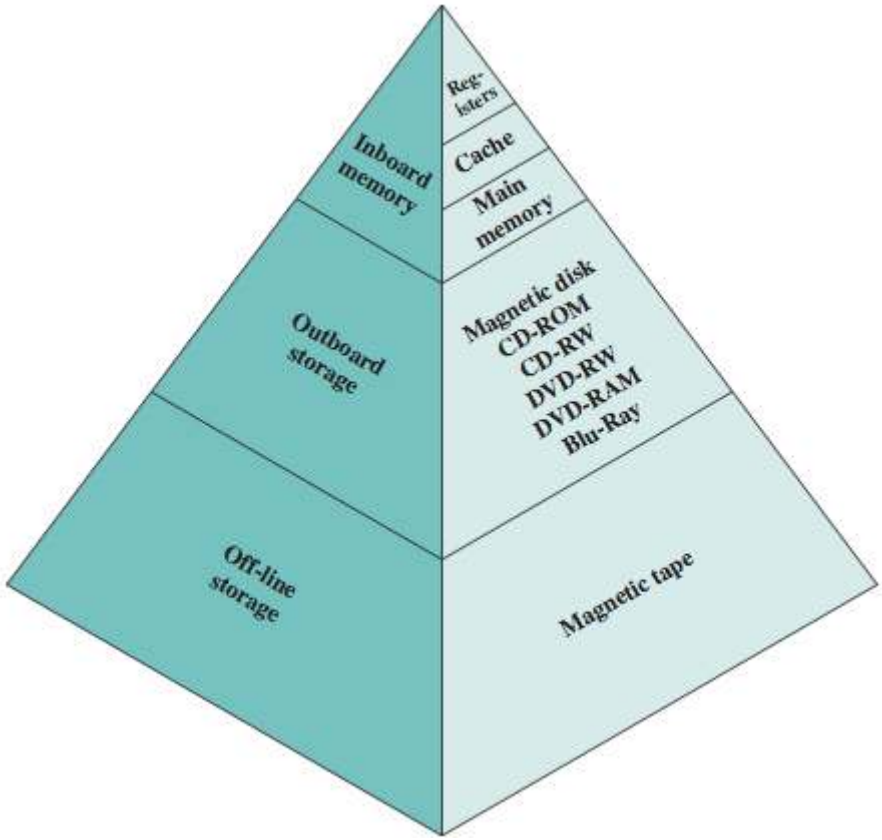
DX = FF09

Question 14

Complete

Marked out of 1.00

For memory hierarchy below, which relationship hold when moving downward



Select one or more:

- [ ] Increasing capacity
- [x] Increasing access time
- [x] the processor accesses more often
- [x] Decreasing cost per bit
- [ ] Decreasing frequency of access by the processor

Question 15

Complete

Marked out of 1.00

Given an assembly code copying the memory buffer Buff1 to Buff2:

```
        PUSH DS
        POP   ES
        LEA   SI, Buff1
        LEA   DI, Buff2
        MOV  CX,20
        ;--- Start of block
cp_loop:
        MOV  AL, Byte Ptr [SI]
        MOV  Byte Ptr ES:[DI], AL
        INC   SI
        INC   DI
        LOOP cp_loop
        ; ---End of block
```

Choose equivalent string operations in place of block

Select one or more:

- [ ]
```
        STD
cp_loop:
        MOVSB
        LOOP cp_loop
```
- [x]
```
        CLD
cp_loop:
        MOVSB
        LOOP cp_loop
```
- [ ]
```
        CLD
        REP MOVSB
```
- [ ]
```
        CLD
cp_loop:
        REP MOVSB
        LOOP cp_loop
```

Question 16

Complete

Marked out of 1.20

What is the correct sequence of instruction cycle?

Step 3	Decode
Step 1	Calculate operand address
Step 6	Execution
Step 4	Fetch opcode
Step 5	Store result
Step 2	Fetch operand

Question 17

Complete

Marked out of 1.00

A memory chip has 12 address pins, determine the maximum memory words of this chip?

Select one:

- 4000
- 2048
- 4096
- 2048K

Question 18

Complete

Marked out of 1.00

Given a code snippet:

```
int n = 10;
do {
    n--;
} while (n > 0);
```

Which ones are the equivalent logic sequence of instructions in Assembly

Select one or more:

-
```
mov cx, 10
a_label:
.....
dec cx
cmp cx,0
jz  a_label
```
-
```
mov cx, 10
a_label:
.....
dec cx
loop  a_label
```
-
```
mov cx, 10
a_label:
dec cx
cmp cx, 0
jz e_label
jmp a_label
e_label:
```
-
```
mov cx, 10
a_label:
.....
loop  a_label
```

Question 19

Not answered

Marked out of 2.00

Make use of string operations, write a sequence of instructions to locate the last space character on the 10th line of screen by peeking at the display memory starting from B800. The result is read from the SI register.

Question 20

Complete

Marked out of 1.00

Memory dump at 1D20:0200 as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers: DS = 1D20, SI = 200, BX = 202, AX = 0103

Identify correct value of AX register after XLAT instruction is executed.

AH = 01h

AL = 47h

Question 21

Complete

Marked out of 0.50

The result of an IMUL instruction is 0060, what is the correct state of Carry flag and Overflow flag?

Select one or more:

- [ ] OF=1
- [ ] CF=1
- [x] OF=0
- [x] CF=0

Question 22

Complete

Marked out of 0.50

The instruction that enables subtraction with borrow is

Select one:

- DEC
- SUB
- None of the choices are correct
- SBB

Question 23

Complete

Marked out of 0.50

After executing PUSH EAX instruction, the stack pointer

Select one:

- increment by 1
- increment by 2
- decrements by 4
- decrement by 1

Question 24

Not answered

Marked out of 1.00

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number E8 (in hex) to decimal.

Answer:

Question 25

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

```
MOV DL,FF
MOV AL,F6
IMUL  DL
```

watch point:

CF = set

OF = reset

Question 26

Complete

Marked out of 1.00

A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines?

Select one:

- 15 address pins, 8 data pins
- 32 address pins, 3 data pins
- 5 address pins, 3 data pins
- 32 address pins, 4 data pins

Question 27

Complete

Marked out of 1.00

What is the correct value of SI, AL (in hex) at watch point:

```
01:             MOV SI, 300h
02:             MOV AL, 10h
03:             MOV CX, 7
04: Loop_label:
05:             MOV [SI], AL
06:             ADD AL,10h
07:             INC  SI
08:             LOOP Loop_label
```

watch point:

AL = 70h

SI 70

Question 28

Complete

Marked out of 0.50

the instruction, CMP to compare source and destination operands by _____

Select one:

- adding
- subtracting
- comparing
- dividing

Question 29

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of CF and OF at watch point?

```
MOV AX,140h
MOV CX,8h
MUL  CX
```

watch point:

CF= reset

OF= not defined

Question 30

Not answered

Marked out of 0.50

Write mask byte (in hex) to set bit 6th, 4th of a byte value with OR instruction (LSB is the 1st bit).

Answer:

Question 31

Complete

Marked out of 0.50

In multiplication instruction, the result is taken from AX means the source operand is _____ bit

Select one:

- 4
- 8
- None of the choices are correct
- 16

Question 32

Complete

Marked out of 1.00

Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of BX register follows the execution of MOV BX, [1D49] is F57F. What is the endian type of this computer system

Select one:

- big-endian
- level-endian
- little-endian
- non-endian

Question 33

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

```
MOV AL, 0F
ADD AL, F1
```

watch point:

Zero flag (OF) = reset ▼

Carry flag (CF) = set ▼

Question 34

Not answered

Marked out of 1.00

the memory stack area of a program shown in figure

The value of SP register is 1D48. What is the value of SP follows the execution of **POP SI**

Answer:

Question 35

Complete

Marked out of 1.00

Structural components of computer include:

Select one or more:

- [ ] Interrupt
- [x] Central processing unit
- [x] Memory
- [ ] DMA
- [x] I/O
- [ ] System interconnection

Question 36

Complete

Marked out of 1.00

Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation?

Select one:

- ( ) Bus Arbiter
- ( ) Direct Memory Access (DMA)
- ( ) Bus master
- (•) Programmed I/O

Question 37

Complete

Marked out of 1.00

Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system:

rotational delay: time for the sector in the request track to reach the head

seek time: time for the head to settle at the request track

access time: seek time + rotational delay

Question 38

Complete

Marked out of 1.00

Which set of registers are valid for addressing a memory location?

Select one or more:

- [ ] SS:DI
- [ ] DS:BX
- [ ] DS:SI
- [x] CS:IP

Question 39

Not answered

Marked out of 1.00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity

Answer: Choose...

Question 40

Complete

Marked out of 1.00

A processor with 16-bit instruction set. The instruction composed of 2 fields: the first byte contains the opcode and the remainder the operand or an operand address.

What is the maximum directly addressable memory capacity?

Select one:

- 256
- 1024
- 512
- 256K

Question 41

Complete

Marked out of 1.00

The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left

Temporal locality — the tendency for a processor to access memory locations that have been used recently

the tendency of execution to involve a number of memory locations that are clustered

Spatial locality — tendency to use large cache and prefetch mechanism

Question 42

Complete

Marked out of 1.00

Convert -89.2345 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa) in hex

Answer: C2B27810

Question 43

Complete

Marked out of 1.00

In computer organization, the CPU transfer rate is much higher than that of memory. It is easy to match performance of these components by:

Select one:

- Introducing cache memory
- producing faster memory module
- increase the bus speed
- increase I/O speed

Question 44

Complete

Marked out of 1.00

Select correct match for AL and carry flag at watch point #1:

```
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
```

watch point #1:

```
.....
```

AL: 6A

Carry flag: set

Question 45

Not answered

Marked out of 2.00

Write a sequence of instructions to sum up 10 values of word in memory starting from 200h. The result must be stored at memory location 300h.

◄ Announcements

Return to: BÀI THI CUỐI KỲ...

Bai thi ktmt k16 - KTMT

Computer Architecture and Assembly language (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

THI Kiến trúc máy tính và hợp ngữ (Thi Chung)

Bắt đầu vào lúc	Monday, 28 May 2018, 1:10 PM
State	Finished
Kết thúc lúc	Monday, 28 May 2018, 2:14 PM
Thời gian thực hiện	1 giờ 4 phút

Câu hỏi 1

Hoàn thành

Đạt điểm 1,00

Consider the following assembly instruction sequence

```
        CMP DL, 0
        JB    x_label
        CMP DL, 9
        JA    a_label
        ADD DL, 30h
        JMP  x_label
a_label:
        CMP DL, 0Fh
        JA    x_label
        ADD DL, 31h
x_label:
        MOV AL, DL
watch point:
...
```

Choose correct value of AL register at watch point for different value of DL?

DL=55h [85h]

DL=0FFh [41h]

DL=10 [38h]

DL=8 [0FFh]

Câu hỏi 2

Hoàn thành

Đạt điểm 1,00

Select correct match for AX (Decimal) at watch points:

```
                    MOV AX, 1BC
                    MOV CL, 2
                    SHL  AX, CL
watch point #1:
                    ADD  AX, 166
watch point #2:
                    SHR   AX, CL
watch point #3:
                    SHR   AX, CL
                   ......
```

watch point #1: [1064]

watch point #2: [266]

watch point #3: [266]

Câu hỏi 3
Hoàn thành
Đạt điểm 0,50

if the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is called

Select one:
- intrasegment mode
- intersegment mode
- intrasegment indirect mode
- intrasegment direct mode

Câu hỏi 4
Hoàn thành
Đạt điểm 1,00

Structural components of computer include:

Select one or more:
- [x] System interconnection
- [ ] Interrupt
- [x] Central processing unit
- [x] I/O
- [x] Memory
- [ ] DMA

Câu hỏi 5
Hoàn thành
Đạt điểm 0,50

Which could be correct ones for the destination operand in a data movement instruction?

Select one or more:
- [ ] immediate data
- [ ] all choices are correct
- [x] register
- [x] memory location

Câu hỏi 6
Hoàn thành
Đạt điểm 0,50

the instruction, JMP C008:2000h is an example of

Select one or more:
- [ ] intrasegment mode
- [x] near jump
- [ ] intersegment jump
- [x] far jump

Câu hỏi 7
Hoàn thành
Đạt điểm 1,00

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 00 40 08 42 - 99 80 3E 20 99 00 75 24

SI = 120

The following instruction is executed:

MOV EAX, [SI+4]

Assume the value in EAX is a 32-bit floating-point binary, what is the value of EAX in decimal?

Answer: 4000

Câu hỏi 8

Hoàn thành

Đạt điểm 1,00

Given a code snippet:

```
int n = 10;
do {
    n--;
} while (n > 0);
```

Which ones are the equivalent logic sequence of instructions in Assembly

Select one or more:

- [x]
```
mov cx, 10
a_label:
 .....
 loop  a_label
```
- [ ]
```
mov cx, 10
a_label:
 .....
 dec cx
 cmp cx,0
 jz  a_label
```
- [ ]
```
mov cx, 10
a_label:
 .....
 dec cx
 loop  a_label
```
- [x]
```
 mov cx, 10
a_label:
   dec cx
  cmp cx, 0
  jz e_label
  jmp a_label
e_label:
```

Câu hỏi 9

Hoàn thành

Đạt điểm 1,00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

```
MOV AX,30
MOV CX,FFFF
MUL  CX
```

watch point:

CX = FFFF

AX = FFD0

DX 002F

Câu hỏi 10

Không trả lời

Đạt điểm 0,50

Write mask byte (in hex) to set higher 4 bits in a byte value with OR instruction (LSB is the 1st bit).

Answer:

Câu hỏi 11
Hoàn thành
Đạt điểm 0,50

After executing PUSH EAX instruction, the stack pointer

Select one:

- increment by 1
- decrements by 4
- decrement by 1
- increment by 2

Câu hỏi 12
Không trả lời
Đạt điểm 1,00

Given an assembly code copying the memory buffer Buff1 to Buff2:

```
        PUSH DS
        POP   ES
        LEA   SI, Buff1
        LEA   DI, Buff2
        MOV  CX,20
        ;--- Start of block
cp_loop:
        MOV  AL, Byte Ptr [SI]
        MOV  Byte Ptr ES:[DI], AL
        INC   SI
        INC   DI
        LOOP cp_loop
        ; ---End of block
```

Choose equivalent string operations in place of block

Select one or more:

- ☐
```
CLD
cp_loop:
    MOVSB
    LOOP cp_loop
```
- ☐
```
STD
cp_loop:
    MOVSB
    LOOP cp_loop
```
- ☐
```
CLD
cp_loop:
    REP MOVSB
    LOOP cp_loop
```
- ☐
```
CLD
REP MOVSB
```

Câu hỏi 13
Hoàn thành
Đạt điểm 0,50

the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is

Select one:

- CMPS
- SCAS
- CMPS
- REP

Câu hỏi 14
Hoàn thành
Đạt điểm 0,50

Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.

Answer: AND AL, 01111111B

Câu hỏi 15

Không trả lời

Đạt điểm 1,00

Convert -89.2345 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa) in hex

Answer:

Câu hỏi 16

Không trả lời

Đạt điểm 1,50

Given a row of memory image in debug

072C:FFF0 00 00 00 01 00 00 2C 07 - 07 01 2C 07 17 72 00 00

SS=072C, SP=FFF8, DS = 072C

Assume the stack now stores two (2) 16-bit parameters and one (1) 16-bit return address in following order: stack top (return address) >> parameter #1 >> parameter #2.

The following sequence of instructions are executed. What is the correct values at watch points?

MOV BP, SP

watch point #1 (BP):

MOV AX, [BP+2]

watch point #2 (AX):

ADD AX, [BP+4]

watch point #3 (AX):

MOV DI, 120

MOV [DI], AX

watch point #1: Chọn...

watch point #2: Chọn...

watch point #3: Chọn...

Câu hỏi 17

Hoàn thành

Đạt điểm 0,50

The instruction that subtracts 1 from the contents of the specified register/memory location is

Select one:

- DEC
- SUB
- SBB
- INC

Câu hỏi 18
Không trả lời
Đạt điểm 1,00

Memory dump at 1D20:0200 shown as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers:

DS = 1D20, ES = 1D20, DI = 20A

The following sequence of instructions are executed:

```
MOV SI,208h
MOV AX,0040h
MOV CX,000Ah
CLD
REPNZ SCASB
```

watch point:

```
. . . . .
```

What is the correct value of AX, SI, DI registers at watch point?

DI = Chọn...

AX = Chọn...

SI = Chọn...

Câu hỏi 19
Hoàn thành
Đạt điểm 1,00

What is the meaning of Amdahl's law in processor performance evaluation?

Select one:

- the cost reduce when moving from single-core to multicore processor
- the maximum speedup of a multicore processor
- the potential speedup of a program using multiple processor compared to a single processor
- the speedup of a multicore processor when increasing system bus speed

Câu hỏi 20
Hoàn thành
Đạt điểm 0,50

Which are the correct actions for LODSW string operation if DF is reset (=0)

Select one or more:

- [ ] decrease DI by 2
- [ ] Load 16-bit value at memory location pointed by ES:[DI] into AX
- [x] increase SI by 2
- [x] Load 16-bit value at memory location pointed by DS:[SI] into AX

Câu hỏi 21
Không trả lời
Đạt điểm 1,00

When many devices of different transmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this:

Select one:

- PCI Express bus
- Multiple-Bus hierarchies
- PCI bus
- Split system bus into local bus and memory bus

Câu hỏi 22
Hoàn thành
Đạt điểm 0,50

the instruction, CMP to compare source and destination operands by _____

Select one:
- adding
- comparing
- dividing
- subtracting

Câu hỏi 23
Hoàn thành
Đạt điểm 1,00

To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?

Select one or more:
- [ ] Make use of both on-chip and off-chip cache memory
- [x] Make wider data bus path
- [x] Using higher-speed bus and us hierarchy
- [x] To move data directly by DMA

Câu hỏi 24
Hoàn thành
Đạt điểm 1,00

The following sequence of instructions are executed. What is the correct value of AX, DX at watch point?

```
MOV DL,FF
MOV AL,42
IMUL  DL
```

watch point:

AX = FFBE

DX = 0000

Câu hỏi 25
Hoàn thành
Đạt điểm 0,50

In the RCR instruction, the contents of the destination operand undergoes function as

Select one:
- carry flag is pushed into LSB then MSB is pushed into carry flag
- overflow flag is pushed into MSB then LSB is pushed into carry flag
- carry flag is pushed into MSB then LSB is pushed into carry flag
- auxiliary flag is pushed into LSB then MSB is pushed into carry flag

Câu hỏi 26
Hoàn thành
Đạt điểm 0,50

Which could be correct ones for the source operand in an instruction?

Select one or more:
- [x] immediate data
- [x] memory location
- [ ] indirect data
- [x] register

Câu hỏi 27
Hoàn thành
Đạt điểm 1,00

Convert the 32-bit floating point number A3358000 (in hex) to decimal.

Note:

Result with exponent should be written like (e.g): 1.2345678x10^-13 or 1.2345678x10^13 (no space between digits/characters)

Answer: -9.83913471531×10^-18

Câu hỏi 28
Hoàn thành
Đạt điểm 1,00

Select correct match for register values at watch points:

```
                MOV AX, 152D
                ADD AX, 003F
watch point #1:
                ADD AH, 10
watch point #2:
                ......
```

watch point #2: AH = 25

watch point #1: AL = 6C

Câu hỏi 29
Hoàn thành
Đạt điểm 0,50

Which are the correct actions for SCASW string operation if DF is set (=1)

Select one or more:

- [x] decrease DI by 2
- [x] compare the value in AX register with 16-bit value at the memory location pointed by ES:[DI] and set/clear flag bits accordingly
- [ ] increase DI by 2
- [ ] compare the value in AX register with 16-bit value at the memory location pointed by DS:[SI] and set/clear flag bits accordingly

Câu hỏi 30
Hoàn thành
Đạt điểm 1,00

What is the correct value of SI, AL (in hex) at watch point:

```
01:             MOV SI, 300h
02:             MOV AL, 10h
03:             MOV CX, 7
04: Loop_label:
05:             MOV [SI], AL
06:             ADD AL,10h
07:             INC  SI
08:             LOOP Loop_label
```

watch point:

SI 80h

AL = 80h

Câu hỏi 31
Hoàn thành
Đạt điểm 1,00

Select the correct sequence of instructions to compute -1024/128 (all values are in hex).

Step 1: CWD

Step 2: MOV CX,80

Step 3: MOV CL,80

Step 4: IDIV CL

Câu hỏi 32

Hoàn thành

Đạt điểm 1,00

Select correct match for AL and carry flag at watch point #1:

```
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
```

watch point #1:

```
.....
```

AL: 0A

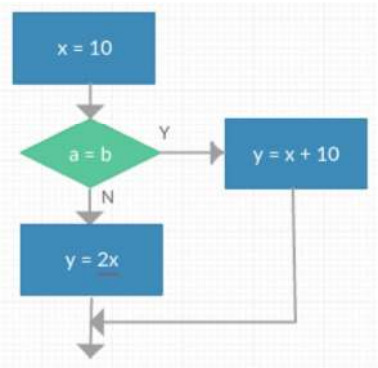
Carry flag: set

Câu hỏi 33

Hoàn thành

Đạt điểm 1,00

Given a flowchart of an algorithm:



Select the correct instruction sequence:

Select one or more:

☐
```
    mov dl,10
    cmp al,bl
    jnz n_label
    add dl,10
    jmp e_label
n_label:
    mov cl,1
    shl dl,cl
e_label:
    mov dh,dl
```

☑
```
    mov dl,10
    cmp al,bl
    jnz n_label
    add dl,10
    mov dh,dl
    jmp e_label
n_label:
    mov cl,1
    shl dl,cl
e_label:
    mov dh,dl
```

☐
```
    mov dl,10
    cmp al,bl
    jnz n_label
    add dl,10
    jmp e_label
n_label:
    mov cl,1
    shr dl,cl
e_label:
    mov dh,dl
```

☐
```
    mov dl,10
    cmp al,bl
    jz  n_label
    mov cl,1
    shl dl,cl
    jmp e_label
n_label:
    add dl,10
e_label:
    mov dh,dl
```

Câu hỏi 34
Hoàn thành
Đạt điểm 0,50

After executing the POP EAX instruction, the stack pointer

Select one:
- decrements by 4
- decrements by 2
- increments by 4
- increment by 1

Câu hỏi 35
Hoàn thành
Đạt điểm 0,50

Sign-extend number BF (8-bit binary) to 16-bit. Write result in hex

Answer: 191

Câu hỏi 36
Hoàn thành
Đạt điểm 0,50

Which of the following instructions are not valid?

Select one or more:
- [x] MOV DS, B800h
- [ ] MOV AX, [BP+2]
- [x] MOV SP, SS:[SI+2]
- [ ] MOV AX, SI

Câu hỏi 37
Hoàn thành
Đạt điểm 1,00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

```
MOV AL, 0F
ADD AL, F1
```

watch point:

Zero flag (OF) = reset

Carry flag (CF) = set

Câu hỏi 38
Hoàn thành
Đạt điểm 1,00

Major structural components of the CPU include:

Select one or more:
- [x] Registers
- [x] Arithmetic and Logic Unit
- [ ] Instruction Pointer (PC)
- [x] Interconnections
- [x] Control Unit
- [ ] Instruction Register

Câu hỏi 39
Hoàn thành
Đạt điểm 1,00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity

Answer: 512 KB

Câu hỏi 40

Hoàn thành

Đạt điểm 1,00

What best describe the Spatial and Temporal Locality?

Temporal locality	be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy
Spatial locality	be exploited by moving data between cache and memory more efficient

Câu hỏi 41

Hoàn thành

Đạt điểm 1,00

Given a code snippet:

```
int ax, bx;
...
if (ax >= bx)
   ax -=bx;
else
   bx -=ax;
```

What is the equivalent logic sequence of instructions in Assembly

Select one:

- cmp ax,bx
  jl a_label
  sub ax,bx
  jmp x_label
  a_label:
  sub bx,ax
  x_label:
- cmp ax,bx
  jbe a_label
  sub ax,bx
  jmp x_label
  a_label:
  sub bx,ax
  x_label:
- cmp ax,bx
  ja a_label
  sub ax,bx
  jmp x_label
  a_label:
  sub bx,ax
  x_label:
- cmp ax,bx
  jge a_label
  sub ax,bx
  jmp x_label
  a_label:
  sub bx,ax
  x_label:

Câu hỏi 42

Hoàn thành

Đạt điểm 0,50

Which of the following is not a data copy/transfer instruction?

Select one or more:

- [x] ADC
- [ ] MOV
- [ ] LEA
- [x] DAS

Return to: General