Thi Kiến Trúc Máy Tính và Hợp Ngữ

Computer Architecture and Assembly language (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

THI Kiến trúc máy tính và hợp ngữ (lớp CHẴN)

Started on	Monday, 30 December 2019, 1:10 PM
State	Finished
Completed on	Monday, 30 December 2019, 2:20 PM
Time taken	1 hour 10 mins

Question 1

Complete

Marked out of 1.00

Which ones are not correct for static RAM?

Select one or more:

- [x] Cheaper than dynamic RAM because simpler chip controller
- [x] Cost per bit is higher than dynamic RAM
- [ ] Cost per bit is lower than dynamic RAM
- [x] faster than dynamic RAM because they are made from capacitor

Question 2

Complete

Marked out of 1.00

Match the correct definition of flag bits in PSW.

indicates the result of an arithmetic or comparison operation	CF
contains the carry from bit 3 to bit 4 following an arithmetic operation	AF
indicates the overflow of leftmost bit of data after an arithmetic operation	OF
shows the sign of the result of an arithmetic operation	SF

Question 3

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

```
MOV AX,0020
MOV CX,0010
MUL  CL
```

watch point:

AX = 020F

CX = 0010

DX 00FF

Question 4

Complete

Marked out of 1.00

To evaluate processor performance, the following indicators and formulas are used:

Cycles per instruction $$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Time to execute a program $$T = I_c \times CPI \times \tau$$

Or $$T = I_c \times [p + (m \times k)] \times \tau$$

In which:
p: the number of processor cycles needed to decode and execute the instruction
m: the number of memory references needed
k: the ratio between memory cycle time and processor cycle time
τ: cycle time = *1/f*

Which of the following system attributes contribute to p (the processor cycles needed to decode and execute the instruction)

Select one or more:

- [ ] Processor implementation
- [ ] Compiler technology
- [ ] Cache and memory hierarchy
- [x] Instruction set architecture

Question 5

Complete

Marked out of 1.50

A system programmer needs to compute 163250 % 32767 + 257 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?

Step 1: MOV EAX,27BD2

Step 2 MOV BX,7FFC

Step 3: DIV BX

Step 4: ADD EAX,101

Result:
EAX = 20000

EDX = 7DB2

Question 6

Not answered

Marked out of 1.00

Convert the 32-bit floating point number 3E580000 (in hex) to decimal.

Answer:

Question 7

Complete

Marked out of 1.00

Major structural components of the CPU include:

Select one or more:

- [ ] Instruction Pointer (PC)
- [x] Arithmetic and Logic Unit
- [ ] Interconnections
- [x] Registers
- [ ] Instruction Register
- [x] Control Unit

Question 8

Not answered

Marked out of 1.00

Convert the 32-bit floating point number 44363800 (in hex) to decimal.

Answer:

Question 9

Complete

Marked out of 0.50

Which are the correct inputs for XLAT instruction

Select one or more:

- [ ] look-up index must be loaded into DL
- [ ] DS:[SI] pointed to look-up table
- [x] DS:[BX] pointed to look-up table
- [x] look-up index must be loaded into AL

Question 10

Complete

Marked out of 1.50

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Calculate MIPS rate for this program

Given:

$$\text{MIPS rate} = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

Answer: 8545.994

Question 11

Complete

Marked out of 1.00

Select correct match for register values at watch points:

MOV AX, 4FCA

ADD AX, DDA9

watch point #1:

ADD AH, F3

watch point #2:

.....

watch point #2: AH = 30

watch point #1: AL = 83

Question 12

Complete

Marked out of 1.00

Which statement is correct about interrupt vector table?

Select one or more:

- [x] Store in the beginning area of the main memory
- [ ] Store in the ending area of 1024K of the main memory
- [ ] Take up 1024 bytes in the main memory
- [ ] Store on disk

Question 13

Complete

Marked out of 1.50

A system programmer needs to divide -6247 by 300 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?

Step 1: MOV AX,E799

Step 2: CDW

Step 3: MOV BX,012C

Step 4: IDIV BX

Result:

AX = FFEC

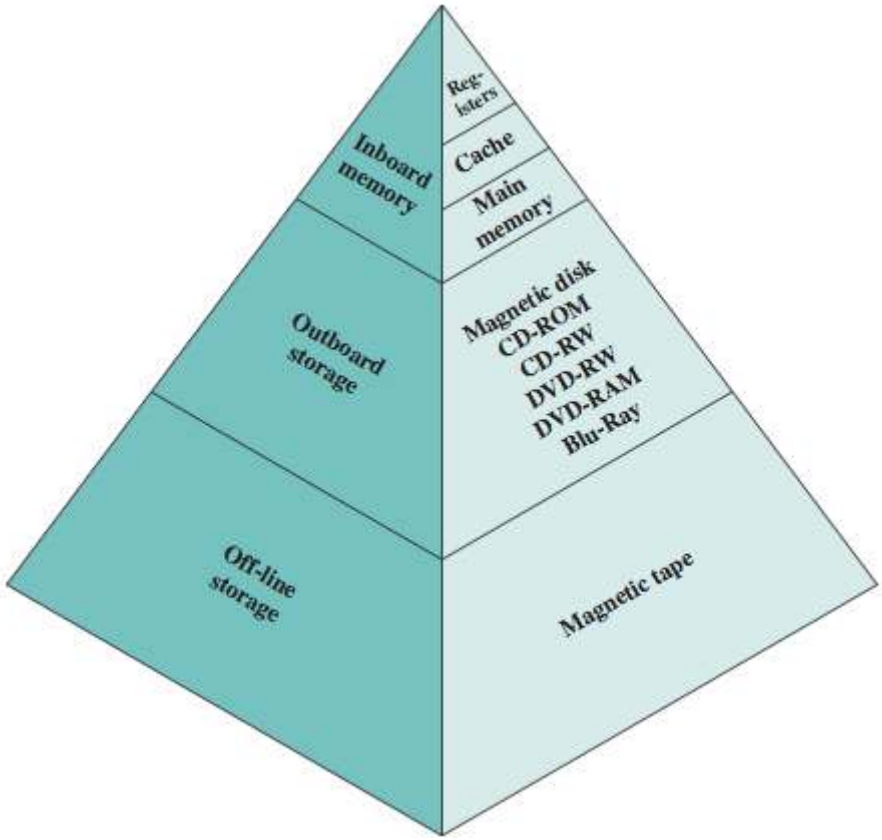
DX = FF09

Question 14

Complete

Marked out of 1.00

For memory hierarchy below, which relationship hold when moving downward



Select one or more:

- [ ] Increasing capacity
- [x] Increasing access time
- [x] the processor accesses more often
- [x] Decreasing cost per bit
- [ ] Decreasing frequency of access by the processor

Question 15

Complete

Marked out of 1.00

Given an assembly code copying the memory buffer Buff1 to Buff2:

```
        PUSH DS
        POP   ES
        LEA   SI, Buff1
        LEA   DI, Buff2
        MOV  CX,20
        ;--- Start of block
cp_loop:
        MOV  AL, Byte Ptr [SI]
        MOV  Byte Ptr ES:[DI], AL
        INC   SI
        INC   DI
        LOOP cp_loop
        ; ---End of block
```

Choose equivalent string operations in place of block

Select one or more:

- [ ]
```
        STD
cp_loop:
        MOVSB
        LOOP cp_loop
```
- [x]
```
        CLD
cp_loop:
        MOVSB
        LOOP cp_loop
```
- [ ]
```
        CLD
        REP MOVSB
```
- [ ]
```
        CLD
cp_loop:
        REP MOVSB
        LOOP cp_loop
```

Question 16

Complete

Marked out of 1.20

What is the correct sequence of instruction cycle?

Step 3	Decode
Step 1	Calculate operand address
Step 6	Execution
Step 4	Fetch opcode
Step 5	Store result
Step 2	Fetch operand

Question 17

Complete

Marked out of 1.00

A memory chip has 12 address pins, determine the maximum memory words of this chip?

Select one:

- 4000
- 2048
- 4096
- 2048K

Question 18

Complete

Marked out of 1.00

Given a code snippet:

```
int n = 10;
do {
    n--;
} while (n > 0);
```

Which ones are the equivalent logic sequence of instructions in Assembly

Select one or more:

-
```
mov cx, 10
a_label:
.....
dec cx
cmp cx,0
jz  a_label
```
-
```
mov cx, 10
a_label:
.....
dec cx
loop  a_label
```
-
```
mov cx, 10
a_label:
dec cx
cmp cx, 0
jz e_label
jmp a_label
e_label:
```
-
```
mov cx, 10
a_label:
.....
loop  a_label
```

Question 19

Not answered

Marked out of 2.00

Make use of string operations, write a sequence of instructions to locate the last space character on the 10th line of screen by peeking at the display memory starting from B800. The result is read from the SI register.

Question 20

Complete

Marked out of 1.00

Memory dump at 1D20:0200 as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers: DS = 1D20, SI = 200, BX = 202, AX = 0103

Identify correct value of AX register after XLAT instruction is executed.

AH = 01h

AL = 47h

Question 21

Complete

Marked out of 0.50

The result of an IMUL instruction is 0060, what is the correct state of Carry flag and Overflow flag?

Select one or more:

- [ ] OF=1
- [ ] CF=1
- [x] OF=0
- [x] CF=0

Question 22

Complete

Marked out of 0.50

The instruction that enables subtraction with borrow is

Select one:

- DEC
- SUB
- None of the choices are correct
- SBB

Question 23

Complete

Marked out of 0.50

After executing PUSH EAX instruction, the stack pointer

Select one:

- increment by 1
- increment by 2
- decrements by 4
- decrement by 1

Question 24

Not answered

Marked out of 1.00

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number E8 (in hex) to decimal.

Answer:

Question 25

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

```
MOV DL,FF
MOV AL,F6
IMUL  DL
```

watch point:

CF = set

OF = reset

Question 26

Complete

Marked out of 1.00

A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines?

Select one:

- 15 address pins, 8 data pins
- 32 address pins, 3 data pins
- 5 address pins, 3 data pins
- 32 address pins, 4 data pins

Question 27

Complete

Marked out of 1.00

What is the correct value of SI, AL (in hex) at watch point:

```
01:             MOV SI, 300h
02:             MOV AL, 10h
03:             MOV CX, 7
04: Loop_label:
05:             MOV [SI], AL
06:             ADD AL,10h
07:             INC  SI
08:             LOOP Loop_label
```

watch point:

AL = 70h

SI 70

Question 28

Complete

Marked out of 0.50

the instruction, CMP to compare source and destination operands by _____

Select one:

- adding
- subtracting
- comparing
- dividing

Question 29

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of CF and OF at watch point?

```
MOV AX,140h
MOV CX,8h
MUL  CX
```

watch point:

CF= reset

OF= not defined

Question 30

Not answered

Marked out of 0.50

Write mask byte (in hex) to set bit 6th, 4th of a byte value with OR instruction (LSB is the 1st bit).

Answer:

Question 31

Complete

Marked out of 0.50

In multiplication instruction, the result is taken from AX means the source operand is _____ bit

Select one:

- 4
- 8
- None of the choices are correct
- 16

Question 32

Complete

Marked out of 1.00

Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of BX register follows the execution of MOV BX, [1D49] is F57F. What is the endian type of this computer system

Select one:

- big-endian
- level-endian
- little-endian
- non-endian

Question 33

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

```
MOV AL, 0F
ADD AL, F1
```

watch point:

Zero flag (OF) = reset ▼

Carry flag (CF) = set ▼

Question 34

Not answered

Marked out of 1.00

the memory stack area of a program shown in figure

The value of SP register is 1D48. What is the value of SP follows the execution of **POP SI**

Answer:

Question 35

Complete

Marked out of 1.00

Structural components of computer include:

Select one or more:

- [ ] Interrupt
- [x] Central processing unit
- [x] Memory
- [ ] DMA
- [x] I/O
- [ ] System interconnection

Question 36

Complete

Marked out of 1.00

Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation?

Select one:

- ( ) Bus Arbiter
- ( ) Direct Memory Access (DMA)
- ( ) Bus master
- (•) Programmed I/O

Question 37

Complete

Marked out of 1.00

Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system:

rotational delay: time for the sector in the request track to reach the head

seek time: time for the head to settle at the request track

access time: seek time + rotational delay

Question 38

Complete

Marked out of 1.00

Which set of registers are valid for addressing a memory location?

Select one or more:

- [ ] SS:DI
- [ ] DS:BX
- [ ] DS:SI
- [x] CS:IP

Question 39

Not answered

Marked out of 1.00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity

Answer: Choose...

Question 40

Complete

Marked out of 1.00

A processor with 16-bit instruction set. The instruction composed of 2 fields: the first byte contains the opcode and the remainder the operand or an operand address.

What is the maximum directly addressable memory capacity?

Select one:

- 256
- 1024
- 512
- 256K

Question 41

Complete

Marked out of 1.00

The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left

Temporal locality — the tendency for a processor to access memory locations that have been used recently

the tendency of execution to involve a number of memory locations that are clustered

Spatial locality — tendency to use large cache and prefetch mechanism

Question 42

Complete

Marked out of 1.00

Convert -89.2345 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa) in hex

Answer: C2B27810

Question 43

Complete

Marked out of 1.00

In computer organization, the CPU transfer rate is much higher than that of memory. It is easy to match performance of these components by:

Select one:

- Introducing cache memory
- producing faster memory module
- increase the bus speed
- increase I/O speed

Question 44

Complete

Marked out of 1.00

Select correct match for AL and carry flag at watch point #1:

```
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
```

watch point #1:

```
.....
```

AL: 6A

Carry flag: set

Question 45

Not answered

Marked out of 2.00

Write a sequence of instructions to sum up 10 values of word in memory starting from 200h. The result must be stored at memory location 300h.

◄ Announcements

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