Trắc nghiệm KTMT

Computer Architecture and Assembly language (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

TRẮC NGHIỆM

1. **Given 8bit floatingpoint binary format: 1 (sign) + 3 (exponent) + 4 (mantissa)**
   Convert the 8bit floating point number (số đề cho) (in hex) to decimal

Answer: **57 = 5.75** *(57: đề, 5.75: đáp án)*

E7 = -11,5

68 = 12

2. **Convert the 32bit floating point number (số đề cho) (in hex) to decimal.**
   Note: Result with exponent should be written like (e.g): 1.2345678x10^-13 or 1.2345678x10^13 (no space between digits/characters)

Answer: **C4361000 = 728,25** *(C4361000: đề, -728,25: đáp án)*

7665000 = 1.1611679x10^33

3. **Convert (số đề cho) to IEEE 32-bit floating point format (1 sign + 8 exponent + 23 mantissa) in hex**

Answer: **-89.2345 = C2B27800** *(-89.2345: đề, C2B27800: đáp án)*

39887.5625 = 471BCF90

0.1015625 = 3DD00000

4. **A system programmer needs to divide 6247 by 300 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?**

Answer: **Step 1: MOV AX, E799**

Step 2: CDW

Step 3: MOV BX, 012C

Step 4: IDIV BX

Result:

AX = FFEC

DX = FF09

5. **Write mask byte (in hex) to clear the lower 4 bit of a byte value with AND instruction.**

Answer: F0

6. **EAX now stored a 32bit IP address of a host. The network ID (netID) is 20 bit and can be extracted from IP byte anding with a 32bit mask. Write correct instruction to extract netID from EAX register.**
   Note: Immediate value must be written in hex

Answer: AND EAX, FFFFF000

7. **The following sequence of instructions are executed. What is the correct values at Watch point?**

```
MOV AX, 67FE
MOV BX, AX
MOV CL, BH
MOV CH, BL
```

Watch point:

Answer: **CX = FE67**

BX = 67FE

8. **The following sequence of instructions are executed. What is the correct value of flag bits at Watch point?**

```
MOV EAX, 12AE
SUB EAX, 12AF
```

Watch point:

Answer: **Sign flag = set**

Zero flag (OF) = reset

Carry flag (CF) = set

9. **The following sequence of instructions are executed. What is the correct value of CF and OF at Watch point?**

```
MOV AX, 140h
MOV CX, 8h
MUL CX
```

Watch point:

Answer: **CF = reset**

OF = reset

10. **The following sequence of instructions are executed. What is the correct value of AX, CX, DX at Watch point?**

```
MOV AX, 30
MOV CX, FFFF
MUL CX
```

Watch point:

Answer: **CX = FFFF**

AX = FFD0

DX = 002F

11. The following sequence of instructions are executed. What is the correct value of flag bits at Watch point?

MOV DL, FF

MOV AL, F6

IMUL DL

Watch point:

Answer: **CF =**

OF =

12. The following sequence of instructions are executed. What is the correct value of AX, CX, DX, at Watch point ?

MOV AX, 0020

MOV CX, 0010

MUL CL

Watch point:

Answer: **CX =**

DX =

AX =

13. The following sequence of instruction are executed. What is the correct value of flag bits at Watch point?

MOV AL, -5

SUB AL, 124

Watch point:

Answer: **Carry flag (CF) =**

Sign flag (SF) =

Overflow flag (OF) =

Zero flag (OF) =

14. The following sequence of instructions are executed. What is the correct value of AX, DX at Watch point?

MOV DL, FF

MOV AL, 42

IMUL DL

Watch point:

Answer: **AX = 41BE**

DX = 00FF

15. **The following sequence of instructions are executed. What is the correct value of flag bits at Watch point?**

Answer: **OF = set**

CF = set

16. **The following sequence of instructions are executed. What is the correct value of flag bits at Watch point?**

```
MOV AL,78
MOV BL,2
MUL BL
```

Watch point:

Answer: **Carry flag (CF) = set**

Overflow flag (OF) = no

17. **The following sequence of instructions are executed. What is the correct value of EAX, EBX, EDX at Watch point?**

```
MOV EAX ,00002000
MOV EBX ,00100000
MUL EBX
```

Watch point:

Answer: **EDX =**

EAX =

EBX =

18. **Physical address of the stack pointer is 2DA82, stack segment located at 1DAE. Computer the value of SP register?**

Answer: FFA2

19. **Match the following hexadecimal numbers to octal**

Answer: **E7 = 347**

6E = 156

A9 = 251

20. **Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D**

Answer: f 100 1FF 0D

21. **Match the correct answer for binary operations on the left**

Answer: **1111111 111 = 1111000**

1100111 111

1100111 111 = 1100000

1010101 + 10101 = 1101010

1010110 101 = 1010001

1110011 + 11001 = 10001100

1111111 + 11111 = 10011110

22. Convert the following binary numbers to hexadecimal

Answer: 10101001 = A9

01101110 = 6E

11100101 = E5

11100111 = E7

23. To isolate one or more bits in a byte value, use _____ instruction.

Answer: AND

24. To clear one or more bits in a byte value, use _____ instructions.

Answer: AND

25. To encrypt a byte value, use _____ instruction.

Answer: XOR

26. To test one bit in a byte value without destructing (non – destructive) the byte, use _____ instruction.

Answer: TEST

27. To test one bit in a byte value which can be destructive, use _____ instruction

Answer: AND

28. Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E 99 80 3E 20 99 00 75 24

Initially, AX=BX=CX=DX=0, SI=121

What are value of CX,DX after execution of the following instructions?

MOV DX, [SI]

MOV CX, [SI+2]

Answer: DX = D096

CX = D0E0

29. Select correct match for register values at Watch points:

MOV AX, 152D

ADD AX, 003F

Watch point #1:

ADD AH, 10

Watch point #2:

.....

Answer: Watch point #1: AL = 6C

Watch point #2: AH = 25

30. A memory location located in extra segment which now has value of 564F. This memory managed by ES:SI registerpair. SI now points to 905F. Compute the physical address of this memory location

Answer: 5F54F

31. Select correct match for AL and carry flag at Watch point #1:

```
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
```

Watch point #1:

.....

Answer: Carry flag = set

AL = 0A

32. Which of the following instructions are not legal addressing?

Select one or more:

Answer: MOV AX, [BX+SP]

MOV AX, [SP+1]

33. Compute the physical address of stack top if stack pointer is FFAE and stack segment located at 1DAE

Answer: 2DA8E

34. Signextend number 1011 0101 (8bit binary) to 16bit

Answer: 1111111110110101

35. Given a code snippet:

```
int n = 10;
do {
    n--;
} while (n > 0)
```

Which ones are the equivalent logic sequence of instruction in Assembly

Answer:

36. In computer, how does the processor serve multiple interrupt request from devices? Select one:

Answer: Each device are assigned an interrupt priority, the device with lower priority will be served

37. **In multiplication instruction, when the source operand is 16 bit, how can the result be taken?**

Answer:

38. **Memory dump at 1D20:0200 as below:**

    1D20:0200 00 20 10 5D 55 47 00 90 – 00 10 20 30 40 50 60 70

    Given value of registers: DS = 1D20, SI = 200, BX = 202, AX = 0103

    Identify correct value of AX register after XLAT instruction is executed

Answer: **AL =**

AH =

39. **Which of the following instructions are not valid?**

Answer:

40. **Which could be correct ones for the destination operand in a data movement instruction?**

Answer: **Register**

Memory location

41. **Which are correct action for LODSB string operation if DF is reset (=0)**

    Select one or more:

Answer: **Increase SI by 1**

Load 8-bit value at memory location pointed by DS:[SI] into AL

(ghi chú: DF=0 tăng, DF=1 giảm)

42. **Which are correct action for LODSW string operation if DF is reset (=0)**

    Select one or more:

Answer: **Increase SI by 2**

Load 16-bit value at memory location pointed by DS:[SI] into AX

43. **Which are correct action for STOSB string operation if DF is reset (=0)**

    Select one or more:

Answer: **Increase DI by 1**

Store 8-bit value from AL into memory location pointed by ES:[DI]

44. **Which are correct action for SCASW string operation if DF is reset (=0)**

    Select one or more:

Answer: **Increase DI by 2**

Compare value in AL register with memory location pointed by ES:[DI]

45. The memory stack area of a program shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of PUSH SI

Answer:

46. Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E 99 80 3E 20 99 00 75 24

SI = 120, DI = 128

Select correct sequence of instructions to subtract words at [DI] from [SI] then store the result at memory location 12A

Answer: Step 1:

Step 2:

Step 3:

Step 4:

47. Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E 99 80 3E 20 99 00 75 24

SI = 120, DI = 128

Select correct sequence of instructions to add words at [SI] and [DI] then store the sum at memory location 12A

Answer: Step 1: MOV AX, [SI]

Step 2: ADD [SI], [DI]

Step 3: MOV BX, 012A

Step 4: MOV [BX], AX

48. The instruction that adds contents of memory location specified in a register to the contents of a register is

Answer: ADD

49. Physical address of the instruction pointer is 2040E, code segment located at 1FAF. Compute the value of IP register?

Answer: 91E

50. In multiplication instruction, the result is taken from AX means the source operand is _____ bit

Answer: 16

51. After each execution of PUSH instruction, the stack pointer is

Answer: decrement by 2

52. After each execution of POP instruction, the stack pointer is

Answer: increment by 2

53. The instruction, CMP to compare source and destination operands by _____

Answer: subtracting

54. Match the decimal value of the following 2's complement.

Answer: 10010111 = -105

11010110 = -42

11010000 = -48

55. Câu 3:What is the correct value of SI, AL(in HEX) at Watch point:

```
01: MOV SI, 300h
02: MOV AL, 10h
03: MOV CX, 7
04: Loop_label:
05: MOV [SI], AL
06: ADD AL, 10h
07: INC SI
08: LOOP Loop_label
```

Watch point:

Answer: SI = 307h

AL = 80

56. Given a code snippet

```
if (a >= 0 && a <= 9)
        x = a + 30h;
else if (a >= 10 && a <= 15)
        x = a + 55;
```

The logic of the above code snippet in assembly is (with missing lines):

```
01:     CMP DL, 0
02:     ----------; possibly missing code
03: CMP DL, 9
04:     ----------; possibly missing code
05:     ADD DL, 30h
06:     ----------; possibly missing code
a_lable:
```

08: CMP DL, 0Fh

09: ----------; possibly missing code

10: ADD DL, 55

x_label:

12: MOV AL, DL

…

Choose correct missing instructions in the above sequence of instructions

Answer: 02: JB x_Label

04: JA x_Label

06: JMP x_Label

09: JA x_Label

57. In multiplication instruction, when the value of source operand is 12 (decimal), the other operand is loaded in AX. Which registers can be used to load source operand? Select one or more:

Answer: DX

BX

58. The instruction that subtracts 1 from the contents of the specifiled register/memory location is

Answer: DEC

59. Which are correct input for XLAT instruction. Select one or more:

Answer: DS:[BX] pointed to look-up table

look-up index must be loaded into AL

60. Major structural components of the CPU include:

Select one or more:

Answer: Arthmetic and Logic Unit

Interconnections

Registers

Control Unit

61. Basic functions that a computer can perform including:

Select one or more:

Answer: Data processing

Data movement

Control

Data storage

62. The instruction, MOV AX, 1234h is an example of

Answer: **Immediate addressing mode**

63. What is the correct sequence of instruction cycle?

Answer: **Step 1: Fetch opcode (Fetch instruction) (aka – pre – fetch)**

Step 2: Decode

Step 3: Calculate operand address (evaluate address) (address generation)

Step 4: Fetch operand (read memory data)

Step 5: Execution (ALU access)

Step 6: Store result (write back memory data)

64. Which one best describe cache hit and cache miss?

Answer: **Cache miss ratio: the number of memory accesses that CPU must retrieve from the main memory per the total number of memory accesses**

Cache hit ratio: the number of memory accesses that the CPU can retrieve from the cache per the total number of memory accesses

65. For cache write policies, which are often used for writehit and writemiss

Answer: **Write-hit: Write-back**

Write-miss: Write-allocate

66. Choose correct features for SRAM and DRAM

Answer: **DRAM: Slower access time, cheaper cost per bit, can manufacture with large size**

SRAM: Faster access time, cost more per bit, smaller size

67. Identify the correct sequence to update a page onto a flash memory?

Answer: **Step 1: the entire block is being read from flash into RAM then request data in page is update**

Step 2: the entire block of flash memory are erased

Step 3: the entire block from RAM then is written back to the flash memory

68. Choose correct set of registers for x86 processor

Answer: **Data pointer to source memory in extra segment ES: SI**

Pointer to variable in stack SS: BP

Instruction pointer CS: IP

Data pointer in data segment DS: BX

69. Match the definition of flag bits in PSW

Answer: Contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation: CF

Determine the direction for moving or comparing data between memory areas: DF

Determine whether an external interrupts are to be ignored or processed: IF

The processor switches to singlestep mode: TF

70. What are components of Von Neumann, namely IAS computer?

Answer: Memory

CPU

Bus

I/O Equipments

71. Which is not correct about MOORE law?

Answer: The number of transistors that could be put on a single chip was triple every year nowadays

Likely triple after 2000

72. For better speed, in CPU design, engineers make use of the following techniques:

Answer: Branch prediction

Pipelining

Speculative execution

73. To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?

Answer: Make wider data bus path

Make use of both onchip and offchip cache memory

Using higherspeed bus and us hierarchy

74. What is the meaning of Amdahl's law in processor performance evaluation?

Answer: The potential speedup of a program using multiple processor compared to a single processor

75. What are the processor's instruction categories?

Answer: Data processing

Control

Processor I/O

Processor Memory

76. Bus is a shared transmission medium, multiple devices connect to it buy only one at a time can successfully transmit. Which component in computer facilitates this operation?

Answer: Bus Arbiter

77. When many devices of different tranmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this:

Answer: MultipleBus hierarchies

78. What are the features of directmapping cache organization?

Answer: Thrash > low hit ratio

Simple and inexpensive

79. Which ones are not correct for static RAM?

Answer: Faster than dynamic RAM because they are made from capacitor

Cheaper than dynamic RAM because simpler chip controller

Cost per bit is lower than dynamic RAM

80. Which one is not correct?

Answer: EEPROM is erasable by exposing under UV

EPROM is erasable electrically

Flash memory can only be erased electrically byte by byte

81. Which statements are correct for HDDs?

Answer: Bits are stored on tracks

Head, Track, Sector are key parameters for access data on hard disk

82. What is correct about the function of TRIM command in SSD?

Answer: Allow OS to notify SSD the presence of occupied blocks of data which are no longer in use and can be erased internally

83. Which set of registers are valid for addressing a memory location?

Answer: DS:SI

DS:BX

CS:IP

84. Which are valid based index addressing?

Answer: [BX+SI]

[BX+DI]

85. Which are valid index addressing?

Answer: [SI]

[BX]

[BP]

86. 8088 is 16 bit processor, the maximum addressable memory is:

Answer: 1024K

87. Which are correct about the Pointer registers of IA-32 processors:

Select one or more:

Answer: Stark Pointer (ESP): The 32 bit pointer to the top of stark

Base Pointer (EBP): The 32 bit pointer refers to stark memory

Instruction Pointer (EIP): The 32 bit register points to the next instruction to be excute

88. Which are correct about the Data registers of IA32 processors:

Select one or more:

Answer: Lower halves of the 16-registers can be used as 8-bit data registers: AH, AL, BH, BL, CH, CL, DH, DL

Complete 32-bit registers: EAX, EBX, ECX, EDX

Lower halves of the 32-registers can be used as 4 16-bit data registers: AX, BX, CX, DX

89. Which are correct about 32 bit Index registers of IA32 processors:

Answer: EDI: 32 bit pointer to destination memory in data movement instructions

DI: 16 bit pointer to destination memory in data movement instructions

SI: 16 bit pointer to source memory in data movement instructions

ESI: 32 bit pointer to source memory in data movement instructions

90. Which statement is correct about interrupt vector table?

Answer: Take up 1024 bytes in the main memory

Store in the beginning area of the main memory

91. Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of DX register follows the execution of MOV DX, [1D4D] is 127B. What is the endian type of this computer system?

Answer: bigendian

92. Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of BX register follows the execution of MOV BX, [1D49] is F57F. What is the endian type of this computer system?

Answer: littleendian

93. Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction MOV AX, [1D4B] executed

Answer: 5A2D

94. Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of EAX follow the execution of this code

```
MOV   BX, 1D4C
MOV   EAX, [BX]
```

Answer: 125A

95. Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of SP register is 1D48. What is the value of SI follows the execution of POP SI

Answer: 1D48

96. Part of memory as shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of PUSH SI

Answer: 1D4E

97. The value in CS is 1FD0h what is the location of next instruction from 00000h if instruction pointer is 3CD4h

Answer: 3CD5H *(chưa chắc)*

98. Select correct items to describe best about CISC

Answer: Number of clocks per instruction: multiclock

Code size of program: small code size

Assembly code: simpler

Instruction set: complex

Bytes per instruction: different for variety of instructions

99. What best describe the Spatial and Temporal Locality?

Answer: Temporal locality: be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy

Spatial locality: be exploited by using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic

100. The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left

Answer: Temporal locality: the tendency for a processor to access memory locations that have been used recently

Spatial locality: the tendency of execution to involve a number of memory locations the are clustered

tendency to use large cache and prefetch mechanism

101. What can be concluded from the following chart of processor trends:

Cho hình vẽ biểu đồ có Transistors, Frequency, Power, Cores từ năm 1970 – 2010

Answer: The multi-core processors and level off clock speed help to make heat dissipation of CPU chip less

102. To evaluate processor performance, the following indicators and formulas are used:

Đề cho công thức của Cycles per instruction (CPI), Time to execute a program (T = Ic x CPI x t Or T = Ic x [p + (m x k) x t]) In which p:…, m:…, k:…, t:...

Which of the following system attributes affects Ic (the number of instructions of a program)

Answer: Instruction set architecture

Compiler technology

103. To evaluate processor performance, the following indicators and formulas are used:

Đề cho công thức của Cycles per instruction (CPI), Time to execute a program (T = Ic x CPI x t Or T = Ic x [p + (m x k) x t]) In which p:…, m:…, k:…, t:...

Which of the following system attributes affects cycle time t

Answer: Processor implementation

Cache and memory hierarchy

104. Key parameters to consider when evaluating processor hardware include:

Answer: **reliability**

performance

power consumption

size

cost

105. A memory chip has 12 address pins, determine the maximum memory words of this chip?

Answer: 4096

106. Which of the following best describe the memory chip with pinout as shown below:

Đề cho hình thanh ghi TMS4464

Answer: DRAM 64Kx4bit

107. Choose the correct structure of memory chip as shown below

Đề cho hình thanh ghi TMS4016

Answer: SRAM 2Kx8bit

108. The three key characteristics of memory are: capacity, access time and cost. Which of the following relationships hold for a variety of memory technologies?

Answer: **Faster access time, greater cost per bit**

Greater capacity, smaller cost per bit

Greater capacity, slower access time

109. A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines?

Answer: **15 address pins, 8 data pins**

110. In the interconnection system, the number of address lines are governs by

Answer: CPU

111. For memory hierarchy below, which relationship hold when moving downward

Đề cho hình cái tháp (mặt trái 3 tầng, mặt phải 5 tầng)

Answer: **Increasing access time**

Decreasing cost per bit

Decreasing frequency of access by the processor

Increasing capacity

112. Identified correct addressing mode of the following instructions?

Answer: **MOV AX, BX: Register**

MOV BP, [BX+SI]: Base plus index

MOV AX, ARRAY [BX+SI]: Base relative plus index

MOV AX, [BX]: Register indirect

MOV AX,[1234h]: Direct

MOV AX, 3540h: Immediate

113. Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs

Đề cho cái hình gồm Instruction Type, Instruction Count (millions), Cycles Per Instruction

Determine the effective, CPI, MIPS rate and execution time for each machine.

Answer: **CPI_b: 1.92**

CPU Time_a: 0.2

CPU Time_b: 0.23

CPI_a: 2.22

MIPs_b: 104

MIPs_a: 90

114. Choose correct RAID volume definitions for a request 2T storage.

Answer: **RAID 1 Mirror volume: 2 x 2T HDDs are needed, no data lost when th primary storage fails**

Spanned Volume: 2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails

RAID 0 Striped volume: 2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails

RAID5 Volume: At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time

115. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 30% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor?

Answer: 23%

116. Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB, the average seek time is 10.2 ms and the drive

rotates at 3600 rpm. What is average access time. Given: Rotational delay = 1/(2r), where r is the rotational speed in revolutions per second

Answer: 16.3 – ms

117. Select the correct sequence of instruction to compete -1024/128 (all values are in hex)

Answer: Step 1: MOV AX, FC00
Step 2: CWD
Step 3: MOV CX, 80
Step 4: IDIV CX

118. The instruction that loads the AH register with the lower byte of the flag register is

Answer: LAFH

119. Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system:

Answer: Access time: transfer time
Rotational delay: time for the sector in the request track to reach the head
Seek time: time for the head to settle at the request track

120. In multiplication instruction, when the source operand is 8 bit, _____ will be multiplied with source

Answer: AL

121. Structural components of computer include:

Answer: Memory
Syetem interconnection
I/O
Central processing unit

122. Which is correct about dual-layer DVD?

Answer: DVD drives has double laser head for reading from or writing to this disk