ĐỀ LẺ
1/ CF=1, OF=1
2/ DVD drives has double laser head for reading from or writing to this disk
3/ Pineline architeture, Branch prediction, Speculative execution
4/ 10h,01h,10h,01h
5/ 5MB/s
6/ Seek Time = time for the head to settle at the request track, Rotational delay = time for the sector in the request track to reach the head, Access time = access time + settle time
7/ Increase DI by 2, Load 16-bit value at memory location pointed by ES:[DI] into AX
8 / introducing cache memory
9/Increasing access time, Decreasing cost per bit, Decreasing frequency of access by the processor, Increasing capacity
10/ MOV DS, B800h - MOV SP,SS:[SI+2]
11/ 1111 1111 1011 0101
12/ Temporal locality = the tendency for a processor to access memory locations that have been used recently; Spatial locality = the tendency of execution to involve a number of memory locations that are clustered = tendency to use large cache and prefetch mechanism
13/faster than dynamic RAM because they are made from capacitor, Cheaper than dynamic RAM because simpler chip controller, Cost per bit is lower than dynamic RAM
14/ MOV AX, [BX+SP] ; MOV AX, [SP+1]
15/ I/O, Memory, System interconnection, Central processing unit
16/ 4096
17/ 262.144 MB
18/ DRAM = Slower access time, cheaper cost per bit, can manufacture with larger size, SRAM = Faster access time, cost more per bit, smaller size
19/ AX = 0040, CX = 0010, DX =0000
20/ Bits are stored on tracks; Head, Track, Sector are key parameters for access data on hard disk
21/ DS:[BX] pointed to look-up table, Look-up index must be loaded into AL
22/ SI=307h, AL=80h
23/ Cache and memory hierarchy, Processor implementation
24/ XOR
25/ AL
26/ MOV AX,166-MOV CL,2-SHR AX,CL-MOV BX,AX-??-ADD AX,BX
27/ 3DD00000
28/ LAFH
29/ OF = set, CF = set
30/ESI, SI, EDI, DI
31/ Step 1: MOV AX,FC00; Step 2: CWD; Step 3: MOV CX, 80; Step 4: IDIV CX
32/ 25.80645161
33/ Fetch opcode, decode, Calculate operand address, Fetch operand, Execution, Store result
34/ -728.25
35/ E9
36/ 1024K
37/ 28
38/ subtracting
39/ 0.003875
40/ 5A2D
41/ Digital logic level, Microarchitecture level, Instruction set level, Operating system level, Assembly Language level, High level programming language, Applications
42/ 1D4E
43/ SRAM 2Kx8bit
44/ 12
45/ RAID 1 Mirror volume: 2 x 2T HDDs are needed, no data lost when th
primary storage fails; Spanned Volume: 2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails; RAID 0 Striped volume: 2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails; RAID5 Volume: At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time

ĐỀ CHẴN

1/ Cheaper than dynamic RAM because simpler chip controller , Cost per bit is higher than dynamic RAM, faster than dynamic RAM because they are made from capacitor

2/ indicates the result of an arithmetic or comparison operation = CF, contains the carry from bit 3 to bit 4 following an arithmetic operation =AF, indicates the overflow of leftmost bit of data after an arithmetic operation =OF, shows the sign of the result of an arithmetic operation = SF

3/ AX=0200,CX=0010,DX=0000

4/ Processor implementation, Instruction set architecture

5/

6/ 0.2109375

7/ Arthmetic and Logic Unit, Interconnections, Registers, Control Unit

8/ 728.875

9/ DS:[BX] pointed to look-up table, look-up index must be loaded into AL

10/ 25.80645161

11/AL=73, AH=20

12/ Take up 1024 bytes in the main memory, Store in the beginning area of the main memory

13/ MOV AX, E799 - CDW - MOV BX, 012C - IDIV BX - AX=FFEC - DX=FF09

14/Increasing access time, Decreasing cost per bit, Decreasing frequency of access by the processor, Increasing capacity

15/ B,C

16/ Fetch opcode, decode, Calculate operand address, Fetch operand, Execution, Store result

17/ 4096

18/ D

19/

20/

21/ OF=0,CF=0

22/ SSB

23/ decrements by 4

24/ -12.0

25/ CF=OF=set

26/ 15 address pins, 8 data pins

27/ SI = 307h, AL = 80h

28/ subtracting

29/ OF=reset, CF=reset

30/ 28

31/ 16

32/ little-endian

33/ OF = set, CF = set

34/ 1D4A

35/ I/O, Memory, System interconnection, Central processing unit

36/ Bus Arbiter

37/ Seek Time = time for the head to settle at the request track, Rotational delay = time for the sector in the request track to reach the head, Access time = seek time + rotional delay

38/ DS:BX, DS:SI, CS:IP

39/ 262.144 MB

40/ 256 bytes (2^(16-8))

41/ Temporal locality = the tendency for a processor to access memory locations that have been used recently; Spatial locality = the tendency of execution to involve a number of memory locations that are clustered = tendency to use large cache and prefetch mechanism

42/ C2B27800

43/ Introducing cache memory

44/ CF = set, AL=0A

45/

ĐỀ CHUNG

1/ 41h,38h,55h,0FFh
2/ 1776,1942,485
3/intersegment mode
4/System interconnection, Central processing unit, I/O, Memory
5/ register, memory location
6/intersegment jump, far jump
7/
8/ mov cx, 10 - a_label: ..... - dec cx - cmp cx,0 - jz a_label
9/ AX=FFD0, CX=FFFF, DX=002F
10/ F8
11/decrements by 4
12/ A, D
13/REP
14/ 80h
15/ C2B27800
16/
17/DEC
18/
19/the potential speedup of a program using multiple processor compared to a single processor
20/ Increase SI by 2, Load 16-bit value at memory location pointed by DS:[SI] into AX
21/MultipleBus hierarchies
22/subtracting
23/ Make wider data bus path, Make use of both onchip and offchip cache memory, Using higherspeed bus and us hierarchy
24/ AX = 41BE, DX = 00FF
25/ carry flag is pushed into MSB then LSB is pushed into carry flag
26/ register, immediate data, memory location
27/-9.83913471531*10^-18
28/ Watch point #1: AL = 6C, Watch point #2: AH = 25
29/ decrease DI by 2, compare the value in AX register with 16-bit value at the memory location pointed by ES:[DI] and set/clear flag bits accordingly
30/ SI = 307h, AL = 80h
31/ Step 1: MOV AX, FC00 - Step 2: CWD - Step 3: MOV CX, 80 - Step 4: IDIV CX
32/ Carry flag = set, AL = 0A
33/ A
34/ increments by 4
35/ 1111111110111111
36/ MOV DS, B800h - MOV SP, SS:[SI+2]
37/ OF = set, CF = set
38/ Arthmetic and Logic Unit, Interconnections, Registers, Control Unit
39/262.144 MB
40/ Temporal locality: be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy , Spatial locality: be exploited by using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic
41/ A,B
42/ DAS