1/ Assembly

- MOV AX, 67FE - MOV BX, AX - MOV CL, BH - MOV CH, BL ➔ CX = FE67, BX = 67FE
- MOV EAX, 12AE - SUB EAX, 12AF ➔ Sign flag = set, Zero flag (OF) = reset, Carry flag (CF) = set
- MOV AX, 140h - MOV CX, 8h - MUL CX ➔ CF = reset, OF = reset
- MOV AX, 30 - MOV CX, FFFF - MUL CX ➔ CX = FFFF, AX = FFD0, DX = 002F
- MOV DL,FF - MOV AL, 42 - IMUL DL ➔ AX = 41BE, DX = 00FF
- MOV AL,78 - MOV BL,2 - MUL BL ➔ Carry flag (CF) = set, Overflow flag (OF) = no
- MOV AX, 152D - ADD AX, 003F - Watch point #1: ADD AH, 10 - Watch point #2 ➔ Watch point #1: AL = 6C, Watch point #2: AH = 25
- MOV DX, [SI] - MOV CX, [SI+2] ➔ DX = D096, CX = D0E0
- MOV BL, 8C - MOV AL, 7E - ADD AL, BL - Watch point #1 ➔ Carry flag = set, AL = 0A
- MOV AX, Val – MOV BX, AX – SHL AX,2 – ADD AX, BX – SHL BX,3 – SUB AX,BX ➔ -3val
- MOV AL, 0F - ADD AL, F1 ➔ OF = set, CF = set

- What will be the value of the destination operand after each of the following instructions execute in sequenceMov edx, var4 – Movzx edx, var2 – Mov edx, [var4+4] – Movsx edx, var1 ➔ 00000001h, 00001000h, 00000002h, FFFFFFFCh
- What is the correct value of SI, AL(in HEX) at Watch point: 01: MOV SI, 300h - 02: MOV AL, 10h - 03: MOV CX, 7 - 04: Loop_label: - 05: MOV [SI], AL - 06: ADD AL, 10h - 07: INC SI - 08: LOOP Loop_label==>SI = 307h, AL = 80
- What is the correct value of flag bits at Watch point ➔ OF = set, CF = set

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- Which of the following instructions are not legal addressing? ➔ MOV AX, [BX+SP] - MOV AX, [SP+1]
- Which set of registers are valid for addressing a memory location? ➔ DS:SI, DS:BX, CS:IP
- Which are valid based index addressing? ➔ [BX+SI], [BX+DI]
- Which are valid index addressing? ➔ [SI], [BX], [BP]

- Select the correct sequence of instruction to compete -1024/128 (all values are in hex)➔ Step 1: MOV AX, FC00 - Step 2: CWD - Step 3: MOV CX, 80 - Step 4: IDIV CX
- Select correct sequence of instructions to add words at [SI] and [DI] then store the sum at memory location 12A ==> Step 1: MOV AX, [SI] - Step 2: ADD [SI], [DI] - Step 3: MOV BX, 012A - Step 4: MOV [BX], AX

- Given a code snippet. The logic of the above code snippet in assembly is (with missing lines): ==> 01: CMP DL,0 - 02: JB x_Label - 03:CMP DL,9 - 04: JA x_Label - 05:ADD DL,30h - 06: JMP x_Label - 08:CMP DL, 0Fh - 09: JA x_Label - 10:ADD DL, 55 - 12:MOV AL,DL
- Given a code snippet. What is the equipvalent logic sequence of instruction in Assembly➔ cmp ax,bx – jl a_label – sub ax,bx – jmp x_label – a_label: - sub bx,ax – x_label:
- Given a code snippet: Which ones are the equivalent logic sequence of instructions in Assembly ➔ mov cx, 10 - a_label: ..... - dec cx - cmp cx,0 - jz a_label
- Given an assembly code copying the memory buffer Buff1 to Buff2 ➔ CLD REP MOVSB, LOOP CLD cp_loop: MOVSB LOOP cp_loop

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- Write a logical shift intruction that divies EBX by 4 ➔ shr ebx, 2
- Write instructions that jump to label L1 when the unsigned integer in DX is less than or equal to the integer in CX➔ cmp dx,cx / jbe L1

- A system programmer needs to divide -6247 by 300 ➔ Step 1: MOV AX, E799 - Step 2: CDW - Step 3: MOV BX, 012C - Step 4: IDIV BX➔ AX = FFEC, DX = FF09
- Identified correct addressing mode of the following instructions? ➔ MOV AX, BX: Register - MOV BP, [BX+SI]: Base plus index - MOV AX, ARRAY [BX+SI]: Base relative plus index - MOV AX, [BX]: Register indirect - MOV AX,[1234h]: Direct - MOV AX, 3540h: Immediate

- Var3: 1,2,7,2,1,3
- Implement the following pseudocode in assembly language➔cmp ebx,ecx ; ja L1; cmp ebx,val1; ja L1; mov X,2; jmp next; L1: mov X,1; next

2/ Use _____ instructions

- To isolate one or more bits in a byte value ➔AND
- To clear one or more bits in a byte value➔ AND
- To encrypt a byte value ➔XOR
- To set one or more bits in a byte valye➔OR
- To test one bit in a byte value without destructing (non – destructive) the byte ➔ TEST
- To test one bit in a byte value which can be destructive ➔ AND

3/ Convert the 8bit floating point number (số đề cho) (in hex) to decimal

- 57 = 5.75, E7 = -11.5, 68 = 12, 26 = 0.6875, d3 = -4.75, 1a = 0.40625. e8 = -12.0 , 3b = 1.6875

4/ Convert the 32bit floating point number (số đề cho) (in hex) to decimal

- C4361000 = 44361000 = 728.25, be580000 = -0.2109375, a3358000 = -9.83913471531*10^-18, 76650000 = 1.16116794981*10^33, 3E580000=0.2109375

5/ Convert (số đề cho) to IEEE 32-bit floating point format (1 sign + 8 exponent + 23 mantissa) in hex

- -89.2345 = C2B27800, 39887.5625 = 471BCF90, 0.1015625 = 3DD00000, -1313.3125 = c4a42a00

6/ Which are correct action for (đề cho) string operation if DF is reset (=0)

- LODSB ➔ Increase SI by 1, Load 8-bit value at memory location pointed by DS:[SI] into AL
- LODSW➔ Increase SI by 2, Load 16-bit value at memory location pointed by DS:[SI] into AX
- STOSB ➔ Increase DI by 1, Store 8-bit value from AL into memory location pointed by ES:[DI]
- SCASW ➔ Increase DI by 2, Compare value in AL register with memory location pointed by ES:[DI] (=0)
- SCASW ➔ Decrease DI by 2, compare the value in AX register with 16-bit value at the memory location pointed by ES:[DI] and set/clear flag bits accordingly (=1)

7/ Part of memory as shown in figure

- The value of DX register follows the execution of MOV DX, [1D4D] is 127B. ➔ big-endian
- The value of BX register follows the execution of MOV BX, [1D49] is F57F ➔ little-endian
- The value of SP register is 1D48. What is the value of SP follows the execution of POP SI ➔ 1D48
- The value of SP register is 1D50. What is the value of SP follows the execution of PUSH SI➔1D4E
- What is the value of AX register after instruction MOV AX, [1D4B] executed ➔ 5A2D
- What is the value of EAX follow the execution of this code MOV BX, 1D4C-MOV EAX, [BX]➔125A

8/ Hình ảnh

- What can be concluded from the following chart of processor trends (biểu đồ)➔ The multi-core processors and level off clock speed help to make heat dissipation of CPU chip less
- Which of the following best describe the memory chip with pinout as shown below ➔ DRAM 64Kx4bit
- Which of the following system attributes affects Ic (the number of instructions of a program) ➔ Instruction set architecture, Compiler technology
- Which of the following system attributes affects cycle time t ➔ Processor implementation , Cache and memory hierarchy
- Choose the correct structure of memory chip as shown below➔ SRAM 2Kx8bit
- For memory hierarchy below, which relationship hold when moving downward (tháp)➔ Increasing access time, Decreasing cost per bit, Decreasing frequency of access by the processor, Increasing capacity
- Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz➔ CPI_b: 1.92, CPU Time_a: 0.2, CPU Time_b: 0.23, CPI_a: 2.22, MIPs_b: 104, MIPs_a: 90

9/Chuyển đổi

- Match the following hexadecimal numbers to octal➔E7 = 347, 6E = 156, A9 = 251
- Match the decimal value of the following 2's complement. ➔ 10010111 = -105, 11010110 = -42, 11010000 = -48
- Convert the following binary numbers to hexadecimal ➔ 10101001 = A9, 01101110 = 6E, 11100101 = E5, 11100111 = E7
- Compute the physical address of stack top if stack pointer is FFAE and stack segment located at 1DAE➔ 2DA8E
- Write mask byte (in hex) to clear the lower 4 bit of a byte value with AND instruction ➔F0

- Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit) ➔ 96
- Write mask byte (in hex) to set bit 6th, 4th of a byte value with OR instruction (LSB is the 1st bit) ➔ 50
- EAX now stored a 32bit IP address of a host. The network ID (netID) is 20 bit and can be extracted from IP byte anding with a 32bit mask. Write correct instruction to extract netID from EAX register. Note: Immediate value must be written in hex ➔ AND EAX, FFFFF000
- Physical address of the stack pointer is 2DA82, stack segment located at 1DAE. Computer the value of SP register? ➔ FFA2
- Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D ➔f 100 1FF 0D
- A memory chip has 12 address pins, determine the maximum memory words of this chip➔4096
- 8088 is 16 bit processor, the maximum addressable memory is ➔ 1024K
- For 8086 microprocessor, the stack segment may have a memory block of a maximum of➔64KB
- The value in CS is 1FD0h what is the location of next instruction from 00000h if instruction pointer is 3CD4h ➔ 3CD5H
- A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines? ➔ 15 address pins, 8 data pins

10/ Selection

- Which are correct input for XLAT instruction➔ DS:[BX] pointed to, look-up table look-up index must be loaded into AL
- Which of the following instruction is not valid ➔ MOV SP, SS:[SI+2] - MOV DS, B800h
- Which of the following is not a data copy/transfer instruction? ➔ DAS
- Which one best describe cache hit and cache miss? ➔Cache miss ratio: the number of memory accesses that CPU must retrieve from the main memory per the total number of memory accesses, Cache hit ratio: the number of memory accesses that the CPU can retrieve from the cache per the total number of memory accesses
- Which is not correct about MOORE law? ➔ The number of transistors that could be put on a single chip was triple every year nowadays, Likely triple after 2000
- Which ones are not correct for static RAM? ➔ Faster than dynamic RAM because they are made from capacitor, Cheaper than dynamic RAM because simpler chip controller, Cost per bit is lower than dynamic RAM
- Which one is not correct? ➔ EEPROM is erasable by exposing under UV EPROM is erasable electrically Flash memory can only be erased electrically byte by byte
- Which statements are correct for HDDs? ➔ Bits are stored on tracks - Head, Track, Sector are key parameters for access data on hard disk
- Which are correct about the Pointer registers of IA-32 processors ➔ Stark Pointer (ESP): The 32 bit pointer to the top of stark, Base Pointer (EBP): The 32 bit pointer refers to stark memory, Instruction Pointer (EIP): The 32 bit register points to the next instruction to be excute
- Which are correct about the Data registers of IA32 processors ➔ Lower halves of the 16-registers can be used as 8-bit data registers: AH, AL, BH, BL, CH, CL, DH, DL - Complete 32-bit registers: EAX, EBX, ECX, EDX - Lower halves of the 32-registers can be used as 4 16-bit data registers: AX, BX, CX, DX
- Which are correct about 32 bit Index registers of IA32 processors ➔ EDI: 32 bit pointer to destination memory in data movement instructions, DI: 16 bit pointer to destination memory in data movement instructions, SI: 16 bit pointer to source memory in data movement instructions, ESI: 32 bit pointer to source memory in data movement instructions
- Which statement is correct about interrupt vector table? ➔ Take up 1024 bytes in the main memory, Store in the beginning area of the main memory
- Which could be correct ones for the destination operand in a data movement instruction? ➔ Register, Memory location
- Which could be correct ones for the source operand in an instruction➔register, immediate data, memory location

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- What is the correct sequence of instruction cycle➔Step 1: Fetch - Step 2: Decode - Step 3: Calculate operand addresWWhics - Step 4: Fetch operand - Step 5: Execution - Step 6: Store result
- What are components of Von Neumann, namely IAS computer? ➔ Memory, CPU, Bus, I/O Equipments

- What are the processor's instruction categories? ➔ Data processing, Control Processor, I/O, Processor Memory
- What are the features of directmapping cache organization? Answer: Thrash > low hit ratio Simple and inexpensive
- What is correct about the function of TRIM command in SSD? ➔ Allow OS to notify SSD the presence of occupied blocks of data which are no longer in use and can be erased internally
- What is the meaning of Amdahl's law in processor performance evaluation? ➔ The potential speedup of a program using multiple processor compared to a single processor
- What best describe the Spatial and Temporal Locality? ➔ Temporal locality: be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy , Spatial locality: be exploited by using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic

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- Select correct items to describe best about CISC ➔ Number of clocks per instruction: multiclock, Code size of program: small code size, Assembly code: simpler, Instruction set: complex, Bytes per instruction: different for variety of instructions
- Select correct definition of seek time, rotational delay, access time, transfer time for hard drives with moveable-head system: ➔ Access time: transfer time - Rotational delay: time for the sector in the request track to reach the head - Seek time: time for the head to settle at the request track
- Select correct level for contemporary computer multilevel machine ➔ Digital logic level, Microarchitecture level, Instruction set level, Operating system level, Assembly Language level, High level programming language, Applications

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- Choose correct RAID volume definitions for a request 2T storage. ➔ RAID 1 Mirror volume: 2 x 2T HDDs are needed, no data lost when th primary storage fails - Spanned Volume: 2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails - RAID 0 Striped volume: 2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails - RAID5 Volume: At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time
- Choose correct features for SRAM and DRAM ➔DRAM: Slower access time, cheaper cost per bit, can manufacture with large size, SRAM: Faster access time, cost more per bit, smaller size
- Choose correct set of registers for x86 processor ➔ Data pointer to source memory in extra segment ES: SI, Pointer to variable in stack SS: BP, Instruction pointer CS: IP, Data pointer in data segment DS: BX

- Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 30% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor? ➔ 23%
- Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB, the average seek time is 10.2 ms and the drive rotates at 3600 rpm. What is average access time. Given: Rotational delay = 1/(2r), where r is the rotational speed in revolutions per second ➔16.3 – ms
- Consider a 16-bit microprocessor, with a 16-bit external data bus, driven by an 10-MHz input clock. What is the maximum data transfer rate across the bus that this microprocessor can sustain? ➔5MB/s
- Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity ➔ 262.144 MB
- Consider a single-level paging system with 12-bit virtual addresses, 24-bit physical addresses, and a 256 (28) byte page size. ➔ 0x400
- Consider the following paging memory system: There are 4 page table entries (with values of 0xC, 0x2, 0x8, 0x5 for entries 0…3, respectively). The physical memory is 128 bytes, with frames of 8 bytes each. What is the physical address (in hex) that corresponds to virtual address 0x03? ➔ 0x63
- Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table. ➔ P2 has the maximun performnace
- An 8-way set-associative cache is made up of 32 bit words, 4 words per line and 4096 sets, how big is the cache in Kbytes? ➔512

- A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. ➔16 bit
- Computer A has an overall CPI of 1.3 and can be run at a clock rate of 600MHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 750 Mhz. this program has exactly 100,000 instructions. How many instructions would the program? ➔ 65.000

- Major structural components of the CPU include➔Arthmetic and Logic Unit, Interconnections, Registers, Control Unit
- Structural components of computer include ➔ Memory, Syetem interconnection, I/O, Central processing unit.
- Basic functions that a computer can perform including➔Data processing, Data movement, Control, Data storage
- For cache write policies, which are often used for writehit and writemiss ➔ Write-hit: Write-back Write-miss: Write-allocate
- Identify the correct sequence to update a page onto a flash memory? ➔ Step 1: the entire block is being read from flash into RAM then request data in page is update, Step 2: the entire block of flash memory are erased, Step 3: the entire block from RAM then is written back to the flash memory
- Match the definition of flag bits in PSW ➔ Contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation: CF, Determine the direction for moving or comparing data between memory areas: DF, Determine whether an external interrupts are to be ignored or processed: IF, The processor switches to singlestep mode: TF
- Match the correct definition of flag bits in PSW ➔ indicates the result of an arithmetic or comparison operation = CF, contains the carry from bit 3 to bit 4 following an arithmetic operation =AF, indicates the overflow of leftmost bit of data after an arithmetic operation =OF, shows the sign of the result of an arithmetic operation = SF
- For better speed, in CPU design, engineers make use of the following techniques: ➔ Branch prediction, Pipelining, Speculative execution, Out of order execution, Cache memory, Multicore processors, Clock frequency, Instruction set architecture
- To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design? ➔ Make wider data bus path, Make use of both onchip and offchip cache memory, Using higherspeed bus and us hierarchy
- The principle of cache memory relies on key features: locality of reference which involves spatial and temporal locality. Match the definition to keywords on the left ➔ Temporal locality: the tendency for a processor to access memory locations that have been used recently, Spatial locality: the tendency of execution to involve a number of memory locations the are clustered tendency to use large cache and prefetch mechanism
- Key parameters to consider when evaluating processor hardware include ➔ reliability, performance, power consumption, size, cost
- The three key characteristics of memory are: capacity, access time and cost. Which of the following relationships hold for a variety of memory technologies? ➔ Faster access time, greater cost per bit - Greater capacity, smaller cost per bit - Greater capacity, slower access time

11/ Knowledge

- The instruction, JMP C008:2000h is an example of ➔ far jump, intersegmet jump
- The instruction, CMP to compare source and destination operands by ➔ subtracting
- The instruction, MOV AX, [3004h] is an example of ➔ dirrect addressing mode
- The instruction, MOV AX, 1234h is an example of ➔ Immediate addressing mode
- The instruction, MOV AX, 0005h belongs to which addressing mode ➔Immediate
- The instruction that is used to transfer the data from source operand to destination operand is ➔ data copy/transfer instruction
- The instructions that involve various string manipulation operations are ➔ string instructions
- The instruction that pushes the contents of the specified register/memory location on to the stack is ➔ PUSH
- The instructions that are used for reading an input port and writing an output port respectively are➔IN,OUT

- The instruction that is used for finding out the codes in case of code conversion problems is➔XLAT
- The instruction that loads effective address formed by destination operand into the specified source register is➔LEA
- The instruction that subtracts 1 from the contents of the specifiled register/memory location is ➔ DEC
- The instruction that loads the AH register with the lower byte of the flag register is ➔LAHF
- The instruction that enables subtraction with borrow is ➔ SBB
- The instruction that supports addition when carry exists is ➔ADC
- The instruction that adds contents of memory location specified in a register to the contents of a register is ➔ ADD
- the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is ➔REP
- The instructions that are used to call a subroutine from a main program and return to the main program after execution of called function are ➔ CALL,RET
- The instructions that are needed by the processor is stored in ➔ Memory
- The instruction that can affect stack pointer is ➔ random access memory or ram
- The flag that the instruction SBB uses is ➔carry flag
- The result of an IMUL instruction is 0060, what is the corect state of Carry flag and Overflow flag ➔ CF=0,OF=0
- The result of an IMUL instruction is FFA0, what is the corect state of Carry flag and Overflow flag➔CF=OF=1

- After each execution of PUSH instruction, the stack pointer is ➔ decrement by 2
- After each execution of POP instruction, the stack pointer is ➔ increment by 2
- After excuting PUSH EAX instruction, the stack pointer ➔decrements by 4
- After executing the POP EAX instruction, the stack pointer ➔ increments by 4

- In multiplication instruction, when the value of source operand is 12 (decimal), the other operand is loaded in AX. Which registers can be used to load source operand? ➔ DX, BX
- In multiplication instruction, when the source operand is 8 bit, ? will be multiplied with source➔ AL
- In multiplication instruction, the result is taken from AX means the source operand is bit ➔ 16
- In multiplication instruction, the upper half of the result is nonzero implies which state of Carry flag and Overflow flag? ➔ CF=1, OF=0
- In computer, how does the processor serve multiple interrupt request from devices? ➔ Each device are assigned an interrupt priority, the device with lower priority will be served
- In the interconnection system, the number of address lines are governs by ➔ CPU
- In the RCR instruction, the contents of the destination operand undergoes function as ➔carry flag is pushed into MSB then LSB is pushed into carry flag

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- When many devices of different tranmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this: ➔ MultipleBus hierarchies
- Which is correct about dual-layer DVD? ➔ DVD drives has double laser head for reading from or writing to this disk
- Physical address of the instruction pointer is 2040E, code segment located at 1FAF. Compute the value of IP register? ➔ 91E
- Bus is a shared transmission medium, multiple devices connect to it buy only one at a time can successfully transmit. Which component in computer facilitates this operation? ➔Bus Arbiter
- How many times the instruction blow will loop? ➔ 1
- if the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is called ➔ intersegment mode
- . The number of PUSH instructions and POP instructions in a subroutine must be ➔ both must be equal
- The stack segment register contains ➔ base address of the stack segment
- The stack pointer register contains ➔ offset of address of stack segment