Quan T. Mai

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Fayetteville, Arkansas, US https://quanmai.github.io

EDUCATION

University of Arkansas at Fayetteville, Arkansas, United States Spring 2020 - Present
PhD Student in Computer Engineering, CSCE Department

- Cumulative GPA (until present): 4.0/4.0

DaNang University of Science and Technology, DaNang, Viet Nam Aug 2011-June 2016
Bachelor of Science in Electronics Engineering, Faculty of Electronics and Telecommunication, the Center of Excellence

- Cumulative GPA: 3.44/4.0 (and 8.28/10)
- Senior Thesis: High speed Pseudo two-port memory developed on 28nm technology running at 1.5GHz with 0.9V power supply

RESEARCH INTERESTS

High Performance Computing
Deep Learning
Machine Learning
Graph Neural Networks and applications in solving routing problems

SKILLS

Programming languages: C++, Python, CUDA, DPC++
Working on HPC environment, Linux
Deep learning framework: Pytorch, Tensorflow

WORK EXPERIENCE

Graduate Intern, HPC Solution Architect, Intel Corporation Spring 2022-May 2022
Implemented a Molecular Dynamics sample using Intel OneAPI DPC++, running 10x faster than naive C++ implementation.

Research Assistant, Computer System Lab, CSCE, University of Arkansas Spring 2020-Fall 2021
Work under guidance of Dr. Miaoqing Huang on High Performance Computing projectts
Teaching Assistant, Algorithms, CSCE, University of Arkansas Fall 2020
Hold office hours weekly, grade assignments for CSCE4133-Algorithms lectured by Dr. Ukash Nakarmi
Teaching Assistant, Operating Systems, CSCE, University of Arkansas Spring 2021
Hold office hours weekly, grade assignments for CSCE3613-Operating Systems lectured by Dr. Lora Streeter
Lab Assistant, Programming Foundation II, CSCE, University of Arkansas Summer 2021
Hold office hours, taught students to program C++ for CSCE2014-PFII lectured by Dr. Lora Streeter
Teaching Assistant, Cloud Computing and Security, CSCE, University of Arkansas Fall 2021
Hold office hours weekly, grade assignments for CSCE4783-Cloud Computing and Security lectured by Dr. Miaoqing Huang

IP Design Engineer, eSilicon (now Synopsys), Danang City August 2016 - October 2019
Circuit design team, work major in developing high speed / ultra-high speed Pseudo two ports (P2P) SRAM on the cutting edge of process: 28nm, 14nm, 10nm, 7nm and 5nm technology

HONORS AND AWARDS

First prize, Sunflower Mission – Engineering & Technology Scholarship Winter 2015

PUBLICATIONS

Q. Mai, U. Nakarmi (2022), "BrainVGAE: End-to-end Graph Neural Networks for Autism Classification on ABIDE dataset using Variational Graph Auto-Encoder and Deep Domain Adaptation", under review

T. Kamucheka, **Q. Mai**, M. Huang, X. Liu (2021), "CuSMC: Fast Parallel Implementation for Sequential Monte-Carlo on GPU", under review; GitHub code: https://github.com/tkamucheka/CuSMC

M. D. Le, V. Singh Rathour, Q. S. Truong, **Q. Mai**, P. Brijesh and N. Le, "Multi-module Recurrent Convolutional Neural Network with Transformer Encoder for ECG Arrhythmia Classification," 2021 IEEE EMBS International Conference on Biomedical and Health Informatics (BHI), 2021, pp. 1-5, doi: 10.1109/BHI50953.2021.9508527