Optimization and Synthesis of Quantum Circuits with Global Gates

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Extended abstract

Physical realizations of quantum computers in the current era greatly vary in multiple, non-trivial aspects. A fundamental difference between two hardware realizations of a quantum computer can be the choice of implementation of their qubits. Current candidates for qubit implementations are superconducting circuits [10], trapped ions [7], nitrogen-vacancy centers [8], and neutral atoms [9], to name a few. Each choice of qubit implementation comes with distinct features that need to be considered when compiling and synthesizing circuits for a quantum computer based on it. For example, the connectivity between qubits in a superconducting quantum computer is limited to a connectivity graph that depends on a specific topology, while on a trapped ion quantum computer the connectivity is all-to-all. This all-to-all connectivity naturally gives us a special set of quantum gates to work with, in which we have access to powerful multi-qubit entangling gates that we refer to as *global* gates. If we have a quantum circuit described on an arbitrary gate set that we want to run on a trapped ion quantum computer, we need a way to synthesize it such that we take advantage of the global gates we have available. Recent advances [13] have shown that we can do quantum circuit synthesis with the ZX-calculus by restricting ourselves to a target gate set when doing a process called *circuit extraction*. In this work we aim to combine both ideas.

Contributions. We propose a method for converting any input quantum circuit into one using the gate set native to ion trap quantum platforms. Our synthesis algorithm is based on the ZX-calculus and consists of a circuit extraction procedure that outputs a circuit with global entangling gates and arbitrary single-qubit gates. In the process, we aim to minimize the number of global gates we generate, which are powerful but more costly than single-qubit operations. We develop a Python implementation of our algorithm and run benchmarks over different classes of quantum circuits.

We assume the native gate set of an ion trap quantum computer to be arbitrary single-qubit gates and global (sometimes referred to as multi-qubit) entangling gates [14, 2]. These global entangling gates consist of a set of 2-qubit Mølmer-Sørensen (MS) XX interactions between any subset of qubits in the system. We define the MS gate on qubits i and j as the matrix exponential $XX(\alpha)_{i,j} = e^{-i\frac{\alpha}{2}X_iX_j}$, for $\alpha \in [0, 2\pi)$ and X_iX_j the Pauli X on qubits i and j. Global MS (GMS) interactions are defined as

$$\mathrm{GMS}(\alpha)_S = \prod_{i<j\in S} XX(\alpha)_{i,j} \tag{1}$$

for $S \subseteq Q$ a subset of the available qubits. Note that we can (mostly) use global XX and ZZ gates interchangeably, since we can define $ZZ(\alpha)_{i,j} := H_iH_j\, XX(\alpha)_{i,j}\, H_iH_j$ and $\mathrm{GZZ}(\alpha)_S := H_S\ \mathrm{GMS}(\alpha)_S\, H_S$ where H_S denotes applying a Hadamard gate on all qubits in S.

Global entangling gates such as the GMS have been used to more efficiently synthesize layers of CNOT gates when the CNOTs are arranged in so-called *fanout* gates [12]. A fanout gate consists of a

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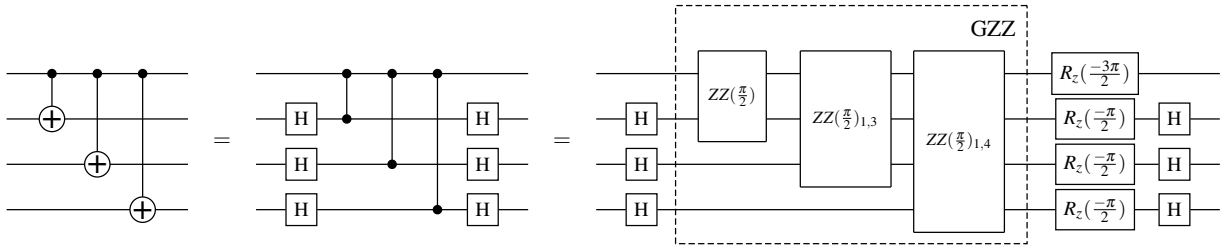
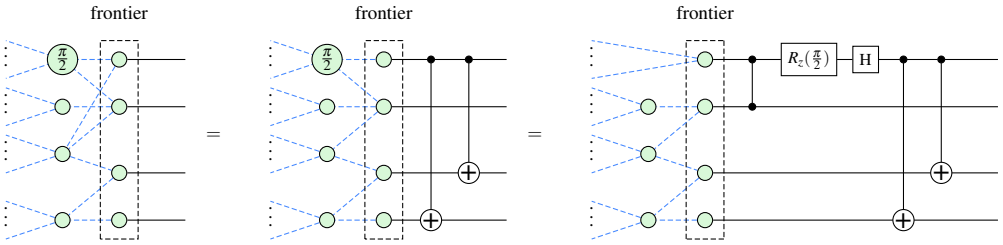


Figure 1: Implementing a fanout gate with one GZZ and single-qubit gates.

layer of CNOT gates that have a common control qubit, and can be implemented with just a single GZZ gate (see Figure 1) and some additional single-qubit gates. As we will see later, we can also potentially gather multiple fanout gates into the same GZZ gate. By extracting layers of CNOTs in the shape of fanout gates during the ZX-calculus circuit extraction process, we aim to gather as many CNOTs as we can into the least amount of global gates.

We are now going to briefly comment on how circuit optimization and extraction works in the ZX-calculus [1, 6], and how we use it to synthesize and optimize circuits with global gates. We omit here the basic definitions and equational rules of the ZX-calculus, which can be found in Appendix A, and explained thoroughly in Refs. [3, 16]. The ZX-calculus is a formal diagrammatic framework useful for reasoning about quantum mechanics [4] but also as a tool for circuit optimization [11, 1] and synthesis [5, 13]. The process of optimizing a circuit using the ZX-calculus usually involves transforming a quantum circuit as a ZX-diagram, rewriting the diagram in graph-like form and then applying a series of rewrite rules that decrease the size (number of vertices) of the diagram until they cannot be applied anymore [6]. Once this process is finished, we have a reduced ZX-diagram that implements the same unitary that we were given as a quantum circuit. To get a quantum circuit back, we are required to perform circuit extraction on our reduced ZX-diagram. Circuit extraction usually involves constructing a quantum circuit from right to left by iteratively extracting quantum gates from the "frontier" of the ZX-diagram. When we extract gates from the frontier, we progressively advance the frontier until reaching the end, which means that we have finished the extraction. For instance, two rounds of extraction in which we extract CNOT gates and then single-qubit gates and a CZ would look as follows (in which dashed blue lines represent edges with a Hadamard on them):



If we calculate the adjacency matrix M between the frontier vertices and their neighbours to the left at any given time, extracting a CNOT gate with control qubit i and target qubit j equates to performing the row operation $r_i \leftarrow r_i \oplus r_j$, for r_i, r_j rows in M and $\oplus$ addition modulo 2. These CNOTs can be added to the quantum circuit we are building as a Gaussian Elimination process until we make one or more frontier vertices have only one neighbour (equivalent to a row in M with all zero entries except for a

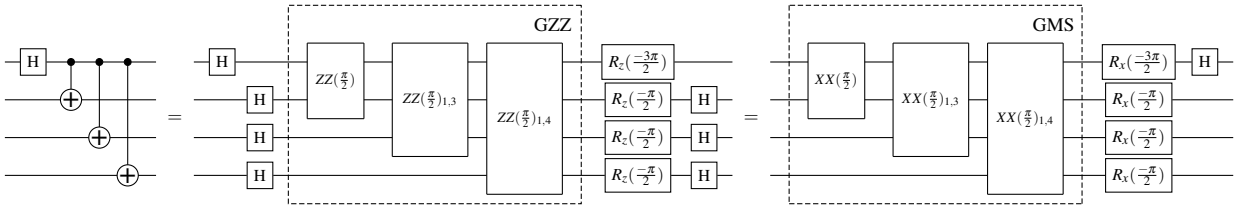


Figure 2: A better extraction of a fanout gate followed by a Hadamard.

single 1), in which case we can move the frontier vertex to the right, extracting a Hadamard gate with it unless it is the last vertex.

The main observation for our work is that the shape of the layer of CNOT gates we are extracting can be made into a sequence of fanout gates and that, under certain conditions that we will see later, some of these fanout gates can be put together into the same GMS gate. We make use of the fact that, once we extract a vertex after applying a fanout gate to the circuit, we will have a Hadamard in front of the fanout gate that we can commute through, resulting in the equations of Figure 2. If the extracted vertex is the last one on that row meaning that no Hadamard will be present, we can always add a redundancy of two Hadamards and commute one of them.

This gives us a series of $XX(\frac{\pi}{2})$ and $R_x(-\frac{\pi}{2})$ rotations and a Hadamard gate for each extracted vertex. The objective is to combine as many $XX(\frac{\pi}{2})$ rotations as possible that originate from different fanout gates into the least amount of GMS gates. We develop two algorithms to achieve this, which mostly differ in how vertices are chosen for extraction. Both algorithms are in the process of being implemented and tested against each other and other synthesis tools at the time of writing.

Algorithm 1: Max-vertices. Here we aim to maximize the number of vertices that we extract at once for each time we get a new frontier, while trying to fit their corresponding fanout gates in the least amount of GMS gates. The intuition behind it is that extracted single-qubit or CZ gates get in the way when creating GMS gates, so we try to minimize the number of times we extract anything that is not a GMS. Steps are as follows.

1. Calculate the biadjacency matrix between our current frontier and its neighbours, together with the fanout gates necessary to extract every vertex that can be extracted.

2. Construct the GMS by taking the vertices with the smallest (in the number of CNOTs) fanout gates that can fit into the same GMS. A fanout gate fits into the GMS we are currently constructing if the control qubit involved in the fanout has not been used yet, and the qubits used as targets have not been used yet or used only as targets in the previously added fanouts. If no fanouts fit in the GMS we are currently building, start building a new GMS.

3. Once decided which fanouts will get added to the GMS, we extract them together with the Hadamard gates that we will then commute as in Figure 2. Single-qubit R_x gates are also merged together whenever possible.

4. Extract single-qubit gates and CZ gates from the frontier, if any. Any qubit that had an R_z, Hadamard, or CZ gate extracted cannot be used anymore in the GMS that is currently being built, while qubits with extracted R_x gates can still be taken into account since we can commute the R_x through the XX rotations of the current GMS. If there are still extractable vertices go back to **Step 1**, otherwise we are done.

Algorithm 2: Greedy selection. The second algorithm works similarly to **Max-vertices**, with the difference that in **Step 2** we only extract the vertex with the smallest fanout gate that fits into the current GMS or create a new one if none of them fit. The motivation behind this is that early experiments show that sometimes we only need a single CNOT to extract a vertex, so there can be some advantage in moving the frontier as frequently as possible in search of vertices that only require one CNOT to be extracted.

With this work, we expand on the methods for quantum circuit synthesis with the ZX-calculus. The target hardware in mind is that of ion trap quantum computers, which are a promising technology due to their all-to-all connectivity between qubits, a property that not all quantum platforms based on other qubit implementations enjoy. We turn an input quantum circuit into a ZX-diagram and perform circuit optimization [6] on it. Then, we apply our synthesis algorithm directly on the reduced ZX-diagram. This algorithm also aims to minimize the number of global gates necessary to implement the original circuit. The entire process converts a circuit with an arbitrary gate set into one that uses GMS gates and arbitrary single-qubit unitaries.

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A ZX-calculus

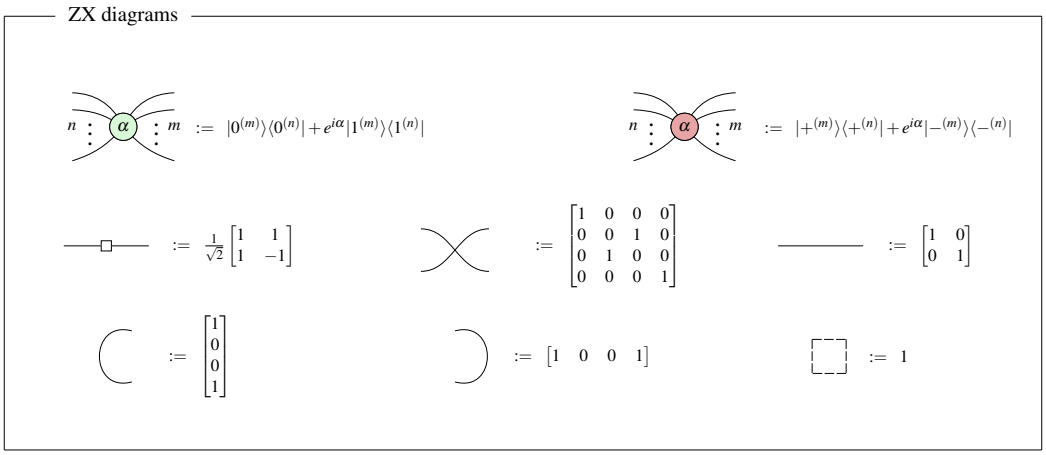

Figure 3: The generators of the ZX-calculus and their definitions, with $\alpha \in \mathbb{R}$ and $|x^{(n)}\rangle$ being shorthand for $|x\rangle \otimes \cdots \otimes |x\rangle$ done n times.

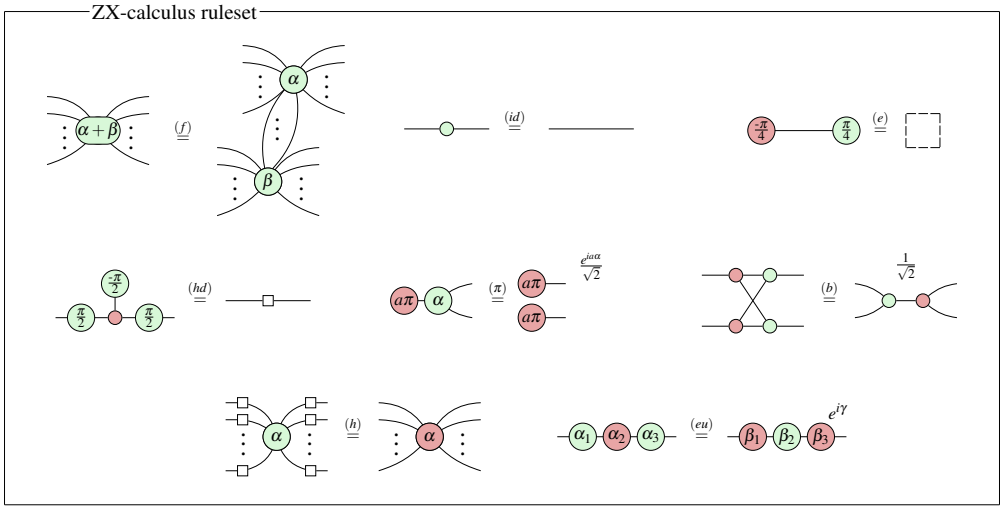

Figure 4: ZX-calculus ruleset. We omit the relationship between the phases in the (eu) rule. For more information we refer to [15].