Automated Synthesis of Fault Tolerant State Preparation Circuits for Quantum Error Correcting Codes

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I. OVERVIEW

Quantum bits and quantum operations suffer from unavoidable decoherence and noise. Therefore, quantum error correction mechanisms need to be used to ensure that quantum algorithms can be run in a fault tolerant way to control the accumulation of errors. Error correcting codes leverage redundancy by encoding quantum information in logical qubits, formed of entangled states of noisy, physical qubits.

Consequently, it is important that universal operations can be carried out on the encoded information in a fault tolerant way and that errors during the execution can be detected and corrected. A central ingredient in fault tolerant quantum algorithms is the initialization of a logical state for a given quantum error correcting code from a set of noisy qubits. In particular, for small code instances that are realizable on currently available hardware, non-deterministic schemes consisting of a generally non-fault tolerant preparation circuit and a verification circuit that checks for dangerous spreading errors have demonstrated promising results. However, known constructions are mostly done manually, and no algorithmic techniques exist for constructing depth- or gate-optimal circuits. Hence, current methods are explored for specific code instances and for the special case of distance 3 codes only.

In this work, we propose an algorithmic approach for the construction of fault tolerant state preparation circuits for arbitrary CSS codes. On the one hand, we rely on SAT techniques for obtaining provably optimal depth- or gate-optimal preparation and verification circuits. On the other hand, we show that the problem of finding a verification circuit for a given preparation circuit in such schemes is NP-complete for CSS codes in general and devise an efficient heuristic for generating said circuits. Based on these methods, we also generalize the non-deterministic state preparation scheme beyond distance 3 and numerically demonstrate that the generated circuits exhibit the desired logical error rates. We make an implementation of the proposed methods as a software tool publicly available as part of the Munich Quantum Toolkit (MQT) on GitHub.

II. MAIN TECHNICAL CONTRIBUTIONS

Intuitively, a requirement for fault tolerant circuits is that errors on single qubits cannot uncontrollably "spread" to multiple qubits, for instance, through CNOT gates. For *Calderbank-Shor-Steane* (CSS) codes, one way of initializing an encoded state fault tolerantly is to prepare all physical qubits in $|0\rangle$ or $|+\rangle$ and perform one round of error correction—projecting the product state onto the logical code space. Especially for smaller code instances that are relevant for near-to-midterm devices, this general procedure introduces a significant overhead in terms of circuit size since all stabilizer generators need to be measured multiple times.

An alternative scheme that tries to reduce the number of measurements needed is a non-deterministic protocol, based on post-selection [1–3]. Therein, initialization is performed in two steps:

1. Prepare the state using a non-fault tolerant state preparation circuit.
2. Conduct specific measurements on the prepared states using a so-called *verification circuit* that detects if an error spreads through the circuit. If any of these measurements measure a -1 eigenvalue, the state is discarded, and the procedure is restarted.

While this and related techniques were successfully demonstrated recently in experiment [2–9], there are two clear drawbacks to these previous approaches: First, these methods rely on manual construction, which is tedious and becomes infeasible when scaling to larger codes where both the set of dangerous errors and the possible verification measurements blow up. Moreover, as for the general scheme outlined above, there is no guarantee that these manually constructed circuits are gate- or depth-optimal. Second, these constructions have only been explored for specific code instances for small distance 3 (or 2) codes.

In general, constructing a verification circuit that ensures that the overall scheme is fault tolerant is highly non-trivial and depends on the code (and the logical state we want to prepare). The manual construction in existing works is thus not generally applicable. With ever-improving error rates on current devices, experimental demonstrations of higher distance codes might be possible with a verification-based scheme. For this, the construction needs to be generalized beyond distance 3, and

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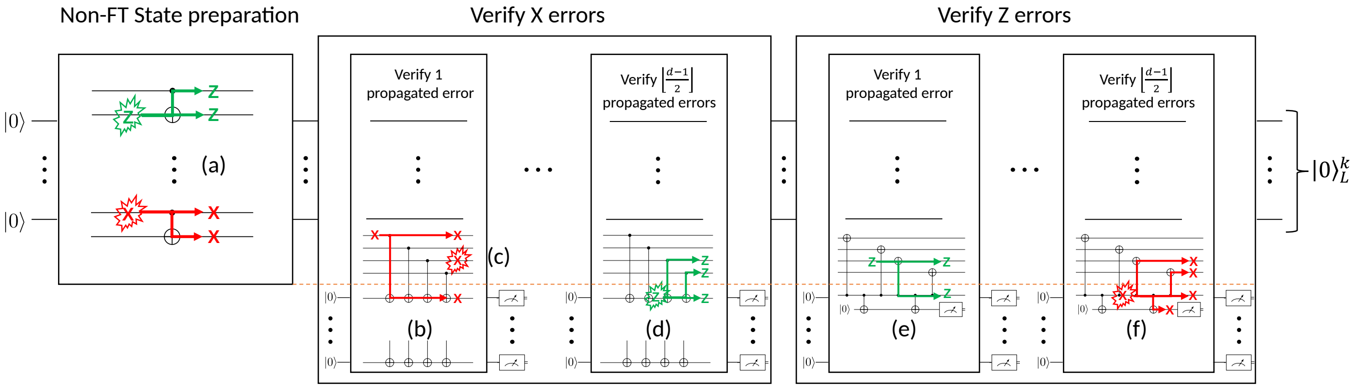

FIG. 1: Full fault tolerant state preparation protocol for CSS codes. A non-fault tolerant state preparation circuit is followed by a sequence of stabilizer measurements to check if any errors propagated through the circuit. If no measurement in the verification blocks indicates an error, the state is accepted. **(a)** Errors in the non-fault tolerant state preparation circuits propagate to higher-weight errors through CNOTs between data qubits. **(b)** If an error of at most weight i occurred in the state preparation circuit and propagated to a higher-weight error, measurements in the ith layer of the verification circuit detect this error. **(c)** Propagated errors are still detected by later layers of verification, even if further errors occur during a stabilizer measurement. **(d)** Z errors on the ancilla during the verification of X errors propagate to the data qubits. **(e)** If a Z error propagated through the non-FT state preparation circuit *or* the Z measurements of the previous verifications, it is later detected by flag fault tolerant measurements. **(f)** Propagated X errors on the X measurement ancillae are detected by flag qubit measurements.

algorithmic methods that can be applied to a broad range of codes must be developed.

In this work, we address these issues and propose methods for the automated construction of fault tolerant state preparation circuits. Our main contributions are as follows:

- For synthesizing *state preparation circuits* for CSS codes, we propose methods for constructing gate- or depth-optimal (non-fault tolerant) circuits. The synthesis problem is encoded into an SMT or SAT formula, which is solved by a reasoning engine to provide provably optimal circuits.

- Given the complexity of synthesizing optimal state preparation circuits, solving such instances comes at a high computational cost that becomes prohibitive for larger codes. Therefore, we also propose a heuristic algorithm for synthesizing state preparation circuits. Numerical evaluations show that this heuristic produces near-optimal state preparation circuits for smaller codes.

- For synthesizing *verification circuits* for a given state preparation circuit, we propose another SAT-solving-based method for synthesizing gate-optimal verification circuits.

- We also provide a heuristic synthesis method for synthesizing verification circuits using a variant of the classical greedy Set Cover algorithm.

- We furthermore generalize the post-selection scheme by solving multiple instances of the verification circuit synthesis problems and utilizing flag-fault tolerant measurement schemes to construct preparation circuits for higher-distance codes.

Our proposed generalized scheme is summarized in Figure 1. In short, our contributions can be viewed as providing optimal circuits for every sub-circuit depicted in Figure 1.

All proposed methods are made publicly available in the form of open-source software as part of the Munich Quantum Toolkit (MQT) [10] at https://github.com/cda-tum/mqt-qecc.

III. NUMERICAL STUDY

We use our methods to synthesize non-deterministic fault tolerant state preparation circuits for various CSS codes and provide numerical simulations of the constructed circuits under a circuit level noise model using Stim [11] to investigate the success rate and the logical error rates.

Figure 2 shows logical error and acceptance rates for various state preparation circuits for the logical $|0\rangle_L^k$ state of well-known $[\![n,k,d]\!]$ CSS codes and a depolarizing circuit-level noise model. The acceptance rate is the probability that a state will be accepted, i.e., all verification measurements yield a $+1$ eigenvalue.

To show the benefit of our method for constructing optimized fault tolerant state preparation circuits for distance 5 codes, we have also simulated state preparation with “naive” verification circuits where all stabilizer generators are measured twice—with flags if necessary.

To compare the impact on non-parallelizable two-qubit gates, we have simulated the circuits assuming maximum parallelism (all gates in one layer can be executed in parallel) and minimum parallelism (only one gate can be executed at a single time step). The latter case incurs more "idling" errors, which naturally leads to lower acceptance and higher logical error rates. The results of these simulations can be seen in Figure 3 for parallel gates and Figure 4 for non-parallel gates.

These results show that optimizing the proposed generalized non-deterministic fault tolerant state preparation scheme brings little to no benefit for higher distances if gates can be executed in parallel. This is due to the fact that even though the CNOT count of the optimized circuits is significantly lower, the depth of the optimized circuit is about as high as the depth of the naive verification circuit. The acceptance rate of the optimized circuit naturally scales much better. However, with physical error rates below $5 \cdot 10^{-4}$ where the larger codes exhibit better physical error rates, the difference in acceptance rate is negligible.

The improvement of the optimized circuits is drastic when all CNOTs have to be executed sequentially. In this case, the optimized scheme outperforms the naive one by orders of magnitude in logical error and acceptance rates.

These results show that optimized state preparation schemes are suited for quantum computing platforms with a lower degree of parallelism. The difference is less stark for architectures like neutral atoms, where two-qubit gates can be performed globally, assuming idling errors are manageable. For these systems, alternative schemes with a high degree of parallelism, like in the preparation of the Golay code [12], could be exploited.

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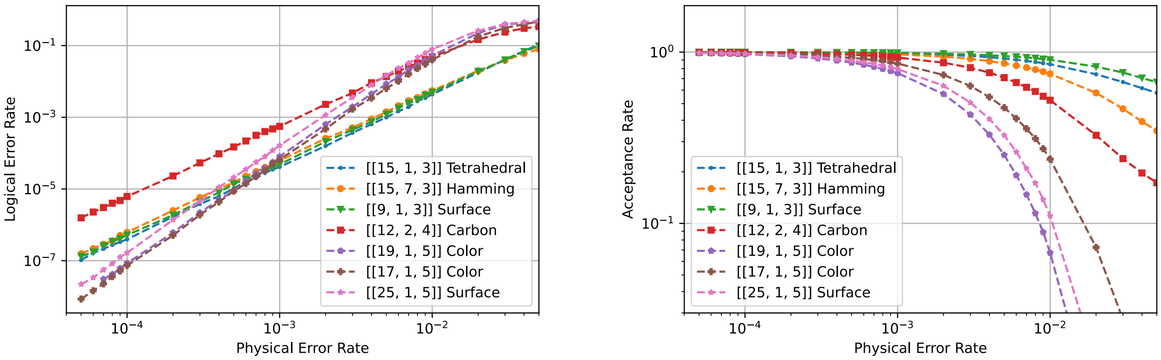

FIG. 2: Logical error rate and acceptance rate for non-deterministic fault tolerant state preparation circuits for the logical $|0\rangle_L^k$ state constructed with our methods for various $d = 3$ and $d = 5$ CSS codes under circuit-level depolarizing noise using a LUT decoder.

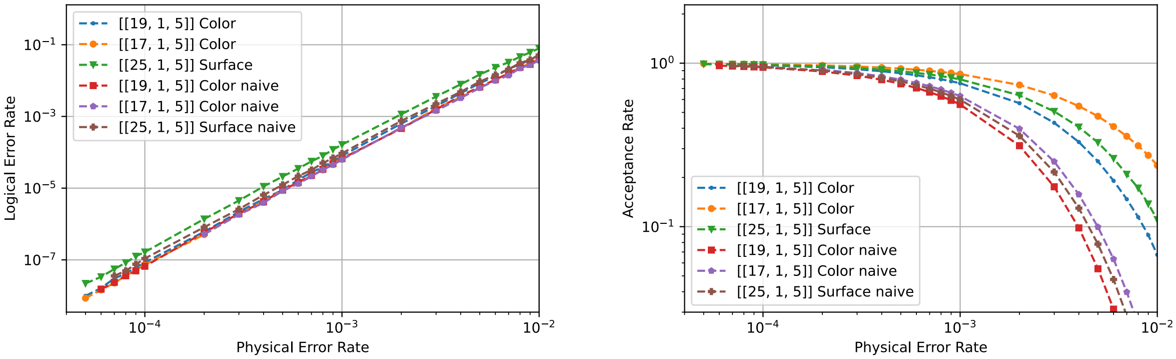

FIG. 3: Logical error rate and acceptance rate for non-deterministic fault tolerant state preparation circuits for the logical $|0\rangle_L$ state constructed with our methods for 2D color and surface codes with $d = 5$ under circuit-level depolarizing noise with parallel gate execution using a LUT decoder.

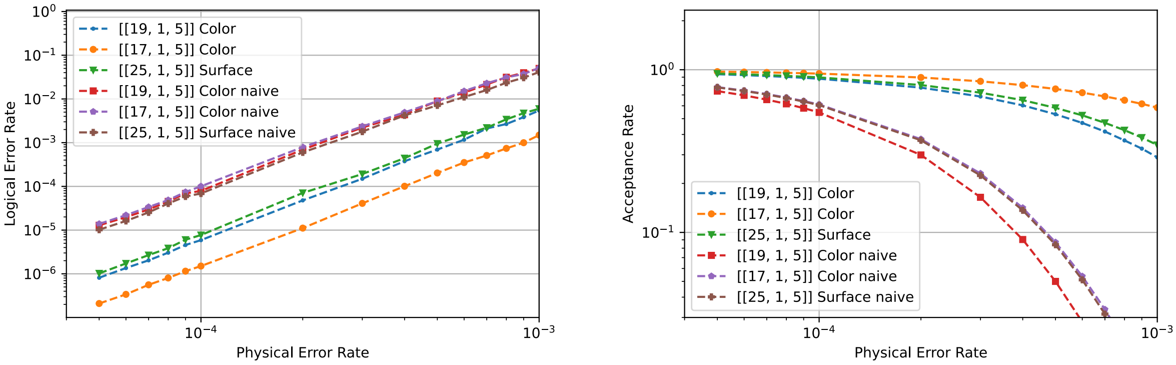

FIG. 4: Logical error rate and acceptance rate for non-deterministic fault tolerant state preparation circuits for the logical $|0\rangle_L$ state constructed with our methods for 2D color and surface codes with $d = 5$ under circuit-level depolarizing noise with sequential gate execution using a LUT decoder.