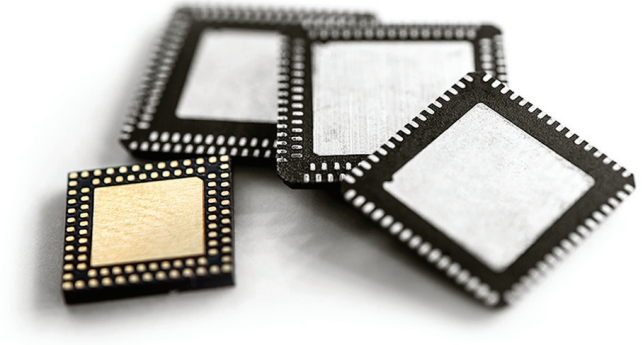
QFN

Quad Flat No-Lead Package

HIGHLIGHTS

- **Punch or Saw singulated formats**
- **Body sizes from 1.0 x 1.3mm to 12 x 12mm**
- **Pin counts from 4L to 156L**
- **Square or rectangular body sizes**
- **Leads on four sides of the body (QFN)**
- **Leads on two opposing sides of the body (DFN)**
- **Dual row lead design options**
- **Thin package thickness options**



FEATURES

- Body sizes: 1.0 x 1.3 to 12 x 12mm
- Lead pitch: 0.40, 0.50, 0.65 and 0.80mm
- Custom lead/pitch configurations available
- Package profile heights: 0.45, 0.55, 0.75, 0.85 and 0.90mm
- Option for non-exposed die pad
- Available in gold or copper wirebond versions
- Multi-die versions available
- Chip-on-Lead (COL) using Wafer Backside Coating (WBC) available
- Thin packages per JEDEC available (V, W, U, X)
- Green materials set
- Option for 100% matte Sn or PPF
- Small chip scale design offers 50% reduction in board space (16L TSSOP vs. 16L QFN)
- 33% weight reduction (16L TSSOP vs. 16L QFN)
- Excellent thermal & electrical performance
- Full in-house package and leadframe design capability
- Full in-house assembly and test capability
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Wide range of open tool leadframe and die pad sizes available

DESCRIPTION

STATS ChipPAC's Quad Flat No-Lead (QFN) and Dual Flat No-Lead (DFN) package offering includes QFNs, QFNp, VQFN, WQFN, UQFN, XQFN, QFNp-dr and QFNs-mr. QFN is a leadframe based, plastic encapsulated chip scale package (CSP) that provides customers with an ideal choice for many applications where size, weight and thermal and electrical performance are important. A leadless package, QFN's electrical connections are achieved by way of lands located on the bottom side of the component to the surface of the PCB. QFN packages have proven to be successful for a number of applications such as wireless handset, power management, analog baseband and Bluetooth devices.

STATS ChipPAC offers multiple QFN configurations in either punch or saw singulated formats. Punch singulated packages are individually "punched" from molded strips during final assembly; saw singulated packages are assembled in an array format and separated into individual components during the final sawing operation.

QFNp is a punched singulated package that features a thin, lightweight profile and excellent heat dissipation capability. QFNp offers a more compact, high performance and cost effective solution than conventional leadframe packages, particularly for mobile and handheld applications.

QFNp-dr is a punch singulated dual row package that features a significantly higher number of I/O terminal pads in a smaller footprint. The key to the increased performance capability of the QFNp-dr is in its leadframe design which features two rows of staggered I/O terminal pads with an exposed die pad for die grounding and improved thermal performance.

The QFN saw singulated multi-row or QFNs-mr package is a saw singulated package in a land grid array (LGA) format with square or rectangular body sizes. By using a saw singulated manufacturing process, STATS ChipPAC can offer customers higher I/O count in a multi-tier format while retaining the same package size.

JCET STATSChipPAC
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QFN

Quad Flat No-Lead Package

SPECIFICATIONS

Die Thickness	100-350µm
Wire	
Gold:	18-33µm (0.7-1.3mils) diameter
Copper: QFN	18-30µm (0.7-1.2mils) diameter *Contact STATS ChipPAC for availability.*
Copper: QFN-dr	18-25µm (0.7-1.0mils) diameter *Contact STATS ChipPAC for availability.*
Lead Finish	Matte Tin or preplated Ni/Pd/Au
Marking	Laser
Packing Options	Tape & reel, tube, JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC MSL 3/2/1 (depending on package)
Temperature Cycling	–65°C/150°C, 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C, 100% RH, 2 atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs

THERMAL PERFORMANCE, θja (°C/W)

Package	Body Size (mm)	Pad Size (mm)	Die Size (mm)	Thermal Performance θja(°C/W)	Thermal Vias (on test board)
48L UQFN	7 x 7 x 0.50	5.1 x 5.1	2.26 x 2.26	26.3	25
64L QFN	9 x 9 x 0.85	7.3 x 7.3	4.52 x 4.52	19.2	36
76L QFN-dr	8 x 8 x 0.85	5.28 x 5.28	4.52 x 4.52	26.6	16

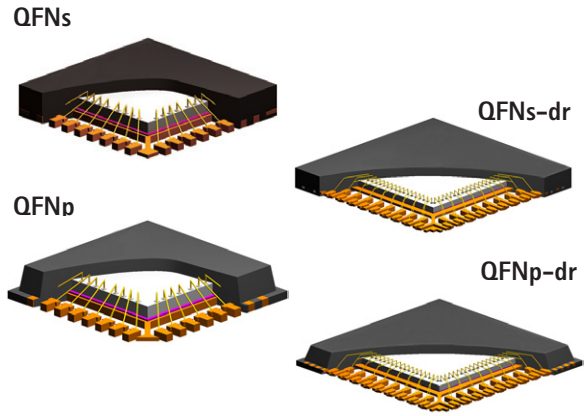
Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

ELECTRICAL PERFORMANCE

Package	Body Size (mm)	Frequency	Length	Inductance (nH)	Capacitance (pF)
48L UQFN	7 x 7 x 0.50	100 MHz	Self (short)	0.88	0.191
			Mutual	0.20	0.032
			Self (long)	0.98	0.223
			Mutual	0.27	0.064
76L QFN-dr	8 x 8 x 0.85	100 MHz	Self (short)	1.33	0.180
			Mutual	0.45	0.080
			Self (long)	1.68	0.270
			Mutual	0.53	0.110

Note: Results are simulated values per JEDEC EIA/JEP123 standards.

CROSS-SECTIONS



PACKAGE CONFIGURATIONS

Pkg Size (mm)	Lead Pitch (mm)	Lead Count
1.0 x 1.3	0.50	4
2 x 2	0.65 / 0.50	4 / 8
2 x 3	0.50	6 / 8
3 x 3	0.80 / 0.65 / 0.50 / 0.40	4 / 8 / 12/ 16 / 20
4 x 4	0.80 / 0.65 / 0.50 / 0.40	12 / 14 / 16 / 20 / 24 / 28
5 x 5	0.80 / 0.65 / 0.50 / 0.40	14 / 16 / 20 / 28 / 32 / 40
6 x 5	0.80 / 0.65 / 0.50	18 / 20 / 22 / 32
6 x 6	0.80 / 0.65 / 0.50 / 0.40	20 / 24 / 28 / 32 / 36 / 38 / 40 / 48
7 x 7	0.80 / 0.65 / 0.50 / 0.40	28 / 32 / 36 / 40 / 44 / 48 / 56
8 x 8	0.80 / 0.65 / 0.50 / 0.40	28 / 32 / 36 / 40 / 44 / 48 / 52/ 56 / 64
9 x 9	0.65 / 0.50 / 0.40	44 / 48 / 56 / 60 / 64 / 72
10 x 10	0.50 / 0.50* / 0.40	64 / 68 / 72 / 84 / 88 / 132*
11 x 11	0.50 / 0.50*	80 / 148*
12 x 12	0.50 / 0.50*	88 / 156*

Note: *Dual Row configuration

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