

Ruling Quantum Technologies with Embedded Rust

Robert Jördens

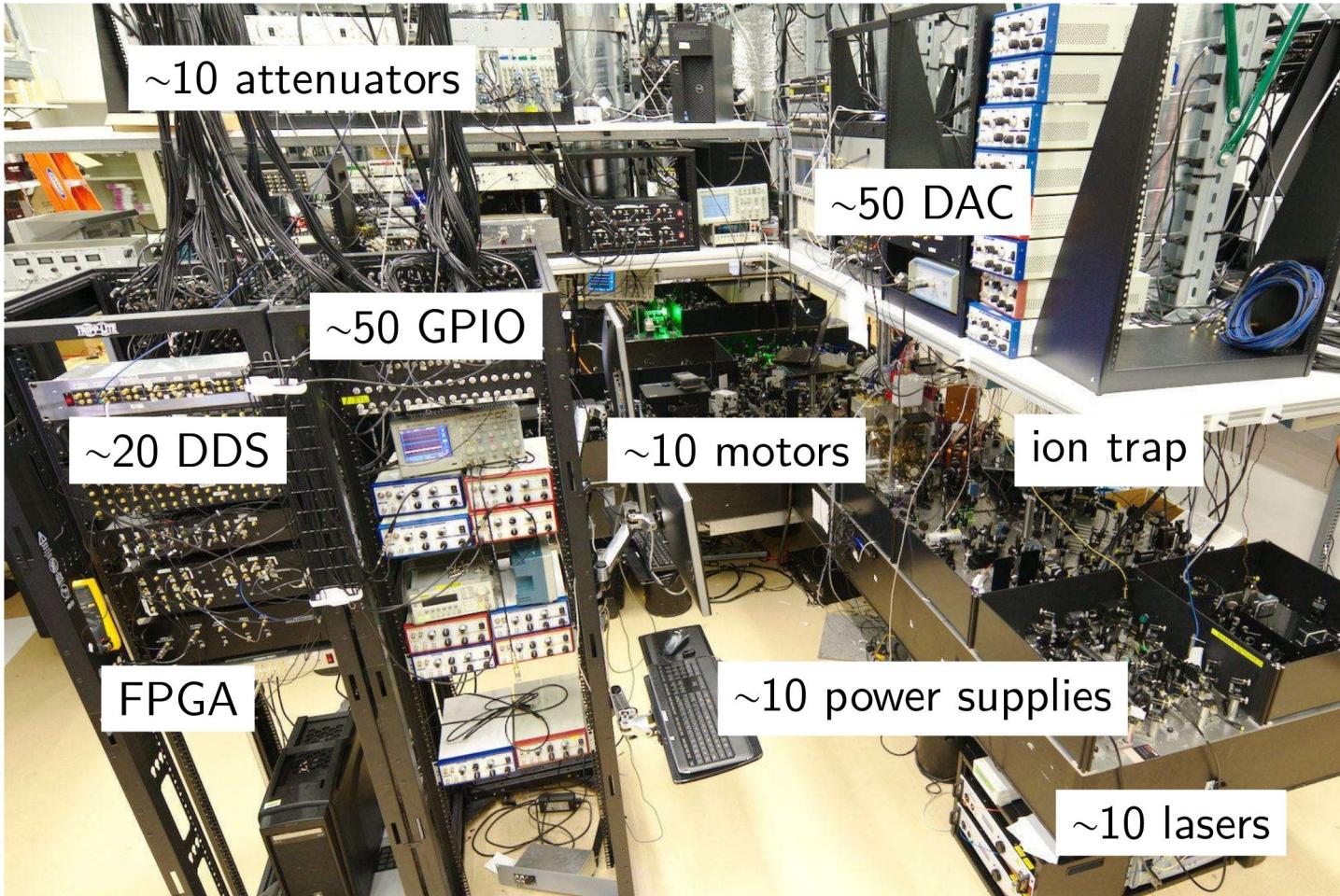
QUARTIQ GmbH and M-Labs Ltd



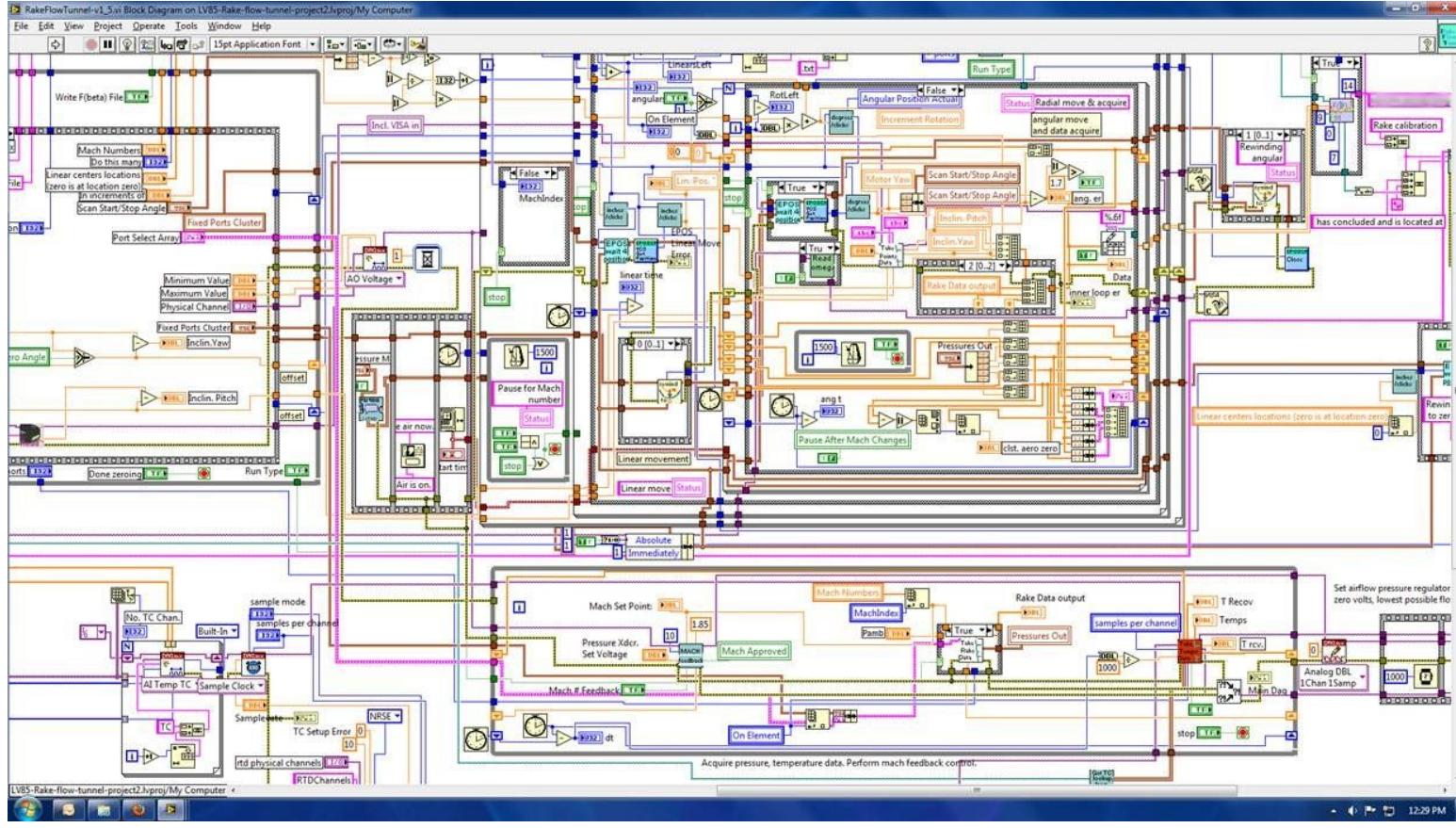
Open tools for open science

Oxidize 1k, 2020-03-20, @world

Quantum Technology in the Lab



Traditional QT Programming Language and Style





M-Labs QUARTIQ

creo TECH
Instruments S.A.

PTB
Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin



opticlock

UNI
FREIBURG

UNIVERSITY OF OXFORD
NQIT
Networked Quantum Information Technologies

UNIVERSITY OF MARYLAND

ARL iqI JOINT QUANTUM INSTITUTE

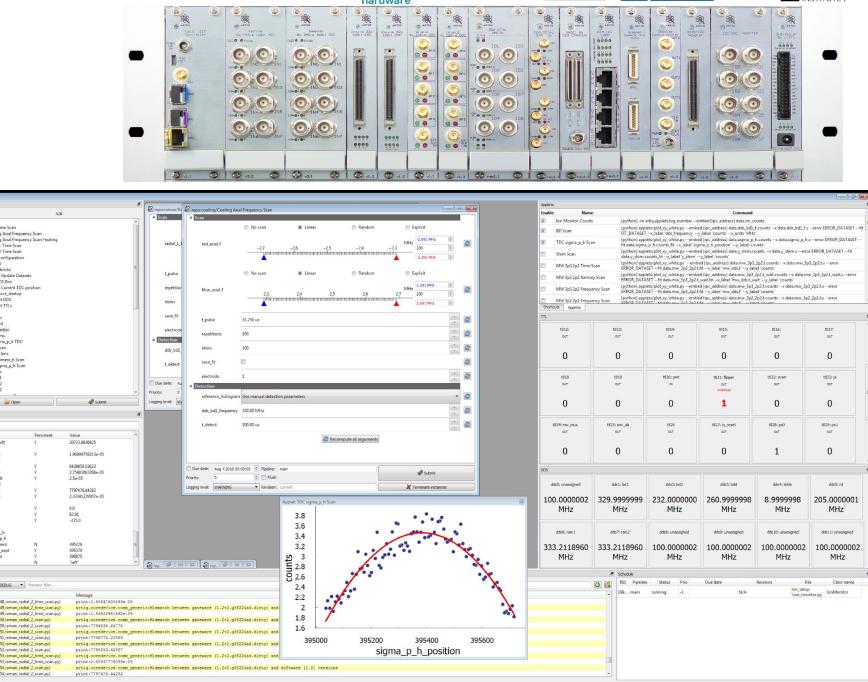
Leibniz
Universität
Hannover

- Experiment control framework for all time scales from months down to picoseconds
- LGPLv3 using Python, LLVM, Rust, Mor1kx, Qt5...
- Comprehensive automatic continuous integration, hardware-in-the-loop testing

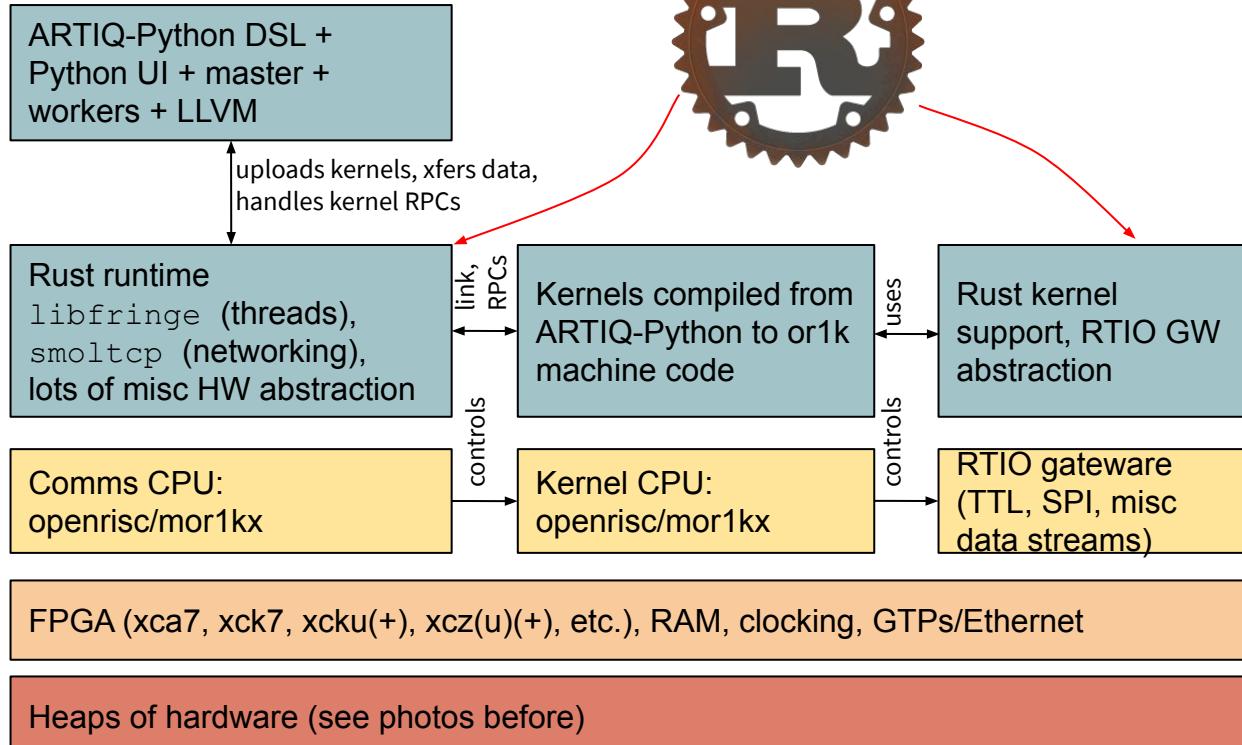
```
trigger.sync()
start = now()
for i in range(3):
    delay(5*us)
    dds.pulse(900*MHz, 7*us)
at(start + 1*ms)
dds.pulse(200*MHz, 11*us)

# wait for trigger input
# capture trigger time

# first pulse 5 µs after trigger
# re-reference time-line
# exactly 1 ms after trigger
```



Rust in ARTIQ

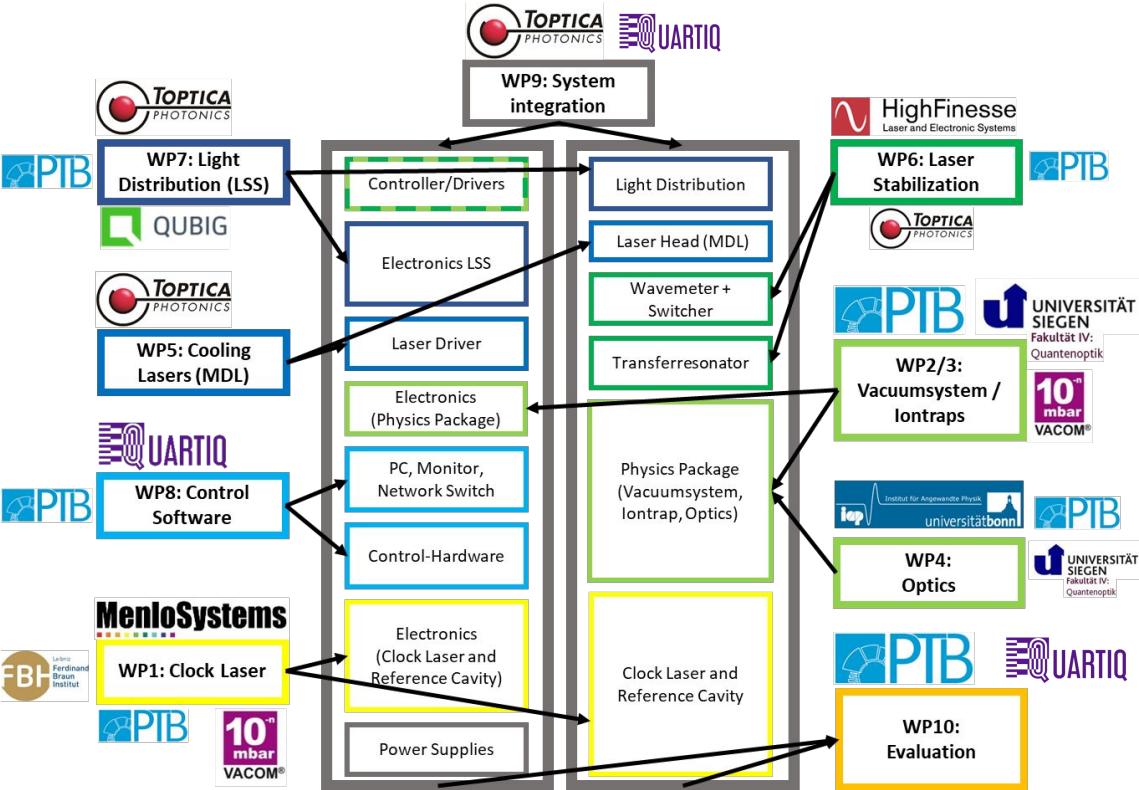
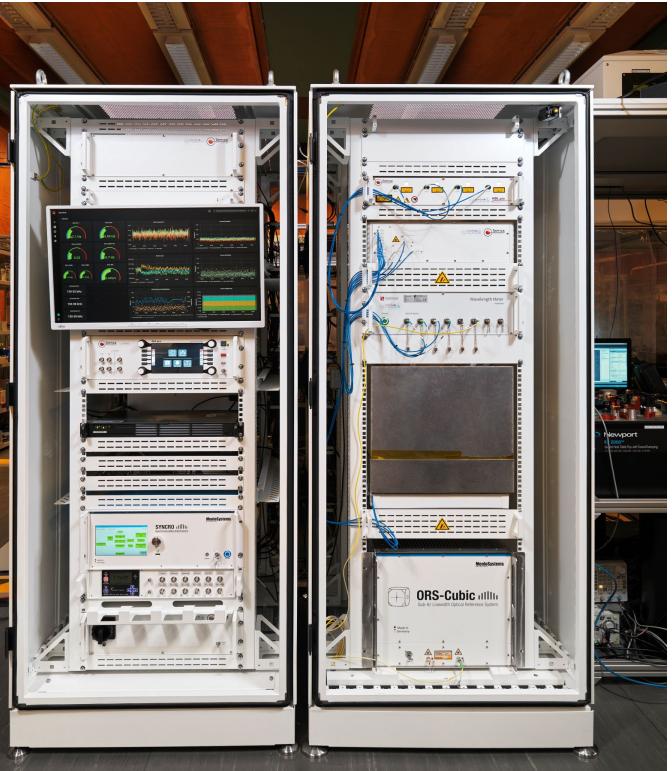


- Started with C and lm32 in 2014
- Ported to Rust in 2016
- Developed smoltcp networking stack (supports both no_std and std)
- Moving to riscv (for soft core) and ARM (Zynq PS hard silicon) and considering better DSL/toolchain design
- Looking at RTFM-rs and async-await for the runtime
- **Sticking with Rust!**

Optical Single-Ion Clock for End Users

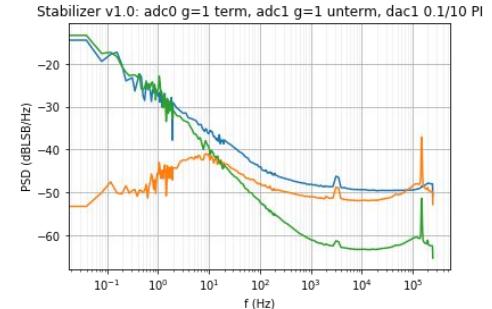
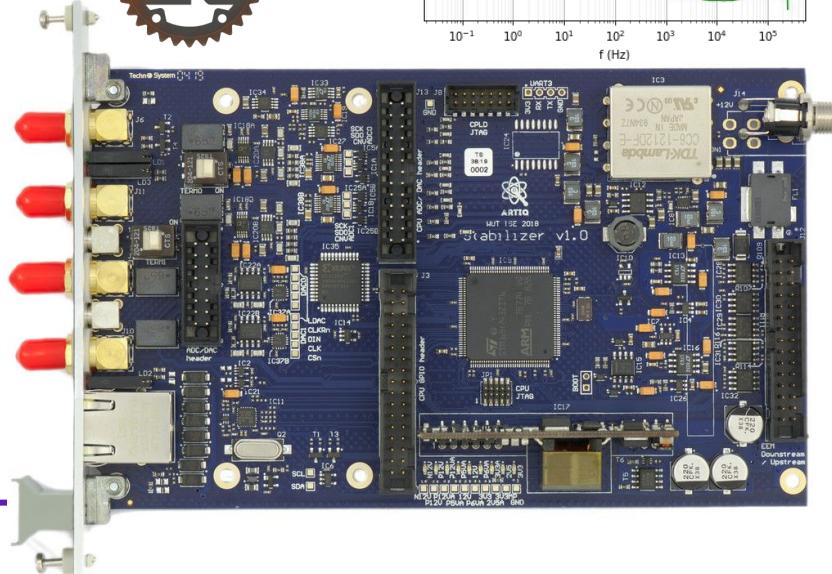
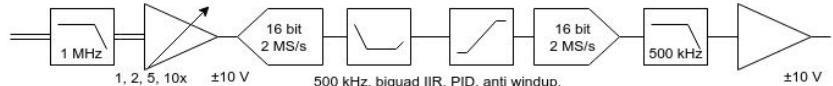


Federal Ministry
of Education
and Research



Stabilizer: ~MHz embedded PID controller

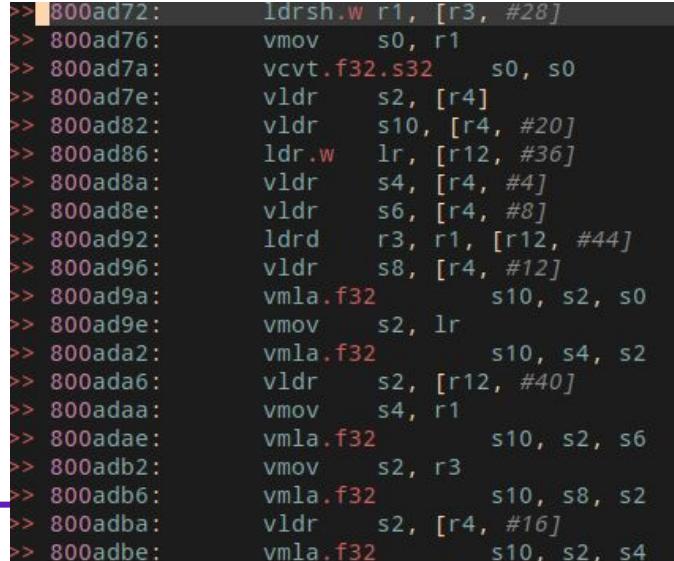
- STM32H743 (480 MHz, 2 MB FLASH, 1 MB SRAM)
- 2 ADCs, 2 DACs, filters, PGAs, Power-over-Ethernet
- Mezzanine connectors for different frontends (RF modulation, current drive etc)
- Controlled through Ethernet or ARTIQ (real-time)
- Use cases:
 - Stabilize laser beam powers
 - Stabilize magnetic fields at ion to nT (Nanotesla)
 - Stabilize laser frequencies to atomic transitions
 - Stabilize optical effective path length through fibers to nm (Nanometer)
 - Modulate/demodulate/feedforward
 - Software-defined Radio
- Big thanks to Embedded Rust, rtfm-rs, smoltcp!
- Would like to use more IoT protocols with no_std Rust: CoAP, MQTT



Cognitive Style of Rust for Embedded and DSP

- Proportional/Integral/Derivative (PID) controllers are just IIR filters
- The core of IIR and FIR implementations are the same
- The core of every FIR filter is a multiple-accumulate (MACC) operation, a.k.a. vector dot product
- **Beautiful concise and accurate syntax**
- Don't worry about array bounds handling or filter size
- Just relax and rely on monomorphization, loop unrolling
- **Compiles to really good machine code** (here: second order IIR/5-tap FIR mixed with data shuffling INSNS)
- Could gain a bit with 16 bit integer math and SIMD (SMLALD for dual MACC) at the cost of readability, flexibility, and maintainability
- Would like to see VMAXNM and VMINNM be used
- Overhead due to peripheral flag handling, data clipping etc. larger than net filter math
- One processing iteration (two PID loops) is about 350 ns

```
48 fn macc<T>(y0: T, x: &[T], a: &[T]) -> T
49 where
50     T: Add<Output = T> + Mul<Output = T> + Copy,
51 {
52     x.iter()
53         .zip(a.iter())
54         .map(|(&i, &j)| i * j)
55         .fold(y0, |y, xa| y + xa)
56 }
```

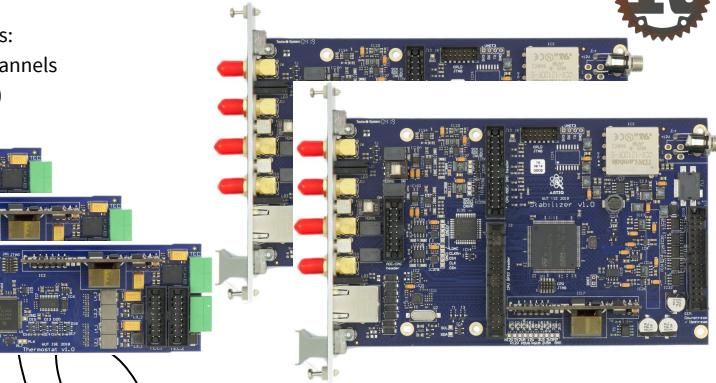


```
>> 800ad72: ldrsh.w r1, [r3, #28]
>> 800ad76: vmov s0, r1
>> 800ad7a: vcvt.f32.s32 s0, s0
>> 800ad7e: vldr s2, [r4]
>> 800ad82: vldr s10, [r4, #20]
>> 800ad86: ldr.w lr, [r12, #36]
>> 800ad8a: vldr s4, [r4, #4]
>> 800ad8e: vldr s6, [r4, #8]
>> 800ad92: ldrd r3, r1, [r12, #44]
>> 800ad96: vldr s8, [r4, #12]
>> 800ad9a: vmla.f32 s10, s2, s0
>> 800ad9e: vmov s2, lr
>> 800ada2: vmla.f32 s10, s4, s2
>> 800ada6: vldr s2, [r12, #40]
>> 800adaa: vmov s4, r1
>> 800adae: vmla.f32 s10, s2, s6
>> 800adb2: vmov s2, r3
>> 800adb6: vmla.f32 s10, s8, s2
>> 800adba: vldr s2, [r4, #16]
>> 800adbe: vmla.f32 s10, s2, s4
```

AI-ARTIQ: Laser control platform

- Complete hardware and software stack for integrated control of complex laser modules
- QUARTIQ, Createch (Warsaw), Ferdinand Braun Institute, and University of Warsaw
- Replacing the expert (a.k.a. Physics Grad student) by many cascaded control loops, multiple-input-multiple-output, networked IoT schemes
- High speed control up to MHz loop bandwidth
- Ultra-precise temperature and current control
- Many interconnected temperature and laser current control modules
- Lots of IoT-style networking, DSP, hardware co-design, embedded Rust programming, system design, and Physics
- **Started this year, hiring right now!**

Array of temperature controllers:
Peltier, μK stability, multiple channels
(Sinara-Thermostat as stand-in)



Ferdinand Braun Institute Berlin: Micro-integrated extended cavity diode laser module for precision iodine spectroscopy in space, used in the JOKARUS experiment

QUARTIQ GmbH

Founded 2017 in **Berlin**, Germany

At home in **Quantum Technologies** together with sister company **M-Labs Ltd** (Hong Kong)

QUARTIQ+M-Labs providing control systems to world leading QT research groups since 2014



Software

- **FPGA** Gateware (TDC, SDRAM, RTIO, CPU, GTx...)
- High-performance **metaprogramming** languages (**Migen**, MiSoC)
- Embedded ecosystem development (**Rust**, OpenRISC, LM32, RISCV-V)
- Full-stack control software from GUI to HW gates (**ARTIQ**)
- **DSP** solutions in software and gateware

Hardware (Sinara ecosystem)

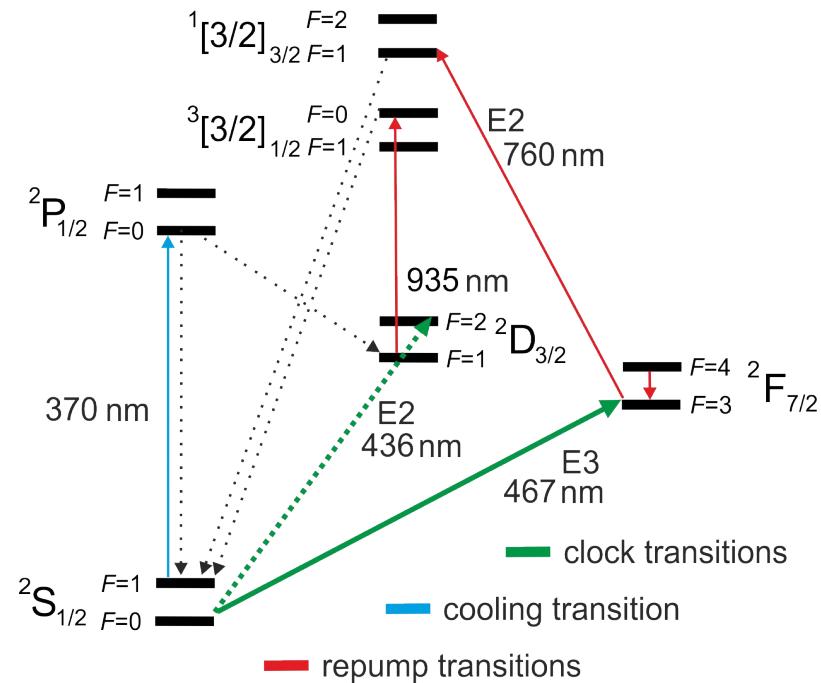
- **DDS** and **PLL/VCO** synthesizers
- Precision **ADC/DAC** analog interfaces
- **TDC/DTC** time-digital converters
- Frame **grabbers** for EMCCD cameras
- High-density/isolated/fast **digital IO**
- Fast and flexible **PID** controllers
- Stable **Temperature** controllers
- High-density/high-efficiency RF **power amplifiers**
- High-density **GS/s AWGs**

Custom solutions

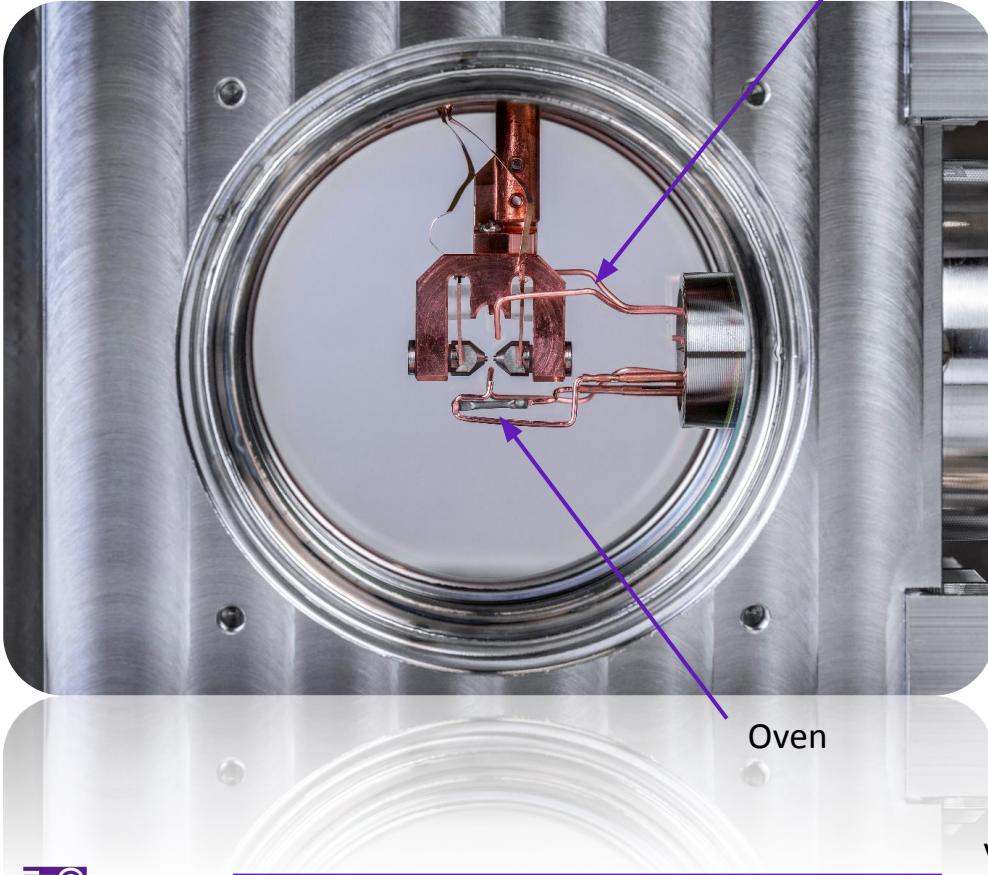
- **Satellite** payload electronics and control software
- Custom **control** systems
- Control system **consulting**
- Development of quantum physics control **algorithms**

Optical single-ion clock for users

- Targeted specs:
 - 10x better frequency stability than a H-maser
 - <1000 kg, <3.5 kW
- Based on single $^{171}\text{Yb}^+$ ion, E2 transition
 - Diode lasers available for all transitions, low power
 - Very long ion trapping times
 - Two clock transitions: E2 and E3
 - E2: secondary representation of the SI second with 6×10^{-16} uncertainty
 - E3: upgrade opportunity: 3×10^{-18} uncertainty demonstrated
- Two mobile 19 " racks

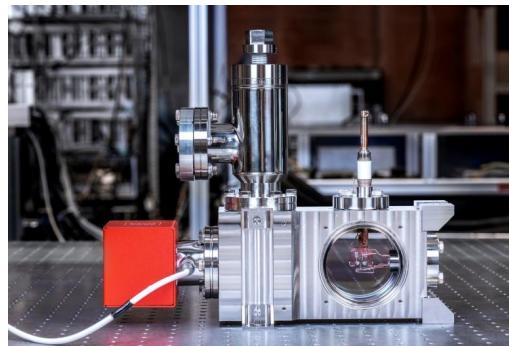


Physics package



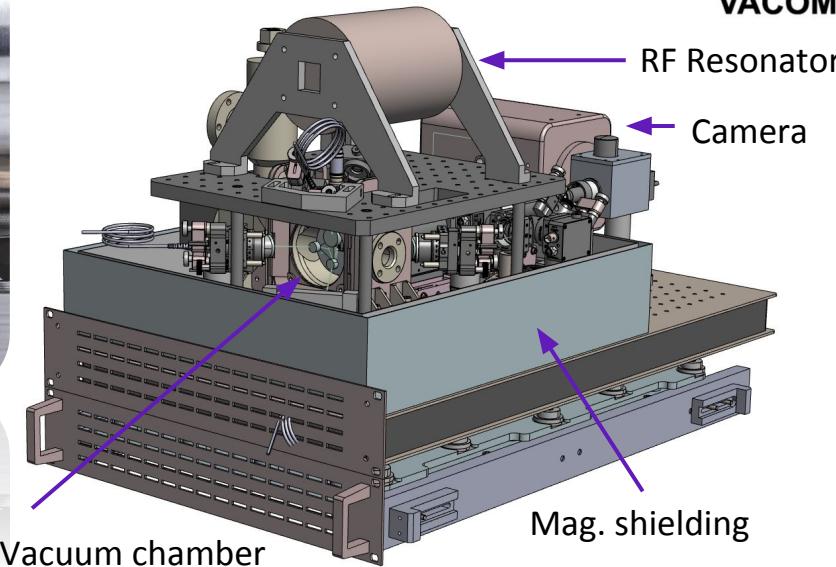
DC electrode

Oven



universität bonn

10⁻ⁿ
mbar
VACOM®



RF Resonator

Camera

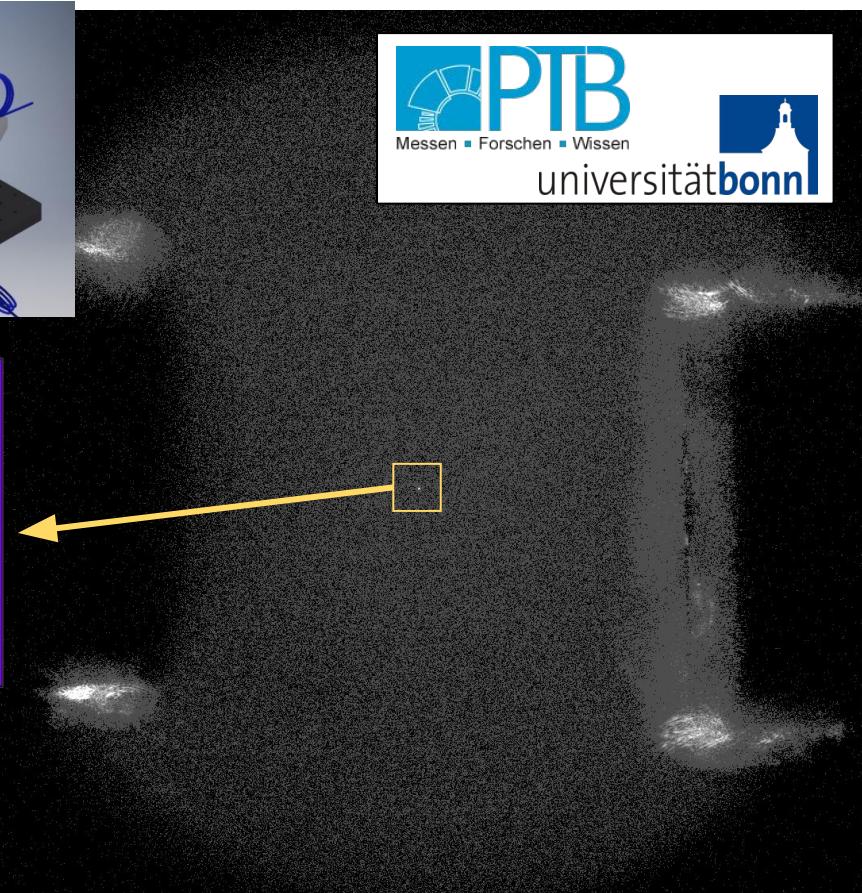
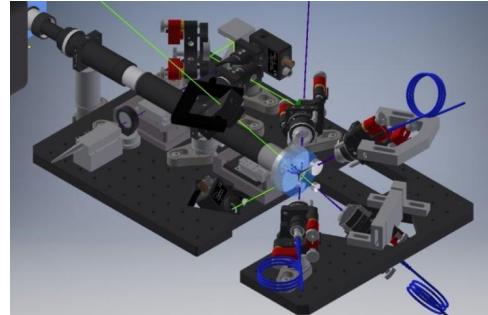
Vacuum chamber

Mag. shielding

Physics package: fluorescence detection and beam shaping

Four confocal laser beams

- 2x cooling beam (370 nm)
- 1x multi-chromatic beam
(370 nm, 399 nm, 760 nm, 935 nm)
- 1x clock beam (435 nm)



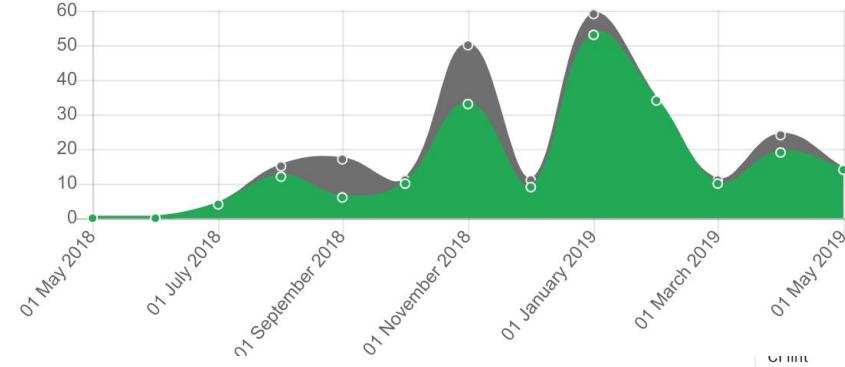
Detection

- Wavelength: 370 nm
- Numerical aperture: 0.38
- Field of view: 340 µm
- Magnification: 10x - 50x

Continuous Integration, Continuous Deployment

- Continuous automatic and autonomous tests of code, algorithms, configuration
- Prevents errors and bugs from being introduced
- Including tests with hardware-in-the-loop (HITL)

Pipelines for last year



Date	Pipelines Run
01 May 2018	0
01 July 2018	2
21 September 2018	10
01 November 2018	50
01 January 2019	55
01 March 2019	10
01 May 2019	15

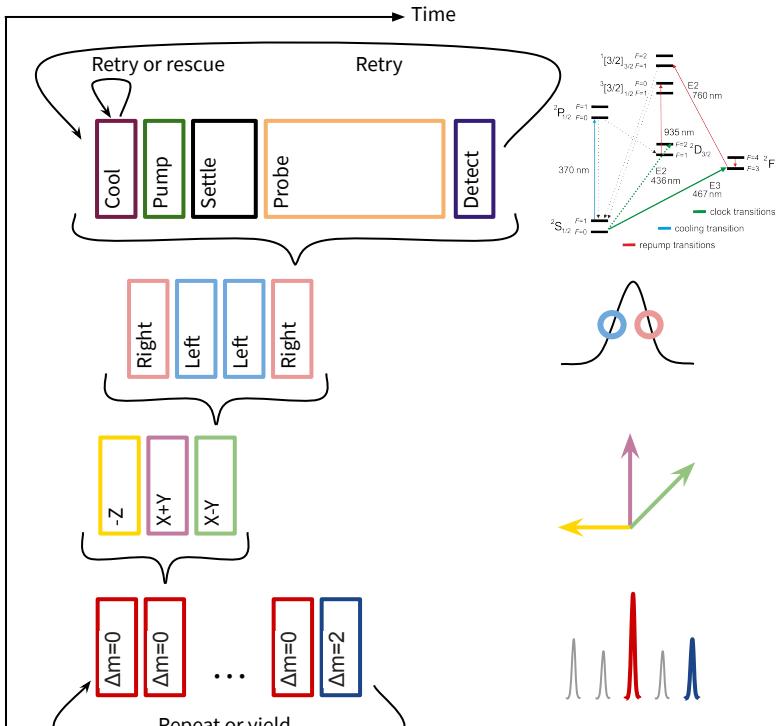
QUARTIQ > opticlock > opticlock > Jobs

All 257 Pending 0 Running 0 Finished 257

Status	Job	Pipeline	Stage	Name	Coverage
passed	#212409781 ⚡ master -o 9c839436 hitl opticlock quartiq	#61286290 by 🌱	test	basic	⌚ 00:01:02 📅 12 hours ago
passed	#212383386 ⚡ master -o bbca228c hitl opticlock quartiq	#61279459 by 🌱	test	basic	⌚ 00:01:00 📅 13 hours ago
passed	#212363540 ⚡ master -o c307cf50 hitl opticlock quartiq	#61274536 by 🌱	test	basic	⌚ 00:00:50 📅 13 hours ago
passed	#212343342 ⚡ master -o 91485d40 hitl opticlock quartiq	#61269872 by 🌱	test	basic	⌚ 00:01:05 📅 14 hours ago

Open t

Clock cycle pattern



Probe cycle: probe E2 transition, reject cooling/pumping/detection failures; accumulate photon timing correlation to trap RF phase to determine electric field stability

Modulation cycle: modulate probe frequency to discriminate; reject clock laser drift aliasing

Orientation cycle: three highly orthogonal magnetic field orientations; determine/reject quadrupole shift; apply clock laser feedback

Supercycle: determine magnetic fields and thus 2nd order Zeeman shifts; adjust probe power; yield to other calibration experiments; determine probe polarization stability; adjust probe power

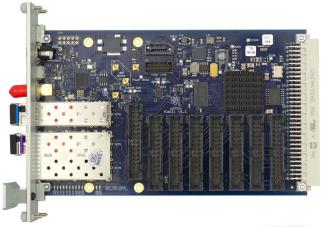
Sinara hardware: FPGA/μC



**Sayma-AMC/Sayma-RTM/
Metlino:** 8 channel 2.4
GS/s smart AWG, telco
grade μTCA high reliability
redundancy crate



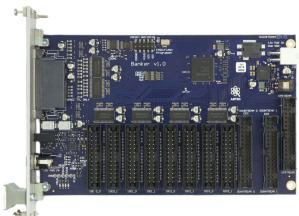
Humpback: carrier for
single-board-computers
/microcontrollers, 3
channel EEM, FPGA



Kasli: 12 channel EEM
(Eurocard extension
module) controller with
FPGA, gigabit transceivers



Thermostat: compact
2 channel, 12 W,
sub-mK, networked,
temperature controller,
power-over-Ethernet

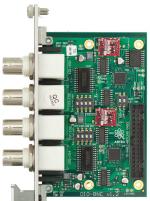


Banker: 128 channel
digital I/O with FPGA and 3
channel EEM, for complex
programmable digital
applications



Stabilizer: 2 channel, 1
MS/s ADC+DAC with
400 MHz
microprocessor, 1
EEM, networked, PoE,
mezzanine options

Sinara hardware: digital I/O



DIO-BNC/DIO-SMA: 8 channel isolated digital input/output, switchable termination



DIO-RJ45: 16 channel LVDS digital input/output for high interference suppression



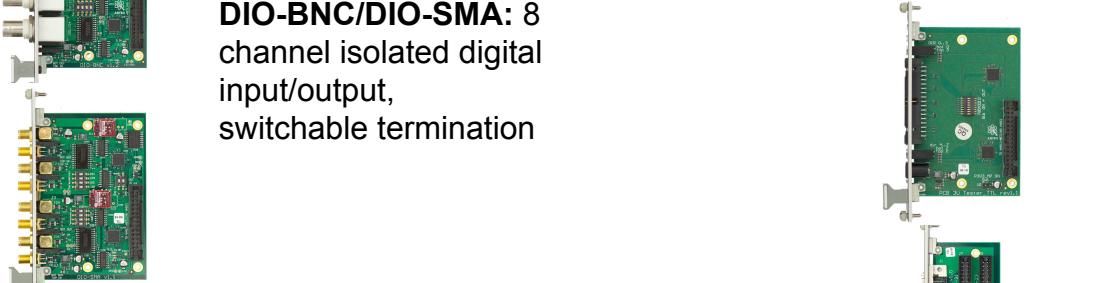
Grabber: digital CCD frame grabber, 3/6/9/10 tap, for low-latency image processing



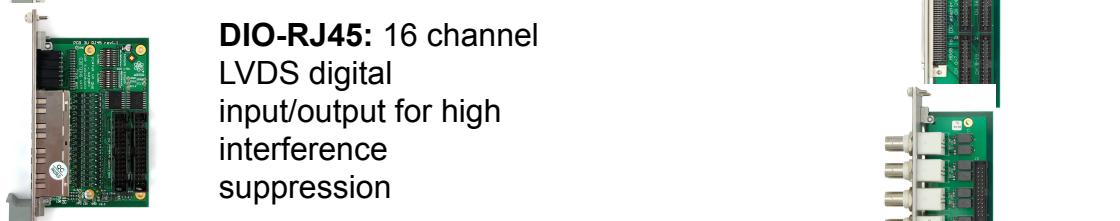
Banker-EDGE: modular DIN-rail digital I/O, signal buffers, breakout



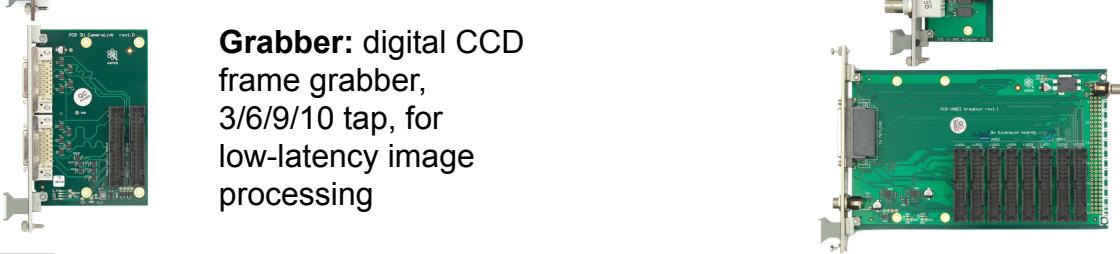
Tester: LVDS-TTL adapter for EEM development and prototyping



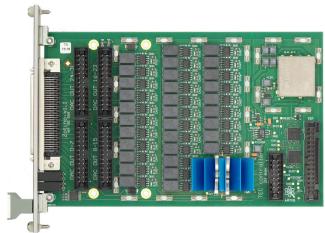
HD68/IDC: DAC/ADC break-out and adapters



VHDCI: 8 channel EEM-VHDCI adapter for remote modules



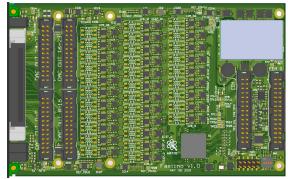
Sinara hardware: DAC/ADC



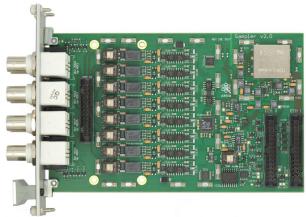
Zotino: 32 channel, 16 bit DAC, 1 MS/s aggregate



Novogorny/Sampler: 8 channel 1 MS/s 16 bit ADC with 1/10/100/1000 programmable gain amplifier, integrated termination, differential sensing



Fastino: 32 channel, 16 bit DAC, 2.5 MS/s each channel



(in planning) **Phaser:**
4 channel (2xI/Q)
quadrature 1 GS/s
DAC, integrated I/Q
upconverters and
interpolators

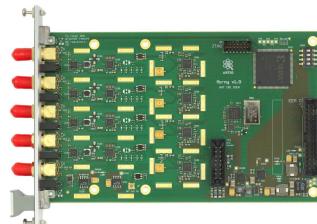
Sinara hardware: radio frequency/microwave



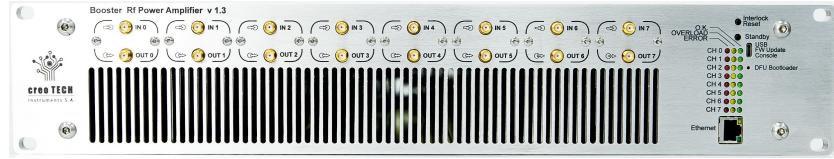
Urukul-AD9910: 4 channel, 1 GS/s DDS, deterministic phase, integrated PLL, digital attenuator, high isolation RF switch, RAM pulse shaping, ramp generator



Urukul-AD9912: 48 bit frequency resolution variant



Mirny: 4 channel, 50 MHz - 13.6 GHz PLL, digital attenuator, high isolation RF switch, mezzanines for upconversion, frequency multiplication



Booster: 8 channel, 40-500 MHz RF power amplifier, networked, comprehensively monitored and supervised



Clocker: 4+4 clock fanout/buffer with 2 channel multiplexer, up to 1 GHz, ultra low jitter