

MAX803 delay: 3.3ms max

CRESET high to first MCLK edge: 1.2ms

CONFIG TIME: MCLK Frequency:
230ms (slow, default) 7.5MHz (slow, default)
110ms (medium) 24MHz (medium)
70ms (fast) 40MHz (high)

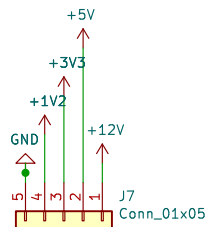
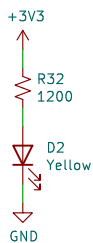
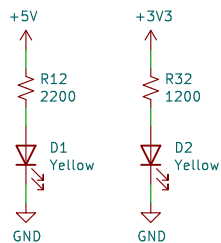
49 clock cycles from CDONE going high to PIO going active

Host PC reset pulse appears to be about 350ms min

0.4V/ms to 10V/ms ramp rate range

1.2V: 0.12ms to 3ms

3.3V: 0.33ms to 8.25ms



GRAPHICS GREMLIN (with HDMI)

DESIGN BY @TubeTimeUS
Modified by @yeokm1

Sheet: /power/
File: power.kicad_sch

Title: Power Regulators and Reset Circuit

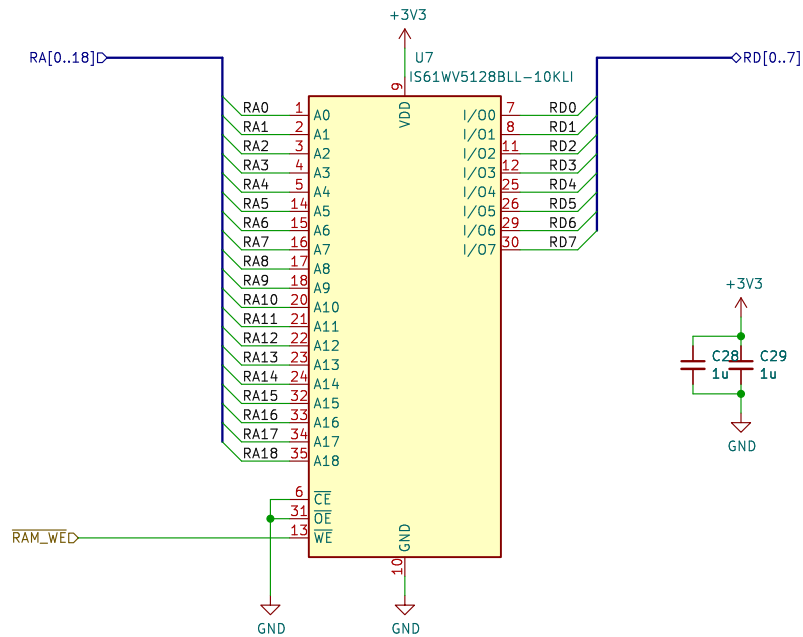
Size: A4 Date: 2023-09-17

KiCad E.D.A. kicad 7.0.7

Rev: 2.2

Id: 3/6

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GRAPHICS GREMLIN (with HDMI)

DESIGN BY @TubeTimeUS
Modified by @yeokm1

Sheet: /RAM/

File: RAM.kicad_sch

Title: SRAM

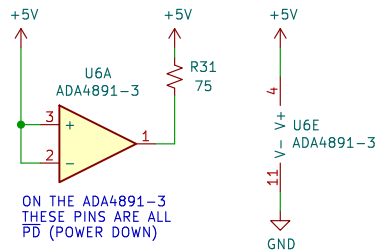
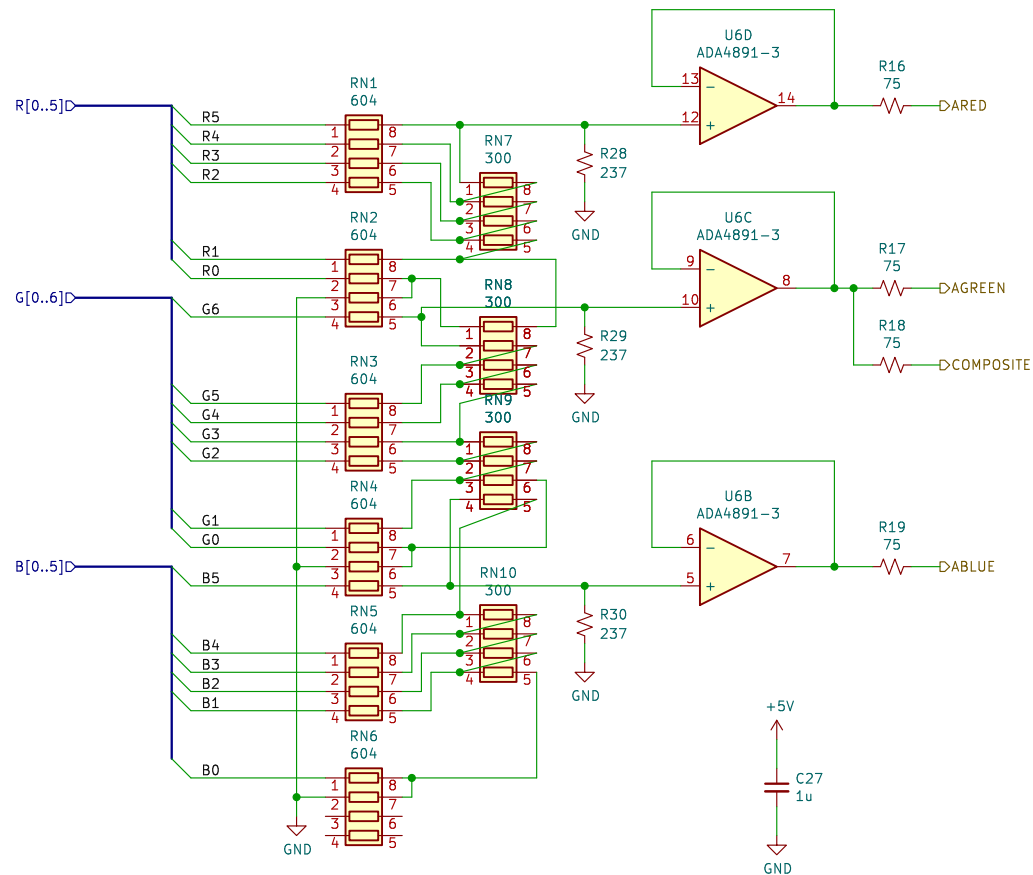
Size: A4 Date: 2023-09-17

KiCad E.D.A. kicad 7.0.7

Rev: 2.2

Id: 4/6

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GRAPHICS GREMLIN (with HDMI)
DESIGN BY @TubeTimeUS
Modified by @yeokm1

Sheet: /vga_dac/

File: vga_dac.kicad_sch

Title: Resistor Ladder DAC and Output Buffer

Size: A4

Date: 2023-09-17

Rev: 2.2

KiCad E.D.A. kicad 7.0.7

Id: 5/6

