Topologies

1. The schemes to connect the processors in a parallel machine are called topologies.

2. Ethernet is a connection scheme where all machines on a network are on a single cable; A fully connected configuration is that each processor has one wire for the communications with each other processor.

3. We describe the parallel machine with a graph where each process is a node and two nodes are connected if there is a direct connection between them.

Graphic definition,

The *degree* of a node is the number of other nodes it is connected to.

The *diameter* is defined as the maximum shortest distance, counting of links, between any two nodes.

Connectivity graph is that there is a path between every pair of vertices in the graph.

Congestion/contention, conflict between two simultaneous messages.

Bisection width, the minimum number of links that have to be removed to partition the processor graph into two unconnected graphs. The bisection width ω describes how many messages can, guaranteed, be under way simultaneously in a parallel computer.

Bisection bandwidth, the bandwidth across the bisection width, which is the product of the bisection width, and the capacity (in bits per second) of the wires.

Aggregate bandwidth, the total data rate if every processor is sending: the number of processors times the bandwidth of a connection times the number of simultaneous sends a processor can perform.

To have all processors on the same memory bus, UMA or SMP model.

4. Linear arrays and rings.

5. 2D or 3D arrays. To organize the processors in a two-dimensional or three-dimensional *Cartesian Mesh*. Every processor has a coordinate (i, j) or (i, j, k), and it is connected to its neighbors in all coordinate directions. Torus connections are grid-based designs which connect the left and right sides if a 2D grid, as well as the top and the bottom.

6. *Hypercubes*. An n-dimensional hypercube computer has 2^n processors, with each processor connected to one other in each dimension. The Gray code offers a way to embed a one-dimensional ‘mesh’ into a hypercube.

7. *Switched networks* are made out of switching elements, each of which have a small number of inbound and outbound links. Some popular designs are *the crossbar*, *the butterfly exchange* and *the fat tree*.

Cross bar, Butterfly exchange, Fat-trees.

8. Cluster networks, case study, stampede.

9. Bandwidth and latency.

Latency: setting up a communication between two processors takes an amount of time that is independent of the message size.

Bandwidth: after a transmission between two processors has been initiated, the main number of bytes per second that can go through the channel.

10. Locality in parallel computing.

Between cores, private cache, shared cache. Between sockets. Through the network structure.

Questions

1. What is Gary code? How does it work?

2. What is the difference between butterfly exchange model and fat-tree model?

Answers

1. *Bisection width*, the minimum number of links that have to be removed to partition the processor graph into two unconnected graphs. The bisection width ω describes how many messages can, guaranteed, be under way simultaneously in a parallel computer.

2. The *diameter* is defined as the maximum shortest distance, counting of links, between any two nodes.

3. Switched network.