STM32 LQFP64 EVK V2.0 User Guide

LPWA&LTE Module Series

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About Document

Revision History

Version	Date	Author	Description
V1.0	2025-06-05	Fugui Wang	Creation of the document

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1 Preface

In this article, it mainly illustrates the HW connection and individual function on STM32 LQFP64 EVK V2.0 Board and Quectel LPWA/LTE module Carrier Board.

2 Summary

Connected with the TE_A of Quectel LPWA/LTE module, this carrier board can facilitate compiling reference codes in client side.

2.1. Application Modules

Module Series	Type
LTE	EC2X Series; EG2X Series; EC200X Series; EG9X Series; EC600X Series; EC800X Series
LPWA	BG95; BG96; BG77X Series

Note

For STM32 LQFP64 EVK V2.0, it supports installation and communication of standard LTE TE_A or LPWA TE_A. While the communication between MCU and module, corresponding SW shall be applied. For specific info, please refer to <SW Illustration>.

2.2. Key Features

Table 1: Key Features

Component	Description
Power Supply	DC Supply Voltage: 4.5~5.5 V; Typical supply voltage: 5 V;
TE-A	Supports LPWA&LTE module
(U)SIM	2 SIM card connectors. Supports SIM card insertion detect. The connector is connected with LPWA&LTE module. Either Single card or Dual card is determined by specific module.
TYPE-C USB to UART*4	4 UART-to-USB interfaces. Specific translator Type: CP2108 ● Interface0: Communicates with DEBUG port ● Interface1: Communicates with MCU DEBUG port ● Interface2: Reserved. ● Interface3: Reserved.
TYPE-C USB	USB2.0. Communicates with USB in LPWA&LTE module by default
Status Indication LED	5 LEDs
Button and Switch	PWRKEY Button (S201); Module's PWRKEY (S302); Module's RESET(S301); MCU RESET(S101)
Antenna Adapter	2 antenna adapters IPX: Connects with LPWA&LTE TE_A antenna interface SMA: External antenna
MCU DEBUG	2 methods SWD Interface (J604) JTAG Interface (J101)
SD Interface	Supports SD card. Communicates with MCU by default. SD2.0. Max.: 32 GB
SPI FLASH	Standard SPI: 64 Mb
TYPE-C USB (ST LINK)	Connect MCU to debug and update program in a method of SWD

2.3. Component Layout

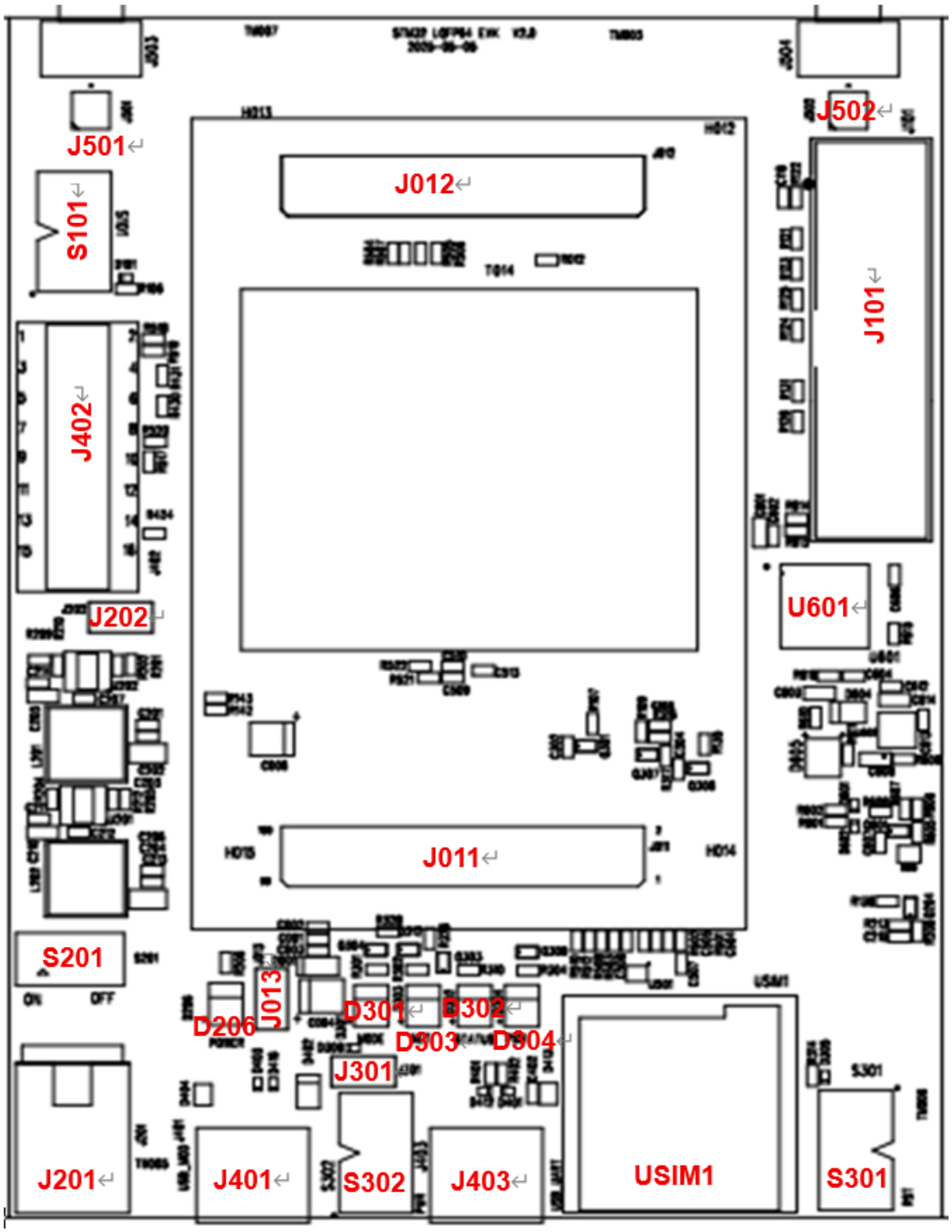


Figure 1: Top Layout

Note

If it is necessary to query corresponding component location on EVK, please refer to ***Reference [2]***

Table 2: Components Function

Component	Placement No.	Description
TE-A Interface	J011 & J012	Connects to TE-A of LPWA&LTE module
Power Input Interface	J201 J401 J403	DC adaptor jack. Typical voltage: 5 V/2 A TYPE-C USB Interface: 5 V Input TYPE-C USB Interface: 5 V Input
Power Switch	S201	Power ON/OFF
TYPE-C USB	J401	USB2.0. Connects to the USB interface of module Used for Power Supply
TYPE-C USB	J403	USB2.0 to 4*UART Used for Power Supply
(U) SIM	USIM1, USIM2	2 SIM card interfaces
PWRKEY	S302 J301	PWRKEY button. Power on/off module Jumper. Reserved for PWRKEY short.
RESET	S301	Reset module
VBAT	J103	Jumper. VBAT power test
3.3 V	J202	Jumper. MCU, SD and SPI FLASH Power test points
POWER LED	D206	Power Input indicator
MODE LED	D301	LTE Registration status indicator
NET LED	D303	Network status indicator
STATUS LED	D302	Operation Status indicator of module
*PSM LED	D304	PSM or Sleep indicator
JTAG	J101	STM32 JTAG: Updates firmware or debugs
Reserved DEBUG	J402	2 serial interfaces are reserved. Used for data transmission between MCU and MAIN_UART in module; Emergency download control; USB Switch Control*
MCU (ST LINK)	U601	Type: STM32F103CBT6. As MCU of ST LINK, it can be connected with PC to debug, update program for external MCU or U101

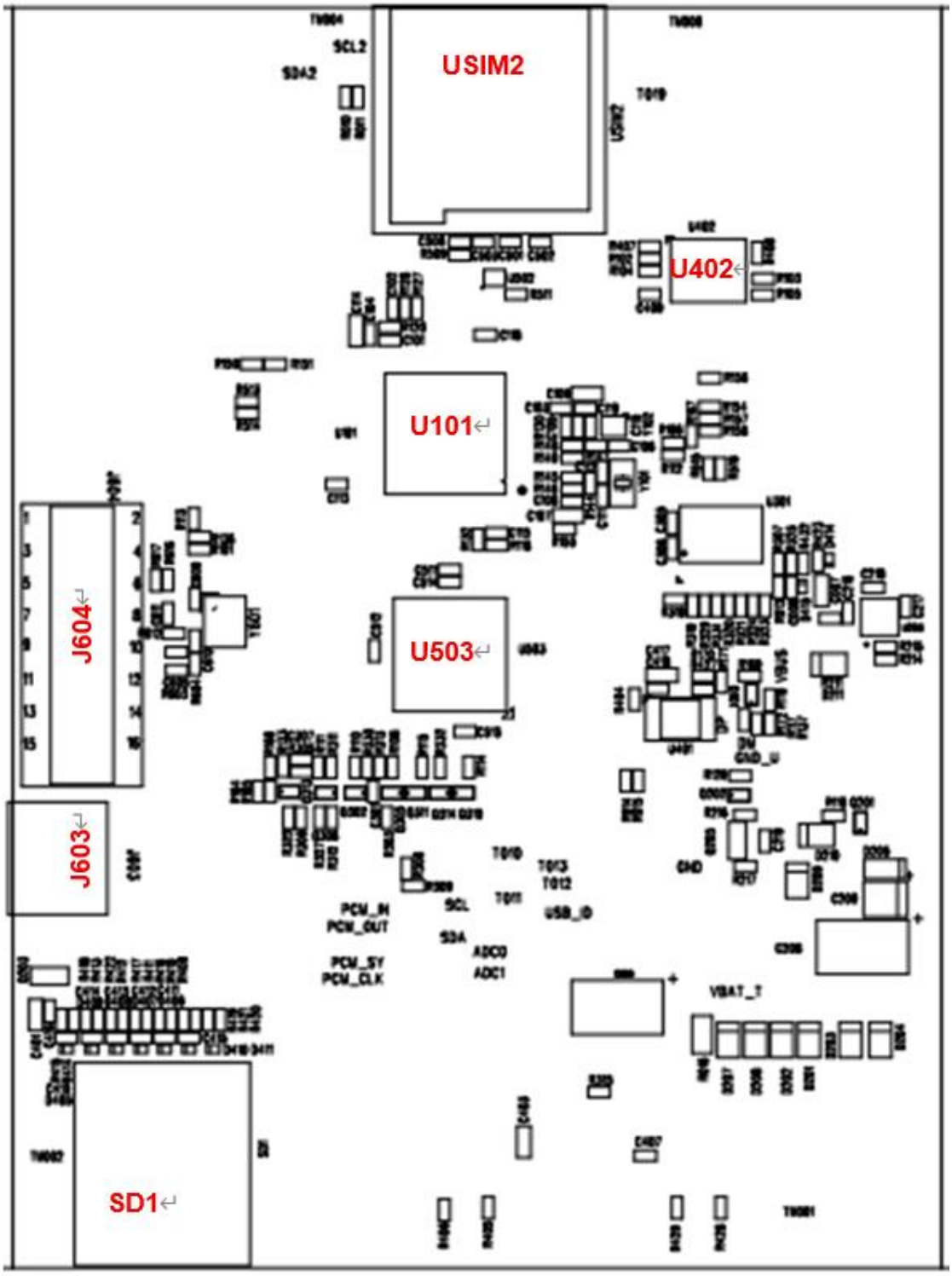


Figure 2: Bottom Layout

Note

If it is necessary to query corresponding component location on EVK, please refer to **Reference [3]**

Table 3: Components Function

Component	Placement No.	Description
USIM2 Card	USIM2	USIM2 Interface (Supported or not is determined by module)
SD Card	SD1	SD Card (Connects to STM32)
SPI FLASH	U402	Type: W25Q64JVZPIQ. Default Value: 64 Mb
USB Switch	U401	Connects the USB interface to peripheral TYPE-C or MCU
USB to TTL	U503	USB-to-4*UART. Type: CP2108
MCU	U101	STM32F413RGT6 (Default type). Communication between Host with LTE or LPWA module
SWD Debug Interface	J604	Reserves USB_ID to control Host-Slave Handover by USB interface of U101 Reserves SWD Debug interface of U101. Thus, it can debug or update program in U101 via U601. Reserves SWD Debug interface of U601.
TYPE C USB	J603	Connected with external PC, the ST LINK (U601) USB interface will debug or update program in external MCU or U101 via U601.

2.4. Top View and Bottom View

Figure 3 and Figure 4 show the top view and bottom view of carrier board.

Figure 3: Top View of Carrier Board

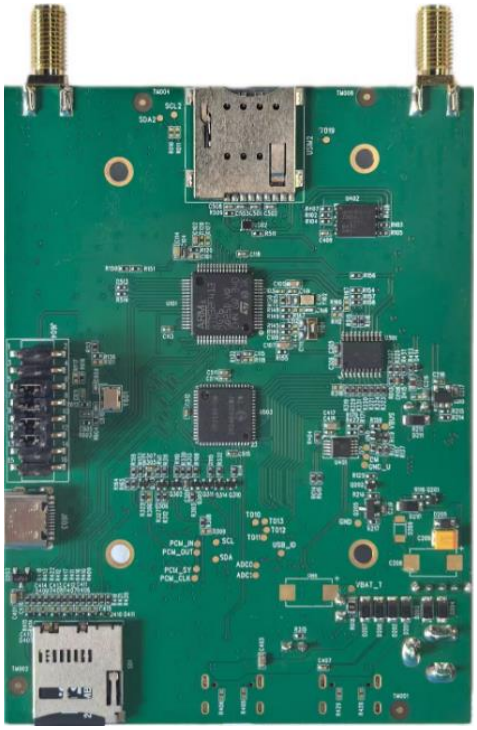


Figure 4: Bottom View of Carrier Board

2.5. TE-A Installation

Figure 5: Top View after Installing

3 Application Interfaces

In this chapter, it will illustrate hardware interfaces on carrier board. See following contents in detail.

- LTE&LPWA TE_A Interface
- Power Input interface
- Power Supply
- TYPE-C USB Interface (J401)
- TYPE-C USB Interface (J403)
- SIM1 Card Interface
- Button (PWRKEY/RESET)
- Status indication LED
- JTAG
- SWD
- USB_ID*
- Reserved DEBUG interface
- SD Card interface
- SPI flash
- SIM 2 Card Interface
- MCU

3.1. TE-A Interface

Connected to the J011 and J012 of STM32 EVK via BTB connector, the TE-A is to adapt LPWA&LTE module, allowing client to test features in LPWA&LTE module easily or develop application.
See connection between EVB and TE-A below.

Figure 6: Connection between LPWA&LTE TE-A and EVK

3.2. Power Supply Interface

There are three power sources for carrier board, including USB_MODE interface (J401), USB_UART interface (J403) and external power supply input (J201). Connected to the buck converter, it can not only be capable to power peripherals such as MCU SPI FLASH and SD Card in EVB with 3.3 V, but also provide necessary VBAT (3.8 V) in programming carrier board and module.

Considering that the max stream in module is about 2 A, it is suggested to power by external adaptor connecting to J201 jack for sake of stable power supply.

See simplified power diagram and corresponding interfaces. (The dashed line in red as **Figure 7** indicates it is available to short)

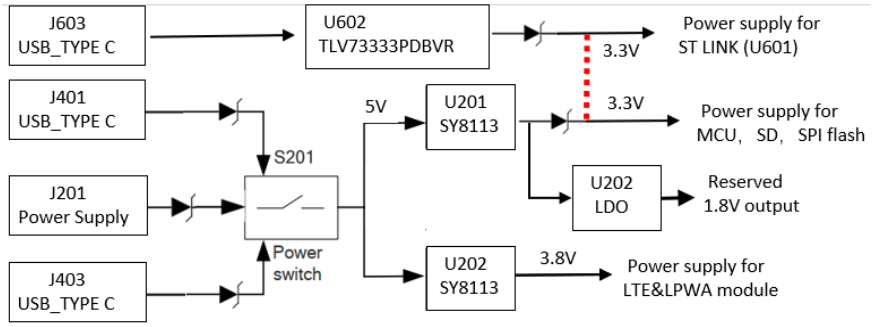


Figure 7: Power Supply for STM32 LQFP64 EVK

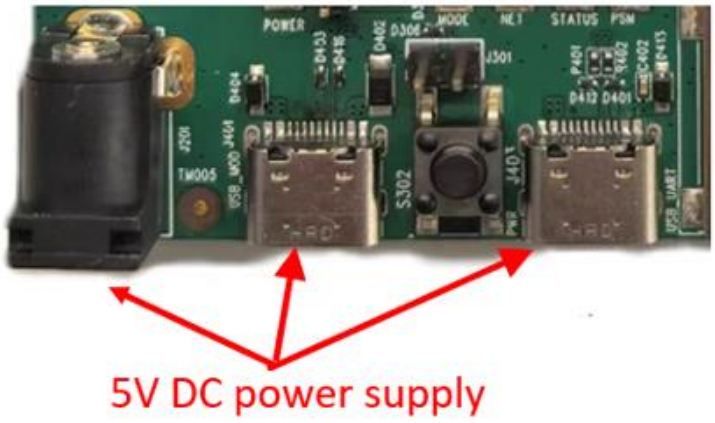


Figure 8: POWER Interface

Before connecting to power, it is mandatory to select adequate DC adaptor (5 V/2 A) for power supply. See following Power Plug Design (DC005-5.5*2.1mm) for reference.

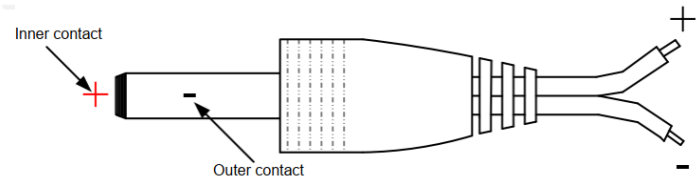


Figure 9: Power Plug Design

3.3. Power Switch (S201)

- Turn the button to the “ON” to power up MCU and TE_A
- Turn the button to the “OFF” to power down MCU and TE_A.

Figure 10: Power Switch

3.4. TYPE-C USB Interface (J401)

Following U401 indicates the USB Switch. Currently, the USB_SWITCH is high level by default. Additionally, the TYPE-C USB interface (J101) is connected to the USB2.0 in LPWA&LTE module, including high-speed (480 Mbps), full-speed (12 Mbps) and low speed (1.5 Mbps). It can be used in AT command communication, data transmission, firmware upgrade and GNSS NEMA Output. Besides that, following M_USB_VBUS can be considered as the power input of the whole carrier board.

Once the USB2.0 in LPWA or LTE module shall communicate with MCU, please pull down USB_SWITCH as LOW.

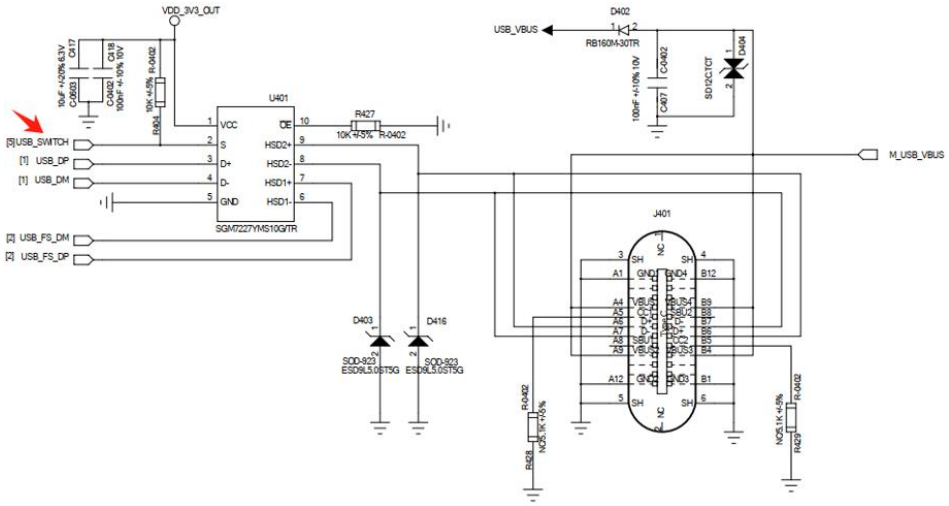


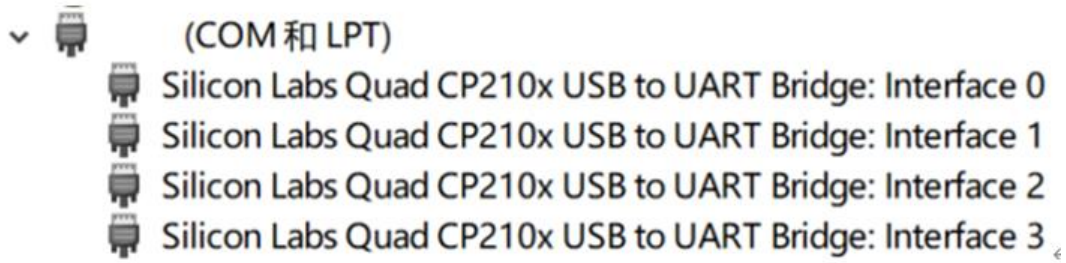
Figure 11: TYPE-C USB Interface Diagram

Note

For USB_SWITCH operation, please refer to *Reserved Debug Interface (Section 3.12) Illustration.*

3.5. TYPE-C USB Interface (J403)

The USB interface on this carrier board connects with CP2108 (USB-to-4*UART) by default. Additionally, 4 ports are virtualized vividly.



- **Interface0**: Connects to DEBUG interface of LPWA&LTE module
- **Interface1**: Connects to MCU DEBUG interface
- **Interface2**: Reserved. Receive data transmitted from module
- **Interface3**: Reserved. Receive data transmitted from MCU

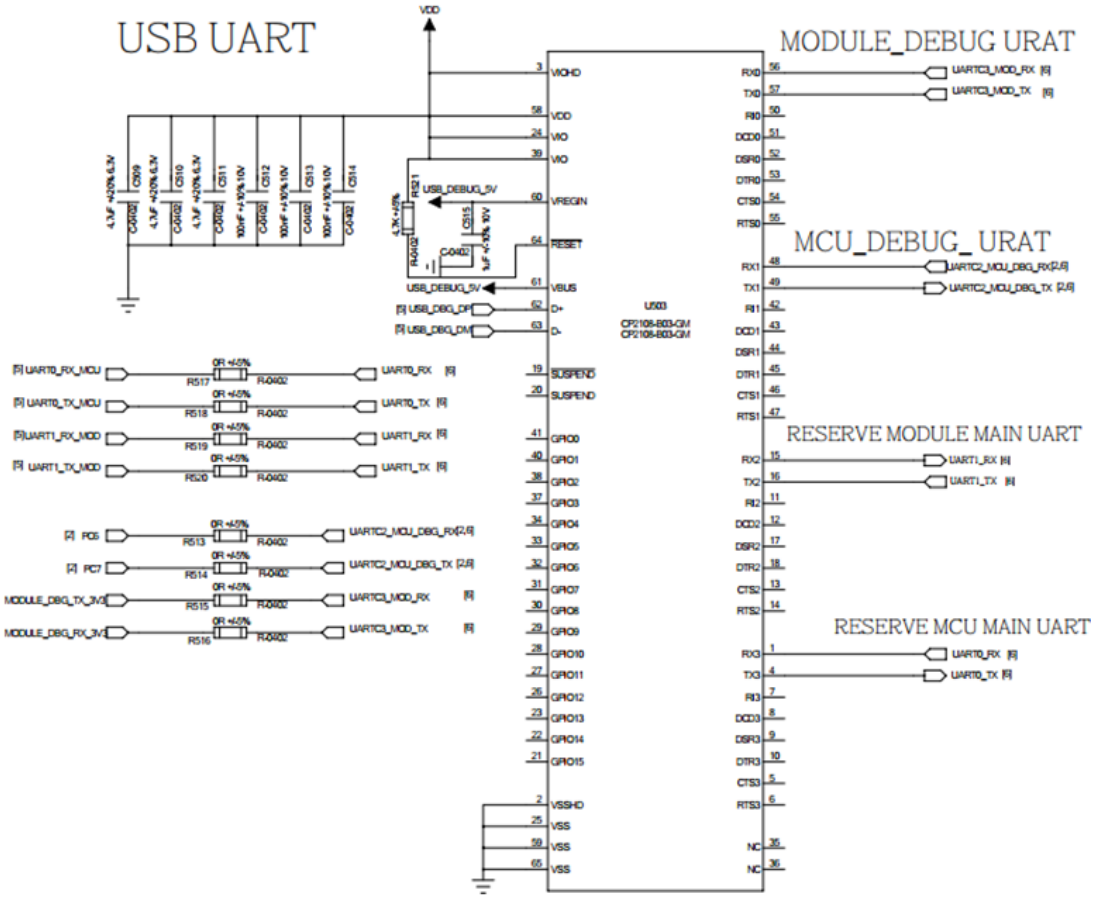


Figure 12: USB-to-UART*4

Note

For Interface2 and Interface3 operation, please refer to *Reserved Debug Interface Illustration.*
Upon specific diagram related to **Figure 12**, please refer to *Reference [1]*

3.6. SIM1 Card Interface

All LPWA&LTE modules support USIM1 definitely. See following USIM1 connection.

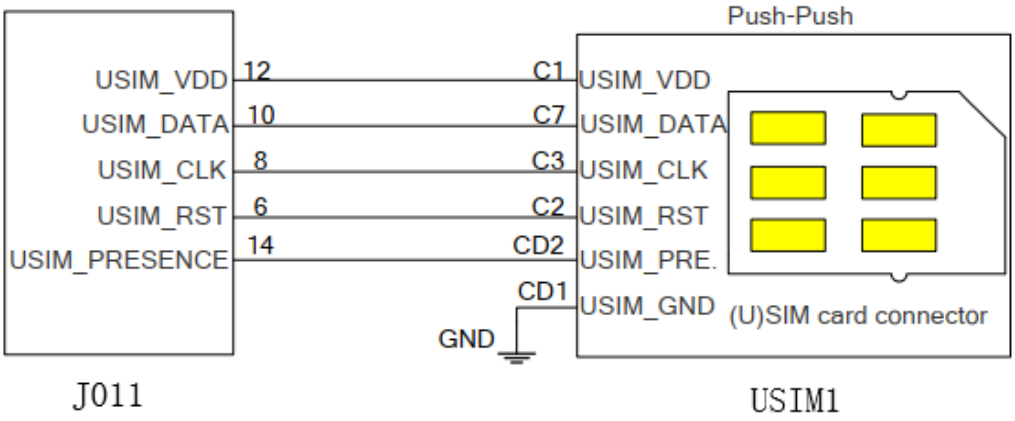


Figure 13: USIM1 Interface Connection

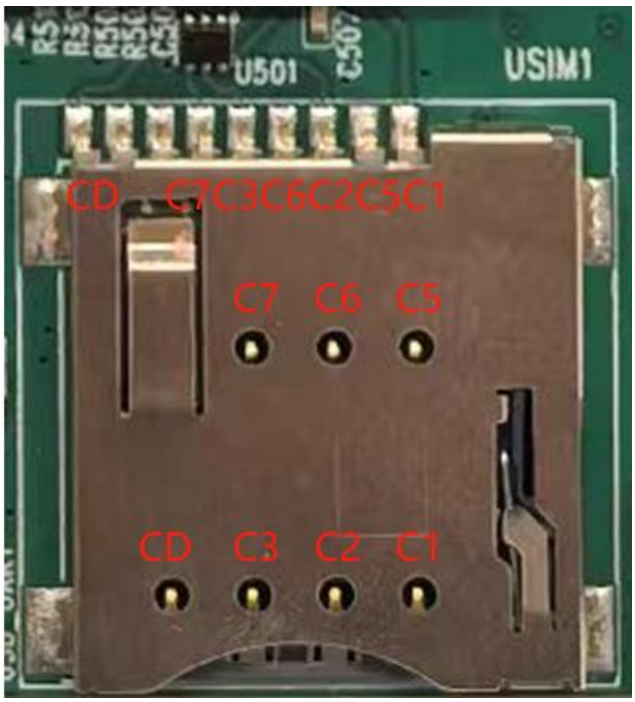


Figure 14: USIM1 Pin Assignment

3.7. Button (PWRKEY/RESET)

The S302 can be used to power on/off LTE&LPWA module.

If corresponding LTE&LPWA module supports always low PWEKEY pin to implement auto start, please short J301 if this function is necessary in debugging module.

Once the module is initiated, if it is necessary to reboot module, please try click S301 button.

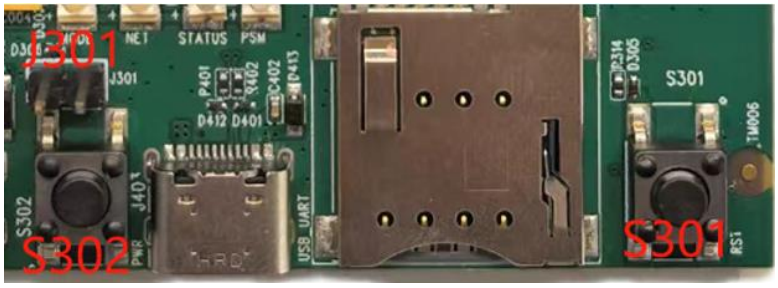


Figure 15: PWRKEY & RESET

3.8. Status Indication LED

This EVB contains 5 status indication LEDs (D206, D301, D302, D303 and D304). See following figure for individual location.

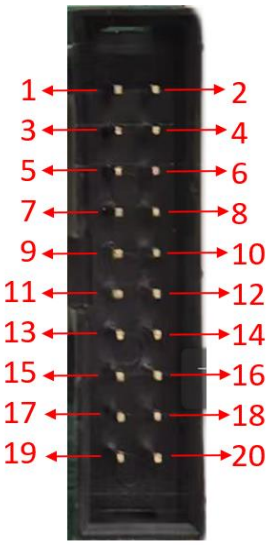
Figure 16: Status indicator

Table 4: LED Status Indicator Illustration

PIN name	Description
D206	Power on/off indicator. Indicates whether the EVB power supply is ready or not.
D301	Network mode indicator, which indicates the registered network status of module Always high Registered on LTE network Always low Others
D303	Network Status indicator, which notifies whether the module is registered Flicker slowly (200 ms high/1800 ms low) Network searching Flicker slowly (1800 ms high /200 ms low) IDLE Flicker quickly (125 ms high/125 ms low) Data Transfer Always high Voice calling
D302	Indicates module's operation status
D304	Sleep indicator/PSM indicator

3.9. JTAG DEBUG Interface

Embedded in EVB, the JTAG interface will make it convenient to debug MCU (U101) or upgrade firmware. See following JTAG interface pin definition.



1	3.3V	2	NC
3	JTRST	4	GND
5	JTDI	6	GND
7	JTMS	8	GND
9	JTCK	10	GND
11	NC	12	GND
13	JTDO	14	GND
15	RST	16	GND
17	NC	18	GND
19	NC	20	GND

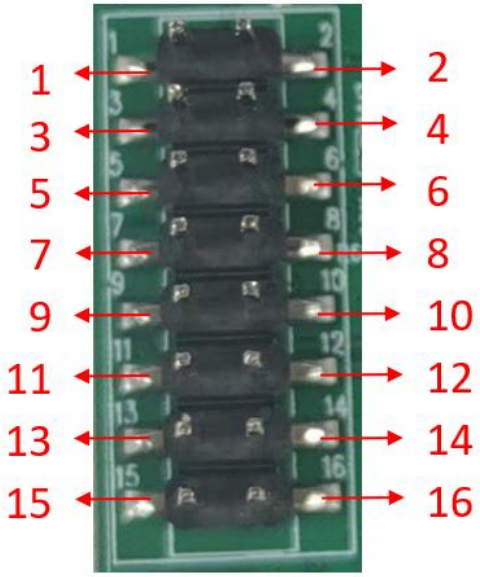
Figure 17: JTAG Pin Definition

Table 5: JTAG Pin Illustration

No.	JTAG Name	Description
1	3.3 V	Power Supply 3.3 V
3	JTRST	Test Reset
5	JTDI	Test Data IN
7	JTMS（JTMS_SWD）	Test Mode Select
9	JTCK	Test Clock
11	NC	
13	JTDO	Test Data Out
15	RST（RST_MCU）	RESET MCU
17	NC	
19	NC	
2	NC	Reserves 0 Ω to Power supply (3.3 V)
4,6,8,10,12, 14,16,18,20	GND	Connects to GND

3.10. SWD DEBUG Interface

Embedded in EVB, the SWD interface will make it convenient in debugging MCU or upgrading firmware. See following SWD interface pin definition.



1	GND	2	USB_ID
3	PB3_SWO	4	STM_SWO
5	PA14_TCK	6	T_JTCK
7	PA13_TMS	8	T_JTMS
9	JT_RST	10	T_NRST
11	VDD_3V3	12	LINK_3V3
13	STLINK_RST	14	STM_JTMS
15	GND	16	STM_TCK

Figure 18: SWD Interface Pin Definition

Table 6: SWD Pin Illustration

No.	SWD Name	Description
1	GND	GND
2	USB_ID	Reserved to switch and control Host-Slave of USB interface in U101. For specific, please refer to Chapter USB_ID
3	PB3_SWO	JTAG interface of U101 for testing data out.
4	STM_SWO	Reserved in U601 to communicate with PB3_SWO in U101
5	PA14_TCK	SWD interface of U101, which serves as CLK pin.
6	T_JTCK	Reserved in U601 to communicate with PA14_TCK in U101. Short PIN5 and PIN6 via Jumper by default.
7	PA13_TMS	SWD interface of U101. DATA I/O pin
8	T_JTMS	Reserved in U601 to communicate with PA13_TMS in U101. Short PIN7 and PIN8 via Jumper Cap by default.
9	JT_RST	RESET pin in U101

10	T_NRST	Reserved in U601 to control U101 RESET pin. Short PIN9 and PIN10 via Jumper
11	VDD_3V3	Default 3.3V Power Supply in U101
12	LINK_3V3	Default 3.3V Power Supply in U601. Short PIN11 and PIN12 via Jumper
13	STLINK_RST	RESET pin in U601
14	STM_TJMS	SWD interface of U601. DATA I/O pin
15	GND	GND
16	STM_TCK	SWD interface of U601, which serves as CLK pin

3.11. USB_ID*

As following figure shows, GND_U, DM, DP and VBUS test points are reserved. Both PA12 and PA11 in MCU can be multiplexed as USB interface, which supports USB OTG.
The reserved USB_ID will be used to switch the USB interface in MCU as HOST or Device. The reserved 2pin for J604 will be taken as USB_ID.
If it is necessary for MCU to multiplex PA12 and PA11 of USB interface as device, the GND_U, DM, DP and VBUS shall be connected.
If it is necessary for MCU to multiplex PA12 and PA11 of USB interface as HOST, please short PIN1 and PIN2 of J604, leaving USB_ID (MCU PA0) as low. Generally, it does not short PIN1 and PIN2 in J604 by default, as a result, the USB_ID (MCU PA0) is high.

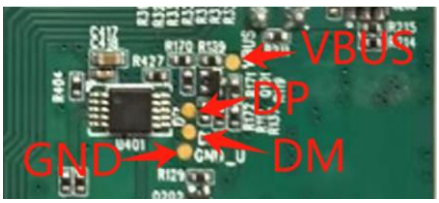


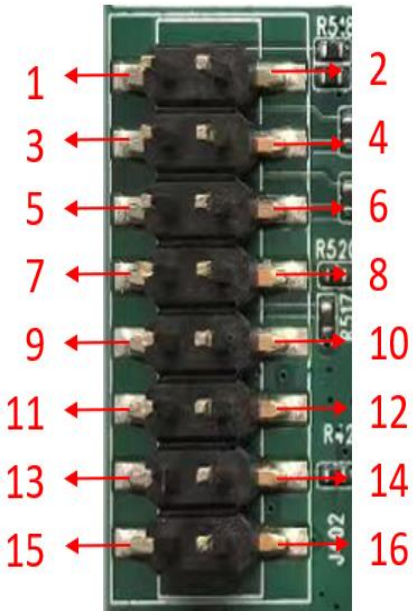
Figure 19: MCU USB Interfaces

Note

1) The high/low USB_ID used to switch as HOST or DEVICE mode is determined by specific SW. Currently, only control port is reserved for further debugging.
2) Please confirm whether the USB interface in MCU shall communicate with LTE&LPWA module, which can be switched via USB_SWICTH.
3) MCU herein described refers to U101 chip.

3.12. Reserved DEBUG Interface (J402)

As one reserved interface, the J402 is capable to implement tests on some common functions by jumping interface socket.



1	UART0_TX	2	UART1_RX
3	MCU_MAIN_RX	4	MAIN_TX
5	MCU_MAIN_TX	6	MAIN_RX
7	UART0_RX	8	UART1_TX
9	GND	10	GND
11	USB_SWITCH	12	1V8_OUT
13	GND	14	VDD_EXT
15	USB_BOOT	16	VDD_EXT_OUT

Figure 20: Reserved Debug Interface Pin Definition

Table 7: Reserved Debug Interface Pin Definition

No.	Pin Name	Description
1	UART0_TX	Reserved for USB-to-TTL Interface3, which will be used to transfer data
3	MCU_MAIN_RX	MCU MAIN RX, which is connected to the MAIN TX of LTE&LPWA module by default
5	MCU_MAIN_TX	MCU MAIN TX, which is connected to the MAIN RX of LTE&LPWA module by default
7	UART0_RX	Reserved for USB-to-TTL Interface3, which will be used to receive data
9，10，13	GND	Connects to GND
11	USB_SWITCH	U401 switches control pins. The pin11 is high level by default, the USB interface of the module is connected to J401. If the 11 pin is connected to ground at a low level, the USB interface of module is connected to the MCU (U101).
15	USB_BOOT	LPWA&LTE Emergency download Port
2	UART1_RX	Reserved for USB-to-TTL Interface2, which will be used to receive data

4	MAIN_TX	LTE&LPWA module MAIN TX, which is connected to the MCU RX by default
6	MAIN_RX	LTE&LPWA module MAIN RX, which is connected to the MCU TX by default
8	UART1_TX	Reserved for USB-to-TTL Interface2, which will be used to transfer data
12	1.8 V	Reserve external 1.8 V
14	VDD_EXT	1.8 V Voltage domain, which is connected to VDD_EXT_OUT by default
16	VDD_EXT_OUT	LTE&LPWA Module VDD_EXT (1.8 V) Power Output

Reserved Debug Interface Function Illustration

- PIN1, PIN7 and PIN9: Reserve one-lane, which is corresponding to USB-to-TTL Interface3.
- PIN2, PIN8 and PIN10: Reserve one-lane, which is corresponding to USB-to-TTL Interface2.
- The voltage in above two lanes is 3.3 V.
- PIN3: MCU_MAIN RX pin. PIN4: LPWA&LTE Module_MAIN TX pin. Generally, PIN3 and PIN4 are connected.
- PIN5: MCU_MAIN TX pin. PIN6: LPWA&LTE Module_MAIN RX pin. Generally, PIN5 and PIN6 are connected.

If it is necessary to monitor the data interacted between MCU and LPWA&LTE module, please short PIN5 and PIN7, PIN2 and PIN4 separately. Additionally, the USB-to-TTL Interface3 and Interface2 can be used to print data.

- USB_SWITCH (PIN11): Always High, which controls U401 (USB Switch chip), allowing communication between LPWA&LTE module and external TYPE-C USB (J401).

By jumping USB_SWITCH (PIN11) and GND (PIN9), the USB_SWITCH pin will turn to low and control U401 (USB switch chip), allowing communication between USB interface in LPWA&LTE module and USB interface multiplexed from PA12 and PA11 in MCU.

- USB_BOOT (PIN15): Emergency download pin. If it is needed to enter emergency download mode, according to the corresponding module, The USB-BOOT can be pulled up to high level (connect 16 pins) or pulled down to ground to low level (connect 13 pins) to enter emergency download mode.
- PIN12: Reserved to connect to external LDO to output 1.8 V. This 1.8 V is manipulated by MCU
- PIN16: VDD_EXT pin to output 1.8 V. Generally, the PIN16 and PIN14 is connected by 0 Ω resistor .

3.13. SD Card Interface

The SD card interface is embedded in carrier board, which will be used to connect between SD card and MCU and save data.

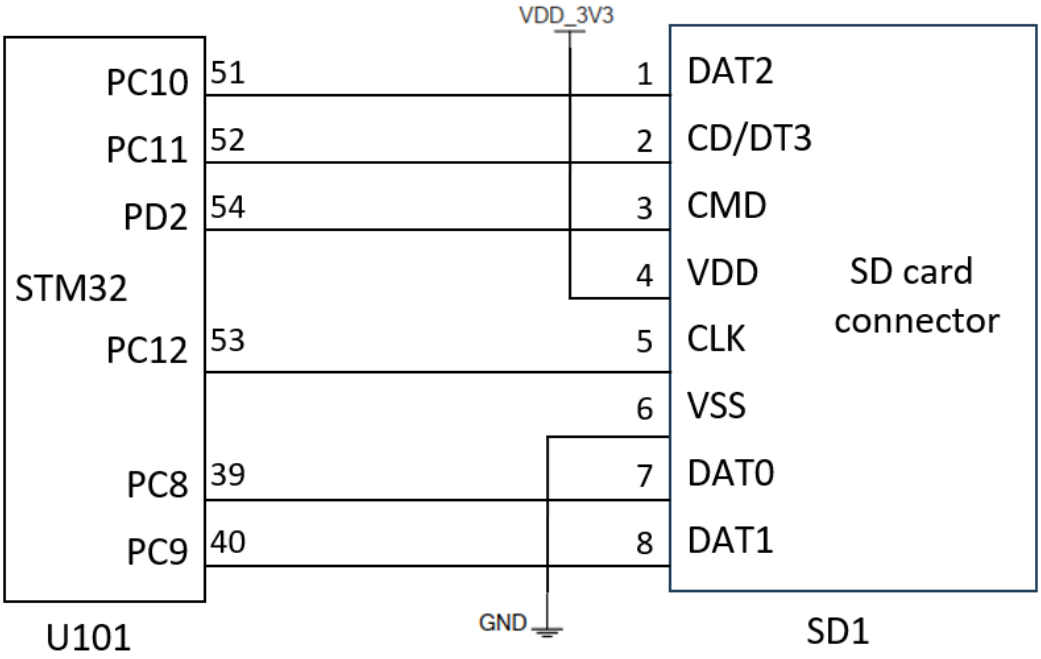


Figure 21: SD & MCU Connection

Figure 22: SD Card Pin Assignment

3.14. SPI FLASH

One SPI FLASH, with a type of W25Q64JVZPIQ (U402), is embedded in carrier board. See following figure in detail.

Figure 23: SPI FLASH Location

Table 8: SPI Flash GPIO Configuration

MCU Port	MCU Pin No.	Function
PA4	32	SPI_NSS
PA5	11	SPI_CLK
PA6	13	SPI_MISO
PA7	15	SPI_MOSI

3.15. USIM2

The carrier board supports USIM1 and USIM2. The USIM1 is on the top of the carrier board while the USIM2 on the bottom. All LTE&LPWA modules support USIM1definitely. However, whether USIM2 is supported or not is determined by specific LTE&LPWA module.

Under the circumstance that the module supports dual sim cards, LPWA&LTE module will support DSSS normally. The SIM card switch will be implemented via AT command.

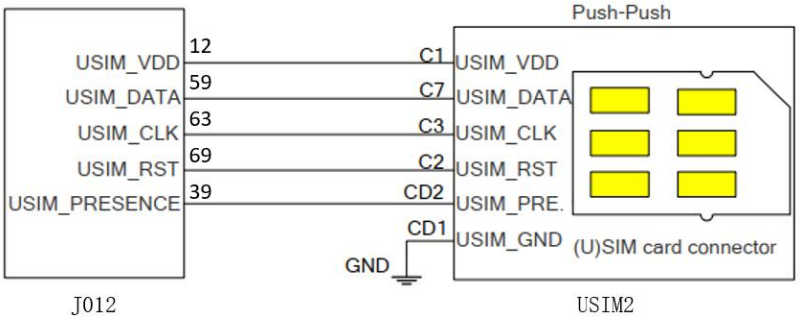


Figure 24: USIM2 Interface Connection

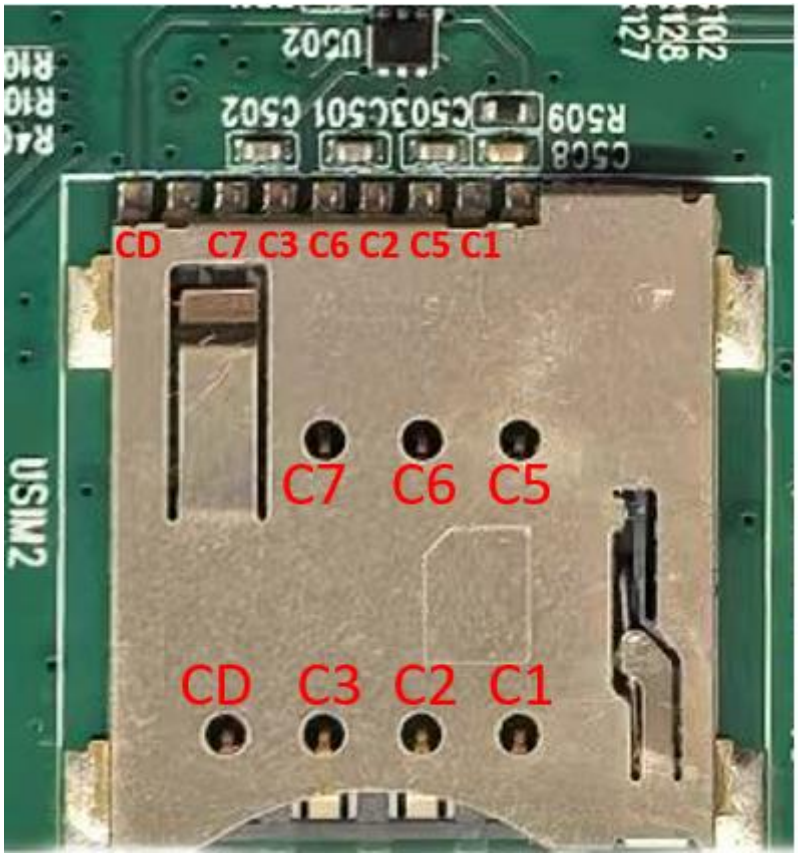


Figure 25: USIM2 Pin Assignment

See following AT commands to switch between USIM1 and USIM2

Take EC25-E module as an example, it is available to switch SIM card via AT command **AT+QDSIM=0/1**. By executing **AT+QDSIM=0**, it will switch as USIM1, which will take effect by rebooting. By executing **AT+QDSIM=1**, it will switch as USIM2. See following procedure.

AT+QDSIM=1 // Switch to USIM2
OK
AT+CFUN=1,1 // Reboot module
OK

AT+QDSIM=0 // Switch to USIM1
OK
AT+CFUN=1,1 // Reboot module
OK

Note

For AT command to switch SIM cards, please refer to corresponding module application documentation.

3.16. MCU Pin Definition

See following descriptions.

Table 9: IO Parameter Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bilateral Port
OD	Open Drain
PI	Power Input
PO	Power Output

Table 10: MCU Pin Function and GPIO Configuration

Pin No.	Pin Name	I/O	Description	Illustration
1	VBAT	PI	VDD	3.3V Input
2	PC13	DI	NET_STATUS	NET Status Detect
3	PC14-OSC32_IN	AI	OSC_IN	32.768K Clock Input
4	PC15- OSC32_OUT	AO	OSC_OUT	32.768K Clock Output
5	PH0-OSC_IN (PH0)	AI	OSC_IN	16M Clock Input
6	PH1- OSC_OUT	AI	OSC_OUT	16M Clock Output
7	NRST	DI	NRST	MCU RESET
8	PC0	DO	PWRKEY	Power ON/OFF. Valid in High Level
9	PC1	DI	RI	RING Detect
10	PC2	DO	PC2	Reserve 1.8V Enable Control.

				Valid in High level
11	PC3	DO	RESET	Control Reset. Valid in High level
12	VSSA/VREF-	GND	GND	GND
13	VDDA/VREF+	PI	VDD	3.3V Input
14	PA0	DI	Module_CTS	Cancel Transfer
15	PA1	DO	Module_RTS	Request Transfer
16	PA2	DO	Module_RX	MCU MAIN_UART TX
17	PA3	DI	Module_TX	MCU MAIN_UART RX
18	VSS	GND	GND	GND
19	VDD	PI	VDD	3.3V Input
20	PA4	DO	SPI1_NSS	SPI FLASH Slave Select
21	PA5	DO	SPI1_SCK	SPI FLASH Clock
22	PA6	DI	SPI1_MISO	SPI SLASH Data RX
23	PA7	DO	SPI1_MOSI	SPI SLASH Data TX
24	PC4	DO	AP_READY	MCU Status Output
25	PC5	DO	DTR	Wakeup
26	PB0	DO	PON_TRIG	Trigger Wakeup from PSM
27	PB1	DI	STATUS	Status Indicator
28	PB2	DI	SLEEP_DET	Sleep Indicator
29	PB10	I/O	NC	
30	PB11/VCAP1	PO		Connect 4.7 uF Capacitor for Internal Power Supply
31	VSS	GND	GND	GND
32	VDD	PI	VDD	3.3 V Input
33	PB12	DO	W_DISABLE	Control Module Airplane Mode
34	PB13	DO	USB_RENUMn	USB Enumeration Operation Control

35	PB14	I/O	NC	MCU_ID,Reserved pull up/down resistors by default
36	PB15	DO	USB_OTG_EN	USB_VBUS Input Detect Control
37	PC6	DO	DEBUG_RX	MCU DEBUG_UART TX
38	PC7	DI	DEBUG_TX	MCU DEBUG_URAT RX
39	PC8	I/O	SDIO_D0	SD Card Bus DATA0
40	PC9	I/O	SDIO_D1	SD Card Bus DATA1
41	PA8	DI	NET_MODE	Network Mode Detect
42	PA9	DI	USB_VBUS_DET	MCU USB Slave Mode Input Detect
43	PA10	DI	USB_ID	MCU USB Interface Host-slave Handover Control
44	PA11	I/O	USB_DM	USB Differential Data Negative Signal
45	PA12	I/O	USB_DP	USB Differential Data Positive Signal
46	PA13 (JTMSSWDIO)	I/O	TDO	JTAG: Select test mode SWD: Data IN/OUT
47	VSS	GND	VSS	GND
48	VDD	PI	VDD	3.3V Power Input
49	PA14 (JTCKSWCLK)	DI	TCK	JTAG: Clock Signal SWD: Clock Signal
50	PA15 (JTDI)	DI	TDI	JTAG: Test Data IN
51	PC10	I/O	SDIO_D2	SD Card BUS DATA2
52	PC11	I/O	SDIO_D3	SD Card BUS DATA2
53	PC12	DO	SDIO_CK	SD Card BUS Data Clock
54	PD2	I/O	SDIO_CMD	SD Card BUS Data Command
55	PB3 (JTDO-SWO)	DO	SWO	JTAG: Test Data OUT
56	PB4 (NJTRST)	DI	NJTRST	JTAG: Test Reset
57	PB5	DO	WAKEUP_IN	WAKEUP Module
58	PB6	DO	POWER_ON	Power ON Module

59	PB7	DI	DCD	Carrier Detect (Reserved)
60	BOOT0	DI	BOOT0	Connect 10K Resistor to GND
61	PB8	DO	SD_EN	SD Card Power Enable Control
62	PB9	DI	SD_IN_DET	SD Card Insertion Detect
63	VSS	GND	GND	GND
64	VDD	PI	VDD	3.3V Power Input

4 Appendix A Reference (TBD)

Table 11: Referential Documents

Document Name	Illustration
[1] STM32 LQFP64 EVK V2.0.pdf	
[2] STM32-LQFP64 EVK V2.0-TOP SILK SCREEN.pdf	
[3] STM32-LQFP64 EVK V2.0-BOTTOM SILK SCREEN.pdf	