

# Queen's Power Group

Kingston, Ontario, Canada

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## A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters

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# Presentation Overview



- 1. Introduction***
- 2. Limitations of Conventional Control Methods During a Load Transient**
- 3. Proposed Optimal Transient Response Algorithm**
- 4. Derivation of the Optimal Control Algorithm for Practical Implementation**
- 5. Experimental Results**
- 6. Conclusions**

# 1. Introduction

- **Increasing demand for dynamic performance including:**
  - Minimum output voltage overshoot/undershoot
  - Minimum output voltage recovery time
- **Output voltage deviates under line or load changes**
- **Different control algorithms achieve different dynamic performance**

# Introduction Continued ...



- In theory there exists a best possible dynamic performance
  - Minimum overshoot and/or recovery time
- **KEY:** determine best possible dynamic response and a method to realize it!
- Paper proposes an optimal control algorithm using principle of capacitor charge balance
  - Algorithm implemented digitally using an FPGA

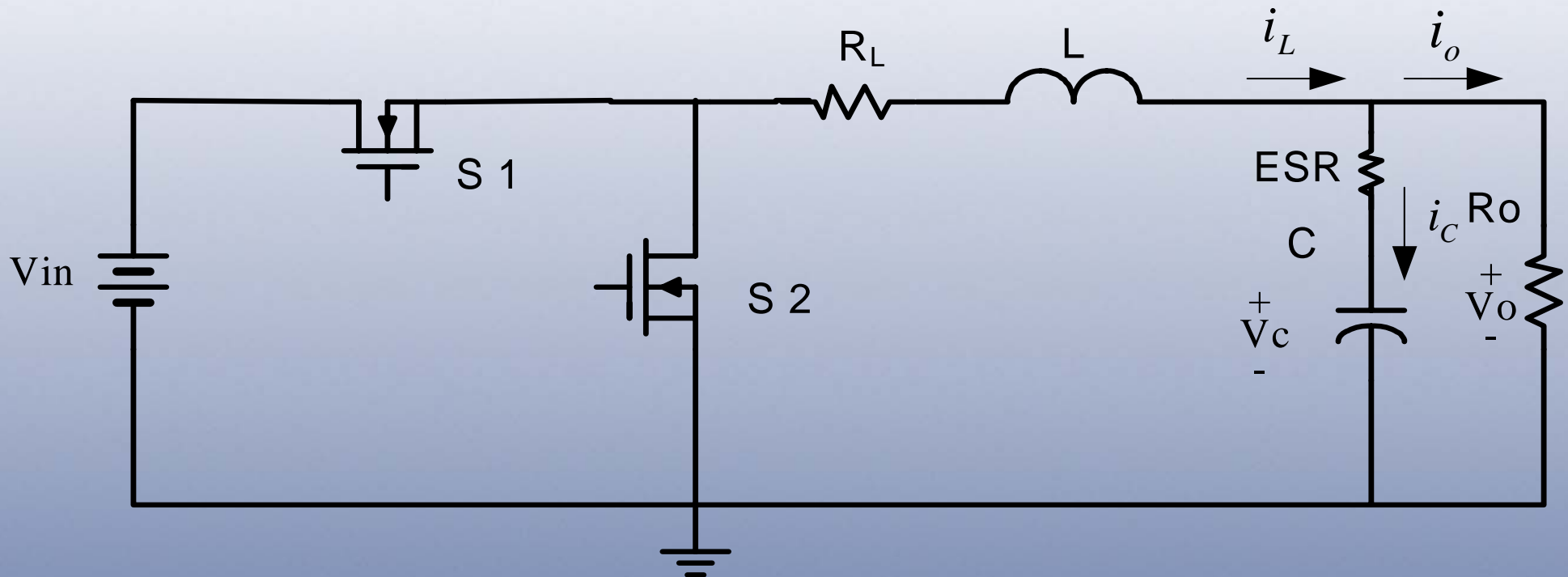
# Presentation Overview



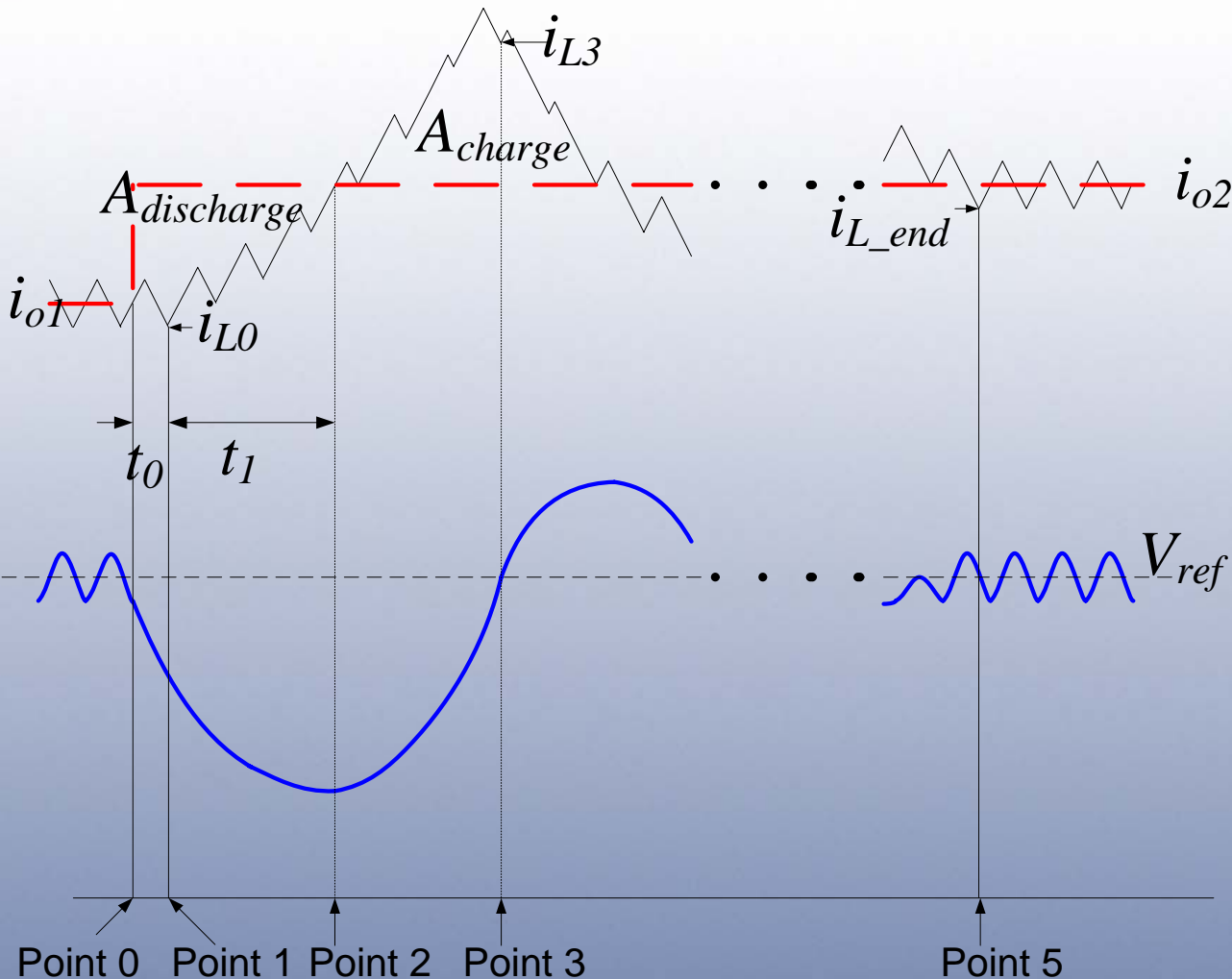
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## 2. Limitations of Conventional Control Methods During a Load Transient

**e.g. Buck converter under voltage mode control**



# Voltage Mode Controlled Buck: Positive Load Current Step



## Point 0:

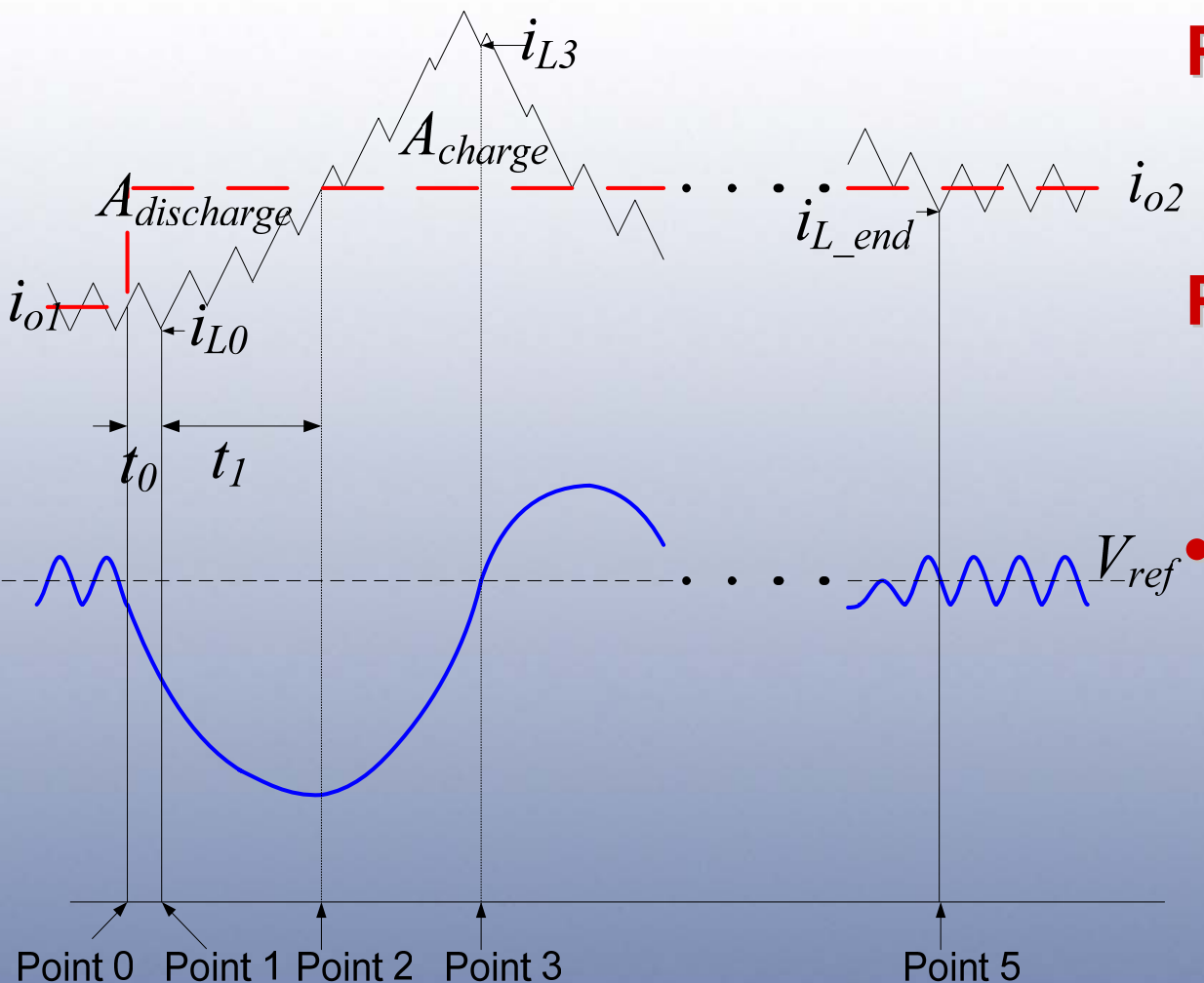
1. Load steps
2. Output not sensed yet
3.  $I_L$  unchanged
4. Capacitor discharges

## Point 1:

1. Output drop sensed
2.  $D$  increases
3.  $I_L$  increases
4. But,  $I_L < i_o$
5. Capacitor continues to discharge



# Voltage Mode Controlled Buck: Positive Load Current Step



## Point 2:

1.  $I_L = I_o$ , cap drop is maximum

## Point 3:

1. Transient continues to point 3 and beyond

**D never 100% !!!**

- Response not optimal
- similar response for other linear methods



# Voltage Mode Controlled Buck: Positive Load Current Step



## **DISADVANTAGE - D not 100% during $t_1$ :**

- Inductor current does not increase at max possible slew rate
- $t_1$  is NOT minimized
- $A_{\text{discharge}}$  is not minimized
- Capacitor voltage drop is not minimized

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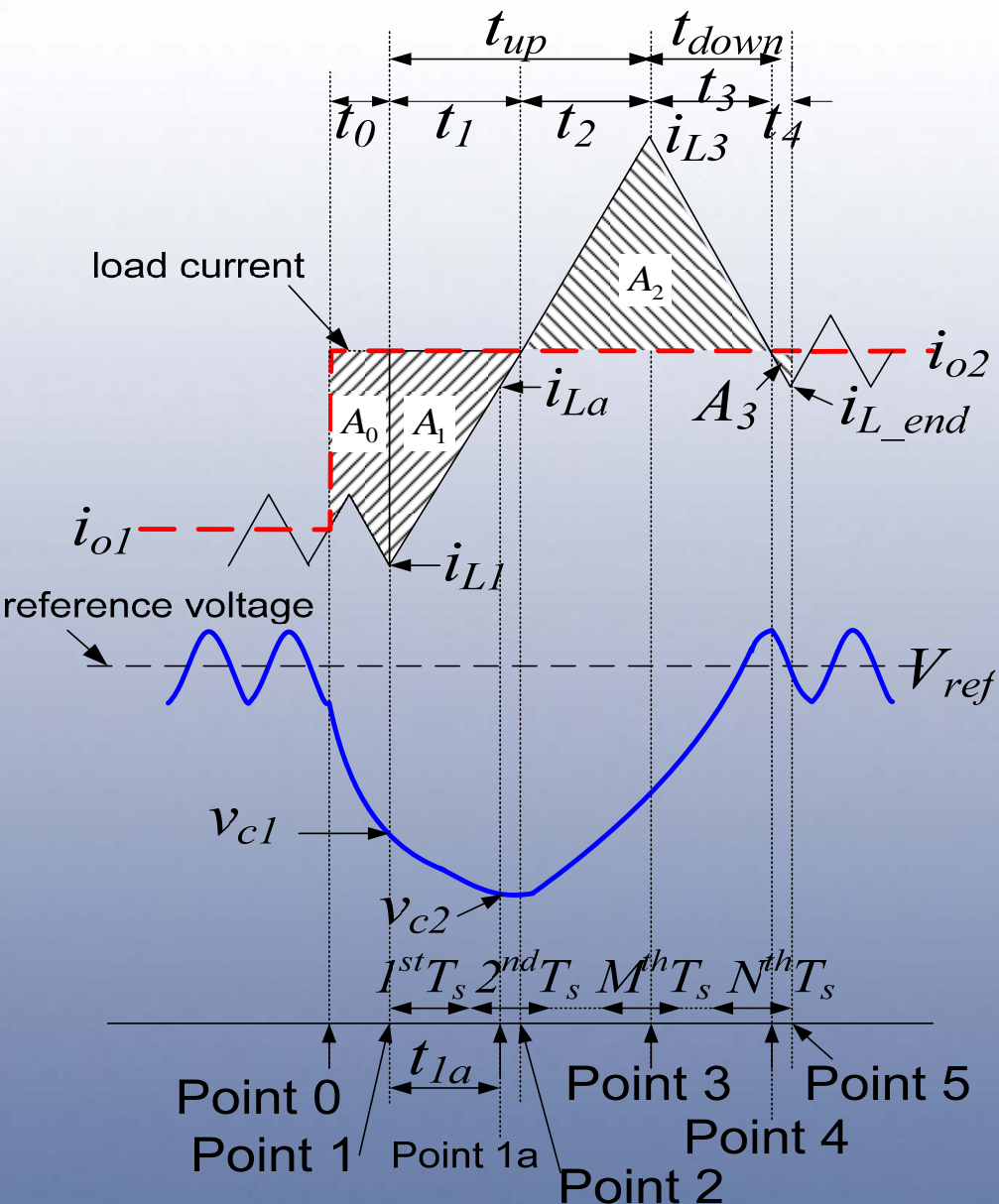
### 3. Proposed Optimal Transient Response Algorithm



**Necessary and sufficient conditions for the best possible dynamic performance:**

1.  $I_L$  rise at max slew rate at beginning of transient, then at the peak it should drop at max slew rate
2. Transient ends when capacitor charge balance is achieved
3.  $D$  set to new steady-state value at end of transient

# Optimal Transient Response Algorithm Under Load Step



- **Point 0:**

1. Load steps
2. Output not sensed yet
3.  $I_L$  unchanged
4. Capacitor discharges

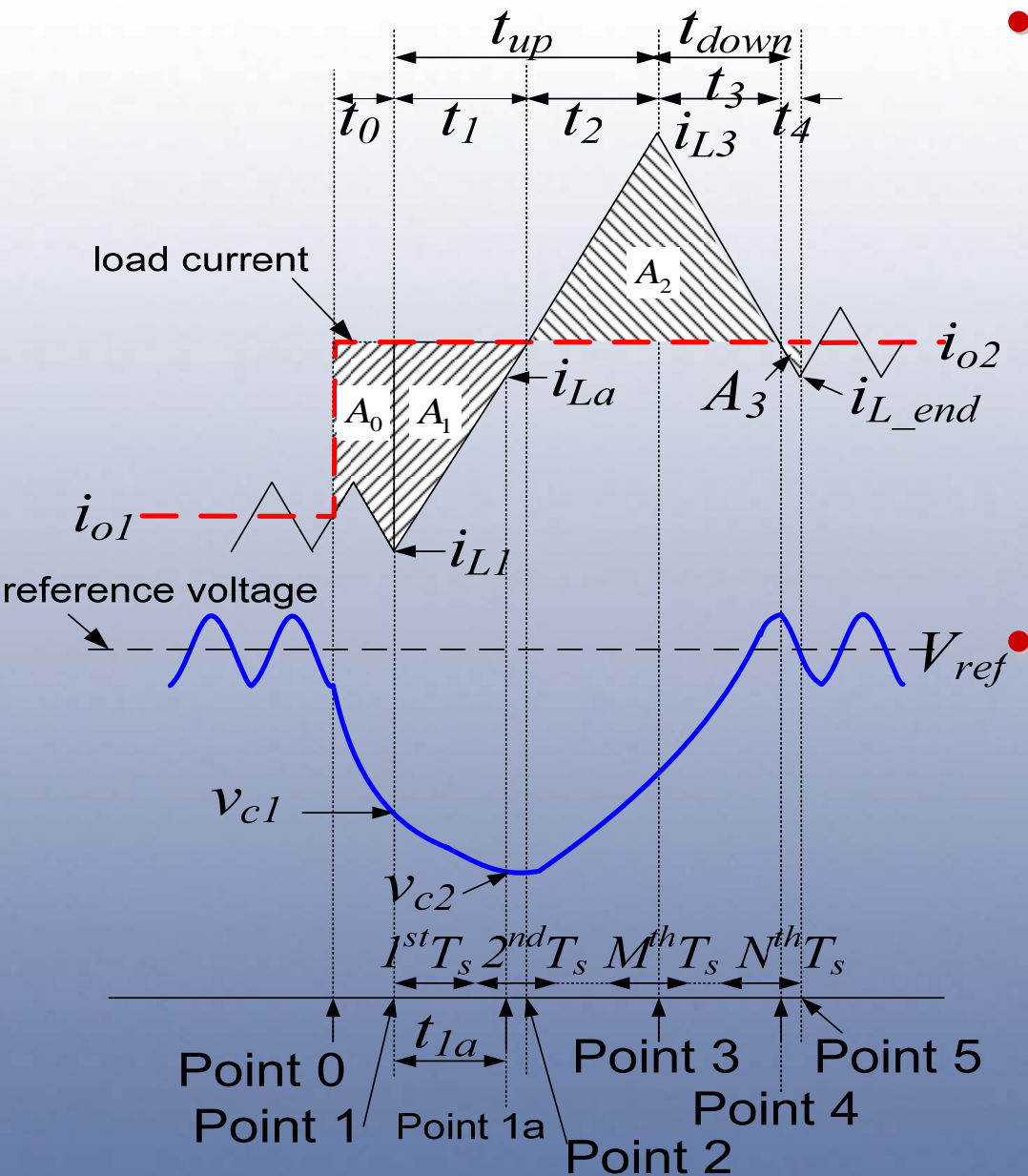
- **Point 1:**

1. Output drop sensed as large signal transient
2.  $D=100\%$
3.  $I_L$  increases at max slew rate
4. But,  $I_L < i_o$
5. Capacitor continues to discharge

- **Point 2:**

1.  $I_L = i_o$ ,
2. Capacitor drop is maximum
3.  $D$  continues at 100%

# Optimal Transient Response Algorithm Under Load Step



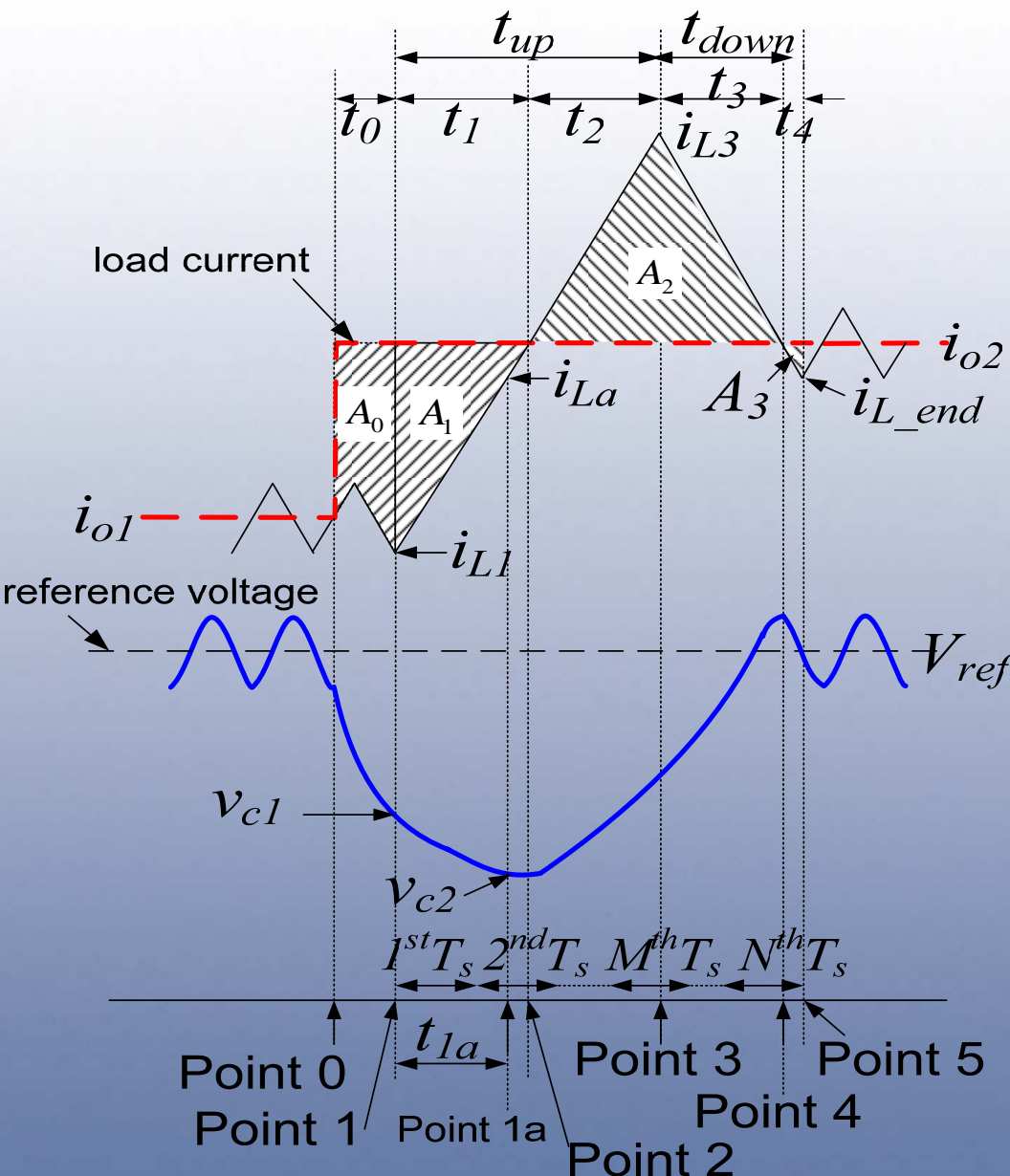
## Point 3:

1. Inductor current reaches peak,  $i_{L3}$  using optimum  $t_{up}$
2. Inductor current then enters maximum down slope interval until point 4
3.  $D=0\%$
4.  $i_L > i_o$

## Point 4:

1.  $i_L = i_o$
2.  $D=0\%$
3.  $i_L$  continues to decrease until end of switching cycle at point 5

# Optimal Transient Response Algorithm Under Load Step



## Point 5:

1.  $i_L$  reaches new steady-state value,  $i_{L\_end}$
2. Charge delivered from capacitor = charge delivered to capacitor
3. Large signal transient ends
4. Conventional small-signal controller takes over

## KEY - need to determine:

- Optimized up time,  $t_{up}$
- Optimized down time,  $t_{down}$



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## 4. Derivation of the Optimal Control Algorithm for Practical Implementation



- **Equations used for digital implementation**
- **Covered in more detail in the paper**
- **Six key steps after sensing large signal transient condition:**

1. **Sense large signal transient in output voltage, then apply maximum rising slew rate**

$$\frac{di_L}{dt} = \frac{v_{in} - v_o}{L}$$

2. **Estimate new load,  $i_{o2}$**

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{La}) - \frac{C \cdot (v_{0a} - v_{o1}) - C \cdot (i_{La} - i_{L1}) \cdot ESR}{t_{1a}}$$

# Derivation of the Optimal Control Algorithm for Practical Implementation

## 3. Calculate capacitor discharge portion $A_0$

$$A_0 = C \cdot (v_{C0} - v_{C1}) \approx C \cdot (V_{ref} - v_{C1}) = C \cdot (V_{ref} - v_{o1} + i_{C1} \cdot ESR)$$

$$= C \cdot (V_{ref} - v_{o1} + (i_{L1} - i_{o2}) \cdot ESR)$$

## 4. Calculate $t_1$ and discharge portion $A_1$

$$t_1 = \frac{i_{o2} - i_{L1}}{(v_{in} - v_o') / L} \quad A_1 = \frac{1}{2} t_1 (i_{o2} - i_{L1})$$

## 5. Calculate $t_4$ and discharge portion $A_3$

$$t_4 = \frac{i_{o2} - i_{L\_end}}{v_o' / L} \quad A_3 = \frac{1}{2} t_4 \cdot (i_{o2} - i_{L\_end})$$

## 6. Calculate charge $A_2$ and time periods $t_2$ and $t_3$

$$A_2 = \frac{1}{2} (t_2 + t_3) \cdot (i_{L3} - i_{o2}) \quad t_2 = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2} \frac{v_{in}}{v_o'} \frac{v_{in} - v_o'}{L}}} \quad t_3 = \frac{v_{in} - v_o'}{v_o'} t_2$$

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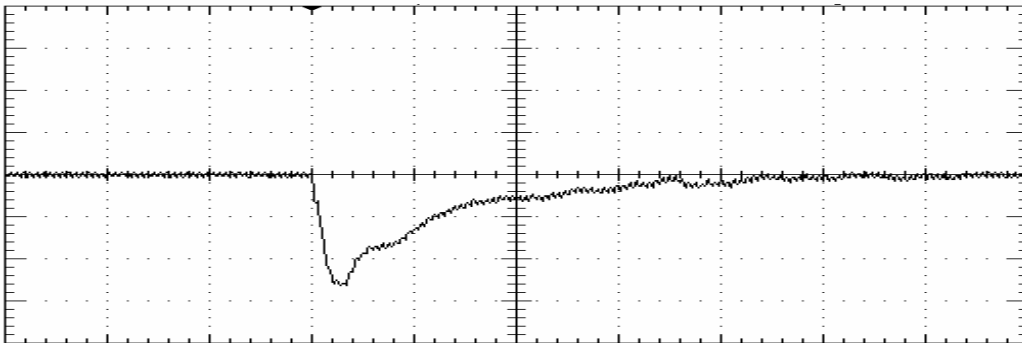


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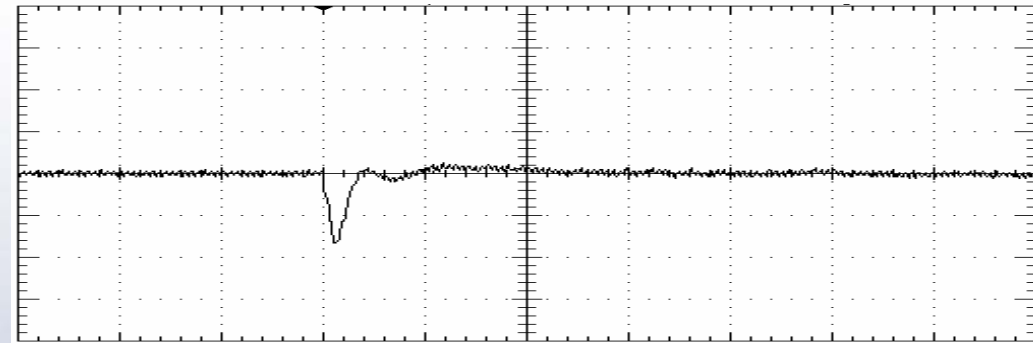
# 5. Experimental Results

- **FPGA was used to implement the proposed optimal control algorithm with a synchronous buck converter**
- **Buck Parameters:**
  - $V_{in}=5V$
  - $V_o=2.5V$
  - load power=25 W
  - $L=1\mu H$ ,
  - $C=235\mu F$
  - $ESR=1m\Omega$
  - $R_L=2m\Omega$
  - $f_s=400khz$

# Output Voltage Response to Load Step from 0A to 5A



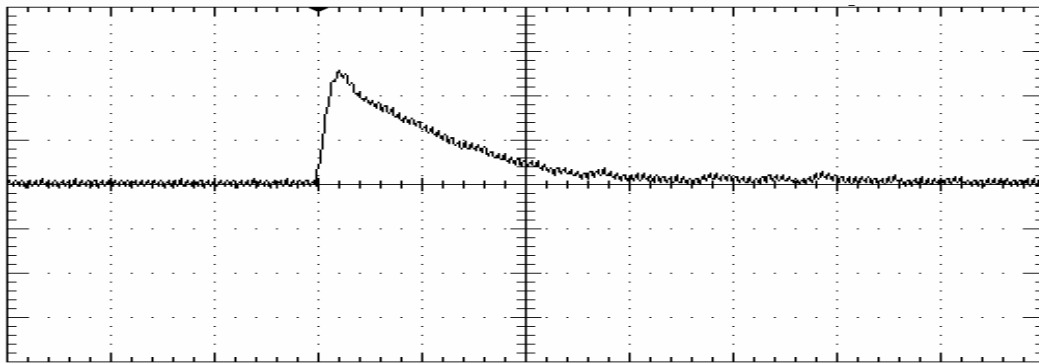
(a) Current mode PID controller



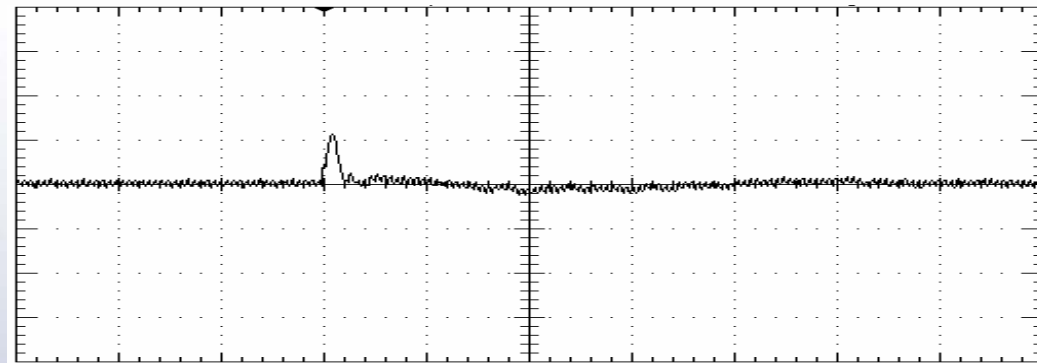
(b) Proposed optimal control algorithm

(X axis: 40us/div; Y axis: 50mv/div)

# Output Voltage Response to Load Step from 5A to 0A



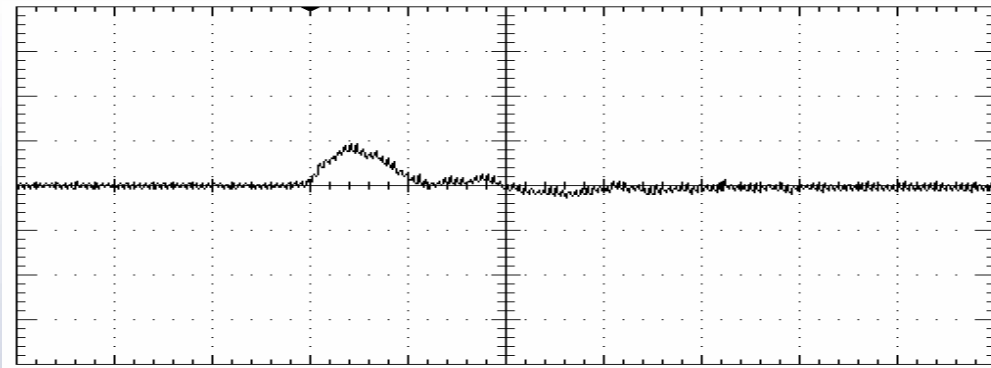
(a) Current mode PID controller



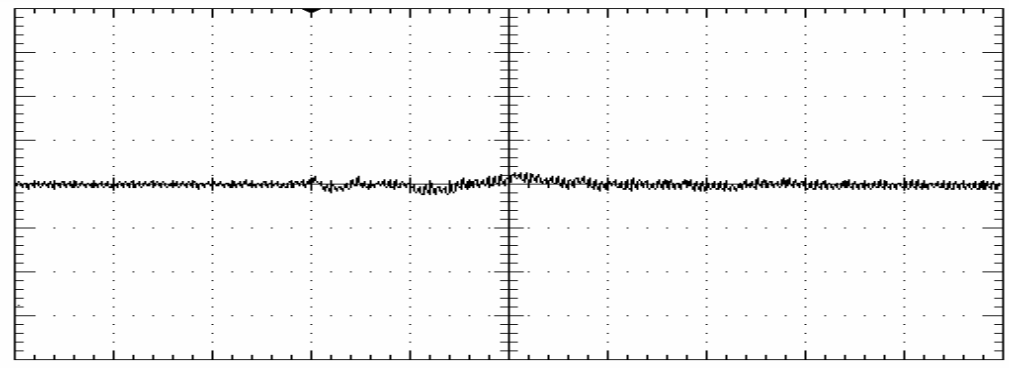
(b) Proposed optimal control algorithm

(X axis: 40us/div; Y axis: 50mv/div)

# Output Voltage Response to Input Step from 5V to 7.5V



(a) Current mode PID controller



(b) Proposed optimal control algorithm

(X axis: 40us/div; Y axis: 50mv/div)



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## 6. Conclusions

- New optimal control algorithm to improve DC-DC converter dynamic performance proposed
- Capacitor charge balance is used to determine the optimal number of switching cycles to return the output to its nominal value
- *Minimum overshoot/undershoot and recovery time is achieved*
- Algorithm is implemented digitally
- Thank you for attending ... questions???