Topology and Analysis of a New Resonant Gate Driver

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Outline

- Introduction
- Proposed Resonant Gate Driver and Operation
- Loss Analysis and Optimization Design
- Experimental Results
- Conclusion

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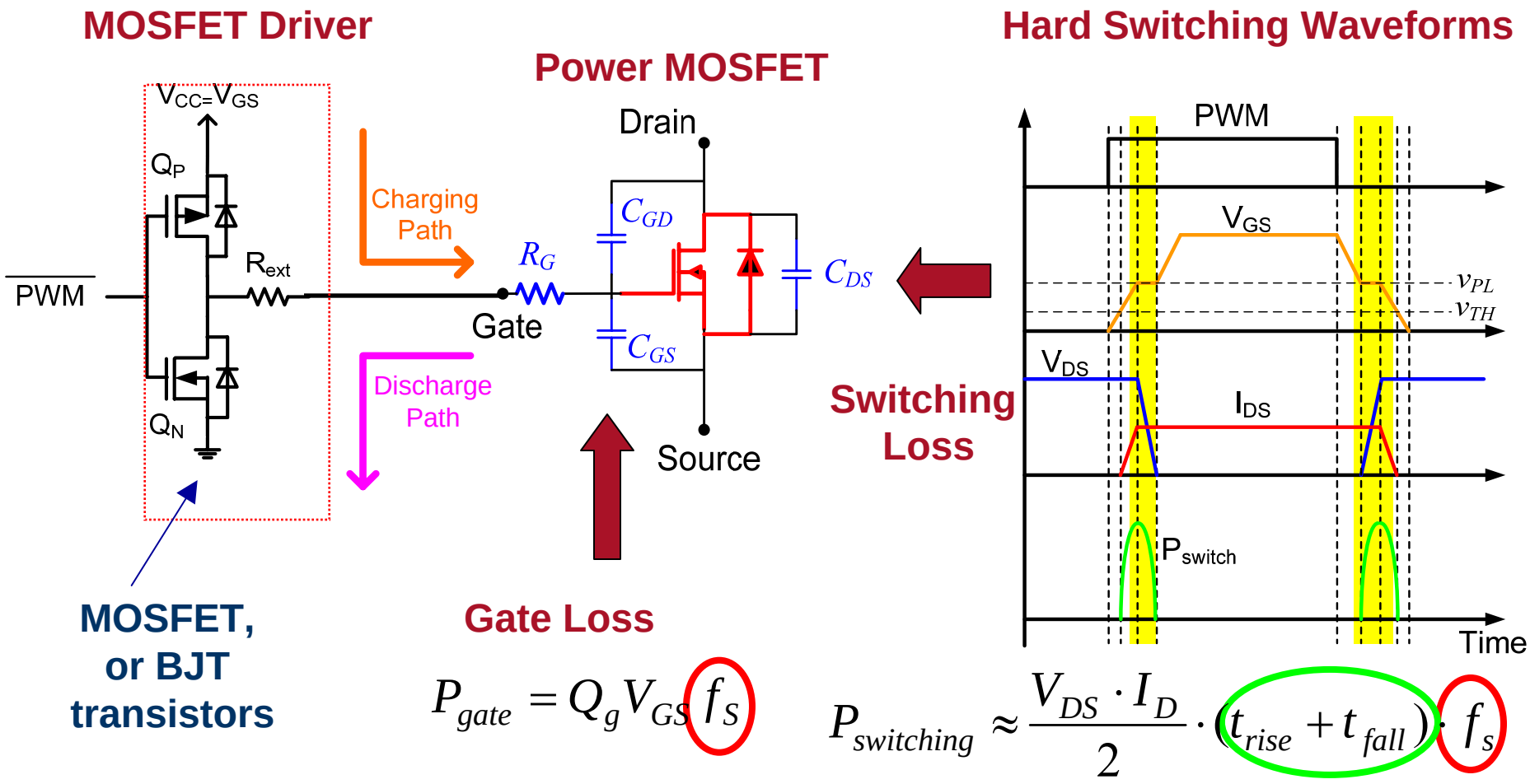
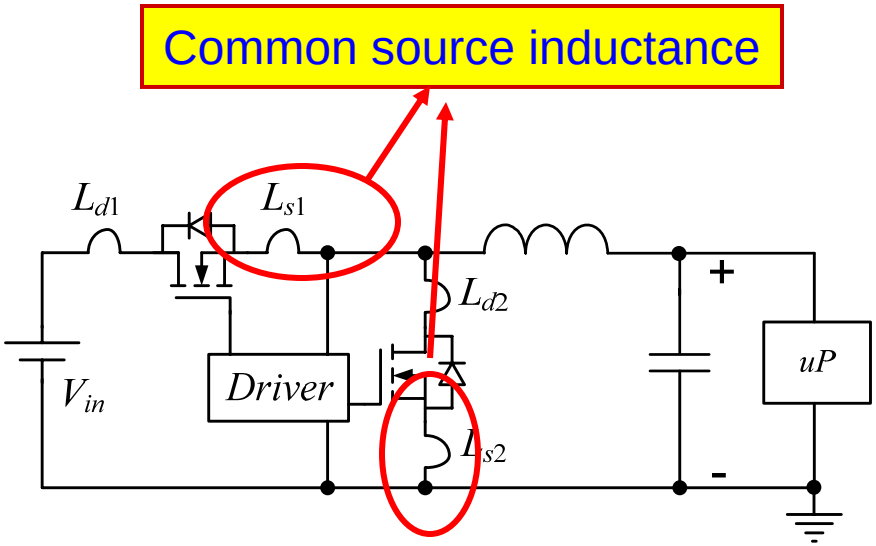
Conventional MOSFET Driver



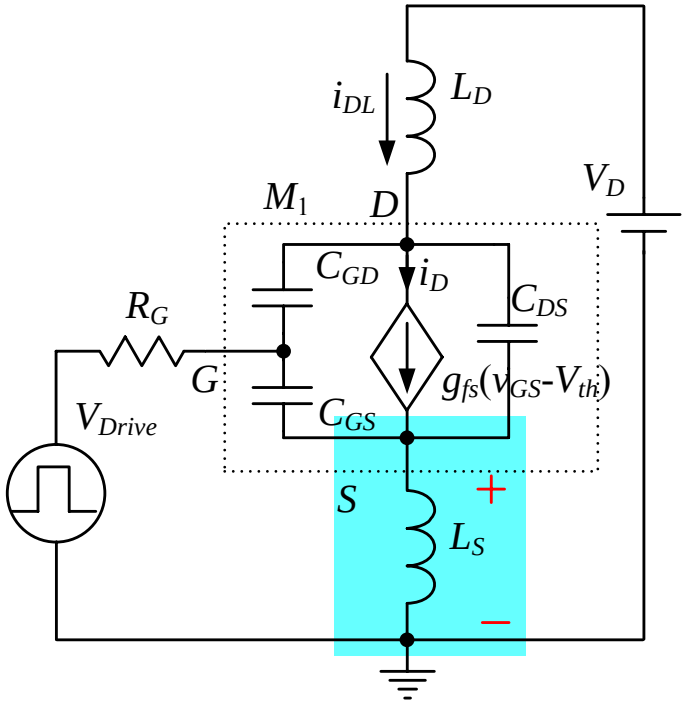
$$P_{gate} = Q_g V_{GS} f_S$$

$$P_{switching} \approx \frac{V_{DS} \cdot I_D}{2} \cdot (t_{rise} + t_{fall}) \cdot f_s$$

Switching Loss: Common Source Inductance

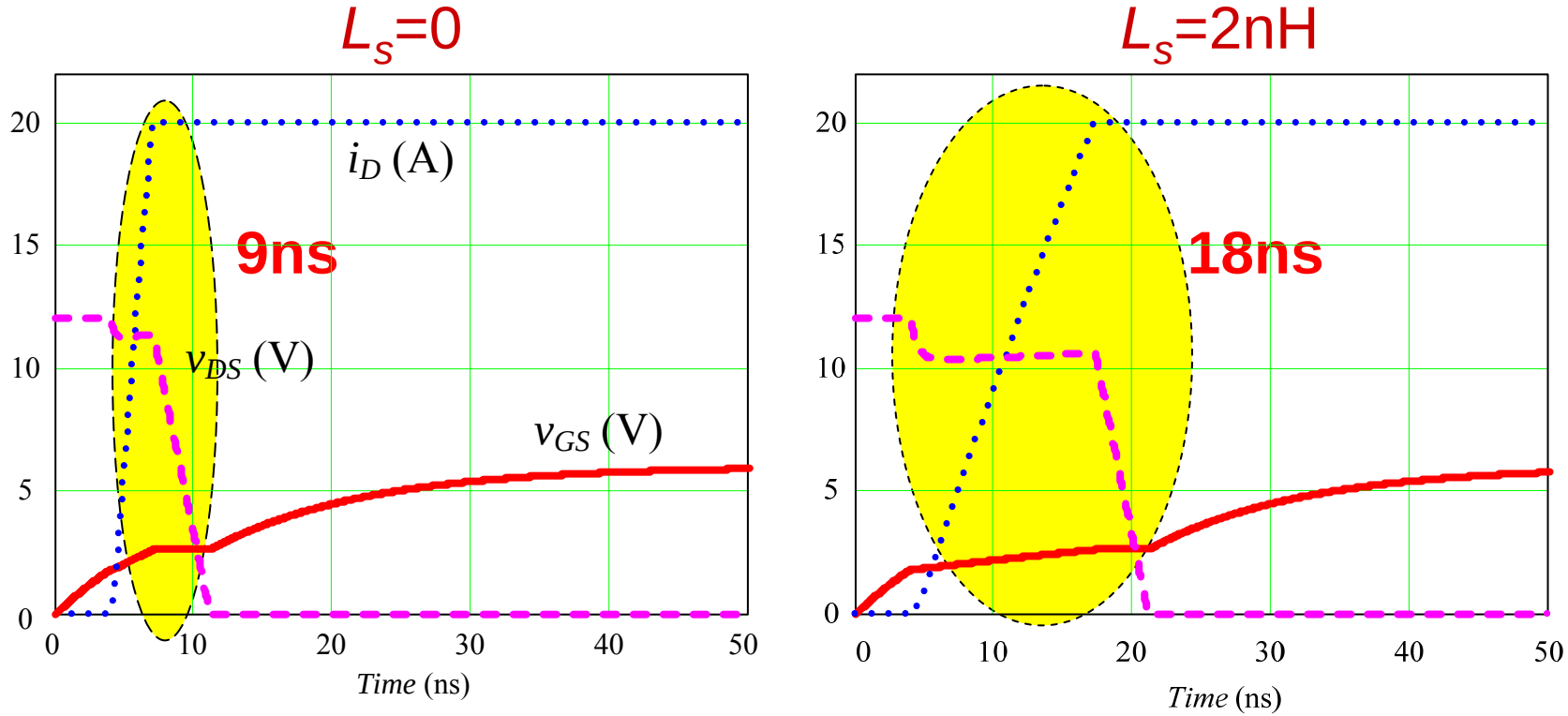


Buck converter with parasitic inductors



Equivalent circuit of MOSFET switching transition (turn-on)

Switching Loss: Common Source Inductance



V_D=12V, I_L=20A, f_s=1MHz, MOSFET: IRF7821

Switching loss increases significantly due to common source inductance!

Resonant Gate Drive Techniques

Limitations of voltage source driver:

- No gate charge energy recovered
- Low switching speed and high switching loss due to common source inductance

Resonant gate driver techniques:

- ✓ Many good circuits proposed since 1990s, but generally unused
- ✓ Existing methods emphasize gate energy savings, but ignore **potential switching loss savings**

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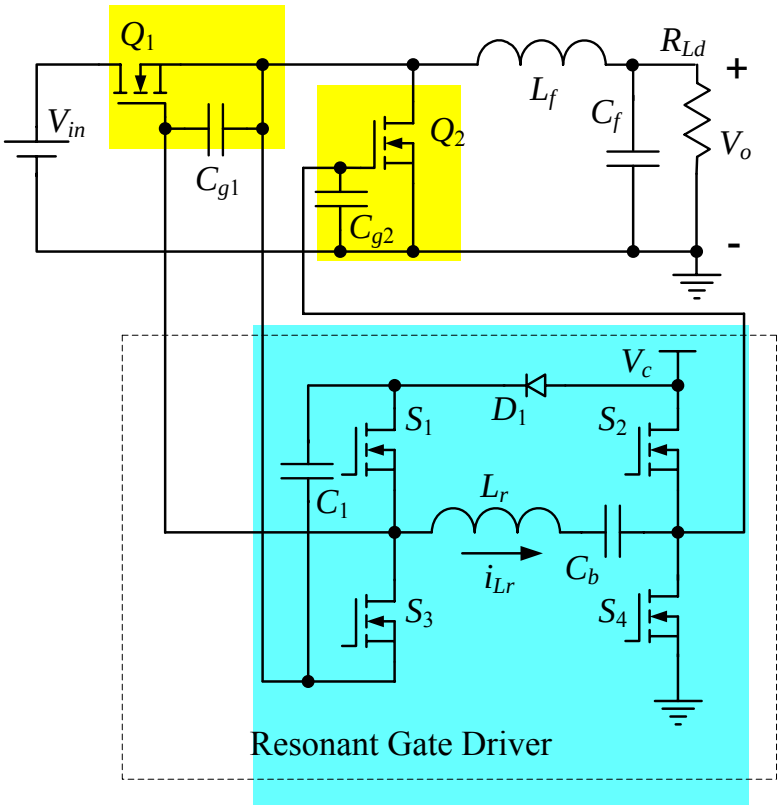
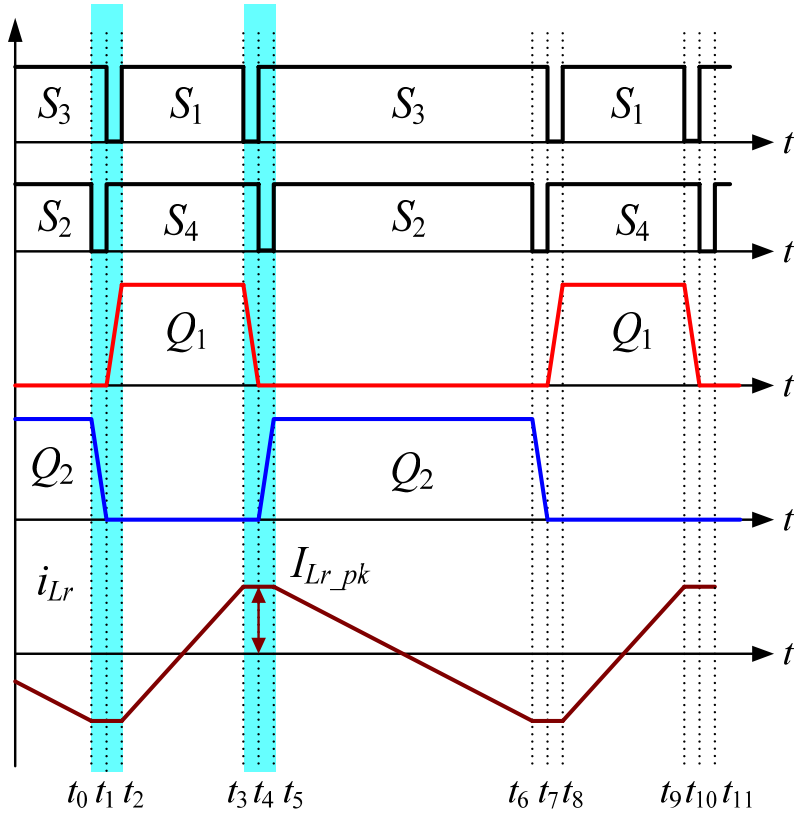
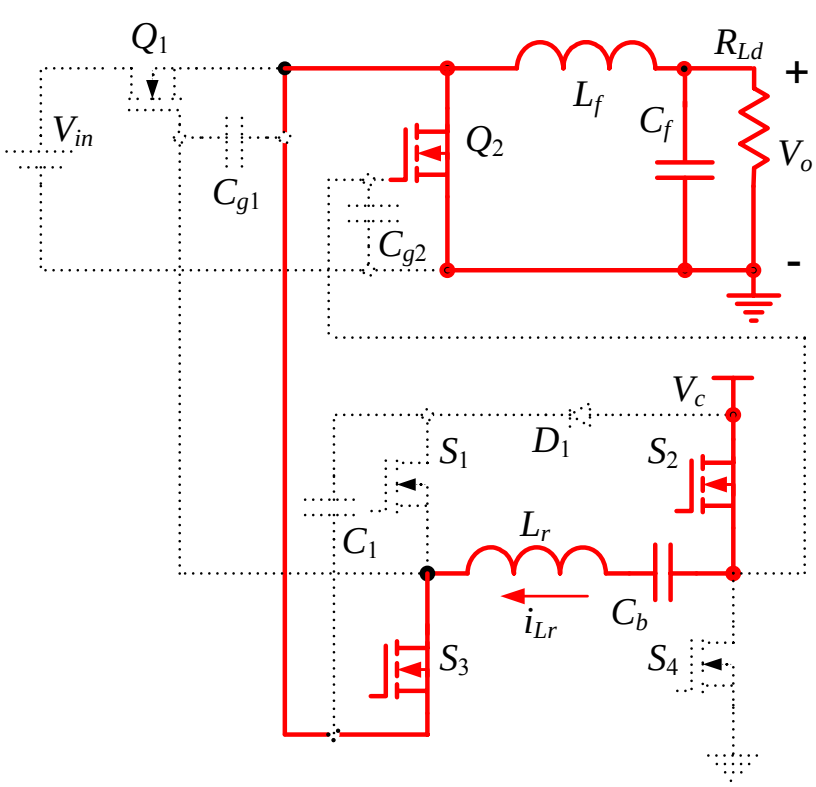
Proposed Dual Channel High-Side and Low-Side Gate Driver

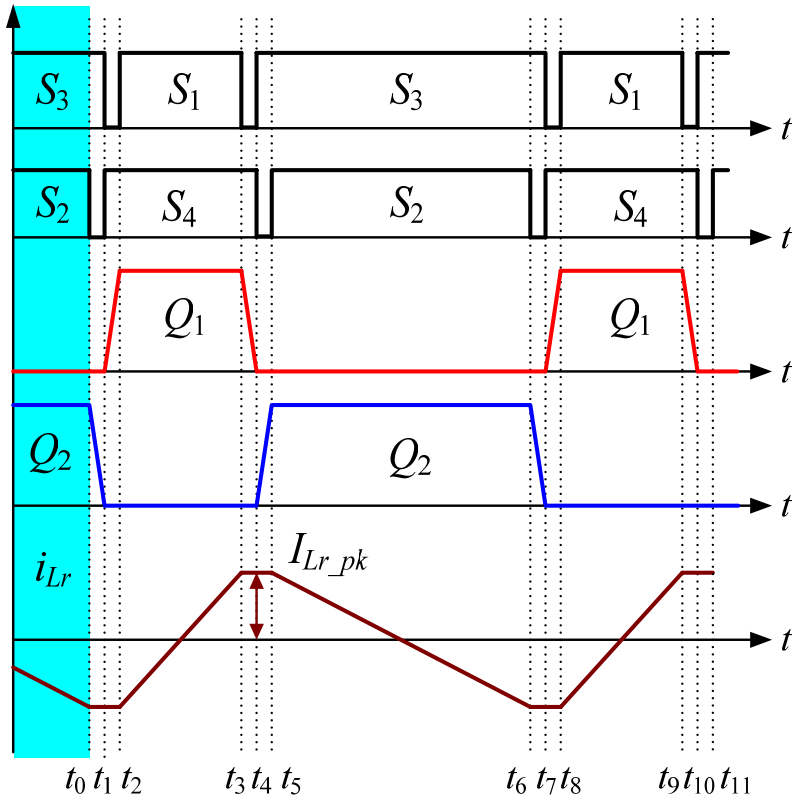




Key waveforms

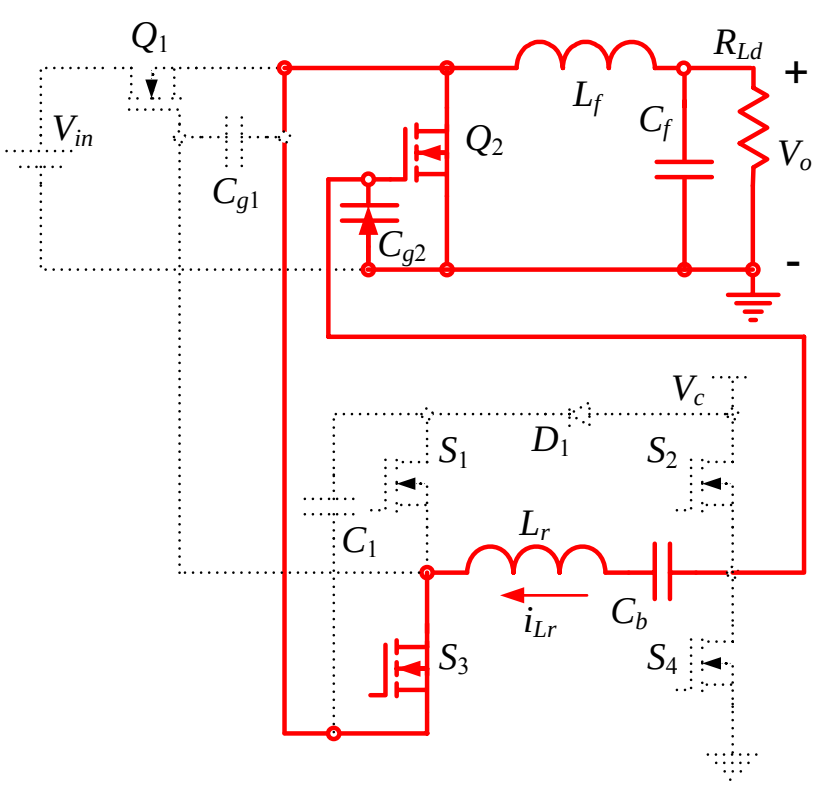
Before t_0

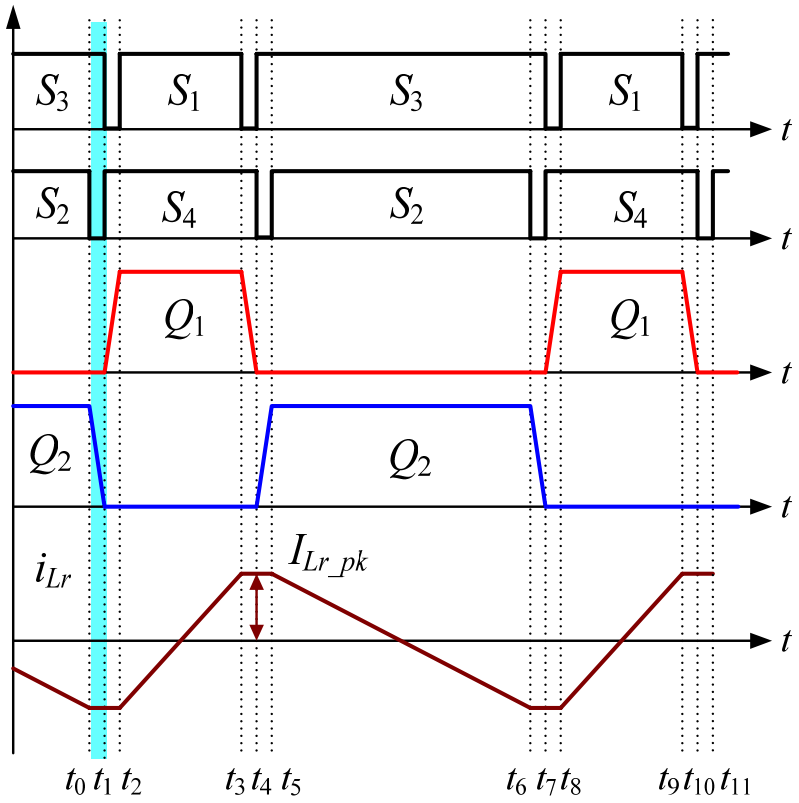




Key waveforms

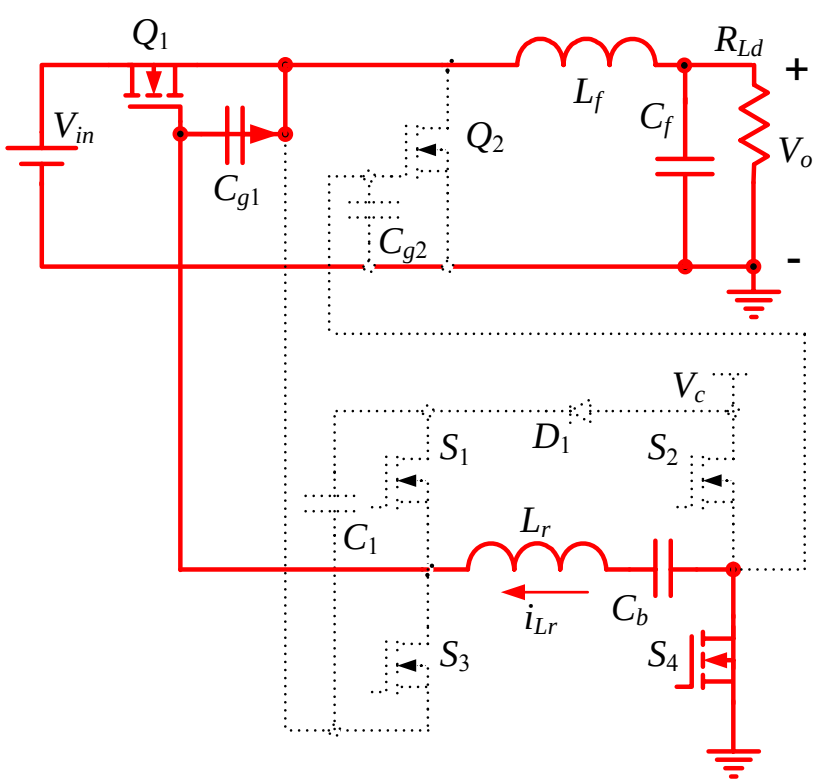
Turn-off Q_2: [t_0, t_1]

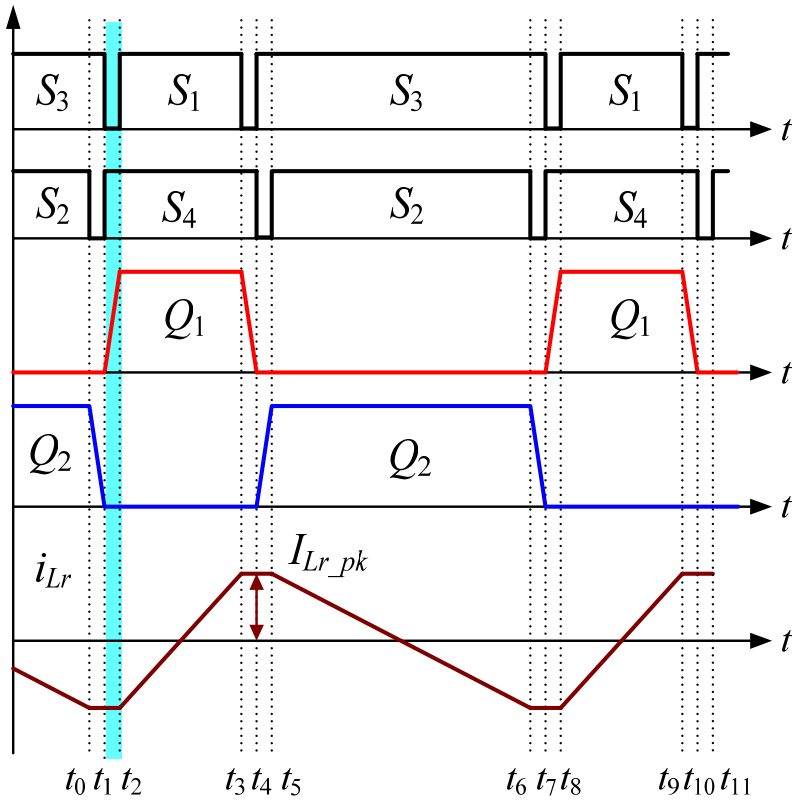




Key waveforms

Turn-on Q_1: [t_1, t_2]





Key waveforms

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Driver Loss Analysis

- The conduction loss of S_1-S_4

$$P_{cond\_s1-s4} = 2I_{s1\_RMS}^{\ 2} \cdot R_{ds(on)} + 2I_{s2\_RMS}^{\ 2} \cdot R_{ds(on)}$$

$R_{ds(on)}$ is the on-resistance of S_1-S_4

- The resonant inductor loss

$$P_{ind} = P_{copper} + P_{core}$$

- The loss of MOSFET mesh resistance R_G

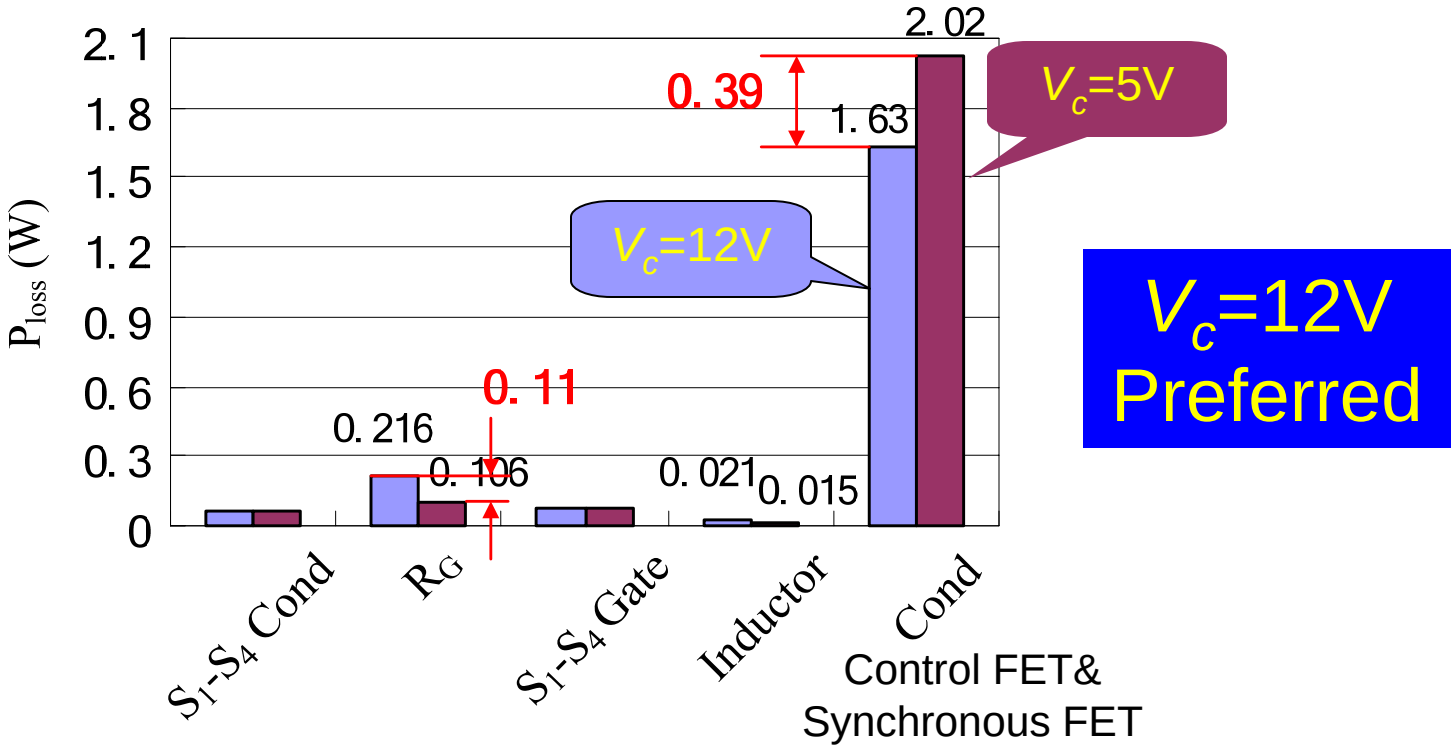
$$P_{RG} = 2R_{G1}I^{2}_{Lr\_pk} \cdot t_{sw1} \cdot f_s + 2R_{G2}I^{2}_{Lr\_pk} \cdot t_{sw2} \cdot f_s$$

t_{sw1} and t_{sw2} are the switching time, I_{Lr_pk} is the peak current of resonant inductor

- The loss of gate charges of switches S1-S4

$$P_{Gate} = 4 \cdot Q_{g\_s} \cdot V_{gs\_s} \cdot f_s$$

V_{cc} Selection of Resonant Gate Driver

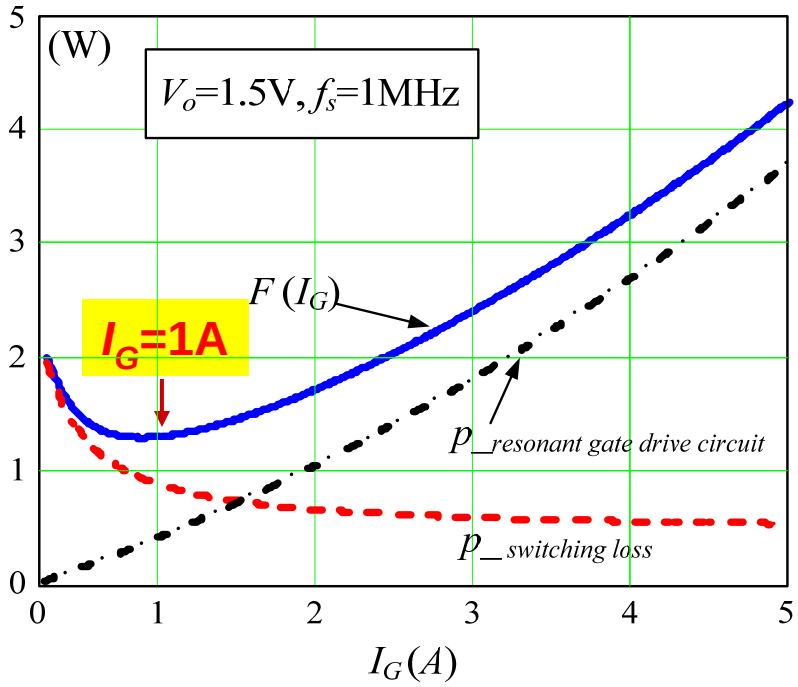


V_{in}=12V; I_o=20A; f_s=1MHz;

Q_1: IRF7821(30V, $R_{DS(on)}$=9mΩ@V_{GS}=6V); Q_2: FNS7088(30V, $R_{DS(on)}$=3.5mΩ@V_{GS}=6V);

S_1-S_4: FDN335N(20V N-channel, $R_{DS(on)}$=0.07Ω@V_{GS}=4.5V); L_r=2.2uH.

Gate Charge Current I_G Selection



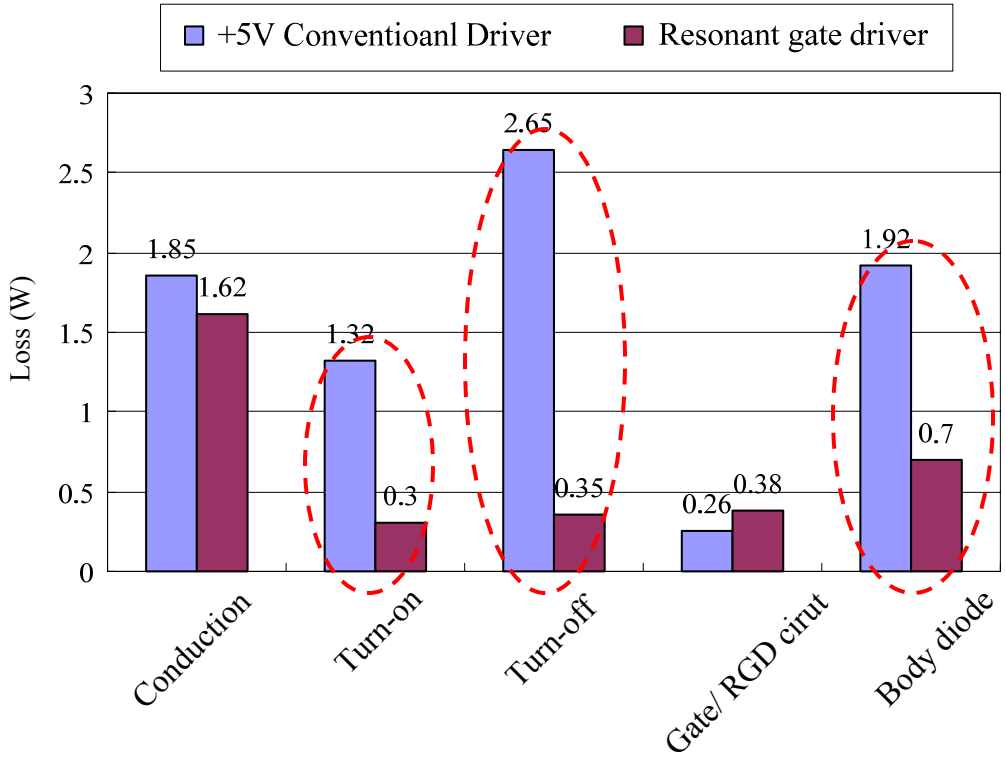
1. Switching loss $P_{switching}(I_G)$ as function of driven current I_G is calculated

2. Total loss $P_{circuit}(I_G)$ of the resonant gate drive circuit as function of driven current I_G is calculated

3. The Objective function is established by adding switching loss and the resonant gate driver loss together

$$F(I_G) = P_{circuit}(I_G) + P_{switching}(I_G)$$

Conventional Driver vs. Resonant Driver



V_{in}=12V; V_o=1.5V; I_o=20A; f_s=1MHz;

Control FET: IRF7821(30V, $R_{DS(on)}$=9mΩ@V_{GS}=6V)

Syn FET: FNS7088 (30V, $R_{DS(on)}$=3.5mΩ@V_{GS}=6V)

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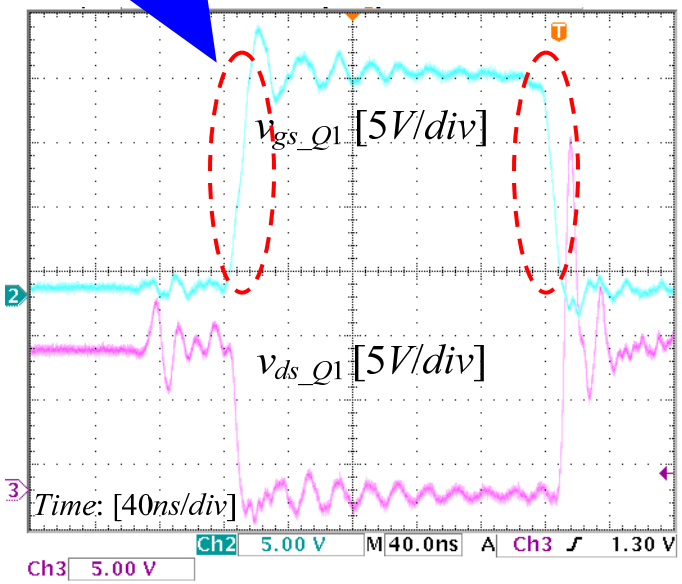
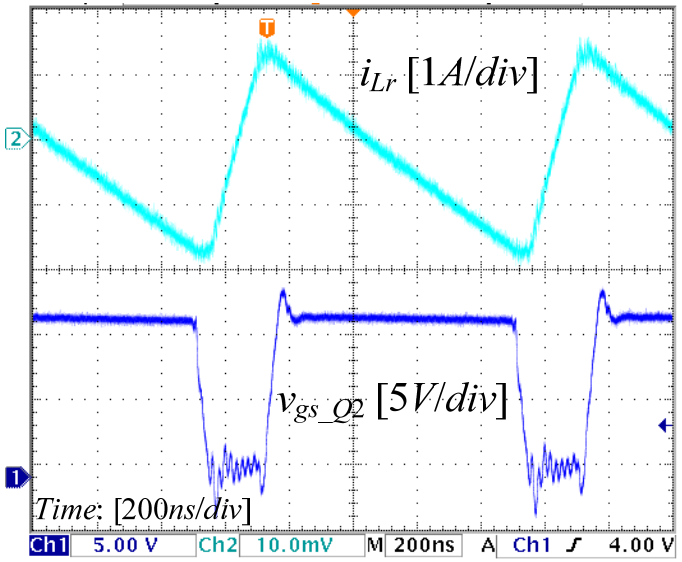
Experimental Results: Fast Switching Speed

Fast speed
No miller plateau



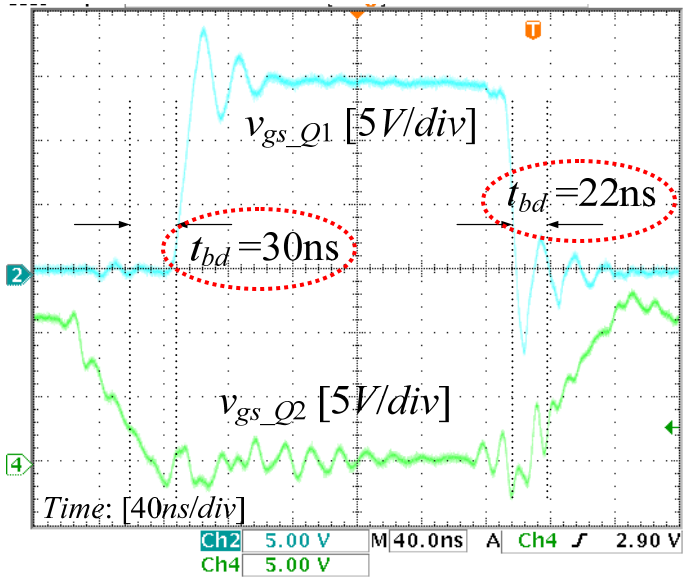
Gate drive signal and drain-source voltage (control FET)



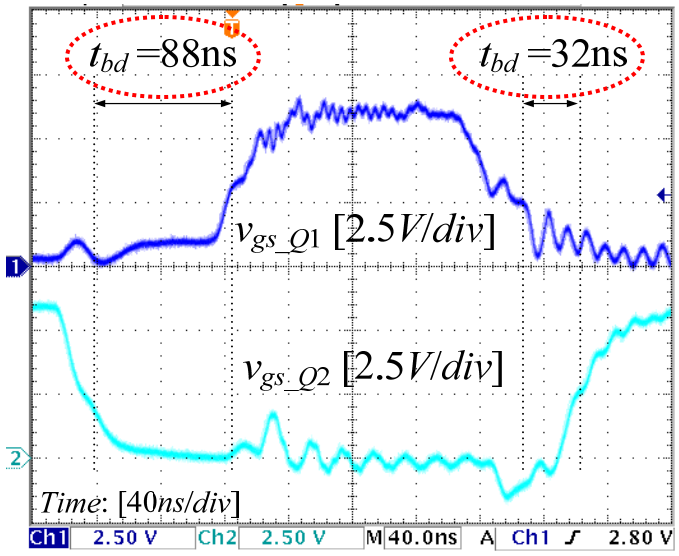
Resonant inductor current and drain-source voltage (Synchronous FET)

V_{in}=12V; I_o=20A; f_s=1MHz; Control FET: IRF7821;Syn FET: FNS7088

Experimental Results: Reduced Dead Time



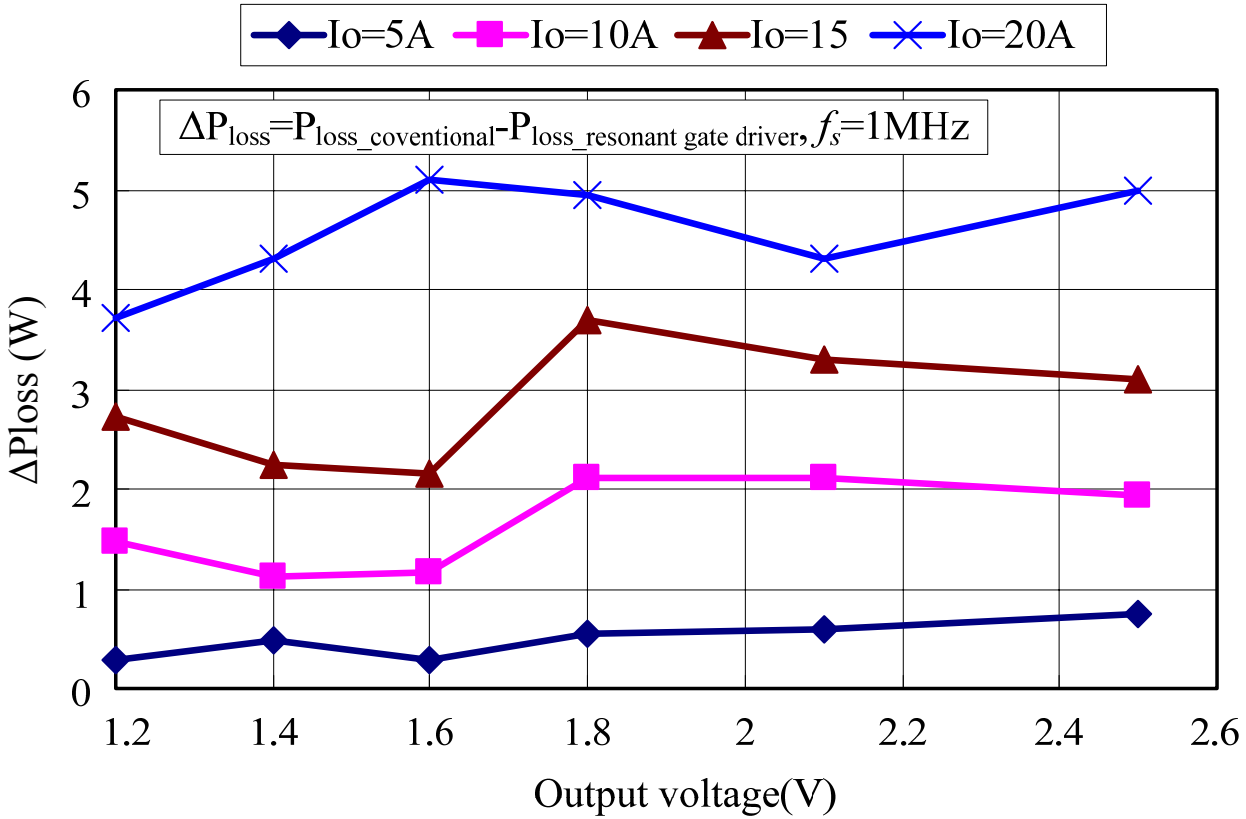
Resonant gate driver



Conventional gate driver (TPS2832 TI)

V_{in}=12V; V_o=1.5V; I_o=20A; f_s=1MHz; Control FET: IRF7821;Syn FET: FNS7088

Experimental Results: Loss Savings



4.5W Loss Reduction
@Vo=1.5V/20A(15% of the output power)

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Conclusion

- A New Resonant Driver Proposed
  - ✓ Switching Loss Reduction
  - ✓ Immunity to Common Source Inductance
  - ✓ Gate Energy Recovery
  - ✓ ZVS for Driver Switches
  - ✓ High *Cdv/dt I*mmunity (Low Impedance)
  - ✓ Reduced Body Diode Conduction Time
- Loss Analysis and Design Procedure Presented
- 4.5W Loss Reduction @Vo=1.5V/20A/1MHz(15% of output power)

Thank You For Your Time

Other Resonant Gate Drive Material at:

www.QueensPowerGroup.com