

Queen's Power Group

Kingston, Ontario, Canada

www.queenspowergroup.com



A New Resonant Gate Drive Circuit with Efficient Energy Recovery and Low Conduction Loss

Presented By: Wilson Eberle

Authors: Wilson Eberle

P.C. Sen

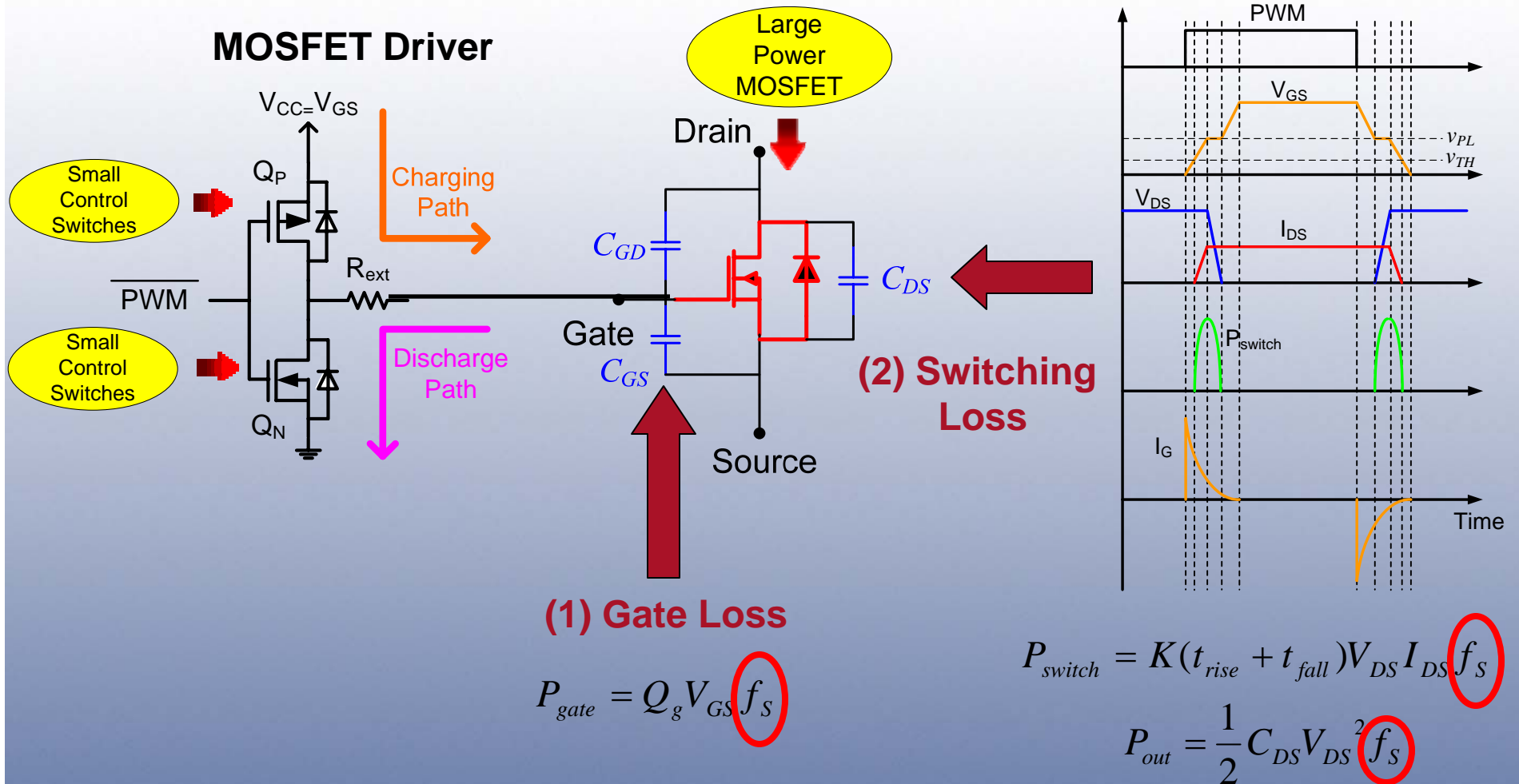
Yan-Fei Liu

Presentation Overview



- 1. Introduction***
- 2. Proposed Circuit and Waveforms**
- 3. Logic Implementation**
- 4. Loss Analysis**
- 5. Design Procedure**
- 6. Design Example**
- 7. Simulation Results**
- 8. Conclusions**

Conventional Lossy RC-Type Voltage Drive

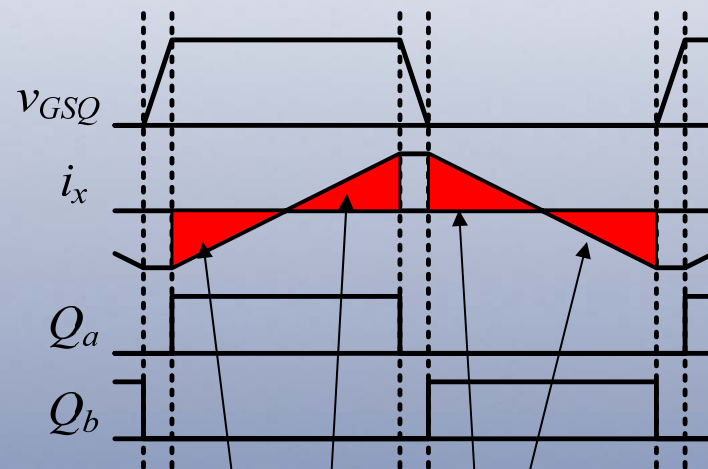
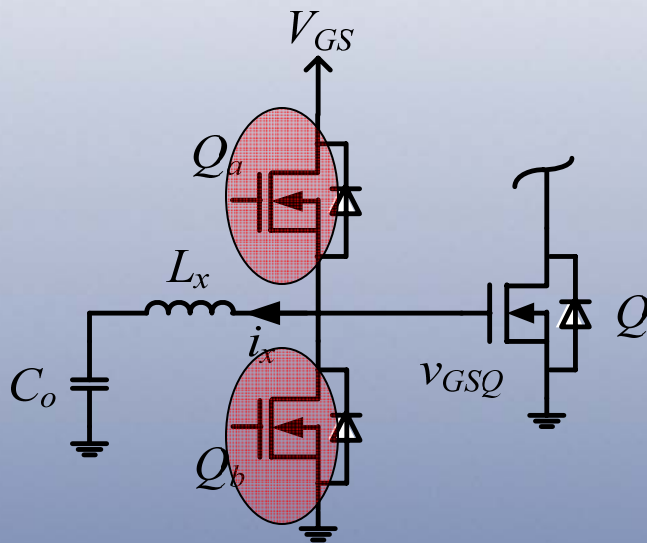


Resonant Gate Drive Review



Existing techniques suffer from at least one of three problems:

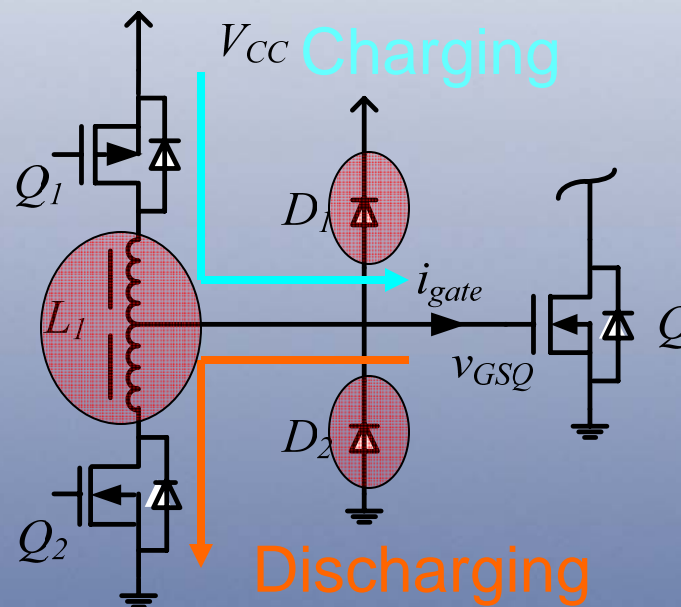
1. Circulating current conduction loss [1]



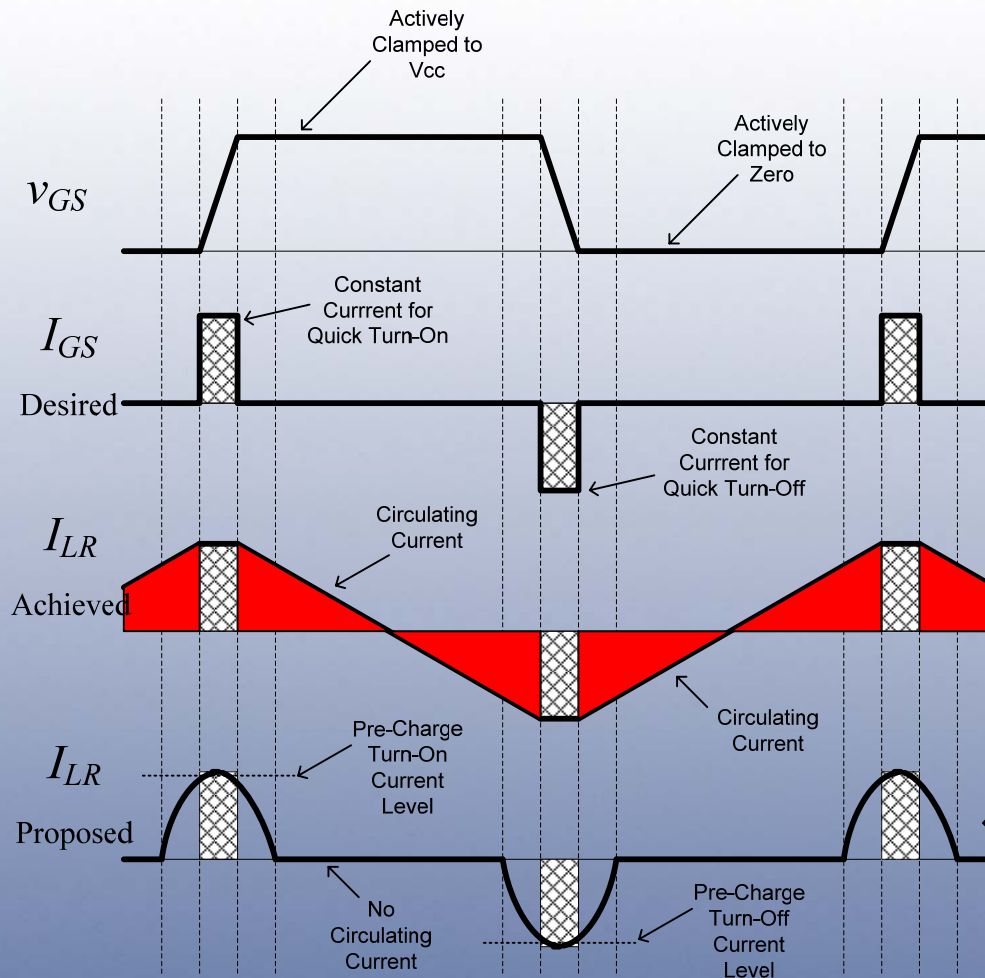
**Circulating
Current
Loss**

Resonant Gate Drive Review

2. Slow turn-on and/or turn-off through inductance [2]-[9]
3. Gate not actively clamped high and/or low, so false triggering (Cdv/dt) can result [2]-[7],[9]



Evolution of the Proposed Driver



Current Source
Drive For Speed

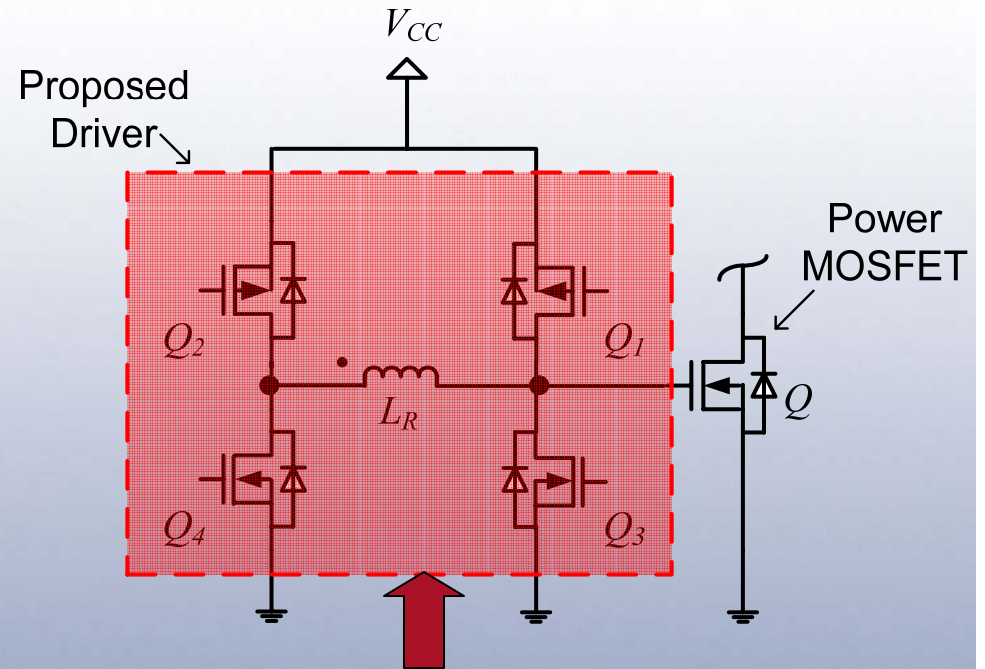
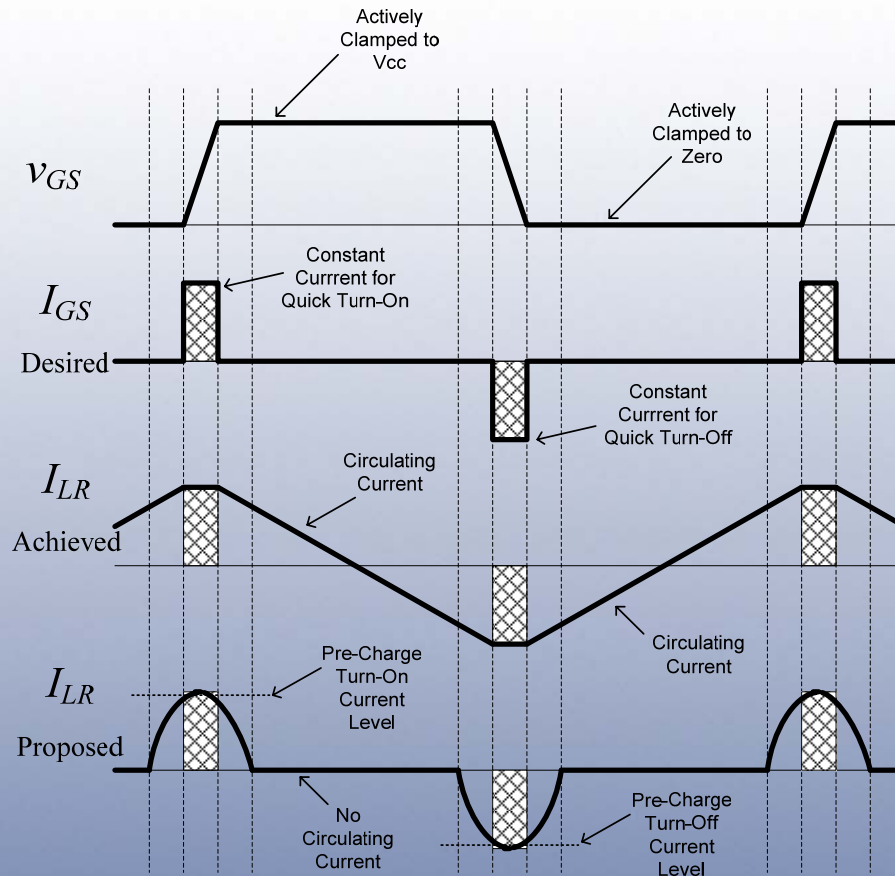
Discontinuous
Inductor Current
With Pre-Charge
Minimizes Conduction
Loss

Presentation Overview



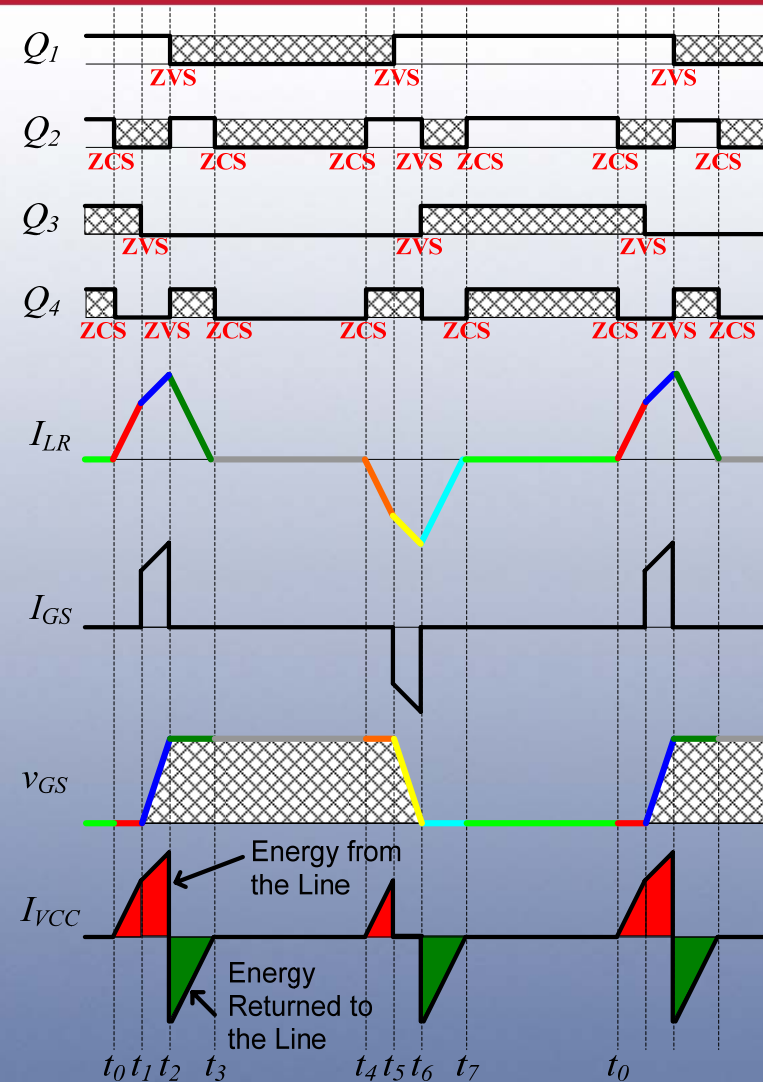
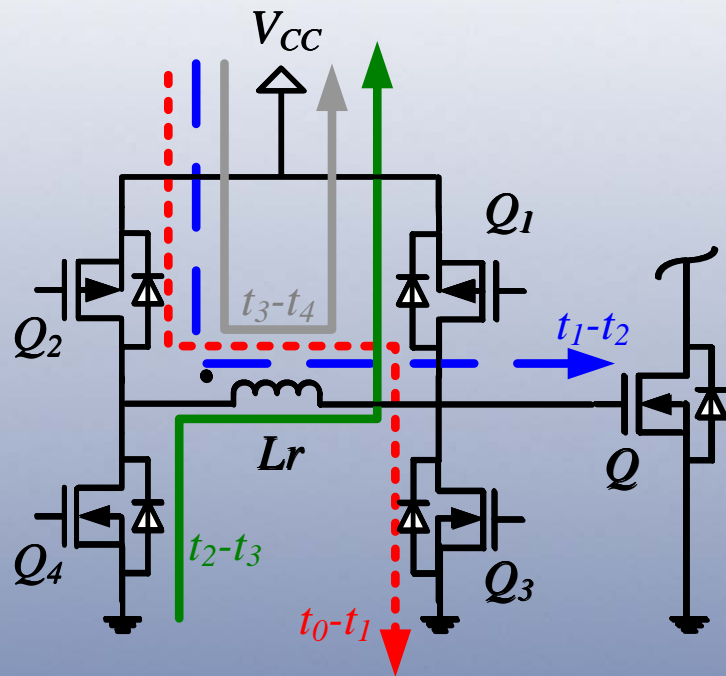
1. Introduction
2. *Proposed Circuit and Waveforms*
3. Logic Implementation
4. Loss Analysis
5. Design Procedure
6. Design Example
7. Simulation Results
8. Conclusions

Evolution of the Proposed Driver

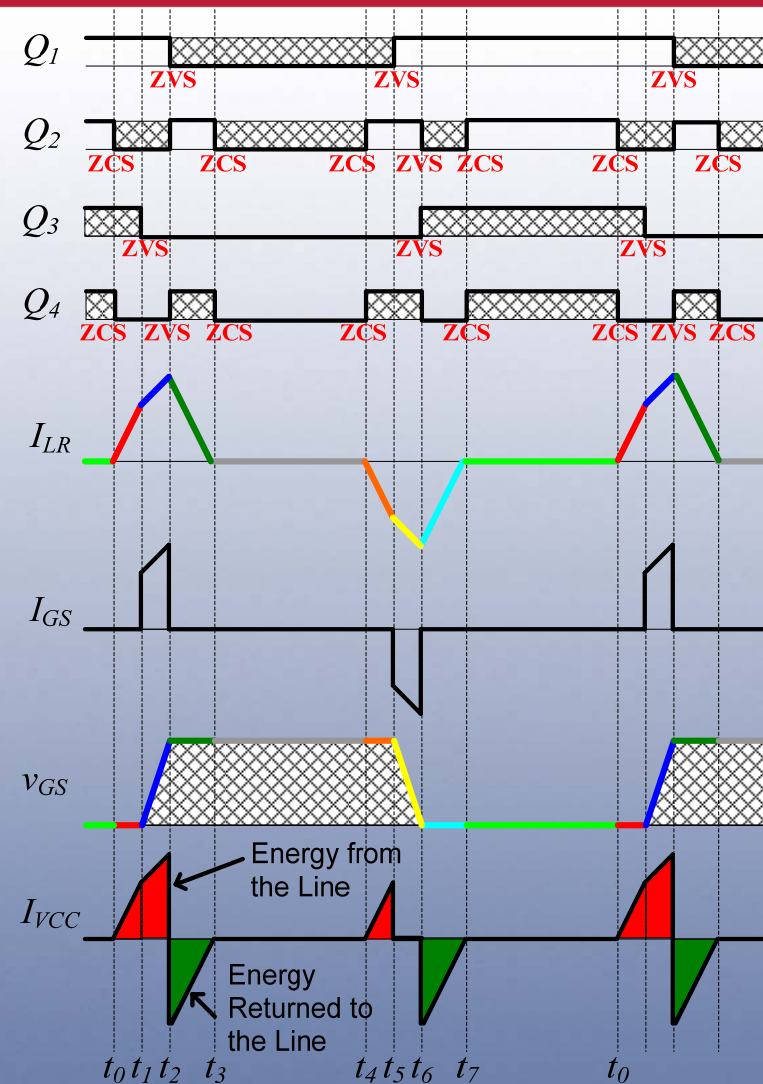
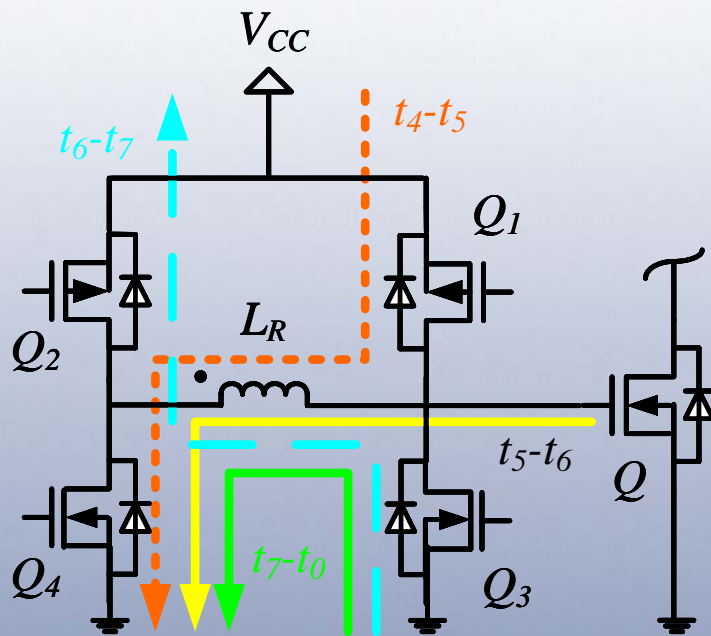


Discontinuous
Current By Controlling
4 Control Switches
 Q_1 - Q_4

Switch Control of Proposed Driver: Turn-On Sequence



Switch Control of Proposed Driver: Turn-Off Sequence

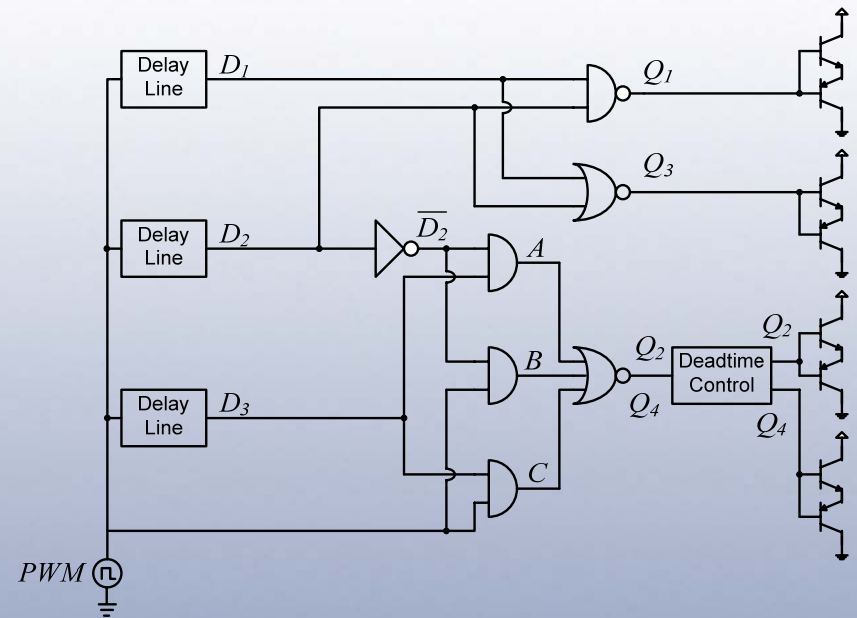
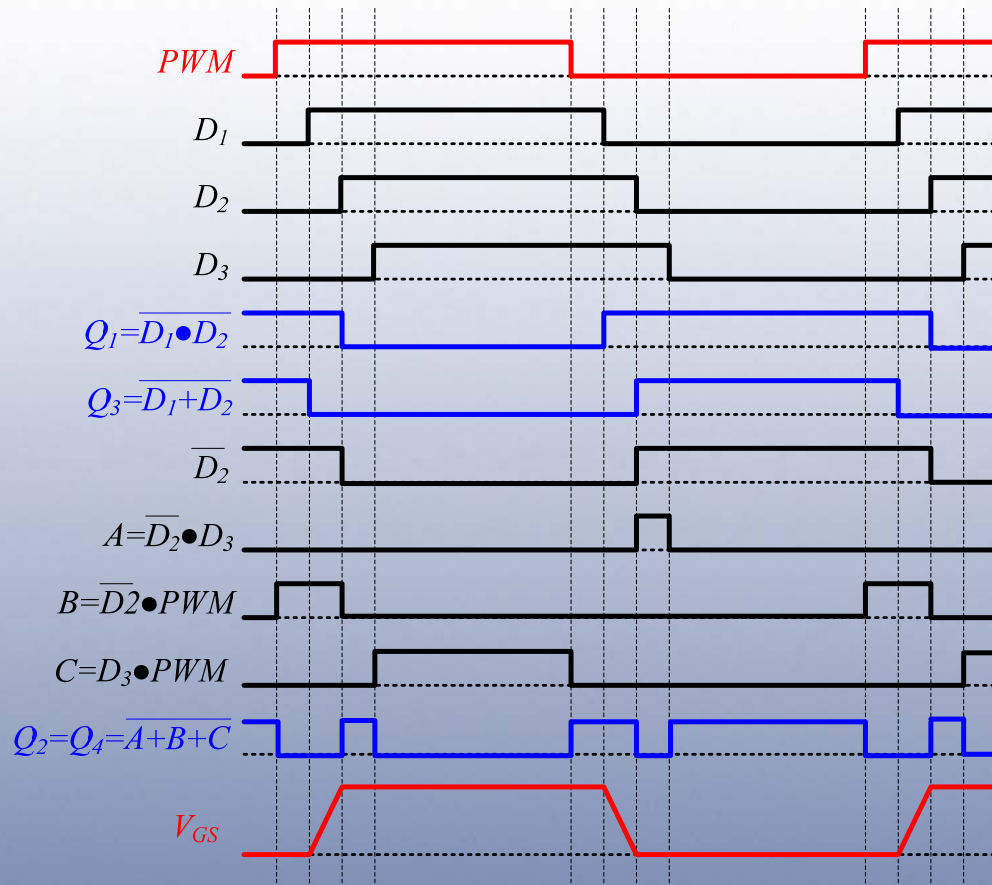


Presentation Overview



1. Introduction
2. Proposed Circuit and Waveforms
3. *Logic Implementation*
4. Loss Analysis
5. Design Procedure
6. Design Example
7. Simulation Results
8. Conclusions

Logic Implementation



7 logic components
3 delay elements

Presentation Overview



1. Introduction
 2. Proposed Circuit and Waveforms
 3. Logic Implementation
 4. *Loss Analysis*
 5. *Design Procedure*
 6. *Design Example*
 7. Simulation Results
 8. Conclusions
- More In
The Paper***
-
- Three arrows originate from the right side of the text "More In The Paper" and point to items 4, 5, and 6 of the list, which are "Loss Analysis", "Design Procedure", and "Design Example" respectively.

Losses



1. Conduction loss in switches, inductor & R_g ; **MOSFET R_g biggest contributor**
2. Q2/Q4 gate loss at 3 times switching frequency
3. Some CV^2 loss at 2 times switching frequency in Q2/Q4
4. Turn-off loss in Q2/Q4 at switching frequency
5. Inductor core loss

- 1. Calculate optimized inductance:
170nH**
- 2. Calculate optimized delay
times: $t_1=24\text{ns}$, $t_2=90\text{ns}$,
 $t_3=149\text{ns}$**

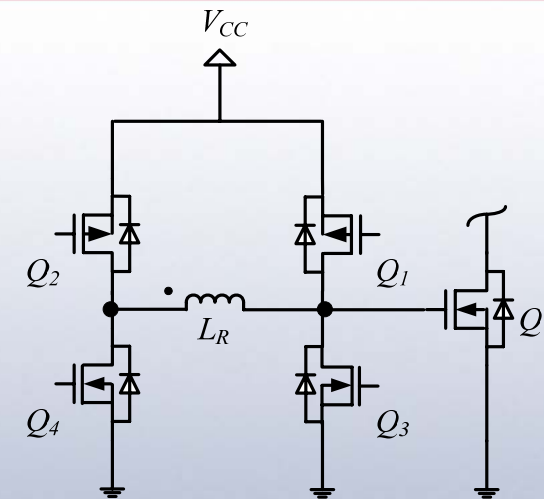
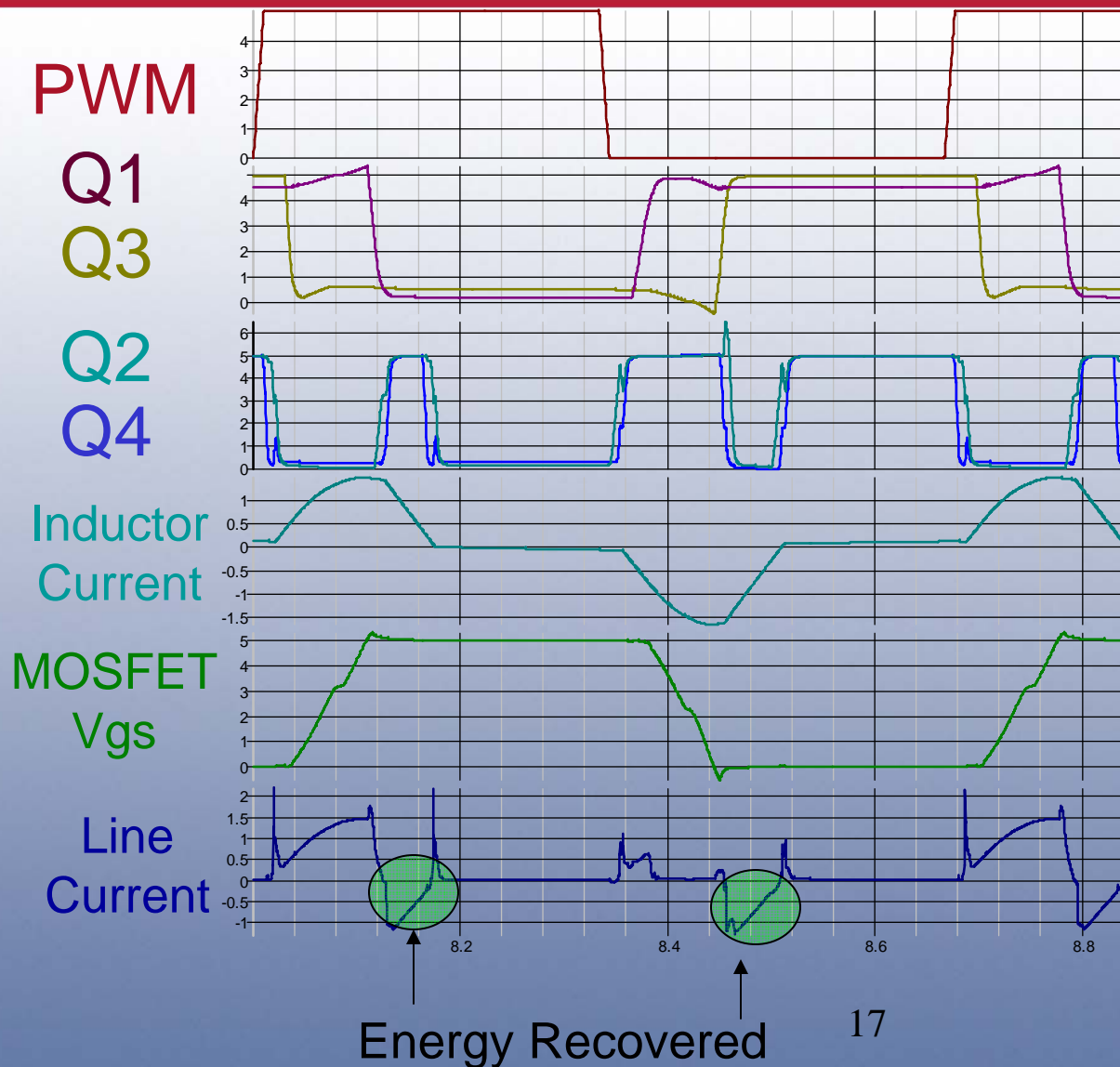
Presentation Overview



1. Introduction
2. Proposed Circuit and Waveforms
3. Logic Implementation
4. Loss Analysis
5. Design Procedure
6. Design Example
- 7. *Simulation Results***
8. Conclusions

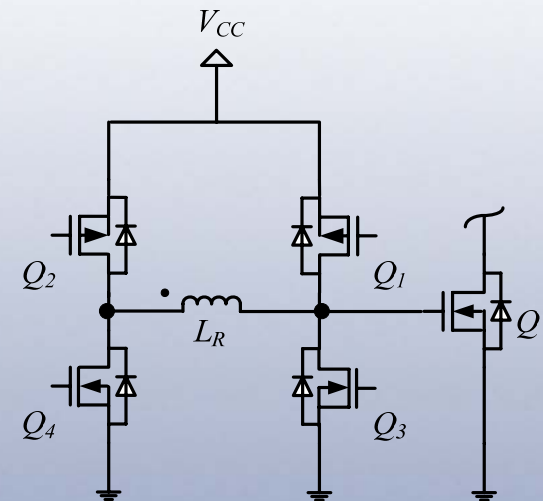
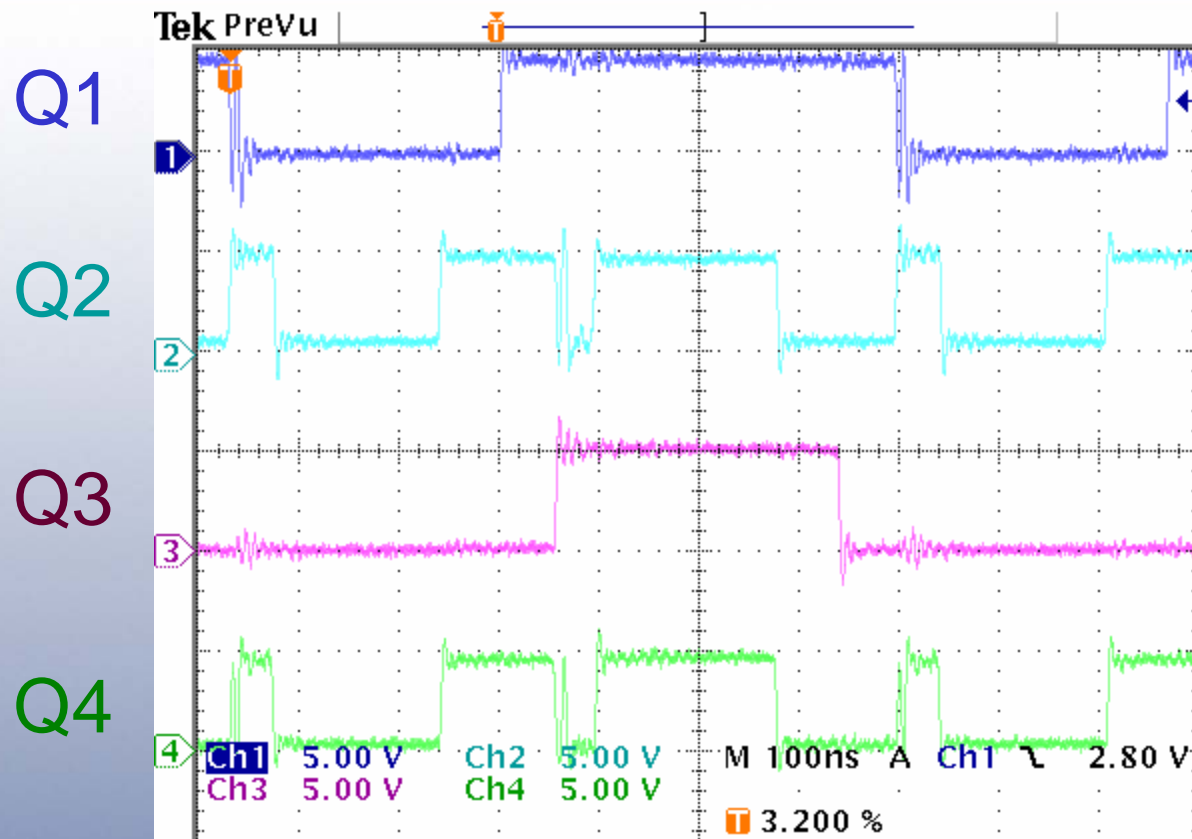
SIMetrix Simulation Results

1.5MHz, $L_R=170\text{nH}$, 2-IRF6691 MOSFETs



- Conventional driver gate loss: **1.2W+**
- Proposed driver loss: **496mW**
- **59% recovery**

Experimental Results



Preliminary Results: more at APEC 06

Presentation Overview



1. Introduction
2. Proposed Circuit and Waveforms
3. Logic Implementation
4. Loss Analysis
5. Design Procedure
6. Design Example
7. Simulation Results
8. *Conclusions*

Conclusions



- **New resonant gate driver proposed**
- **Solves problems of existing drivers:**
 1. **High conduction loss**
 - **SOLUTION:** discontinuous inductor current
 2. **Slow turn-on/turn-off**
 - **SOLUTION:** pre-charge current before switching
 3. **Poor Cdv/dt immunity (false triggering)**
 - **SOLUTION:** actively clamping power MOSFET gate through low impedance control switches
- **Partial gate energy recovery**
- **Reduction in switching loss by fast switching**
– SIGNIFICANT!

Thank You For Your Time

**Stay Tuned for More on this Driver
and others from The Queen's
Power Group at APEC 06 in Dallas**

Questions?