Queen's Power Group
Kingston, ON, Canada

A High Efficiency Synchronous Buck VRM with Current Source Gate Driver

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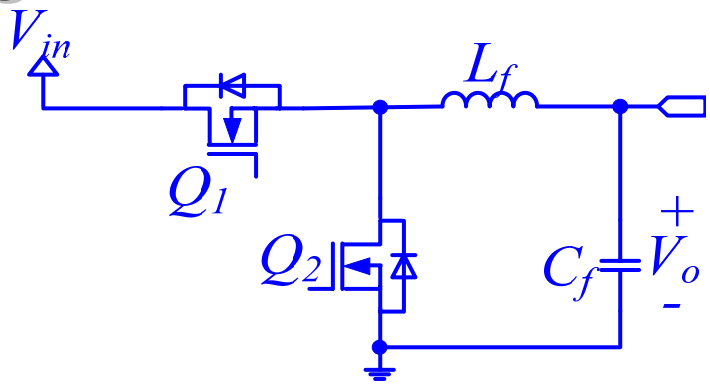
Outline

1. Introduction
    1. Why you should use current source gate drive
    2. Drawbacks of existing voltage source and resonant based drivers
2. Proposed Driver and Operation
3. Driver Design Procedure
4. Driver Optimization in the VRM
5. Logic and Level Shift Circuits
6. Experimental Results
7. Conclusions

Introduction

- **Application:** low voltage high current voltage regulator modules

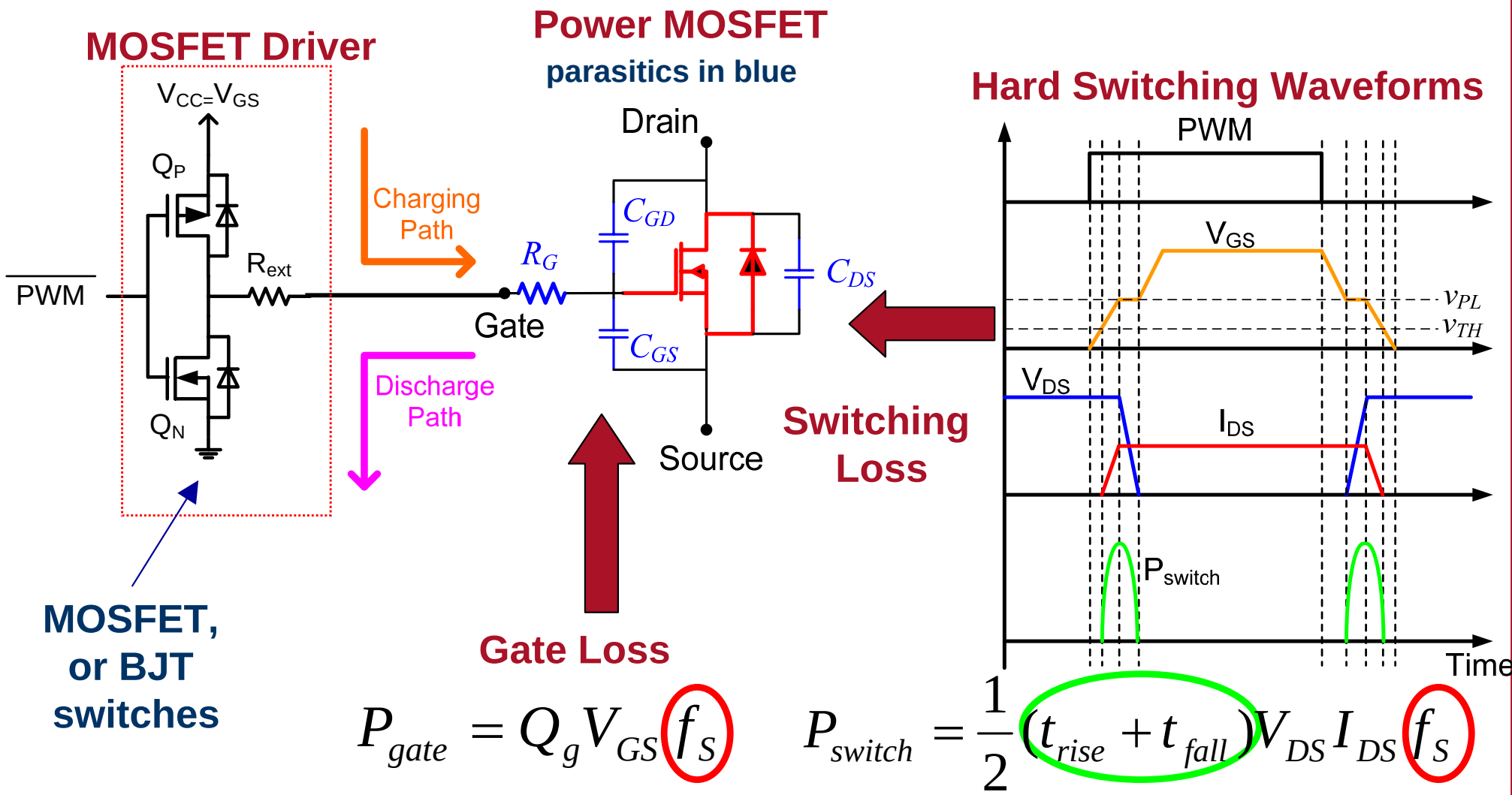


Topology of Choice

Synchronous Buck

- **Trend to increase switching frequency for improvements in:**
  - + **power density**
  - + **dynamic performance**

Drawbacks of Increased Switching Frequency with Conventional Drivers



$$P_{gate} = Q_g V_{GS} f_S \qquad P_{switch} = \frac{1}{2}(t_{rise} + t_{fall}) V_{DS} I_{DS} f_S$$

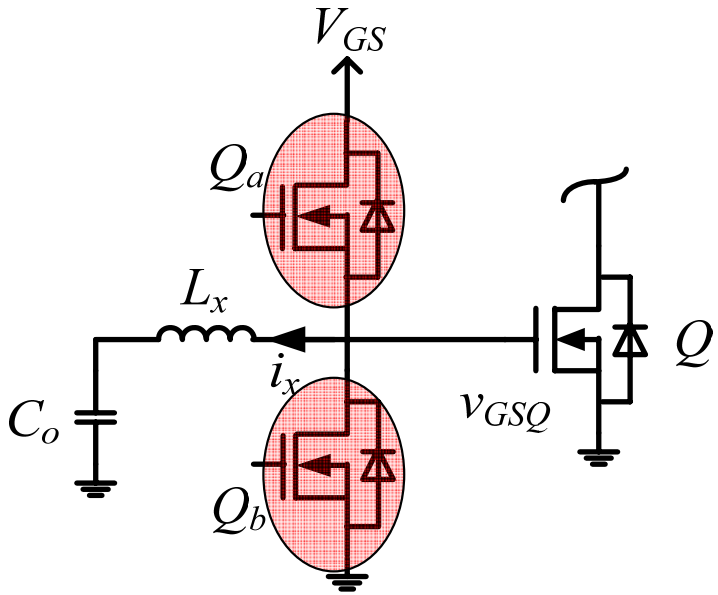
Resonant Gate Drive Techniques

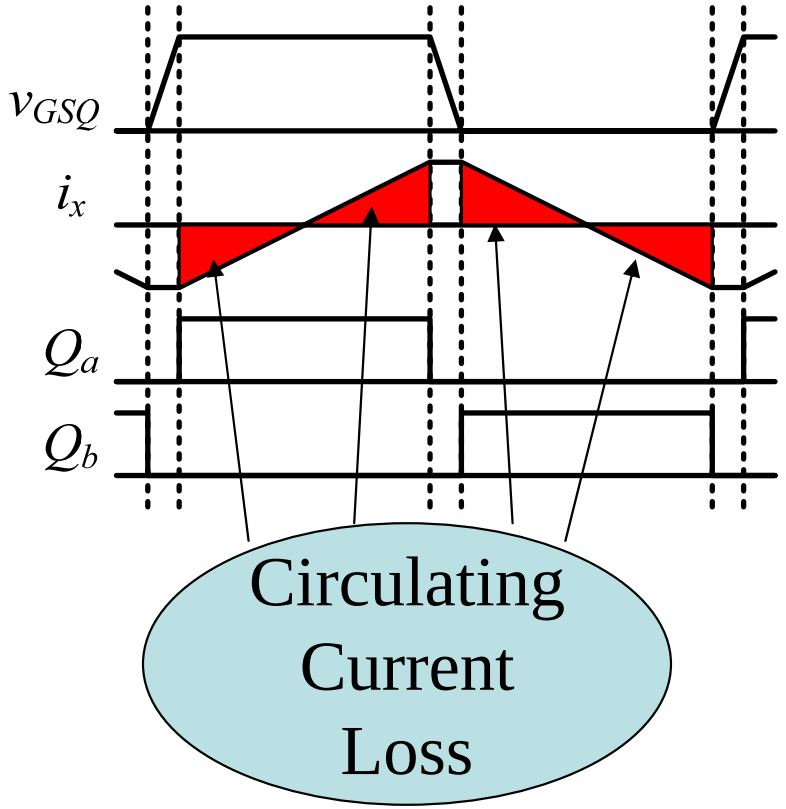
+ Many good (~10) circuits proposed since early 1990s, but generally unused
- LC resonant charging of the power MOSFET gate from zero initial current
- These circuits emphasize gate energy savings, but ignore, or can't achieve potential switching loss savings

Resonant Gate Drive Review

Existing techniques suffer from at least one of five problems:

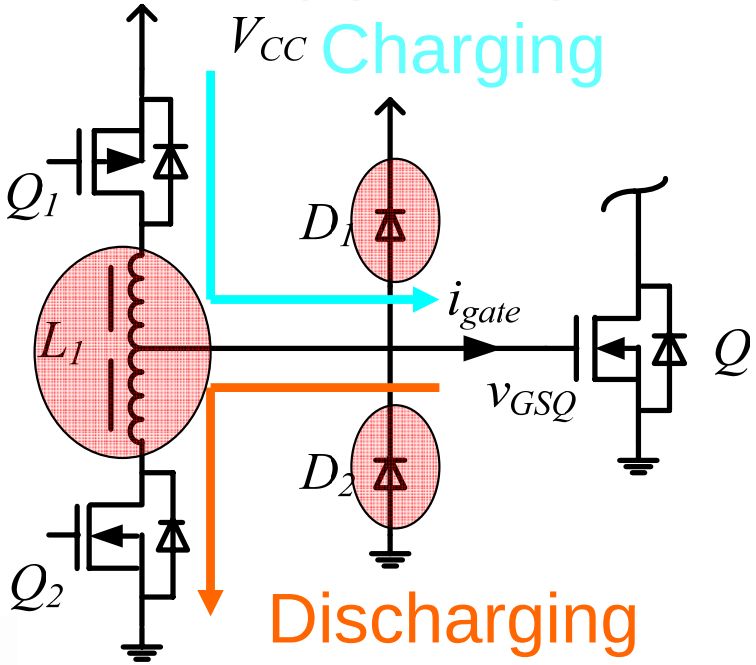
1. **Circulating current conduction loss**
2. **Peak current dependent on duty cycle**

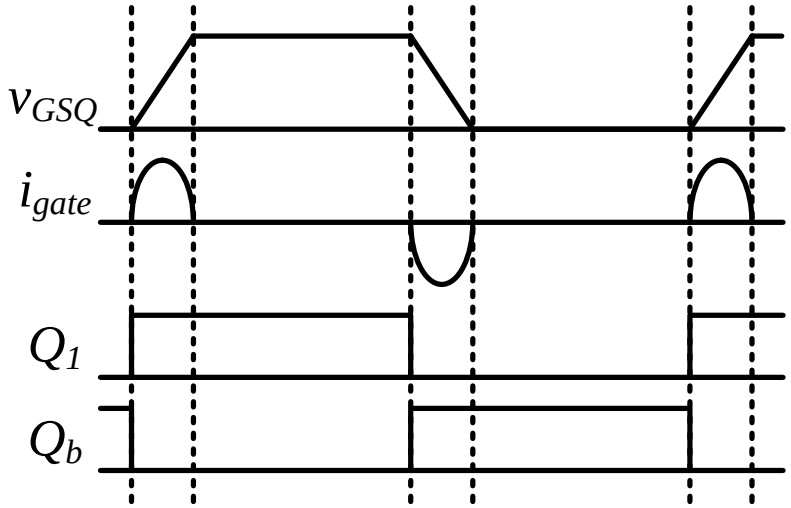




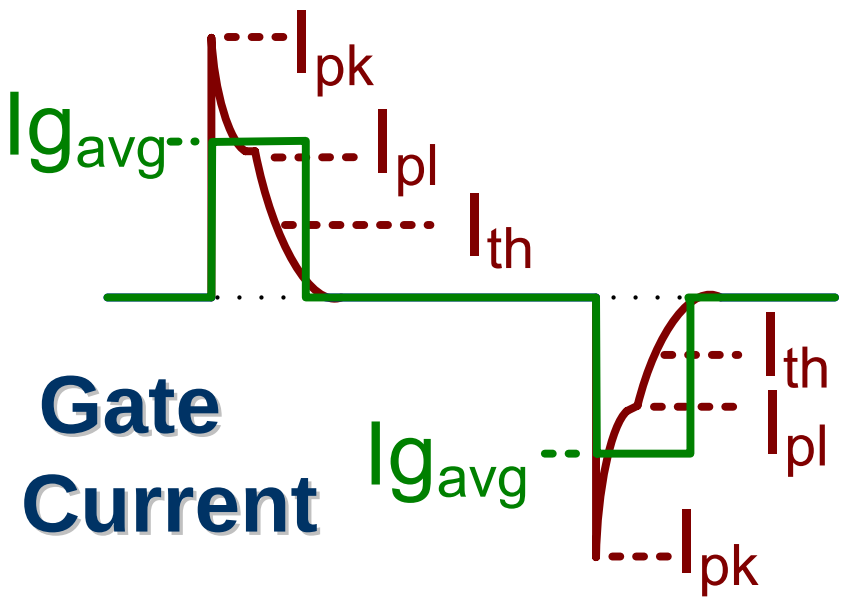
Resonant Gate Drive Review

3. Large inductance, bulky transformer, or coupled inductor
4. Slow turn-on and/or turn-off
5. Gate not actively clamped high and/or low, so false triggering (Cdv/dt) can result





Conventional vs. Resonant Drive Switching Loss Savings



Voltage source RC-type charging limits speed

Constant current source type charging improves speed!

CURRENT SOURCE DRIVERS CAN REDUCE TURN-ON AND TURN-OFF LOSS!

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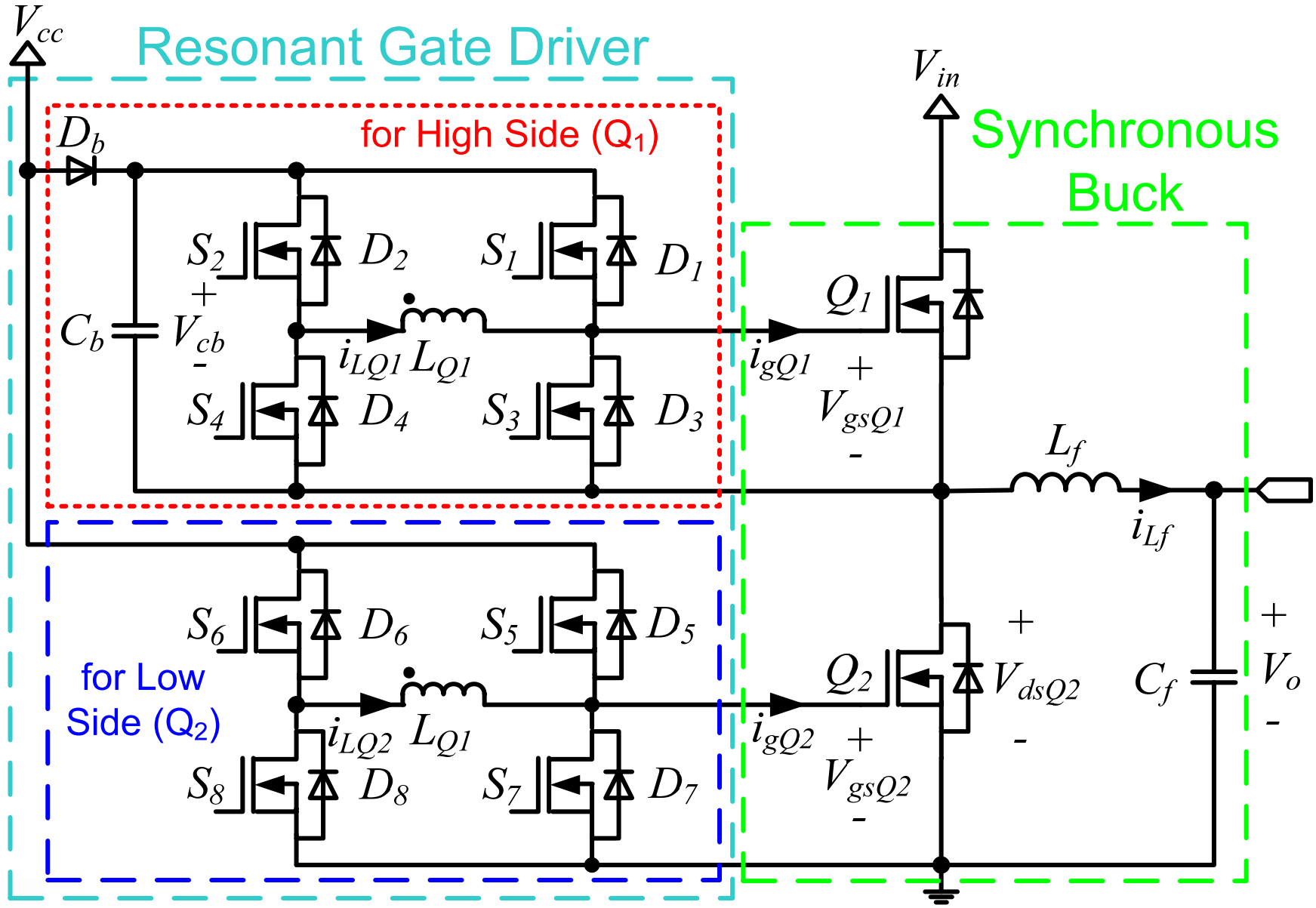
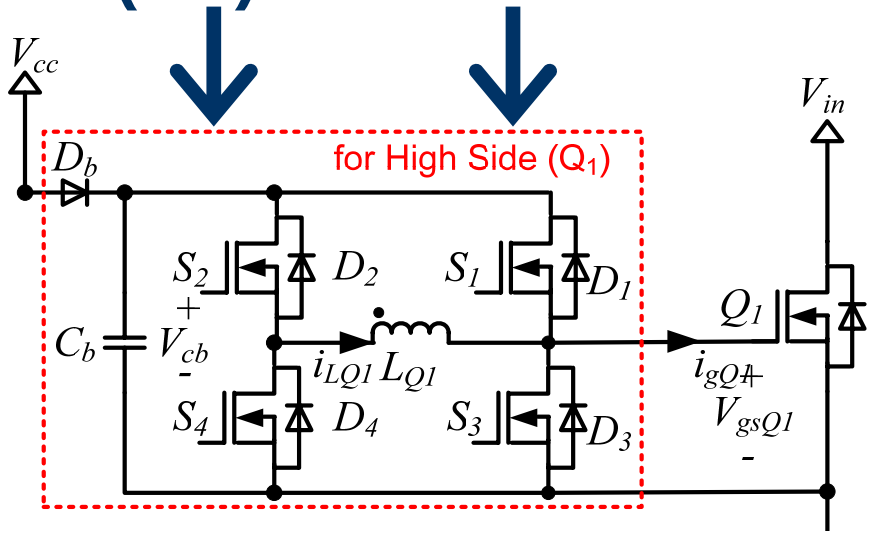
Proposed Driver



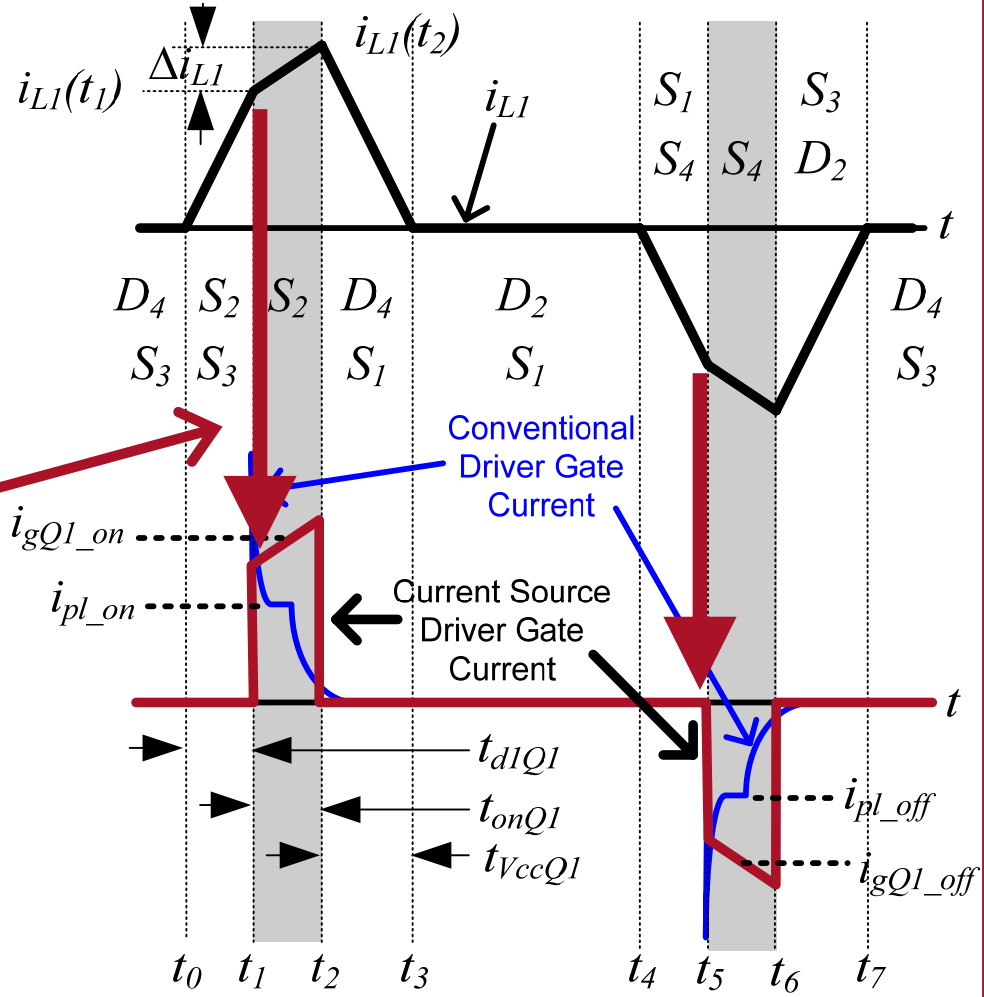
Creating a Discontinuous Current Source

Independent control of high side (HS) MOSFET and SR

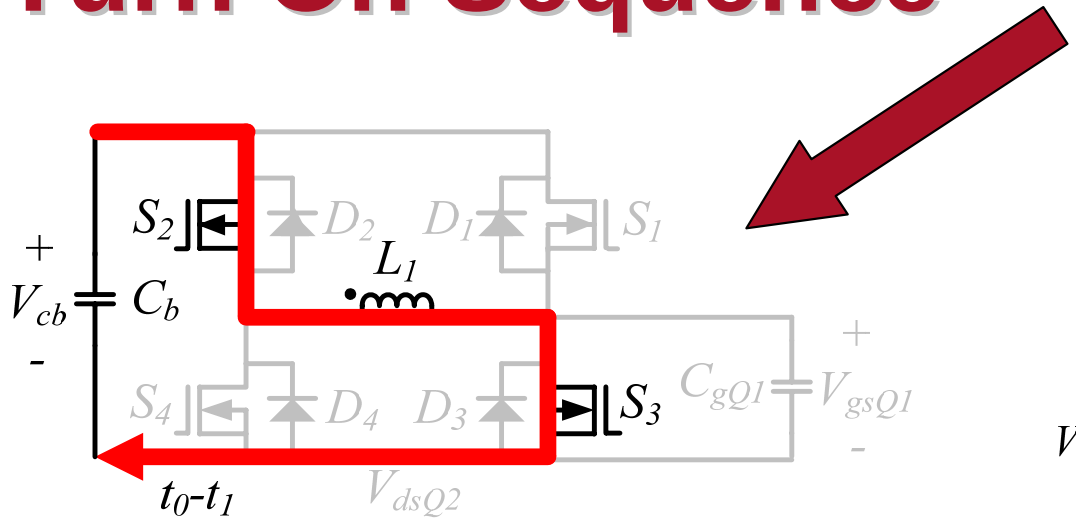


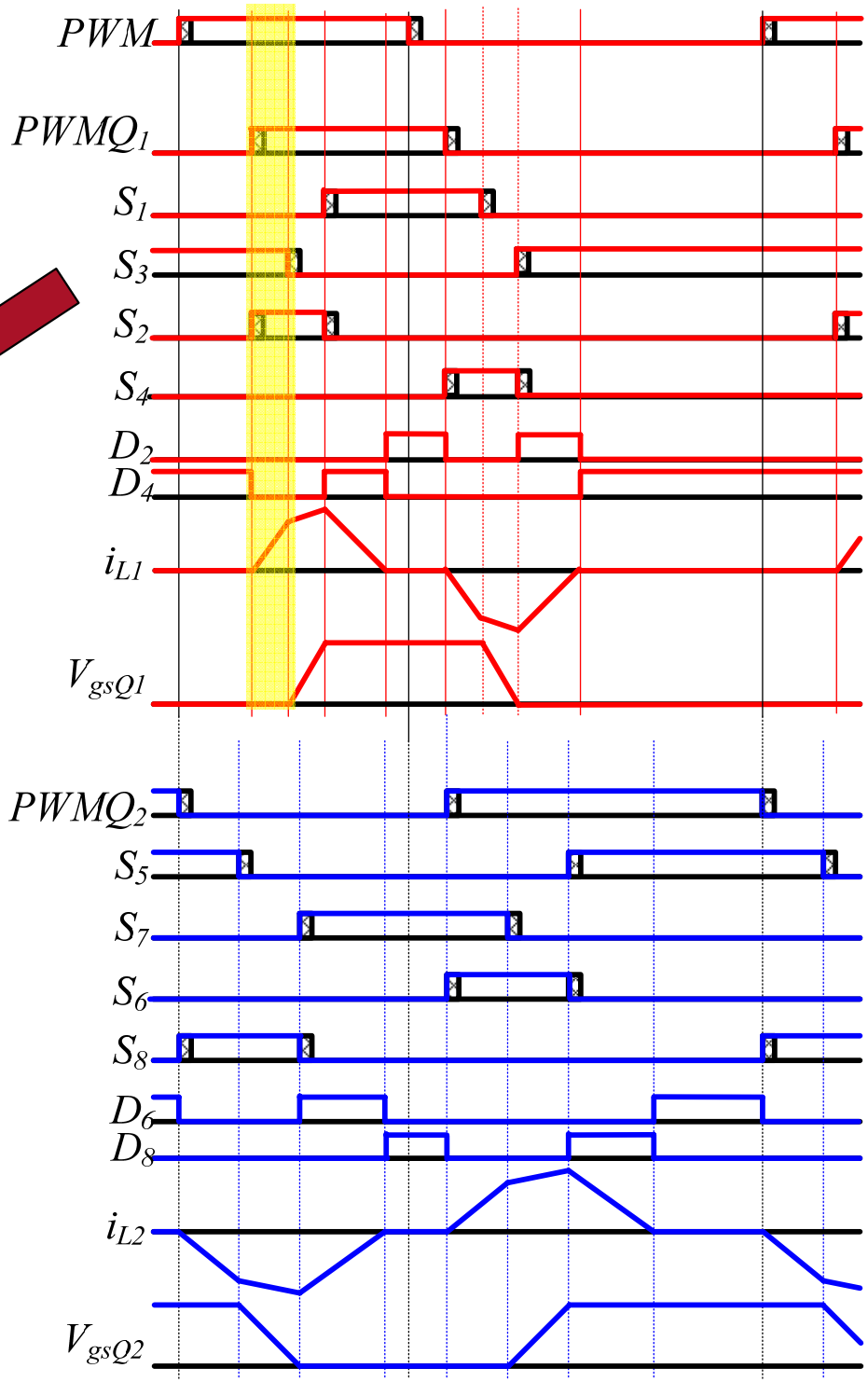
Key To Speed:

- Create discontinuous inductor current source, then
- Divert inductor pre-charge current to the gate



High Side MOSFET Turn On Sequence





- Dictated by $PWMQ_1$ signal
- Independent control of HS MOSFET and SR

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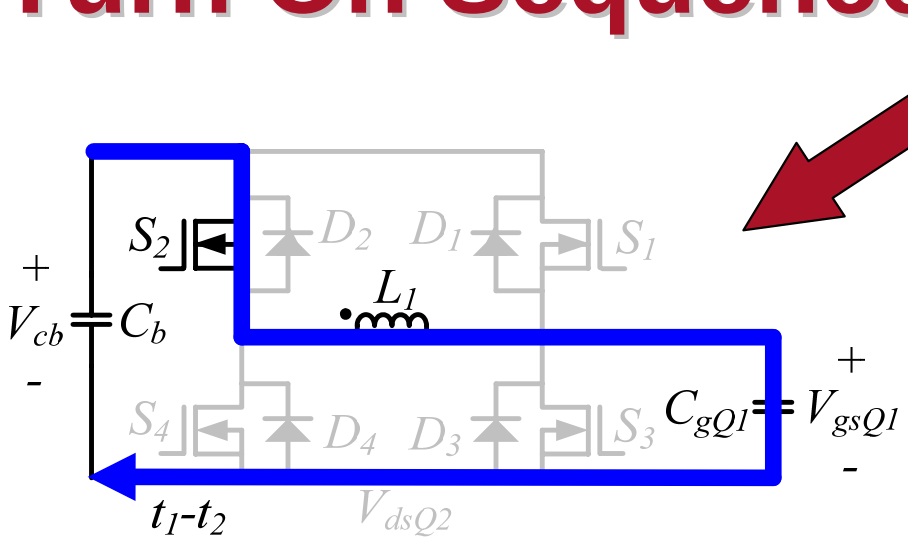

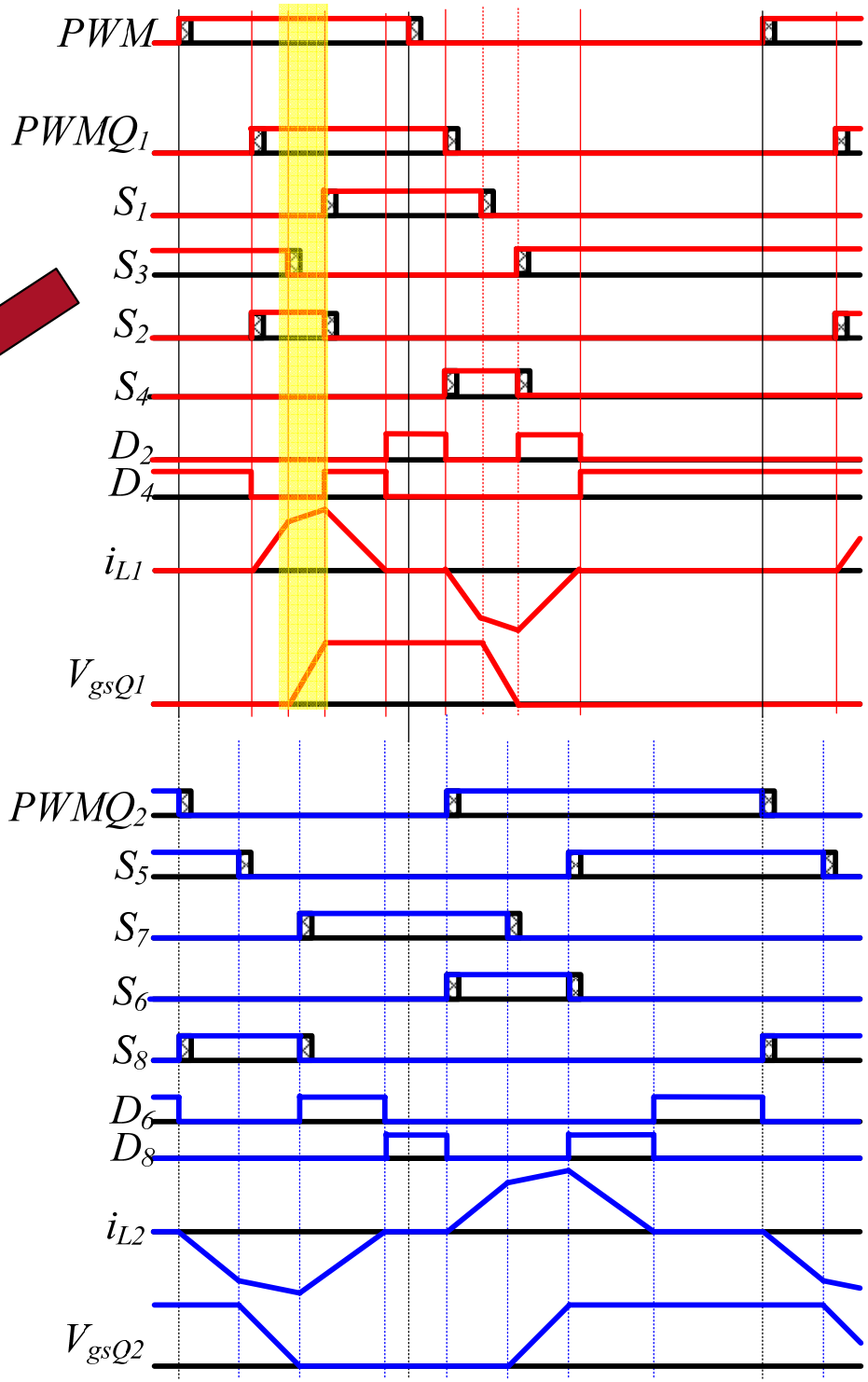

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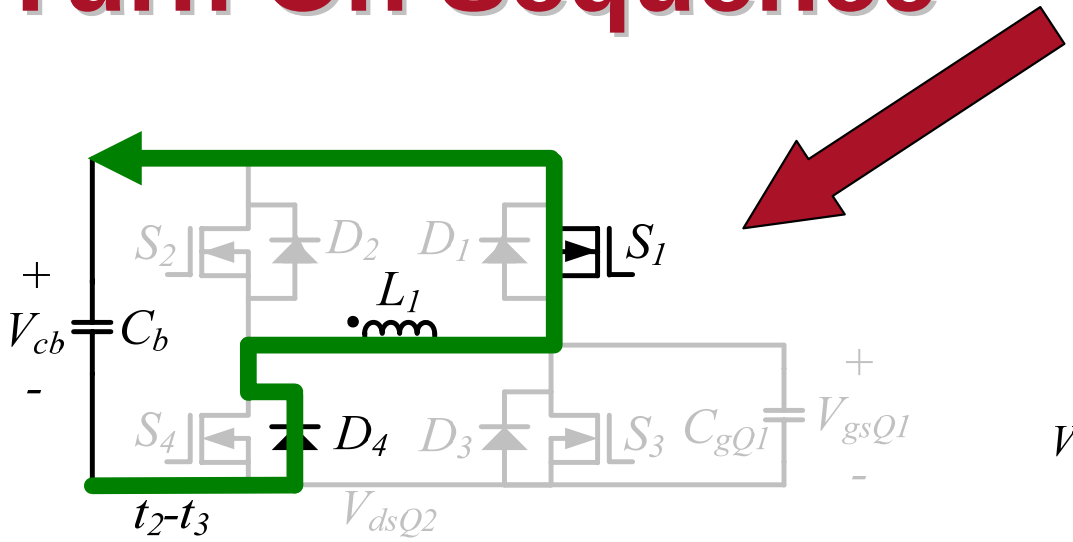

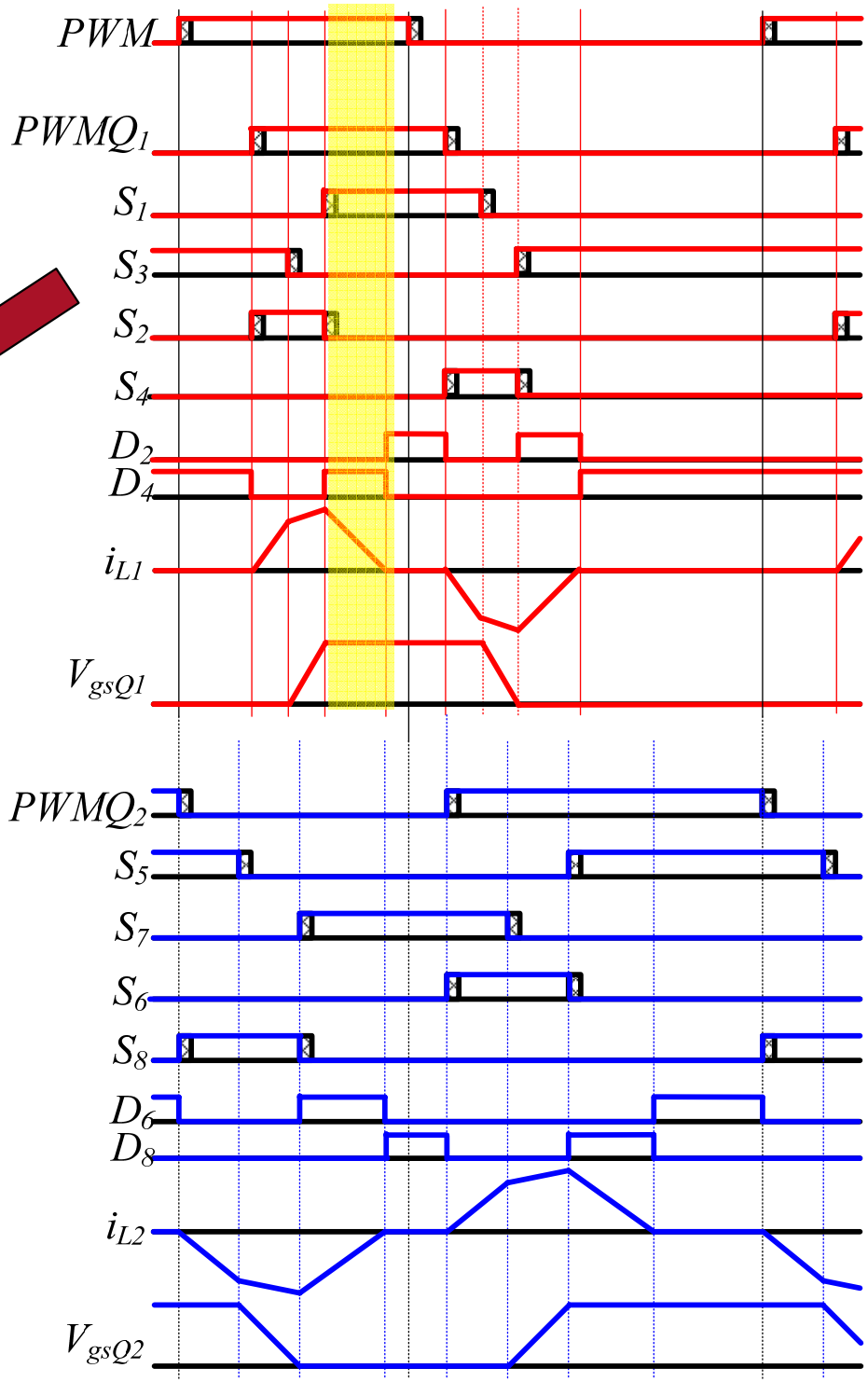

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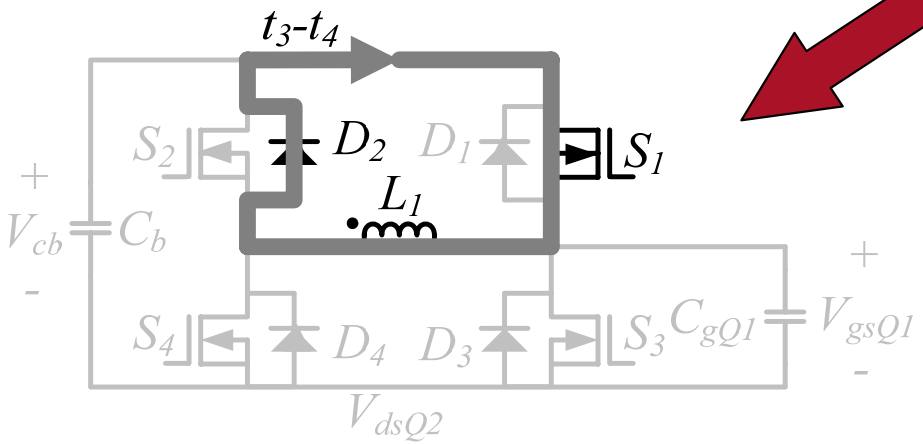
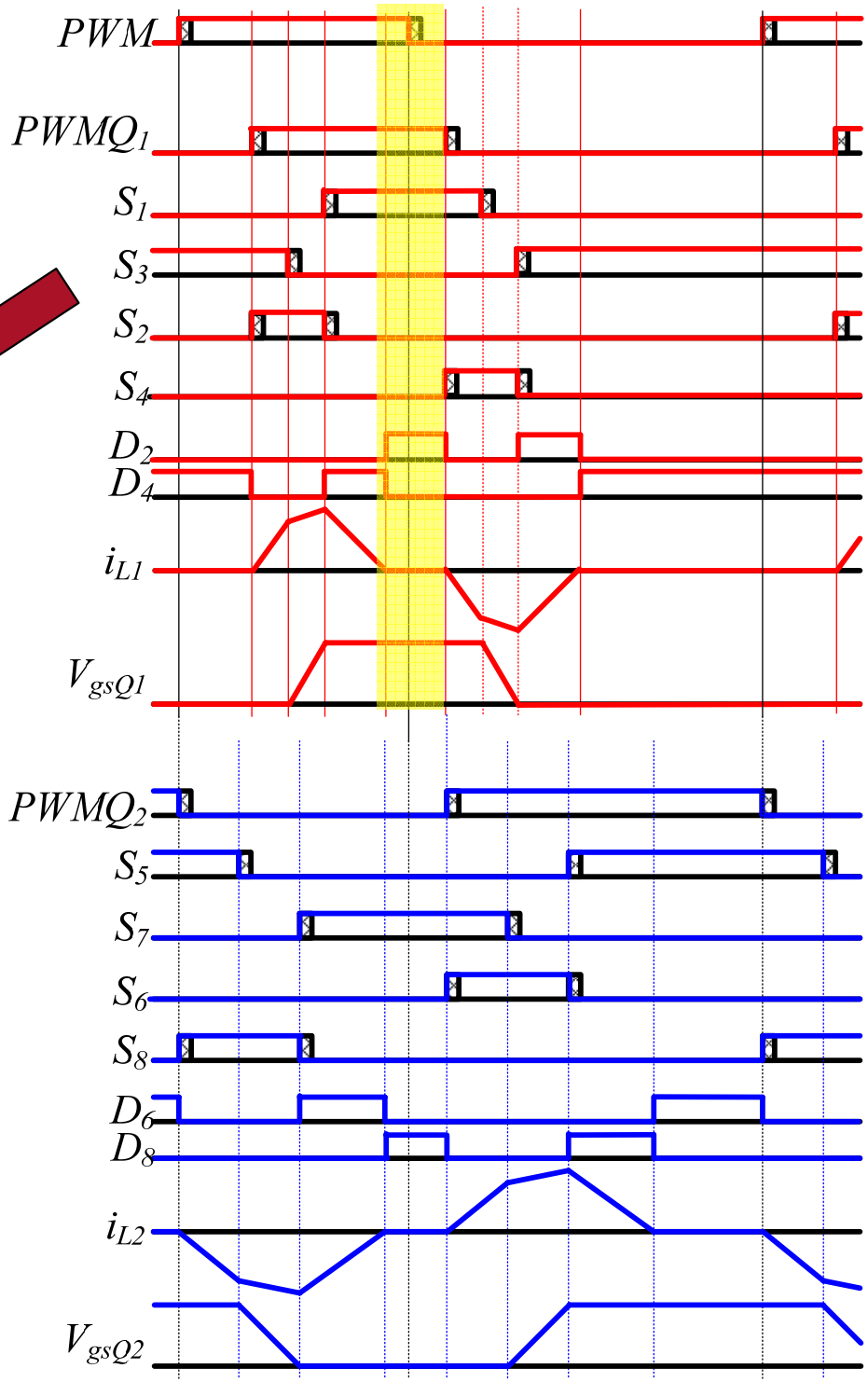
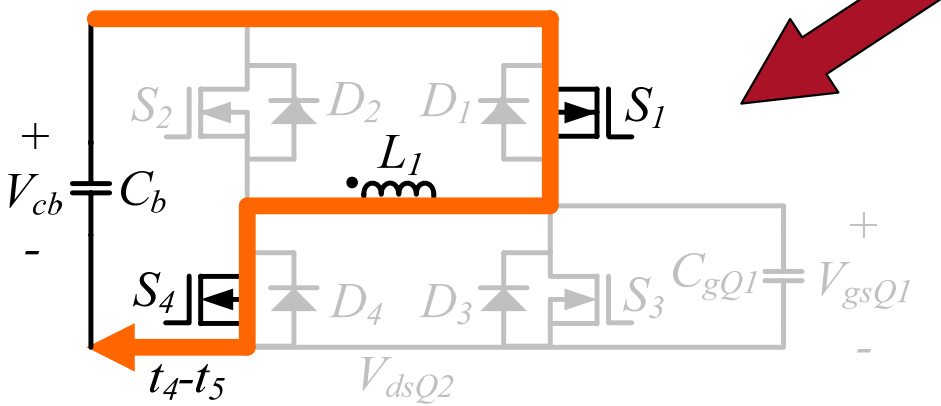
High Side MOSFET Turn On Sequence

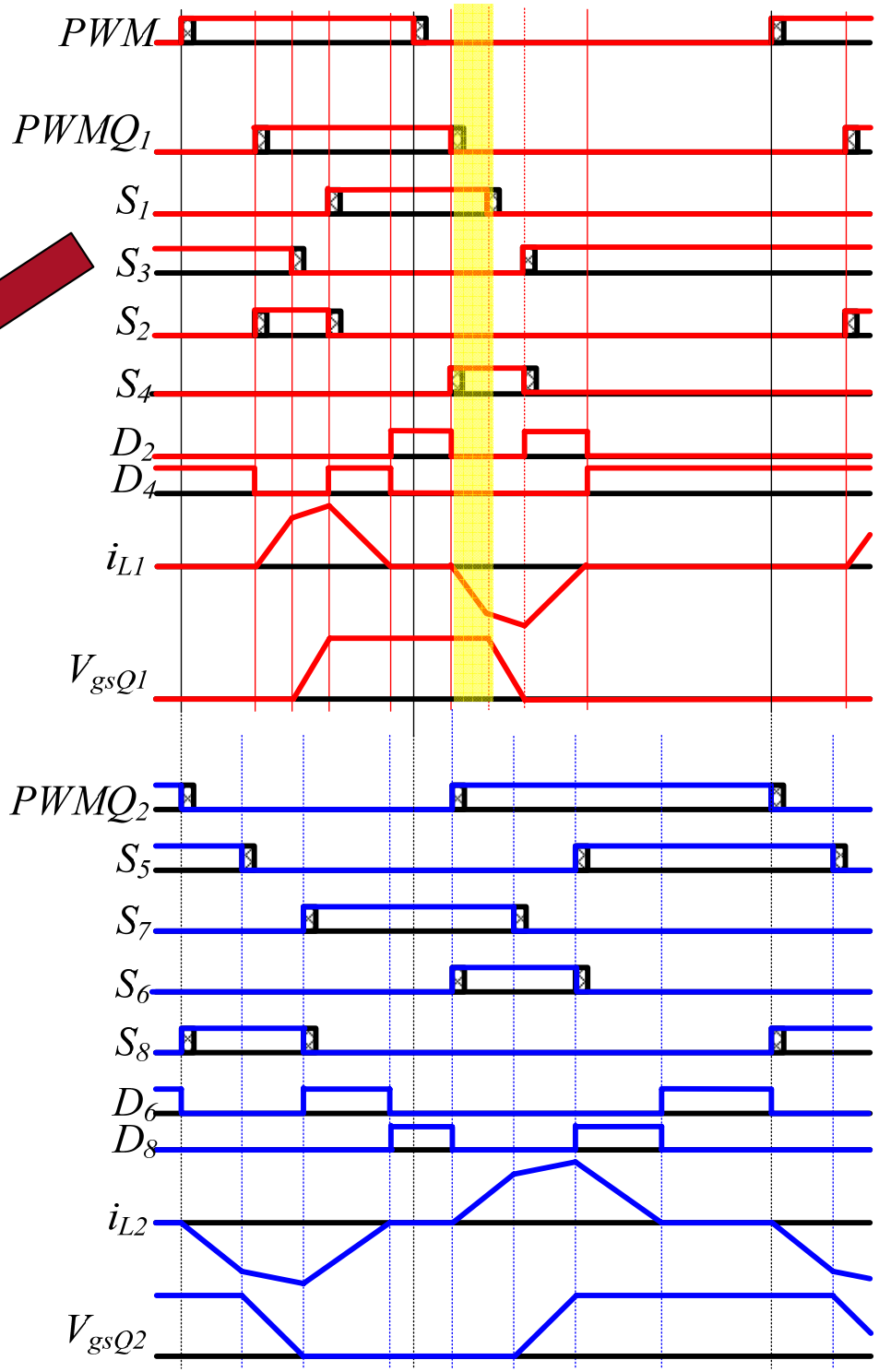




- **Dictated by $PWMQ_1$ signal**
- **Independent control of HS MOSFET and SR**

High Side MOSFET Turn Off Sequence

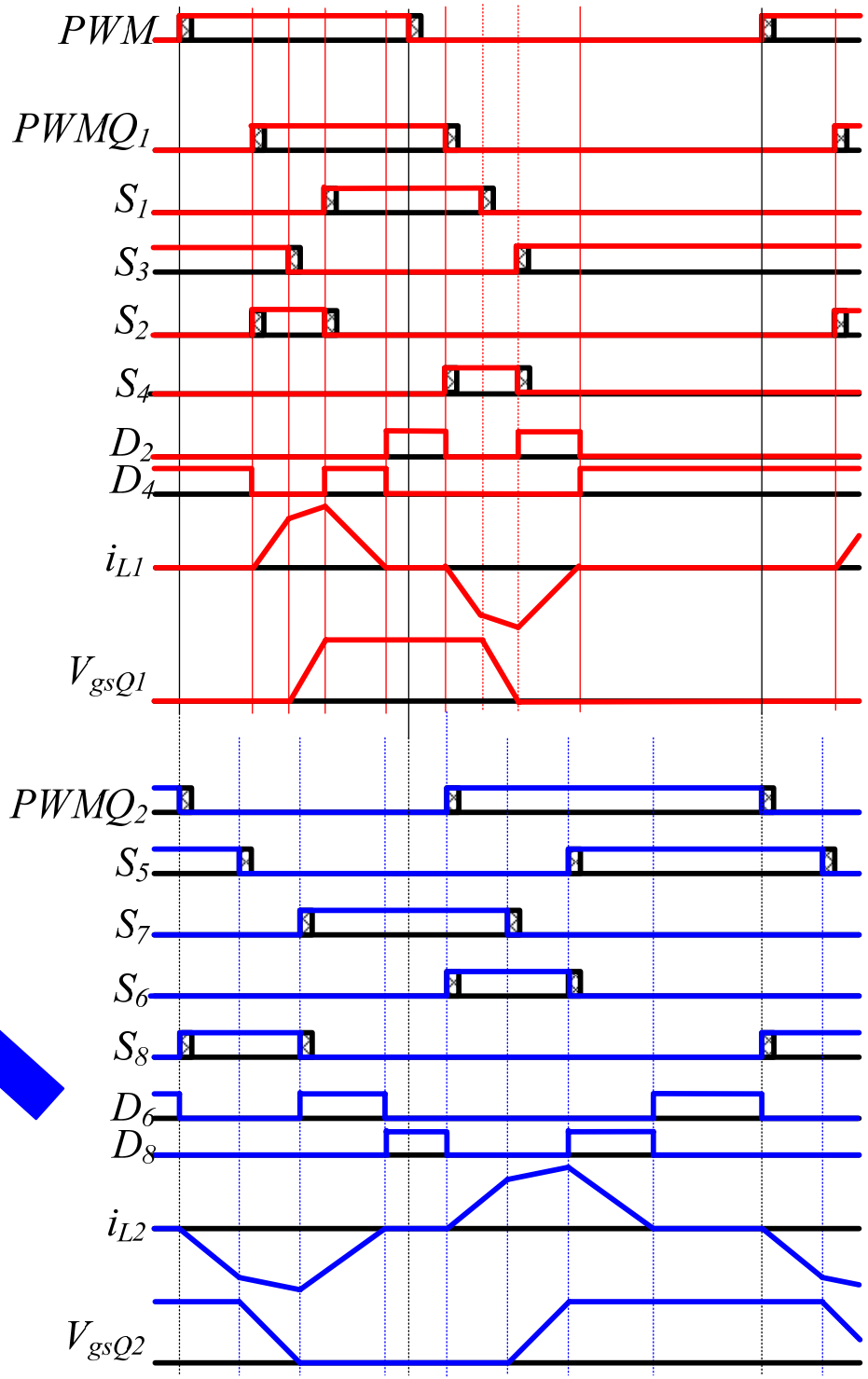




- **Dictated by $PWMQ_1$ signal**
- **Independent control of HS MOSFET and SR**

SR Operation

- Same procedure for SR
- Different time intervals due to larger gate charge
- Dictated by $PWMQ_2$ signal



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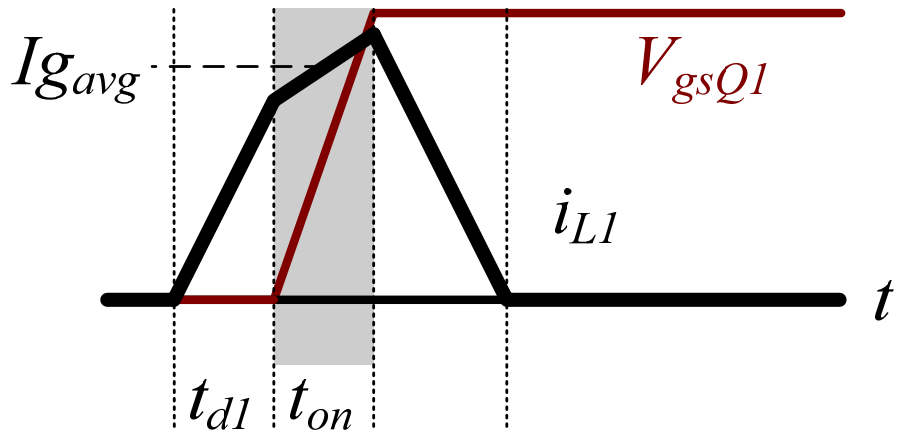
Driver Design

1. **Set the turn on time, or average gate current**
2. **Set inductor pre-charge time**
3. **Calculate the inductor value**

$$t_{on} = \frac{Q_g}{Ig_{avg}}, Ig_{avg} = \frac{Q_g}{t_{on}}$$

$$t_{d1} \approx \frac{1}{2} t_{on}$$

$$L_1 = \frac{V_{cb} t_{on}}{Q_g} \left(\frac{t_{on}}{4} + t_{d1} \right)$$



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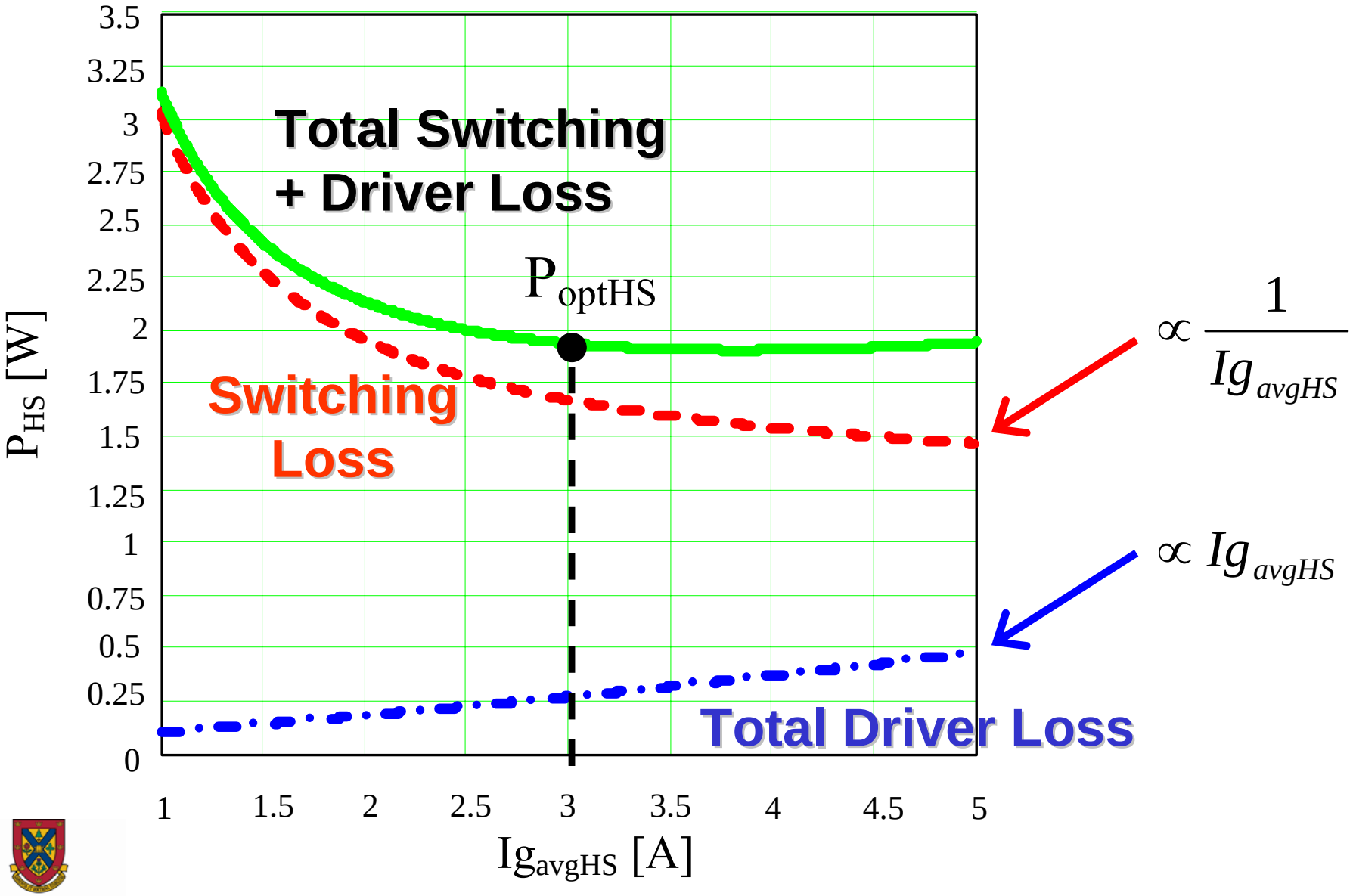
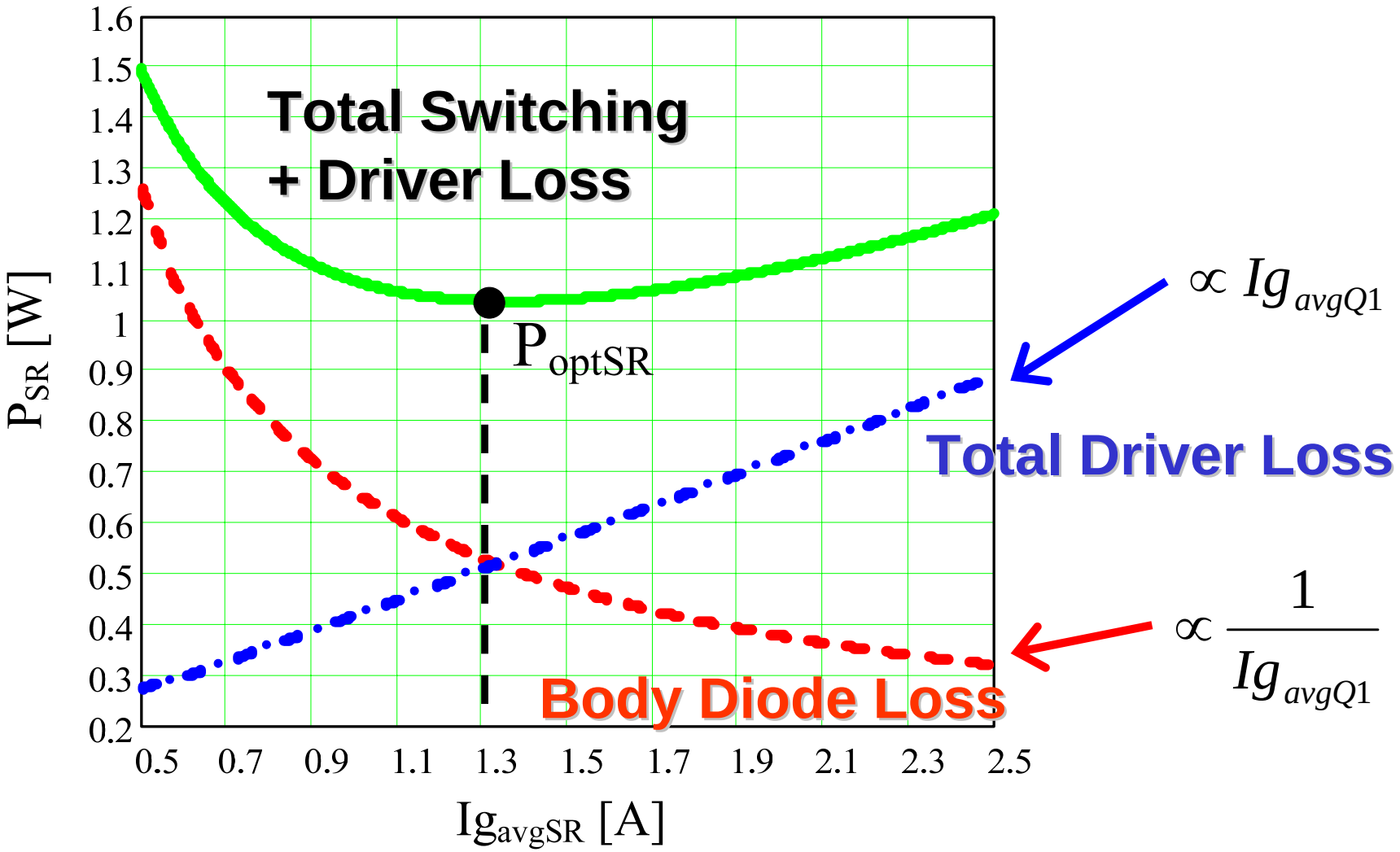
Optimizing HS Gate Current w.r.t. Driver Loss and Switching Loss



Optimizing SR Gate Current w.r.t. Driver Loss and Body Diode Loss



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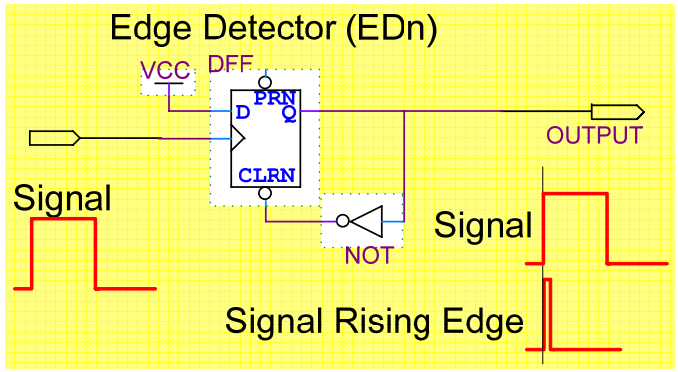
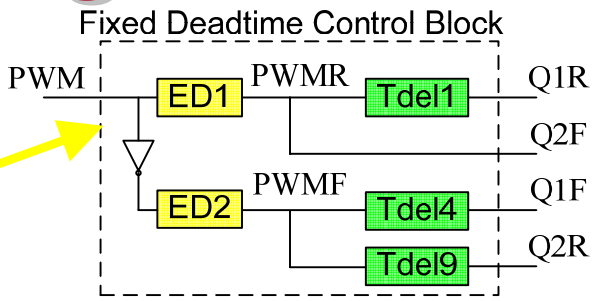
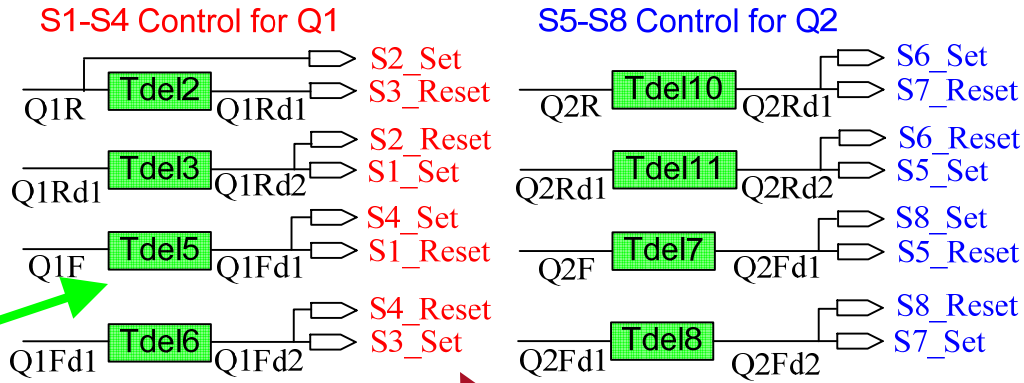
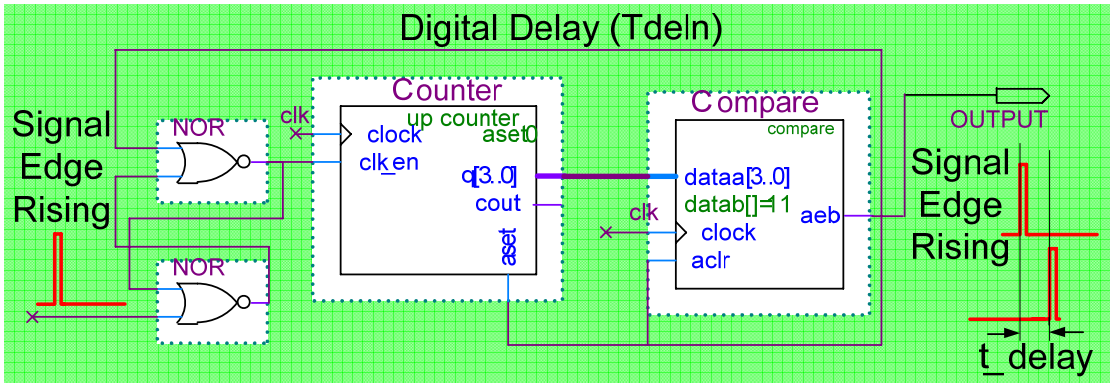
Logic Generation for Deadtime and S_1-S_4 Gating Signals









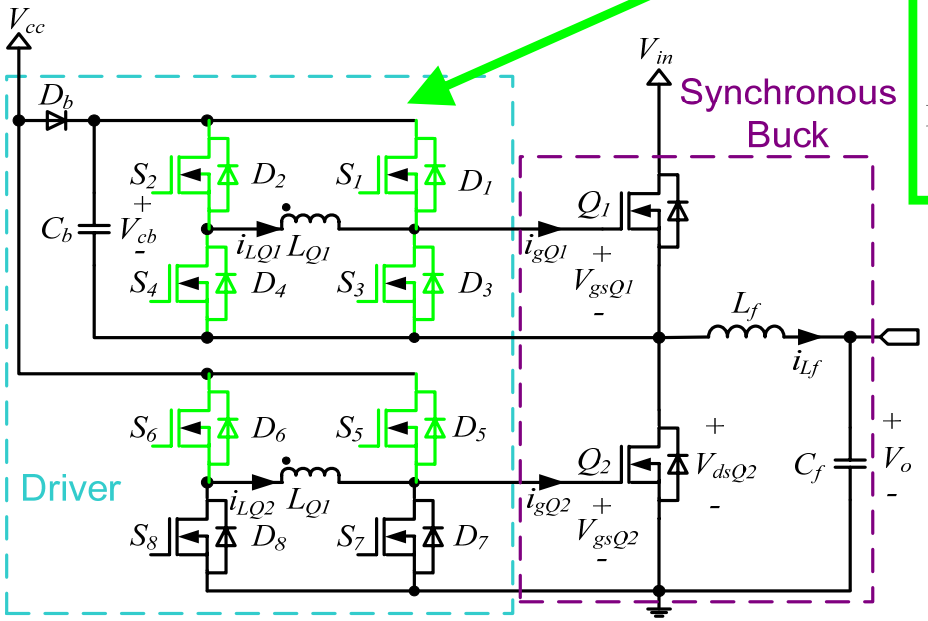
HS MOSFET

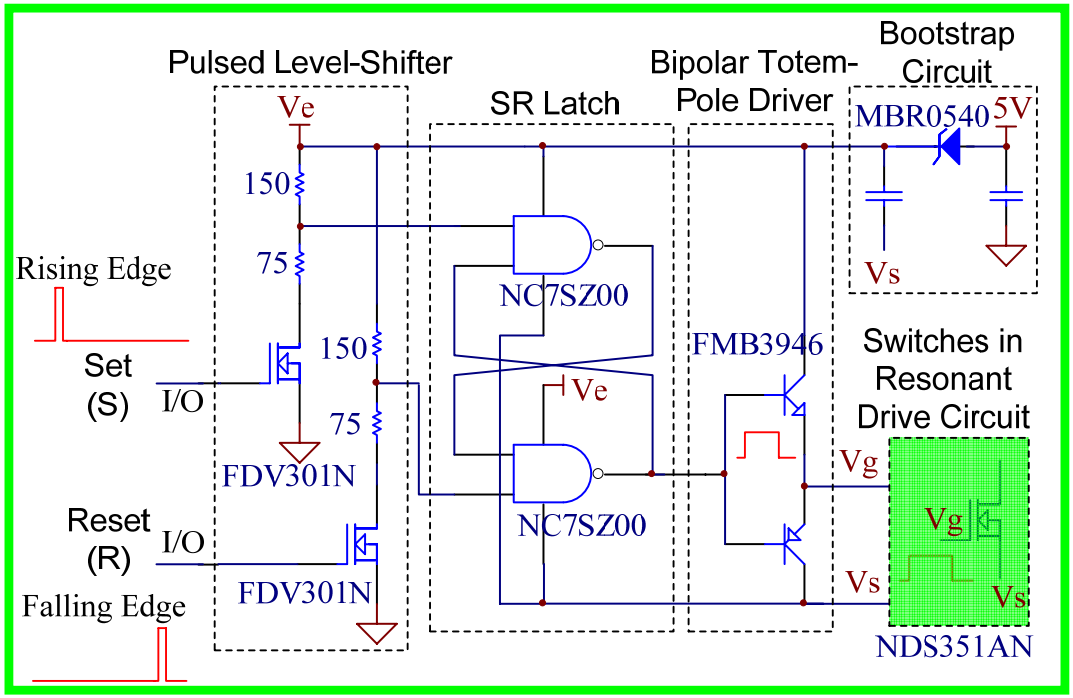
SR

Gating Signal Outputs

Level Shift Circuit

6 Switches (S_1-S_6) Require Level Shift Circuits





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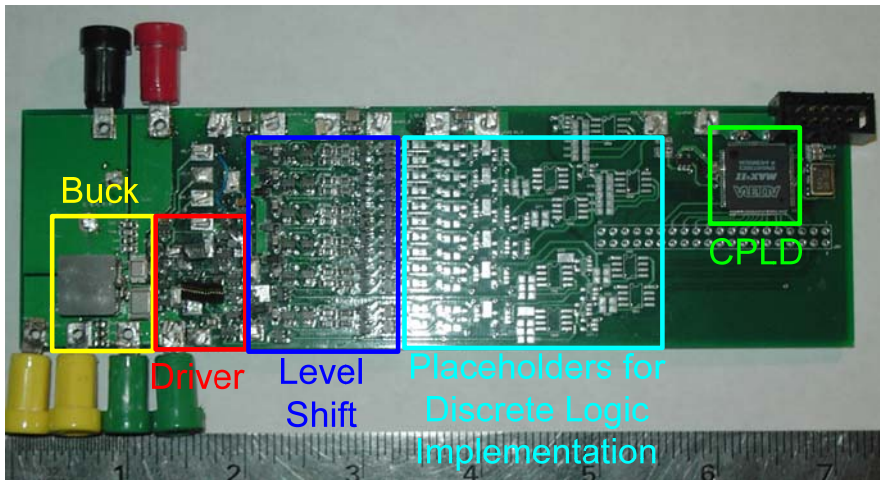
Experimental Setup and Specs

- **Single Phase Apples to apples comparison**
- **6-layer, 2oz**
- **12V Input**
- **1.3V Output**
- **Up to 30A Load**
- **1MHz**
- **IRF6617 HS**
- **IRF6691 SR**
- **330nH inductor: Vishay IHLP5050FD**

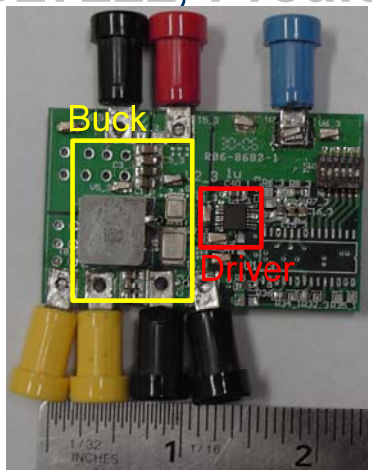
Current Source Driver

S_1-S_8: NDS351AN, L_1: 68nH, L_2: 307nH
2.5ns fixed maximum deadtime



Conventional Driver

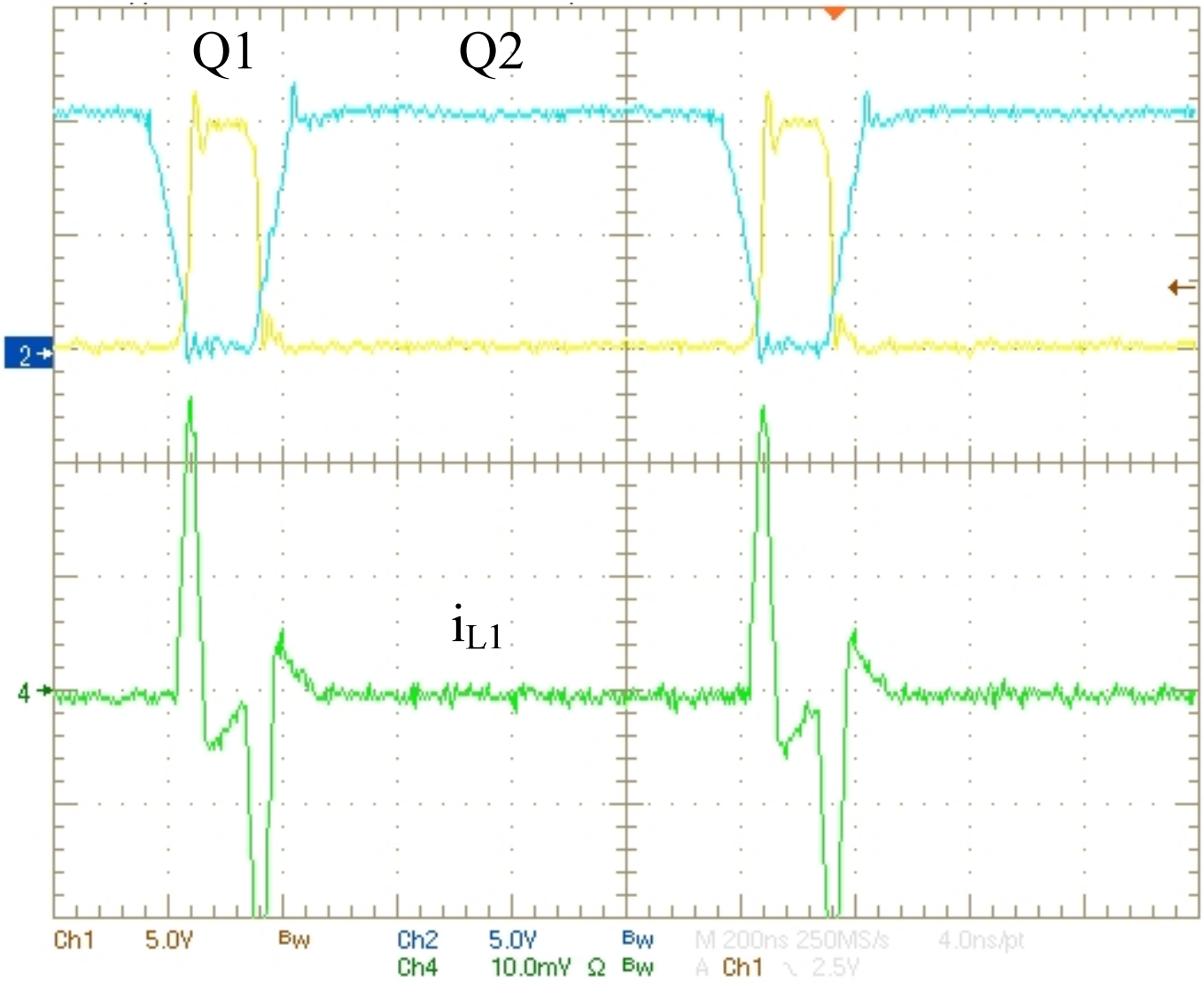
UCC27222, Predictive deadtime control



Waveforms

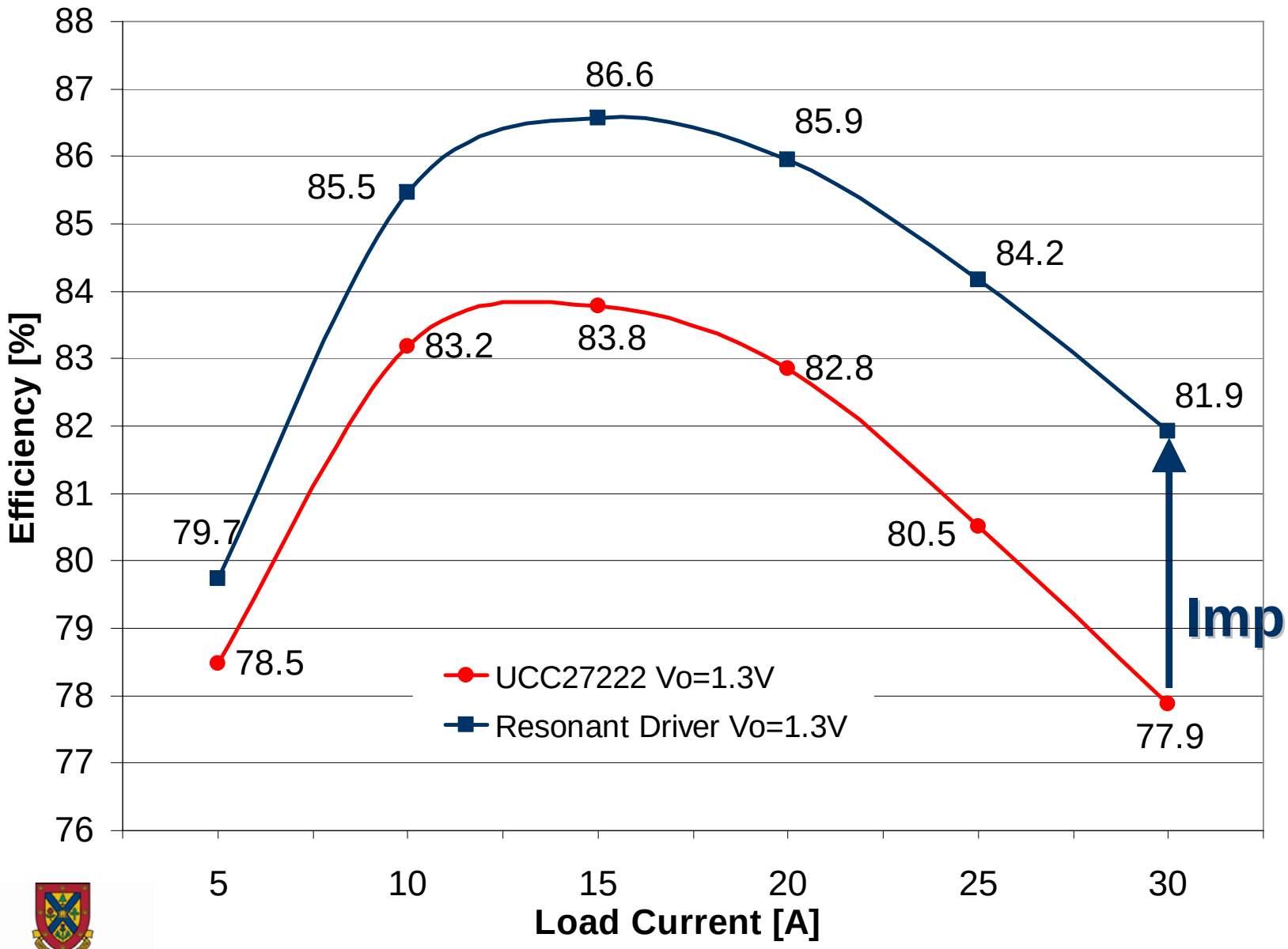
HS MOSFET and SR gate-source waveforms

HS MOSFET Driver Inductor Current Waveform



Efficiency vs. Load

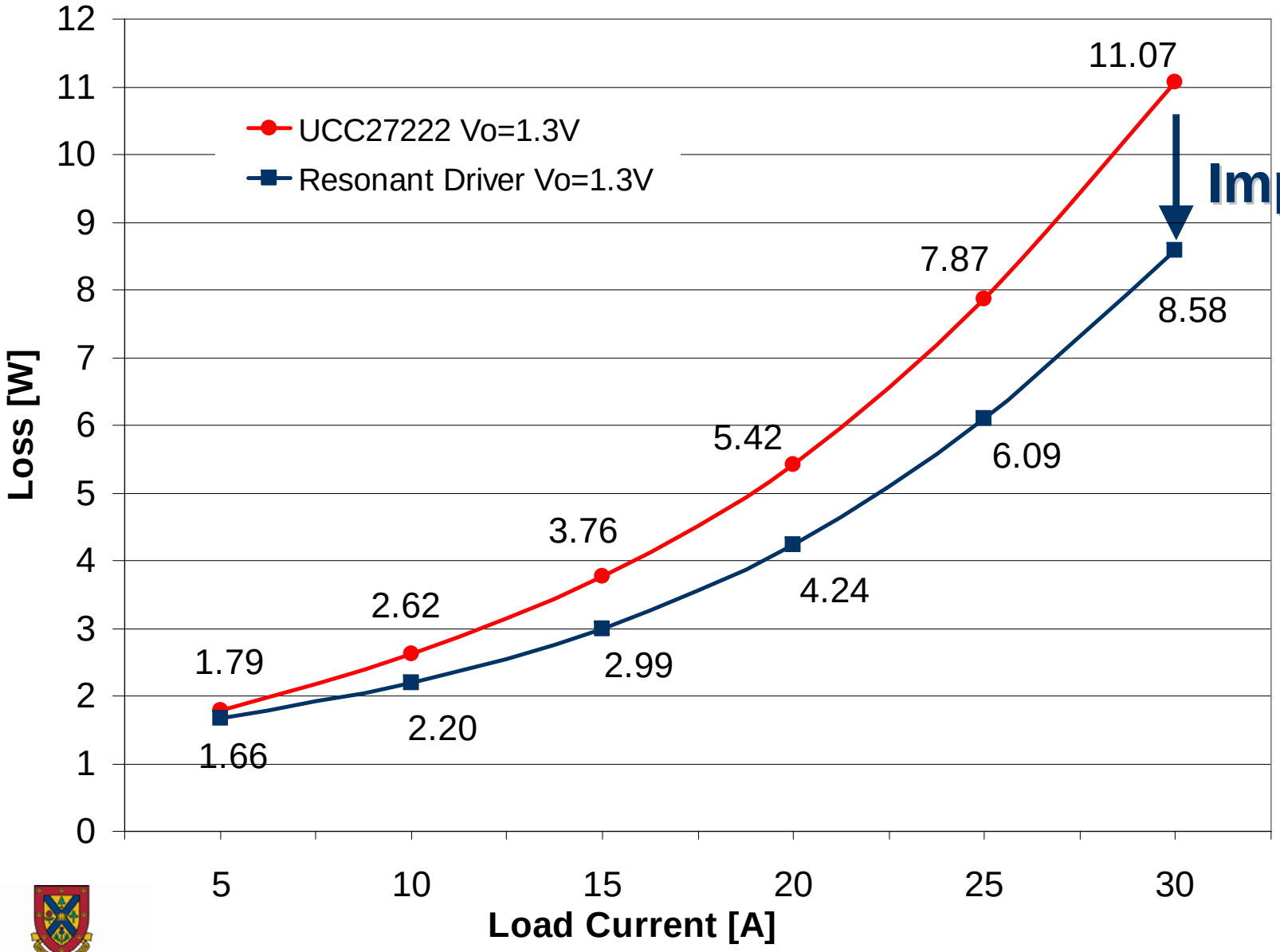
1MHz, 12V input, 1.3V load, 10V Vcc



4% Improvement!

Power Loss vs. Load

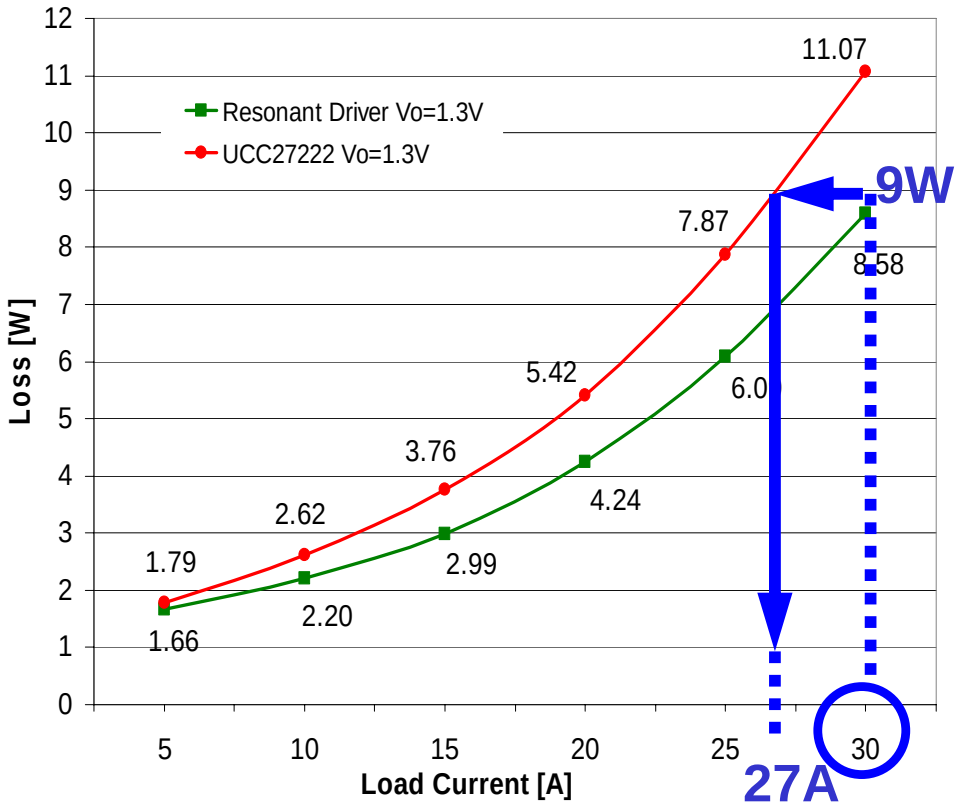
1MHz, 12V input, 1.3V load, 10V Vcc



2.5W Improvement Per Phase!

Implications of Loss Savings

- 15W savings (2.5Wx6) in a 6 phase VRM, or
- 120A output, assuming loss limited to 9W per phase:
  - 5 phases required for conventional driver (27A max per phase; 120A/27A=5 phases)
  - 4 phases required for current source driver (30A max per phase; 120A/30A=4 phases)
- 1 phase eliminated: A SIGNIFICANT COST SAVINGS



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Summary of Advantages

- Current source drive to increase switching speed, decrease switching loss and decrease conduction loss
- SR gate energy recovery (~50%) or higher operating Vcc
- Small driver inductors:
  - HS MOSFET: <100nH compared to 1uH+ for other competitor current source gate driver
- Optimized independent control of HS and SR gate currents
- Potential driver integration with no additional pins for HS MOSFET and 1 additional pin for SR

Conclusions

- Novel current source gate driver for synchronous buck VRM proposed
- Driver operation, design, optimization, logic, level shift and experimental results presented
- Driver achieves 4% efficiency improvement and 2.5W savings over conventional at 1MHz
- Elimination of 1 phase at 1.3V/120A load

Acknowledgements

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Ontario Centres of Excellence

C&D Technologies

Other interesting material available at:

www.queenspowergroup.com

Questions?