MOSFET Switching Loss Model and Optimal Design of A Current Source Driver Considering the Current Diversion Problem

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Abstract – A new analytical switching loss model for power MOSFETs driven by the Current Source Driver (CSD) is presented in this paper. The gate current diversion problem, which commonly exists in existing CSDs, is analyzed mathematically. In addition, a new accurate switching loss model considering every switching interval piecewisely is proposed. Based on the proposed loss model the optimal design of the CSD inductor is achieved to minimize the total power loss for the buck converter. The experimental result verifies the proposed switching loss model and optimal design. The measured loss matches the calculated loss very well; the error between the calculated loss and measured one is less than 10% from 5A load to 30A load with 12V input and 1.3V output. Compared with the previous work, the efficiency with the optimal CSD inductor is improved from 86.1% to 87.6% at 12V input, 1.3V/20A output and from 82.4% to 84.0% at 12V input, 1.3V/30A output at 1MHz switching frequency. Compared with the commercial DrMOSs from Renesas and International Rectifier, the buck converter with the optimal CSD still shows better performance.

Index Terms: current-source driver (CSD), power MOSFET, buck converter, voltage regulator (VR), common source inductor, loss model, current diversion problem, optimal design, Driver-MOSFET (DrMos)

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This paper falls in the category of: low power converters

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I. INTRODUCTION

As predicted by Moore´s Law, the number of transistors on a chip will double about every two years, which has been verified by Intel in the past 40 years. With more and more transistors on a microprocessor, power density has become a more critical parameter to evaluate the performance of Voltage Regulators (VRs) of a microprocessor.

Recently, a great deal of effort has been made to increase the power density of the VRs. One interesting area is to replace the magnetic-based converter with switched capacitor (also called charge pump) which consists of the inductorless configuration [2]. However, the large current spike, high EMI noise and narrow range of the voltage regulation limit the application of the switched capacitor [3]-[5].

Another interesting research field, which especially attracts the attention of semiconductor industries, is to integrate the VR into a single integrated chip, or called system-on-a-chip (SoC).[6]-[8] However, due to the tight cost requirement of the commercial products, the integration of the inductor with high current handling capability becomes the bottle neck, limiting the present current level of the SoC under 12Ampere [9] .

One of the practical ways is increasing the switching frequency of the VRs into MHz range to improve the dynamic performance and reduce the size of the passive components [10]-[12]. As the frequency increases, the frequency dependent losses such as switching loss and gate drive loss become a penalty for VRs driven with conventional voltage source drivers (VSD) [13]-[15]. In order to recover the gate driver loss dissipated in the charge and discharge path in the conventional voltage source driver, Resonant Gate Drive (RGD) techniques are proposed [16]-[19]. However, while RGD can recover the gate energy loss – it cannot reduce the switching loss, which is much higher than the gate loss in high frequency applications.

Recently, Current Source Drivers (CSDs) are proposed to reduce the switching loss by charging and discharging the MOSFET with a nearly constant current [20]-[23]. Another advantage of the CSDs is that the gate drive voltage of CSDs is bipolar [25], which means that CSDs can turn off the power MOSFET with a negative voltage. The CSD proposed in [21]-[23] can turn off the power MOSFET with -0.7V, while the CSD presented in [24] can turn off the power MOSFET with -3.5V. In comparison, conventional VSD

can only turn off the power MOSFET with +0.5V. Therefore, compared to VSD, CSDs can significantly reduce the turn-off loss, which is the dominant part of the whole switching loss.

However, during the switching transitions the current in the Current Source (CS) inductor is diverted, which reduces the effective driver current of the MOSFET. This is known as the current diversion problem, which commonly exists in CSDs. Therefore, the current diversion problem needs to be analyzed mathematically in order to predict and optimize the performance of the CSDs more accurately.

An analytical loss model, which thoroughly analyzes the impact of the parasitic inductance in CSDs, is presented in [27] to evaluate the performance of the CSDs. In addition, a generalized method to optimize the overall performance of the buck converter with a CSD is analyzed in the proposed model. A piecewise model that enables quick calculation and estimation of the switching loss is also proposed in [28]. However, the current diversion problem, which reduces the effective gate current and the switching speed, has not been investigated yet.

In this paper, a new analytical switching loss model considering the current diversion problem is proposed; the effective gate charging and discharging current is accurately determined. Moreover, the optimal current source inductor is obtained to maximize the overall efficiency of the buck converter. Since the model focuses on the performance of the CSD during turn-on and turn-off transitions of control FET, the parasitic inductances such as common source inductance and switching loop inductance for control FET that affect the switching transition have been considered. There are also some other parasitic elements from the PCB such as on-board inductance between the control FET and synchronous rectifier (sync FET). However, pervious studies in [29] and [30] have demonstrated that the on-board inductance mainly affects the ringing performance of the converter, but would barely introduce additional loss. The on-board resistance result from the layout increases the absolute value of the overall loss; but it will not interfere with the optimization procedure for the CSD as performance of the CSD is independent of the parasitic resistance.

The proposed switching loss model is presented in section II of this paper. Section III explains the procedures to obtain the optimal current source inductor. The experimental results of a synchronous buck converter with 12V input, 1.2V/30A output, 1MHz switching frequency and discussions are presented in section IV to validate the proposed loss model and optimal design of the CSD. Finally, the conclusions are drawn in section V.

II. Proposed Switching Loss Model Considering The Current Diversion

This section presents the operation principles of the CSD and a new switching loss model considering the gate current diversion problem.

The equivalent circuit of the MOSFET driven by proposed CSD is shown in Fig. 1 , where the power MOSFET Q is represented by a typical capacitance model, L_S is the common source inductance including the PCB track and the bonding wire inside the MOSFET package and L_D is the switching loop inductance.

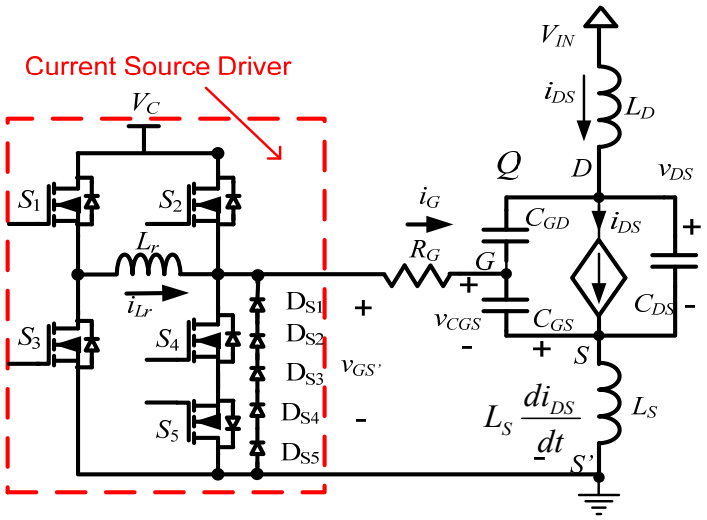


Fig. 1 Equivalent circuit of MOSFET with the proposed CSD

For the purpose of the transient analysis, the following assumptions are made [31]:

1) when $v_{CGS} < V_{TH}$, MOSET is OFF and I_{DS}=0. ($t<t_1$ or $t>t_4$ in Fig. 2)

2) when $v_{CGS} > V_{TH}$ and $v_{DS}>i_{DS}R_{DS(ON)}$, MOSFET is ACTIVE and $i_{DS}=g_{FS}(v_{CGS}-V_{TH})$. ($t_1<t<t_2$ or $t_3<t<t_4$ in Fig. 2)

3) when $g_{FS}(v_{CGS}- V_{TH}) > v_{DS}/R_{DS(ON)}$, the MOSFET is fully ON. ($t_2<t<t_3$ in Fig. 2)

where i_{DS} is the drain current of the Q, g_{FS} is the transconductance, v_{DS} is the voltage across the drain-source capacitance of the Q , v_{CGS} is the voltage across the gate-source capacitance of the Q, V_{TH} is the threshold voltage of Q , $R_{DS(ON)}$ is the on-state resistance of Q.

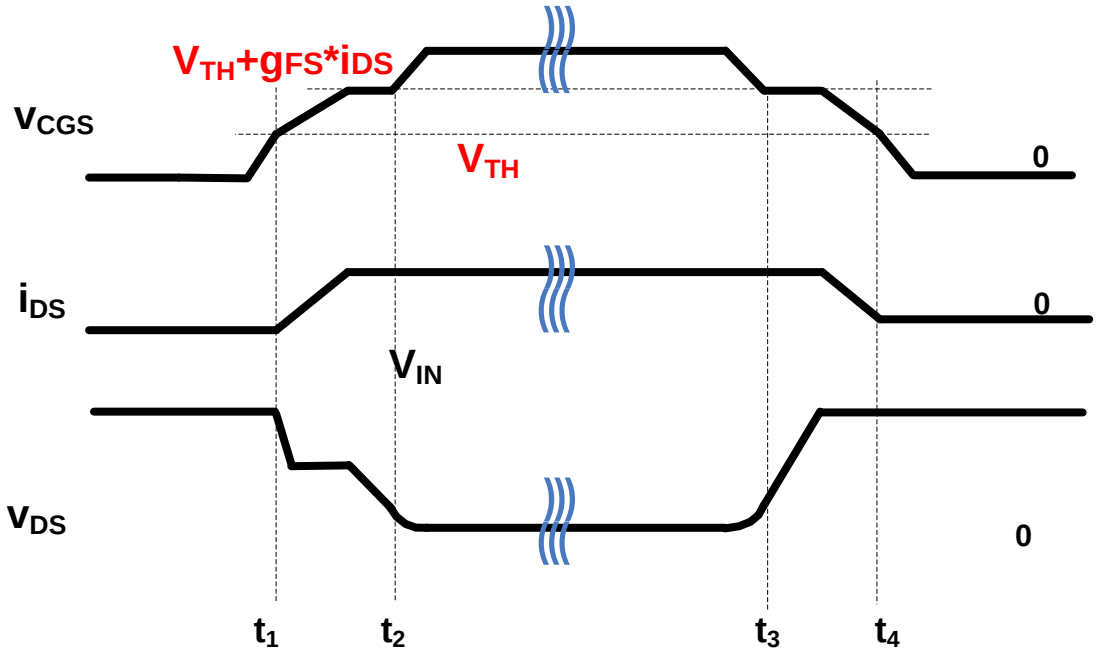


Fig. 2 Assumptions for power MOSFET for transient analysis

During the *Active State* when switching loss happens,

$$i_{DS} = g_{FS}(v_{CGS} - V_{TH}) \tag{1}$$

According to Fig. 1, i_G is the effective current to charge or discharge Q as shown below,

$$i_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt} \tag{2}$$

v_{DS} is given as,

$$v_{DS} = V_{IN} - L_D\frac{di_{DS}}{dt} - L_S\frac{d(i_{DS} + i_G)}{dt} \tag{3}$$

The detailed switching waveforms are illustrated in Fig. 3, where v_{GS1} to v_{GS5} are the gate drive signals for driver switches S_1 to S_5 in Fig. 1, i_{Lr} is the driver inductor current of L_r; $v_{GS'}$, as shown in (4), is the gate source voltage of Q including the effect of the common source inductance and the gate resistance, P_{SW} is the switching loss of the Q.

$$v_{GS'} = -i_G R_G + v_{CGS} - L_S\frac{d}{dt}(i_{DS} + i_G) \tag{4}$$

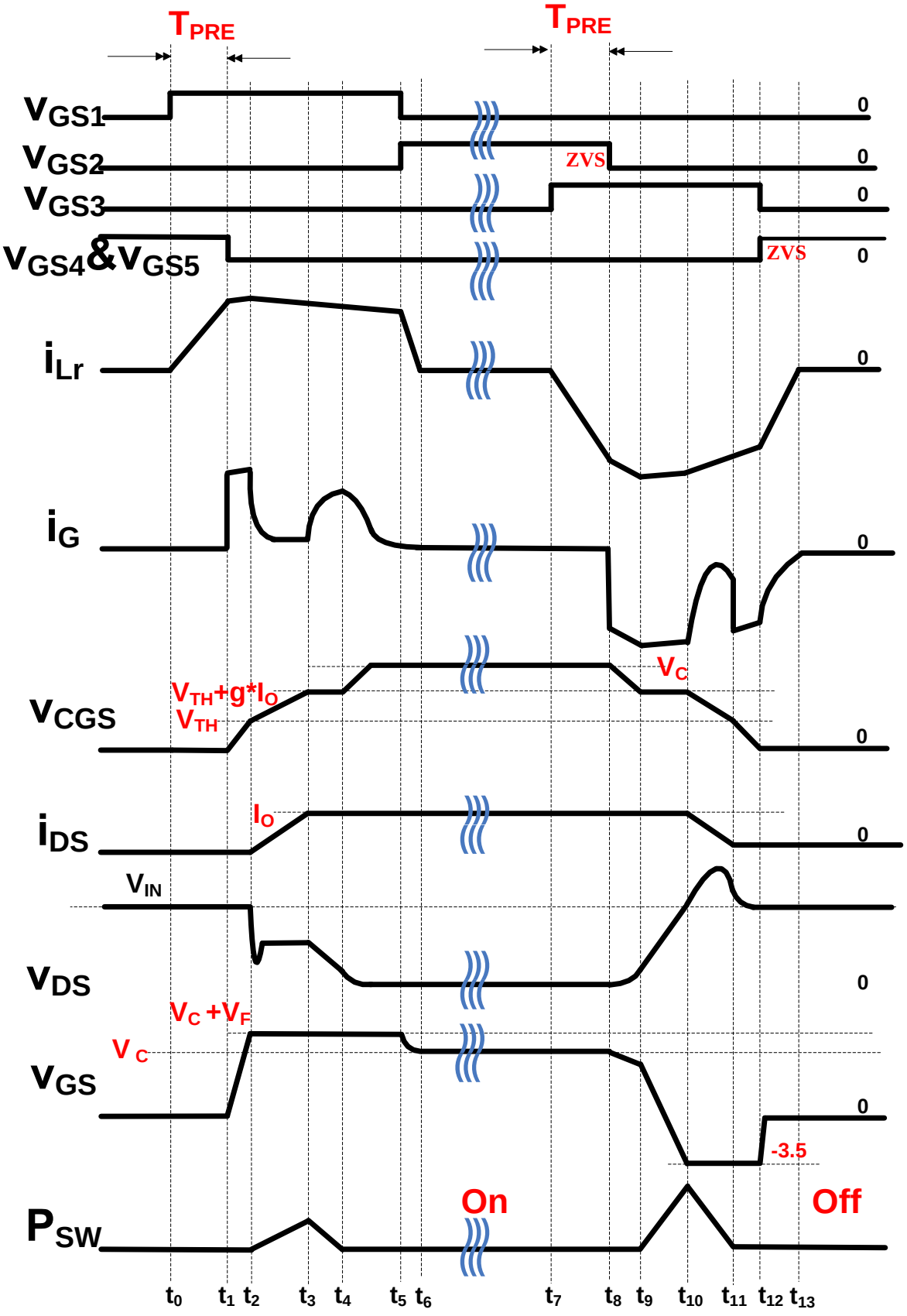


Fig. 3 MOSFET switching transition waveforms

The operation principle of the turn-on transition is presented as follows. Prior to t_0, the power MOSFET is clamped in the OFF state by S_4 and S_5. It is noted that it is difficult to derive accurate equations for the MOSFET capacitances due to their non-linear characteristic and limited information from the datasheet as well. So in this paper, the capacitances of MOSFET have been assumed to be constant as approximation, despite that some errors might be introduced.

A. Turn-ON Transition:

Precharge [t_0, t_1]: At t_0, S_1 is turned on, and the inductor current i_{Lr} rises almost linearly and the interval ends at t_1 which is preset by the designer. The equivalent circuit is given in Fig. 4 (a).The inductor current i_{Lr} is given in (5). The duration of this interval equals T_{PRE}.

$$i_{Lr} \approx \frac{V_C \cdot (t - t_0)}{L_r} \tag{5}$$

Turn-on Delay [t_1, t_2]: At t_1, S_4 &S_5 are turned off; the inductor current i_{Lr} starts to charge the gate capacitance of Q – the equivalent circuit is given in Fig. 4 (b). At this interval, the effective charge current i_G equals i_{Lr}. The initial condition of this interval is $i_{Lr\_t1} = i_{Lr}(t_1\text{-}t_0)$, *and* v_{CGS_t1}=0. This interval ends when v_{CGS} reaches V_{TH}. The differential equations for the circuit are given in (6), where R_{ON}= R_{DSON_S2}+ R_{Lr} + R_G, R_{DSON_S2} is the on-resistance of S_2, R_{Lr} is the dc resistance (DCR) of L_r and R_G is the gate-resistance of the power MOSFET.

$$V_C = (L_r + L_S)\frac{d}{dt}(i_{Lr}) + i_{Lr}R_{ON} + v_{CGS},\ i_{Lr} = (C_{GS} + C_{GD})\frac{d}{dt}(v_{CGS}) \tag{6}$$

Mathematically, there are three possible forms for the equation of the inductor current: over damped, critically damped and under damped – for practical situations, $\omega_0 > \alpha_0$, the equations for i_G, i_{Lr} and v_{CGS} are in the format of under damped as given in (7) ~ (8).

$$v_{CGS} = [A_0 \cos(\sqrt{\omega_0^2 - \alpha_0^2}\,t) + B_0 \sin(\sqrt{\omega_0^2 - \alpha_0^2}\,t)]e^{-\alpha_0 t} + C_0 \tag{7}$$

$$\begin{aligned} i_G = i_{Lr} = (C_{GS} + C_{GD})[&(-A_{01}\sqrt{\omega_0^2 - \alpha_0^2} + B_0\alpha_0)\sin(\sqrt{\omega_0^2 - \alpha_0^2}\,t) \\ &+ (-A_0\alpha - B_0\sqrt{\omega_0^2 - \alpha_0^2})\cos(\sqrt{\omega_0^2 - \alpha_0^2}\,t)]e^{-\alpha_0 t} \end{aligned} \tag{8}$$

Where $\alpha_0 = R_{ON}/2(L_r + L_S)$, $\omega_0 = 1/\sqrt{(L_r + L_S)(C_{GS} + C_{GD})}$,

$A_0 = -[2\alpha_0 i_{Lr\_t1} + (V_C - 2i_{Lr\_t1}R_{ON})/(L_r + L_S)]/[(C_{GS} + C_{GD})\omega_0^2]$,

$B_0 = (i_{Lr\_t1} + (C_{GS} + C_{GD})\alpha_0 A_0/[(C_{GS} + C_{GD})\omega_0^2]$, $C_0 = -A_0$

Drain Current Rising [t_2, t_3]: At t_2, $v_{CGS} = V_{TH}$. During this interval, v_{CGS} keeps increasing, and i_{DS} starts to rise according to the relationship in (1). Since i_{DS} flows through L_S, according to (4), the voltage induced across L_S makes $v_{GS'}$ larger than the driver supply voltage V_C. Therefore, D_2, the body diode of the driver switch S_2, is driven on to clamp $v_{GS'}$ at $V_C + V_F$, where V_F is the forward voltage of D_2.The equivalent circuit is shown in Fig. 4 (c). At this interval, i_G drops sharply because of the voltage clamping. The subtraction of i_{Lr} and i_G is diverted into D_2. The initial condition of this interval is $i_{G\_t2} = i_G(t_2\text{-}t_1)$, $i_{DS\_t2}=0$, *and* $v_{CGS\_t2}=V_{TH}$. The interval ends at t_3 when i_{DS} equals the load current, I_O.

Mathematically, there are three possible forms for the equation of the inductor current– for practical situations, $\omega_1<\alpha_1$, the equations for i_G, i_{Lr} and v_{CGS} are in the format of over damped as given in (9)~(13). It is noted that from (13) that i_G is largely determined by L_S: the larger L_S is, the smaller i_G is.

$$v_{CGS} = A_1 e^{(-\alpha_1-\sqrt{\alpha_1^2-\omega_1^2})t} + B_1 e^{(-\alpha_1+\sqrt{\alpha_1^2-\omega_1^2})t} + C_1 \tag{9}$$

$$i_{DS} = g_{FS}(v_{CGS} - V_{TH}) = g_{FS}(A_1 e^{(-\alpha_1-\sqrt{\alpha_1^2-\omega_1^2})t} + B_1 e^{(-\alpha_1+\sqrt{\alpha_1^2-\omega_1^2})t} + C_1 - V_{TH}) \tag{10}$$

$$i_G = A_1(-\alpha_1 - \sqrt{\alpha_1^2-\omega_1^2}) e^{(-\alpha_1-\sqrt{\alpha_1^2-\omega_1^2})t} + B_1(-\alpha_1 + \sqrt{\alpha_1^2-\omega_1^2}) e^{(-\alpha_1+\sqrt{\alpha_1^2-\omega_1^2})t} \tag{11}$$

$$i_{Lr} = (I_{G\_t2} + V_F/R_G) e^{(-R_G/L_r)t} - V_F/R_G \tag{12}$$

$$v_{DS} = V_{IN} - L_D \frac{d}{dt}(i_G) - (L_S + L_D)\frac{d}{dt}(i_{DS}) \tag{13}$$

Where $\omega_1 = 1/\sqrt{L_S(C_{GS}+C_{GD})}$, $\alpha_1 = [R_G(C_{GS}+C_{GD}) + L_S g_{FS}]/[L_S(C_{GS}+C_{GD})]$, $C_1 = V_F + V_c$,

$A_1 = [(V_{TH} - V_F - V_C)(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) - I_{G\_t2}]/[2\sqrt{\alpha_1^2 - \omega_1^2}]$, $B_1 = V_{TH} - A_1 - C_1$

Miller Plateau [t_3, t_4]: At t_3, $i_{DS} = I_O$. During this interval, v_{CGS} is held at the Miller Plateau voltage. i_G mainly flows through the gate-to-drain capacitance of Q, and v_{DS} decreases accordingly. It is noted that i_G starts to rapid increase since the EMF across L_s falls sharply due to the unchanged i_{DS}, however part of the inductor current is still diverted through D_2. The equivalent circuit is given in Fig. 4 (d). The initial values of the interval are $i_{G\_t3}=i_G(t_3\text{-}t_2)$, $v_{CGS\_t3}=v_{CGS}(t_3\text{-}t_2)$, and $v_{DS\_t3}=v_{DS}(t_3\text{-}t_2)$.The interval ends when v_{DS} equals zero at t_4 . The equations for i_G, v_{CGS} and v_{DS} are given in (14) ~ (15). i_{Lr} remains the same as the previous interval.

$$v_{CGS} = V_{CGS\_t3} \tag{14}$$

$$i_G = [I_{G\_t3} - (V_C + V_F - V_{CGS\_t3})/R_G] e^{(-R_G/L_s)t} + (V_C + V_F - V_{CGS\_t3})/R_G \tag{15}$$

$$v_{DS} = \left(\frac{I_{G\_t3} - (V_C + V_F - V_{CGS\_t3})/R_G}{C_{GD}R_G/L_s}\right)e^{(-R_G/L_s)t} - \frac{(I_{G\_t3} - (V_C + V_F - V_{CGS\_t3})/R_G)t}{C_{GD}} + \left(V_{DS\_t3} - \frac{I_{G\_t3} - (V_C + V_F - V_{CGS\_t3})/R_G}{C_{GD}R_G/L_s}\right) \quad (16)$$

Remaining Gate Charging [t_4, t_5]: At t_4, $v_{DS} = 0$ and v_{CGS} starts to rise again until it reaches V_C. $v_{GS'}$ remains at V_C+V_F, and due to the rising of the v_{CGS}, i_G decreases gradually. The equivalent circuit is given in Fig. 4 (e). The initial values of this interval are: $i_{G\_t4}=i_G(t_4\text{-}t_3)$, $v_{CGS\_t4}=v_{CGS\_t3}$, *and* $v_{DS\_t4}=v_{DS}(t_4\text{-}t_3)$. This interval ends at t_5 when $v_{CGS}= V_C$.

Mathematically, there are three possible forms for the equation of the inductor current– for practical situations, $\omega_2<\alpha_2$, therefore equations for i_G, v_{CGS} and v_{DS} are in the format of over damped given in (16) ~ (19) and i_{Lr} is the same as the previous interval.

$$v_{CGS} = [A_2\cos(\sqrt{\alpha_2^2 - \omega_2^2}\,t) + B_2\sin(\sqrt{\alpha_2^2 - \omega_2^2}\,t)]e^{-\alpha_2 t} + C_2 \quad (17)$$

$$i_G = (C_{GS} + C_{GD})[(-A_2\sqrt{\alpha_2^2 - \omega_2^2} + B_2\alpha_2)\sin(\sqrt{\alpha_2^2 - \omega_2^2}\,t) + (-A_2\alpha_2 - B_2\sqrt{\alpha_2^2 - \omega_2^2})\cos(\sqrt{\alpha_2^2 - \omega_2^2}\,t)]e^{-\alpha_2 t} \quad (18)$$

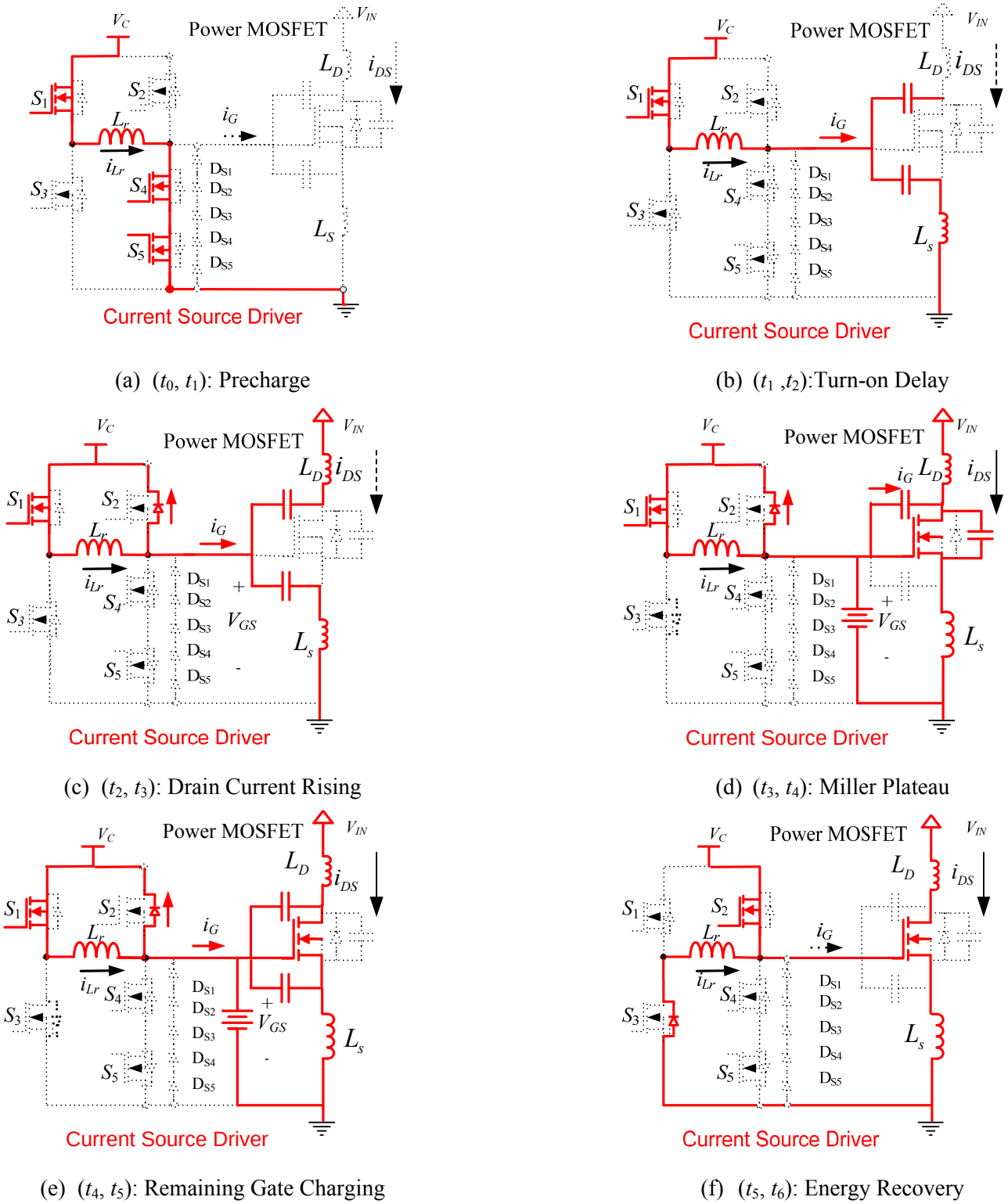
$$v_{DS} = V_{DS\_t4} - \frac{(v_{CGS} - V_{DS\_t4})(V_{DS\_t4} - I_O R_{ON@V_c})}{V_C - V_{CGS\_t4}} \quad (19)$$

Where $\omega_2 = 1/\sqrt{L_S(C_{GS} + C_{GD})}$, $\alpha_2 = R_G/L_S$, $A_2 = V_{CGS\_t3} - C_2$, $B_2 = [I_{G\_t4}/(C_{GS} + C_{GD}) - A_2\alpha_2]/\sqrt{\alpha_2^2 - \omega_2^2}$,

$C_2 = V_C + V_F$ and $R_{ON@VC}$ is the on-resistance of the MOSFET when $V_{CGS}=V_C$

Energy Recovery [t_5, t_6]: At t_5, S_2 is turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to V_C. The initial value of this interval is $i_{Lr\_t5} = i_{Lr}(t_5\text{-}t_2)$, and this interval ends when i_{Lr} becomes zero. The equivalent circuit is illustrated in Fig. 4 (f). The equation for i_{Lr} is in (20). It is noted that the current slew rate of this interval is larger than that of the *Precharge* interval due to the larger voltage drop across the inductor L_r during this interval.

$$i_{Lr} = [I_{G\_t5} + (V_C + V_F)/(R_{ON\_S2} + R_{L_r})]e^{[-(R_{ON\_S2} + R_{L_r})/L_r]t} - (V_C + V_F)/(R_{ON\_S2} + R_{L_r}) \quad (20)$$



(a) (t_0, t_1): Precharge

(b) (t_1, t_2):Turn-on Delay

(c) (t_2, t_3): Drain Current Rising

(d) (t_3, t_4): Miller Plateau

(e) (t_4, t_5): Remaining Gate Charging

(f) (t_5, t_6): Energy Recovery

Fig. 4 Turn-on transition

B. Turn-OFF Transition:

In this section, the turn-off transition is analyzed. Prior to t_7, the power MOSFET is clamped in the ON state by S_2.

Predischarge[t_7, t_8]: At t_7, S_3 is turned on, and the inductor current i_{Lr} rises almost linearly and the interval ends at t_8 which is preset by the designer. The equivalent circuit is shown in Fig. 5 (a). The equation for i_{Lr} is given in (21). The duration of this interval equals T_{PRE}.

$$i_{Lr} \approx -\frac{V_C \cdot (t - t_7)}{L_r} \tag{21}$$

Turn-off Delay [t_8, t_9]: At t_8, S_2 is turned off. In this interval, v_{CGS} decreases until $V_{TH} + I_O * g_{FS}$ which ends the interval. The equivalent circuit is given in Fig. 5 (b). The initial condition of this interval is $i_{G\_t8} = i_{Lr\_t8} = i_{Lr}(t_8)$, $v_{CGS\_t8} = V_C$. The way to solve the equations for i_G, i_{Lr} and v_{CGS} are the same as *Turn-on Delay* interval.

Miller Plateau [t_9, t_{10}]: At t_9, $v_{CGS} = V_{TH} + I_O * g_{FS}$. In this interval, v_{CGS} holds at the Miller plateau voltage, $V_{TH} + I_O * g_{FS}$. i_G (equal to i_{Lr}) strictly discharges the gate-to-drain capacitance C_{GD} of Q, and v_{DS} rises until it reaches V_{IN} at t_{10}. The equivalent circuit is illustrated in Fig. 5 (c). The equations of this interval can be obtained in the same way as the *Miller Plateau* in turn-on interval.

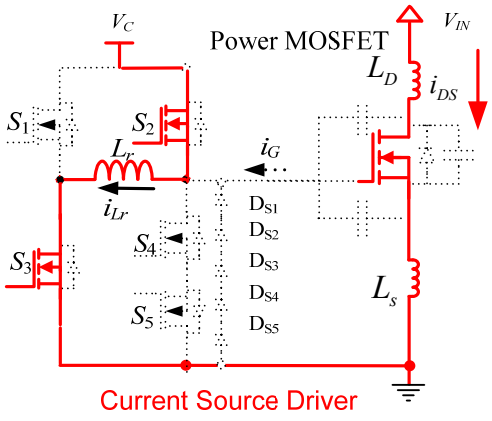
Drain Current Drop [t_{10}, t_{11}]: At t_{10}, $v_{DS} = V_{IN}$ and v_{CGS} continues to decrease from $V_{TH} + I_O * g_{FS}$ to V_{TH}. i_{DS} falls from I_O to zero according to relationship in (1). According to (4), due to the induction EMF across L_s, the series connected diodes D_{S1} to D_{S5} are driven on to clamp $v_{GS'}$ at around -3.5V. The voltage across the current source inductor becomes -3.5V, so i_{Lr} decreases at a higher rate than in the turn-on transition. The equivalent circuit of this interval is given in Fig. 5 (d).

By comparison, the CSD proposed in [21] only can clamp $v_{GS'}$ to -0.7V during this interval. According to [25], the CSD in [21] turns off the power MOSFET within 15.6nS while the turn-off time of the CSD shown in this paper is 8.7nS. This means that the turn-off loss of the CSD in this paper (Fig. 1) is much smaller than that of the CSD in [21]. It is worth mentioning that v_{DS} in this interval will keep rising due to effect of the L_S. Therefore, the derivation of the equations in this interval needs to solve the 3rd order differential equations set in (22).

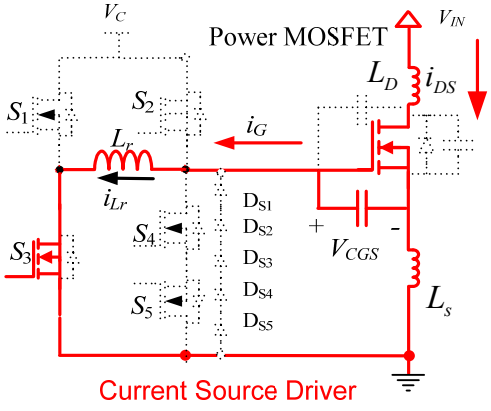
$$\begin{cases} L_S \dfrac{d}{dt}(i_{DS} + i_G) + v_{CGS} + i_G R_G + V_F = 0 \\ i_{DS} = g_{FS}(v_{CGS} - V_{TH}) \\ i_G = (C_{GS} + C_{GD}) \dfrac{d}{dt}(v_{CGS}) - C_{GD} \dfrac{d}{dt}(v_{DS}) \\ L_S \dfrac{d}{dt}(i_G) + (L_D + L_S) \dfrac{d}{dt}(i_{DS}) + v_{DS} - V_{IN} - V_F = 0 \end{cases} \tag{22}$$

Remaining Gate Discharging [t_{11}, t_{12}]: At $t_{11,}$ v_{CGS}= V_{TH}. In this interval, v_{CGS} continues to decrease until it equals zero; it is noted that v_{DS} continues to rise during this interval. The equivalent circuit is shown in Fig. 5 (e). The equations in this interval have the same form as the equations in *Remaining Gate Charging* Interval.

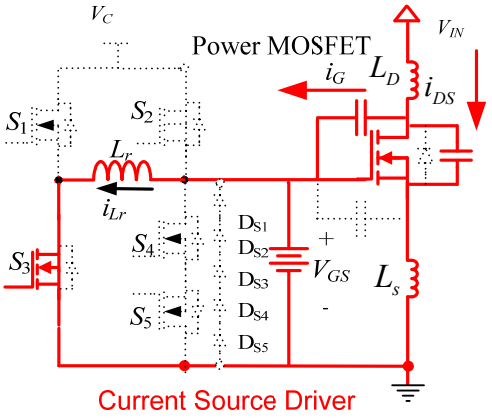
Energy Recovery [t_{12}, t_{13}]: At t_{12}, S_4 &S_5 are turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to ground. The equivalent circuit is given in Fig. 5 (f). This interval is the same as the *Energy Recovery* in turn-on transition.



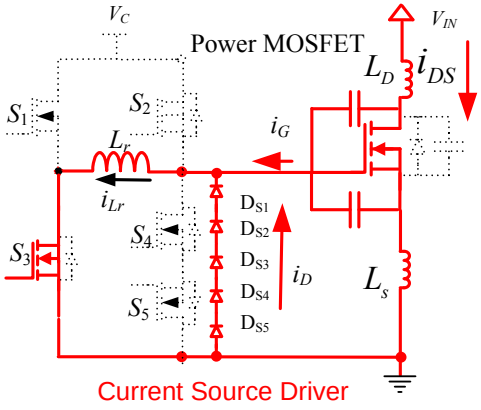
(a) (t_7, t_8): Predischarge



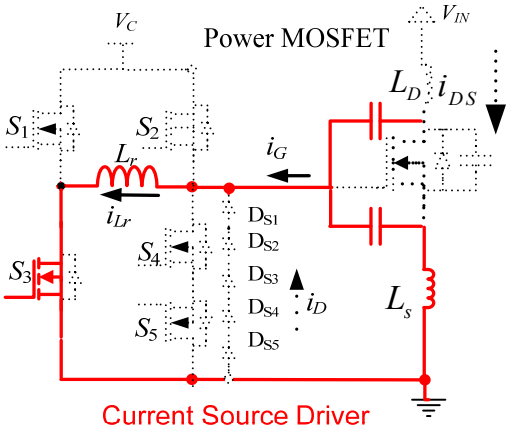
(b) (t_8 ,t_9): Turn-off Delay



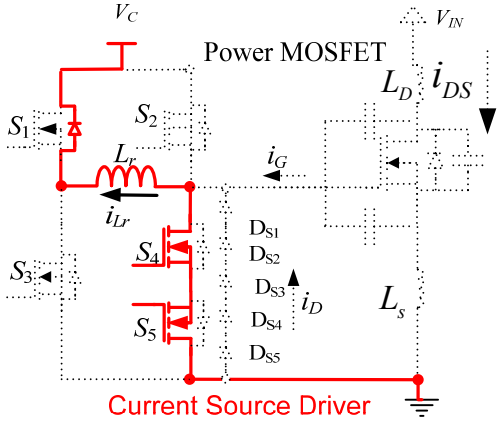
(c) (t_9, t_{10}): Miller Plateau



(d) (t_{10}, t_{11}): Drain Current Drop



(e) (t_{11}, t_{12}): Remaining Gate Discharge



(f) (t_{12}, t_{13}): Energy Recovery

Fig. 5 Turn-off transition

C. Total Loss for the power MOSFET driven with the proposed CSD:

In this section, the procedure to calculate the total loss of the power MOSFET driven with the proposed CSD will be explained.

1. Turn-on loss P_{SW_ON} equals the energy lost in each turn-on transition times F_S, where F_S is the switching frequency. As expressed in (23), before turn-on transition begins, some energy has already been stored in the output capacitance of the MOSFET. This energy together with the energy supplied by the source is dissipated through the turn on transition.

$$P_{SW\_ON} = E_{Lost\_ON} \cdot F_S = \left(\frac{C_{oss} \cdot Q_{oss}}{2} + \int_{t2}^{t4} (i_{DS} \cdot v_{DS}) dt \right) \cdot F_S \tag{23}$$

Turn-off loss P_{SW_OFF} equals the energy lost in each turn-off transition times F_S. After turn-off transition ends, some energy is still stored in the output capacitance of the MOSFET; therefore P_{SW_OFF} can be derived in (24).

$$P_{SW\_OFF} = E_{Lost\_OFF} \cdot F_S = \left(\int_{t9}^{t11} (i_{DS} \cdot v_{DS} \cdot F_S) dt - \frac{C_{oss} \cdot Q_{oss}}{2} \right) \cdot F_S \tag{24}$$

Switching loss, P_{SW} equals the sum of turn-on loss P_{SW_ON} and turn-off loss P_{SW_OFF}, as derived in (25).

$$P_{SW} = P_{SW\_ON} + P_{SW\_OFF} \tag{25}$$

2. The gate driver loss P_{DR} is made up of conduction loss P_{DR_COND}, gate drive loss P_{DR_GATE} and output loss P_{DR_OUT} as given in (26).

$$P_{DR} = P_{DR\_COND} + P_{DR\_GATE} + P_{DR\_OUT} \tag{26}$$

3. Conduction loss P_{COND} is calculated in (27), where I_O is the drain-to-source current when power MOSFET is on, $R_{DS(ON)}$ is the on-resistance of the MOSFET, T_{ON} is the on time and T_S is the switching cycle.

$$P_{COND} = {I_O}^2 \cdot R_{DS(ON)} \cdot \frac{T_{ON}}{T_S} \tag{27}$$

4. The total loss for the power MOSFET driven with proposed CSD, P_{SUM}, is

$$P_{SUM} = P_{DR} + P_{SW} + P_{COND} \tag{28}$$

III. Optimal Design of Inductor Value of the CSD

According to [21], the RMS current of the current source inductor L_r during the precharge and predischarge interval, I_{Lr_RMS}, is calculated in (29), where T_{PRE} is the prechage time (t_0-t_1) and predischarge time (t_7-t_8). Therefore, the conduction loss at these two intervals is positively related to the precharge time T_{PRE}.

$$I_{Lr\_RMS} \approx i_{Lr\_t1} \cdot \sqrt{\frac{T_{PRE} \cdot F_S}{3}} \approx \frac{V_C \cdot T_{PRE}}{L_r} \cdot \sqrt{\frac{T_{PRE} \cdot F_S}{3}} \tag{29}$$

As the current in the current source inductor between Fig. 4 (b) to (e) and between Fig. 5 (b) to (e) roughly remains constant, therefore the RMS current for these two intervals is approximately the same as i_{Lr_t1}.

The RMS current during Fig. 4 (f) and Fig. 5 (f) is approximately the same as (29) according to [21]. Therefore, T_{PRE} should be set as short as possible within the practical limits of the driver to minimize the conduction loss. Taken the logic limits into consideration, T_{PRE} is set to be 20 nanoseconds. And it needs to be pointed out that the design procedure presented here is also applicable to other conditions.

In order to maximize the overall efficiency of the buck converter with the proposed CSD, P_{SUM} should be minimized. Since the conduction loss and output loss for power MOSFET are relatively constant for the given duty cycle and load current, the optimal design of the CSD involves a trade-off between driver loss and switching loss, and there is an optimal inductor current, I_{Lr_OPT}, where P_{SUM} reaches the minimal value as illustrated in [27]. It is noted that it is hard to derive the equations of P_{SUM} with inductor current I_{Lr} as the only variable. Therefore, in this paper, the optimal inductor current where P_{SUM} becomes minimal is obtained in a numerical way – in other words, P_{SUM} are plotted versus different inductor current values I_{Lr}, from which the optimal inductor current I_{Lr_OPT} is approximately obtained. With T_{PRE} fixed to 20ns and

according to (29), it can be inferred that there is also an optimal current source inductor L_{r_OPT}, corresponding to the optimal inductor current I_{Lr_OPT}, as given in (30).

$$L_{r\_OPT} = \frac{V_C \cdot T_{PRE}}{I_{Lr\_OPT}} \tag{30}$$

To validate the analysis, the following conditions are used: V_{IN}=12V, V_O=1.3V, I_O=30A, V_C=5V, F_S=1MHz, *Q:* SI7386DP, drive switches S_1-S_4: FDN335, Anti-diodes D_{S1} ~ D_{S5}: MBR0520. Typically, the parasitic inductance value for Power PAK SO-8 package is tested by the semiconductor manufacturers in [32]-[33] and range from approximately 250pH-1nH. In this model, L_S=1nH and L_D=1nH are used.

Fig. 6 illustrates the plot of the equation P_{SUM} versus the CSD inductor value within practical range using MathCAD. It is noted that, in comparison with the driver loss, the switching loss is the dominant loss of the power MOSFET. It is observed that the optimal current source inductor is around 25nH, where P_{SUM} is the minimum. As is shown in Fig. 7, the peak inductor current at this moment equals 4A.

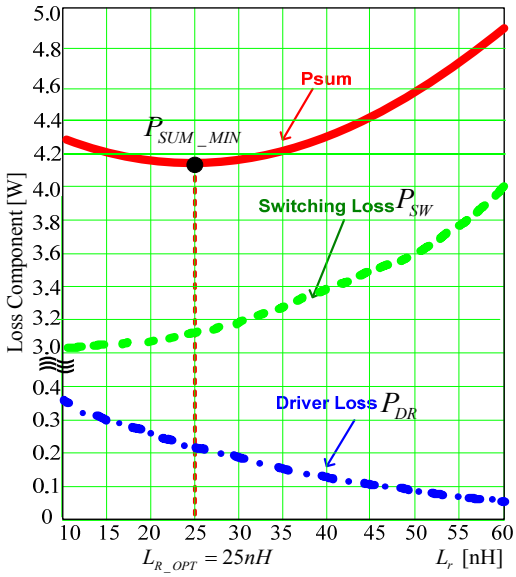


Fig. 6 Total loss versus current source inductor value

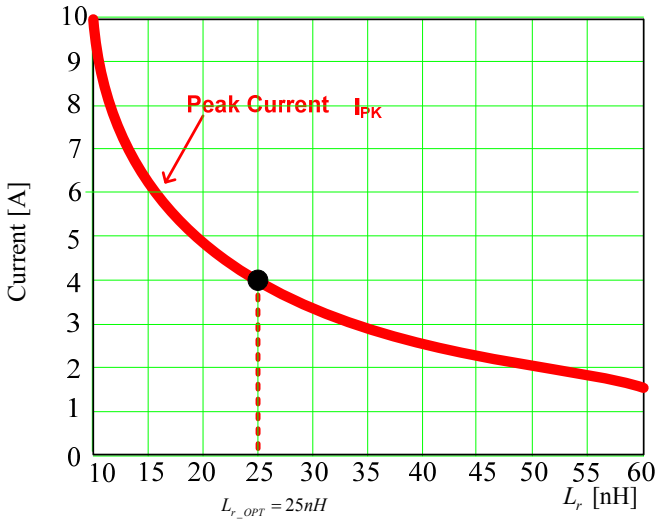


Fig. 7 Peak current versus current source inductor value

IV. Experimental Results And Discussions

A. Hardware Setup

A prototype of a synchronous buck converter as shown in Fig. 8 was built to verify the proposed switching loss model and the optimal design of the current source inductor. The control FET of the converter is driven with the proposed CSD, while the sync FET is driven with a conventional voltage source driver since the switching loss for sync FET is very small.

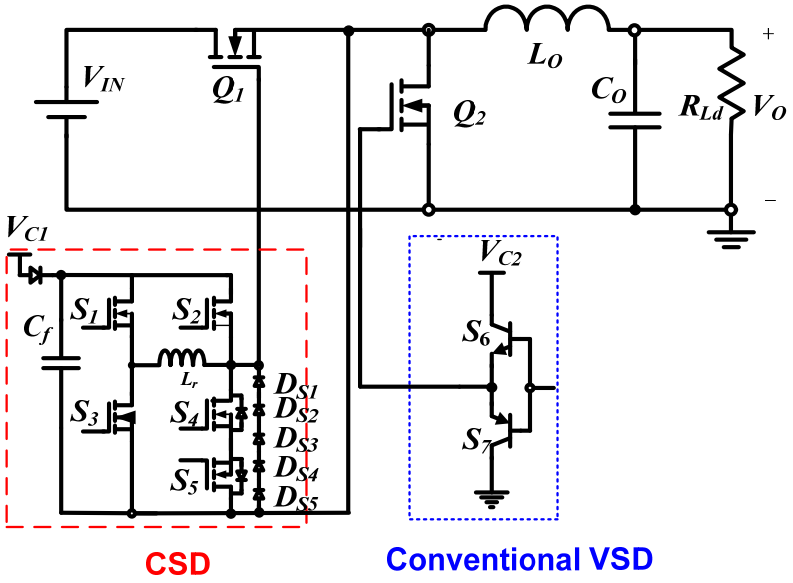


Fig. 8 Synchronous buck converter with proposed CSD

The PCB consists of 6-layer, 4-oz copper, and the photo of the prototype is shown in Fig. 9. The components used are: Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: L_O=330nH (IHLP-5050CE-01); current-source inductor: L_r=23nH (Coilcraft 2508-23N_L); drive switches S_1-S_4: FDN335; Anti-diodes D_{S1}

~ D_{S5}: MBR0520. Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. For common practice, the driver voltages for the control FET and sync FET are both set to be 5V. The operating conditions are: input voltage V_{IN}: 12V; output voltage V_O: 1.2V~1.5V; switching frequency F_S: 500 kHz ~1MHz.

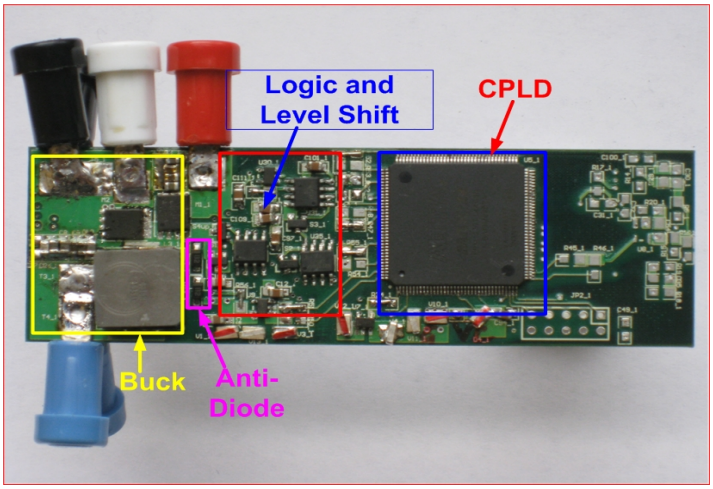


Fig. 9 Photo of the buck converter driven with CSD shown in Fig. 1

The gate driver signals for V_{GS_Q1} and V_{GS_Q2} are shown in Fig. 10. It is observed that during turn-off transition, V_{GS_Q1} is clamped to about -3.5V. It is noted that V_{GS_Q1} is impacted the parasitic from the differential probe, so it is not exactly the same as the waveforms shown in Fig. 3. But it is clearly seen around about -3.5V on V_{GS_Q1}. The current waveform of the CSD inductor is impossible to obtain without breaking the setup of the prototype and therefore, is not provided.

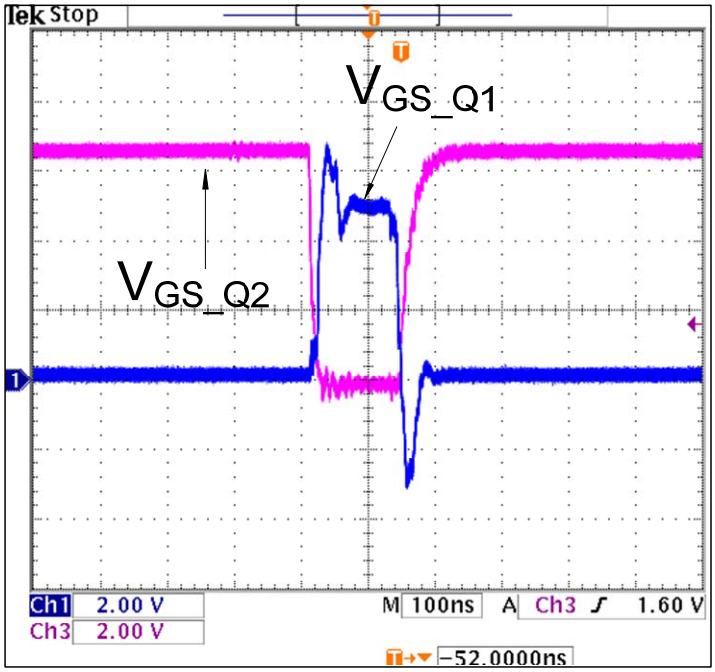


Fig. 10 The waveforms of driver signals V_{GS_Q1} & V_{GS_Q2}

It is noted that the BVdss capability of control FET could be reduced due to the negative gate voltage V_{GS_Q1}. However, designers normally obey an 80% margin rule [34], which means that the maximum voltage stress measured across any MOSFET must not exceed 80% of the MOSFET's BVDSS. This requires both good layout design and reasonable selection of the MOSFET based on the application conditions [35]. The switching node waveform for synchronous buck converter at 12Vin, 1.2Vout and 30A is shown in Fig. 11. It is observed that the voltage stress for sync FET is 18V while the voltage stress for control FET is 15V, therefore, it still meets the requirements for the 80% margin in this design.

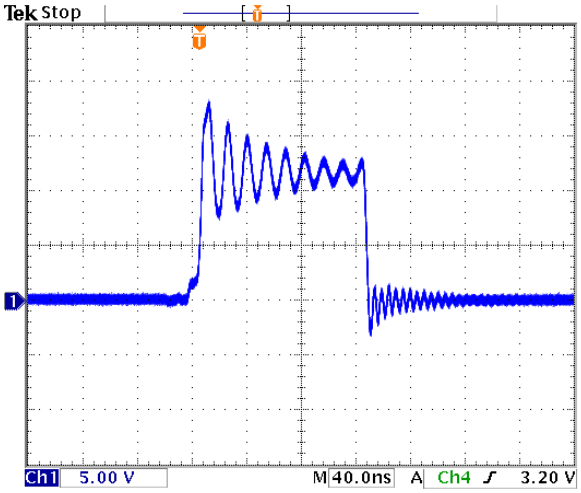


Fig. 11 The switching node waveform of the synchronous buck converter at 12Vin, 1.2Vout and 30A

Fig. 12 to Fig. 14 illustrate the measured efficiencies comparison with 12Vin/1.2Vout at 500kHz, 750kHz and 1MHz between the optimized bipolar CSD and VSD, which is implemented with Intersil synchronous buck gate driver ISL6613. It is observed that the optimized bipolar CSD has achieved better performance than the VSD at all conditions. The efficiency improvement achieved by the bipolar CSD at 30A load is 1.4% at 500 kHz and 2.5% at 1MHz. That is because that the bipolar CSD, compared with VSD, achieves much lower the switching loss, which is proportional to the switching frequency.

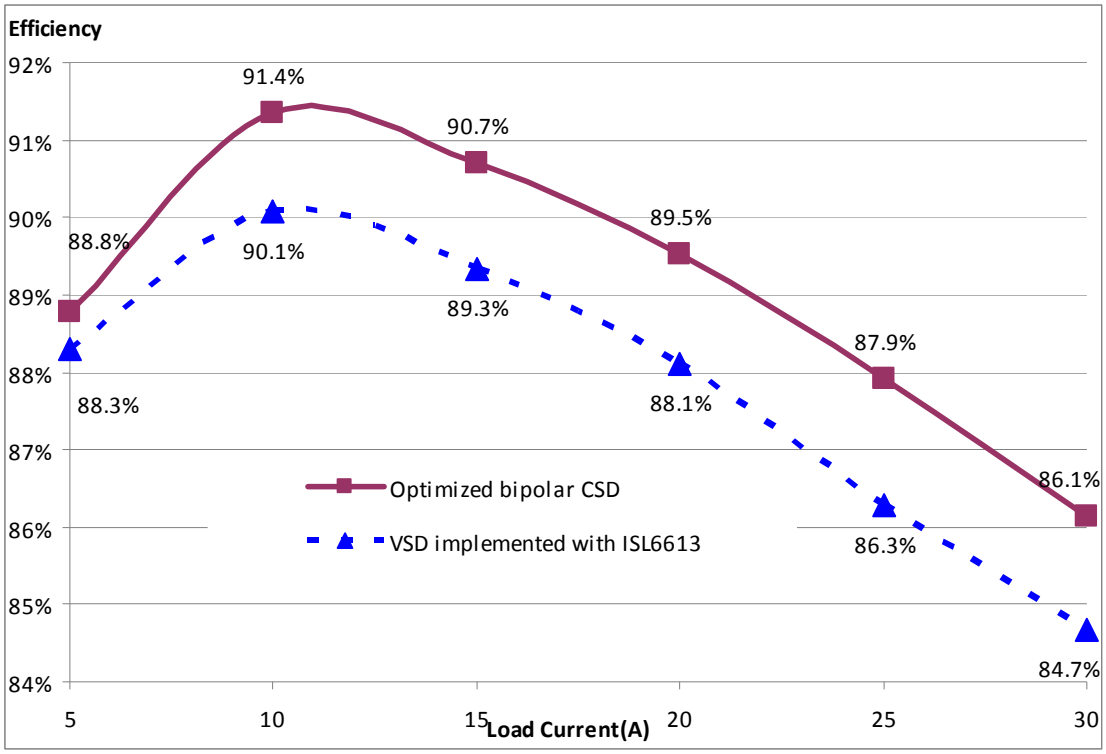


Fig. 12 Measured efficiency comparison between the bipolar CSD and VSD for 12Vin, 1.2Vout @500kHz

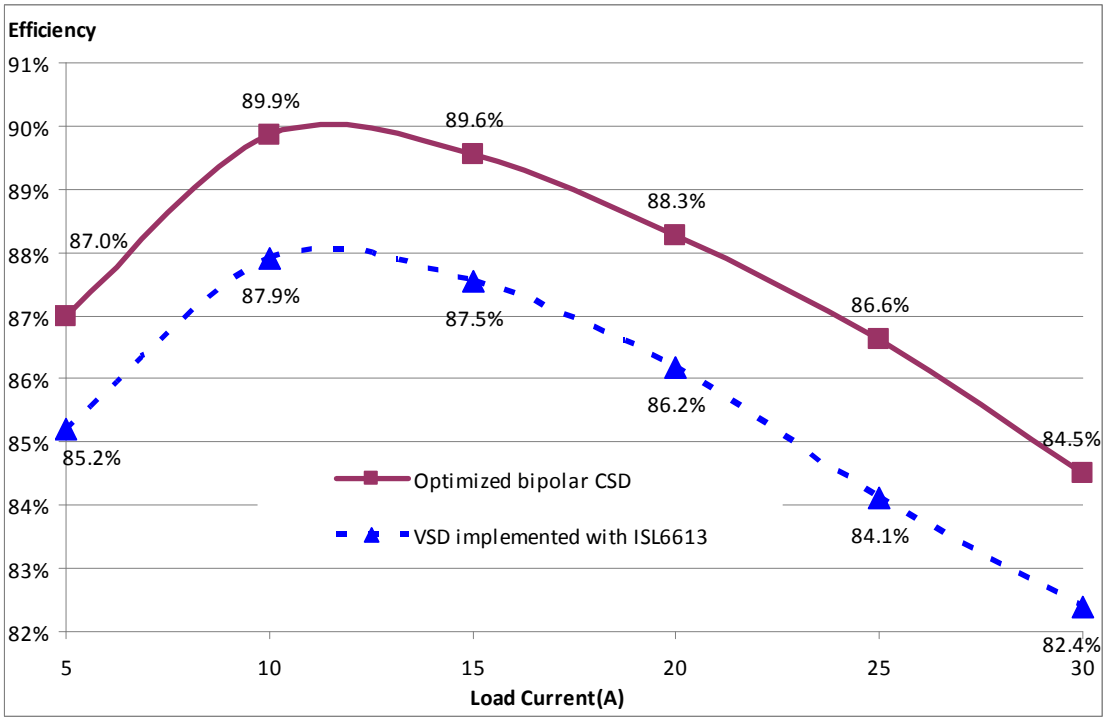


Fig. 13 Measured efficiency comparison between the bipolar CSD and VSD for 12Vin, 1.2Vout @750kHz

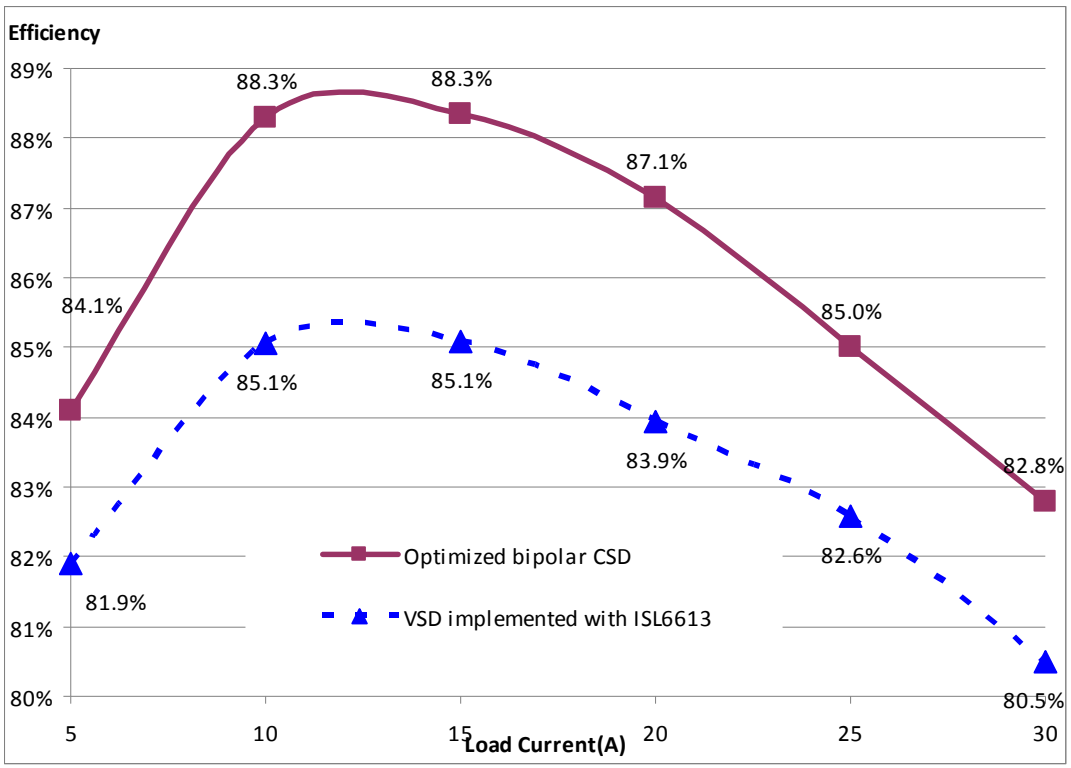


Fig. 14 Measured efficiency comparison between the bipolar CSD and VSD for 12Vin, 1.2Vout @1MHz

B. Verification and Discussions of the Proposed Switching Loss Model

1. *Verification of the Proposed Switching Loss Model*

In addition to the loss for control FET illustrated in section II, the loss of the buck converter in Fig. 8 also includes the following major losses:

1) Loss for output inductor

Under continuous current mode, there is always current flowing through the output inductor. Therefore, the parasitic resistance of the output inductor, often called DCR, introduces conduction loss. The accurate calculation of this portion of loss should consider the ripple of the inductor current as shown in Fig. 15.

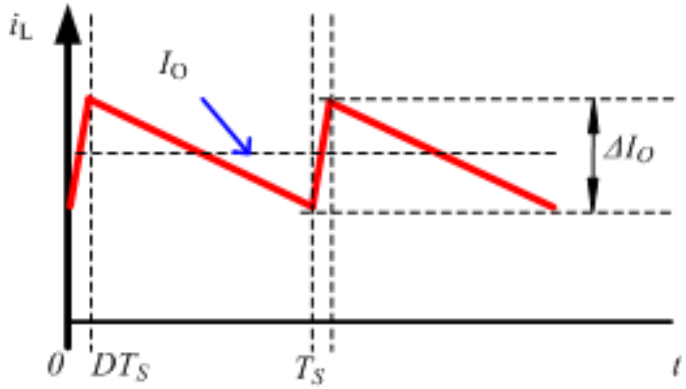


Fig. 15 Total loss versus. current source inductor

Assuming there is no iron loss in the inductor, the RMS of the inductor current, I_{L_RMS} is calculated in (31) [29]. And the conduction loss for inductor is calculated in (32), where I_O is the load current of the buck converter, V_O is the output voltage, V_{IN} is the input voltage, T_S is the switching cycle, L_O is the value of the output inductor and DCR is the parasitic resistance of the output inductor.

$$I_{L\_RMS}=\sqrt{\frac{\int_0^{DT_s} i_{IN}^2 dt+\int_{DT_s}^{T_s} i_{IN}^2 dt}{T_S}}\approx\sqrt{I_O{}^2+\frac{\triangle I_O{}^2}{12}}\approx\sqrt{I_O{}^2+\frac{V_O{}^2(V_{IN}-V_O)^2T_S{}^2}{12L_O{}^2V_{IN}{}^2}} \tag{31}$$

$$P_L=I_{L\_RMS}{}^2\cdot DCR=[I_O{}^2+\frac{V_O{}^2(V_{IN}-V_O)^2T_S{}^2}{12L_O{}^2V_{IN}{}^2}]\cdot DCR \tag{32}$$

2) Loss for sync FET of the buck converter

The loss for sync FET consists of conduction loss, gate driver loss, reverse recovery loss and switching loss.

The energy supplied by the source to drive the sync FET is totally dissipated into heat during turn-on and turn-off transition. Therefore, the gate driver loss P_{DR_SR} is given in (33), where Q_{G_SR} is the total gate charge for sync FET, V_{C_SR} is the gate drive voltage for sync FET and F_S is the switching frequency.

$$P_{DR\_SR}=Q_{G\_SR}\cdot V_{C\_SR}\cdot F_S \tag{33}$$

Conduction loss P_{COND_SR} is calculated in (34), where I_{SR_RMS} is the RMS current of the sync FET, $R_{DS(ON)\_SR}$ is the on-resistance of the sync FET, T_{ON_SR} is the on-time of the sync FET , T_{ON} is the on-time for Ctrl FET, and T_S is the switching cycle.

$$P_{COND\_SR}=I_{SR\_RMS}{}^2\cdot R_{DS(ON)\_SR}\cdot\frac{T_S-T_{ON}}{T_S} \tag{34}$$

The body diode of sync FET contributes to reverse recovery loss due to the characteristic of P-i-N diode; also the reverse recovery charge Q_{RR_SR} is highly dependent on the di/dt rate and forward current in the diode. In this paper, Q_{RR_SR} is obtained from datasheet for approximation. Reverse recovery loss for sync FET P_{QRR_SR} is calculated in (35), where V_{IN} is the drain-to-source voltage across the sync FET when it is off.

$$P_{QRR\_SR}=V_{IN}\cdot Q_{RR\_SR}\cdot F_S \tag{35}$$

The output loss for sync FET P_{OUT_SR} is calculated in (36), where Q_{OSS_SR} is the charge for the output capacitance of the sync FET.

$$P_{OUT\_SR}=\frac{V_{IN}\cdot Q_{OSS\_SR}\cdot F_S}{2} \tag{36}$$

The switching loss of the sync FET P_{SW_SR} is made up of the turn-on loss $P_{SW(ON)\_SR}$ and turn-off loss $P_{SW(OFF)\_SR}$ of sync FET, as shown in (37).

$$P_{SW\_SR} = P_{SW(ON)\_SR} + P_{SW(OFF)\_SR} \tag{37}$$

The turn-on loss and turn-off loss for sync FET equals the energy supplied by the source as there are no energy transfer on the output capacitance during turn-on and turn-off transitions. The equations for $P_{SW(ON)\_SR}$ and $P_{SW(OFF)\_SR}$ are shown in (38) and (39) proposed in [36], where V_{TH_SR} is the gate threshold voltage of the sync FET, g_{FS_SR} is the transconductance of the sync FET, R_{DR_SR} is the on-resistance of the driver, R_{G_SR} is the gate resistance of the sync FET, C_{ISS_SR} is the input capacitance of the sync FET, V_{F_SR} is the body diode forward voltage of sync FET, V_{SPE_SR} is the specified gate voltage of the sync FET according to the datasheet, $R_{DS(ON)\_SR}$ is the on-resistance of the sync FET when gate drive voltage equals V_{SPE_SR}.

$$\begin{aligned} P_{SW(ON)\_SR} = & \ln\frac{V_{C\_SR} - V_{TH\_SR}}{V_{C\_SR} - V_{TH\_SR} - I_O/g_{FS\_SR}} \cdot (R_{DR\_SR} + R_{G\_SR}) \cdot C_{ISS\_SR} \cdot V_{F\_SR} \\ & + \ln\frac{V_{C\_SR} - V_{TH\_SR} - I_O/g_{FS\_SR}}{V_{C\_SR} - 0.9 \cdot V_{SPE\_SR}} \cdot \frac{V_{F\_SR} + I_O \cdot 1.1 \cdot R_{DR\_SR}}{2} \cdot I_O \cdot F_S \end{aligned} \tag{38}$$

$$\begin{aligned} P_{SW(OFF)\_SR} = & \ln\frac{V_{TH\_SR} + I_O/g_{FS\_SR}}{V_{TH\_SR}} \cdot (R_{DR(ON)\_SR} + R_{G\_SR}) \cdot C_{ISS\_SR} \cdot V_{F\_SR} \\ & + \ln\frac{0.9 \cdot V_{SPE\_SR}}{V_{TH\_SR} + I_O/g_{FS\_SR}} \cdot \frac{V_{F\_SR} + I_O \cdot 1.1 \cdot R_{DR(ON)\_SR}}{2} \cdot I_O \cdot F_S \end{aligned} \tag{39}$$

3) Comparison between the calculated and simulated switching loss

The new model proposed in this paper is mainly the switching loss model for control FET that is driven by CSD. In order to verify the switching loss model, simulation for the switching loss model for control FET is conducted using pspice model with Ltspice from Linear Technology [37]. The comparison between the calculated and simulated switching loss for control FET is shown in Fig. 16. It is observed that the calculated loss model is very close to the simulation results using pspice model.

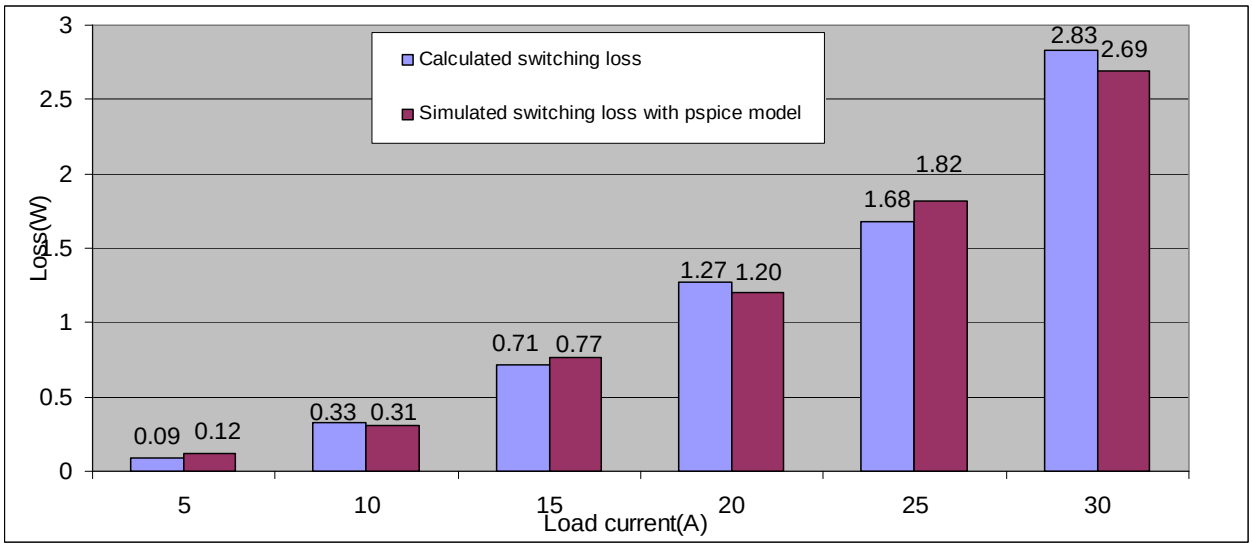


Fig. 16 Comparison between calculated switching and simulated switching loss for control FET

4) Comparison between the calculated total loss and experimentally measured loss

In order to validate the accuracy of the proposed switching loss model, the calculated total loss of the synchronous buck converter as a function of load current is compared to the experimentally measured loss in Fig. 17. The parameters for the modeling are extracted from the components used in experimental prototype in Fig. 9. It is observed that the calculated loss by the loss model proposed in this paper matches the actual loss of the synchronous buck converter very well. The difference between the calculated loss and experimentally measured loss is less than 10% across all load levels from 5A to 30A.

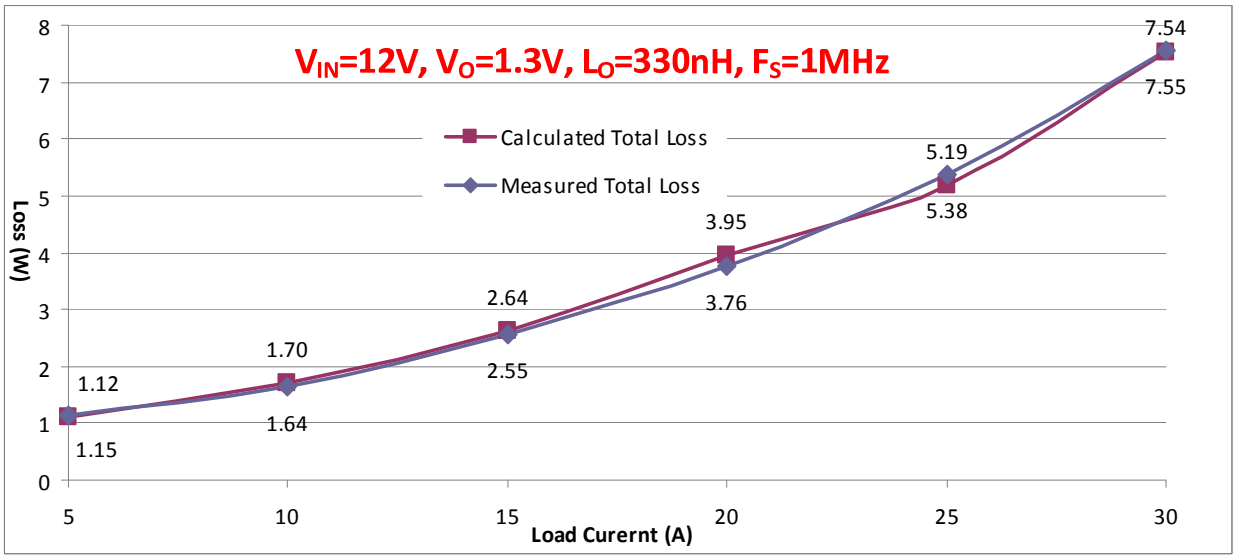


Fig. 17 Comparison between measured loss and calculated loss

2. Loss Breakdown of the Synchronous Buck Converter

The loss breakdown of the calculated loss of the synchronous buck converter is illustrated in Fig. 18. It is observed that for control FET of the synchronous buck converter, switching loss is the dominant loss, taking

up 2.83W out of the 7.54W of total loss (37%); while for SYNC FET, the conduction loss is the dominant loss which is taking up 20% of the total loss.

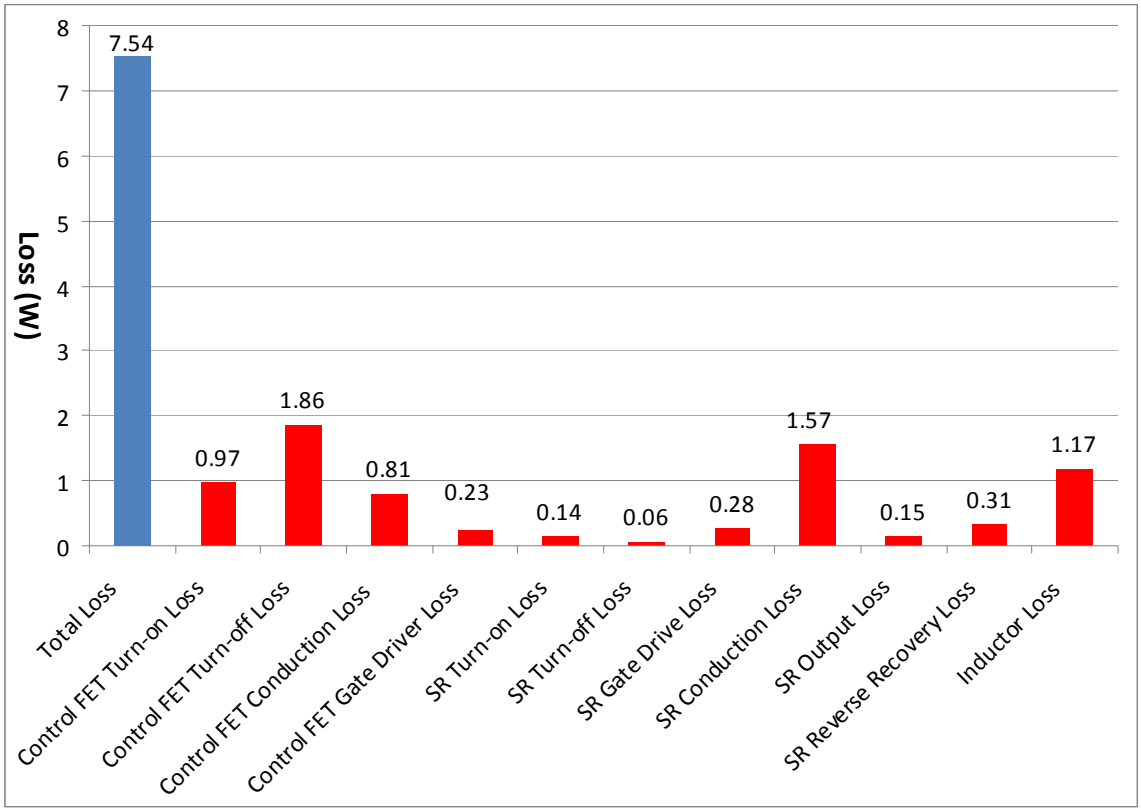


Fig. 18 Calculated loss breakdown of the synchronous buck converter

3. Switching Loss of Control FET Vs. Load Current

The calculated switching loss of the control FET is plotted as a function of the load current in Fig. 19 to study their relationship. First order linear fitting and second order linear fitting are made, respectively, to the points obtained from the proposed switching loss model [38]. It is observed that the coefficient of determination, R^2, for second order polynomial fitting is 0.99, which is larger than the R^2 for first order polynomial fitting (0.83). Since the larger R^2 is, the better the fitting represents the data, so it is inferred that second order linear fitting matches the calculated switching loss points for control FET better. In other words, the switching loss for control FET almost increases proportionally to I_O^2.

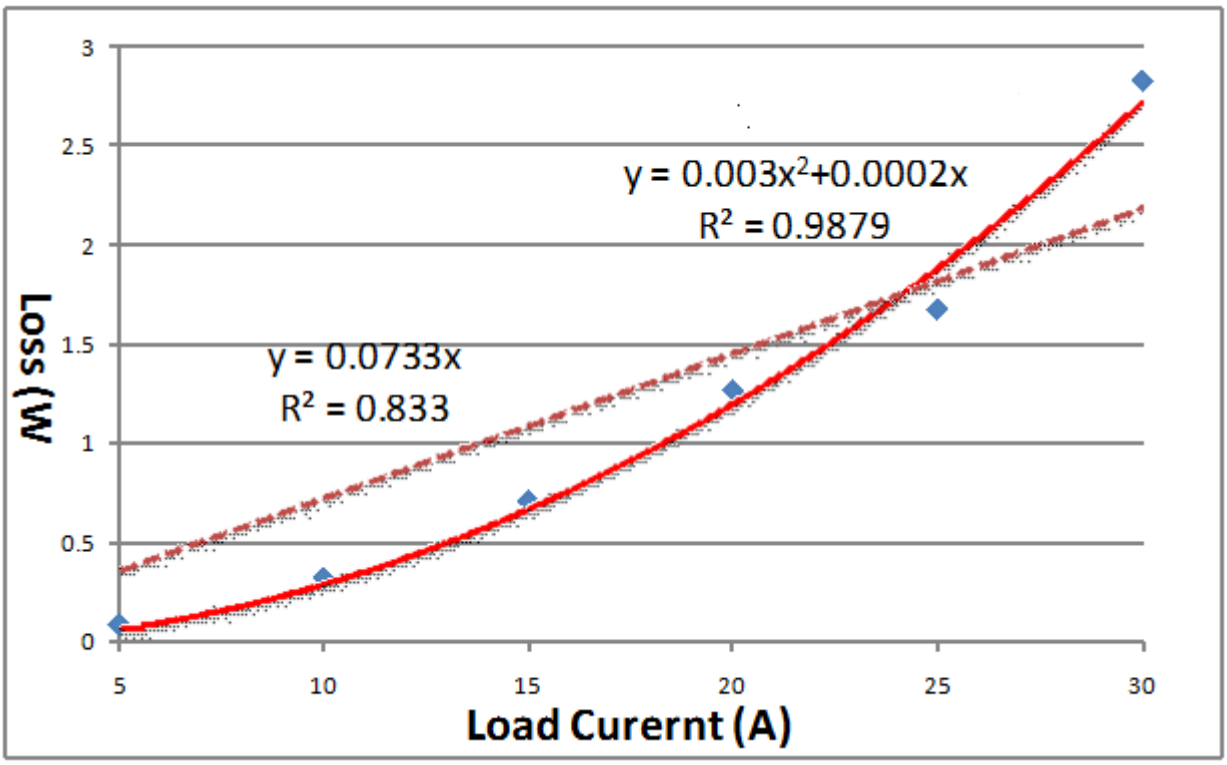


Fig. 19 Polynomial fittings of the switching loss for control FET

The physics behind the quadratic relationship between the switching loss of control FET and load current is the gate-to-source voltage clamping due to the gate current diversion during drain current rising and drain current drop intervals, as analyzed in section II. The equivalent switching circuits in these two intervals are shown in Fig. 20.

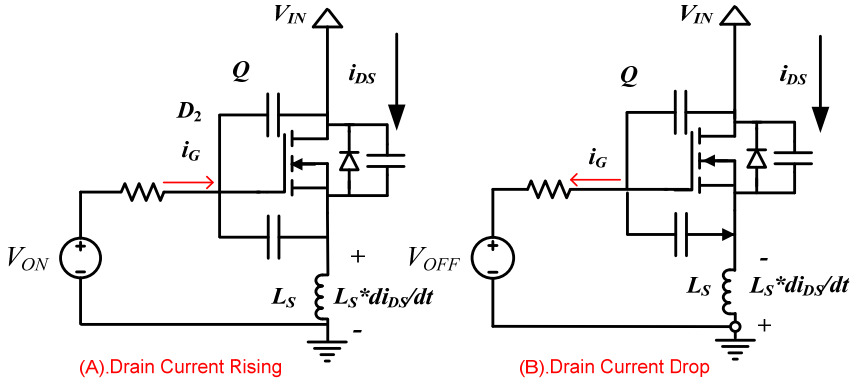


Fig. 20 Equivalent switching circuits when drain current rises and drops

The KVL equation for drain current rising is given in (40), while the equation for drain current drops is given in (41), where T_R is the current rising time and T_F is the current falling time, V_{ON} and V_{OFF} is the clamped gate-to-source voltage due to the gate current diversion during drain current rises or drops.

$$L_S \frac{d}{dt}(i_{DS}) \simeq L_S \frac{\Delta i_{DS}}{\Delta t} = L_S \frac{I_O}{T_R} \simeq V_{ON} - i_G R_G - V_{CGS} \tag{40}$$

$$L_S \frac{d}{dt}(i_{DS}) \simeq L_S \frac{\Delta i_{DS}}{\Delta t} = L_S \frac{I_O}{T_F} \simeq -i_G R_G + V_{CGS} - V_{OFF} \tag{41}$$

It is inferred, from (40) and (41), that both T_R and T_F are proportional to load current I_O. Therefore, the switching loss of control FET, P_{SW} as approximated in (42) is almost proportional to I_O^2.

$$\begin{aligned} P_{SW} &= P_{SW\_ON} + P_{SW\_OFF} \simeq \frac{V_{DS\_RISING} \cdot I_O \cdot T_R}{2} + \frac{V_{DS\_DROP} \cdot I_O \cdot T_F}{2} \\ &\simeq \frac{1}{2} \cdot \left(\frac{V_{DS\_RISING} \cdot L_S}{V_{ON} - i_G R_G - V_{CGS}} + \frac{V_{DS\_DROP} \cdot L_S}{-i_G R_G + V_{CGS} - V_{OFF}} \right) I_O^{\,2} \end{aligned} \tag{42}$$

4. Comparison of the Calculated Loss Among Proposed CSD, Existing CSD and VSD

It is observed from (42) that during drain current drop interval, the clamped gate-to-source voltage, V_{OFF} affects the turn-off loss to a great extent. The more negative V_{OFF} is, the smaller the turn-off loss is introduced. The V_{OFF} for proposed CSD in Fig. 1 is -3.5V,and V_{OFF} for existing CSD in [21] is -0.7V, while for conventional VSD, V_{OFF} is roughly +0.5V. Therefore, the proposed CSD in Fig. 1 is supposed to have smaller switching loss than existing CSD in [21]; both CSDs introduce smaller switching loss than conventional VSD. The calculated loss comparison among the proposed CSD in Fig. 1, existing CSD in [21] and conventional VSD is shown in Fig. 21. It is verified that the proposed CSD in Fig. 1 has the smallest total loss due to the negative gate-to-source voltage during turn-off transition. Therefore, although CSD has higher cost than the VSD, the significant performance improvement makes it a good choice for high-end applications such as servers where the performance has been limited by the figure of merits of the current semiconductor technology.

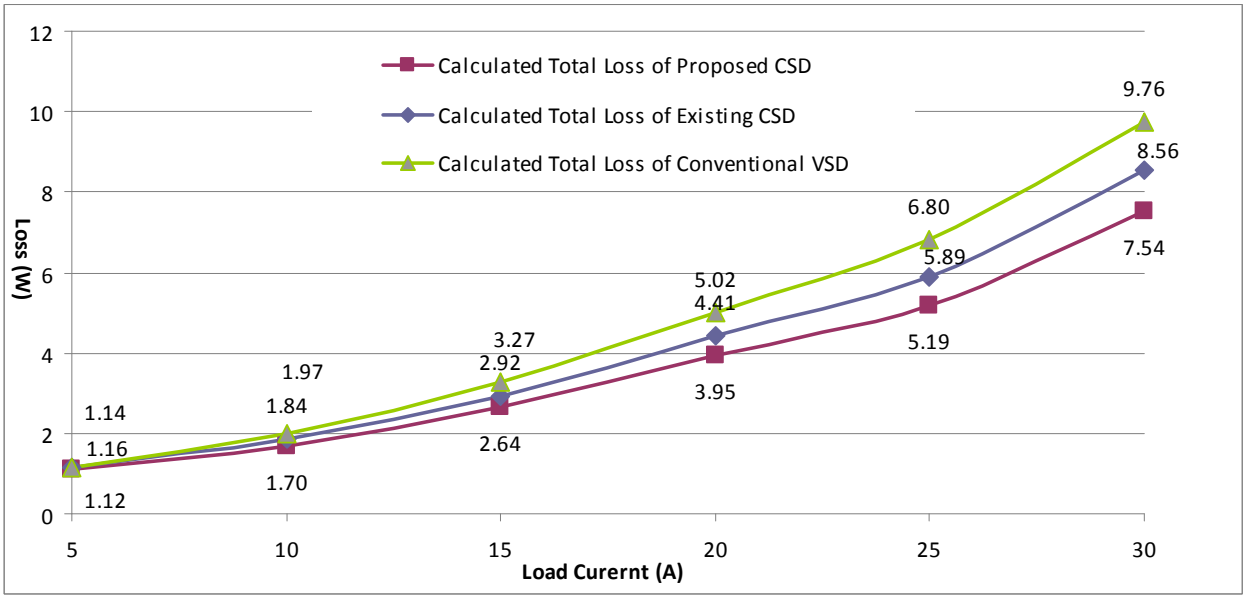


Fig. 21 Calculated loss comparison between proposed CSD (Fig. 1), existing CSD [21] and VSD

C. Verification of the Optimal Design of the CSD Inductor

To validate the optimal design of the CSD inductor, an apple-to-apple comparison between the synchronous buck converters with a 25nH and a 43nH CSD inductor is made. Fig. 22 illustrates the efficiency comparison for two prototypes at 1.3V/1MHz output. It is noted that, comparing to the CSD with 43nH, the CSD with the optimal CSD inductor increases the efficiency at all load currents, improving from 86.1% to 87.6% by 1.5% at 20A load, and from 82.4% to 84.0% by 1.6% at 30A load.

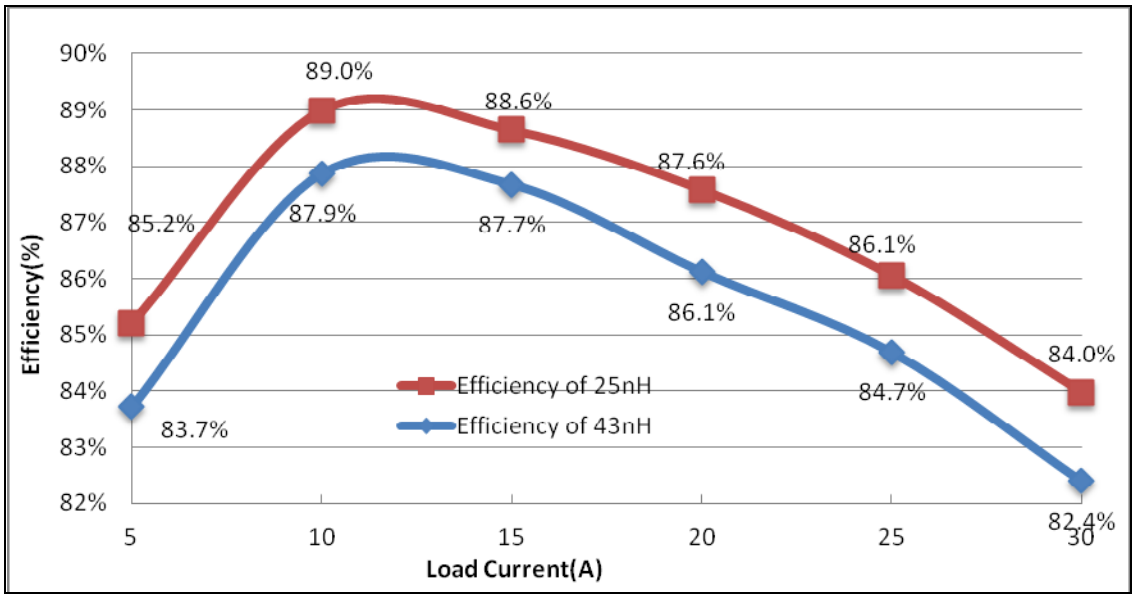


Fig. 22 Measured efficiency comparison for different CSD inductors at 12V input, 1.3V output, 1MHz

D. Comparison between CSD and Commercial Products

The integrated Driver-MOSFET (DrMOS) provides the optimal solution for multiphase synchronous buck converter for its high power density and reduced design time. Compared with commercially available DrMOS solutions, the synchronous buck converter driven with the optimized proposed CSD can achieve better performance.

Fig. 23 illustrates the loss comparison between optimized CSD and DrMOS from Renesas [39]. It is noted that optimized CSD has smaller loss across all load levels (5A~30A load) and at 30A/1.3V load in 500kHz switching frequency, the optimized CSD can save nearly half Watt loss (0.46W). In addition, from the standpoint of the thermal performance, the optimized CSD is better than DrMOS, since the dimension of typical DrMOS is 8 mm by 8 mm by 0.95 mm – in such a small package, even for the same amount of loss, the DrMOS has higher temperature than the optimized CSD.

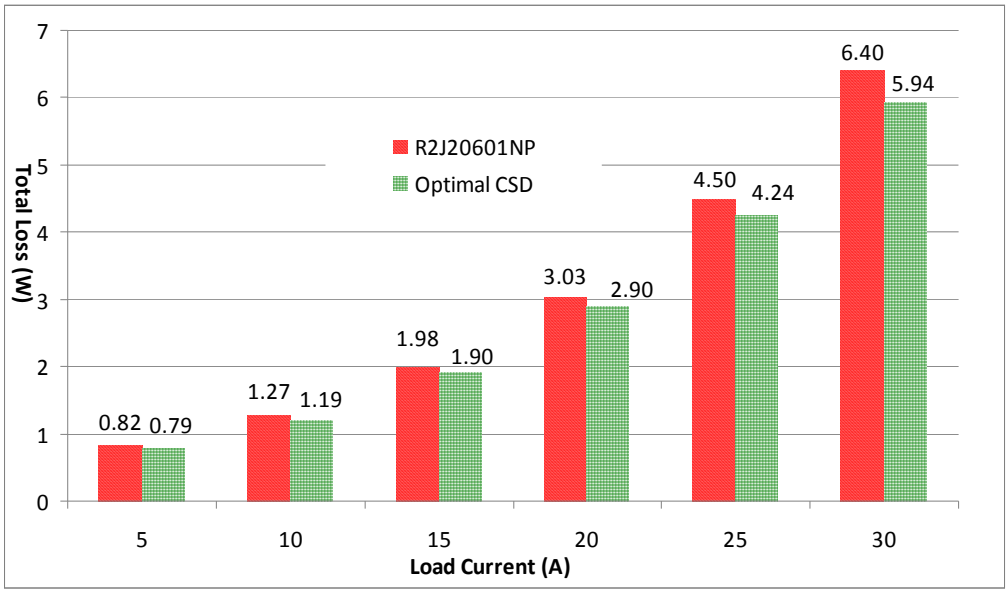


Fig. 23 Comparison between optimized CSD and DrMOS from Renesas

While the loss comparison between optimized CSD and DrMOS-IP2005 [40] from International Rectifier is shown in Fig. 24, from which it is observed that optimized CSD can save nearly a quarter Watt (0.24W) at 1.3V/30A load and 1MHz switching frequency.

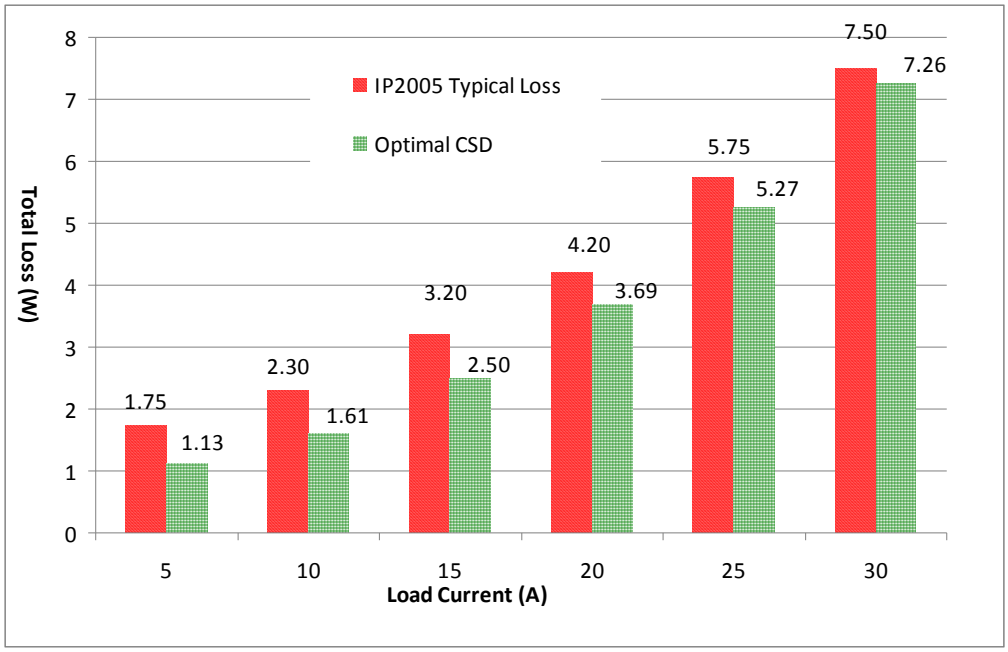


Fig. 24 Comparison between optimized CSD and DrMOS from IR

V. CONCLUSIONS

In this paper, a new accurate switching loss model considering the current diversion is presented for the power MOSFET driven by a CSD, and the analytical equations for each interval to predict the switching loss are derived. Based on the proposed model, the optimal current source inductor is obtained to achieve the maximum overall efficiency of the synchronous buck converter. The experimental results verify the proposed switching loss model. The variation between the calculated loss and the experimentally measured loss is within 0.2W from 5A load to 30A load. The modeling shows that switching loss of the control FET is nearly proportional to the square of load current because of the impact of the common source inductance and the voltage clamping due to the body diode conduction. The optimal design of the CSD inductor is also validated by the experimental results. Compared with the previous work, the CSD with the optimal inductor improves the efficiency by 1.6% at 1.3V output 30A load in 1MHz switching frequency. The buck converter with the optimized CSD shows better performance than DrMOSs from Renesas and International Rectifier.

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