A Quick Capacitor Charge Balance Control Method to Achieve Optimal Dynamic Response for Buck Converters

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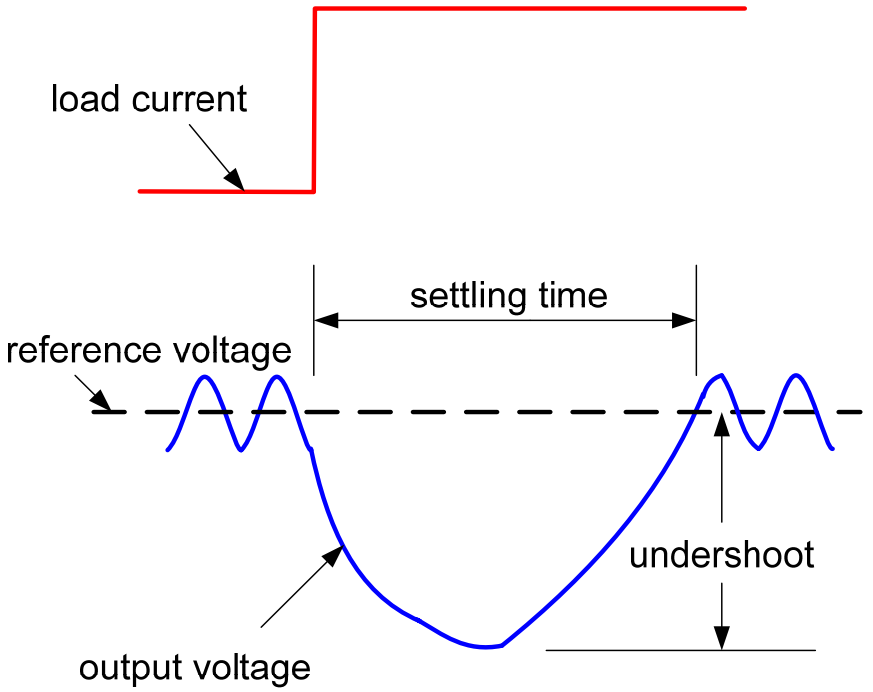
***Presenting Author**

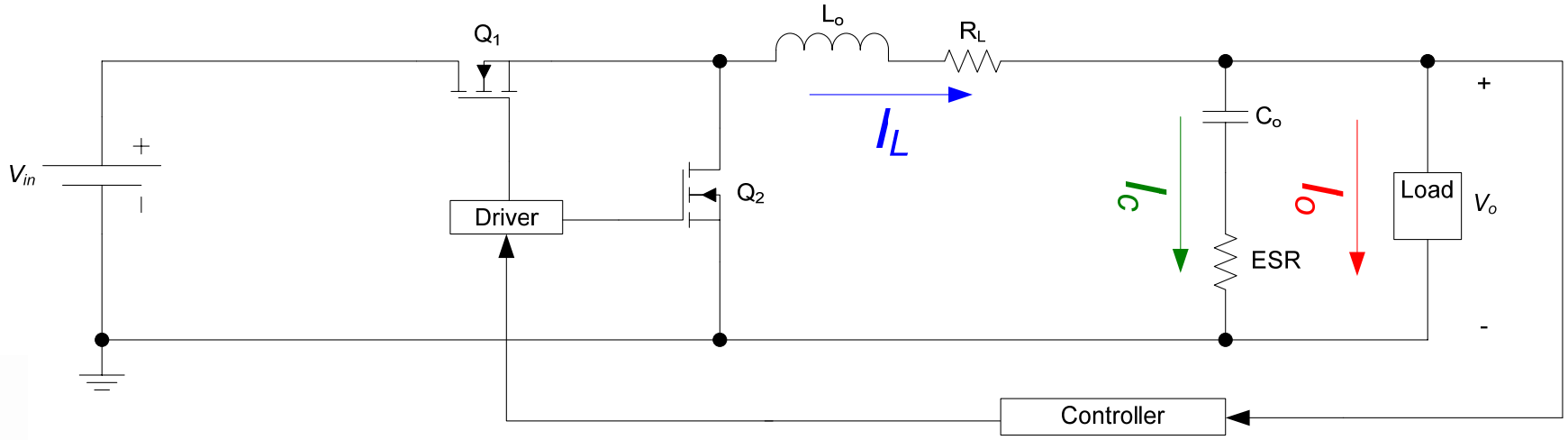
Presentation Outline

- Introduction / Controller Concept
- Controller Derivation
- Controller Operation
- Theoretical Results
- Simulation Results
- Experimental Results
- Conclusion

Buck Converter Under Load Transient

- VRMs undergo rapid, large load variations
- Capacitor must absorb/provide portion of load current
  - Voltage deviates from reference for finite time
- **Goal: Minimize effect of load current transient**





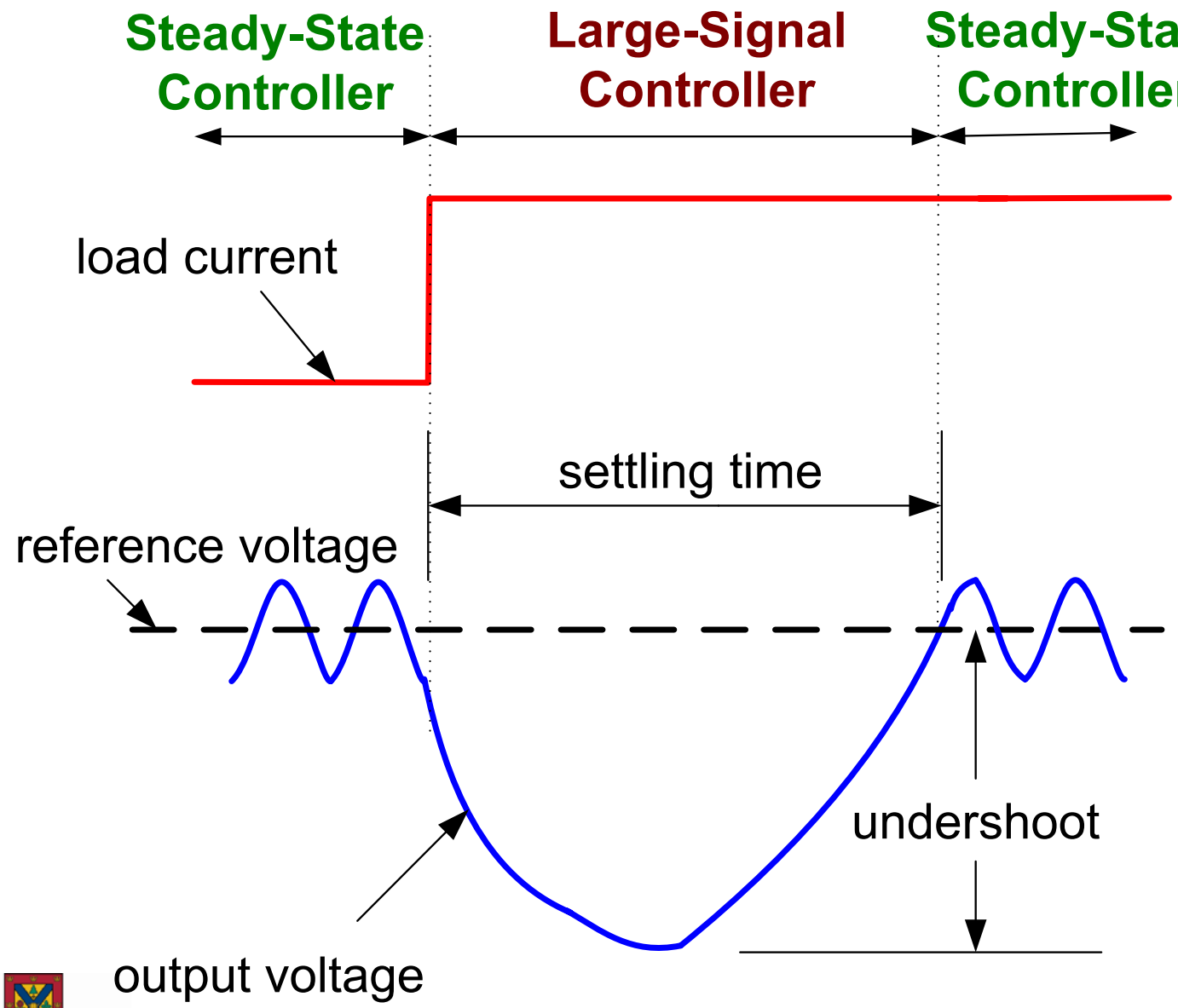
Conventional Controller

- **Designed using frequency-domain small-signal model**

  Goals:

  - **Zero-steady state error**
  - **Widest bandwidth with sufficient phase margin**

Alternative Linear/Non-Linear Control

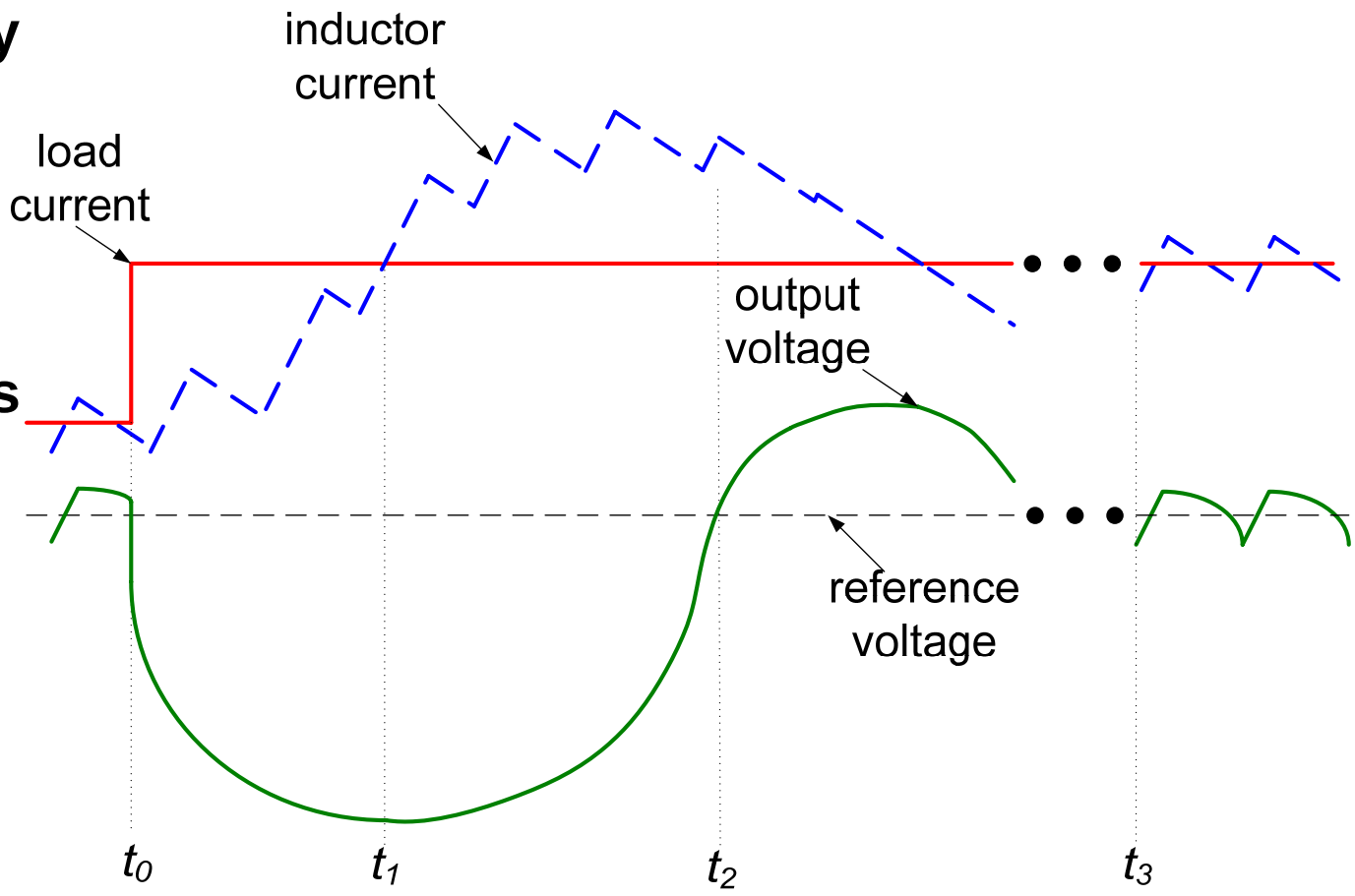


Improved dynamic response achievable

Conventional Response to Positive Load Current Step

- t_0: Load current step
  - Controller slowly begins to increase duty cycle
- t_1: Inductor current equals load current
  - Capacitor begins recharging
- t_2: Output voltage recovered
  - Inductor current > Load current
- t_3: Converter "recovered"

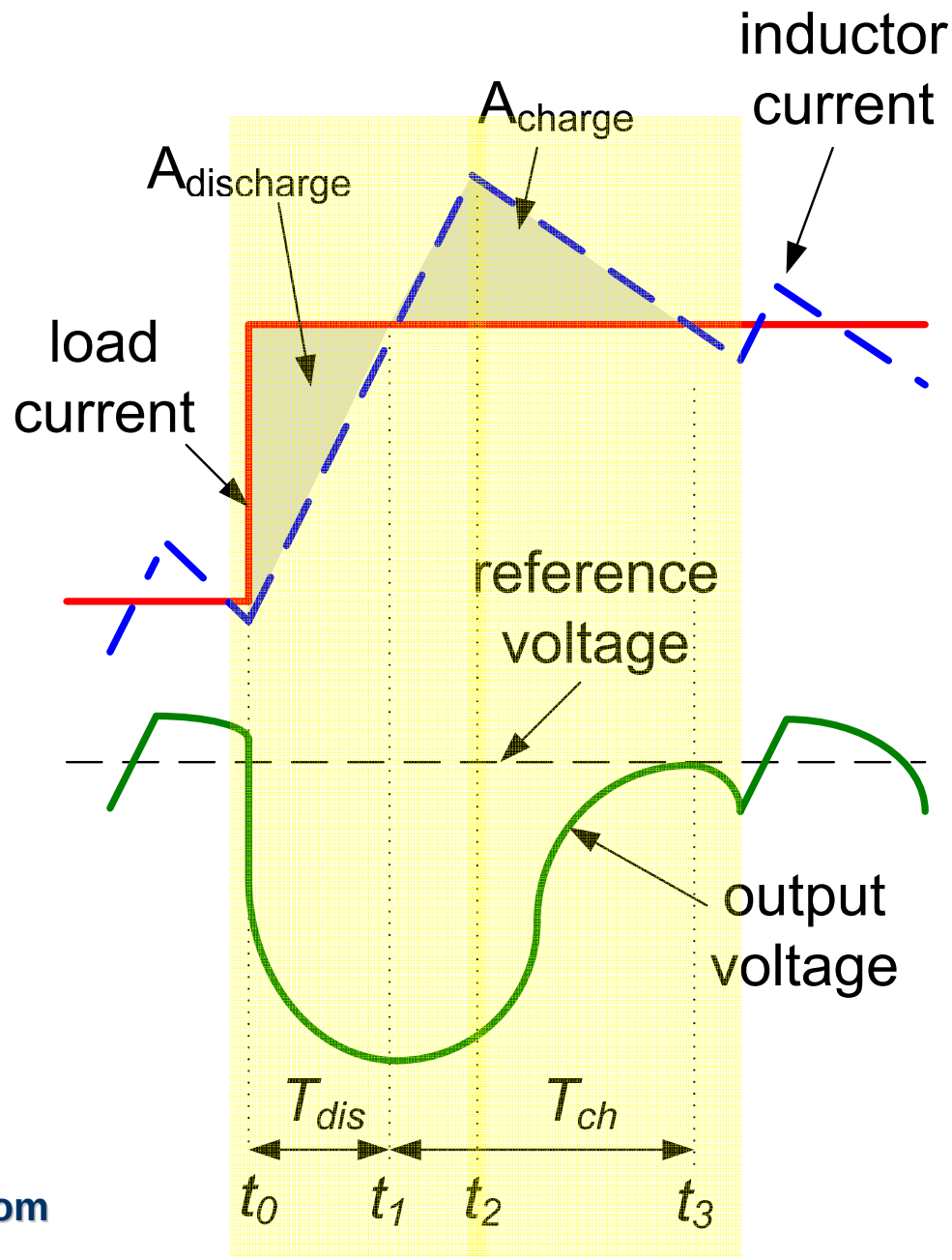
How can we improve this response?



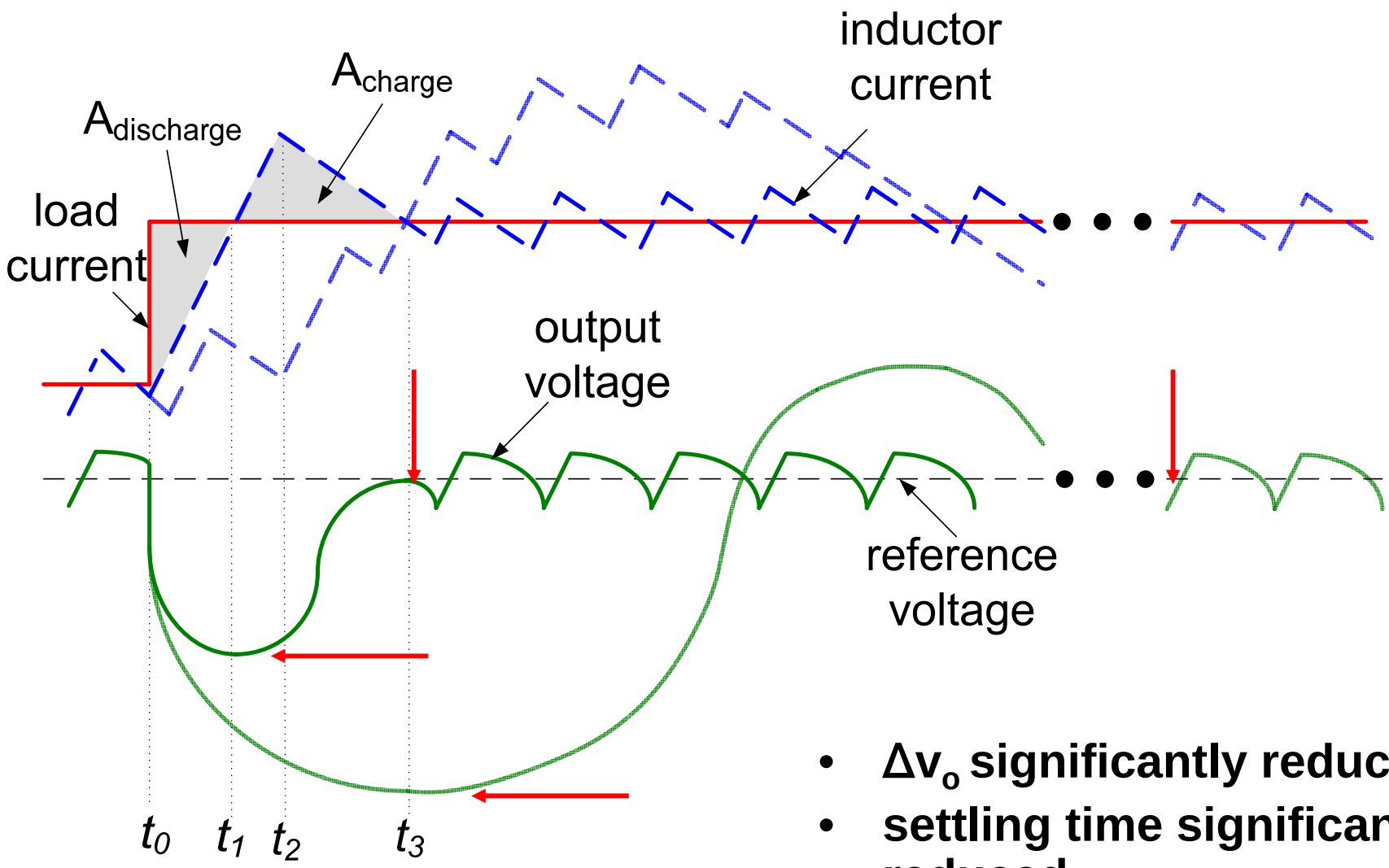
Conventional Control Method

Charge Balanced Response to Positive Load Current Step

- **Set duty cycle to 100% immediately**
  - **Inductor current increases at fastest slew rate**
  - **Minimizes T_{dis}**
  - **Minimizes $A_{discharge}$**
  - **Minimizes Δv_o**
- **Set duty cycle to 0% at t_2 such that $A_{charge} = A_{discharge}$**
  - **Minimizes T_{ch}**
  - **Minimizes settling time**



Comparison with Traditional Controller



- **Δv_o significantly reduced**
- **settling time significantly reduced**

Quick Capacitor Charge Balance Control Method vs. Previous Work[1]

- **Inductor information not required**
  - **Increased accuracy**
- **Only simple analog functions (integration) performed**
  - **Only OpAmps, comparators, multiplexers required**
- **No sampling delay**
  - **Immediate reaction to transient**
  - **Minimum voltage deviation/settling time**

[1] G. Feng, W. Eberle, Y-F. Liu, “A New Digital Control Algorithm to Achieve Optimal Dynamic Response in DC-to-DC Converters”, IEEE 36th Power Electronics Specialists Conference (PESC 05), pp. 2744 - 2749

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Controller Derivation

Goal: $A_{discharge} - A_{charge} = 0$

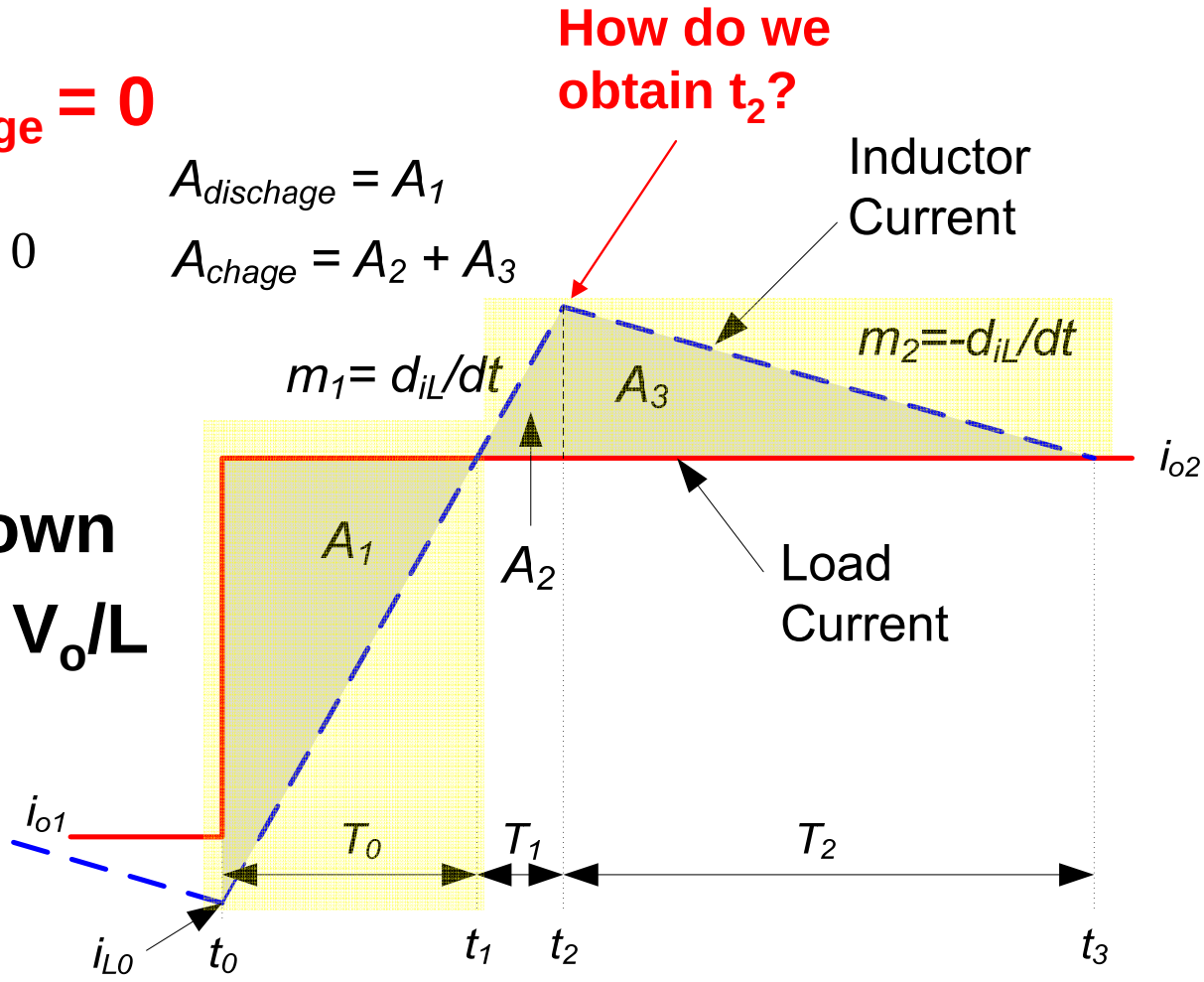
$$\iint_{T0} m_1 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2} (dt)^2 = 0$$

Slopes m_1 and m_2 known

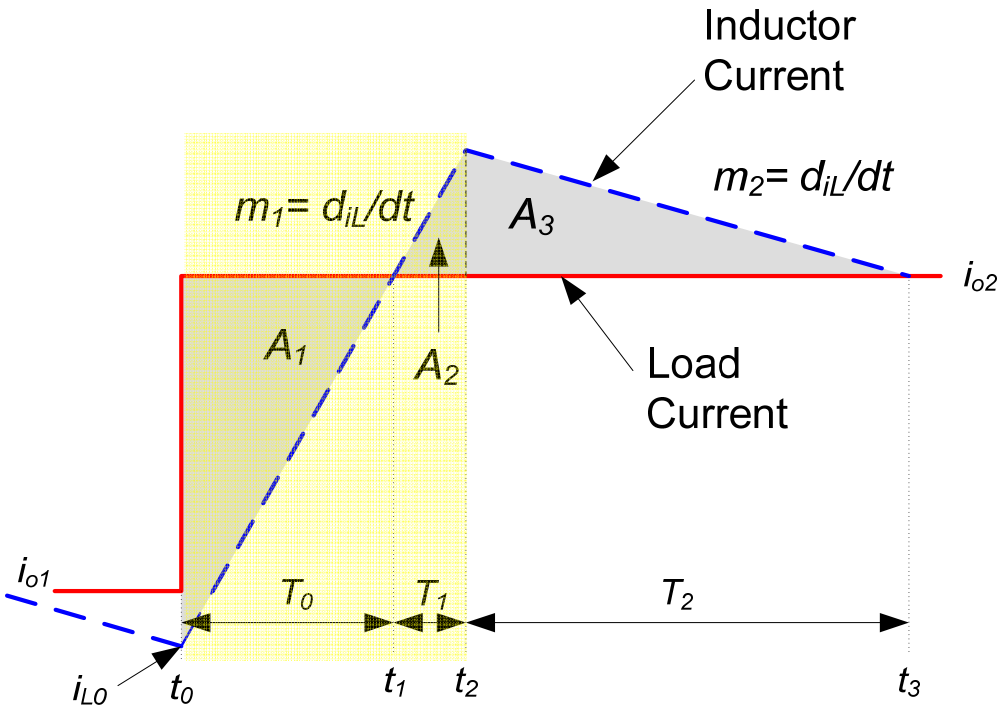
$m_1 = (V_{in} - V_o)/L$, $m_2 = V_o/L$

$$A_{discharge} - A_{charge} = 0$$

$$V_o \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 = 0$$

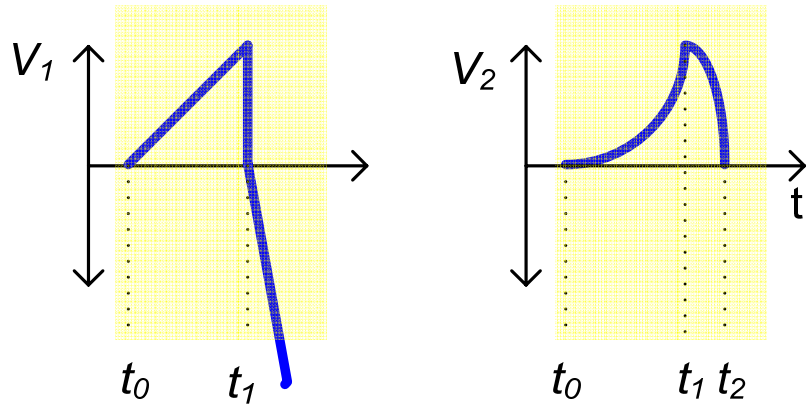


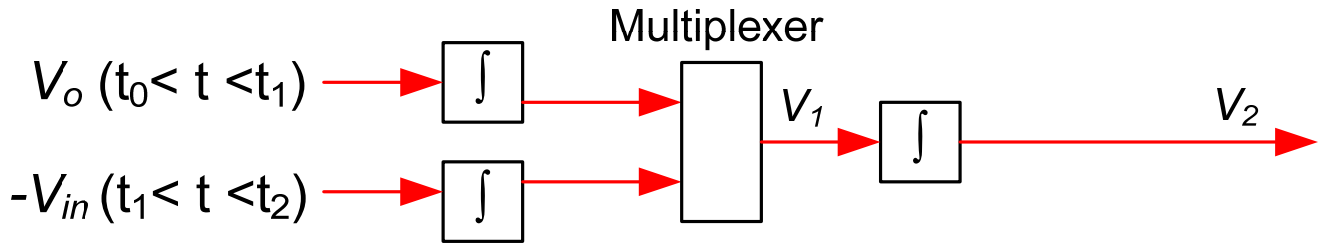
How to Solve t_2



$$A_{discharge} - A_{charge} = 0$$

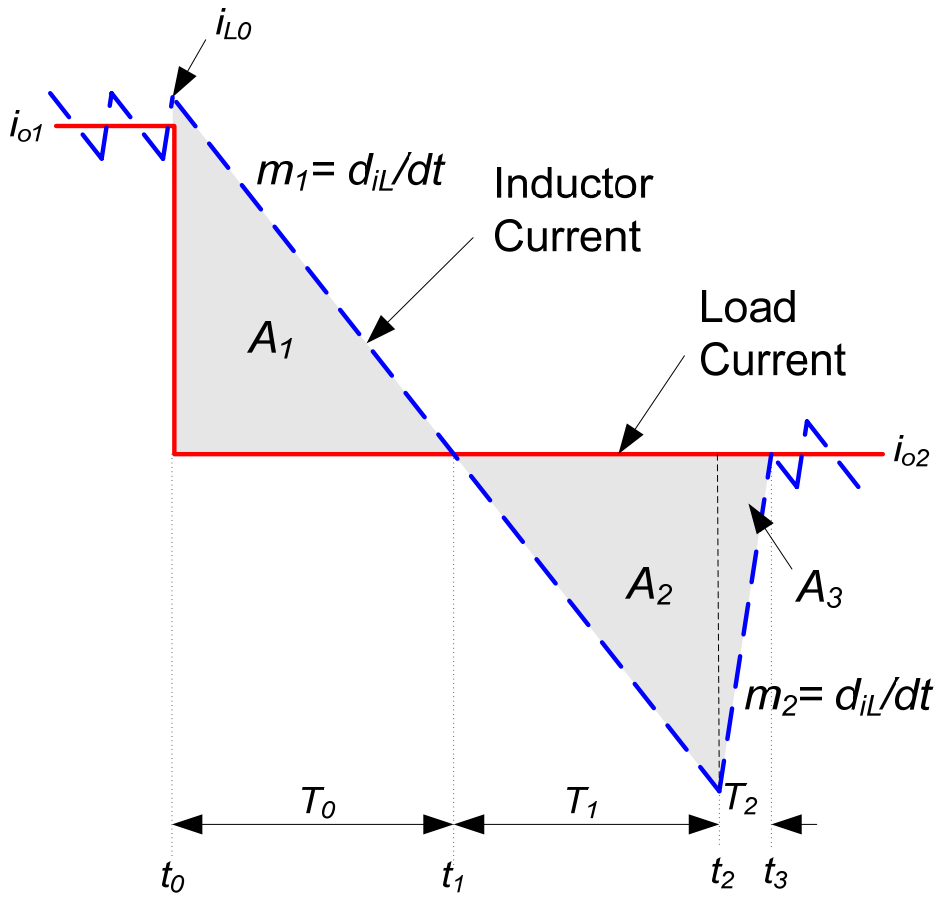
$$V_o \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 = 0$$





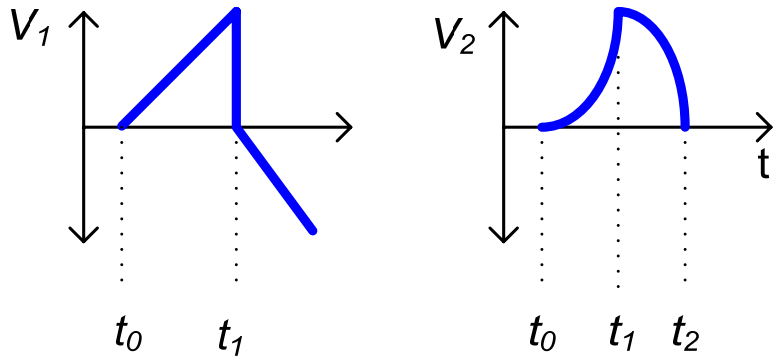
Double Integrator

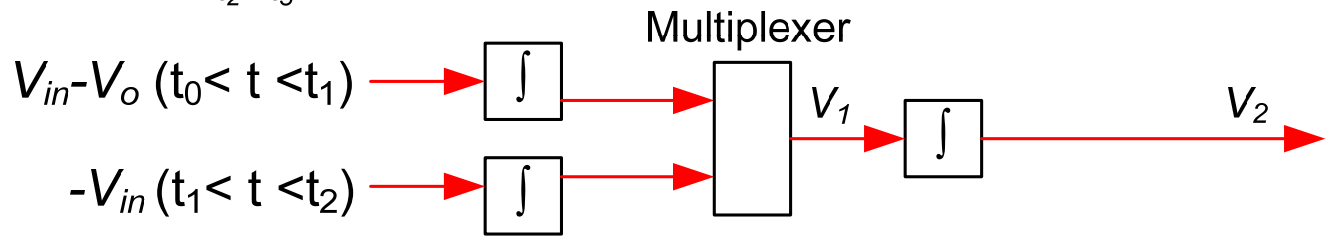
Negative Load Current Step



$$A_{discharge} - A_{charge} = 0$$

$$(V_{in} - V_o)\iint_{T0}(dt)^2 - V_{in}\iint_{T1}(dt)^2 = 0$$





Double Integrator

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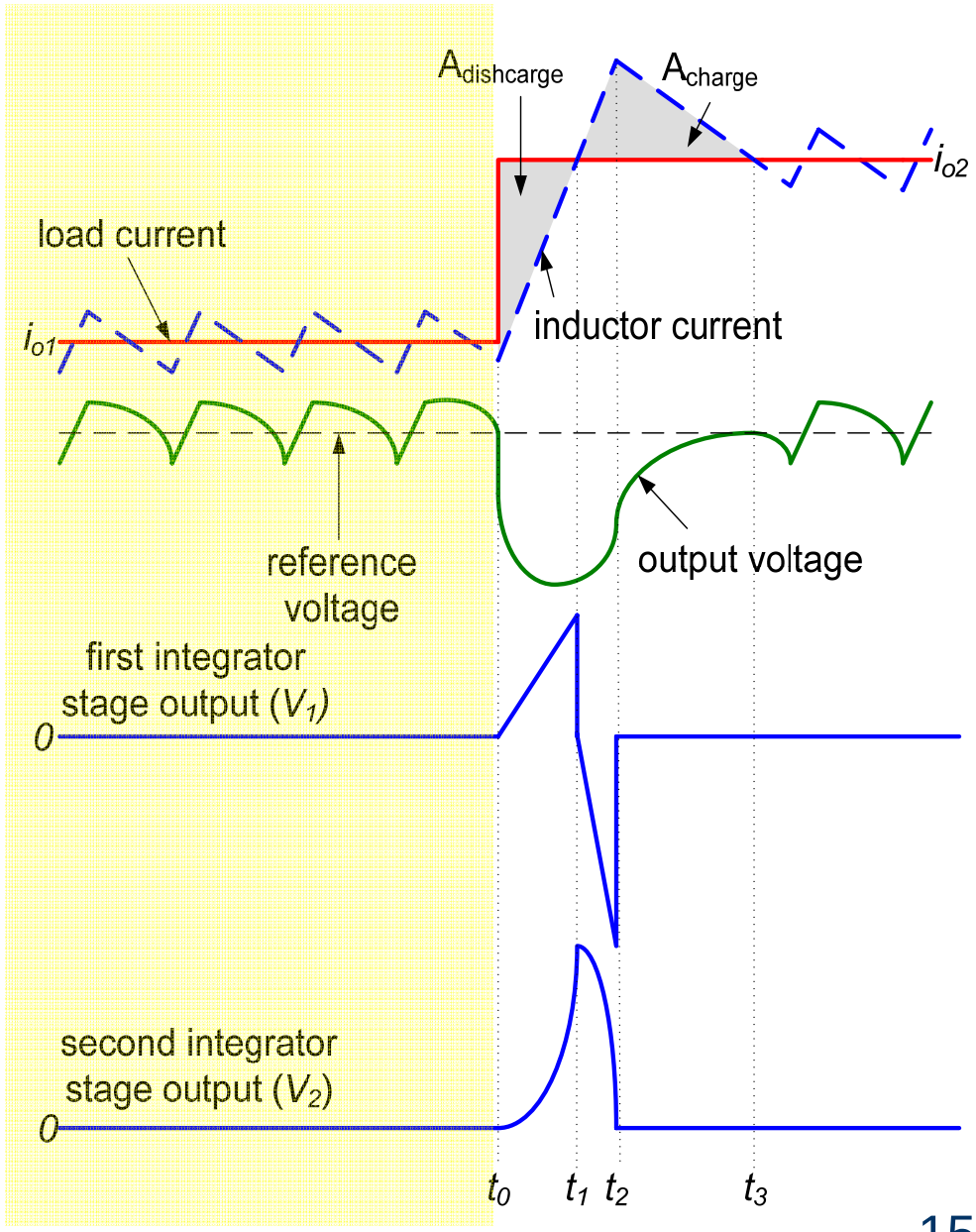
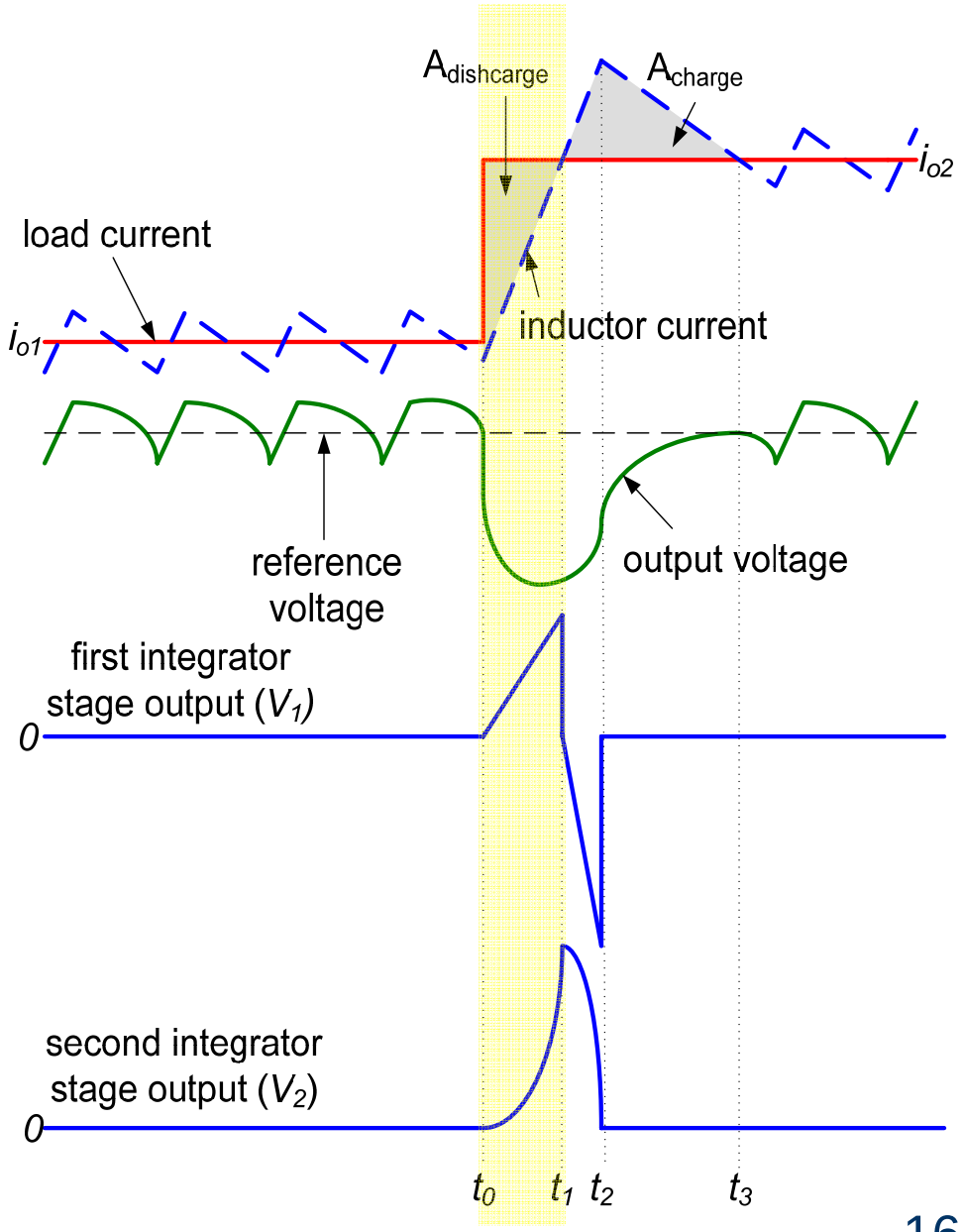
Controller Operation During a Positive Load Current Step

- Capacitor current threshold not exceeded
- Steady-state operation
  - Conventional linear controller in use



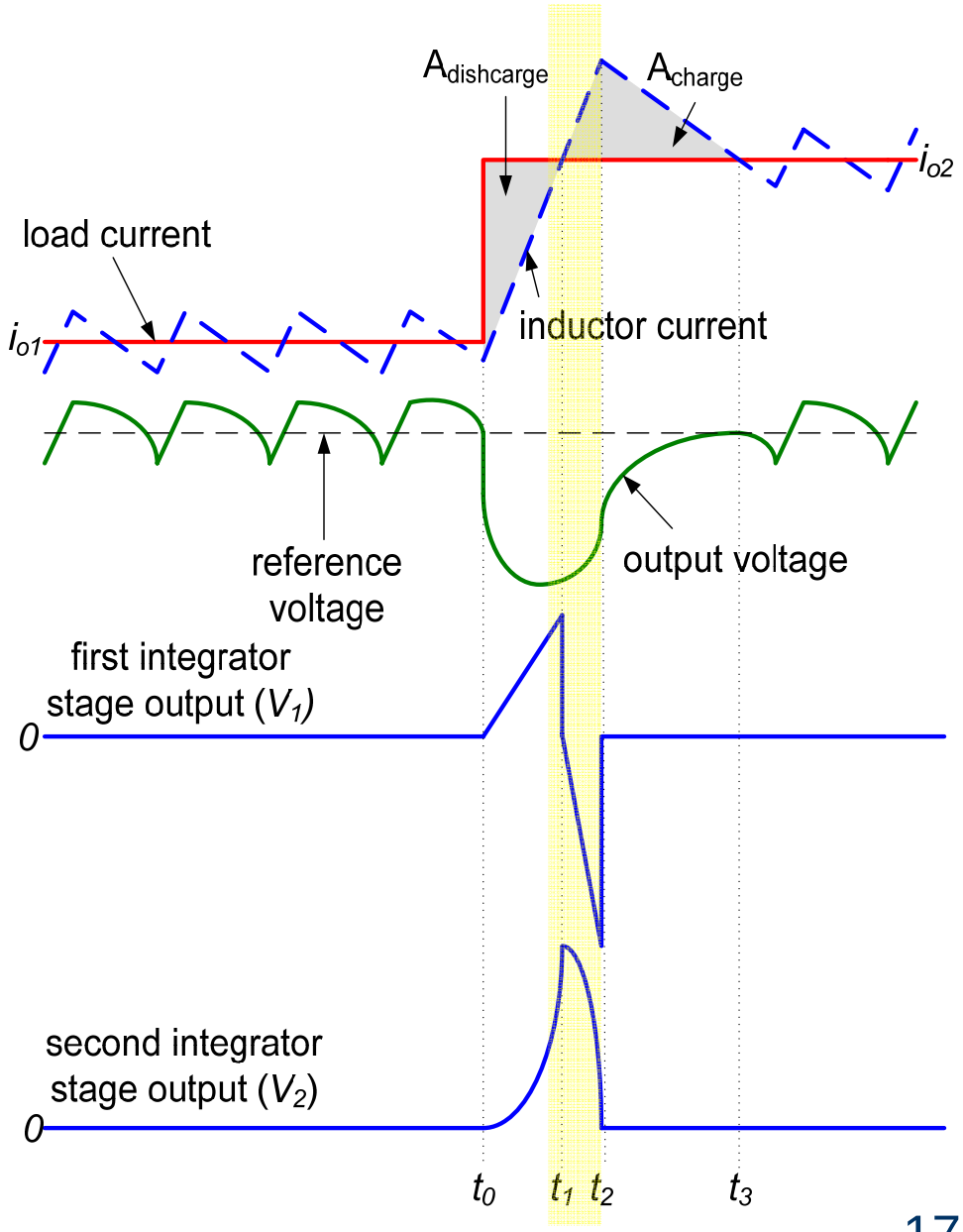
Controller Operation During a Positive Load Current Step

- Capacitor current threshold exceeded (at point t_0)
- Positive load current step detected
  - Duty cycle set to 100%
  - $k*V_o$ applied integrator 1a
  - V_1 increases linearly
  - V_2 increases exponentially



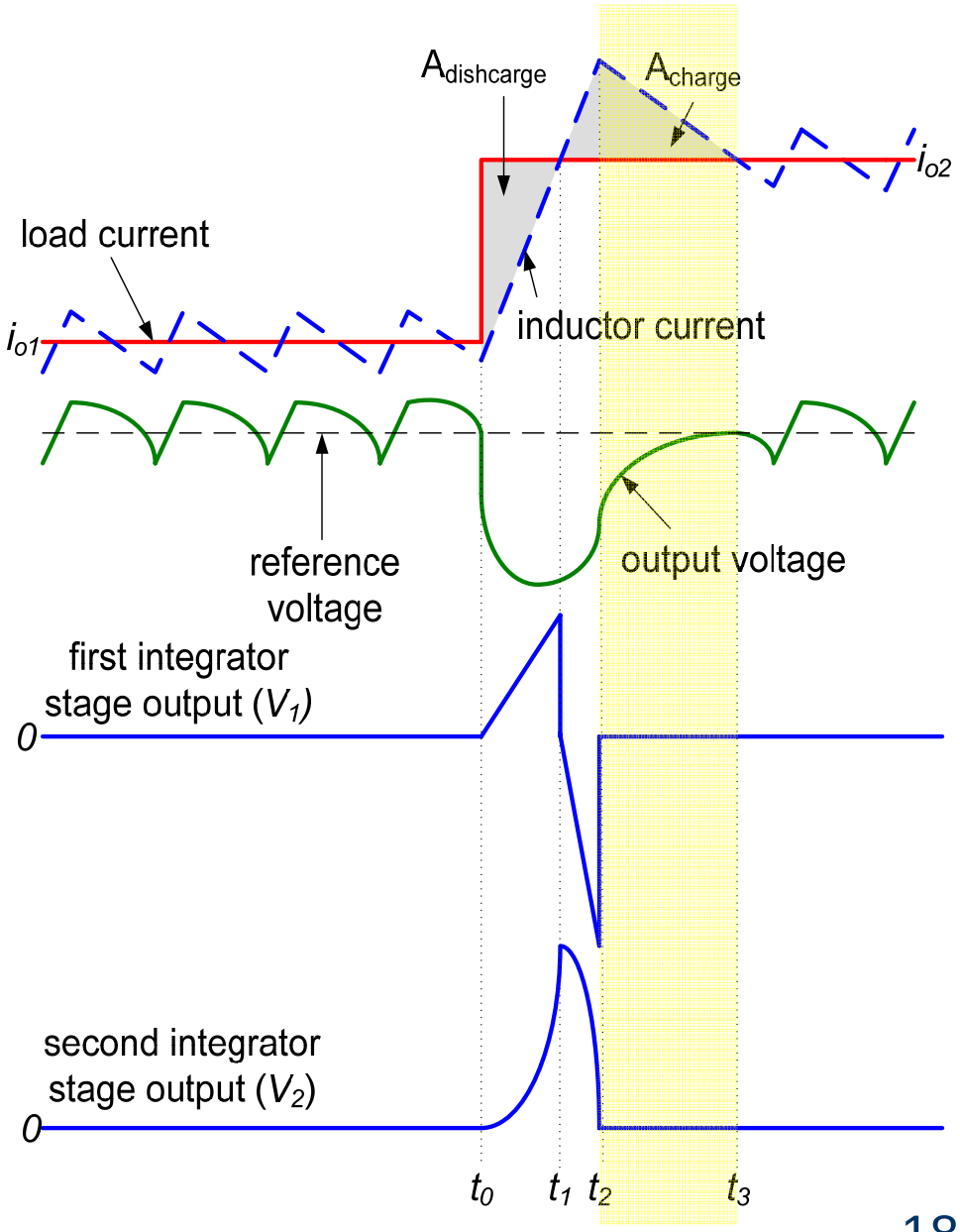
Controller Operation During a Positive Load Current Step

- **Capacitor current zero cross-over detected (at point t_1)**
  - **Integrator 1a reset**
  - **$-k*V_{in}$ applied to Integrator 1b**
  - **V_1 decreases linearly**
  - **V_2 decreases exponentially**
- **Duty cycle remains at 100%**



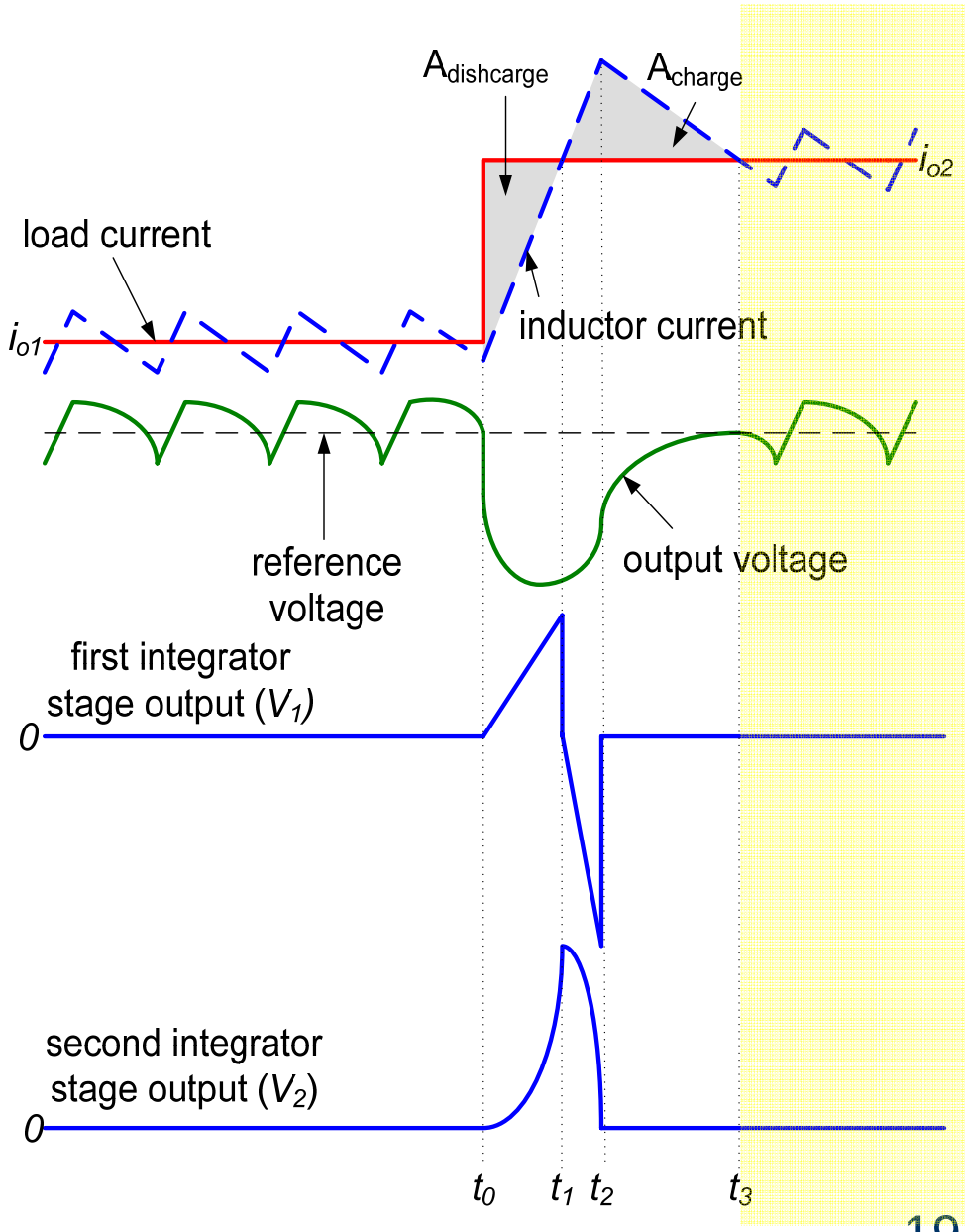
Controller Operation During a Positive Load Current Step

- V_2 zero cross-over detected (at point t_2)
  - Duty cycle set to 0%



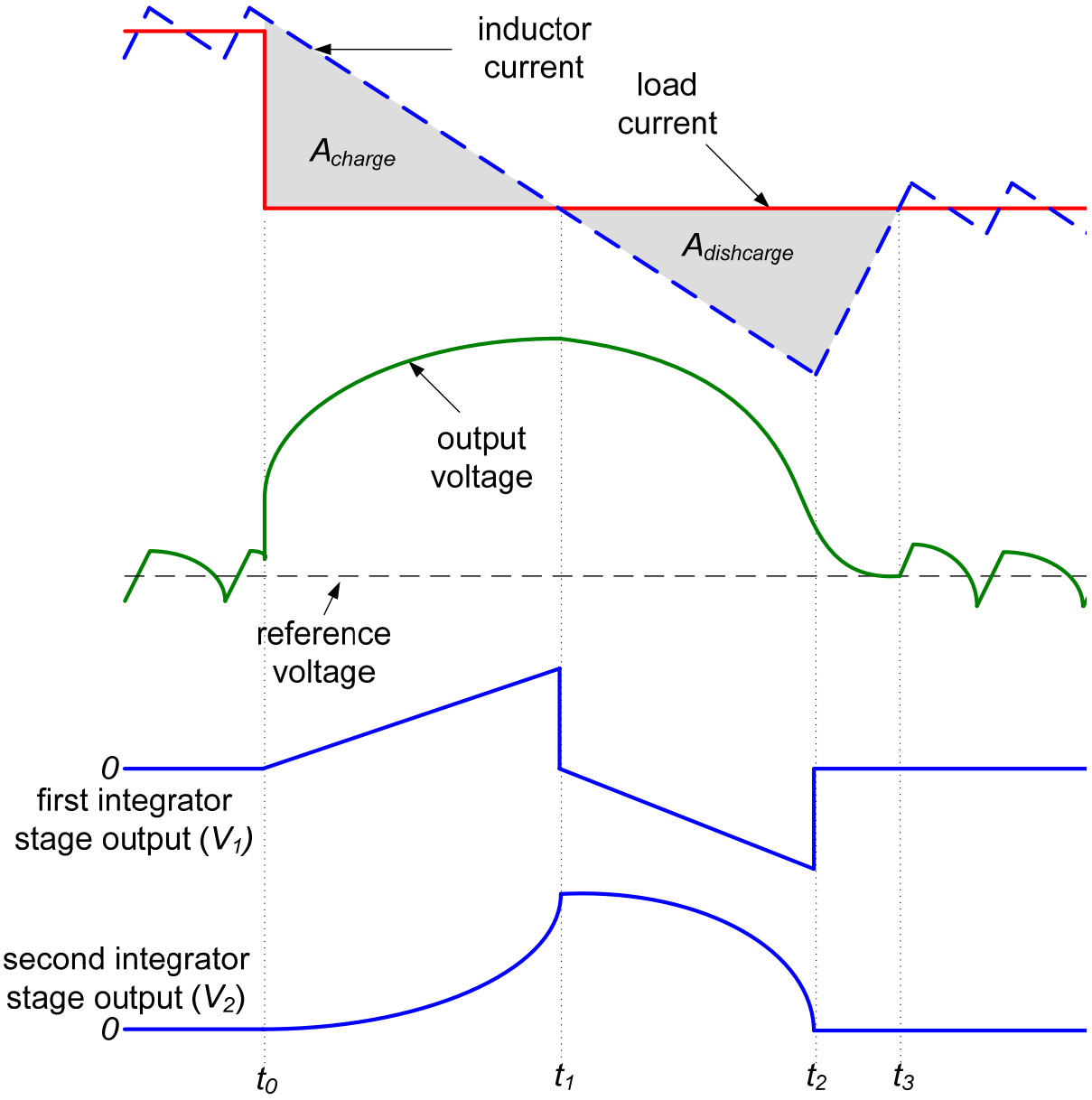
Controller Operation During a Positive Load Current Step

- **Second capacitor current cross-over detected (at point t_3)**
  - **Proposed controller deactivated**
  - **Conventional linear controller resumes operation**

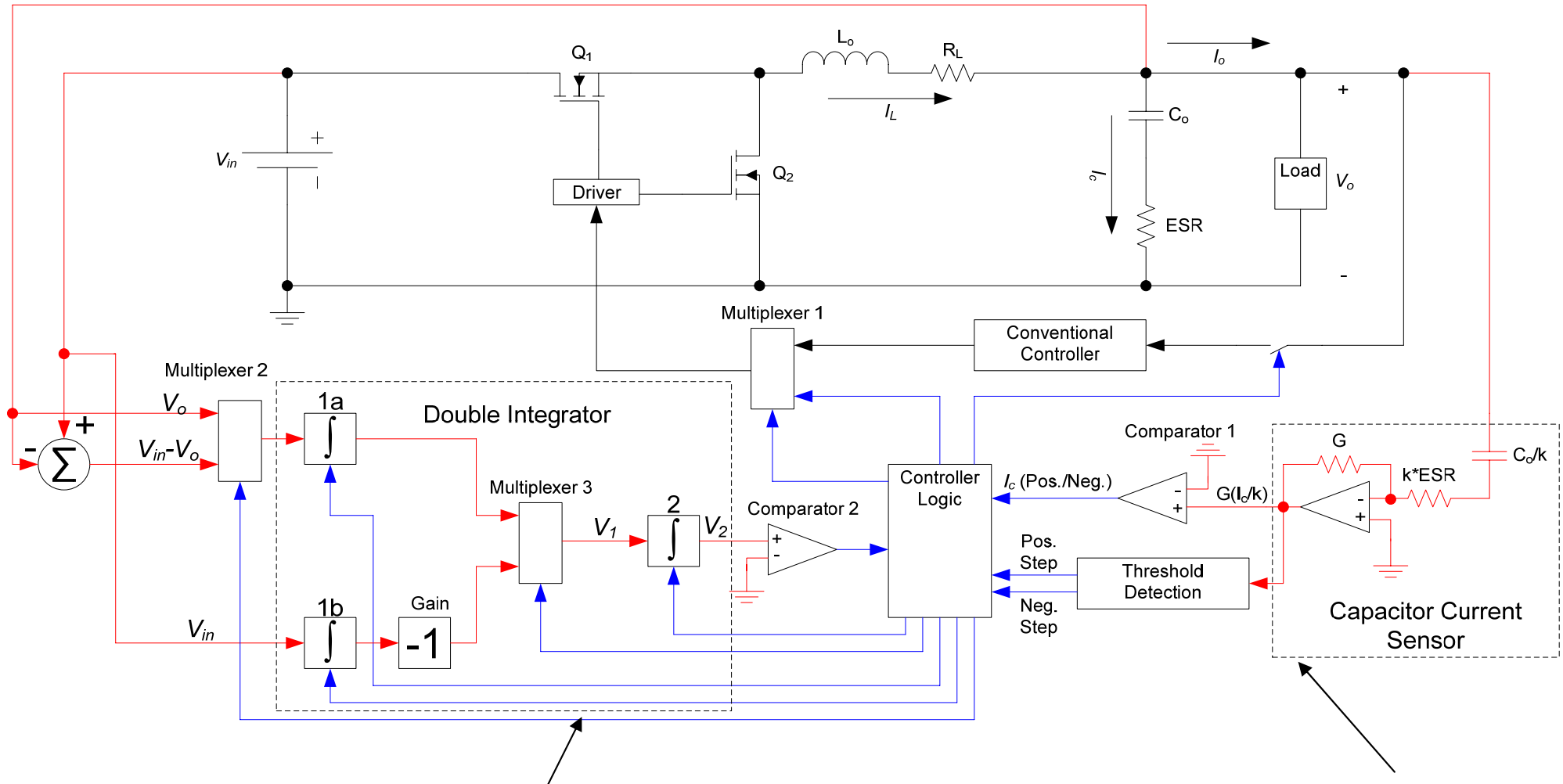


Controller Operation During a Negative Load Current Step

- Similar to positive load current step operation
- (V_{in}-V_o) applied to the double integrator for t_0-t_1



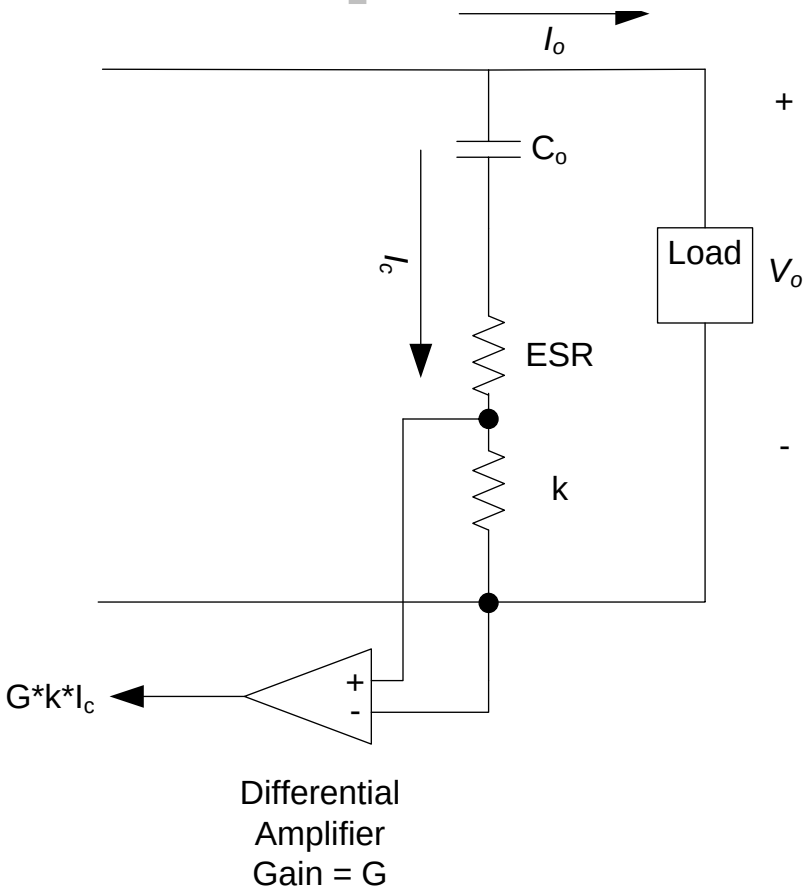
Block Diagram of Proposed Controller

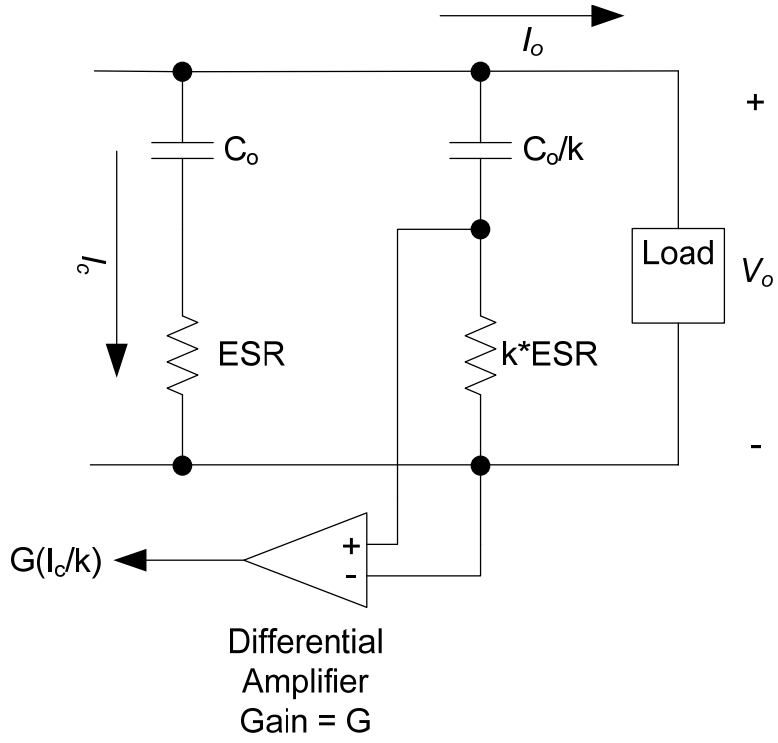


Double integrator calculates t_2

Capacitor current sensor detects load transient and zero cross-over point

Capacitor Current Sensor





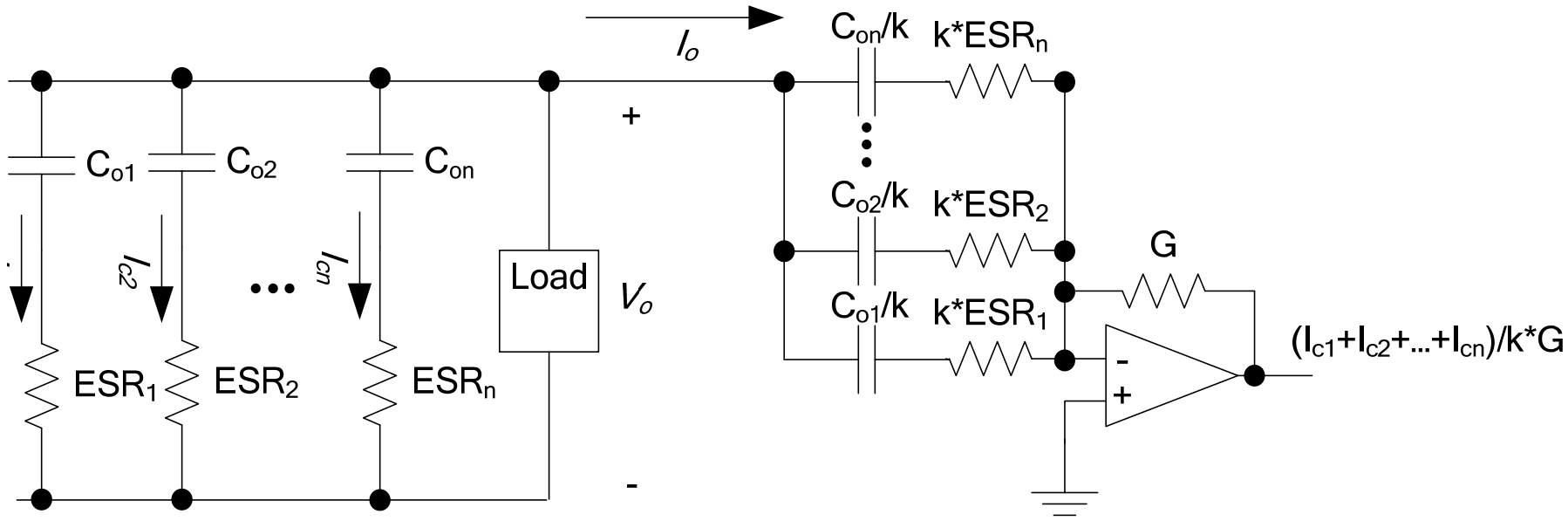
Series Differential Configuration

- Simple
- Effectively increases ESR and ESL
- Increases voltage drop

Parallel Differential Configuration

- Does not increase voltage drop
- Difficult to implement when ESR is low

Capacitor Current Sensor

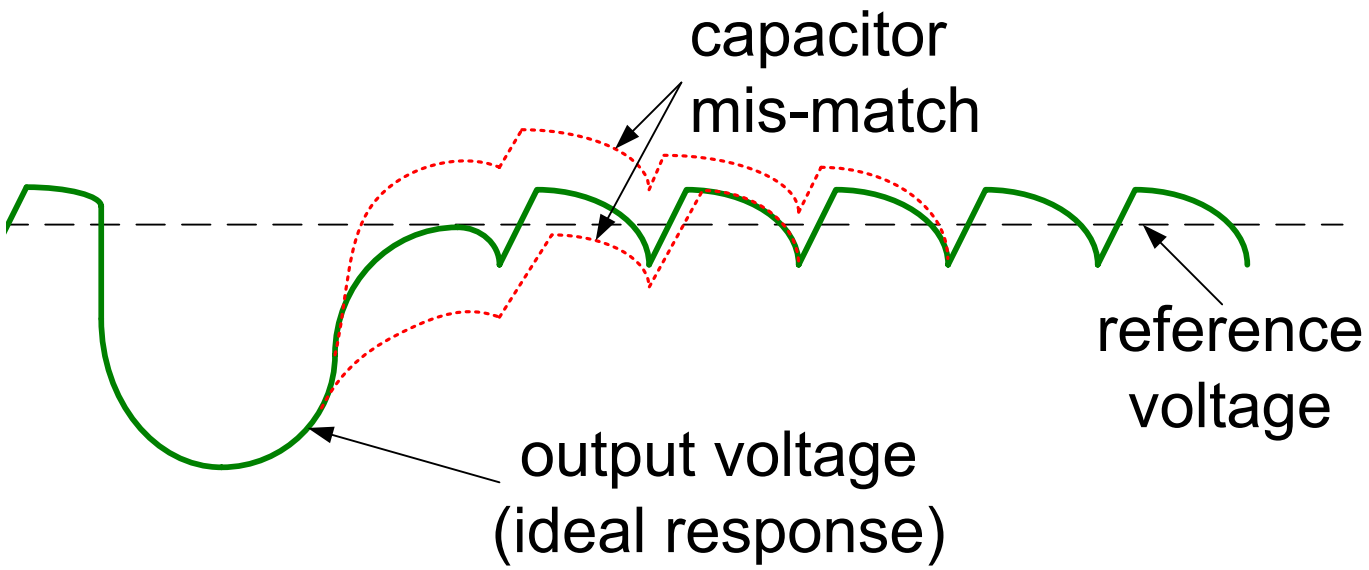


Trans-Impedance Configuration for Multiple Types of Capacitors

- Does not increase voltage drop
- Can be implemented even when using low ESR capacitors
- Is effective for mixed capacitor banks

Effect of Capacitor Tolerance

- **Capacitor mis-match due to tolerance**
- **May cause pre-mature or late detection of capacitor current zero cross-over**
- **Will only effect settling time, not voltage deviation**



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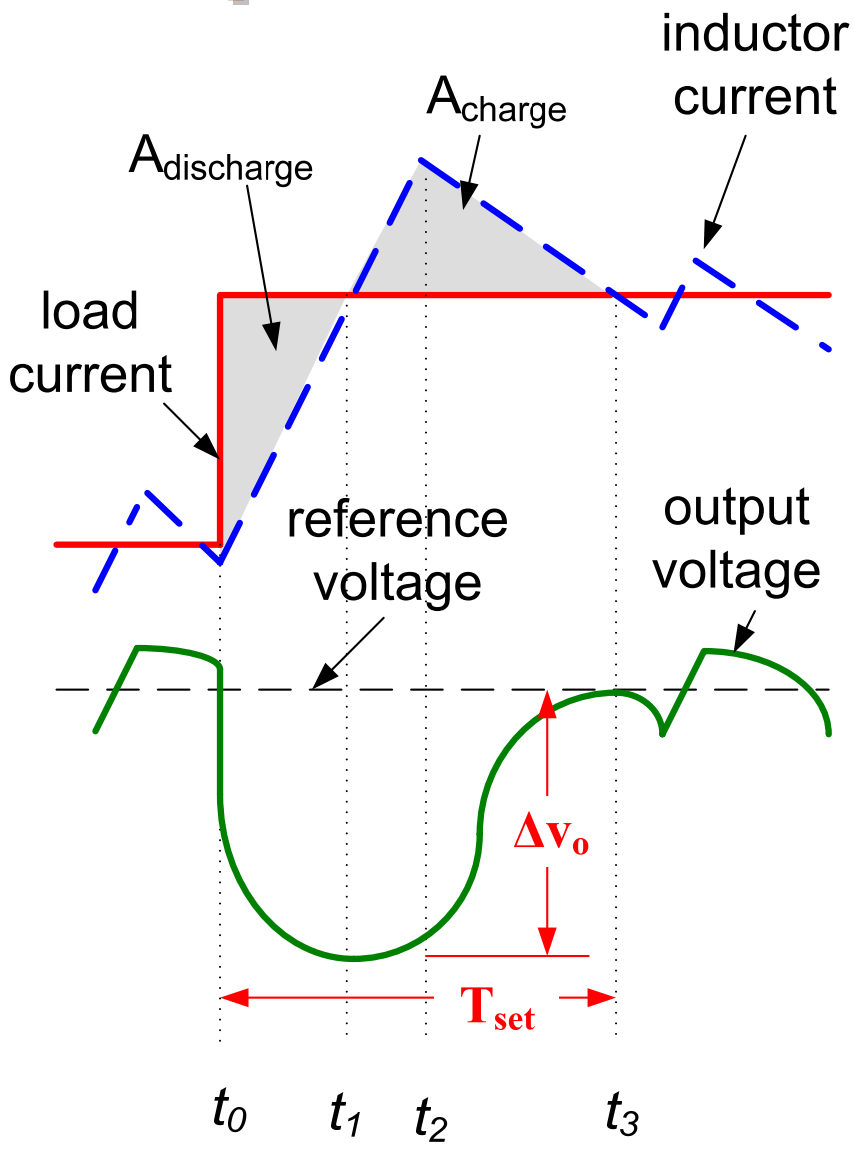
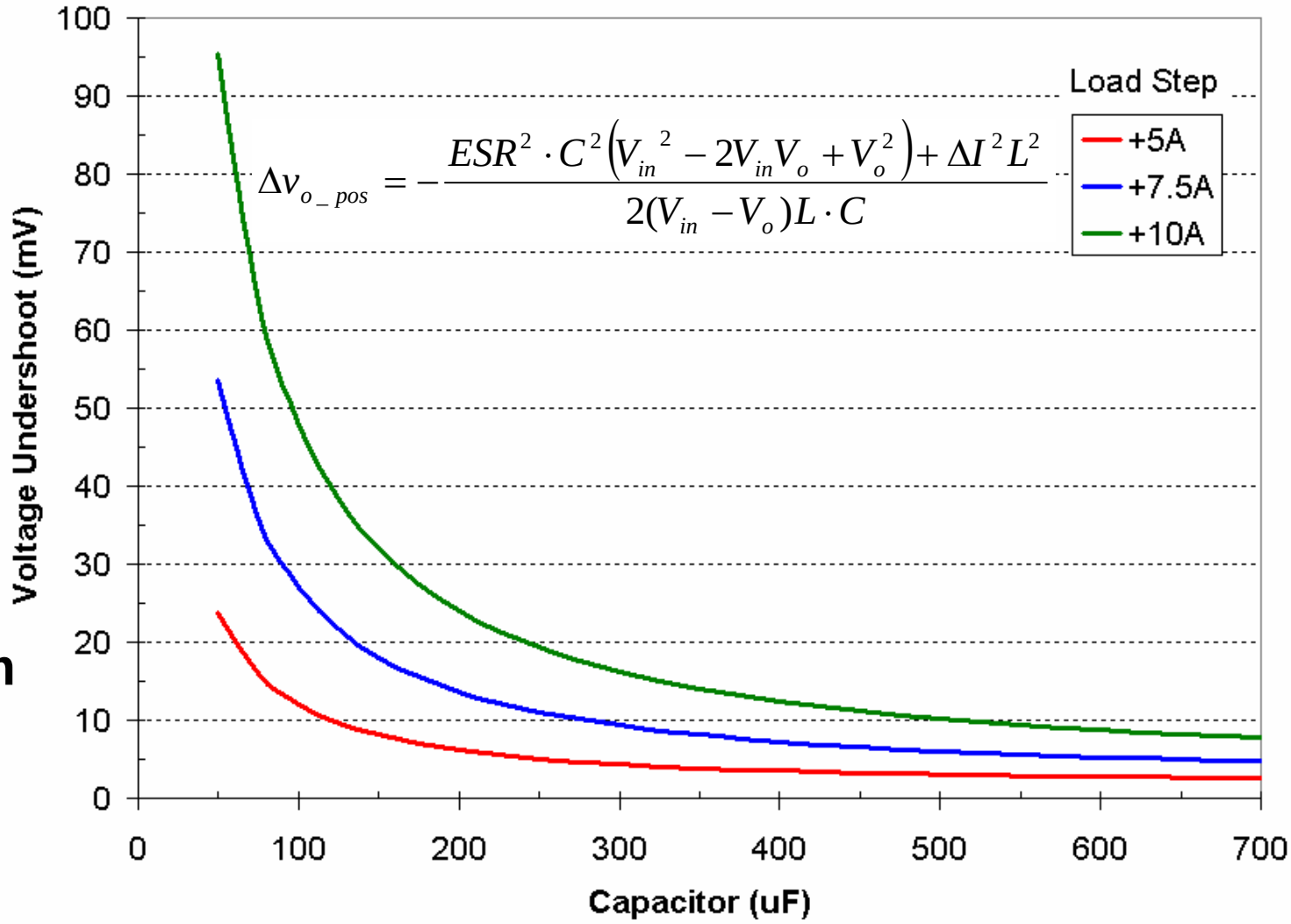
Accurate Calculation of Transient Response

- **Predictable response allows for simple and accurate calculation of voltage undershoot /overshoot (Δv_o) and settling time (T_{set})**
  - **Not possible for controller designed by small-signal model**
- **Greatly simplifies output filter design**



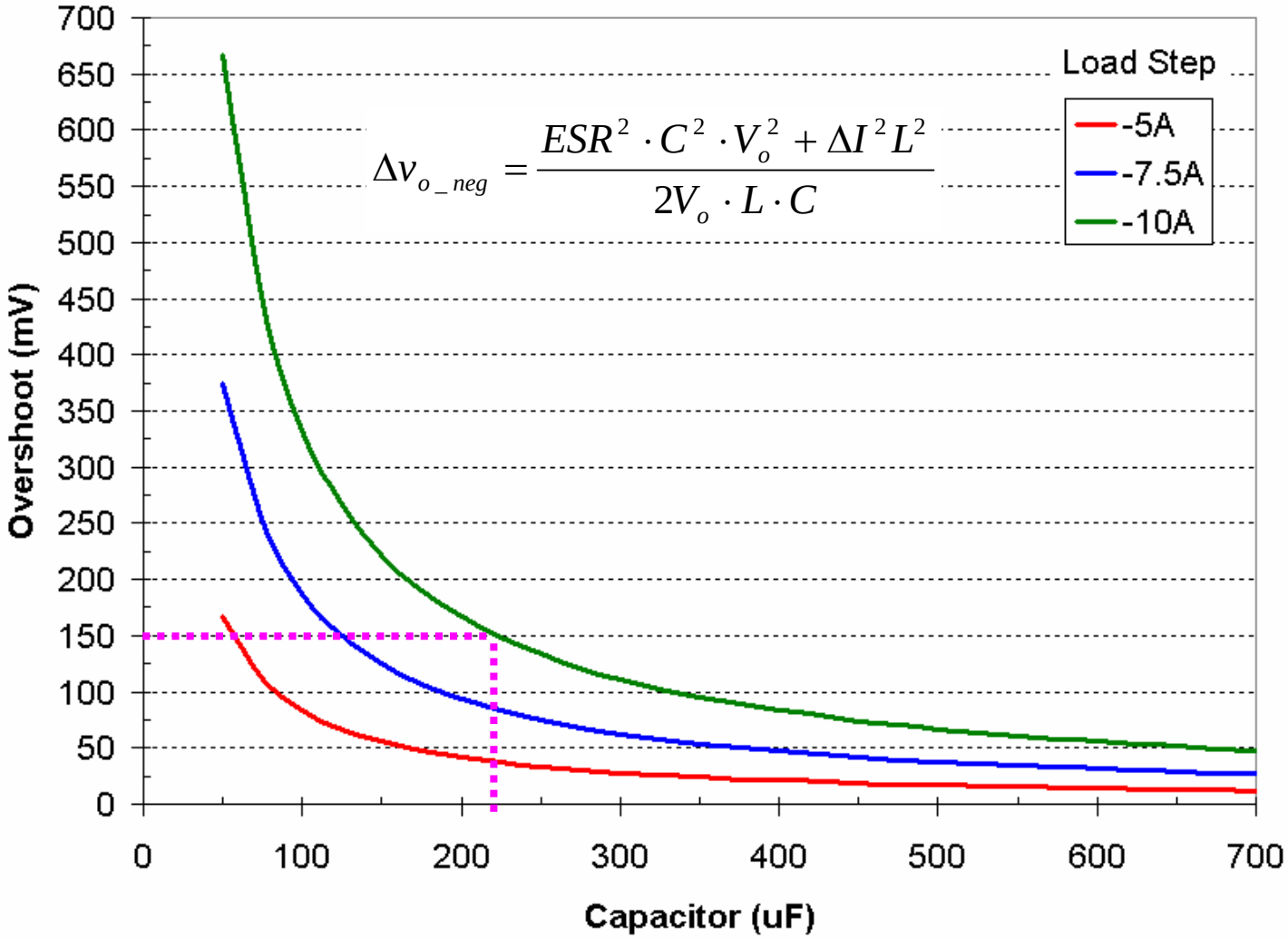
Theoretical Voltage Deviation (Positive Load Current Step)

- **Can choose output capacitance for desired undershoot**
- **V_{in} = 12V**
  V_o = 1.5V
  L=1uH
  ESR=0.5mOhm



Theoretical Voltage Deviation (Negative Load Current Step)

- Can choose output capacitance for desired overshoot
- V_{in} = 12V
  V_o = 1.5V
  L=1uH
  ESR=0.5mOhm
- Example:
  - -10A Step
  - For 150mV max overshoot, choose 215uF

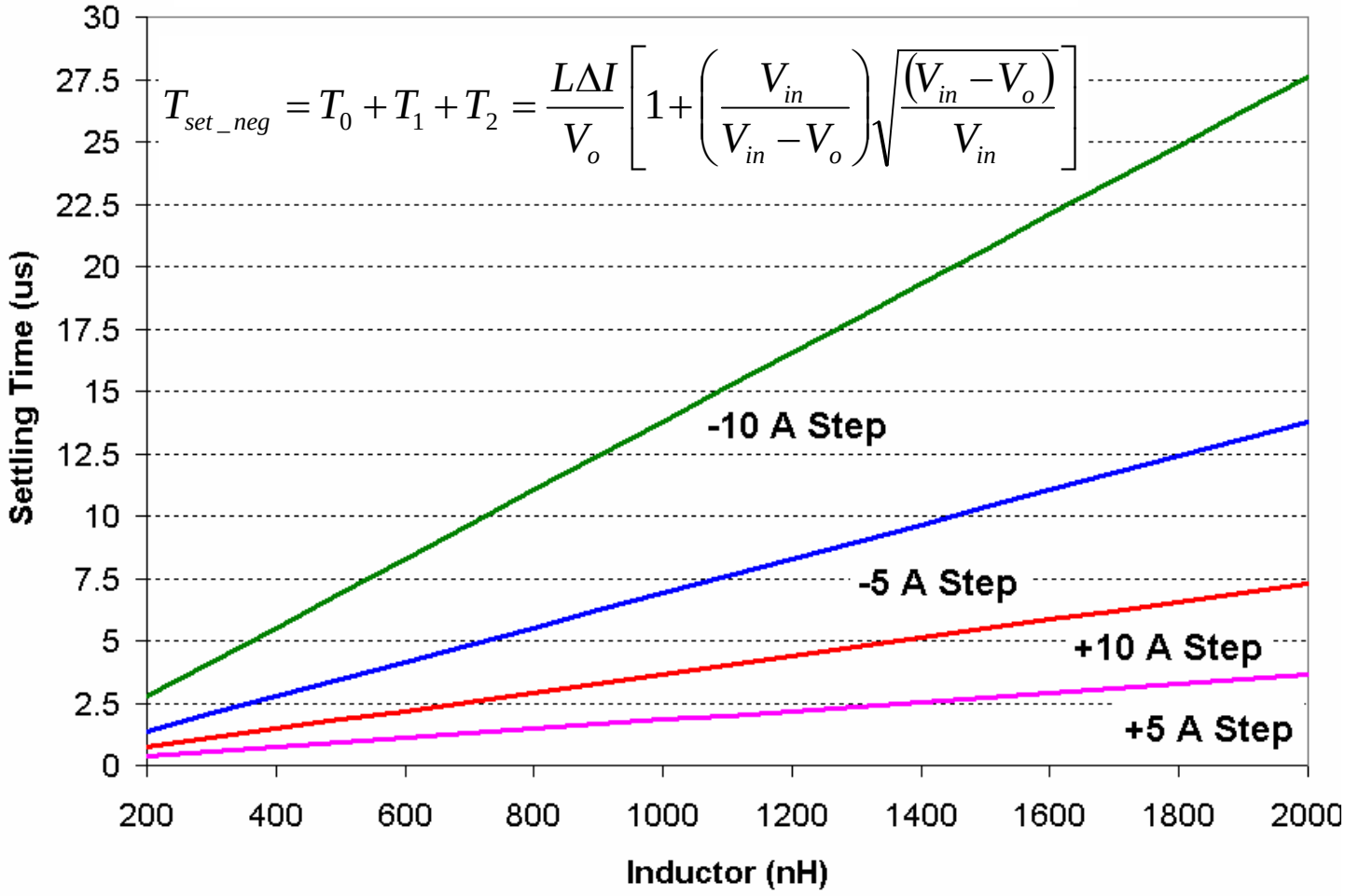


Theoretical Settling Time

$$T_{set\_pos} = T_0 + T_1 + T_2 = \frac{L\Delta I}{(V_{in} - V_o)}\left(1 + \frac{V_{in}}{V_o}\sqrt{\frac{V_o}{V_{in}}}\right)$$

$$T_{set\_neg} = T_0 + T_1 + T_2 = \frac{L\Delta I}{V_o}\left[1 + \left(\frac{V_{in}}{V_{in} - V_o}\right)\sqrt{\frac{(V_{in} - V_o)}{V_{in}}}\right]$$

- **Settling time only dependant on load current step and inductance**
  - **Not dependant on output capacitance**
- **V_{in} = 12V**
  V_o = 1.5V



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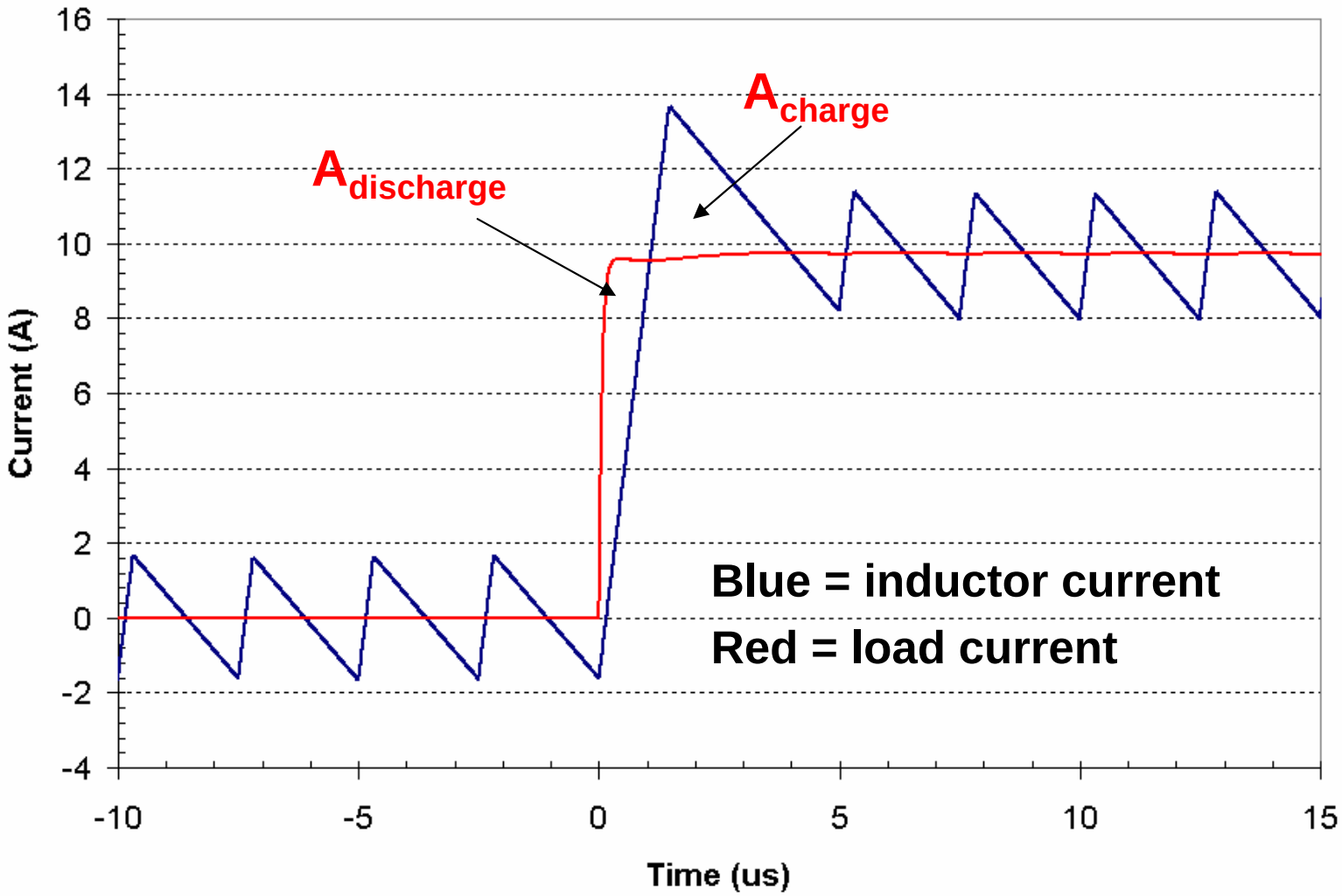
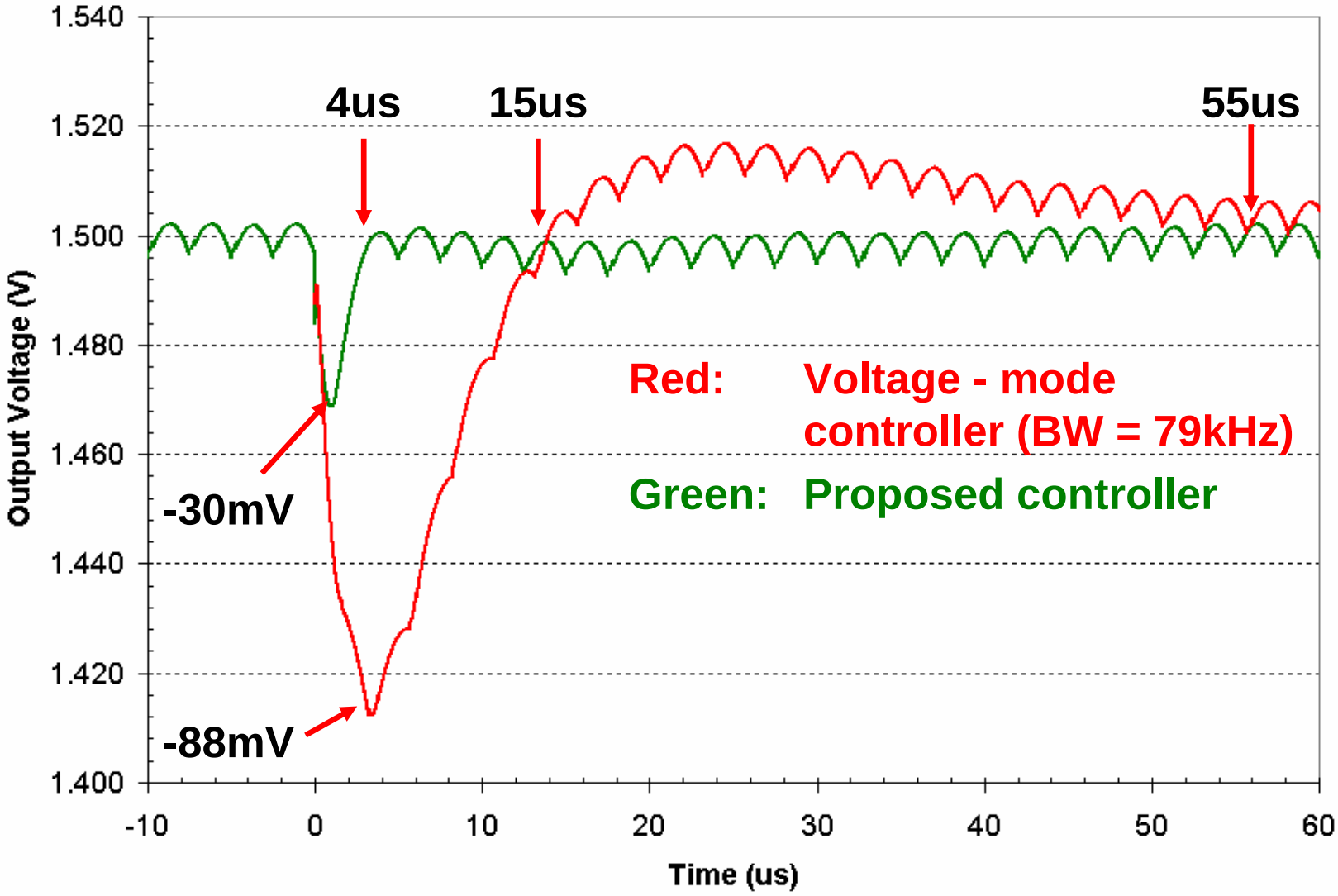
Simulation (10A Step Up)

Buck Converter

V_{in} = 12V
V_o = 1.5V,
f = 400kHz
L = 1uH,
C = 180uF,
ESR = 0.5mOhm
ESL = 100pF



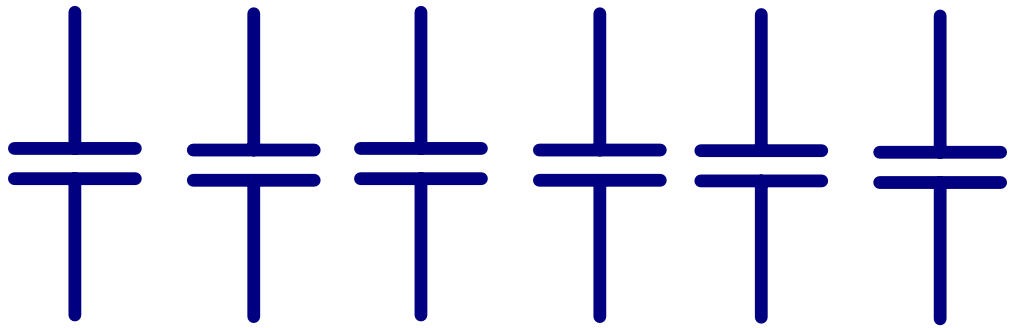
Simulation (10A Step Up)



Capacitor Requirements

Example:

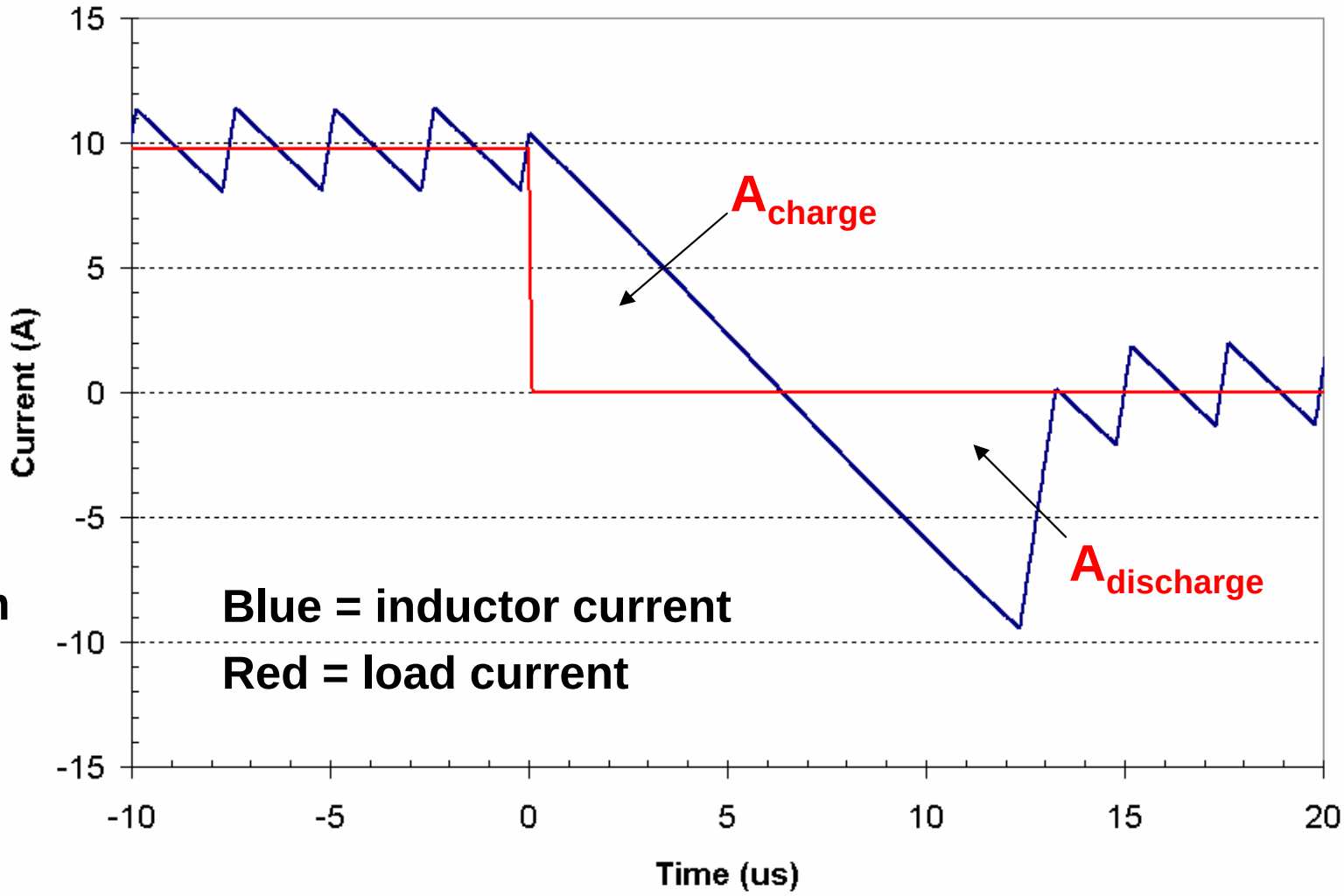
- **-88mV voltage deviation**
- **0→10A step change**
  - **Voltage mode control : 180uF**
  - **Proposed controller: 60uF**



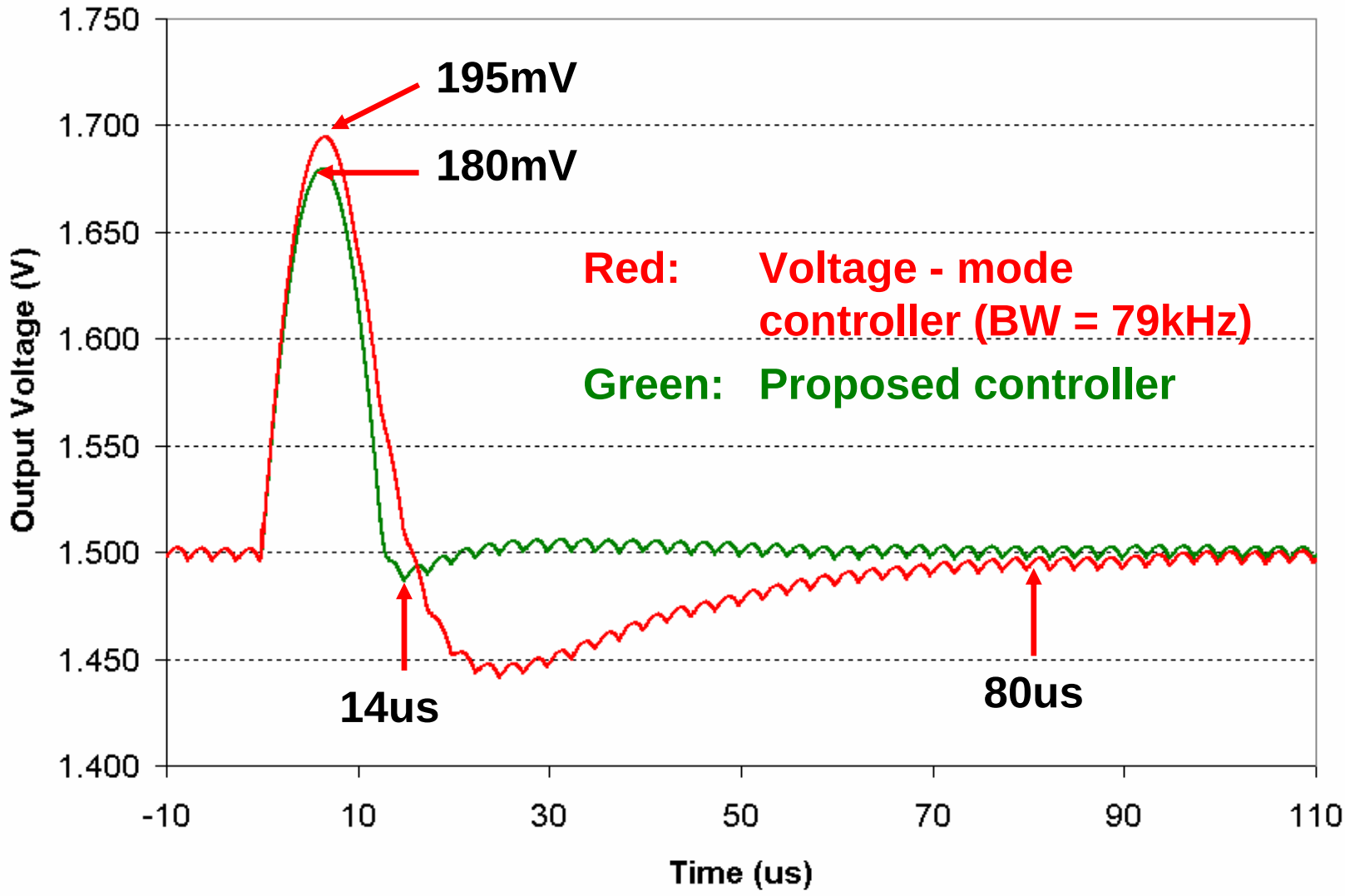
Simulation (10A Step Down)

Buck Converter

V_{in} = 12V
V_o = 1.5V,
f = 400kHz
L = 1uH,
C = 180uF,
ESR = 0.5mOhm
ESL = 100pF



Simulation (10A Step Down)



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Experimental Results (Voltage Mode Controller)

V_{in} = 12V

V_o = 1.5V,

f = 400kHz

L = 1uH,

C = 180uF

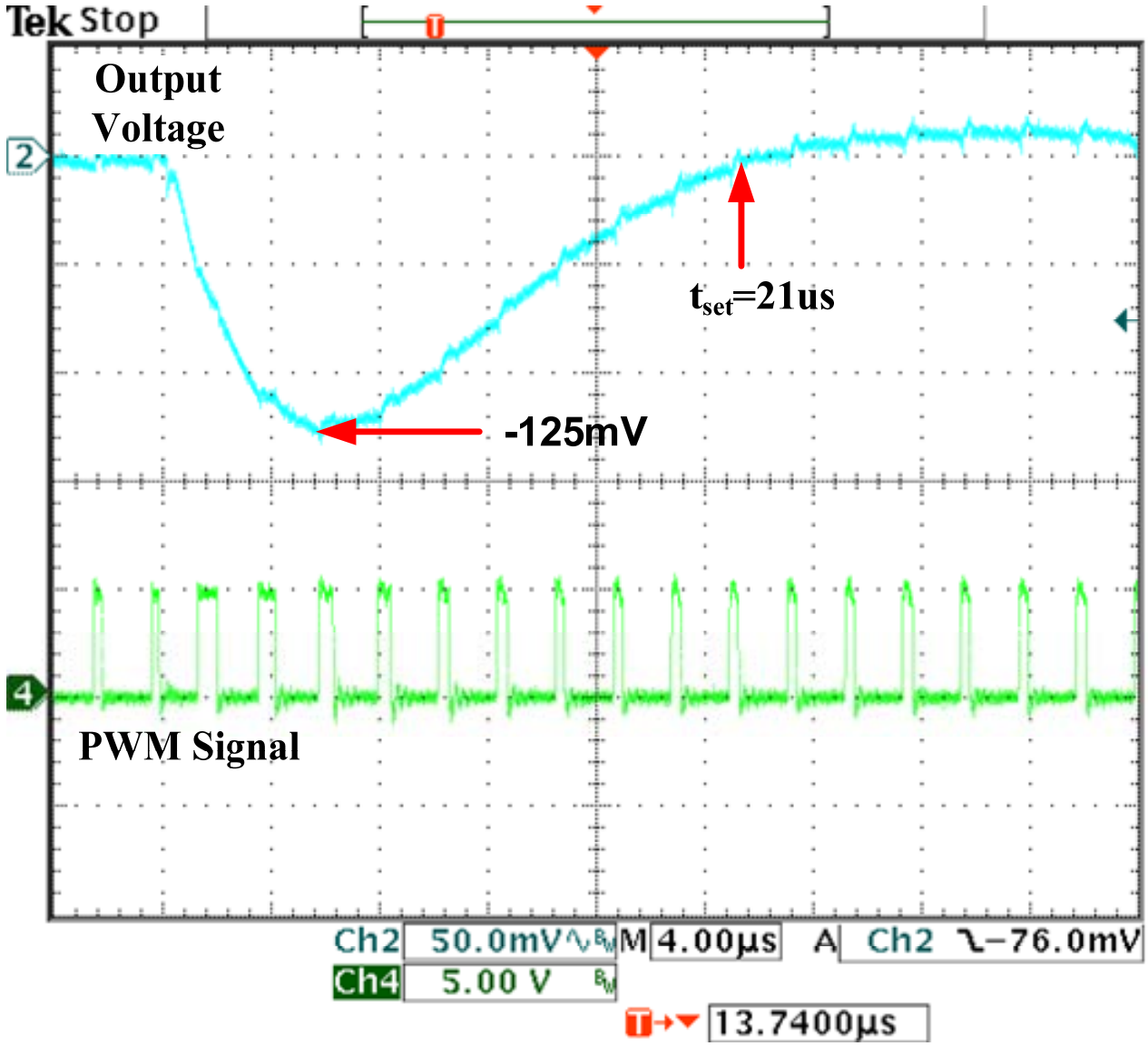
ESR = 0.5mOhm,

ESL = 100pF

Step Up:

0A → ≈10A

di/dt > 50A/us



Experimental Results (Proposed Controller)

Settling time: 4us

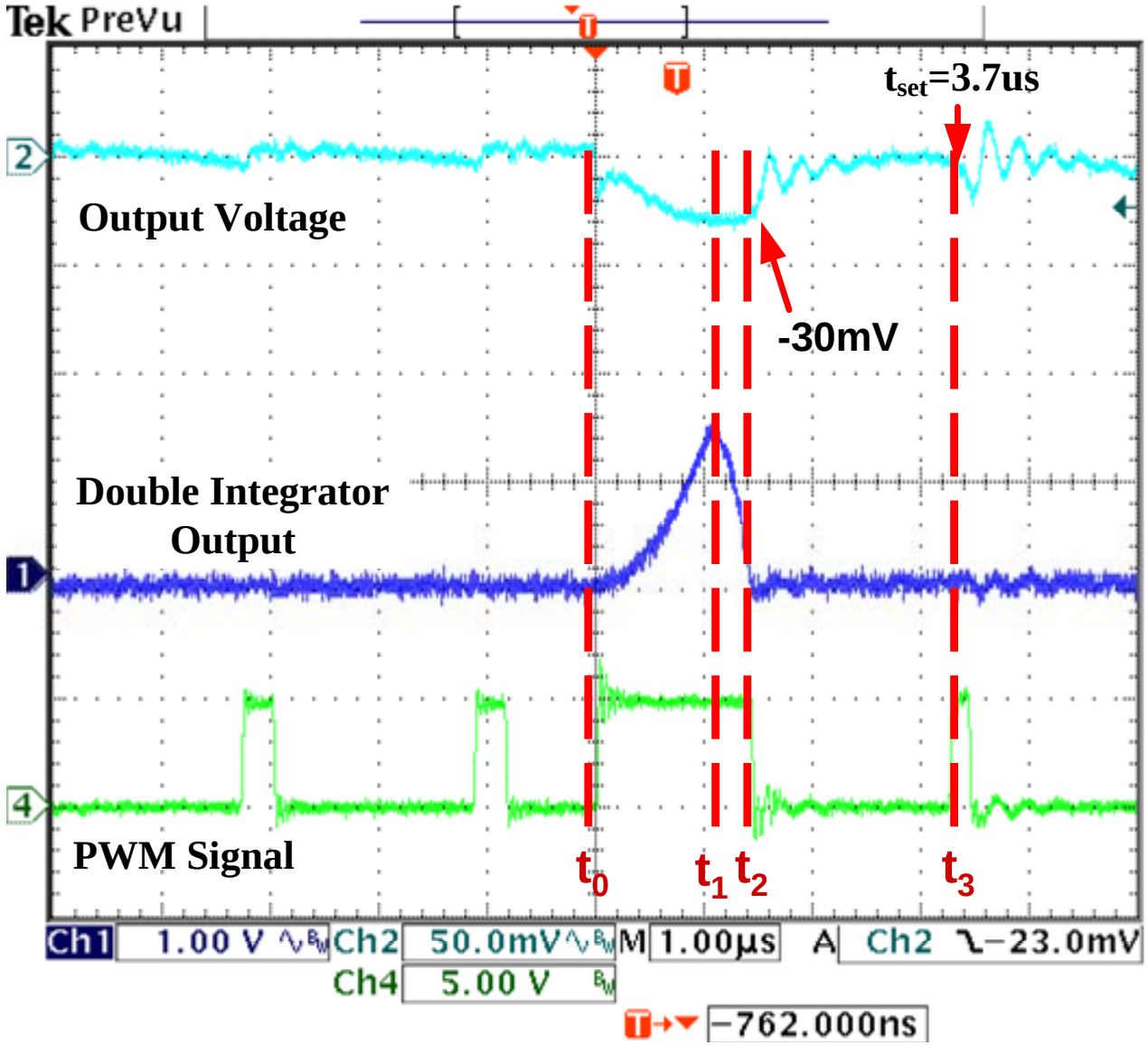
Calculated: 4us

Improved by 80%

Undershoot: 30mV

Calculated: 27mV

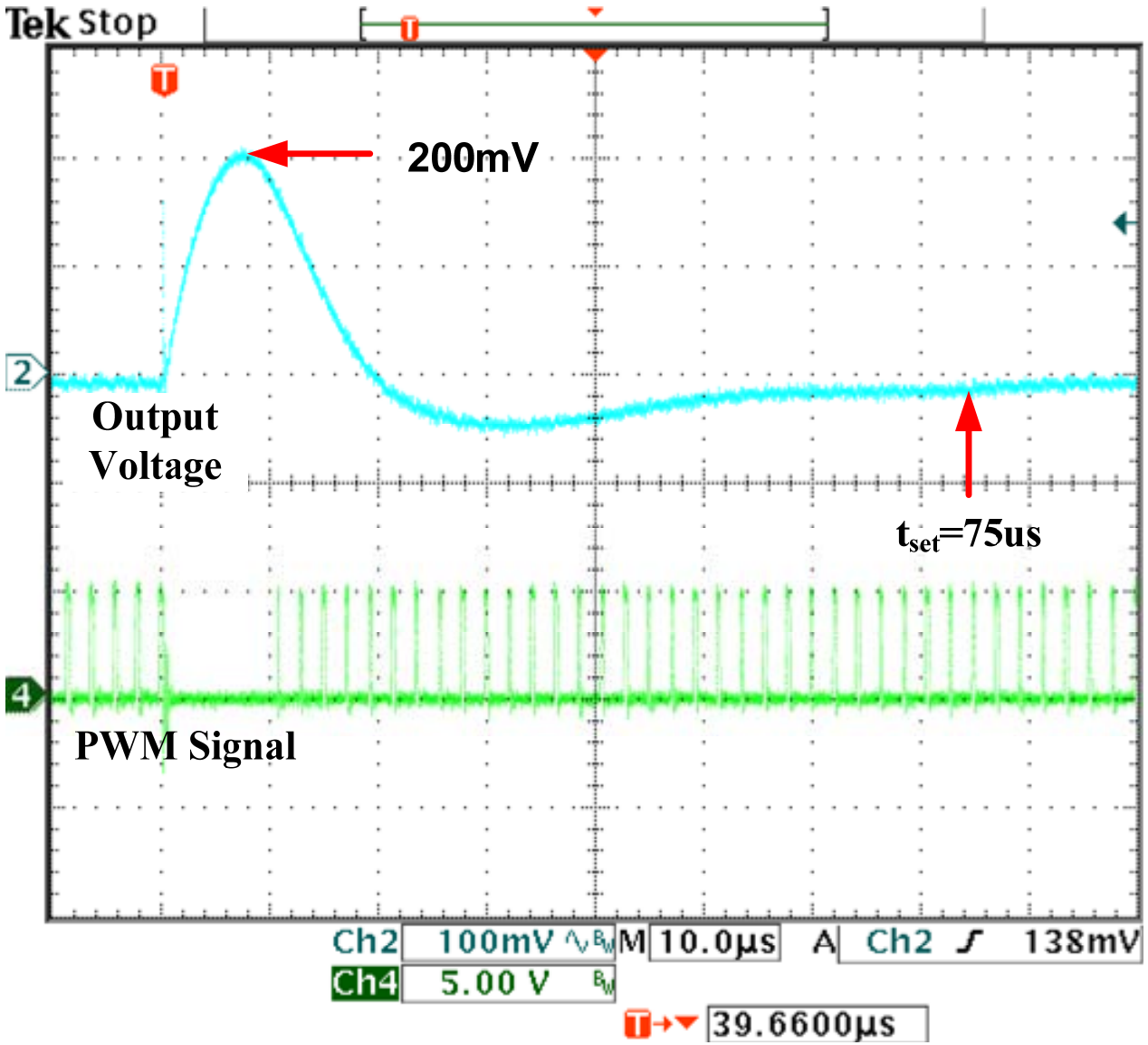
Improved by 76%



Experimental Results (Voltage Mode Controller)

V_{in} = 12V
V_o = 1.5V,
f = 400kHz
L = 1uH,
C = 180uF
ESR = 0.5mOhm,
ESL = 100pF

Step Down:
≈10A → 0A
di/dt > -50A/us



Experimental Results (Proposed Controller)

Settling time: 12us

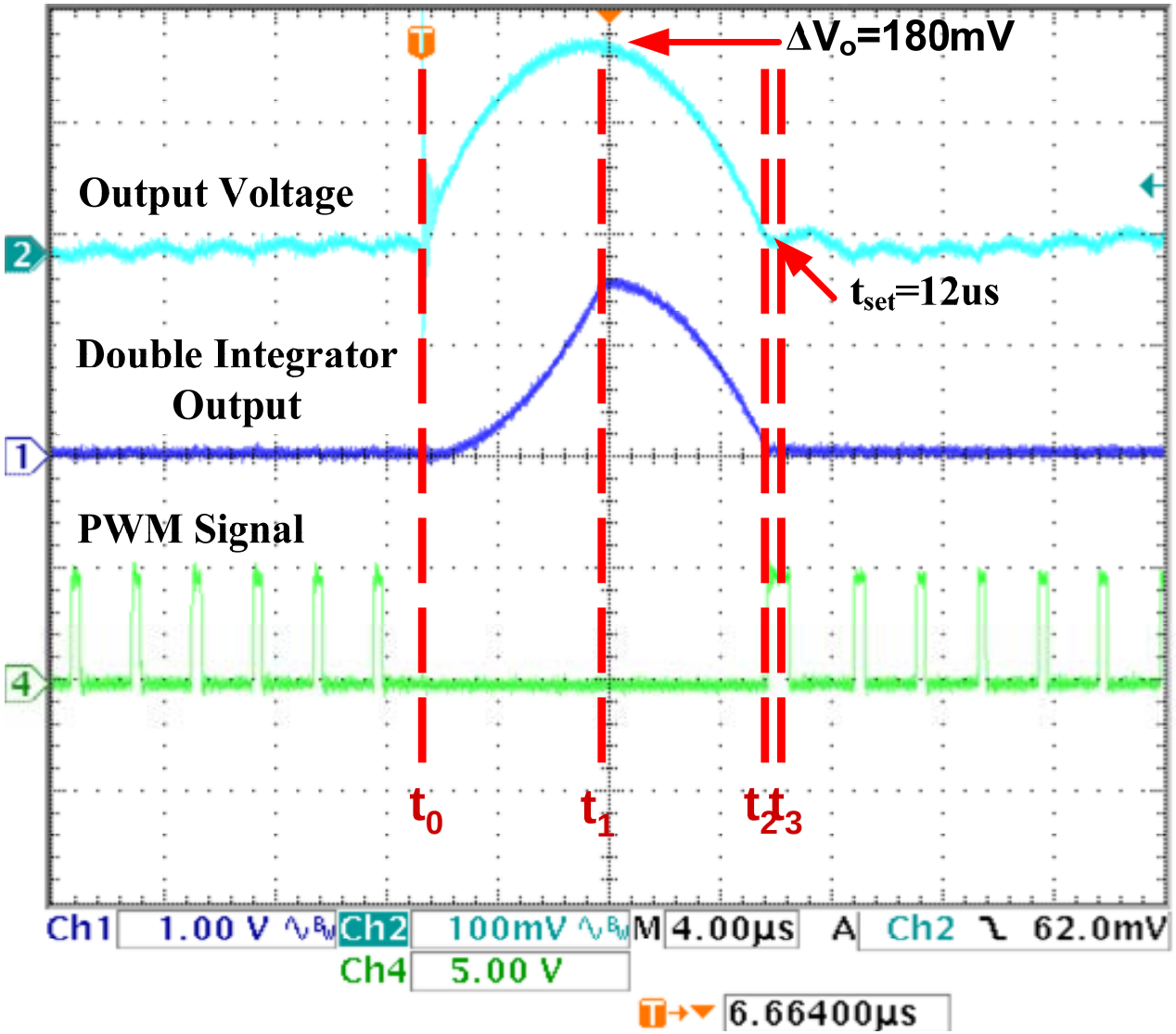
Calculated: 14us

Improved by 83%

Overshoot: 180mV

Calculated: 180mV

- **Asymmetric Response**
- **Improved by 10%**
- **Only modest improvement due to small duty cycle**



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Summary of Advantages

- **Dynamic response to load transient can be accurately predicted**
  - **Greatly simplifies design of converter**
- **Very simple design**
  - **Only simple analog functions required**
- **Optimal response to load transient guaranteed every time**

  For 12V → 1.5V applications:
  - **Proposed controller significantly improves undershoot (76%) and settling time (80%) for load step-up**
  - **Proposed controller improves overshoot (10%) and significantly improves settling time (83%) for load step-down**

Conclusions

- New control method described
- For a positive load current step
  - Duty cycle set to 100% for calculated period of time
  - Duty cycle set to 0% for period of time
- Capacitor current sensor and double integrator used to determine aforementioned time periods

Thank you for your time.

Any Questions?