

# High-Efficiency Dual-Phase *LLC* Converter With Asymmetric Resonant Tanks and Switch-Controlled Capacitor for EV Auxiliary Power Modules

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**Abstract**—A novel asymmetrical resonant tank design is proposed for dual-phase *LLC* dc–dc converters used in the auxiliary power module (APM) of electric vehicles (EVs), featuring built-in redundancy. The proposed design ensures that the impedance of one phase remains consistently either higher or lower than the other phase's impedance across a wide input and output voltage range. Consequently, a single switch-controlled capacitor (SCC) circuit suffices for effective active current sharing, reducing system complexity and implementation costs without compromising efficiency or performance. Each phase of the proposed converter is designed separately to meet the requirements of a wide voltage gain range while maintaining an expected voltage gain relationship between the phases. A sensitivity analysis was conducted, considering the maximum phase-to-phase mismatch resulting from  $\pm 5\%$  component tolerances between the two phases. Experimental results from a full-scale APM implementing the proposed dual-phase *LLC* dc–dc converter, operating with an input voltage of 250–475 V, an output voltage of 9–16 V, and a maximum output current of 285 A (4-kW output power), demonstrate the design's success in achieving effective current sharing across input/output voltage and load ranges. Furthermore, the implemented APM achieves a peak efficiency of 96.3% and a load average efficiency exceeding 95.6% across the high-voltage (HV) battery voltage range.

**Index Terms**—Auxiliary power module (APM), current sharing, dual phase, electric vehicle (EV), *LLC* resonant dc–dc converter, low-voltage dc–dc converter (LDC) converter, redundant, switch-controlled capacitor (SCC).

## I. INTRODUCTION

THE high-voltage (HV) to low-voltage dc–dc converter (LDC) in electric vehicles (EVs), commonly referred to as the auxiliary power module (APM), plays a vital role in supplying the 12-V battery and LV bus that power all auxiliary vehicle loads. As EVs evolve, particularly with the emergence of connected and automated vehicles (CAVs), APMs face growing demands in terms of power, efficiency, and reliability. Future platforms are expected to support 4–5 kW of auxiliary power and handle peak currents of up

to 300–400 A to enable functions such as radar, LiDAR, zonal ECUs, and safety and critical electronics [1]. At the same time, government agencies like U.S. DOE are setting ambitious targets for power density and efficiency [2], while cost-sensitive automotive markets are pushing for system-level integration. Merging the APM with the onboard charger (OBC) and traction inverter into X-in-1 platforms is one approach to reduce cost and volume [3], [4], [5].

To further support system reliability and improve state-of-charge (SoC) consistency, battery balancing circuits are being integrated into APM designs [6], [7], [8]. However, these benefits are accompanied by common technical challenges in APM design. One of the most critical hurdles is managing the wide input/output voltage range resulting from SoC variations in both HV and LV batteries. To address this, recent studies have explored secondary-side control strategies, such as PWM and phase shift modulation of synchronous rectifiers, to extend voltage gain and improve soft-switching performance across broader operating ranges [9], [10].

To meet requirements of high-voltage gain, galvanic isolation, and high-power and high-current capability, most APM implementations rely on half-bridge (HB) or full-bridge (FB) topologies. Phase-shifted FB (PSFB) converters are widely adopted due to their ability to achieve zero-voltage switching (ZVS) using phase shift control and transformer parasitics [11]. PSFB designs face several limitations at light load, including loss of ZVS, load-dependent delay times, and increased rms and circulating currents.

In response, a range of enhancements has been proposed. Auxiliary soft-switching networks [12], digital active EMI filters [13], and planar magnetics [14], [15] have been explored to improve power density and performance. Synchronous rectification (SR) is commonly used to reduce conduction losses. When implemented with FB switching on the secondary side, the resulting topology is known as a dual active bridge (DAB), which enables bidirectional power flow and flexible control [16], [17]. Additional variations, such as reconfigurable current-fed converters [18] and three-phase DABs [19], [20], have been proposed to support ultrawide input voltage operation and improve fault tolerance. Nevertheless, both single- and three-phase DAB topologies suffer from hard switching at turn off, causing efficiency penalties and EMI concerns that can impact the LV bus connected to sensitive electronics.

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A two-stage topology involving an interleaved buck front-end followed by a dc transformer (DCX) stage has been proposed to address switching losses, particularly on the LV side. This configuration enables wide voltage regulation in the buck stage and zero-current switching (ZCS) in the DCX [21]. While this two-stage approach effectively eliminates most switching losses in the DCX stage, it might impact overall power density.

In [22], a novel SR driving method is proposed for a single-stage HB *LLC* converter used in APM applications. This approach controls the secondary-side switches using optimized turn-on and turn-off delays based on 3-D lookup tables. However, conduction loss remains a major contributor to power loss in this topology. To reduce conduction losses in *LLC* converters across wide operating voltage ranges, various hybrid control modes are analyzed in [23]. These modes aim to improve efficiency across input voltage ranges from 300 to 430 V and load ranges from 10% to 100%. However, most of these APM designs are still based on single-phase topologies.

Multiphase architectures offer advantages such as improved efficiency and distributed conduction losses under varying load conditions [24]. Moreover, the reliability of the 12-V supply is critical due to safety-relevant loads [25], and hence, redundancy becomes an important feature of APMs for autonomous platforms. Multiphase resonant converters, however, face inherent challenges such as unbalanced loading and current sharing due to resonant tank component tolerances; even minor impedance mismatches can significantly impact performance [26], [27], [28]. Several approaches have been proposed to address this, such as the dual-loop control in a two-phase *LLC* converter [29], which improves load current distribution but introduces beat-frequency interactions and current ripple fluctuations. Moreover, due to unsynchronized frequencies, interleaving to reduce output current ripple is not feasible with this approach. Other methods, including dual duty cycle control [30] and passive current sharing techniques [31] and [32], offer partial solutions under specific and controlled operating conditions (e.g., near resonant frequency with limited voltage variations). However, these methods often lack a full active control mechanism, and their performance tends to degrade when operating over wider input/output voltage ranges, varying load conditions, and greater phase-to-phase mismatches.

A recent three-phase *LLC* converter proposed in [33] uses switch-controlled capacitors (SCCs) with the same resonant tank design on all phases to achieve precise impedance tuning and current balancing under all APM operating conditions. While this approach offers maximum scalability and redundancy, it comes at the expense of increased system complexity and cost due to the three-phase structure and the inclusion of SCC components in all phases.

To address these limitations, this work proposes a dual-phase *LLC* converter featuring a new asymmetrical resonant tank design that requires only a single SCC circuit. This approach maintains balanced load sharing and high efficiency across all operating conditions while improving power density and reducing cost and system complexity compared to

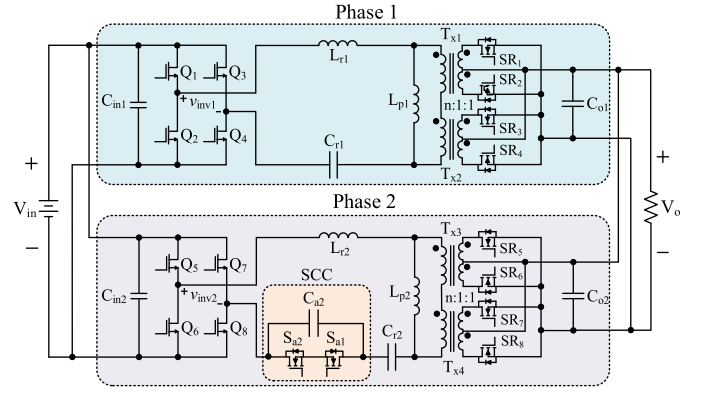


Fig. 1. Proposed dual-phase *LLC* dc-dc converter with one SCC circuit.

the three-phase design in [33]. The proposed design aligns with industry trends targeting high power density, efficiency, and reliable redundancy in next-generation APMs [34], [35], [36], [37].

The rest of this article is organized as follows. Section II introduces the proposed dual-phase *LLC* converter. Section III presents the design considerations and sensitivity analysis. Section IV discusses control implementation, followed by experimental verification using a full-scale proof-of-concept in Section V. Finally, this article is concluded in Section VI.

## II. PROPOSED DUAL-PHASE *LLC* DC-DC CONVERTER FOR APM APPLICATIONS

The impedances of the resonant tanks in multiphase resonant converters dictate the current distribution between the parallel phases. A phase with a resonant tank of larger impedance at a certain frequency will carry less output current. Conversely, an SCC circuit can only reduce the equivalent resonant capacitance compared to the original design. Therefore, the SCC circuit can only increase the output current in a given phase.

Fig. 1 illustrates the proposed two-phase *LLC* converter with an SCC circuit on phase 2. A crucial aspect of the design procedure for the proposed converter is ensuring that, when the SCC circuit is inactive (i.e.,  $C_{a2}$  is shorted), phase 2 always carries a smaller share of output current. When the SCC circuit is operational, phase 2's load needs to be increased to achieve balanced current sharing across all operating points. For manufacturing convenience, the magnetics are designed with equal values (i.e.,  $L_{r1} = L_{r2}$  and  $L_{p1} = L_{p2}$ ), with the resonant capacitance of phase 2 chosen to be larger than that of phase 1 (i.e.,  $C_{r2} > C_{r1}$ ).

The first step in the design procedure involves selecting the transformer turn ratio and the resonant tank parameters of phase 1 for the half-load condition. As mentioned, the resonant inductors of phase 2 are kept identical to those of phase 1. However, the resonant capacitor for phase 2 must be designed such that the impedance of phase 2 (without the SCC capacitor) is higher than that of phase 1, yet becomes lower when the SCC capacitor is connected in series, across the intended switching frequencies. Subsequently, the SCC capacitor is carefully sized to achieve impedance matching under

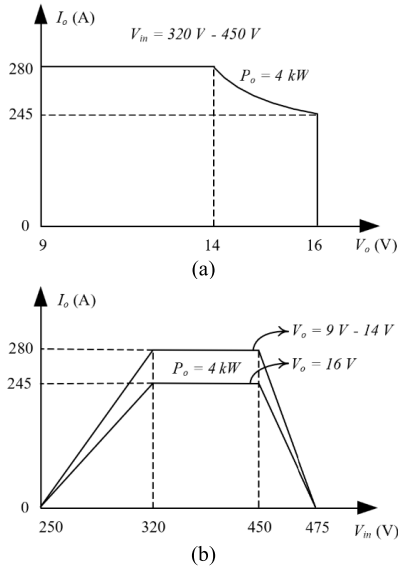


Fig. 2. Output current and power requirements of typical APMs. (a) Versus output voltage. (b) Versus input voltage.

all operational conditions, considering component tolerances. The main requirements and the overall design procedure for the proposed converter are detailed later in this section.

The design specifications for the EV APM are illustrated in Fig. 2 and are aligned with those of commercial products [34], [35], [36], [37]. The target input voltage range is 250–475 V, and the output voltage range is 9–16 V. The converter provides continuous rated output current over the input voltage range of 320–450 V and the output voltage range of 9–14 V. For output voltages between 14 and 16 V, the output current derates to maintain a constant output power of 4 kW. The output current and voltage characteristics of the dc–dc converter are shown in Fig. 2(a).

For input voltages below 320 V and above 450 V, a linear derating feature is implemented, reducing output power from 4 kW to near zero. The derating begins at 280 A for output voltages of 9–14 V and at 245 A for an output voltage of 16 V. This feature is depicted in Fig. 2(b). In addition, when the output voltage varies between 14 and 16 V, the output current is limited by the rated output power. The rated operating condition is defined as a 320-V input voltage and a 14-V output voltage at a maximum load current of 285 A.

In this design, the resonant converter operates within a frequency range of 200–450 kHz to enable miniaturization. GaN switches are utilized for the main switching bridge of each phase to maximize performance across the operating range. The transformer's turn ratio is determined following conventional design approaches. Since most of the operating range is desired to remain below the series resonant frequency (i.e.,  $f_r$ ), the resonant frequency, where the *LLC* tank's voltage gain equals unity, is set for the maximum input voltage and minimum output voltage

$$n = N_p/N_s = V_{in\_max}/V_{o\_min} \quad (1)$$

where  $N_p$  and  $N_s$  are the transformer's primary and secondary number of turns, respectively.

The transformer turn ratio is designed for a normalized gain of 0.9 instead of 1. This choice helps minimize primary-side circulating current, which is critical given the wide input and output voltage ranges of the EV dc–dc converter. This adjustment ensures that the switching frequency can rise above resonance to meet the highest input and lowest output voltage conditions. For a maximum input voltage of 450 V and a minimum output voltage of 9 V, the equivalent transformer turn ratio is calculated as  $0.9 \times (450/9) = 45$ .

In high-current applications, it is common to use two or more center-tapped transformers with series primary windings and parallel secondary windings. This configuration helps distribute the large output current and reduces conduction losses. For this design, two center-tapped transformers are planned for each phase, leading to a final turn ratio of 44. Each transformer will have a turn ratio of  $n:1:1 = 22:1:1$ . The remainder of this article details the resonant tank design for phase 1 (without SCC) and phase 2 (with SCC).

### III. DESIGN CONSIDERATIONS FOR THE PROPOSED DUAL-PHASE *LLC* DC–DC CONVERTER

#### A. Design of the Resonant Components in the Phase Without SCC Circuits

In phase 1, the designed parameters include  $L_{r1}$ ,  $C_{r1}$ , and  $L_{m1}$ . These parameters are designed following conventional *LLC* converter methodologies. The design objective is to ensure the desired frequency range is met, along with all input/output voltage and load regulations while minimizing circulating current on the primary side of the transformers, as detailed in [33].

Identifying key operating corner cases at rated power is essential for properly sizing the *LLC* tank components. The maximum voltage gain occurs at an output of 16 V and a load of 122.5 A with a 320-V input, corresponding to a gain of 2.20. In contrast, the worst case scenario for achieving ZVS corresponds to the full load of 140 A and a nominal output of 14 V, also with a 320-V input, resulting in a gain of 1.93. The minimum voltage gain is observed at a 9-V output and 140-A load with a 450-V input, yielding a gain of 0.88. These critical operating points are summarized in the following for clarity.

1) *Maximum Voltage Gain*:  $44 \times 16/320 = 2.2$ .

2) *ZVS-Critical Voltage Gain*:  $44 \times 14/320 = 1.93$ .

3) *Minimum Voltage Gain*:  $44 \times 9/450 = 0.88$ .

The design process is based on the well-known first harmonic approximation (FHA) method, followed by fine-tuning the parameters using PSIM simulation results to account for higher order harmonics. It should be noted that the voltage gain determined using FHA is lower than the actual gain at switching frequencies far from the resonant frequency.

For this design, the desired resonant frequency is set between 450 and 500 kHz. A relatively small quality factor ( $Q = 0.3$ ) is selected for the worst case scenario to accommodate the wide input/output voltage and load range. In addition, a large inductance ratio ( $L_p/L_r = 6$ ) is chosen to reduce circulating currents. The final resonant tank parameters for phase 1 are summarized in Table I.

TABLE I  
PARAMETERS OF PHASE 1 OF THE PROPOSED CONVERTER

Parameters	Values
$L_r$ inductance	15 $\mu\text{H}$
$L_p$ inductance	90 $\mu\text{H}$
$C_r$ capacitance	8 nF
Transformer turn ratio ( $n$ :1:1)	22:1:1

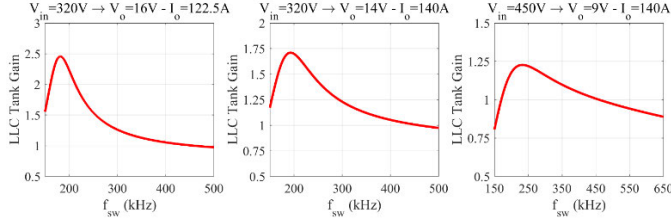


Fig. 3. Plot of voltage gain versus switching frequency at different operating conditions.

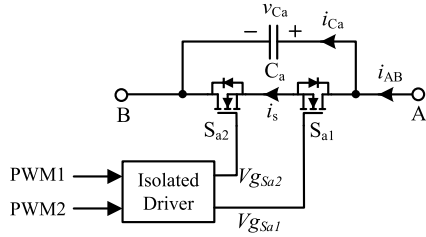


Fig. 4. Structure of the full-wave SCC circuit.

Fig. 3 illustrates the voltage gain curves for various operating conditions. As shown, a voltage gain of 2.2 is achievable for the maximum gain condition [see Fig. 3(a)], and a voltage gain of 0.88 is attainable for the minimum gain condition [see Fig. 3(c)]. As mentioned earlier, the most challenging gain to achieve is for the nominal condition at rated power, as shown in Fig. 3(b). Although the required gain of 1.93 is not achieved using FHA, simulation results indicate that the designed resonant parameters can achieve a voltage gain greater than 1.93.

### B. Overview of the Principles of the Full-Wave SCC Circuit

The SCC circuit is shown in Fig. 4, and its operation is illustrated in Fig. 5. Assuming that a sinusoidal current  $I_{AB}$  flows through the SCC circuit from node A to node B, as shown in Fig. 5, the current zero-crossing points occur at angles 0,  $\pi$ ,  $2\pi$ , and so on.

During the positive half-cycle,  $S_1$  is turned off at an angle of  $2n\pi + \alpha$ . After  $S_1$  is turned off, the current flows from node A to node B via  $C_a$  and charges the capacitor until the next current zero-crossing point at  $(2n + 1) \times \pi$ . Then, the current reverses direction and begins to discharge  $C_a$ . Once  $C_a$  is fully discharged, the negative current is about to flow from node B to node A through the body diode of  $S_1$ . To prevent the body diode from conducting,  $S_1$  is turned on. It remains on for the rest of the cycle and is turned off again at an angle  $(2n + 2) \times \pi + \alpha$ . Following the same procedure,  $S_2$  controls the negative half-cycle.

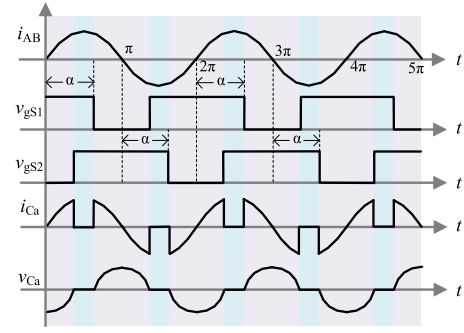


Fig. 5. Typical waveform of the full-wave SCC circuit.

The equivalent capacitance of the SCC circuit, when  $C_a$  is modulated by angle  $\alpha$ , is defined as follows:

$$C_{\text{SCC}} = \frac{C_a}{2 - \frac{(2\alpha - \sin(2\alpha))}{\pi}} \quad (2)$$

where  $C_a$  is the SCC capacitor. The equivalent resulting resonant capacitance can be derived as follows:

$$C_{r\text{-eq}} = \frac{C_{\text{sc}} C_r}{C_{\text{sc}} + C_r} \quad (3)$$

where  $C_r$  is the series resonant capacitor. Based on the above two equations, the equivalent resonant capacitance can be rewritten as follows:

$$C_{r\text{-eq}} = \frac{\pi C_a C_r}{\pi C_a + 2\pi C_r - 2\alpha C_r + C_r \sin(2\alpha)}. \quad (4)$$

When the angle  $\alpha$  ranges from  $\pi/2$  to  $\pi$ , the equivalent capacitance transitions from its minimum to maximum value. In the extreme case where  $\alpha = \pi/2$ , the current  $I_{AB}$  flows through  $C_a$  and bypasses SCC MOSFETs. As a result, the equivalent resonant capacitance reaches its minimum value, which is equal to  $C_r$  and  $C_a$  connected in series. Conversely, when  $\alpha = \pi$ , current  $I_{AB}$  will flow through SCC MOSFETs, bypassing capacitor  $C_a$ , and the equivalent resonant capacitance reaches its maximum value, which is equal to  $C_r$ .

It should be mentioned that the additional loss from the SCC MOSFETs (i.e.,  $S_{a1}$  and  $S_{a2}$ ) is not significant, since these switches block the SCC capacitor voltage and hence operate under ZVS conditions. Therefore, conduction loss primarily governs their selection, representing a tradeoff between efficiency impact and component cost.

### C. Design of the Resonant Components in the Phase With Full-Wave SCC Circuits

In phase 2, the magnetics are identical to those in phase 1 (i.e.,  $L_{r2} = L_{r1}$  and  $L_{p2} = L_{p1}$ ), and therefore, only the resonant capacitance  $C_{r2}$  and the SCC capacitance  $C_{a2}$  need to be designed. The design criteria ensure that the voltage gain of phase 2 remains below that of phase 1 over the entire switching frequency range and under all operating conditions. Both capacitances are designed based on the operating principles of the SCC circuit.

By modulating the full-wave SCC phase angle, the equivalent resonant capacitance in phase 2 is adjusted, which in turn modifies the impedance of phase 2. When the phase angle is

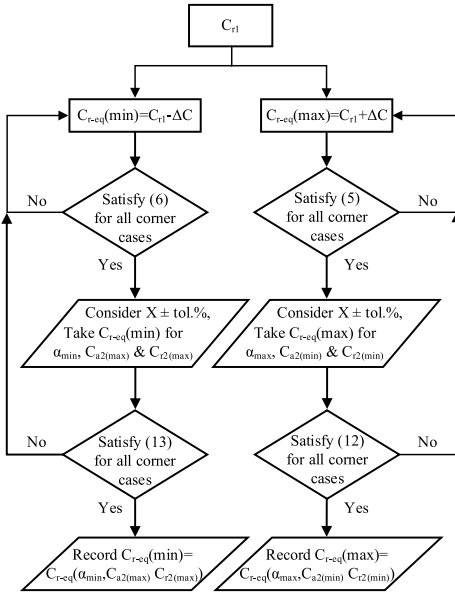


Fig. 6. Flowchart illustrating the selection of maximum and minimum equivalent resonant capacitances.

set to a specific value between its minimum and maximum, the impedance of phase 1 matches that of phase 2, achieving current sharing. If the phase angle increases, the impedance of phase 2 increases, causing phase 2 to carry a smaller share of the current. Conversely, if the phase angle decreases, the impedance of phase 2 decreases, causing phase 2 to carry a larger share of the current.

The design criteria can be summarized as follows.

1) *Maximum Phase Angle*: When  $\alpha$  is at its maximum value, under any component tolerances or operating conditions, phase 2 must carry less current than phase 1.

2) *Minimum Phase Angle*: When  $\alpha$  is at its minimum value, under any component tolerances or operating conditions, phase 2 must carry more current than phase 1.

Component tolerances are the primary factor causing impedance mismatch and current imbalance, which is compensated for by the SCC circuit. In this design,  $\pm 5\%$  tolerances are considered for all resonant elements and the SCC capacitor. The two design criteria mentioned above can be expressed as follows:

$$I_{o2}(M, f_{sw}, L_{p2}, L_{r2}, C_{r-eq}(\alpha=\max)) < I_{o1}(M, f_{sw}, L_{p1}, L_{r1}, C_{r1}) \quad (5)$$

$$I_{o2}(M, f_{sw}, L_{p2}, L_{r2}, C_{r-eq}(\alpha=\min)) > I_{o1}(M, f_{sw}, L_{p1}, L_{r1}, C_{r1}) \quad (6)$$

where  $I_{o1}$  and  $I_{o2}$  are the output currents of phases 1 and 2, respectively;  $M$  is the LLC tank voltage gain;  $f_{sw}$  is the switching frequency that is intended to be identical for both phases; and  $C_{r-eq}(\alpha=\max)$  and  $C_{r-eq}(\alpha=\min)$  represent the maximum and minimum equivalent capacitances when  $\alpha$  values are at their maximum (e.g.,  $\pi$ ) and minimum (e.g.,  $\pi/2$ ), respectively. It should be noted that the values of  $M$  and their corresponding switching frequencies  $f_{sw}$  must satisfy inequalities (5) and (6) for different corner cases. The equivalent

TABLE II  
DESIGNED PARAMETERS OF THE DUAL-PHASE  
LLC DC – DC CONVERTER

Parameters	Phase 1	Phase 2
$L_r$ inductance	15 $\mu$ H	15 $\mu$ H
$L_p$ inductance	90 $\mu$ H	90 $\mu$ H
$C_r$ capacitance	8 nF	11 nF
$C_a$ capacitance	-	9.5 nF

resonant capacitance  $C_{r-eq}$  satisfies

$$\frac{C_{r2}C_{a2}}{C_{r2} + C_{a2}} < C_{r-eq}(\alpha=\min) < C_{r-eq} < C_{r-eq}(\alpha=\max) < C_{r2}. \quad (7)$$

When components' tolerances are considered, the following inequations can be found in (8)–(11), as shown at the bottom of the next page, where the subscripts  $_{\min}$  and  $_{\max}$  denote the minimum and maximum values of the associated variables due to component tolerances, respectively.  $C_{r-eq}(\alpha=\max, C_{a2}=\min, C_{r2}=\min)$  represents the equivalent resonant capacitance when  $\alpha$  is at its maximum,  $C_{a2}$  is minimum, and  $C_{r2}$  is at its minimum. Similarly,  $C_{r-eq}(\alpha=\min, C_{a2}=\max, C_{r2}=\max)$  represents the equivalent resonant capacitance when  $\alpha$  is at its minimum,  $C_{a2}$  is at its maximum, and  $C_{r2}$  is at its maximum.

It is important to note that increasing the value of any component in a passive impedance network increases the total impedance, and a larger impedance results in a smaller output current. Therefore, the two criteria can be identified in (14) and (15), where  $X_{\max} = 1.05 \times X$  and  $X_{\min} = 0.95 \times X$  considering  $\pm 5\%$  tolerances. Here,  $X$  represents  $L_{p1}$ ,  $L_{p2}$ ,  $L_{r1}$ ,  $L_{r2}$ ,  $C_{r1}$ ,  $C_{r2}$ , and  $C_{a2}$ . The two equivalent capacitances  $C_{r-eq}(\alpha=\max, C_{a2}=\min, C_{r2}=\min)$  and  $C_{r-eq}(\alpha=\min, C_{a2}=\max, C_{r2}=\max)$ , which satisfy the design criteria, are determined first.

The selection process for the maximum and minimum equivalent resonant capacitor values for phase 2 is illustrated in the flowchart shown in Fig. 6.

The current sharing performance deteriorates at heavy loads and is less influenced by the voltage gain. Therefore, initial values are obtained using the FHA method and subsequently fine-tuned through PSIM simulations. The two equivalent capacitances are first determined under the heaviest load at the nominal voltage gain and then verified and adjusted for other corner cases. After several iterations, the capacitance values are incrementally increased or decreased based on standard capacitor value steps (i.e.,  $\Delta C$ ), until the final values for the two equivalent capacitances are established as follows:

$$C_{r-eq}(\alpha=\max, C_{a2}=\min, C_{r2}=\min) = 10 \text{ nF} \quad (14)$$

$$C_{r-eq}(\alpha=\min, C_{a2}=\max, C_{r2}=\max) = 6 \text{ nF}. \quad (15)$$

Using the expression for the equivalent resonant capacitance, PSIM simulations, and accounting for the minimum and maximum  $\alpha$  angles,  $C_{r2}$  and  $C_{a2}$  are designed as  $C_{r2} = 11 \text{ nF}$  and  $C_{a2} = 9.5 \text{ nF}$ , respectively.

The final LLC parameters are summarized in Table II.

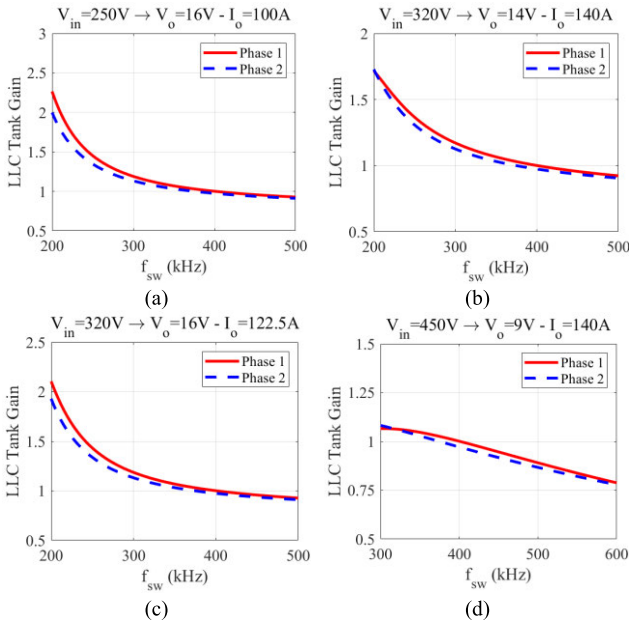


Fig. 7. Voltage gain comparison of the proposed two-phase design for different operating conditions considering  $L_{r1} + 5\%$ ,  $L_{p1} + 5\%$ ,  $C_{r1} + 5\%$ ,  $L_{r2} - 5\%$ ,  $L_{p2} - 5\%$ ,  $C_{r2} - 5\%$ ,  $C_{a2} - 5\%$ , and  $\alpha = 160^\circ$ . (a)  $V_{in} = 250$  V to  $V_o = 16$  V and  $I_o = 100$  A. (b)  $V_{in} = 320$  V.

#### D. Component Tolerance Analysis of the Designed Parameters

To verify that the designed parameters meet the desired tolerances, an analysis was conducted. Fig. 7 illustrates the voltage gain comparison of the two-phase converter, considering a 5% increase in the resonant components of tank 1 and a 5% decrease in the resonant components of tank 2, including the SCC capacitor. In this scenario, the SCC phase angle  $\alpha$  is kept at its maximum to ensure that the voltage gains of phase 2 remain smaller than those of phase 1 under all operating conditions. From Fig. 7, it can be observed that the condition specified in (14) is satisfied across the input/output voltage range at rated power operation. It is worth noting that the minimum input voltage to maximum output voltage range (i.e., 250–16 V) is not a system-level requirement for the EV dc–dc converter; it is shown here to demonstrate the capability of the two-phase SCC-LLC converter.

Fig. 8 illustrates the voltage gain comparison of the two-phase converter, considering a 5% decrease in the resonant components of tank 1 and a 5% increase in the resonant components of tank 2, including the SCC capacitor. In this scenario, the SCC phase angle  $\alpha$  is kept at its minimum to ensure that the voltage gains of phase 2 remain larger than

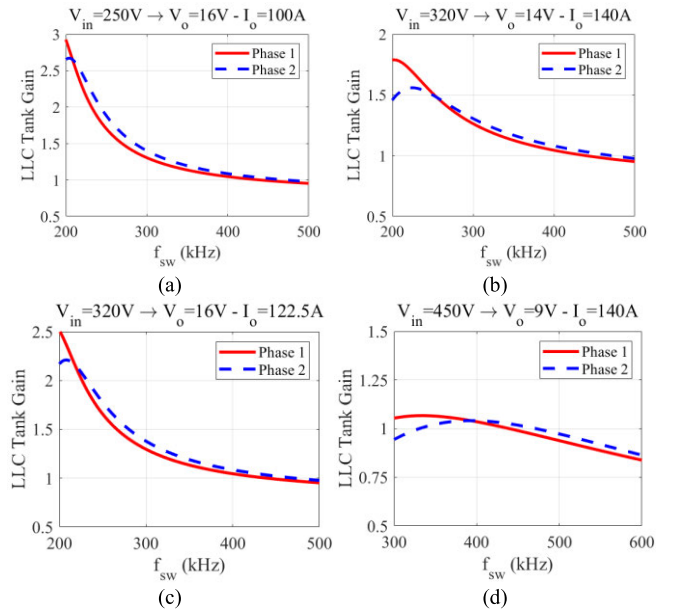


Fig. 8. Voltage gain comparison of the proposed two-phase design for different operating conditions considering  $L_{r1} - 5\%$ ,  $L_{p1} - 5\%$ ,  $C_{r1} - 5\%$ ,  $L_{r2} + 5\%$ ,  $L_{p2} + 5\%$ ,  $C_{r2} + 5\%$ ,  $C_{a2} + 5\%$ , and  $\alpha = 100^\circ$ .

those of phase 1 under all operating conditions. From Fig. 8, it can be observed that the condition specified in (15) is satisfied across the input/output voltage range at rated power operation.

Both Figs. 7 and 8 demonstrate the impedance matching capability and current sharing performance of the proposed design method over a wide range of input/output voltage conditions, even under maximum phase-to-phase mismatch for resonant tank component tolerance variations.

#### IV. CONTROL IMPLEMENTATION

The overall control scheme of the proposed dual-phase LLC dc–dc converter for APM applications is shown in Fig. 9. In this control design, the output current of each phase is sensed and transmitted via a serial peripheral interface (SPI) and digital isolator to the control board for closed-loop current control. The output voltage is also communicated through the same SPI interface for closed-loop voltage regulation. In addition, the input voltage is monitored to enable overvoltage protection (OVP) and undervoltage lockout (UVLO), which control the enabling and disabling of the PWM signals for the primary bridges.

The resonant currents are measured using small current transformers to implement overcurrent protection (OCP).

$$I_{o1}(M, f_{sw}, L_{p1}, L_{r1}, C_{r1}) \leq I_{o1}(M, f_{sw}, L_{p1(\min)}, L_{r1(\min)}, C_{r1(\min)}) \quad (8)$$

$$I_{o1}(M, f_{sw}, L_{p1}, L_{r1}, C_{r1}) \geq I_{o1}(M, f_{sw}, L_{p1(\max)}, L_{r1(\max)}, C_{r1(\max)}) \quad (9)$$

$$I_{o2}(M, f_{sw}, L_{p2}, L_{r2}, C_{r-\text{eq}}(\alpha=\max)) \leq I_{o2}(M, f_{sw}, L_{p2(\min)}, L_{r2(\min)}, C_{r-\text{eq}}(\alpha=\max, C_{a2}=\min, C_{r2}=\min)) \quad (10)$$

$$I_{o2}(M, f_{sw}, L_{p2}, L_{r2}, C_{r-\text{eq}}(\alpha=\min)) \geq I_{o2}(M, f_{sw}, L_{p2(\max)}, L_{r2(\max)}, C_{r-\text{eq}}(\alpha=\min, C_{a2}=\max, C_{r2}=\max)) \quad (11)$$

$$I_{o2}(M, f_{sw}, L_{p2(\min)}, L_{r2(\min)}, C_{r-\text{eq}}(\alpha=\max, C_{a2}=\min, C_{r2}=\min)) < I_{o1}(M, f_{sw}, L_{p1(\max)}, L_{r1(\max)}, C_{r1(\max)}) \quad (12)$$

$$I_{o2}(M, f_{sw}, L_{p2(\max)}, L_{r2(\max)}, C_{r-\text{eq}}(\alpha=\min, C_{a2}=\max, C_{r2}=\max)) > I_{o1}(M, f_{sw}, L_{p1(\min)}, L_{r1(\min)}, C_{r1(\min)}) \quad (13)$$

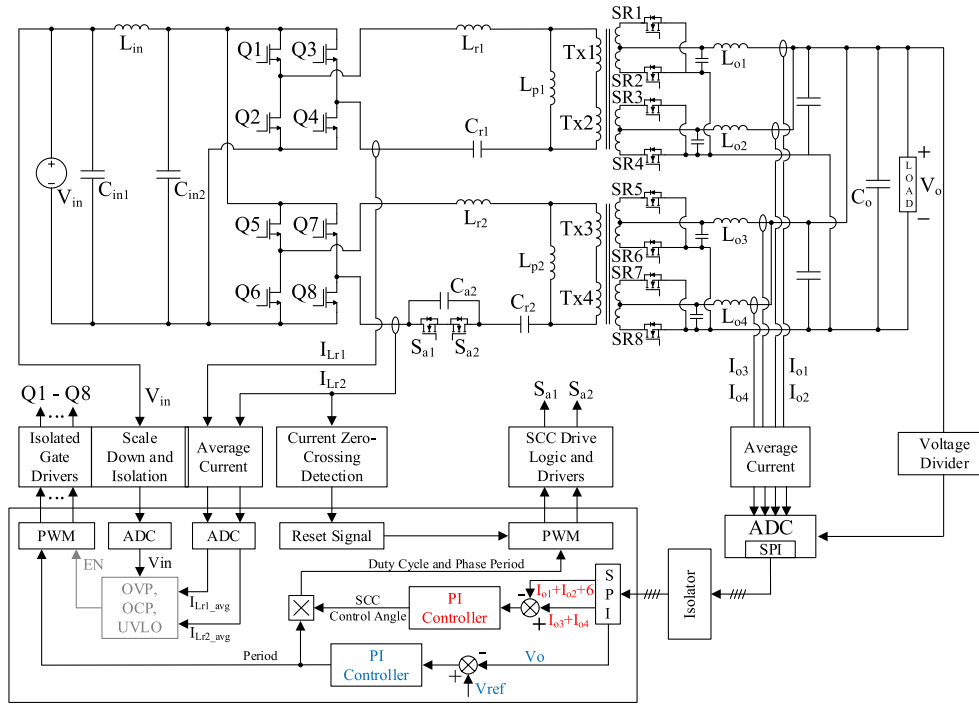


Fig. 9. Overall control scheme of the proposed dual-phase *LLC* dc-dc converter.

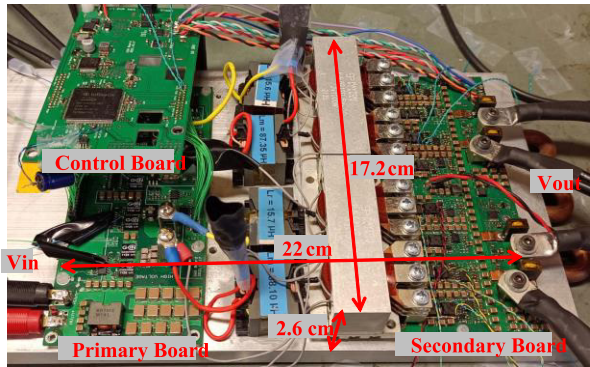


Fig. 10. Implemented 4-kW dc-dc converter laboratory prototype.

Furthermore, the resonant current of phase 2 is also used to synchronize and reset the SCC gate pulse during every switching cycle. Due to hysteresis and the jump in current difference when  $I_{o2}$  approaches  $I_{o1}$ , the current-loop control deliberately maintains  $I_{o2}$  at 6 A higher than  $I_{o1}$ . This offset is influenced by the resolution of the PWM and ADC modules in the implemented MCU.

The output of the outer current-loop PI controller determines the duty cycle of the SCC MOSFETs, while the output of the inner voltage-loop PI controller defines the period of the primary-side switches. Both control variables are essential for calculating the SCC circuit's turn-on time (i.e.,  $\alpha$ ), which enables dynamic adjustment of the equivalent resonant capacitance in phase 2 to achieve impedance matching and current sharing within the defined operational criteria.

If the phase 2 current plus the offset exceeds the phase 1 current, the controller increases  $\alpha$ , which raises the impedance of phase 2 and reduces its load share. Conversely, if the

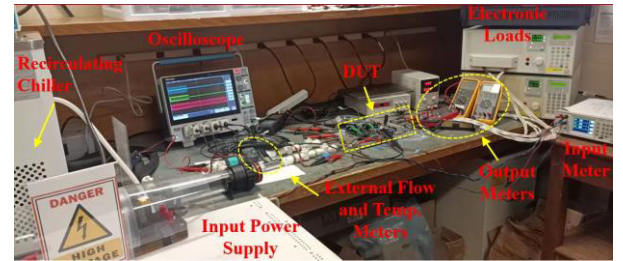


Fig. 11. Performance validation of the DUT using a controlled liquid cooling system.

phase 2 current plus the offset is lower than the phase 1 current, the controller decreases  $\alpha$ , reducing the impedance of phase 2, thereby increasing its load share.

A limiter is applied to the output of the voltage-loop to constrain the switching frequency between the expected operating range of 200 and 450 kHz, ensuring the converter operates within the inductive region and avoids instability in the capacitive region. For the SCC's  $\alpha$  angle, a constraint is also applied between  $100^\circ$  and  $160^\circ$  to utilize the effective capacitance modulation region and avoid slow capacitance variation near  $180^\circ$ .

Another feature of the control implementation is phase management under varying load conditions. Only phase 1 is enabled under light-load conditions, while phase 2 is activated above a certain load to distribute current more effectively. A hysteresis band is incorporated to prevent rapid toggling of phase 2 near the threshold value. The phase transition mechanism operates as follows. When transitioning from single-phase to dual-phase operation (i.e., when  $I_o > 120$  A), the primary switches of phase 2 are activated, and its current-loop PI controller is initialized and enabled to

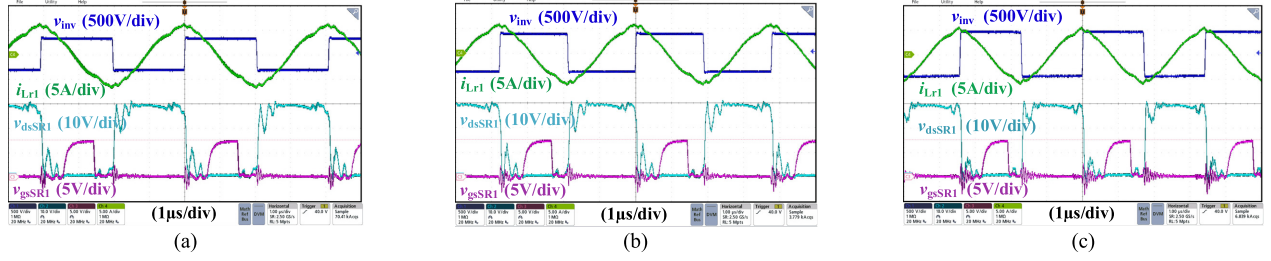


Fig. 12. Experimental results of the single-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 14$  V, and  $I_o = 10$  A; (b)  $V_{in} = 380$  V,  $V_o = 14$  V, and  $I_o = 10$  A; and (c)  $V_{in} = 450$  V,  $V_o = 14$  V, and  $I_o = 10$  A.

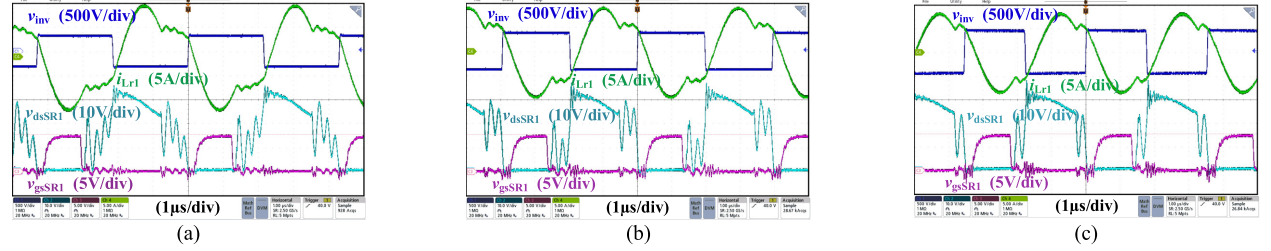


Fig. 13. Experimental results of the single-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 14$  V, and  $I_o = 140$  A; (b)  $V_{in} = 380$  V,  $V_o = 14$  V, and  $I_o = 140$  A; and (c)  $V_{in} = 450$  V,  $V_o = 14$  V, and  $I_o = 140$  A.

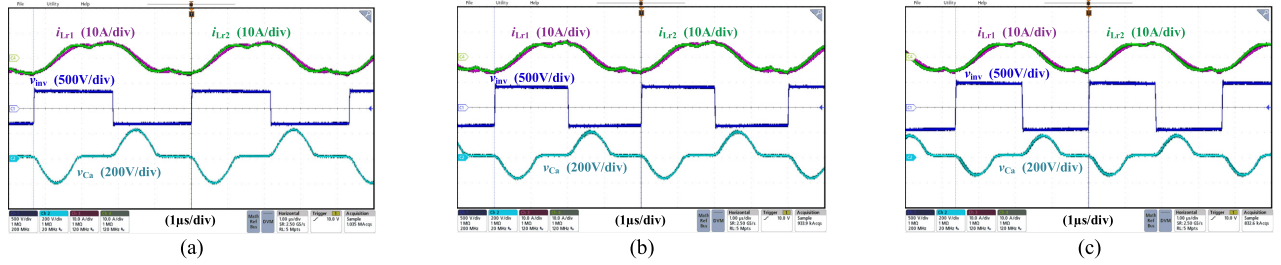


Fig. 14. Experimental results of the two-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 14$  V, and  $I_o = 100$  A; (b)  $V_{in} = 380$  V,  $V_o = 14$  V, and  $I_o = 100$  A; and (c)  $V_{in} = 450$  V,  $V_o = 14$  V, and  $I_o = 100$  A.

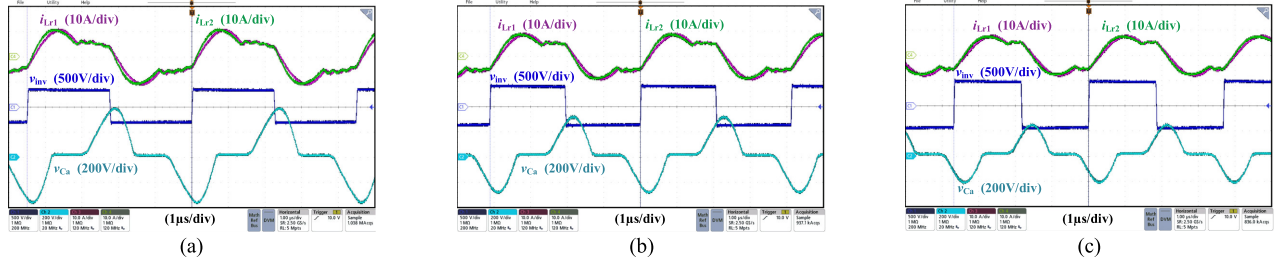


Fig. 15. Experimental results of the two-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 14$  V, and  $I_o = 280$  A; (b)  $V_{in} = 380$  V,  $V_o = 14$  V, and  $I_o = 280$  A; and (c)  $V_{in} = 450$  V,  $V_o = 14$  V, and  $I_o = 280$  A.

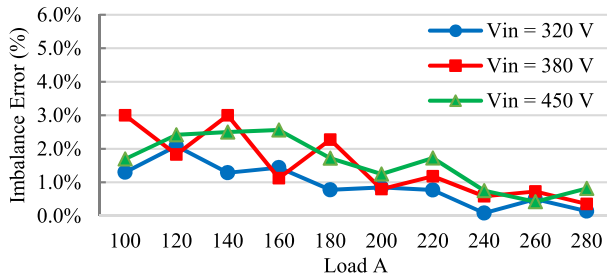


Fig. 16. Current sharing performance of the proposed two-phase SCC-LLC converter from 100 to 280 A.

achieve current sharing. Conversely, during a transition from dual-phase to single-phase operation (i.e., when  $I_o < 100$  A),

the primary switches of phase 2 are deactivated, and its current-loop is disabled.

## V. EXPERIMENTAL RESULTS

A 4-kW laboratory prototype is built to test the performance of the proposed two-phase SCC-LLC converter. The general system specifications used for the design of the prototype and the components used in the prototype are listed in Table III. Fig. 10 shows the 4-kW EV APM laboratory prototype that is mounted on a cold plate for proper thermal dissipation. The dimensions of the prototype are  $22 \times 17.2 \times 2.6$  cm resulting in a 4-kW/L power density.

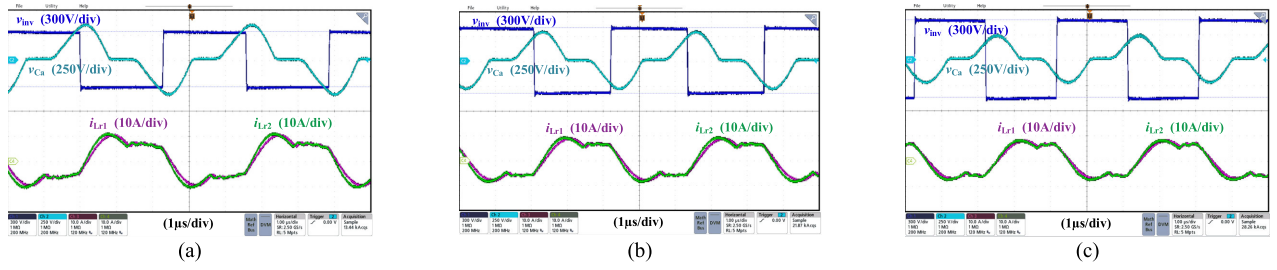


Fig. 17. Experimental results of the two-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 16$  V, and  $I_o = 240$  A; (b)  $V_{in} = 380$  V,  $V_o = 16$  V, and  $I_o = 240$  A; and (c)  $V_{in} = 450$  V,  $V_o = 16$  V, and  $I_o = 240$  A.

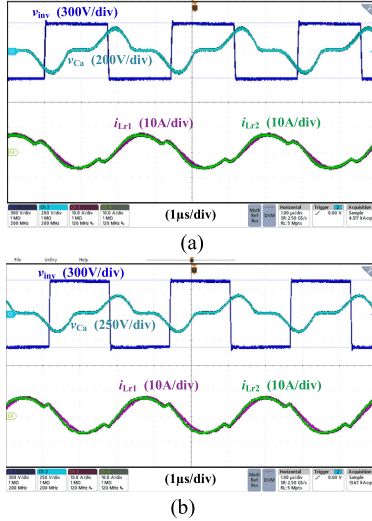


Fig. 18. Experimental results of the two-phase operation for (a)  $V_{in} = 320$  V,  $V_o = 9$  V, and  $I_o = 280$  A and (b)  $V_{in} = 380$  V,  $V_o = 9$  V, and  $I_o = 280$  A.

TABLE III

SYSTEM SPECIFICATIONS AND PARAMETERS OF EACH PHASE IMPLEMENTED IN THE EXPERIMENTAL SETUP

Parameters/Descriptions	Values/Part Number
Input voltage range	250 V – 475 V
Output voltage range	9 V – 16 V
Rated output voltage	14 V
Maximum output current	285 A
Maximum output power	4 kW (2 kW $\times$ 2)
Transformer	$n = 22:1:1$ , ( $\times$ 2)
Switching Frequency	210 kHz – 430 kHz
Parallel inductor	$L_{p1} = 85\mu\text{H}$ , $L_{p2} = 85\mu\text{H}$ , (PQ32/20 - 3C97)
Series inductor	$L_{r1} = 15\mu\text{H}$ , $L_{r2} = 15\mu\text{H}$ , (PQ32/20 - 3C97)
Series capacitor of phase 1	$C_{r1} = 8.1\text{nF}$ ( $4.7\text{nF} \times 4 + 6.8\text{nF} \times 2$ ), (CGA6M1C0G3A472J200AE $\times$ 4 + CGA6M1C0G3A682J200AE $\times$ 2)
Series capacitor of phase 2	$C_{r2} = 10.9\text{nF}$ ( $6.8\text{nF} \times 2 + 15\text{nF} \times 2$ ), (CGA6M1C0G3A682J200AE $\times$ 2 + C3225C0G3A153J250AC $\times$ 2)
SCC capacitor of phase 2	$C_{a2} = 9.4\text{nF}$ ( $4.7\text{nF} + 4.7\text{nF}$ ), (CGA6M1C0G3A472J200AE $\times$ 2)
Primary side switches	650V, 30A, (GS66508B $\times$ 4)
Secondary side switches	40V, 250A, (IAUA250N04S6N007AUMA1 $\times$ 8)
SCC switches	650V, 69A, (IPT65R033 $\times$ 2)
Output capacitor	620 $\mu\text{F}$ ( $10\mu\text{F} \times 31 \times 2$ ) + 180 $\mu\text{F}$ ( $10\mu\text{F} \times 18$ , (12105C106K4Z2A $\times$ 80)
Micro-controller	TC375TP96F300WAAKXUMA1

The final setup to test the 4-kW two-phase operation with a controlled liquid coolant temperature and flow rate is shown

in Fig. 11. The device under test (DUT) is connected to a cold plate, which is connected to the recirculating chiller that can control the temperature of the coolant to replicate the actual condition of the EV powertrain. In the testing, only water is used for the coolant with a flow of 3 L/min. The input power is measured using a Tektronix PA1000 precision power analyzer, the output voltage is measured using a Fluke 87-V digital multimeter, and the output current is measured using a 250- $\mu\Omega$  shunt resistor and a Fluke 87-V multimeter to read the voltage drop. Moreover, three electronic loads are used in parallel to share the maximum load.

First, a single-phase operation will be demonstrated, and then, two-phase testing will be shown. Finally, the phase transition between one- and two-phase operations will be shown to verify the performance during large step load changes.

The experimental waveforms obtained with closed voltage-loop operation for  $V_o = 14$  V and different input voltage levels at light-load conditions are shown in Fig. 12 and at full-load conditions are shown in Fig. 13. It can be observed that the *LLC* dc–dc converter is operating in the inductive region, and ZVS is achieved for the high-voltage primary-side switches and the output low-voltage MOSFETs are switching with ZCS conditions over a wide load range from 7% to 100%.

The experimental waveforms for two-phase operation at different input voltage levels with  $V_o = 14$  V are shown in Fig. 14 at  $I_o = 100$  A load and in Fig. 15 at  $I_o = 280$  A load. A load of 100 A represents the minimum load, at which two-phase operation will be maintained. To prevent frequent toggling between phases, a 20-A hysteresis band has been introduced. In every operating condition, the resonant currents in both phases are nearly identical, demonstrating well-balanced load sharing between the two phases.

Fig. 16 shows the variations in output current differences across the load range. The current difference remains within 5 A across various input voltage levels at  $V_o = 14$  V, ensuring accurate current balancing between the phases over the entire load range.

Figs. 17 and 18 illustrate the boundary LV battery voltage levels,  $V_o = 9$  V and  $V_o = 16$  V, for different HV battery voltage levels. In all these boundary conditions, precise current sharing is maintained, further confirming the robustness of the developed design and current balancing mechanism.

To verify smooth transitions between one- and two-phase operations, step load change tests were performed. Fig. 19(a) illustrates a step load change from 40 to 140 A. Initially,

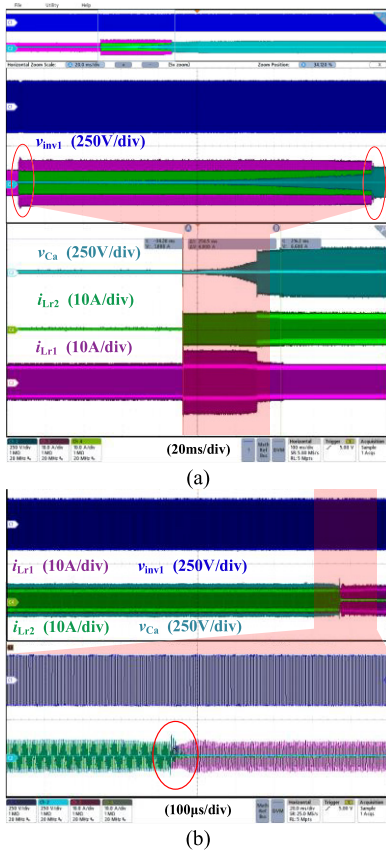


Fig. 19. Phase transition testing with  $V_{in} = 320$  V and  $V_o = 14$  V. (a) Load change from 40 to 140 A (from one-phase to two-phase transition) and (b) load change from 140 to 40 A (from two-phase to one-phase transition).

phase 1 carries the 40-A load. Immediately after the load increases, phase 2 begins to share the current, while the SCC capacitor voltage builds up. Within 250 ms, the load is balanced between the two phases. Notably, only a 2–3 A overshoot is observed in the resonant current of phase 1 during the balancing process, with no extra overshoot occurring at the transition points.

Fig. 19(b) illustrates a step load change from 140 to 40 A. In this case, both phases initially share the load. Once the load decreases to 40 A, the current in phase 2 drops to zero, accompanied by a slight overshoot on the SCC capacitor voltage, while phase 1 resumes carrying the entire load.

It should be noted that the target EV system includes a 12-V battery connected in parallel with the LV bus. As a result, high-frequency and high-magnitude transient currents are primarily supplied by the battery, minimizing stress on the APM.

The prototype was tested under different coolant temperatures for over 10 min to allow component temperatures to stabilize under nominal worst case conditions, specifically at the minimum HV battery voltage and rated current with a 14-V LV battery voltage. For brevity, only the results with a 65 °C coolant temperature are shown in Fig. 20. The temperature of the SRs reached 126 °C, and the GaNs reached 114 °C, both well below their maximum operating junction temperatures of 175 °C and 150 °C, respectively. This demonstrates that the implemented APM can reliably operate under these worst case conditions.

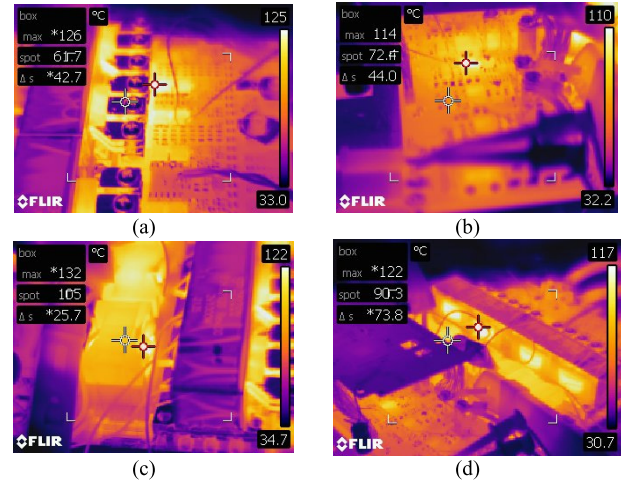


Fig. 20. Thermal images captured for two-phase operation with  $V_{in} = 320$  V,  $V_o = 14$  V, and  $I_o = 280$  A using only liquid cooling with a 65 °C coolant. (a) SR devices, (b) GaN and SCC devices, (c) parallel inductor, and (d) transformer.

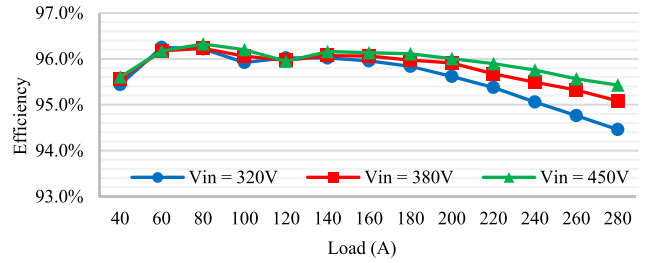


Fig. 21. Efficiency measurement results of the proposed two-phase SCC-LLC converter over the load range.

The efficiency curves of the prototype for various HV battery voltages at the rated LV battery voltage across the load range are illustrated in Fig. 21. It should be noted that phase shedding is employed here. At lighter loads, only phase 1 operates, and both phases begin operating together to share the load only when  $I_o > 120$  A. The average efficiencies for  $V_{in} = 320$  V,  $V_{in} = 380$  V, and  $V_{in} = 450$  V are calculated as 95.6%, 95.8, and 95.9%, respectively.

Table IV presents a comparison of key performance metrics for state-of-the-art dc–dc converters developed for APM applications, including both academic designs and commercial products. Most designs are based on a 400-V HV battery and all utilize a 12-V LV battery, with slight variations in voltage ranges. It can be observed that only a few studies have considered redundancy, which is essential for autonomous vehicles, a feature that has been adopted in recent commercial products from Vitesco [36] and Bosch [37]. The two-phase LLC converter in [29] employs different switching frequencies for each phase with a dual-loop control method to achieve current balancing without adding additional hardware cost. However, this approach is verified only for a fixed output voltage, with a power density of 1 kW/L and a full-load efficiency of 93%. Among the reviewed designs, the three-phase LLC converter in [33] demonstrates the highest peak and full-load efficiency, along with a respectable power density of 3 kW/L. However, its high component count and use of SCC circuits on

TABLE IV  
COMPARISON OF THE PROPOSED DUAL-PHASE *LLC* DC–DC CONVERTER WITH THE STATE-OF-THE-ART APM SOLUTIONS

APM Topology / Unit	Input voltage	Output voltage	Rated Power	Peak Efficiency	Full-Load Efficiency	Switching Frequency	Redundancy
FSFB [12]	300V	12V	2 kW	94 %	93 %	220 kHz - 300 kHz	No
FSFB [14]	220V-475V	8V-14.5V	3.6 kW	N/A	87 %	150 kHz	No
FSFB [15]	400V-800V	13V-15V	2.1 kW	95.1 %	94.7 %	200 kHz	No
DAB [18]	180V-900V	6V-16V	3.2 kW	95 %	94.5 %	~80 kHz	No
Interleaved Buck + DCX [21]	220V-475V	10V-16V	4 kW	96.2 %	90 %	100 kHz - 500kHz + 200kHz	No
1-phase LLC [22]	220V-450V	6.5V-16V	2.5 kW	93.2 %	91 %	90 kHz - 200 kHz	No
2-phase LLC [29]	330V-410V	14V	2.5 kW	95 %	93 %	~160 kHz - ~250 kHz	Yes
3-Phase LLC [33]	250V-430V	9V-16V	3.8 KW	96.7 %	95.8 %	260 kHz - 400 kHz	Yes
Bel 350DNC40-12 [34]	240V-430V	9V-16V	4 kW	93 %	N/A	N/A	No
Bursa BSC624-12 [35]	220V-450V	8V-16V	3.5 kW	94.4 %	N/A	N/A	No
Vitesco [36]	245V-450V	8V-16V	3.6 kW	N/A	N/A	N/A	Yes
Bosch [37]	250V-475V	10.5V-15.5V	3.6 kW	95 %	N/A	N/A	Yes
This Work	250V-475V	9V-16V	4 kW	96.3 %	95.1 %	210 kHz - 430 kHz	Yes

all phases reduce its power density and contribute to increased system cost.

The proposed solution builds upon the design in [33], offering a more balanced tradeoff across key performance metrics. It achieves high efficiency (>96% peak) and a power density of 4 kW/L while minimizing the use of additional SCC components through a new asymmetrically designed dual-phase architecture. Notably, the proposed design also outperforms the two-phase *LLC* converter in [29] in terms of both peak and full-load efficiency as well as power density.

## VI. CONCLUSION

A novel resonant tank design approach for a two-phase SCC-*LLC* converter is proposed for APM applications, reducing the cost and complexity of conventional multiphase *LLC* converters, where each phase requires an SCC circuit, increasing both cost and current balancing control complexity. In the new approach, only one SCC circuit is used on one phase, enabling current sharing over a wide input and output voltage range. The impedance of the phase with an SCC circuit is intentionally designed to be smaller than that of the phase without an SCC across the operating range, allowing impedance matching over the operating point using the SCC

circuit. The design accounts for a maximum phase-to-phase mismatch resulting from  $\pm 5\%$  component tolerances, ensuring high fidelity and reliability in practical implementation. A 4-kW EV APM dc–dc converter prototype demonstrated current balancing within a 5 A set limit, achieving a power density of 4 kW/L and a peak efficiency of 96.3% under maximum coolant temperature.

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