Adaptive Current Source Drivers for Efficiency Optimization of High Frequency Synchronous Buck Converters*

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Abstract **– In this paper, the concept of the adaptive CSDs is proposed for high frequency synchronous buck converters. The idea of the adaptive CSDs is to achieve optimal design of the switching loss reduction and the drive loss reduction for wide load range. It should be noted that the adaptive concept is suitable for both the continuous and discontinuous CSDs regardless the drive circuit topologies. Through investigating the CSD circuits, one simple method to achieve the adaptive drive current based on the adaptive voltages is proposed. The linear regulator can be used to achieve the function of the adaptive voltages and drive currents in a cost-effective manner. A 12V input, 1.3V output and 1MHz synchronous buck converter was built to verify the advantages of the proposed adaptive CSDs.**

Index Terms– current-source driver (CSD), power MOSFET, buck converter, voltage regulator (VR), voltage regulator module (VRM), resonant gate driver

I. INTRODUCTION

Resonant gate driver technique has been used in high current and low voltage application such as Voltage Regulators (VRs). The resonant gate drivers are able to reduce the gate drive loss, i.e. CV^2 loss that happens with the conventional voltage driver, at high frequency operation (>1MHz) [1]-[4].

Current Source Drivers (CSDs) have been proposed in the applications of high frequency low voltage and high current such as Voltage Regulators (VRs). One of the most important benefits of the CSD technology is to achieve significant switching loss reduction of the power MOSFETs at the switching frequency of MHz [5]-[6].

The idea of the CSD circuits is to build a Current Source (CS) to charge and discharge the power MOSFET gate capacitance so that fast switching speed and reduced switching loss can be achieved. Based on this basic idea, different CSD topologies have been proposed. According to the current types of the CS inductor, the CSD topologies can be categorized as the continuous and discontinuous [7]-[11].

The continuous CSDs can use two drive MOSFETs with the complementary control to build a continuous current waveform in the CS inductor. Due to the continuous current, the drive switches are able to achieve Zero Voltage Switching (ZVS), which is beneficial to MHz operation. However, the CS inductor value is relatively high, and is typically around 1μH. Furthermore, the inductor value and the drive currents depend on the switching frequency.

In order to reduce the circulating loss in the driver circuit and reduce the CS inductor value, different discontinuous CSDs have been proposed [12]-[15]. In comparison, the discontinuous CSDs have much lower inductor value, which is around 20nH. This significant inductance reduction leads to size and board area reduction. More importantly, the CS inductor value is independent of the switching frequency so that variable frequency control can be used with this type of CSDs. Nevertheless, to build a discontinuous current, more drive switches are generally needed and sophisticated control timing are also required.

For the CSD technology, high drive currents normally lead to lower switching loss. A stronger drive current is desired to reduce the switching loss further when the power MOSFET carries higher current. Nevertheless, higher drive currents also result in higher circulating loss. However, the present CSD circuits normally use constant drive currents and voltages. For the control MOSFETs, stronger drive currents means fast switching speed and lower switching loss, but results in higher drive circuit loss. This leads to a trade-off between the switching loss reduction and gate drive loss. For the synchronous MOSFETs, stronger drive currents means fast switching speed and then lower body diode loss, but results in higher gate drive loss. This leads to a trade-off between the body diode loss and gate drive loss. However, constant drive currents and voltages limit the optimal operating conditions of the loss reduction. To achieve high efficiency curves through wide load range becomes an important topic for high frequency VRs. High gate drive currents and voltages are beneficial to the nominal load conditions, but hurt light load efficiency, which is of great importance for buck VRs.

Therefore, the adaptive drive current would be beneficial to improve the performance of the CSDs and help to achieve

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optimal design of the switching loss reduction and gate drive loss reduction. The objective of this paper is to propose the adaptive CSD concept to improve the performance of the CSD circuits. The proposed adaptive CSD could achieve different optimal drive currents depending on the drain current in the power MOSFETs, or the load conditions and input voltage. Section II presents the proposed adaptive concept for the CSDs. Section III presents the adaptive continuous CSDs. Section IV presents the adaptive discontinuous CSDs. Section V is the implementation of the adaptive CSDs. Section VI contains the experimental results and discussion. Section VII is the conclusion.

II. Proposed Adaptive CSD Concept for High Frequency MOSFETs

The proposed adaptive CSD concept is illustrated in Fig. 1. This can be regarded as a general structure for the adaptive CSDs. In Fig. 1, S_1 and S_2 form a totem structure to provide a low impedance path for the gate terminal of the power MOSFET Q either during the turn-on condition or turn-off condition. The adaptive parameters are as follows: 1) V_D is a controlled voltage source as the CSD voltage. It can be controlled with the variables in the power circuits such as load currents, drain currents of the switching devices and input voltage etc. Higher drive voltages result in lower $R_{DS(on)}$ and thus lower conduction losses, but increases drive losses. 2) i_{Cs} is a controlled current source as the drive current for Q. It can also be controlled with the loads, drain currents and voltages in the power circuit. Higher drive current reduces the switching loss but increases the gate drive loss.

Compared to other CSD circuits, the controllable drive current and drive voltage is beneficial to the optimal design between the switching loss and drive loss for the wide range operation of the main power MOSFETs. This concept can be extended to most of the CSD circuit topologies. In this paper, two basic structures of the continuous CSD and discontinuous CSD are investigated to achieve this adaptive control.

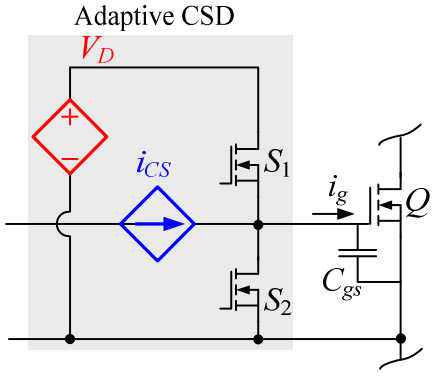

Fig. 1 The proposed discontinuous CSD

III. Adaptive Continuous CSD

A. Circuit Description

Fig. 2 shows the continuous CSD circuit, which is the half-bridge topology and consists of two drive MOSFETs S_1 and S_2. V_c is the drive voltage, L_r is the current source inductor and C_b is the blocking capacitor.

Fig. 3 gives the key waveforms. S_1 and S_2 are switched out of phase with the complimentary control to achieve ZVS. The inductor current is continuous and triangle. The peak portion of the inductor current is used to turn on and turn off the main power MOSFET Q during $[t_0, t_1]$ and $[t_2, t_3]$ as shown in Fig. 3 respectively.

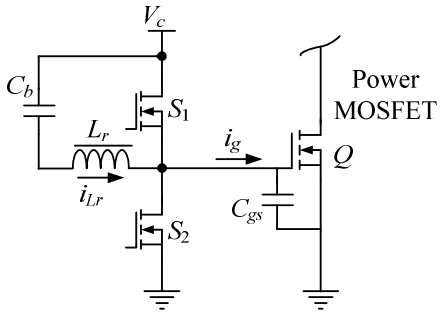

Fig. 2 Continuous CSD

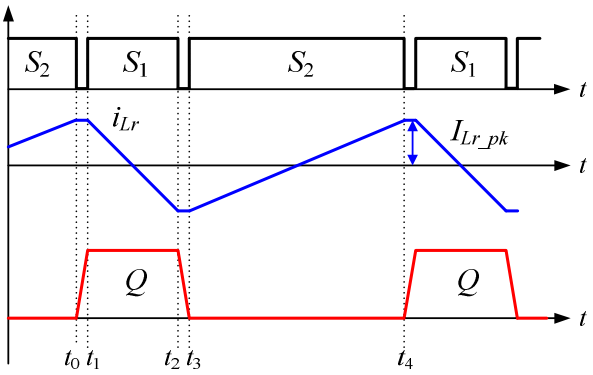

Fig. 3 Key waveforms of the continuous CSD

B. Synchronous Buck Converter with the Continuous CSD

Fig. 4 shows the continuous CSD applied to the synchronous buck converter, where Q_1 is the control MOSFET and Q_2 is the synchronous MOSFET. In Fig. 4, there are two sets of the drive circuits (CSD #1 and CSD #2) and each of them has the structure of the half-bridge topology, consisting of drive MOSFETs S_1&S_2 and S_3 &S_4 respectively. Fig. 5 gives the key waveforms.

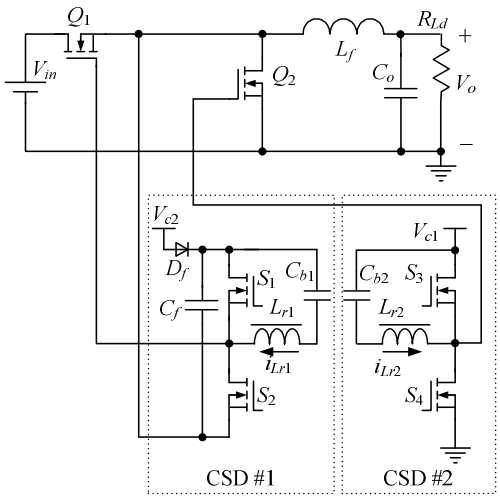

Fig. 4 Buck VR with proposed current-source driver

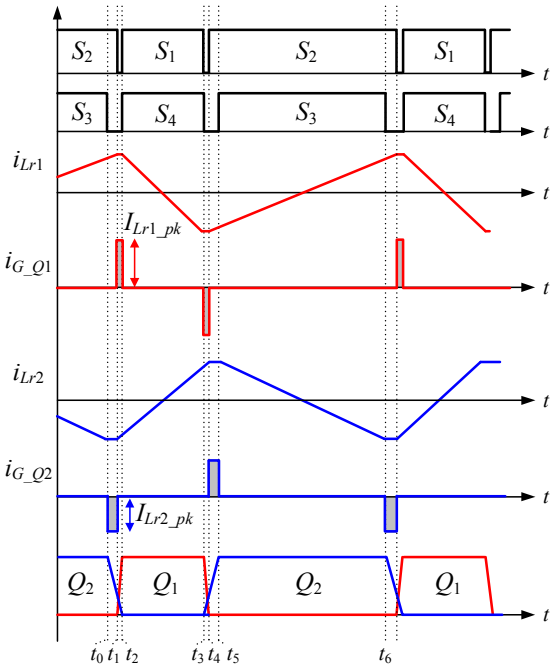

Fig. 5 Key waveforms of the new drive circuit

C. Optimal Design and Adaptive Control with the Continuous CSD

For a given application, in order to achieve fast switching speed, the gate drive current should be chosen properly. The design trade-off is between switching speed, which translates into reduced switching loss and gate drive loss.

The basic idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together. The object function is a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve.

Based on the above idea, Fig. 6 illustrates the optimal curve for the continuous CSDs respectively, which includes the switching loss $p\_{switching\ loss}$, the CSD circuit loss $p\_{CSD\ circuit}$ and the objective function $F(I_G)$ as function of the gate drive current I_G. The specifications of the buck converter are: V_{in}=12V; V_o=1.3V; I_o=30A; V_c=5V; f_s=1MHz; control MOSFET Q_1: Si7386DP; Q_2: IRF6691 and L_f=330nH.

It is observed that $F(I_G)$ is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. As shown in Fig. 6, the optimal drive current I_G is chosen as 1.8A for the continuous one.

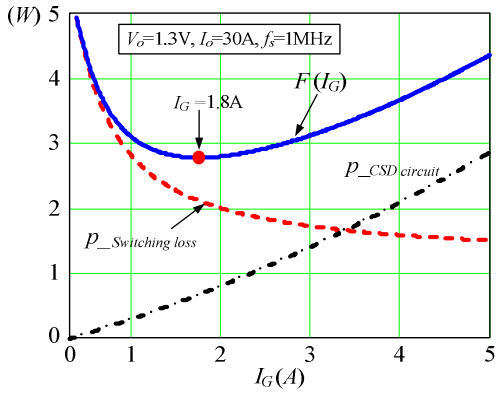

Fig. 6 Optimization curves for the control MOSFET Q_1: power loss vs. gate current

It should be noted that in Fig. 6, the optimal point is decided at the load current of 30A. However, when the load changes, the optimal point will also change depending on the switching loss associated with the drain currents in the MOSFET. Therefore, it is interesting to give the optimal curves under different load conditions as shown in Fig. 7. It is observed that when the load currents increase from 10A to 30A, the optimal drive currents increase accordingly from 1.2A to 1.8A. This means that higher drive currents lead to lower switching losses. So the desired CSD currents should be able to adjust adaptively as the load currents increase.

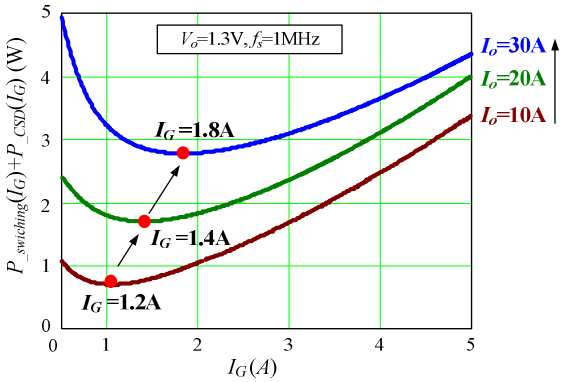

Fig. 7 Optimization curves for the control MOSFET Q_1 with different currents: power loss vs. gate current

Similarly, Fig. 8 gives the optimal curves for the SR MOSFET according to the load conditions. The synchronous MOSFET, Q_2, operates with ZVS since its output capacitance is discharged to zero voltage before it turns on. Therefore, for the synchronous MOSFET, the optimal design involves a tradeoff between body diode conduction loss and gate drive loss. When the load currents increase from 10A to 30A, the optimal drive currents increase from 0.6A to 1.2A. High drive currents lead to lower body diode conduction and body diode loss.

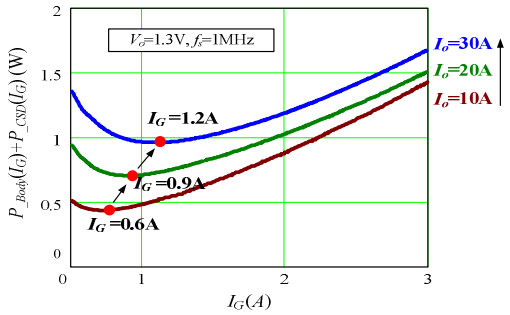

Fig. 8 Optimization curves for the synchronous MOSFET Q_2: power loss vs. gate current

For the continuous CSD, the peak value of the CS inductor current is the drive current, which is

$$I_G = I_{Lr\_pk} = \frac{V_c \cdot D \cdot (1-D)}{2 \cdot L_r \cdot f_s} \qquad (1)$$

where V_c is the drive voltage, D is the duty cycle and L_r is the CS inductor.

Fig. 9 shows the drive current as function of the drive voltages with different duty cycles. For the continuous CSD, with the same duty cycle, the CS inductor currents, i. e. the drive currents, increase linearly when the drive voltages increase. Therefore, the adaptive drive current control of the CSDs can be translated into the adaptive drive voltage control. In this way, the drive voltages can be controlled according to the load conditions, so that higher drive currents can be achieved to the optimal performance of the switching loss reduction.

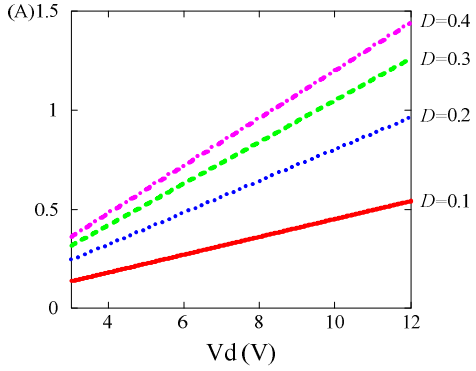

Fig. 9 The CS current as function of the drive voltage with different duty cycles

IV. Adaptive Discontinuous CSD

A. Circuit Description

Fig. 10 shows the discontinuous CSD circuit and Fig. 11 gives the key waveforms. In order to achieve discontinuous inductor current, S_3 and S_4 are inserted in series with the L_r and form a bidirectional switch, so that the current in the inductor can be controlled as desired. The key to this CSD is to control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the inductor current to be used to charge and discharge the power MOSFET gate capacitance as a nearly constant current source.

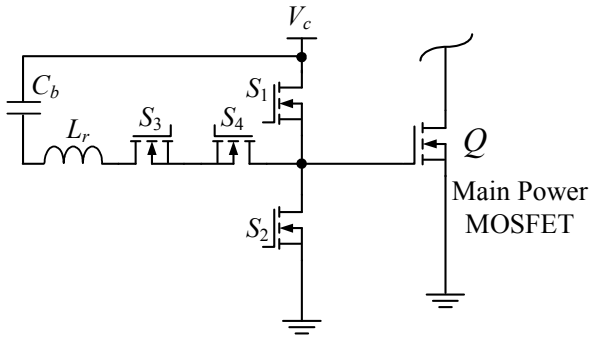

Fig. 10 Discontinuous CSD topology

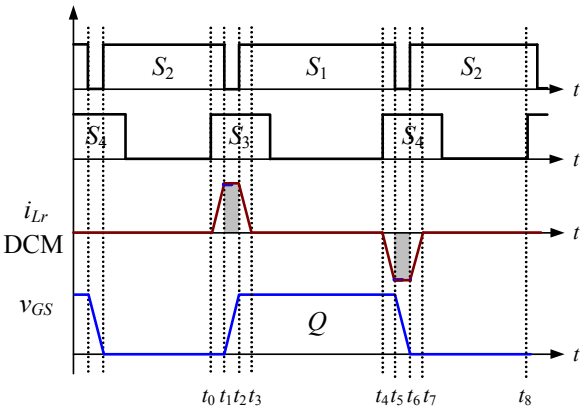

Fig. 11 Discontinuous key waveforms

B. Synchronous Buck Converter with the Discontinuous CSD

Fig. 12 shows the proposed hybrid gate drive scheme for a buck converter. As we know, for a buck VR, the dominant loss is the switching loss. Therefore, for the control MOSFET Q_1, the proposed high side CSD is used to achieve the switching loss reduction. For the SR Q_2, the conventional voltage source driver is used for low cost and simplicity. PWM_SR is the signal fed into the voltage source driver.

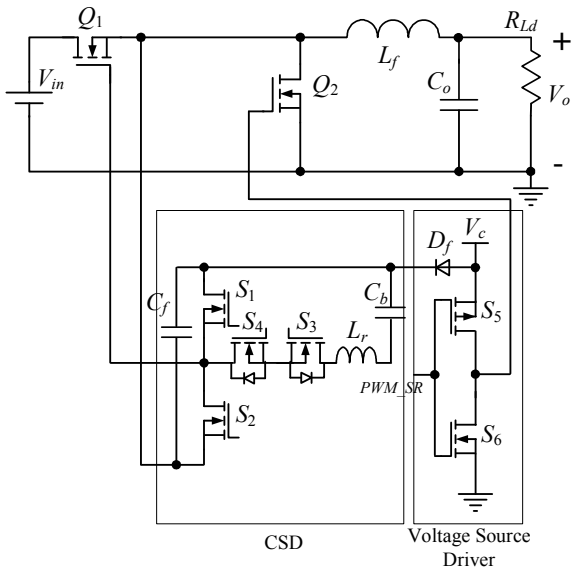

Fig. 12 Buck converter with proposed discontinuous CSD

C. Optimal Design and Adaptive Control with the Discontinuous CSD

Similarly, Fig. 13 shows the adaptive gate current for the discontinuous CSDs. As the load current increases from 10A to 30A, the optimal drive currents increase from 1.8A to 2.8A. It should be noted that at the same load current of 30A, the optimal drive current I_G is chosen as 2.8A for the discontinuous CSD while the optimal drive current is 1.2A for the continuous one. This is because the discontinuous CSD has lower drive circulating loss over the continuous one as shown in Fig. 13, which helps to achieve high drive current.

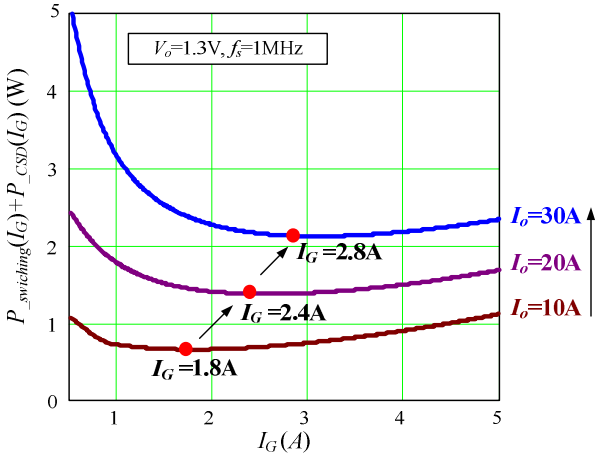

Fig. 13 Discontinuous: Optimization curves for the control MOSFET Q_1: power loss vs. gate current

For the discontinuous CSD, referring to Fig. 11, the pre-charge current to turn on the power MOSFT is

$$I_{G\_on} = \frac{V_D}{2L_r} t_{10} \tag{2}$$

where V_D is the drive voltage and t_{10} is the pre-charge interval.

Similarly, the pre-charge current to turn off the power MOSFET is

$$I_{G\_off} = \frac{V_{Cs}}{L_r} \cdot t_{54} = \frac{V_D}{2L_r} \cdot t_{54} \tag{3}$$

where V_{Cs} is the DC voltage across the capacitor.

Fig. 14 shows the drive current as function of the drive voltages with different duty cycles. Similar to the continuous CSD, the drive currents also increase linearly when the drive voltages increase. So the adaptive drive voltages also lead to the adaptive drive current. More importantly, for the discontinuous CSD, the drive currents are independent with the duty cycles. This makes the discontinuous CSDs suitable for variable fast duty cycle controls.

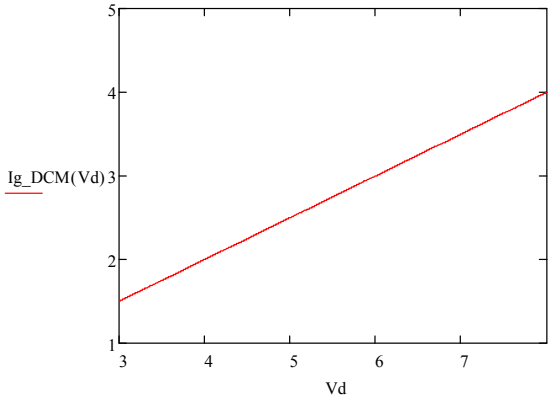

Fig. 14 The CS current as function of the drive voltages

V. Implementation of the Adaptive Drive Voltage for the CSDs

As discussed in Section IV, for both of the continuous and discontinuous CSDs, the drive currents are proportional to the drive voltages. One method to build the adaptive drive currents is to adjust the drive voltages adaptively according to the load currents, or input voltages etc.

Fig. 15 gives an adaptive drive voltage circuit using the basic linear regulator. The advantage of using the linear regulator is that simple implementation and fast voltage change rate. Fig. 16 gives the simulated waveforms using SPICE software. When the reference voltage changes as the load currents, the drive voltages change adaptively accordingly.

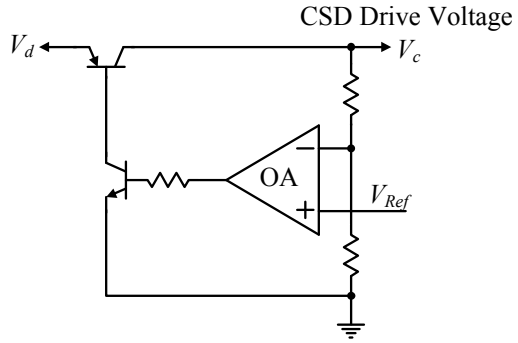

Fig. 15 Adaptive drive voltage circuit using the basic linear regulator

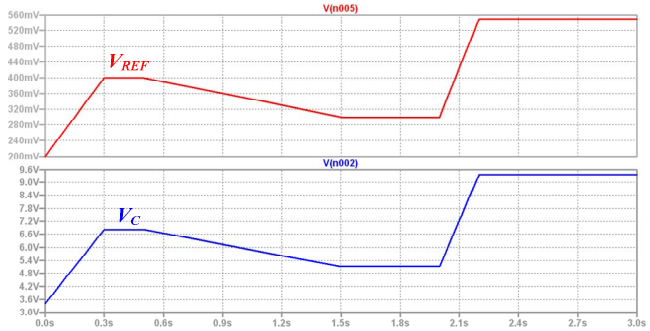

Fig. 16 The simulated waveforms of drive voltage

VI. Experimental Results and Discussion

In order to verify the proposed adaptive concept, the synchronous buck converters with the continuous and discontinuous CSDs were implemented. The specifications of the buck converter prototype are as follows: input voltage V_{in}=12V; output voltage V_o=1.3V; output current I_o=30A; switching frequency f_s=1MHz. The PCB is six-layer with 4 oz copper. The components used in the circuit are listed as follows: Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: L_f=330nH (IHLP-5050CE-01, Vishay); for the continuous CSD, L_r=1μH; for the discontinuous CSD, L_r=22nH; drive switches S_1-S_4: FDN335.

Fig. 17 shows the inductor current i_{Lr} and gate drive signals v_{GS_Q1} (control FET) for the discontinuous CSD at the load current of 30A. Its peak current value is 2.8A, which is the optimized value of the CSD drive current at 8V gate voltage. After the pre-charge time, the inductor current continues to ramp up while charging the gate capacitance of the power MOSFET (Si7386DP) during the turn on interval. During this interval the average drive current is approximately 2.6A. After the power MOSFET turns on, the inductor current ramps back down to zero while the inductor energy is returned to drive voltage source.

Fig. 18 shows the gate drive signals v_{GS_Q1} (control FET) and v_{GS_Q2} (Sync FET). It is observed that v_{GS_Q1} is smooth since the miller charge is removed fast by the constant inductor drive current. Moreover, the total rise time and fall time of v_{GS_Q1} is less than 15ns, which means fast switching speed is achieved. The dead time between two drive voltages is fixed to avoid shoot-through and is minimized to reduce the SR body diode conduction loss.

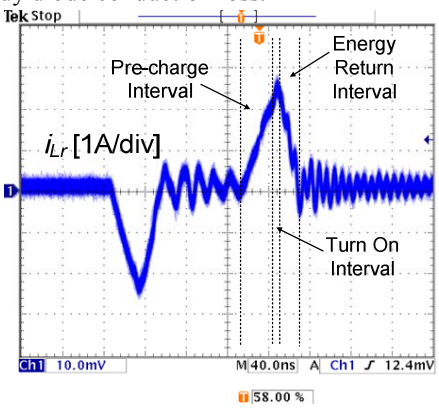

Fig. 17 Inductor current and the gate-to-source voltage at 1MHz

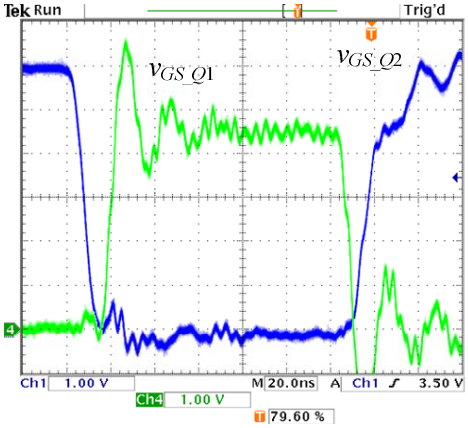

Fig. 18 Gate signals v_{GS_Q1} (control MOSFET) and v_{GS_Q2} (SR)

A benchmark of a synchronous buck converter with the conventional gate driver was also built. The Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver. Fig. 19 shows the measured efficiency comparison between the continuous CSDs with and without the adaptive voltages at 1.3 V output. It is observed that at 5A, the efficiency is improved from 79.1% to 85.7% (an improvement of 6.6%) with the drive voltage of 4V. At 10A, the efficiency is improved from 86.2% to 88.4% (an improvement of 2.2%) with the drive voltage of 5V. It should be also noted that the CSDs improves the efficiency effectively in full load range over the conventional driver.

Fig. 20 shows the measured efficiency comparison between the discontinuous CSDs with and without the adaptive voltages at 1.3 V output. It is observed that at 5A, the efficiency is improved from 80.6% to 86.1% (an improvement of 5.5%) with the drive voltage of 4V. At 10A, the efficiency is improved from 85.6% to 88.6% (an improvement of 3%) with the drive voltage of 5V. It should be also noted that the CSDs improves the efficiency

effectively in the full load range over the conventional driver. The adaptive CSD achieve better efficiency improvement for lower load current range since the switching loss happens with light load current reduces greatly.

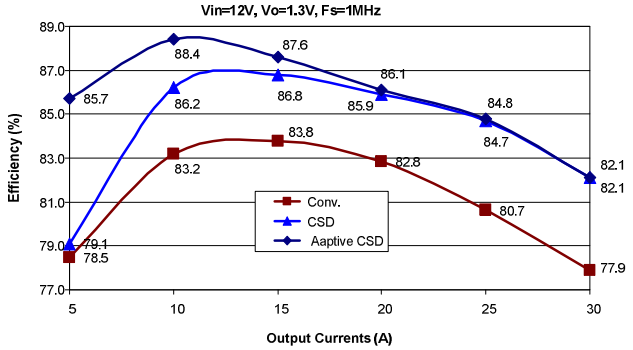

Fig. 19 Efficiency comparison: top: continuous adaptive CSD; mid: continuous CSD; bottom: conventional voltage driver (Conv.)

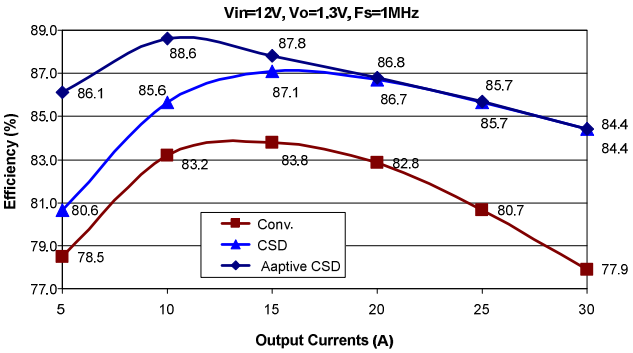

Fig. 20 Efficiency comparison: top: discontinuous adaptive CSD; mid: discontinuous CSD; bottom: conventional voltage driver (Conv.)

VII. CONCLUSIONS

In this paper, the concept of the adaptive CSDs is proposed for the high frequency synchronous buck converters. The idea of the adaptive CSDs is to optimize the switching loss reduction and the drive loss reduction at MHz at different load currents. It should be noted that the adaptive concept is suitable for both the continuous and discontinuous CSDs regardless the drive circuit topologies. Through investigating the CSD circuits, one simple method to achieve the adaptive drive currents based on the adaptive voltages is proposed. The linear regulator can be used to achieve the function of the adaptive voltages and drive currents in a cost-effective manner.

A 12V input, 1.3V output and 1MHz synchronous buck converter was built to verify the advantages of the proposed adaptive CSDs. For the continuous CSD, at 1.3V output, the adaptive CSD improves the efficiency from 79.1% (without adaptive control) to 85.7% (an improvement of 6.6%) at 5 A, and at 10A, from 86.2% to 88.4% (an improvement of 2.2%). Similar efficiency improvements are achieved for the discontinuous CSDs.

REFERENCES

[1] K. Jin, M. Xu, Y. Sun, D. Sterk and F. C. Lee, "Evaluation of self-driven schemes for a 12-V self-driven voltage regulator," *IEEE Trans. Power Electron.*, Vol. 24, No. 10, pp. 2314-2322, Oct. 2009.

[2] L. Huber, K. Hsu, M. M. Jovanovic, D. J. Solley, G. Gurov and R. M. Porter, "1.8-MHz, 48-V resonant VRM: analysis, design, and performance evaluation," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp.79-88, Jan. 2006.

[3] Q. Li and P. Wolfs, "The power loss optimization of a current fed ZVS two-inductor boost converter with a resonant transition gate drive," *IEEE Trans. Power Electron.*, Vol. 21, No. 5, Sep. 2006, pp. 1253 -1263.

[4] G. Spiazzi, P. Mattavelli and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, Vol. 23, No. 4, July 2008, pp. 2082–2092.

[5] Z. Yang, S. Ye and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp.1311-1320, July 2007.

[6] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, Mar. 2008, pp. 678 -691.

[7] K. Yao and F.C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Trans. Power Electron.*, Vol. 17, No. 2, pp.180-186, Mar. 2002.

[8] Y. Ren, M. Xu, Y. Meng and F.C. Lee, "12 V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE PESC*, 2005, pp. 2635-2641.

[9] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching Loss", *IEEE Trans. Power Electron.*, Vol. 23, No. 3, May 2008, pp. 1574-1583.

[10] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu and P. C. Sen, "A 1-MHz high efficiency 12V buck voltage regulator with a new current-source gate driver," *IEEE Trans. Power Electron.*, Vol. 23, No. 6, Nov. 2008, pp. 2817-2827.

[11] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu and P. C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, Mar. 2008, pp. 653 -666.

[12] S. Pan and P. K. Jain, "A new pulse resonant MOSFET gate driver with efficient energy recovery," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, 2006, pp. 1-5.

[13] X. Zhou, Z. Liang and A. Huang, "A new resonant gate driver for switching loss reduction o f high side switch in buck converter," in *Proc. IEEE APEC*, 2010, pp. 1477-1481.

[14] H. Fujita, "A resonant gate-drive circuit capable of high-frequency and high-efficiency operation," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, Apr. 2010, pp. 962-969.

[15] Z. Zhang, J. Fu, Y. F. Liu and P. C. Sen, "Discontinuous current source drivers for high frequency power MOSFETs," *IEEE Trans. Power Electron.*, Vol. 25, No. 7, Jul. 2010, pp. 1863-1876.