

A New High Efficiency Current Source Driver with Bipolar Gate Voltage

Jizhen Fu (*Student Member, IEEE*)¹, Zhiliang Zhang (*Member, IEEE*)²,
Yan-Fei Liu (*Senior Member, IEEE*)^{1,3}, P.C. Sen (*Life Fellow, IEEE*)¹ and Lusheng Ge³

¹ Queen' Power Group, Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6

² Aero-Power Sci-tech Center, College of Automation Engineering

Nanjing University of Aeronautics and Astronautics, Nanjing, P. R. China

³ School of Electrical Engineering and Information, Anhui University of Technology, Ma An
Shan, Anhui Province, China, 243002

jizhen.fu@queensu.ca, zlzhang@nuaa.edu.cn, yanfei.liu@queensu.ca, senp@post.queensu.ca and
lsge@ahut.edu.cn

Abstract –A novel bipolar Current Source Driver (CSD) for power MOSFETs is proposed in this paper. The proposed bipolar CSD alleviates the gate current diversion problem of the existing CSDs by clamping the gate voltage to a flexible negative value (such as -3.5V) during turn-off transition. Therefore, the proposed driver is able to turn off the MOSFET much faster with a higher effective gate current. The idea presented in this paper can also be extended to other CSDs to further improve the efficiency with high output currents. The experimental results verify the benefits of the proposed CSD. For buck converters with 12 V input at 1MHz switching frequency, the proposed driver improves the efficiency from 80.5% using the existing CSD to 82.5% (an improvement of 2%) at 1.2V/30A, and at 1.3V/30A output, from 82.5% using the existing CSD to 83.9% (an improvement of 1.4%).

Index Terms – Voltage Regulators (VRs), Buck Converter, Voltage Source Driver (VSD), Resonant Gate Driver (RGD), Current Source Driver (CSD), Current Diversion Problem, Common Source Inductance

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This paper falls in the category of: low power converters

Corresponding author: Dr. Yan-Fei Liu

Email: yanfei.liu@queensu.ca

Tel: (613)-533-6000 ext. 36731

Fax: (613)-533-6615

Address: Room 410, Walter Light Hall

Department of Electrical and Computer Engineering

Queen's University at Kingston

Kingston, Ontario, Canada, K7L 3N6

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I. INTRODUCTION

The next generation Voltage Regulators (VRs) feature low output voltage, high output current and high power density [1]-[3]. To meet the requirements of the future microprocessors, it is necessary to increase the switching frequency as high as possible ($>1\text{MHz}$) within the practical constraints, in order to reduce the size of passive components and achieve better dynamic performance [4]-[6].

However, as the switching frequency increases, the efficiency of a buck converter using the conventional Voltage Source Driver (VSD) suffers from two main types of frequency-dependent losses: 1) gate drive loss 2) switching loss [7]-[9]. In addition, the impact of parasitic inductance, consisting of the PCB trace inductance and the bonding wire inside the MOSFET package, becomes even worse at higher frequency, which significantly introduces extra switching loss [10]-[13].

One way to reduce the gate drive loss is Resonant Gate Drivers (RGDs) [14]-[17], which can recover part of the gate drive energy. RGDs are especially effective for the synchronous rectifier (SR) of synchronous buck converters, since the SR is designed with large gate charge and small on resistance to reduce its conduction loss during freewheeling mode. Also, some RGDs can drive two MOSFETs with the transformer or coupled inductor [17]-[18]. Nevertheless, the design of the transformer or coupled inductor is really challenging. Most importantly, the RGDs only emphasize on the reduction of gate loss, but they can hardly reduce the switching loss which is the dominant loss for high frequency operations. Therefore, the efficiency improvement potentials for the RGDs are limited.

Current Source Drivers (CSD) that can reduce the switching loss of the power MOSFET are reported in [19]-[26] to improve the performance of RGDs. Either working under continuous current mode [19]-[22] or discontinuous current mode [23]-[26], the existing CSDs can charge

and discharge the power MOSFET with a nearly constant current to accelerate the switching speed. In particular, during turn-off transition where majority of the switching loss happens ([11], [19], [27]), the existing CSDs can turn-off the power MOSFET with a negative voltage (around -0.7V). In other words, compared with the conventional VSDs whose gate drive signal is unipolar, the existing CSDs can achieve bipolar gate driver signal, which means much faster switching speed and smaller switching loss. In order to further improve the performance of the CSD in the previous work, a new bipolar CSD that can turn off the power MOSFET with a flexible negative voltage (such as -3.5V) is proposed in this paper.

The outline of the paper is as follows: in Section II, the limitation of the existing gate drivers (conventional VSD and existing CSDs) during turn-off transition will be illustrated; especially, the current diversion problem of the existing CSDs introduced by the common source inductance is analyzed. Section III reports the topology and the operation principle of the proposed bipolar CSD, and summarizes its advantages. In Section IV, the experimental results are presented to verify the features of the proposed CSD, followed by discussions. Finally, the conclusions are drawn in Section V.

II. LIMITATION OF EXISTING GATE DRIVERS

A. Limitation of Conventional VSDs

The conventional VSD is illustrated in Fig. 1 to drive the power MOSFET, M, whose parasitics are shown: R_G is the gate resistance, C_{GS} is the gate-to-source capacitance, C_{GD} is the gate-to-drain capacitance, C_{DS} is the drain-to-source capacitance, L_S is the common source inductance including the bonding wire inside the MOSFET package and PCB trace inductance and L_D is the switching loop inductance. The conventional VSD has a totem pole configuration, which turns on the MOSFET by turning on the top switch of VSD, S_P ; while turns off the MOSFET by turning on the bottom switch of VSD, S_N .

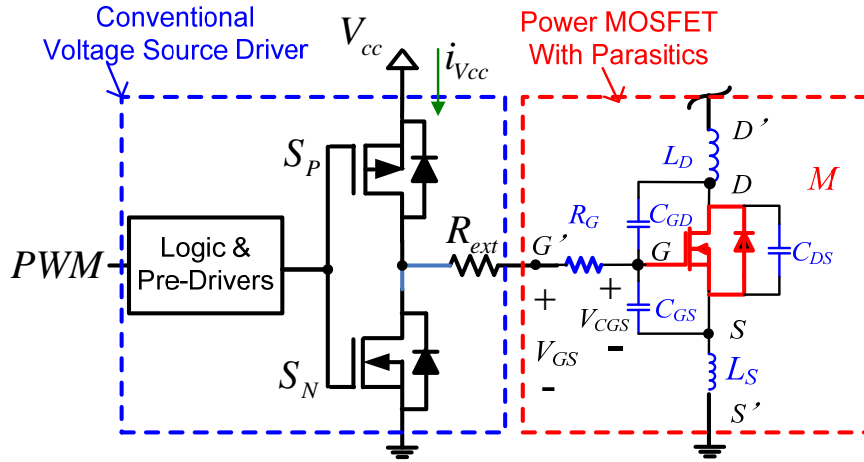


Fig. 1 Conventional VSD with power MOSFET and its associated parasitics

The switching waveforms associated with Fig. 1 are shown in Fig. 2 , where PWM is the PWM signal input of the VSD, V_{CGS} is the voltage across the C_{GS} of M, V_{DS} is the drain-to-source voltage across M, i_{DS} is the drain-to-source current flowing through the M, P_{on} is the turn-on loss and P_{off} is the turn-off loss. It is noted that turn-off loss is the dominant loss of the total switching loss P_{switch} ([11], [19], [27]). It is also observed that, due to the effect of the parasitic inductance, V_{DS} reduces sharply when i_{DS} starts to increases at t_1 and then keeps almost constant during (t_1, t_2) since the rising rate of i_{DS} is almost constant in this interval ([11], [12]).

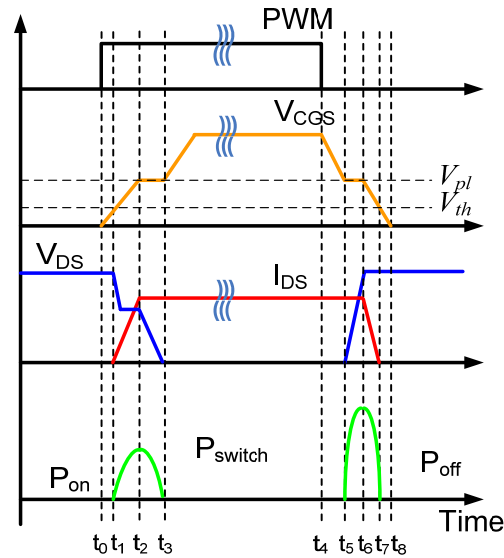


Fig. 2 Switching waveforms of power MOSFET driven by the conventional VSD

The equivalent circuit of the MOSFET driven by the VSD during turn-off transition is given in Fig. 3. When S_N in Fig. 1 is turned on, because of the on resistance of S_N (larger than 0.5Ω), the voltage appearing across the gate-to-source of power MOSFET, V_{GS} , is around 0.5V. Therefore, the main drawback of VSD is that V_{GS} is unipolar, which means V_{GS} is always bigger than zero, even during turn-off transition. It seriously limits the turn-off speed, especially in the presence of the common source inductance in high frequency application as described below.

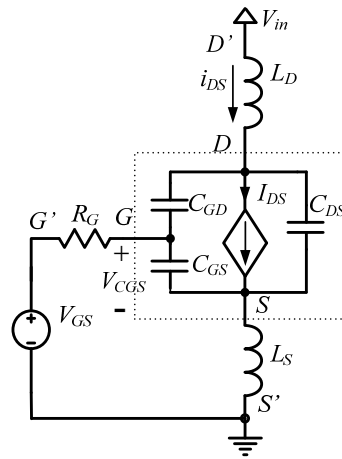


Fig. 3 Equivalent circuit of the MOSFET driven by VSD during turn-off transition

B. Limitation of Existing CSDs (Current Diversion Problem)

The CSD circuits, either working under continuous current mode or discontinuous current mode, can turn on and turn off the power MOSFET with a nearly constant current. One of the representative CSDs is reported in [23] and [24]. As shown in Fig. 4, it has the following advantages:

1. Minimized circulating current and thus minimal conduction loss.
2. Independent of the duty cycle, suitable for narrow duty cycle operation.
3. Lower inductor value, easier for integrated circuit (easier for integration).
4. Soft switching of the driver switches.

However, the CSDs proposed in the previous work have the same gate current diversion problem during switching transition due to impact of the common source inductance. Since the turn-off loss dominates the switching loss, the turn-off transition is focused on in this paper.

During the turn-off transition, the CSD in Fig. 4 can be simplified as the circuit in Fig. 5. The gate-to-source voltage V_{GS} in Fig. 5 is derived as below,

$$V_{GS} = -i_G R_G + V_{CGS} - L_s \frac{di_{DS}}{dt} \quad (1)$$

where V_{CGS} represents the voltage across the gate-to-source capacitance of the MOSFET Q , i_G is the effective discharge current, and i_{DS} represents the drain-to-source current.

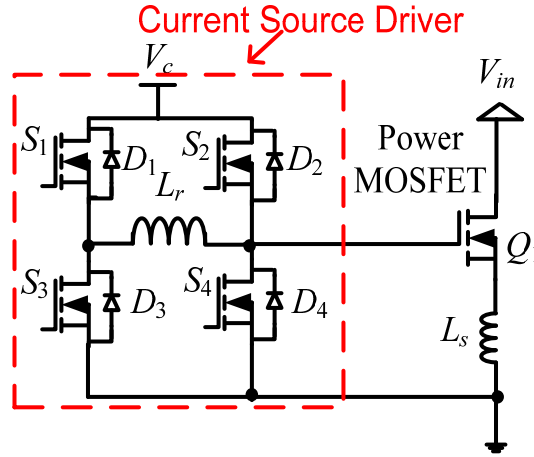


Fig. 4 Topology of the CSD reported in [23] and [24]

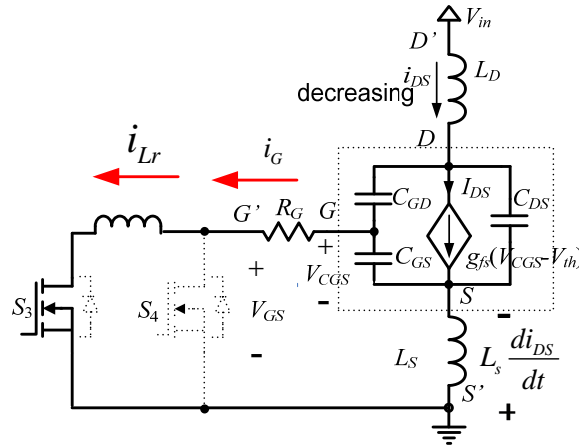


Fig. 5 Simplified discharging circuit of existing CSD in [23] and [24]

The higher the drain current falling rate di_{DS}/dt is, the faster the turn-off transition is achieved. According to the relationship in Equation (1), V_{GS} decreases when di_{DS}/dt increases. However, when V_{GS} goes below -0.7V, the body diode of S_4 , D_4 , in Fig. 4 will conduct, clamping V_{GS} at -0.7V. The equivalent circuit of the CSD after D_4 is driven on is shown in Fig. 6. It is noted

because of the impact of L_s , which significantly limits the turn-off speed.

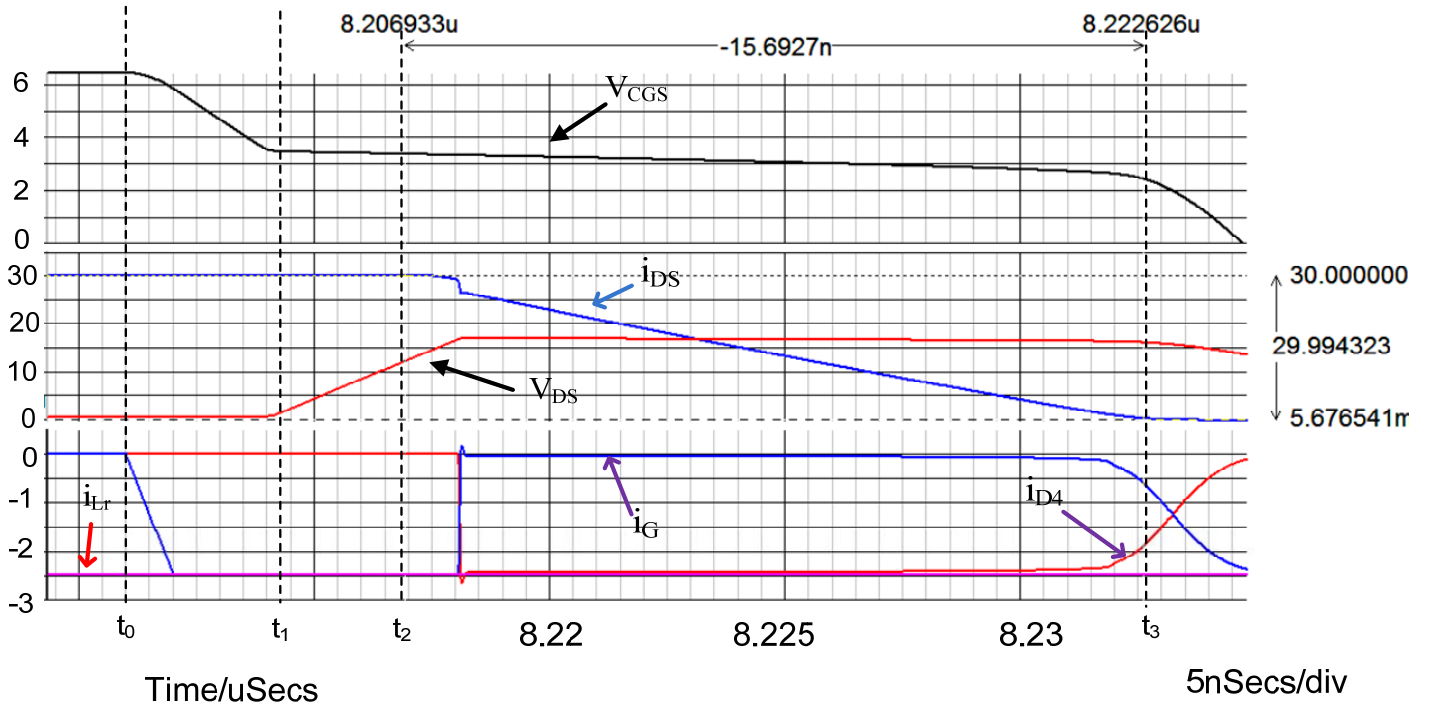


Fig. 7 Simulation waveforms of turn-off transition of CSD in [23] and [24]

III. PROPOSED BIPOLAR CURRENT SOURCE DRIVER CIRCUIT

A. Proposed Bipolar Current Source Driver

In order to alleviate the gate current diversion problem mentioned above and reduce the switching loss, a new bipolar CSD which can turn off the MOSFET with a flexible negative voltage is proposed in this paper. The topology of the proposed CSD is given in Fig. 8. It is noted that compared with the CSD in Fig. 4, S_4 is replaced by a pair of four-quadrant switches, S_4 and S_5 , whose source terminals are connected together to block the conduction of body diodes. Another key feature of the proposed CSD is to use five diodes D_{s1} - D_{s5} as an anti-diode of the S_4 & S_5 branch to create a negative gate voltage (i.e. -3.5V in Fig. 8) during turn-off transition, which can noticeably increase the gate discharge current. It is noted that the number of the diodes used in the proposed bipolar CSD is flexible and dependent on the value of the negative voltage designed during turn-off transition.

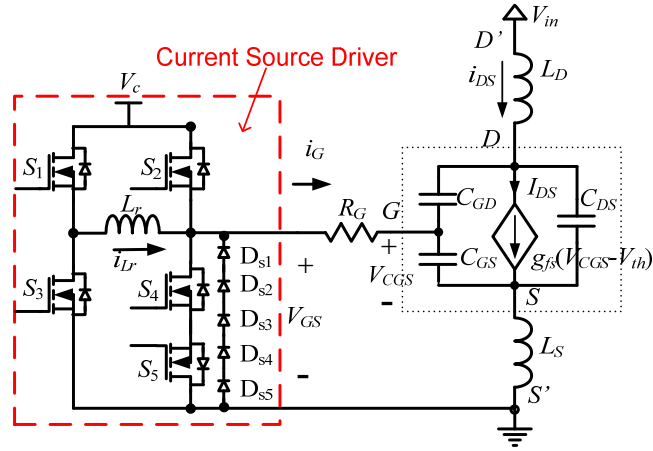


Fig. 8 Power MOSFET driven by the proposed bipolar CSD

The waveforms of the five switch gate driving signals, V_{GS1} - V_{GS5} , the inductor current i_{Lr} , the gate charge/discharge current i_G , the voltage across C_{GS} - V_{CGS} , the drain-to-source current i_{DS} , the drain-to-source voltage V_{DS} , and the gate-to-source voltage V_{GS} are illustrated in Fig. 9. It is noted the gate signals for S_4 and S_5 are exactly the same all through the switching cycles.

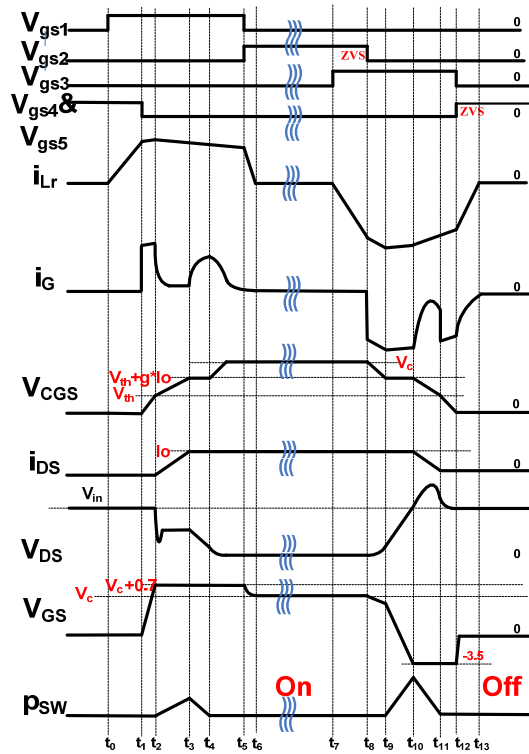


Fig. 9 Waveforms of the proposed bipolar CSD

B. Detailed Turn-On Operation

The operation principle of the turn-on transition is illustrated as follows. Prior to t_0 , the power MOSFET is assumed to be in the OFF state, and S_4 and S_5 are in the ON state.

1. *Turn-On Precharge* (t_0, t_1): At t_0 , S_1 is turned on, and the inductor current i_{Lr} rises almost linearly in the positive direction through the current path shown in Fig. 10 (a). The pre-charge state ends at t_1 , which is usually set by the designer.

2. *Turn-On Delay* (t_1, t_2): At t_1 , S_4 & S_5 are turned off; the inductor current i_{Lr} starts to charge the gate capacitance of Q - the equivalent circuit is given in Fig. 10 (b). At this interval, the effective charge current i_G equals i_{Lr} . This interval ends when V_{CGS} reaches V_{th} .

3. *Drain Current Rising* (t_2, t_3): At t_2 , $V_{CGS} = V_{th}$. During this interval, V_{CGS} keeps increasing, and i_{DS} starts to rise according to the relationship in Equation (3). Since i_{DS} flows through L_S , according to Equation (1), the large voltage induced across L_S makes V_{GS} far larger than the driver supply voltage V_c . Therefore, D_2 , the body diode of the driver switch S_2 , is driven on to clamp V_{GS} at $V_c+0.7$. The equivalent circuit is shown in Fig. 10(c). At this interval, i_G drops sharply because of the voltage clamping. The subtraction of i_{Lr} and i_G is diverted through D_2 .

$$i_{DS} = g_{fs}(V_{CGS} - V_{th}) \quad (3)$$

where g_{fs} is the transconductance of the power MOSFET.

4. *Miller Plateau* (t_3, t_4): At t_3 , $i_{DS} = I_o$. During this interval, V_{CGS} is held at the Miller plateau voltage. i_G mainly flows through the gate-to-drain capacitance of Q , and V_{DS} decreases accordingly. It is noted that i_G starts to rapidly increase since the EMF across L_S falls sharply due to the unchanged i_{DS} , however part of the inductor current is still diverted through D_2 . The equivalent circuit is given in Fig. 10 (d).

5. *Remaining Gate Charging* (t_4, t_5): At t_4 , $V_{DS} = 0$ and V_{CGS} starts to rise again until it reaches V_c . V_{GS} remains at $V_c+0.7$, and due to the rising of the V_{CGS} , i_G decreases gradually. The equivalent circuit is given in Fig. 10 (f).

6. *Energy Recovery* (t_5, t_6): At t_5 , S_2 is turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to V_c . It is noted that the gate voltage of power

MOSFET is clamped to V_c through a low impedance path, which prevents the circuit being false triggered by Cdv/dt effect.

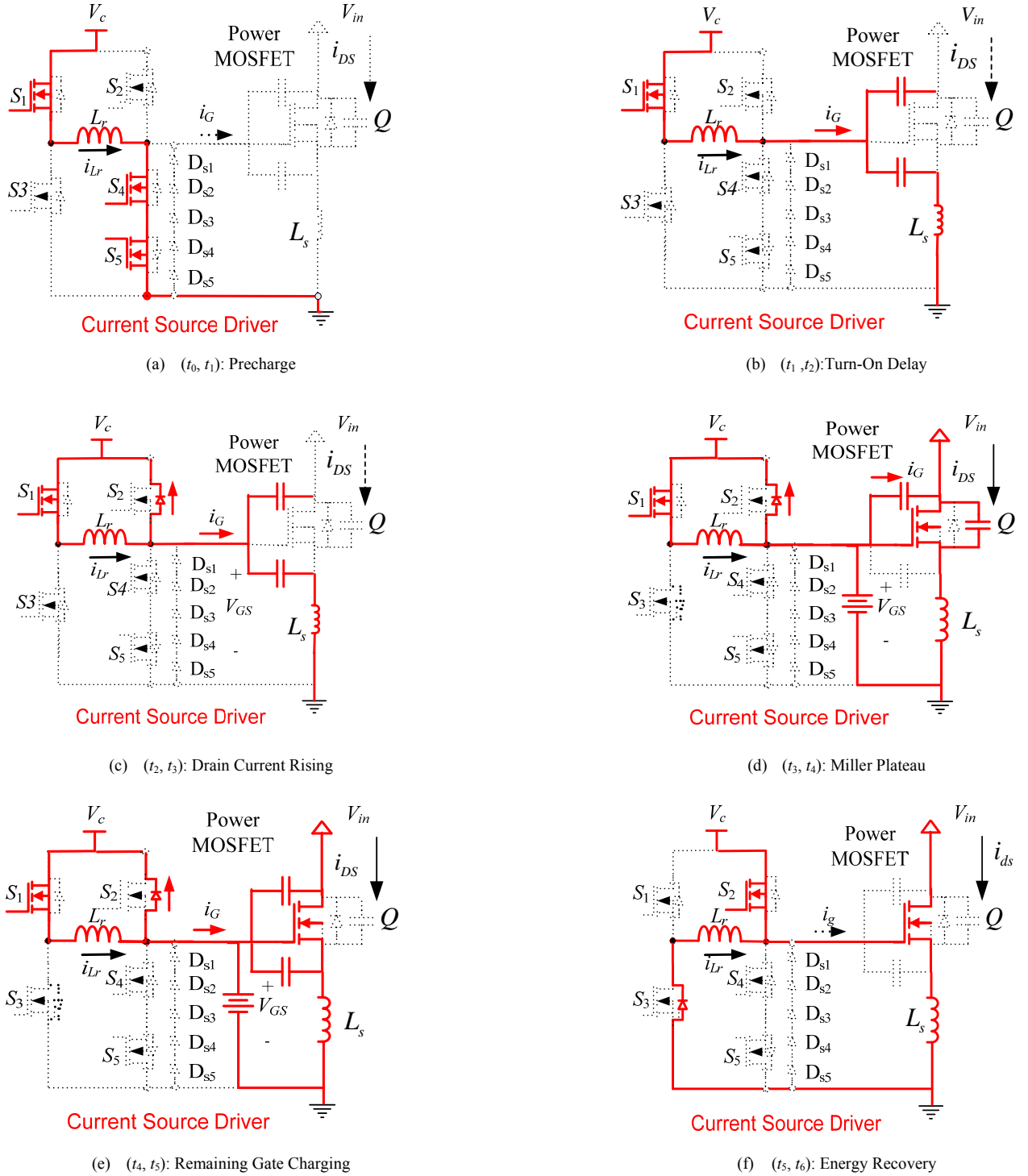


Fig. 10 Turn-on operation

C. Detailed Turn-Off Operation

The operation principle of the turn-off transition is illustrated as follows. Prior to t_7 , the power MOSFET is assumed to be in the ON state and S_2 is also in the ON state.

1. *Turn-Off precharge* (t_7, t_8): At t_7 , S_3 is turned on, and the inductor current i_{Lr} rises almost linearly in the negative direction through the current path shown in Fig. 11 (a). The pre-charge state ends at t_8 , which is set by the designer, and S_2 is turned off with ZVS at t_8 .

2. *Turn-Off Delay* (t_8, t_9): At t_8 , S_2 is turned off. In this interval, V_{CGS} decreases until $V_{th} + I_o * g_{fs}$ which ends the interval. The equivalent circuit is given in Fig. 11 (b).

3. *Miller Plateau* (t_9, t_{10}): At t_9 , $V_{CGS} = V_{th} + I_o * g_{fs}$. In this interval, V_{CGS} holds at the Miller plateau voltage, $V_{th} + I_o * g_{fs}$. i_G (equal to i_{Lr}) strictly discharges the gate-to-drain capacitance C_{GD} of Q, and V_{DS} rises until it reaches V_{in} at t_{10} . The equivalent circuit is illustrated in Fig. 11 (c).

4. *Drain Current Drop* (t_{10}, t_{11}): At t_{10} , $V_{DS} = V_{in}$ and V_{CGS} continues to decrease from $V_{th} + I_o * g_{fs}$ to V_{th} . i_{DS} falls from I_o to zero according to relationship in Equation (3). According to Equation (1), due to the induction EMF across L_s , the series connected diodes D_{s1} - D_{s5} are driven on to clamp V_{GS} at around -3.5V. The voltage across the current source inductor becomes -3.5V, so i_{Lr} decreases at a higher rate than in the turn-on transition. The equivalent circuit of this interval is given in Fig. 11 (d). It is emphasized is that the CSD proposed in [23] and [24] only can clamp V_{GS} to -0.7V. This means that the turn-off speed of the CSD proposed in this paper is much faster than that of the CSD in [23] and [24]. It is worth mentioning that V_{DS} in this interval will keep rising due to effect of the L_s .

5. *Remaining Gate Discharging* (t_{11}, t_{12}): At t_{10} , $V_{CGS} = V_{th}$. In this interval, V_{CGS} continues to decrease until it equals zero; it is noted that V_{DS} continues to rise during this interval. The equivalent circuit is shown in Fig. 11 (e).

6. *Energy Recovery* (t_{12}, t_{13}): At t_{12} , S_3 is turned off and S_4 & S_5 are turned on with ZVS. The body diode of S_1 , D_3 , is forced on by i_{Lr} , and the CSD circuit turns into the mode of energy recovery through the path shown in Fig. 11 (f). During this interval, the energy stored in L_r is recovered to V_c . The interval ends at t_{13} when the inductor current becomes zero.

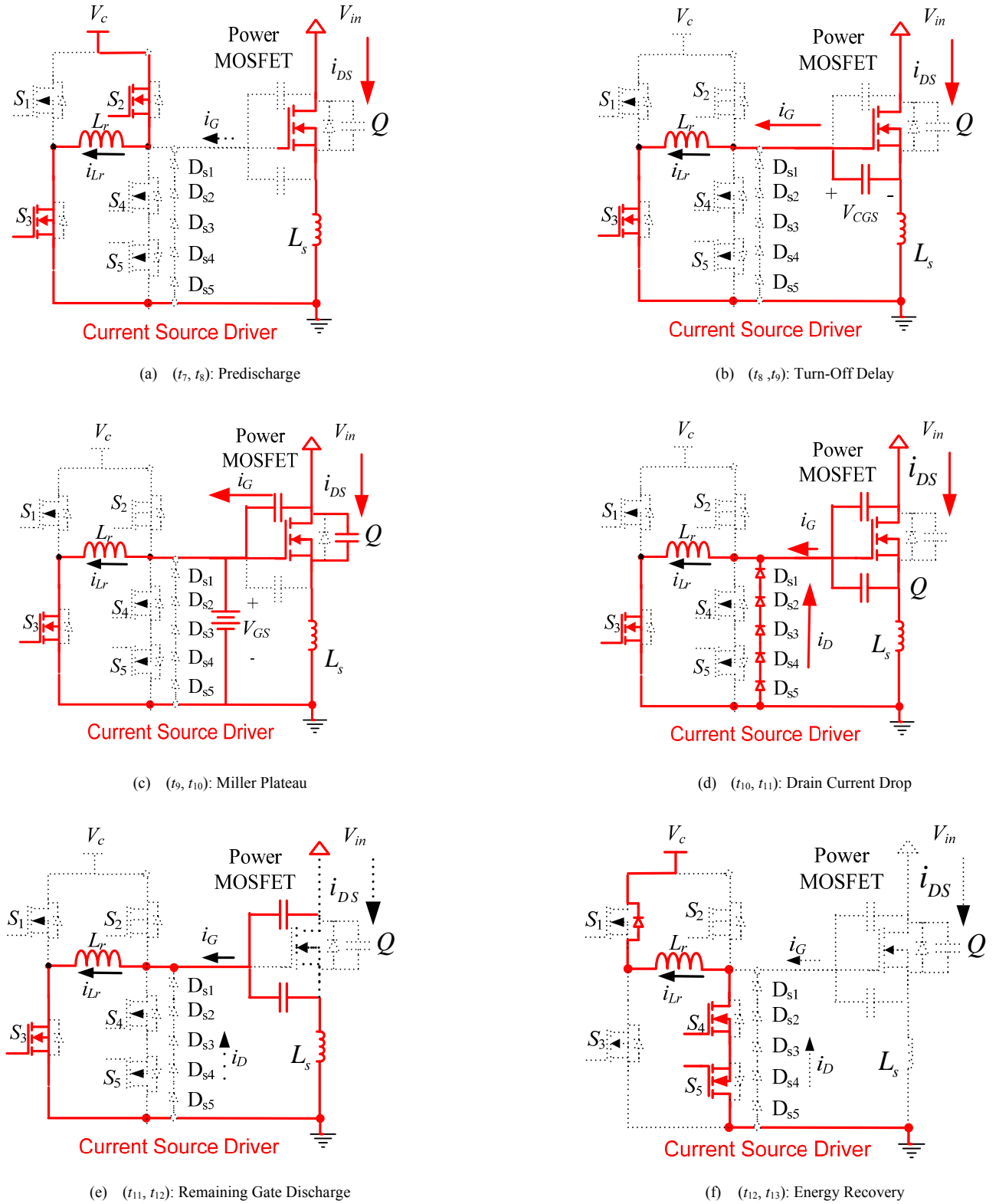


Fig. 11 Turn-off operation

In the analysis above, the detailed switching transition is analyzed. The current diversion problem introduced by the common source inductance is addressed. It is noted that the current diversion problem exists in both turn-on and turn-off transition. However, since the turn-off loss is the dominant loss of the switching loss, only the current diversion in turn-off transition is addressed. It could be concluded that the proposed CSD can achieve bipolar gate drive waveforms because of the diversion of the $D_{s1} \sim D_{s5}$ during turn-off transition.

D. Advantages of the Proposed Bipolar CSD

The proposed CSD circuit in this paper has the following advantages:

1. Significantly Reduced Turn-Off Time and thus Turn-Off Loss.

During the turn-off transition, the gate discharge current is not diverted through the diode set $D_{s1} \sim D_{s5}$ until the gate voltage reaches a much lower voltage (-3.5V) due to the increases or decreases of the current through the power MOSFET. When current decreases during turn-off transition, $V_{GS}=0.5$ V for VSD because of the on resistance of the driver switch, S_N , in Fig. 1; for CSD in Fig. 4, $V_{GS}=-0.7$ V because of the conduction of D_4 ; while for the bipolar CSD in Fig. 8, $V_{GS}=-3.5$ V because of the conduction of $D_{s1} \sim D_{s5}$.

Simulations under the same condition for VSD, the existing CSD in [23] and [24] and the proposed CSD are conducted with SIMetrix to verify the benefit of the proposed CSD. In comparison with the turn-off waveforms of the existing CSD in Fig. 7, the turn-off waveforms of the proposed CSD are shown in Fig. 12. Fig. 13 summarizes the comparison of the current fall time and the average discharging current among the proposed CSD, existing CSD and VSD. It is observed that, for the proposed CSD, it takes 8.7 ns for i_{DS} to decrease from 30A to 0, which is about half of the time needed for existing CSD (15.6 ns) and one third of the time needed for VSD (20.1 ns).

The reason for the significant improvement of the proposed CSD over the existing gate drivers (VSD and existing CSDs) is because that the gate discharge current i_G of the proposed CSD is greatly increased. It is observed from Fig. 13 that the average discharge current i_G of the proposed CSD is four times of that of VSD and twice of that of existing CSD.

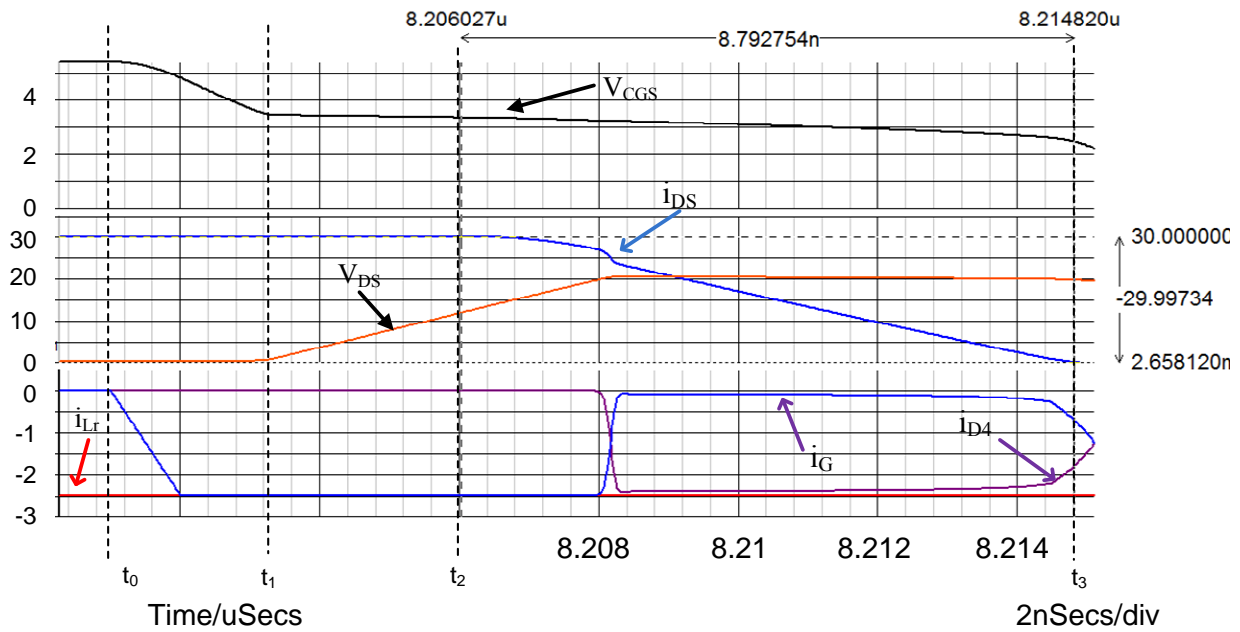


Fig. 12 Simulation waveforms of turn-off transition of proposed CSD

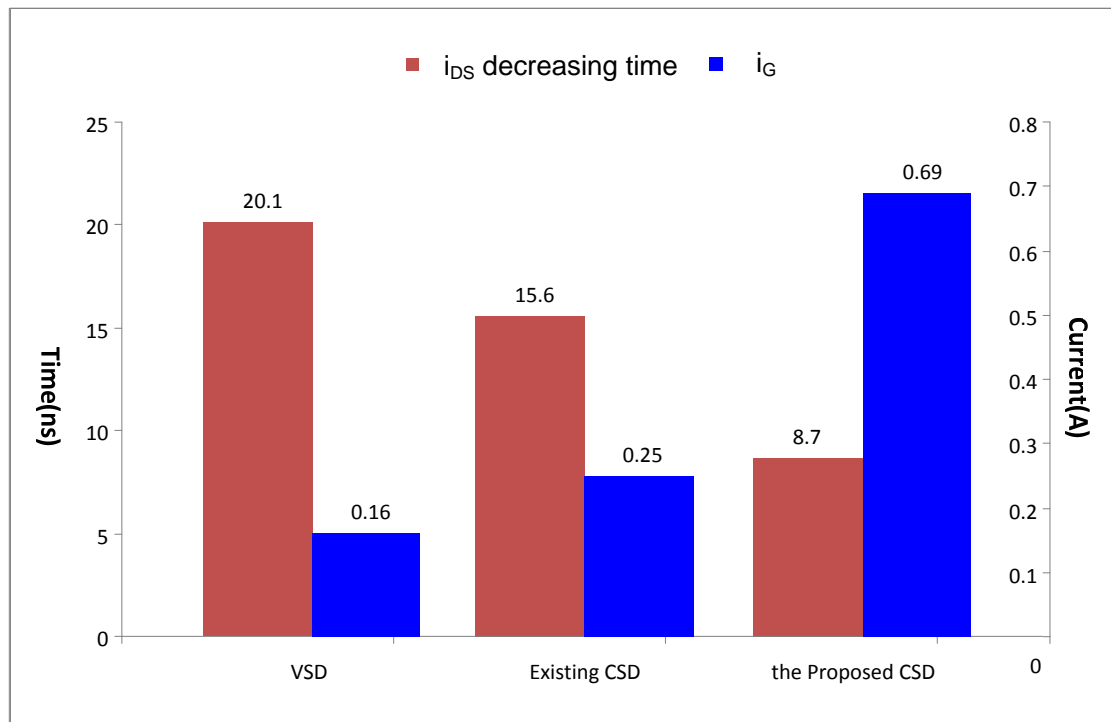


Fig. 13 Comparison of the simulated current fall time and the average discharging current

In order to support the simulation results above, calculations have been done with piecewise linear approximation model [27]. According to the datasheet of power MOSFET Si7386DP used in the simulation [29], gate resistance $R_G=1.7\Omega$. The voltage across the L_s for VSD, existing

CSD and proposed CSD during i_{DS} falling time are calculated and compared in Table I. i_G is obtained from Fig. 13; V_{CGS} is derived by Equation (4) according to piecewise linear approximation; $L_s di_{DS}/dt$ is calculated through Equation (1).

Table I. Comparison of VSD, existing CSD and proposed CSD during turn-off

Driver Type	V_{GS}	i_G	$i_G R_G$	V_{CGS}	$L_s di_{DS}/dt$
VSD	0.5 V	0.16 A	0.27V	2.7 V	1.93 V
Existing CSD	-0.7 V	0.25 A	0.43V	2.7 V	2.98 V
Proposed CSD	-3.5 V	0.69A	1.17V	2.7 V	5.03 V

From Table I, it is observed that the $L_s di_{DS}/dt$ of proposed CSD is around twice of the existing CSD in [23] and [24] and three times of the conventional VSD. In other words, the proposed CSD can decrease the current i_{DS} at a speed of twice of the existing CSD and three times of the VSD, which matches with the simulation results in Fig. 13.

$$V_{CGS} = \frac{V_{pl} + V_{th}}{2} \quad (4)$$

where V_{CGS} is the voltage across the gate-to-source capacitance of the MOSFET Q, V_{pl} means the Miller plateau voltage of Q, and V_{th} is the gate threshold voltage of Q.

2. Better Immunity to Voltage across R_G .

Compared with the VSD and the existing CSD in [23] and [24], the proposed CSD has better immunity to the voltage drop across R_G . As is illustrated in Table I, the proposed CSD can handle 1.17V voltage drop across R_G , while VSD only can handle 0.27V and the existing CSD can handle 0.43V. The larger voltage drop the gate driver can handle, the faster turn-off speed it can achieve. Therefore, the proposed CSD can turn off the power MOSFET with a faster speed than VSD and the existing CSD in [23] and [24].

3. Less Impact of Parasitic Inductance

Whether in the conventional VSD or the existing CSDs, the parasitic inductance, especially common source inductance, significantly reduces the switching speed and hereby increases the switching loss [22]. The proposed bipolar CSD can well alleviate the impact of parasitic inductor

with V_{GS} clamped to a flexible negative voltage (such as -3.5V), which can reduce the turn-off time and hereby improve the efficiency.

4. Smaller Current Source Inductor

The CSD proposed in this paper works in discontinuous current mode, which allows the current source inductor to be very small (tens of nH). It is expected that, with better on-chip inductor techniques on the way, the CSD inductor can be fully integrated into the driver chip in the near future.[30]

5. High Stability and Noise Immunity

The MOSFET is either actively clamped to V_c during on or to zero during off, which will minimize the possibility for MOSFET to be false triggered by Cdv/dt effect and increase the stability of the circuit.

6. Application Extension to other CSDs

The idea presented in this paper can be used to further alleviate the gate current diversion problem during turn-on transition. Fig. 14 shows the topology of a new bipolar CSD with improved turn-on gate current. The CSD in Fig. 14 increases the gate current during turn-on transition based on the same idea presented in this paper. However, it is noted that, since turn-on loss is relatively small compared with turn-off loss, the improvement of the CSD during turn-on transition in Fig. 14 would be less significant than the improvement of the CSD during turn-off transition proposed in this paper.

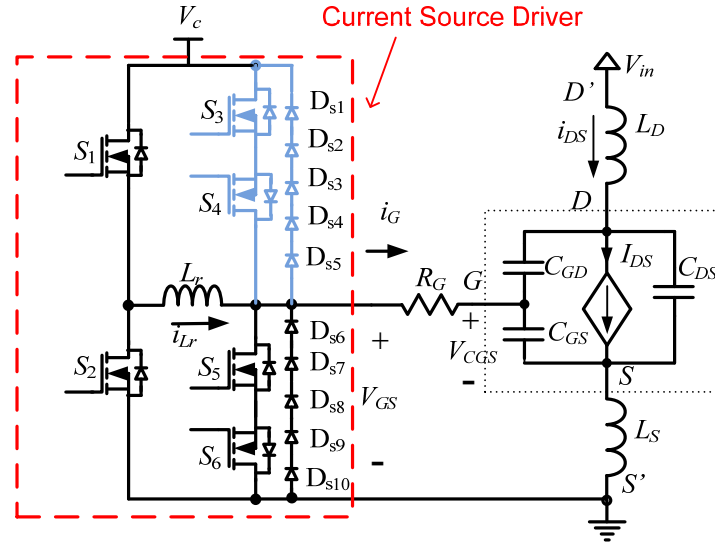


Fig. 14 New bipolar CSD with improved turn-on gate current

Another advantage of the bipolar CSD proposed here is that it can be widely extended to all other existing CSDs to further improve the turn-off speed. Fig. 15 illustrates the improved bipolar CSD operating with continuous inductor current mode to drive both the control FET and SR of the synchronous buck converter [21]. While another improved bipolar CSD with continuous inductor current mode is presented in Fig. 16, which enables magnetic integration of inductor L_{r1} and L_{r2} [22]. In Fig. 17, a discontinuous inductor current mode CSD [26] is improved using the idea presented in this paper to achieve bipolar switching waveforms. It is noted that all the improved portion of the three CSDs are marked in blue colors.

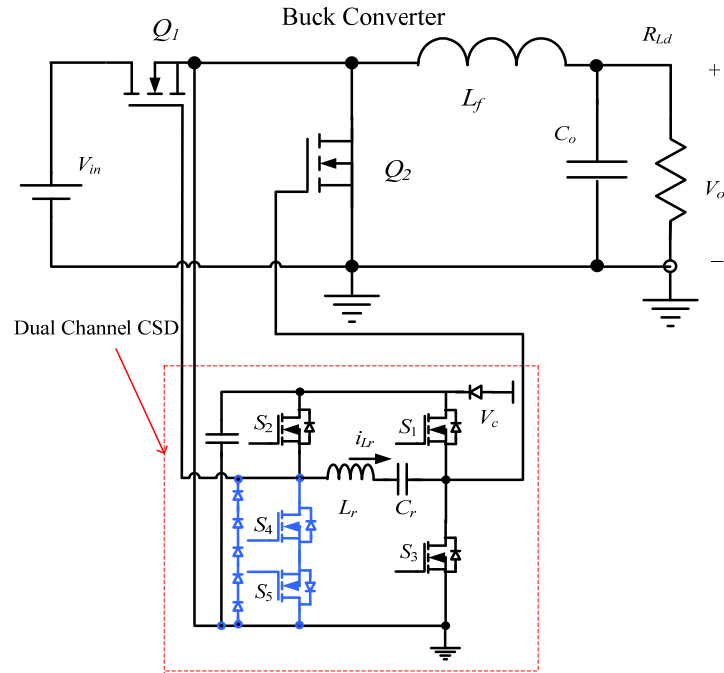


Fig. 15 Improved dual channel bipolar CSD with continuous inductor current mode

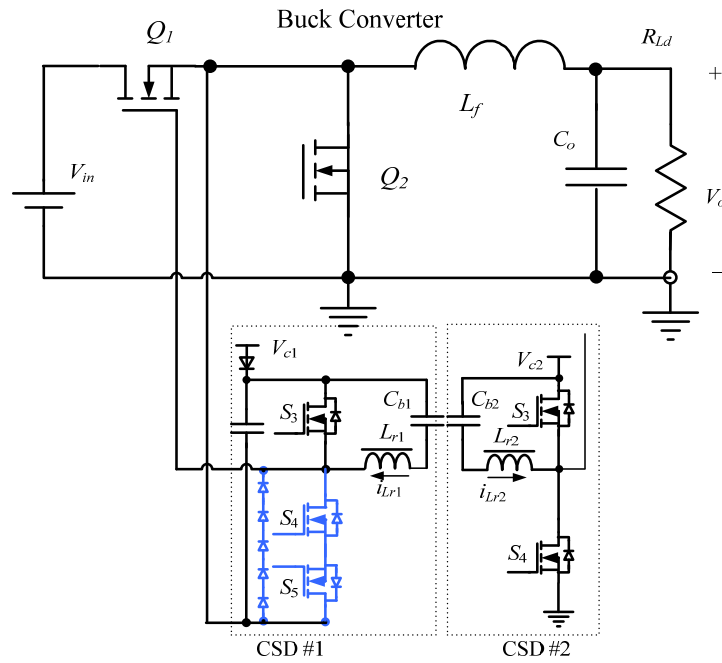


Fig. 16 Improved bipolar CSD working with continuous inductor current mode

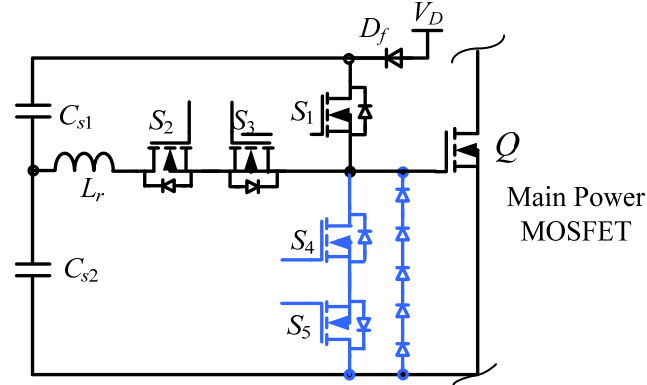


Fig. 17 Improved bipolar CSD working with discontinuous inductor current mode

IV. EXPERIMENTAL VERIFICATION AND DISCUSSION

A prototype for a synchronous buck converter shown in Fig. 18 was built to verify the advantages of the proposed CSD circuit. The control FET of the buck converter is driven by proposed CSD, while the SR is driven by the conventional VSD as the switching loss of the SR is very small. The design parameters are given in Table II.

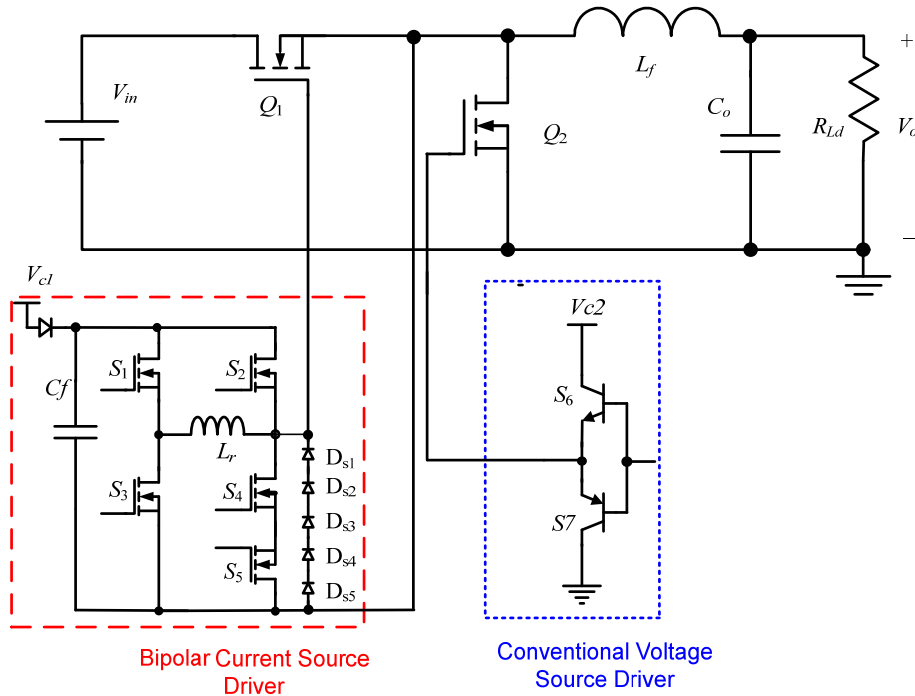


Fig. 18 Buck converter with the proposed bipolar CSD

Table II. Design parameters

Switching Frequency, f_s	1MHz
Input Voltage, V_{in}	12V
Output Voltage, V_o	1.2 and 1.3V
SR Gate Drive Voltage, V_{c2}	6.5V
SR, Q_2	IRF6691
CSD Voltage, V_{c1}	5V
Control FET, Q_1	Si7386DP
Output Inductor, L_f	330nH, Vishay IHLP5050CE
Driver Switches, $S_1 - S_5$	FDN335N
Driver Inductor, L_r	43nH, Coilcraft B10T_L
Diodes, $D_{s1} - D_{s5}$	MBR0520

The photo of the prototype is illustrated in Fig. 19. It uses 6-layer, 4-oz copper PCB. Fig. 20 illustrates the hardware implementation of the proposed CSD. Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. Driver switches $S_1 \sim S_5$ are driven with the level shift circuits.

The level shift circuits for $S_1 \sim S_5$ are implemented by discrete components from Intersil ISL6207 as shown in Fig. 21. The operating principle is as follows:

The voltage to turn on the driver switch ($S_1 \sim S_5$) is supported by the capacitance C_b . The voltage across C_b is built up when the source terminal of the driver switch equals GND, which allows C_b to be charged to V_c .

When the output of the CPLD is “High”, the gate-to-source voltage of the driver switch equals the voltage across C_b ; while when the PWM is “Low”, the gate-to-source voltage of the driver switch equals zero.

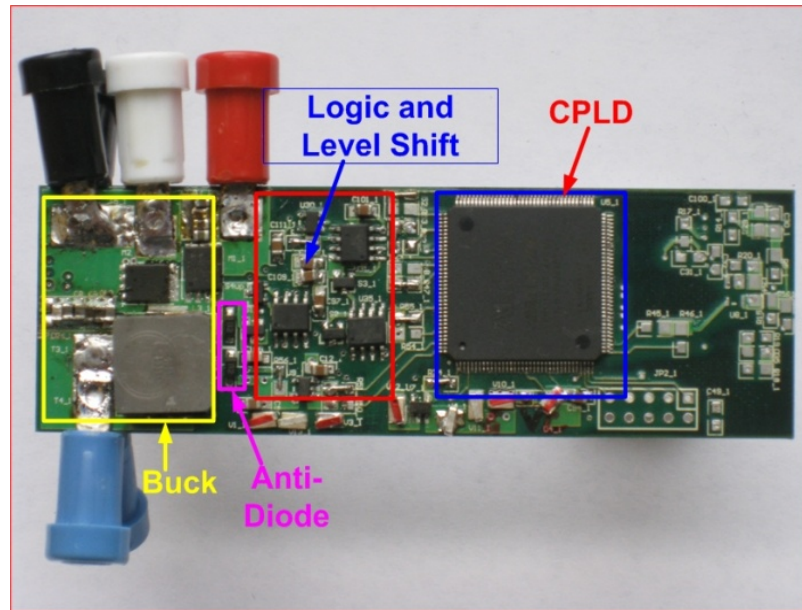


Fig. 19 Photo of prototype with proposed bipolar CSD

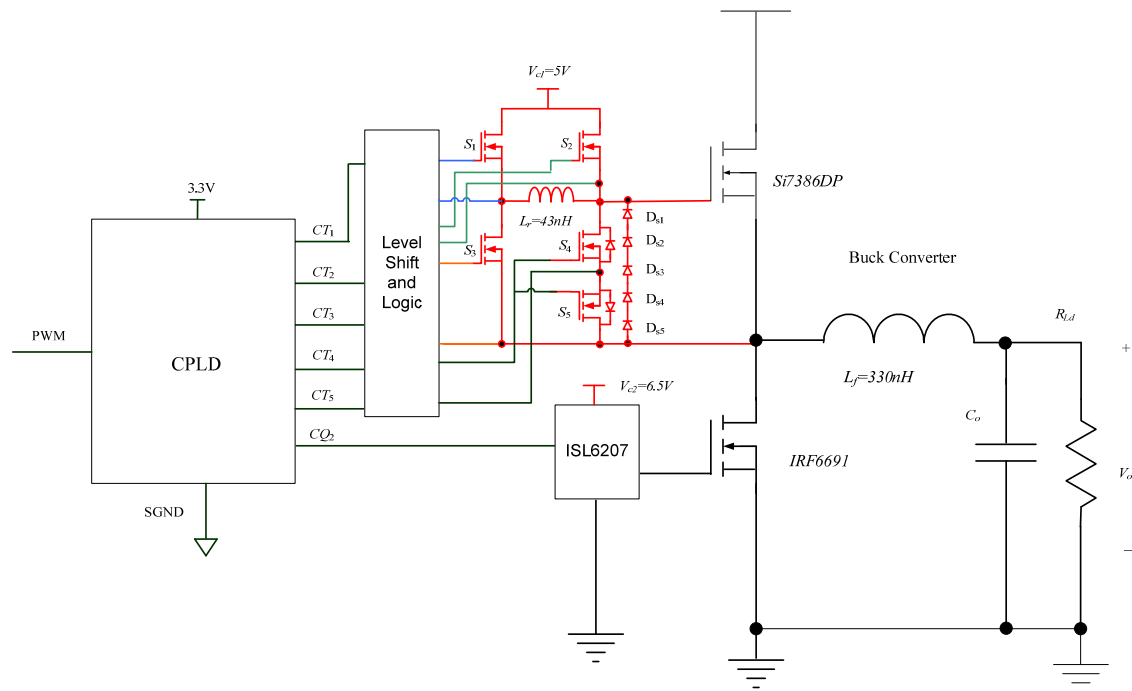


Fig. 20 Hardware implementation of the buck converter driven with the proposed CSD

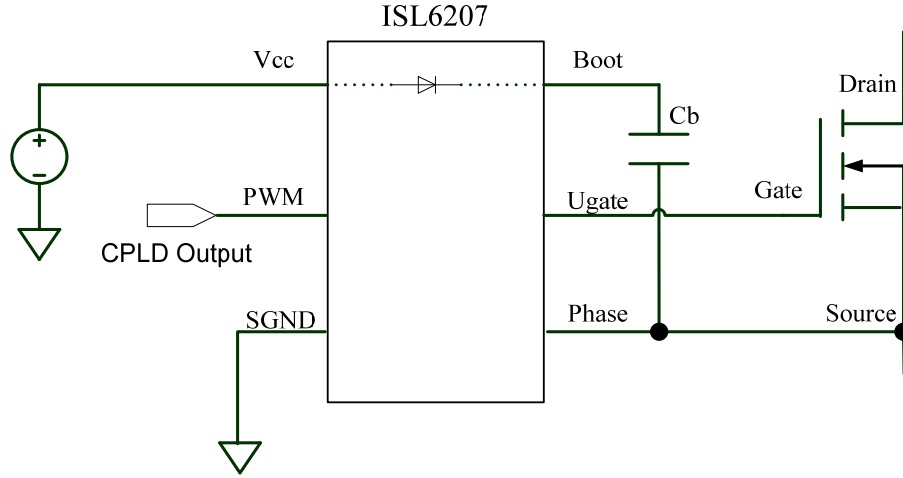


Fig. 21 Implementation of level shift circuits by ISL6207

Fig. 22 shows switch gate signals, V_{GS1} - V_{GS5} and associated modes for turn-on and turn-off transition respectively.

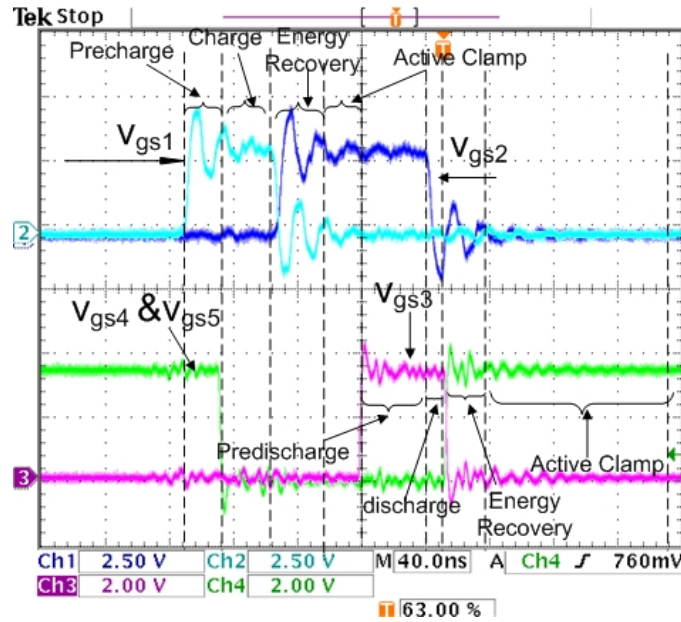


Fig. 22 Driver switch gate signals (V_{GS1} - V_{GS5})

Fig. 23 illustrates that driver inductor current i_{Lr} and the gate-to-source voltage $V_{GS_{Q1}}$ of control FET. It can be observed that Q_1 is charged and discharged with nearly constant current and $V_{GS_{Q1}}$ is clamped to about -3.5V during turn-off transition. Most importantly there is no Miller Plateau observed in $V_{GS_{Q1}}$. It is noted that the effective charge current, i_{G_s} , is hard to

measure without disturbing the circuit operation. Therefore, the measured waveform of i_G is not provided in this paper.

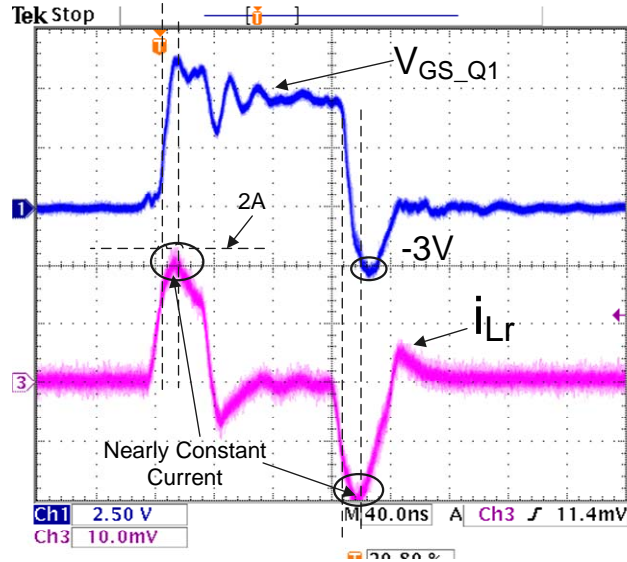


Fig. 23 V_{GS_Q1} and CSD inductor current I_{Lr}

The gate to source voltage waveforms for control FET and SR are shown in Fig. 24. It is observed that the dead time between V_{GS_Q1} and V_{GS_Q2} is minimized to avoid body diode conduction without causing shoot through problem.

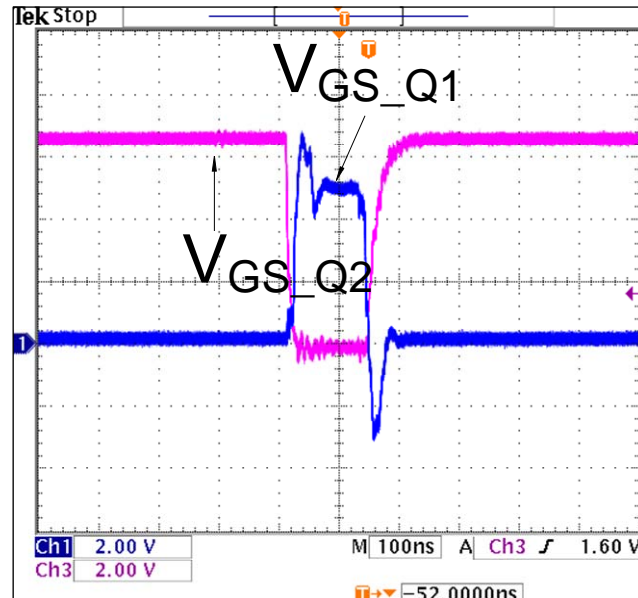


Fig. 24 V_{GS_Q1} & V_{GS_Q2}

Fig. 25 summarizes the measured efficiencies (including gate drive loss) of the proposed CSD in 1.2V and 1.3V output in 1MHz switching frequency with 12V input.

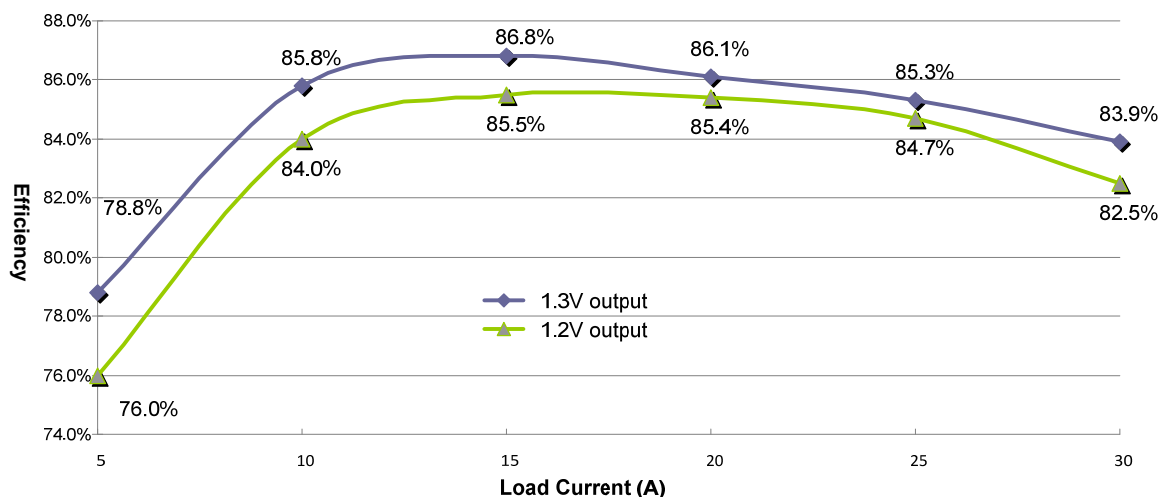


Fig. 25 Efficiencies at 12V input, 1.2V and 1.3V output, 1MHz switching frequency

Fig. 26 shows the efficiency comparison among the proposed bipolar CSD, existing CSD proposed in [23] and [24] and the conventional VSD at 12V input, 1.2V output and 1MHz switching frequency. It is noted that the proposed bipolar CSD increases the efficiency of VSD from 73.1% to 82.5% by 9.4% at 1.2V/30A output and improves the efficiency of the existing CSD from 80.5% to 82.5% by 2% at 30A output.

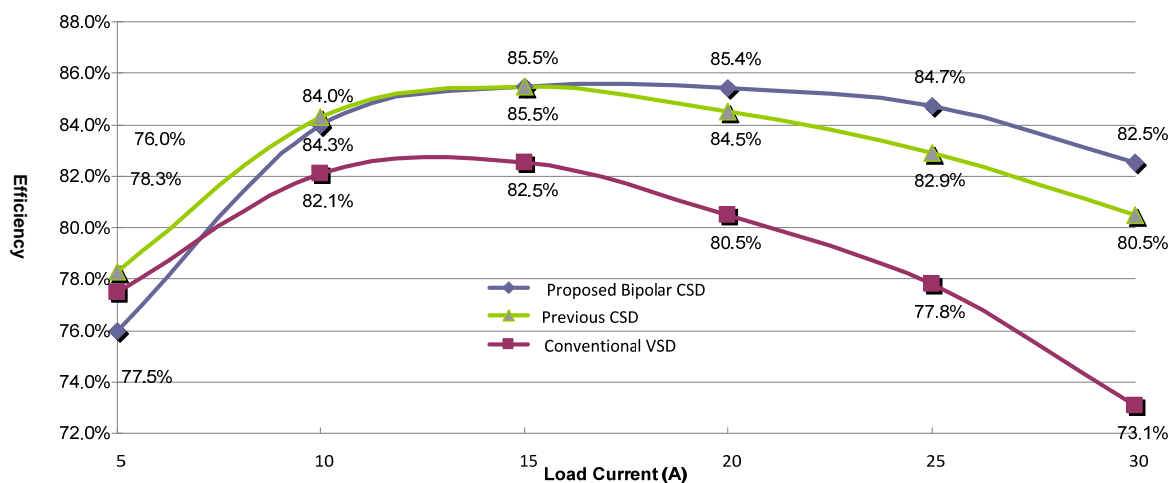


Fig. 26 Measured efficiency comparison at 12V input, 1.2V output, 1MHz switching frequency

Fig. 27 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, existing CSD proposed in [23] and [24] and the conventional VSD at 12V input, 1.2V output and 1MHz switching frequency. It is noted that compared with existing CSD, the proposed CSD saves a 1.08W loss at 30A load. While compared with the conventional VSD, the proposed CSD achieves a loss saving of 5.61W at 30A load.

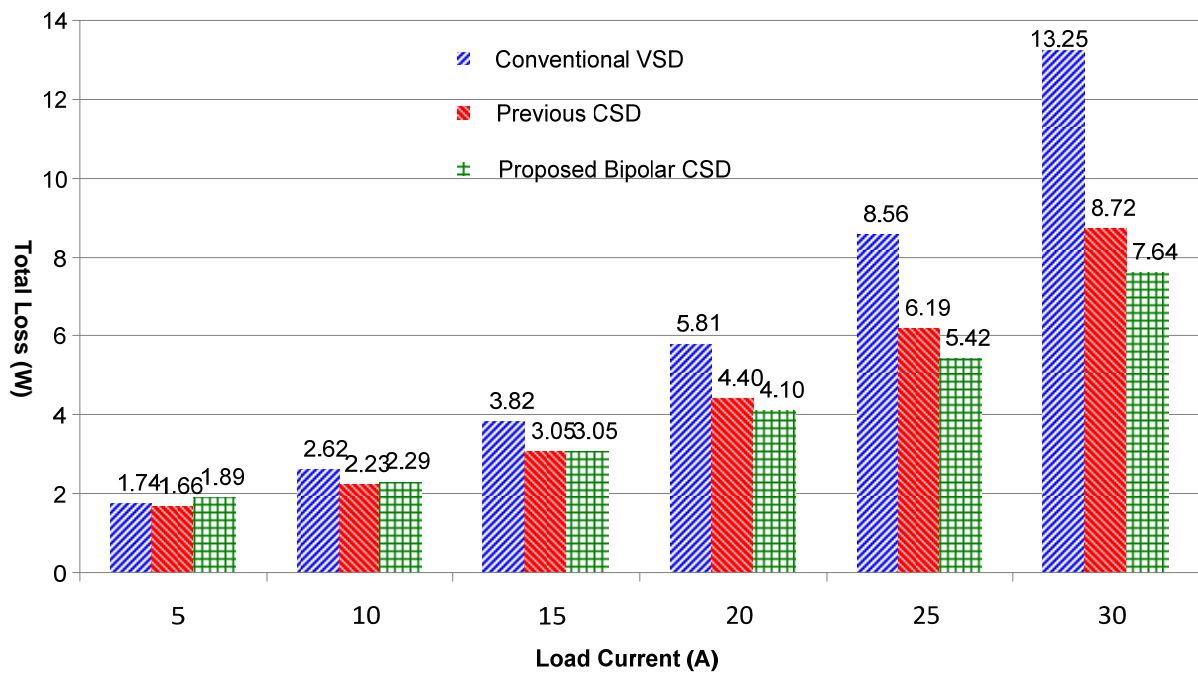


Fig. 27 Total measured loss comparison at 12V input, 1.2V output, 1MHz switching frequency

Fig. 28 shows the efficiency comparison among the proposed bipolar CSD, existing CSD proposed in [23] and [24] and the conventional VSD at 12V input, 1.3V output and 1MHz switching frequency. It is noted that, compared to the conventional VSD, the proposed bipolar CSD increases the efficiency of VSD from 77.5% to 83.9% by 6.4% and improves the efficiency of the existing CSD from 81.9% to 83.9% by 2% at 30A output.

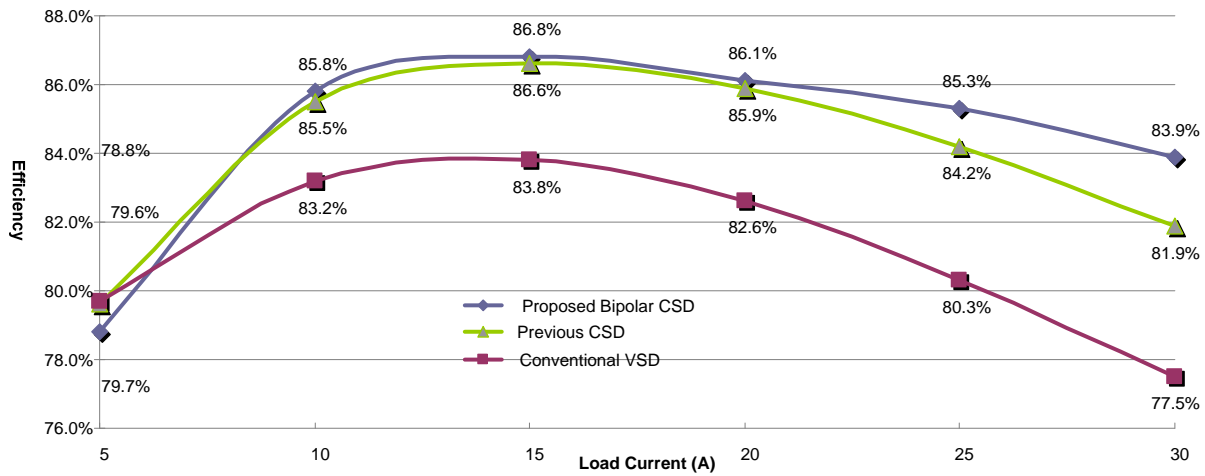


Fig. 28 Measured efficiency comparison at 12V input, 1.3V output, 1MHz switching frequency

Fig. 29 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, existing CSD proposed in [23] and [24] and the conventional VSD at 12V input, 1.3V output and 1MHz switching frequency. It is observed that the proposed bipolar CSD achieves a loss reduction of 3.84W at 30A load compared with VSD. Even compared with CSD in [23] and [24], the proposed bipolar CSD save a loss of 1.14W. It is also observed that the proposed CSD achieves higher efficiency improvement at high load current. This is because the proposed CSD significantly alleviates the gate current diversion problem at high current load.

The VR spends 20% of the time at the full load and spend the other 80% time at light load which is defined as any load below the full load [31]. The main intention of this paper is to propose a negative turn-off technology to reduce the switching loss. The proposed CSD has achieved visible improvement above 70% load; and it could also achieve high efficiency at other load by proper design: in light load, active phase number of the multiphase buck converter can be reduce to make each phase operate at heavy load [32], [33]; while in every light load (<10A), the CSD can be disabled and replaced by the VSD to maintain high efficiency.

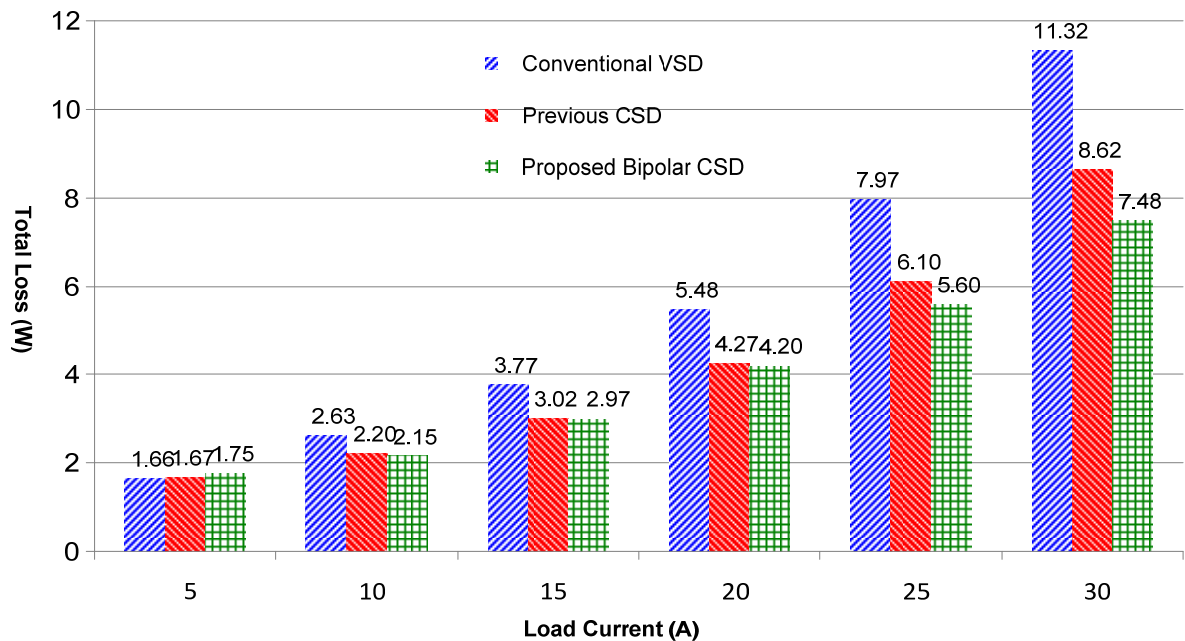


Fig. 29 Total measured loss comparison at 12V input, 1.3V output, 1MHz switching frequency

V. CONCLUSIONS

In this paper, a new bipolar CSD which can achieve much faster switching speed is proposed. The gate current diversion problem that exists in the existing CSDs is analyzed. Compared with previous gate drivers (VSD and existing CSDs), the proposed CSD can turn off the power MOSFET with a flexible negative voltage (such as -3.5V) to accelerate the turn-off speed. The experimental results demonstrate the significant efficiency improvement over the conventional VSD with a 5.62W loss reduction at 1.2V/30A output and a 3.84W loss reduction at 1.3V/30A with 12V input in 1MHz switching frequency. The comparison between the proposed CSD and the existing CSD in [23] and [24] demonstrates the CSD proposed in this paper is a better alternative for next generation VRs. More importantly, the basic idea presented in this paper can be also extended to other existing CSD drivers to further improve their performance with high output current.

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