# Single-Stage LED Driver Achieves Electrolytic Capacitor-Less and Flicker-Free Operation With Unidirectional Current Compensator

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*Abstract*—AC-connected light emitting diode (LED) drivers experience imbalanced energy between input and output in a half-line cycle. To achieve the flicker-free operation, the imbalanced energy needs to be buffered, often by energy-dense electrolytic capacitors. However, electrolytic capacitors are also well-known for their short lifespan. These capacitors are the limiting factor of an LED drivers' lifespan. High voltage film capacitors and a buck converter have been used in the proposed LED driver to buffer the imbalanced energy. When $P_{in} > P_{LED}$, the extra energy is transferred from the ac input directly to the high voltage film capacitors. When $P_{in} < P_{LED}$, the energy is transferred from the high voltage film capacitors to the output by the buck converter. The imbalanced energy goes through two power conversion steps in the proposed LED driver, which is one time less than other comparable electrolytic capacitor-less designs, enabling a higher efficiency to be achieved. A 28 W flyback topology based experimental prototype had been built and tested to verify the proposed design.

*Index Terms*—AC-connected light emitting diode (LED) driver, electrolytic capacitor-less, energy buffering, flicker-free operation, high power factor.

## I. Introduction

LIGHT emitting diodes (LEDs) are a great technological advancement in the lighting industry and have the potential to fundamentally change the future of lighting. They offer numerous advantages over conventional incandescent, neon, and fluorescent lighting devices; most notably their extended lifespan, reduced energy consumption, and low maintenance requirements. The potential energy savings offered by LED lighting are phenomenal. It is estimated that LED lighting could save 348 trillion watts hours of electricity per year by 2027, which equates to the power generated by 44 large power plants, and more than US$ 30 billion at today's electricity prices [1].
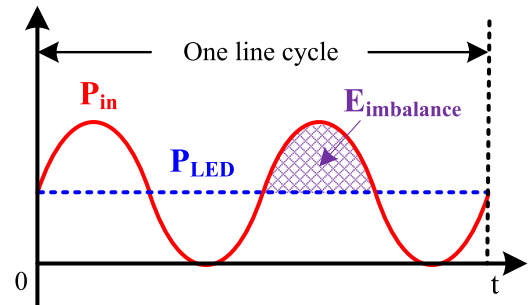
Fig. 1.　Energy imbalance between input and output in an ac-connected LED driver.

LED lighting fixtures are rapidly expanding into many applications as their price continues to fall. The global LED lighting market hit US$ 26.09 billion in 2016 and is expected to reach US$ 54.28 billion by 2022, with an annual growth rate as high as 13% between 2017 and 2022 [2].

An LED driver is the interface between a power source and an LED load, and is required to achieve a proper operation. The LED driver is a critical component in an LED lighting fixture and ultimately determines the cost, size, reliability, and light quality. Advancements in LED driving technology have a great impact on the widespread adoption of LED lighting. Although using LED lighting offers significant advantages, the design of LED drivers can be very challenging. This is especially true when dealing with an ac-connected LED driver, where a lot of rigorous industry standards and regulations kick in. For example, EnergyStar requires power factor correction (PFC) implementation with ac-connected LED drivers. They should have a PF higher than 0.7 for residential usage and 0.9 for commercial usage. In addition, there is also IEC61000-3-2 that imposes limitations on input harmonic currents. To meet these requirements, active PFC technology is usually implemented with ac-connected LED drivers. As a result, the input power becomes a time-varying waveform and there is an imbalanced energy between input and output in a half-line cycle, as shown in Fig. 1. The imbalanced energy leads to many technical challenges that are a driving force behind today's LED lighting research.

In a conventional LED driver, the imbalanced energy is buffered by electrolytic capacitors, which are connected at the output of a PFC stage. This also leads to the generation

of a double-line-frequency ripple voltage at the PFC output. For a single-stage LED driver, the PFC is the only power stage, and therefore, the ripple voltage is directly applied to its LED load. The ripple voltage will produce a significant double-line-frequency ripple current as an LED load has very low intrinsic resistance. The ripple current presents itself as light fluctuation—commonly called flicker. Although double-line-frequency flicker is usually not visible, it has been linked to several serious health issues, such as headaches, fatigue, and even seizures [3]. Two-stage LED drivers are often used to achieve the flicker-free operation. In a two-stage driver, the ripple voltage from a PFC output is filtered by a second-stage converter. This converter removes the double-line-frequency ripple, providing a dc LED voltage at the output of the second-stage converter to achieve the flicker-free operation. The two main drawbacks of two-stage LED drivers are extra power loss from the second power stage, which generally results in a lower efficiency and a higher component count. For example, in a two-stage design with the first stage being a flyback PFC and the second stage being a buck converter, the extra loss generated by the buck converter will reduce the overall efficiency. It is possible to achieve the high efficiency with a two-stage design, such as a boost PFC and an *LLC* converter; however, due to the highly expensive component count, this solution is usually adopted for much higher power applications [27], [28] where the cost is not a critical concern.

In addition to avoiding flicker, extending the lifespan of LED drivers is also paramount. Electrolytic capacitors are often used in conventional designs to buffer the double-line-frequency imbalanced energy. The drawback of using an electrolytic capacitor is their limited lifespan. Although the life of electrolytic capacitors can vary based on the operating temperature and ripple current, it is usually in the range of 1000–10 000 h [4]. The electrolyte gradually dissipates in electrolytic capacitors and capacitance will be reduced over time. LEDs, however, are semiconductor chips that can achieve several decades of lifespan. Therefore, it is critical to eliminate electrolytic capacitors in LED driver designs to achieve significant lifespan extension of LED lighting fixtures.

A variety of LED driving methods had been proposed attempting to reduce flicker, improve efficiency, reduce cost, and eliminate electrolytic capacitors. These previous LED driving methods can be broadly categorized as follows.

1) Input harmonic currents injection methods [5], [6]. Higher order harmonic currents are added to the fundamental ac input current to reduce the imbalanced energy in a half-line cycle. Using this technique, the double-line-frequency ripple voltage at the output of a single-stage LED driver can be reduced as well as flicker.

2) Two-stage integrating methods [7]–[9]. The first-stage PFC and the second-stage dc–dc converter are combined to share power components. These technologies can reduce cost, but sharing components introduces additional constraints on design and operation, which may be unsuitable in certain applications.

3) Ripple voltage cancelation methods [10]–[15]. An opposite ripple voltage is generated and used to cancel the double-line-frequency ripple voltage produced by the
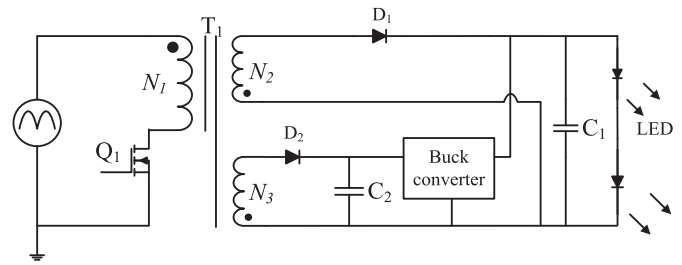


Fig. 2. LED driving method proposed in [26].

main PFC stage of an LED driver. A dc LED voltage can be produced and applied to an LED load to achieve flicker-free LED driving.

4) Active filtering and three-port methods [16]–[18]. The imbalanced energy between the ac input and the LED output is buffered by the film capacitors. A bi-directional dc–dc converter is used to transfer the imbalanced energy between the main circuit and the film capacitors.

5) And other LED driving methods that do not fall into the above-mentioned categories, such as the output current shaping LED driver [19], the two parallel inverted buck converter average current modulation LED driver [20], the averaged LED current modulation method [21], the stacked switch capacitor LED driver [22], the valley-fill LED driver [23]–[25], and the one and a half-stage LED driver [26]. The topology presented in [26], also shown in Fig. 2, may look similar to the topology proposed in this paper; however, it is operated in a very different way. For the topology in [26], in every switching cycle, the energy from the ac input is delivered to the main output capacitor $C_o$ and the storage capacitor $C_{\text{sto}}$. For this topology, the energy transfer process between the two paths is not controllable. In other words, the energy that needs to be buffered cannot be controlled, leaving a significant double-line-frequency output ripple voltage on the LED load, as evidenced in the paper. On the contrary, a key feature of the proposed LED driver, which is illustrated in Fig. 5, is that the amount of energy being delivered to either $C_o$ or $C_{\text{sto}}$ can be well controlled by operating two switches, $S_1$ and $S_2$. Therefore, precise energy buffering can be achieved so that the instantaneous output power is always a constant.

In this paper, a unidirectional current ripple compensator LED driver is proposed to eliminate electrolytic capacitors as well as achieve high power factor, flicker-free LED driving. This converter also offers a superior efficiency compared to a previous electrolytic capacitor-less design. A 28 W experimental prototype had been built and tested to verify the operating principles. The remainder of this paper is arranged as follows. The concept of the proposed LED driver is derived in Section II. The circuit implementation and detailed operating principle are discussed in Section III. The control strategy is discussed in Section IV, and the design analysis is discussed in Section V. Experimental results are discussed in Section VI, and the paper is concluded in Section VII.

Fig. 4. Concept of the proposed unidirectional ripple current compensation LED driver.
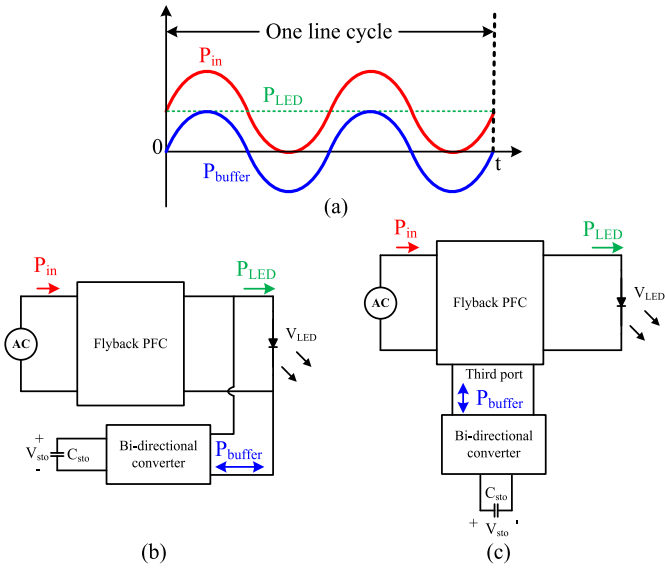


Fig. 3. Previous energy buffering LED driver without an electrolytic capacitor. (a) Key power waveforms. (b) Active filtering LED driver [16], [17]. (c) Three-port LED driver [18].

## II. IDEA OF THE UNIDIRECTIONAL CURRENT RIPPLE COMPENSATOR

Fig. 3 shows the key power waveforms of two existing energy buffering LED drivers. The input power $P_{in}$ is a time-varying waveform with its average being equal to the LED output power $P_{LED}$. The buffered power $P_{buffer}$, which is handled by the bi-directional converters in Fig. 3(b) and (c), is the difference between $P_{in}$ and $P_{LED}$. Fig. 3(b) shows the implementation of an active filtering LED driver. A bi-directional dc–dc converter is paralleled to the LED load to process imbalanced energy and buffers it with the storage capacitor $C_{sto}$. Fig. 3(c) shows the implementation of a three-port LED driver. A dedicated port is used to interfacing with the bi-directional converter to achieve energy buffering. Although the above-mentioned two methods utilize different circuit implementations and control strategies, in both cases the imbalanced energy must go through no less than three power conversion steps.

When $P_{in} > P_{LED}$, the imbalanced energy is transferred from the ac input to the dc output by the main PFC in the active filter LED driving method, experiencing the first power conversion step. The energy is then transferred from the dc output to the storage capacitor $C_{sto}$, by the bi-directional dc–dc converter; this is the second power conversion step. When $P_{in} < P_{LED}$, the imbalanced energy is transferred back from $C_{sto}$ to the LED load by the bidirectional dc–dc converter, experiencing the third power conversion step. In three-port LED drivers, the process is similar. $C_{sto}$ is built with a film capacitor to achieve extended lifespan. The drawback of active filter LED driving or three-port LED driver methods is the generation of significant power loss when buffering imbalanced energy. As described above, the imbalanced energy experienced three power conversion steps with the active filtering LED driving method. As a result, the efficiency of an active filtering LED driver or three-port LED driver is much lower than that of a conventional single-stage
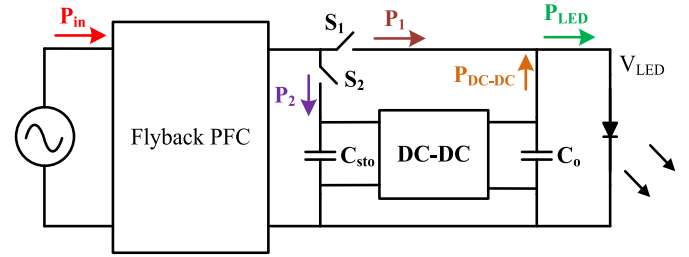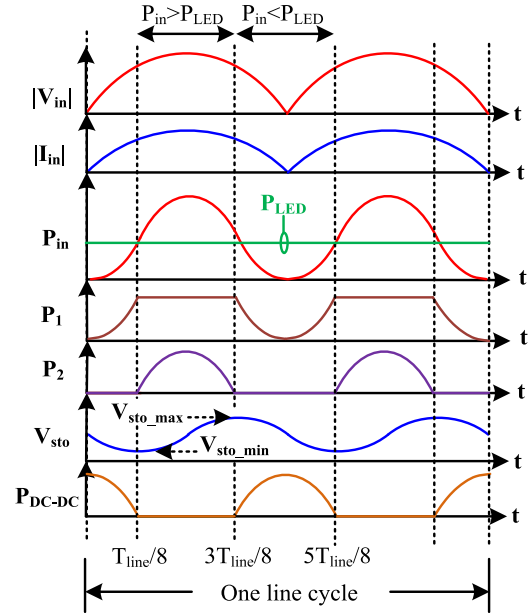


Fig. 5. Key line cycle waveforms of the proposed unidirectional current ripple compensation LED driver.

LED driver. This reduction in efficiency is also evidenced in [16].

The proposed unidirectional current ripple compensator LED driver aims to achieve reduced power conversion loss with the imbalanced energy by restructuring the energy buffering process. The concept of the proposed LED driver is shown in Fig. 4 and the key waveforms in a line cycle are shown in Fig. 5. A flyback PFC is used at the first stage to achieve a high power factor. A total of two switches, $S_1$ and $S_2$, are used to control the energy flow. When $P_{in} < P_{LED}$, the switch $S_1$ is turned ON, while $S_2$ is OFF. In this way, the power delivered to the LED load from ac input $P_1$ is equal to the input power. At the same time, additional energy will be transferred from $C_{sto}$ to the LED load by the dc–dc converter to make up the difference between $P_{in}$ and $P_{LED}$. When $P_{in} > P_{LED}$, by controlling the ON time of $S_1$ and $S_2$ in one switching cycle, the instantaneous ac input power can be split into $P_1$ and $P_2$ with precision. The control circuit design will ensure that $P_1 = P_{LED}$ during this condition, while the excess energy, $P_2 = P_{in} - P_{LED}$, from the ac input will be stored in $C_{sto}$. Under a steady state, the energy stored in $C_{sto}$ during $P_{in} > P_{LED}$ is equal to the amount it releases when $P_{in} < P_{LED}$.
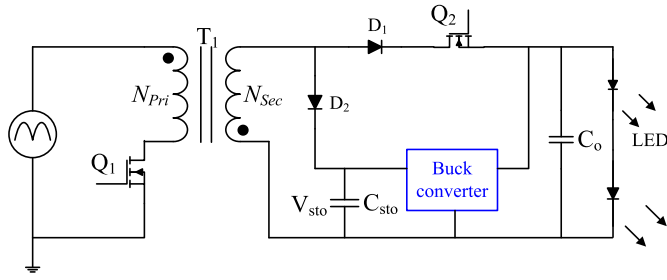
Fig. 6. Circuit implementation of the unidirectional ripple current compensation LED driver.

The above-mentioned description reveals that the imbalanced energy experiences only two power conversion steps in the proposed LED driver. By directly attaching $C_{sto}$ to the main flyback PFC, the extra energy is directly transferred from the ac input to $C_{sto}$, when $P_{in} > P_{LED}$, without the extra power conversion process with a bi-directional converter. One less power conversion step is achieved with the imbalanced energy as compared to active filtering LED drivers. The process of transferring energy back from $C_{sto}$ to LED load is the same with the proposed LED driver and the active filtering LED drivers. It should note that the dc–dc converter is unidirectional in the proposed LED driver.

## III. CIRCUIT IMPLEMENTATION AND OPERATING PRINCIPLE

Fig. 6 shows the circuit implementation of the proposed unidirectional current ripple compensation LED driver. The LED driver includes the main flyback PFC, a buck converter, and one energy channeling MOSFET $Q_2$. In Fig. 4, two switches are needed in the conceptual design to achieve power splitting. By carefully designing the storage capacitor voltage $V_{sto}$, one MOSFET in the design can be removed while achieving energy splitting. More specifically, to achieve this, the voltage $V_{sto}$ needs to be always higher than $V_{LED}$. If this condition is met, then when the MOSFET $Q_2$ is OFF, the current in the secondary side of the transformer $T_1$ only flows in $D_2$, during which the energy is delivered to the storage capacitor $C_{sto}$. When $Q_2$ is turned ON, the secondary-side current flows in $Q_2$ and $D_1$. The voltage across the winding $N_{sec}$ is clamped at $V_{LED}$ (by ignoring the forward voltage drop on $D_1$ and the voltage difference between the drain and the source terminals of $Q_2$). Therefore, if $V_{sto} > V_{LED}$, the diode $D_2$ is reverse biased and blocks any current flow. As shown in Fig. 5, there is a significant ripple voltage on $V_{sto}$ at double-line frequency. The average voltage of $V_{sto}$ can be controlled by a voltage loop that is in Section IV. By selecting a proper capacitor $C_{sto}$, the ripple voltage amplitude on $V_{sto}$ can be controlled, which is explained in Section V. The goal is to keep $V_{sto\_min}$ higher than $V_{LED}$ to ensure $D_2$ remains correctly biased. The flyback PFC shapes the input current to achieve a high power factor and draws energy from the ac input. The buck converter provides the power difference when $P_{in} < P_{LED}$.

### A. Line Cycle Operation

First, the line cycle operation of the proposed LED driver is discussed and the key waveforms in Fig. 5 are also derived. Since a high power factor is achieved with the proposed LED

driver, the input current follows the input voltage. The rectified input voltage $|V_{in}(t)|$ and the rectified the input current $|I_{in}(t)|$ can be expressed as

$$|V_{in}(t)| = V_{in\_pk} \times |\sin(2\pi \times f_{line} \times t)| \quad (1)$$

and

$$|I_{in}(t)| = I_{in\_pk} \times |\sin(2\pi \times f_{line} \times t)| \quad (2)$$

where $f_{line}$ represents the mains frequency, $V_{in\_pk}$ and $I_{in\_pk}$ represent the peak input voltage and peak input current amplitude, respectively. Therefore, the input power, $P_{in}(t)$, can be expressed as

$$P_{in}(t) = V_{in\_pk} \times \sin(2\pi \times f_{line} \times t) \times I_{in\_pk}$$
$$\times \sin(2\pi \times f_{line} \times t)$$
$$= \frac{1}{2} P_{in\_pk} \times [1 - \cos(4\pi \times f_{line} \times t)]. \quad (3)$$

As indicated in (3), the input power $P_{in}$ is a sinusoidal waveform with a dc bias being equal to half the peak value. Assuming no power loss, the LED output power $P_{LED}$ will be equal to the averaged input power and it is a constant. The capacitor $C_{sto}$ is used to buffer the energy difference between the ac input and the LED output. Because the imbalanced energy is buffered by the storage capacitor and leads to a voltage change on $V_{sto}$, the relationship between the imbalanced energy $E_{imbalance}$ and the voltage change on $V_{sto}$, $\Delta V_{sto}$, can be expressed as

$$E_{imbalance} = \frac{1}{2} C_{sto}(V_{sto\_max}^2 - V_{sto\_min}^2)$$
$$= C_{sto}\left(\frac{V_{sto\_max} + V_{sto\_min}}{2}\right)(V_{sto\_max} - V_{sto\_min})$$
$$= C_s \times V_{sto\_avg} \times (\Delta V_{sto}). \quad (4)$$

In (4), $V_{sto\_avg}$ represents the averaged value of $V_{sto}$ in a half-line cycle. The imbalanced energy in a half-line cycle can also be calculated as

$$E_{imbalance} = \frac{1}{\pi} P_{LED} \times \frac{T_{line}}{2}. \quad (5)$$

Therefore, once $V_{sto\_avg}$ and $C_{sto}$ are determined in a design, the voltage change $\Delta V_{sto}$ as well as the minimum and maximum $V_{sto}$ can be calculated.

From $T_{line}/8$ to $3T_{line}/8$, the input power is higher than the LED output power. The difference between $P_{in}$ and $P_{LED}$, $P_2$, is used to charge the storage capacitor $C_{sto}$ and the voltage $V_{sto}$ rises in this period. The instantaneous voltage $V_{sto}(t)$, $V_{sto\_min}$, $C_{sto}$, $P_{in}(t)$, and $P_{LED}$ have the following relationship:

$$\frac{1}{2} \times C_{sto}[V_{sto}(t)^2 - V_{sto\_min}^2]$$
$$= \int_{\frac{T_{fline}}{8}}^{t} [P_{in}(t) - P_{LED}]dt$$
$$\text{When } \frac{T_{line}}{8} < t < \frac{3T_{line}}{8}. \quad (6)$$

During $3T_{line}/8$ to $5T_{line}/8$, $P_{in}$ is lower than $P_{LED}$. $S_1$ is fully ON so that $P_{in}$ is equal to $P_1$. Energy is taken from $C_{sto}$ and the
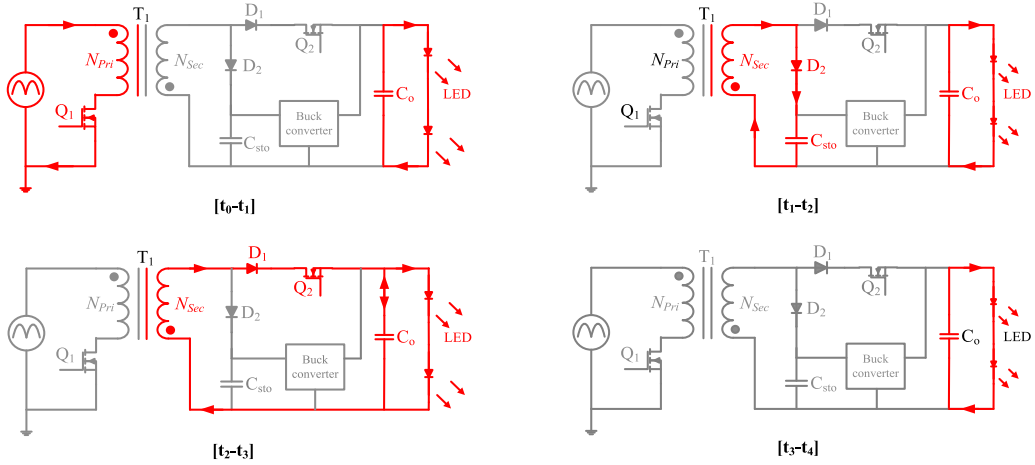
Fig. 7. Switching operation of the LED driver when $P_{\text{in}} > P_{\text{LED}}$ ($Q_2$ under leading edge modulation).

dc–dc converter delivers the difference in power between $P_{\text{in}}$ and $P_{\text{LED}}$ to the output. Therefore, the voltage $V_{\text{sto}}$ falls during this interval. The relationship among $V_{\text{sto}}(t)$, $V_{\text{sto\_max}}$, $C_{\text{sto}}$, $P_{\text{in}}(t)$, and $P_{\text{LED}}$ can be expressed as

$$\frac{1}{2} \times C_{\text{sto}}[V_{\text{sto}}(t)^2 - V_{\text{sto\_max}}^2] = \int_{\frac{3T_{f\text{line}}}{8}}^{t} [P_{\text{in}}(t) - P_{\text{LED}}(t)]dt$$

When $\dfrac{3T_{\text{line}}}{8} < t < \dfrac{5T_{\text{line}}}{8}$. (7)

Combining (3), (6), and (7), the voltage $V_{\text{sto}}$ can be expressed as

$$V_{\text{sto}}(t) =$$

$$\begin{cases} \sqrt{\dfrac{2 \times \int_{\frac{3T_{f\text{line}}}{8}}^{t} \left( \frac{1}{2} P_{\text{in\_pk}} \times [1 - \cos(4\pi \times f_{\text{line}} \times t)] \right) dt}{C_{\text{sto}}} + V_{\text{sto\_min}}^2} \\ \quad \dfrac{T_{\text{line}}}{8} < t < \dfrac{3T_{\text{line}}}{8} \\ \sqrt{V_{\text{sto\_max}}^2 - \dfrac{2 \times \int_{\frac{3T_{f\text{line}}}{8}}^{t} \left( \frac{1}{2} P_{\text{in\_pk}} \times [1 - \cos(4\pi \times f_{\text{line}} \times t)] \right) dt}{C_{\text{sto}}}} \\ \quad \dfrac{3T_{\text{line}}}{8} < t < \dfrac{5T_{\text{line}}}{8}. \end{cases}$$

(8)

The power $P_1(t)$, $P_2(t)$, and $P_{\text{dc}-\text{dc}}(t)$ can be written as

$$P_1(t) = \begin{cases} P_{\text{LED}} & \dfrac{T_{\text{line}}}{8} < t < \dfrac{3T_{\text{line}}}{8} \\ P_{\text{in}}(t) & \dfrac{3T_{\text{line}}}{8} < t < \dfrac{5T_{\text{line}}}{8} \end{cases}$$ (9)

and

$$P_2(t) = \begin{cases} P_{\text{in}}(t) - P_{\text{LED}} & \dfrac{T_{\text{line}}}{8} < t < \dfrac{3T_{\text{line}}}{8} \\ 0 & \dfrac{3T_{\text{line}}}{8} < t < \dfrac{5T_{\text{line}}}{8} \end{cases}$$ (10)

and

$$P_{\text{dc}-\text{dc}}(t) = \begin{cases} 0 & \dfrac{T_{\text{line}}}{8} < t < \dfrac{3T_{\text{line}}}{8} \\ P_{\text{LED}} - P_{\text{in}}(t) & \dfrac{3T_{\text{line}}}{8} < t < \dfrac{5T_{\text{line}}}{8} \end{cases}.$$ (11)

The above-mentioned line cycle operation provides an overview of the proposed unidirectional current ripple compensation LED driver. It is possible to use different topologies to achieve the above-discussed operation. The switching oper-
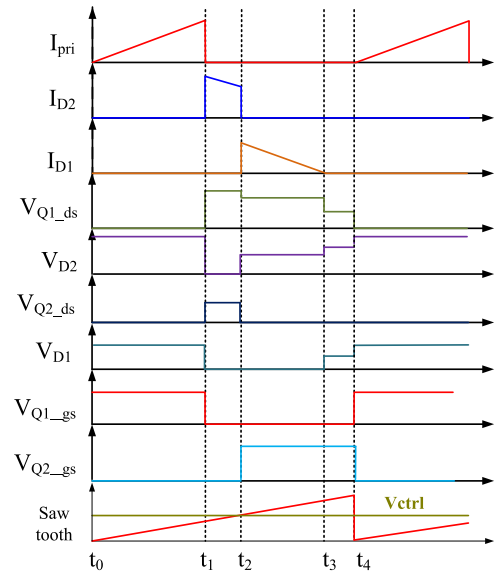


Fig. 8. Key switching waveforms of the proposed LED driver when $P_{\text{in}} > P_{\text{LED}}$ ($Q_2$ under leading edge modulation).

ation that is specifically for the proposed LED driver circuit is discussed below.

### B. Switching Operation

The flyback PFC in the proposed LED driver is operated under constant ON time, fixed switching frequency, and discontinuous conduction mode (DCM) to achieve a high PFC [27]. The design of the buck converter is very generic. To simplify the discussion, the buck converter is represented as a function unit and its switching operation is not of interest. The switching operations to achieve energy buffering are discussed in detail and separately for $P_{\text{in}} > P_{\text{LED}}$ and $P_{\text{in}} < P_{\text{LED}}$.

*1) When $P_{in} > P_{LED}$:* When $P_{\text{in}} > P_{\text{LED}}$, the buck converter is not active. One switching cycle is divided into four time intervals, $[t_0-t_1]$, $[t_1-t_2]$, $[t_2-t_3]$, and $[t_3-t_4]$. Fig. 7 shows the switching operation of each time interval, and Fig. 8 shows the key switching waveforms.
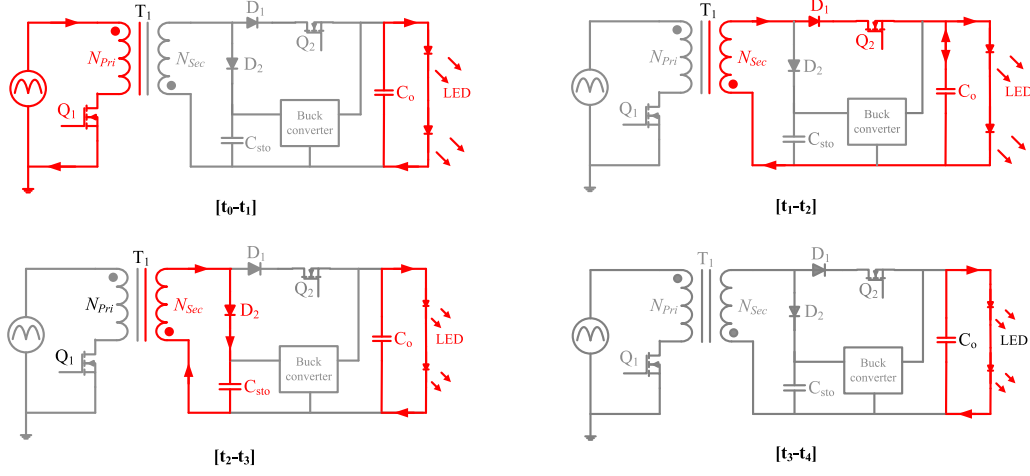
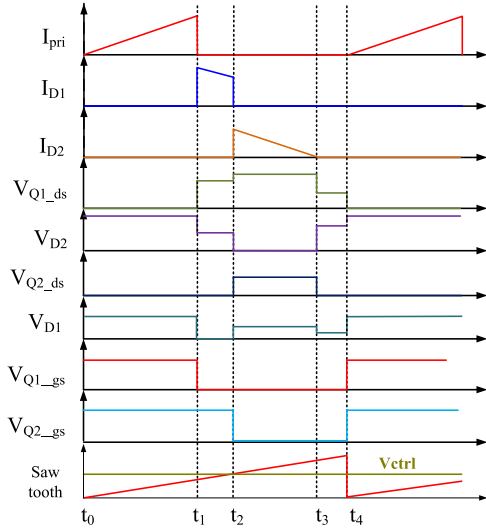Fig. 9. Switching operation of the LED driver when $P_{\text{in}} > P_{\text{LED}}$ ($Q_2$ under trailing edge modulation).



Fig. 10. Key switching waveforms of the proposed LED driver when $P_{\text{in}} > P_{\text{LED}}$ ($Q_2$ under trailing edge modulation).

*2) Time Interval $[t_0–t_1]$:* One switching cycle starts at time $t_0$ when $Q_1$ is turned ON. The switching current in winding $N_{\text{pri}}$, $I_{\text{pri}}$, starts increasing from zero. Due to the opposite orientation between the winding $N_{\text{pri}}$ and $N_{\text{sec}}$, the diodes $D_1$ and $D_2$ are reversely biased, while the body diode of $Q_2$ is forward biased. The voltage across the diodes $D_1$ and $D_2$ can be expressed as

$$V_{D_1(P_{\text{in}} > P_{\text{LED}})}[t_0 - t_1] = V_{\text{LED}} + V_{\text{in}} \times \frac{N_{\text{sec}}}{N_{\text{pri}}} \quad (12)$$

and

$$V_{D2(P_{\text{in}} > P_{\text{LED}})}[t_0 - t_1] = V_{\text{sto}} + V_{\text{in}} \times \frac{N_{\text{sec}}}{N_{\text{pri}}}. \quad (13)$$

This interval ends at time $t_1$ when the main MOSFET $Q_1$ is turned OFF. The switching current in $Q_1$ at time $t_1$ can be expressed as

$$I_{Q_1\_t_1(P_{\text{in}} > P_{\text{LED}})} = \frac{V_{\text{in}} \times (t_1 - t_0)}{L_{\text{pri}}}. \quad (14)$$

The averaged input current in this switching cycle can be expressed as

$$I_{\text{in\_avg}} = \frac{I_{Q_1\_t_1(P_{\text{in}} > P_{\text{LED}})} \times (t_1 - t_0)}{2 \times T_s} = \frac{V_{\text{in}} \times (t_1 - t_0)^2}{2 \times T_s \times L_{\text{pri}}}. \quad (15)$$

Equation (15) indicates that the average input current follows the input voltage when $(t_1–t_0)$ and the switching cycle $T_s$ are constant in a half-line cycle.

*3) Time Interval $[t_1–t_2]$:* As $Q_1$ is turned OFF at time $t_1$, the magnetic current commutes from the primary-side winding to the secondary-side winding. The MOSFET $Q_2$ is still OFF so that the magnetic current flows in diode $D_2$. The energy stored in the transformer is transferred to the capacitor $C_{\text{sto}}$. The voltage across the winding $N_{\text{sec}}$ is clamped at $V_{\text{sto}}$ and reflected to the primary side. The voltage across the drain to source of $Q_1$ can be expressed as

$$V_{Q_1(P_{\text{in}} > P_{\text{LED}})}[t_1 - t_2] = V_{\text{in}} + V_{\text{sto}} \times \frac{N_{\text{pri}}}{N_{\text{sec}}}. \quad (16)$$

When $D_2$ is conducting, the voltage at the anode of diode $D_1$ is equal to $V_{\text{sto}}$ (ignoring the voltage drop of $D_2$). Since $V_{\text{sto}}$ is higher than $V_{\text{LED}}$, which is ensured by the design, the diode $D_1$ is, therefore, forward biased, while the body diode of $Q_2$ is reverse biased. The voltage across the drain to source of $Q_2$ can be expressed as

$$V_{Q_2(P_{\text{in}} > P_{\text{LED}})}[t_1 - t_2] = V_{\text{sto}} - V_{\text{LED}}. \quad (17)$$

This interval ends at $t_2$ when the MOSFET $Q_2$ is turned ON.

*4) Time Interval $[t_2–t_3]$:* The voltage on the secondary-side winding is clamped at $V_{\text{LED}}$ after $Q_2$ is ON. Since $V_{\text{LED}}$ is lower than $V_{\text{sto}}$, the diode $D_2$ becomes reverse biased and the switching current in $D_2$ is zero. The voltage across the diode $D_2$ can be expressed as

$$V_{D_2(P_{\text{in}} > P_{\text{LED}})}[t_2 - t_3] = V_{\text{sto}} - V_{\text{LED}}. \quad (18)$$

The voltage on the secondary-side winding is reflected to the primary-side winding and the voltage on $Q_1$ during this time
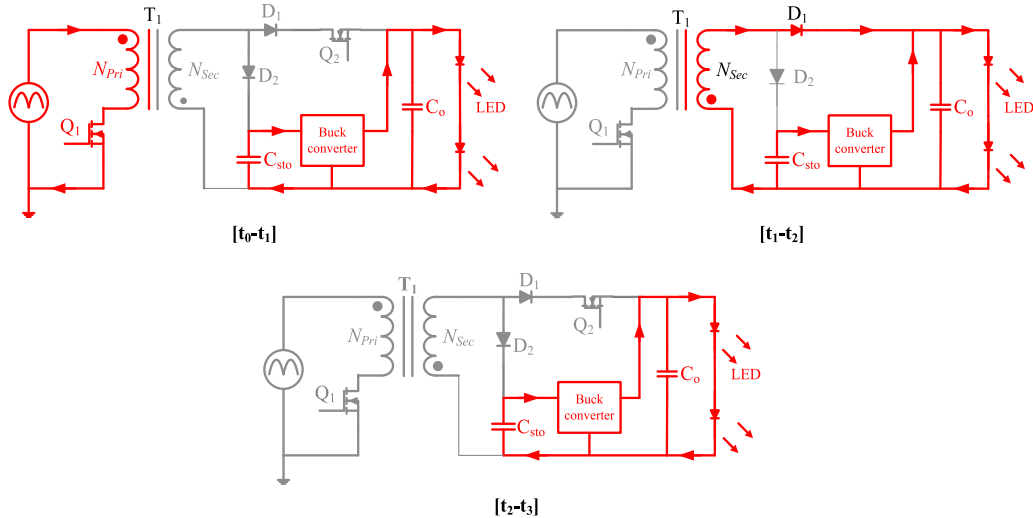
Fig. 11.    Switching operation of the proposed unidirectional current ripple compensation LED driver when $P_{\text{in}} < P_{\text{LED}}$.

interval can be expressed as

$$V_{Q_1(P_{\text{in}} > P_{\text{LED}})}[t_2 - t_3] = V_{\text{in}} + V_{\text{LED}} \times \frac{N_{\text{pri}}}{N_{\text{sec}}}. \qquad (19)$$

Equations (16) and (19) express the voltage stress on $Q_1$ during the time interval $[t_1 - t_2]$ and $[t_2 - t_3]$, respectively. Since $V_{\text{sto}}$ is higher than $V_{\text{LED}}$, $Q_1$ has higher voltage stress during the time interval $[t_1 - t_2]$.

During $[t_2 - t_3]$, the switching current in winding $N_{\text{sec}}$ continues its flow in $D_1$ and $Q_2$ and the flyback transformer releases its remaining energy to the LED load. The switching current in winding $N_{\text{sec}}$ drops to zero at time $t_3$, which ends this time interval.

*5) Time Interval $[t_3 - t_4]$:* To achieve the DCM operation, there is a small-time interval $[t_3 - t_4]$ when there is no active switching operation. The switching cycle ends at $t_4$.

One can also apply leading edge modulation to $Q_2$ to achieve the same function. Fig. 9 shows the operation when with applying trailing edge modulation to $Q_2$. $Q_2$ is turned ON before $Q_1$ is turned OFF. The secondary-side current flows in $D_1$ and $Q_2$ when $Q_1$ is turned OFF. After $Q_2$ is turned OFF, the remaining current is directed to flow in $D_2$. Fig. 10 shows the critical switching waveforms when applying trailing edge modulation to $Q_2$. The current stresses for $D_1, Q_2, D_2$ are different under two modulation schemes. When leading edge modulation is applied to $Q_2$, the peak secondary-side current goes through the diode $D_2$. By contrast, when trailing edge modulation is applied to $Q_2$, the peak secondary-side current goes through the diode $D_1$ and $Q_2$. Under trailing edge modulation, there is no turn ON loss with $Q_2$ since the body diode of $Q_2$ is forward biased when $Q_2$ is turned ON. Switching loss occurs during turn OFF of $Q_2$ when the current in $Q_2$ is not zero. Under leading edge modulation, there is no turn OFF loss with $Q_2$ since the current is already zero when $Q_2$ is turned OFF. The switching loss occurs during turn ON of $Q_2$ when the switching current is not zero.

*6) When $P_{in} < P_{LED}$:* Fig. 11 shows the switching operation during each time interval when $P_{\text{in}} < P_{\text{LED}}$, and Fig. 12 shows the key switching waveforms. One switching cycle is further divided into three time intervals $[t_0 - t_1]$, $[t_1 - t_2]$, and $[t_2 - t_3]$. The
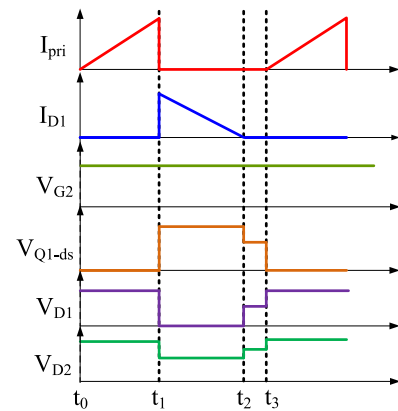


Fig. 12.    Key switching waveforms of the proposed unidirectional current ripple compensation LED driver when $P_{\text{in}} < P_{\text{LED}}$.

MOSFET $Q_2$ is always ON so that $P_{\text{in}} = P_1$. The buck converter is activated, and energy is transferred from $C_{\text{sto}}$ back to the LED load. Since $P_{\text{in}} < P_{\text{LED}}$, the control loop will automatically generate a 100% duty cycle for $Q_2$. Therefore, the switching operation during $P_{\text{in}} < P_{\text{LED}}$ can be understood as a special case of the switching operation under $P_{\text{in}} > P_{\text{LED}}$ and will not be repeated.

*7) Switching Operation Over a Half-Line Cycle:* As the switching operation during $P_{\text{in}} < P_{\text{LED}}$ and $P_{\text{in}} > P_{\text{LED}}$ had been discussed, the switching operation under the scale of a half-line cycle is illustrated in Fig. 13.

## IV. CONTROL SCHEME

Fig. 14 shows the control scheme of the proposed unidirectional current ripple compensation LED driver. There are two current regulation loops and one voltage regulation loop in the system to regulate the LED current and the voltage of the storage capacitor $V_{\text{sto}}$. Although the goal is to buffer the imbalanced energy in every switching cycle, the control is achieved by sensing and regulating currents and voltages.
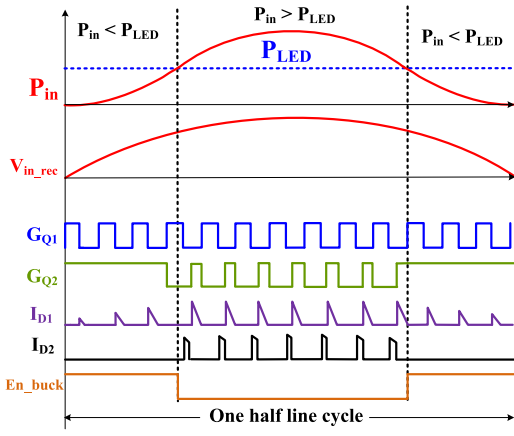
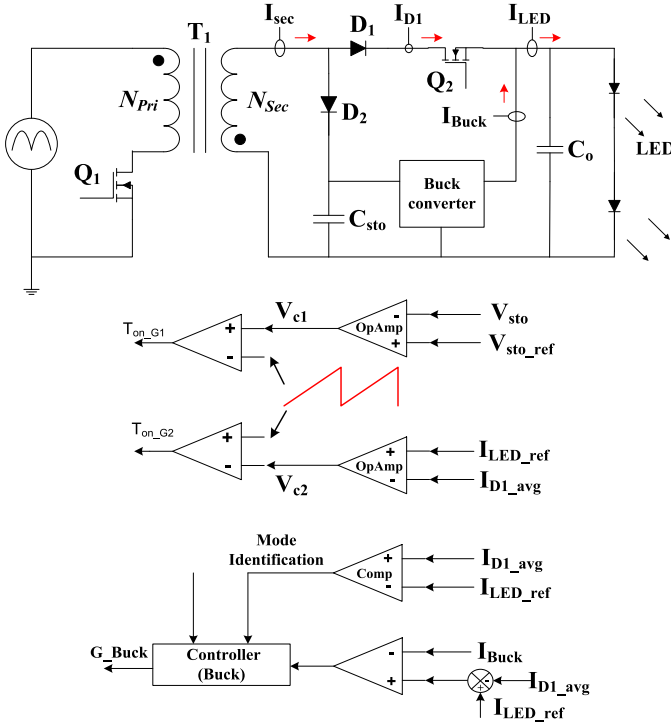Fig. 13. Switching operation over a half-line cycle.



Fig. 14. Control scheme of the proposed unidirectional current ripple compensation LED driver.

TABLE I
EXPRESSION OF THE VOLTAGE STRESS OF EACH COMPONENT

| | |
|---|---|
| $Q_1$ | $V_{in}(t) + V_{sto}(t) \times \dfrac{N_{pri}}{N_{sec}}$ |
| $D_1$ | $V_{in\_pk} \times \dfrac{N_{sec}}{N_{pri}} + V_{LED}$ |
| $D_2$ | $V_{sto}(t) + V_{in}(t) \times \dfrac{N_{sec}}{N_{pri}}$ |
| $Q_2$ | $V_{sto} - V_{LED}$ |

The current in diode $D_1$ is sensed and averaged in every switching cycle. The averaged current in $D_1$, $I_{D1\_avg}$, is then compared with the LED current reference $I_{LED\_ref}$. If $I_{D1\_avg}$ is larger than $I_{LED\_ref}$, the compensated error voltage $V_{c2}$ will be reduced. A reduced $V_{c2}$ will generate a smaller duty cycle for $Q_2$, which will reduce $I_{D1\_avg}$. When $P_{in} > P_{LED}$, the duty cycle of $Q_2$ will be controlled to achieve $I_{D1\_avg} = I_{LED\_ref}$. When $P_{in} < P_{LED}$, because $I_{D1\_avg}$ is always less than $I_{LED\_ref}$, the feedback loop will turn $Q_2$ ON. When it is detected that the duty cycle of $Q_2$ is 100%, the buck converter will be activated. The difference between $I_{LED\_ref}$ and $I_{D1\_avg}$, $I_{LED\_ref} - I_{D1\_avg}$, becomes the output current reference of the buck converter. The current feedback loop of the buck converter ensures that the current generated by the buck converter is equal to its reference.

Therefore, the current delivered to the LED load under both $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$ can be precisely controlled.

The average voltage of $V_{sto}$ is controlled as well to serve two purposes. First, net-zero energy storage with $C_{sto}$ can be achieved by controlling the average voltage of $V_{sto}$. In a half-line cycle, it is expected that the net energy stored in $C_{sto}$ is zero. In this way, the averaged input power is equal to the LED output power. To achieve this, $V_{sto\_avg}$ is compared with the reference voltage $V_{sto\_ref}$. The compensated error $V_{c1}$ determines the ON time of $Q_1$, which controls the input power. Whenever $V_{sto\_avg}$ is not equal to $V_{sto\_ref}$, $V_{c1}$ will be changed by the feedback loop to change the input power. As a chain reaction, $V_{sto\_avg}$ will be adjusted to follow $V_{sto\_ref}$ again. For example, if the net stored energy with $C_{sto}$ is above zero, $V_{sto\_avg}$ will start growing and eventually become higher than $V_{sto\_ref}$. Once this happens, the compensated error signal $V_{c1}$ will be decreased. A decreased $V_{c1}$ would generate a smaller ON time for $Q_1$, which reduces the input power. As the output power remains unchanged, a reduction in the input power will reduce the net energy stored in $C_{sto}$. The feedback loop will continue exert this effect and the net energy storage in $C_{sto}$ will eventually become negative in a half-line cycle. Then, $V_{sto}$ will start decreasing and eventually be brought down to $V_{sto\_avg}$. It is noted that with constant ON time in a half-line cycle, together with the DCM operation, the PFC is achieved automatically, which is also indicated by (15). In addition, $V_{sto}$ should be controlled to maintain a proper operation. Since there is a significant double-line-frequency ripple voltage on $V_{sto}$, one needs to make sure that $V_{sto\_min}$ is always higher than $V_{LED}$. The reference voltage for $V_{sto\_avg}$ should be designed high enough to maintain this condition, which is achieved by the $V_{sto\_avg}$ voltage control loop, as shown in Fig. 14 as well.

## V. DESIGN ANALYSIS

In this section, the design parameters are analyzed to provide a design guideline. The component voltage and current stresses, the design of $V_{sto\_avg}$, and the selection of $C_{sto}$ as well as the selection of the switching frequency for the proposed LED driver are discussed.

### A. Component Voltage Stress

The voltage stress for each component, as described in Section II, is summarized in Table I. The voltage stresses of
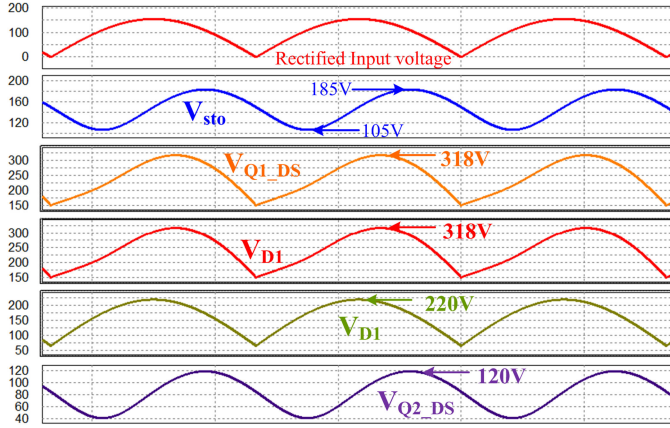
Fig. 15.   Plot of component voltage stresses with the proposed LED driver over a half-line cycle (the simulation is based on the following parameter: $V_{\text{in}} = 110$ Vrms, $V_{\text{LED}} = 65$ V, $P_{\text{LED}} = 28$ W, $V_{\text{sto\_min}} = 105$ V, $V_{\text{sto\_max}} = 185$ V, and $N_{\text{pri}} : N_{\text{sec}} = 1:1$).

the components are determined by the input voltage, the voltage of the storage capacitor voltage $V_{\text{sto}}$, and the LED output voltage. Under 110 Vrms input voltage, 65 V LED output voltage, $N_{\text{pri}} : N_{\text{sec}} = 1:1$, and the storage capacitor voltage $V_{\text{sto}}$ swinging from 105 to 185 V, the maximum voltage of $Q_1, D_1, D_2$, and $Q_2$ is 318, 318, 220, and 120 V, respectively, as plotted in Fig. 15.

### B.  Component Current Stress

In every switching cycle, at time $t_1$, the energy stored in the flyback transformer $E_{\text{Tran\_}t1}$ can be expressed as

$$E_{\text{Tran\_}t1}(t') = \frac{1}{2}L_{\text{pri}} \times I^2_{\text{pri\_}t_1}(t') \qquad (20)$$

where in (20), $L_{\text{pri}}$ represents the inductance of the primary-side winding, $T_s$ represents the switching period, and $I_{\text{pri\_}t1}(t)$ represents the primary-side switching current at time $t_1$ in a switching cycle. The symbol "$(t')$" indicates that $I_{\text{pri\_}t1}$ is a time-varying parameter at a line cycle scale. Therefore, the instantaneous input power can be expressed as

$$P_{\text{in}}(t') = \frac{E_{\text{Tran\_}t_1}}{T_s} = \frac{L_{\text{pri}} \times I^2_{\text{pri\_}t_1}(t')}{2 \times T_s}. \qquad (21)$$

In (21), $T_s$ represents one switching period. Rearranging (21) yields

$$I_{\text{pri\_}t_1}(t') = \sqrt{\frac{P_{\text{in}} \times 2 \times T_s}{L_{\text{pri}}}}. \qquad (22)$$

The switching current in the secondary-side winding at time $t_1$ can be expressed as

$$I_{\text{sec\_}t_1}(t') = \frac{N_{\text{pri}}}{N_{\text{sec}}} \times \sqrt{\frac{P_{\text{in}} \times 2 \times T_s}{L_{\text{pri}}}}. \qquad (23)$$

Replacing $P_{\text{in}}$ with $P_{\text{in\_max}}$ in (22) and (23), the maximum switching current in the primary-side winding and the secondary-side winding, in a half-line cycle, can be calculated

as

$$I_{\text{pri\_max}} = I_{Q_1\_\text{max}} = \sqrt{\frac{4P_{\text{LED}} \times T_s}{L_{\text{pri}}}} \qquad (24)$$

$$I_{\text{sec\_max}} = I_{D_2\_\text{max}} = \frac{N_{\text{pri}}}{N_{\text{sec}}} \times I_{\text{pri\_max}} = \sqrt{\frac{4P_{\text{LED}} \times T_s}{L_{\text{sec}}}}. \qquad (25)$$

With the design specification presented in Table IV, the maximum switching current in $Q_1$ and $D_2$ is calculated to be 2.36 A. When $P_{\text{in}} > P_{\text{LED}}$, the magnetic current starts conducting in $D_1$ at time $t_2$. The energy stored in the transformer at time $t_2, E_{\text{Tran\_}t2}$, can be expressed as

$$E_{\text{Tran\_}t2(P_{\text{in}} > P_{\text{LED}})} = \frac{1}{2}L_{\text{sec}} \times I^2_{D_1\_t2(P_{\text{in}} > P_{\text{LED}})}. \qquad (26)$$

As the remaining energy in the transformer will be transferred to the LED load; therefore,

$$\frac{E_{L\_\text{sec\_}t2(P_{\text{in}} > P_{\text{LED}})}}{T_s} = P_{\text{LED}}. \qquad (27)$$

Combining (26) and (27) yields

$$I_{D_1\_t2}(P_{\text{in}} > P_{\text{LED}}) = \sqrt{\frac{2P_{\text{LED}} \times T_s}{L_{\text{sec}}}}. \qquad (28)$$

It can be understood that, when $P_{\text{in}} > P_{\text{LED}}$, the switching current in $D_1$ at $t_2$ is the maximum current of $D_1$. Therefore,

$$I_{D_1\_\text{max}} = I_{Q_2\_\text{max}} = \sqrt{\frac{2P_{\text{LED}} \times T_s}{L_{\text{sec}}}}. \qquad (29)$$

$I_{D1\_max}$ is calculated to be 1.67 A with the specification and parameters in Table IV.

### C.  Storage Capacitor $C_{\text{sto}}$ Selection

The average voltage of $V_{\text{sto}}, V_{\text{sto\_avg}}$, is closely related to the selection of $C_{\text{sto}}$. Combining (4) and (5), the relationship between $C_{\text{sto}}$ and the voltage $V_{\text{sto\_avg}}$ can be expressed as

$$C_{\text{sto}} = \frac{P_{\text{LED}} \times T_{\text{line}}}{2\pi \times V_{\text{sto\_avg}} \times (\Delta V_{\text{sto}})}. \qquad (30)$$

At the same time, there is another constraint that needs to be maintained at all time

$$V_{\text{sto\_min}} = V_{\text{sto\_avg}} - \frac{\Delta V_{\text{sto}}}{2} > V_{\text{LED}}. \qquad (31)$$

For example, if $V_{\text{sto\_avg}}$ is selected to be 150 V and the LED voltage is 60 V, the peak-to-peak ripple voltage of $V_{\text{sto}}, \Delta V_{\text{sto}}$, should be limited to be less than 180 V. In this way, $V_{\text{sto\_min}}$ is always higher than 60 V. Among $V_{\text{sto\_avg}}, \Delta V_{\text{sto}}$, and $C_{\text{sto}}$, one can first determine values for two parameters, based on the design, and then calculate the third one. $V_{\text{sto\_avg}}$ can be regulated by the control loop as discussed in Section V. Once the allowable $V_{\text{sto}}$ is determined, the capacitor $C_{\text{sto}}$ can be calculated by (30).

As shown in Table I, the voltage stresses of $Q_1, D_2, Q_2$ are related to $V_{\text{sto}}$. A higher voltage of $V_{\text{sto}}$ will result in higher voltage stresses on these components. The maximum voltage stress allowed on these components will, therefore, affect the selection of $C_{\text{sto}}$.

### D. Achieving DCM Operation

Flyback PFC is operated under DCM constant ON time (for $Q_1$) to achieve a high PFC. It can be well understood, when $P_{in} = 2P_{LED}$, the time span $(t_3 - t_0)$ will be stretched to the maximum. Therefore, to achieve DCM operation, one needs to make sure $T_s$ is larger than $(t_3 - t_1)$ when $P_{in} = 2P_{LED}$ with the given circuit parameters. When the input voltage reaches its maximum in a half-line cycle, the primary-side switching current also reaches the maximum. The relationship between them can be expressed as

$$I_{\text{pri\_max}} = \frac{V_{\text{in\_max}} \times (t_1 - t_0)}{L_{\text{pri}}}. \tag{32}$$

Combining (29) and (34) yields

$$(t_1 - t_0) = \frac{\sqrt{4 \times T_s \times P_{\text{LED}} \times L_{\text{pri}}}}{V_{\text{in\_max}}}. \tag{33}$$

When $P_{in} = P_{LED}$, the relationship between the peak switching current in $D_1$ and the timespan $(t_2 - t_3)$ can be expressed as

$$I_{D_1\text{\_max}} = \frac{V_{\text{LED}} \times (t_3 - t_2)}{L_{\text{sec}}}. \tag{34}$$

Combining (29) and (34) yields

$$(t_3 - t_2) = \frac{\sqrt{2 \times T_s \times P_{\text{LED}} \times L_{\text{sec}}}}{V_{\text{LED}}}. \tag{35}$$

The secondary-side winding releases energy to the capacitor $C_{\text{sto}}$ during the time interval $[t_1 - t_2]$. The current change on the secondary-side winding during $[t_1 - t_2]$, the voltage $V_{\text{sto}}$, and the secondary-side inductance $L_{\text{sec}}$ have the following relationship:

$$\frac{V_{\text{sto}} \times (t_2 - t_1)_{\text{max}}}{L_{\text{sec}}} = I_{\text{sec\_max}} - I_{D1\text{\_max}}. \tag{36}$$

Combining (25) and (36) yields

$$(t_2 - t_1)_{\text{max}} = \frac{\left( \sqrt{\frac{4 \times T_s \times P_{\text{LED}}}{L_{\text{pri}}}} - \sqrt{\frac{2 \times T_s \times P_{\text{LED}}}{L_{\text{sec}}}} \right) \times L_{\text{sec}}}{V_{\text{sto}}}. \tag{37}$$

The above-mentioned derivation assumes that the DCM operation has already been achieved and needs to be verified. In other words, one needs to ensure that the sum of $[t_0 - t_1]$, $[t_1 - t_2]$, and $[t_2 - t_3]$ is less than the predefined switching period. As an example, one can define $T_s$ to be 20 $\mu$s. With the circuit parameters in Table IV, $(t_1 - t_0)$ and $(t_3 - t_2)$ are calculated to be 6.1 and 10.3 $\mu$s, respectively. When $P_{in} = 2P_{LED}$, $V_{\text{sto}}$ is at the vicinity of the averaged value 150 V. Using $V_{\text{sto}} = 150$ V in (37), $(t_2 - t_1)$ is calculated to be 1.85 $\mu$s. Therefore, $(t_3 - t_0)$ is equal to 18.2 $\mu$s and is less than the predefined 20 $\mu$s switching period. If, somehow, the initial assumption of the DCM operation is not met, one can reselect the switching period. On the other side, if one aims to operate at a specific switching period (or frequency) for better electromagnetic interference signature or efficiency, the circuit parameters, such as $L_{\text{pri}}, V_{\text{in\_max}}, L_{\text{sec}}$, can be reselected to change the time $(t_1 - t_0), (t_2 - t_1), (t_3 - t_2)$, as indicated by (33), (35), and (37).

At the same time, it is not desirable to make $T_s$ much larger than $(t_3 - t_0)$. Equations (24), (25), and (29) indicate that lower current stresses can be achieved with $Q_1, D_1, Q_2$, and $D_2$ when $T_s$ is smaller. Therefore, $T_s$ should be selected to be the smallest value that achieves the DCM, with some acceptable margin.

### E. Loss Breakdown

One major advantage of the proposed LED driver is a reduction of the power conversion loss. In this section, a breakdown of the proposed unidirectional energy buffering LED driver as well as the previous active filtering LED driver is presented. The MOSFET $Q_2$ is under leading edge modulation in this analysis.

The loss breakdown of the proposed unidirectional energy buffering LED driver and the previous active filter LED driver is presented in Tables II and III. The parameters used for loss calculations are derived or obtained from the datasheets, as presented in the Appendix. One should note that the design of the buck converters is identified in two designs. Therefore, analyzing the detail loss from each component inside the buck converter is not necessary. The efficiency of the buck converter and boost converter is estimated in Tables II and III.

When looking into both designs from the primary side, the operation of the flyback PFC is the same. Therefore, the conduction and switching losses with $Q_1$ are the same in both designs. The leakage inductance loss and the transformer loss are also the same in both designs.

The loss generated by the operation of $Q_2$ is presented in Table II. Because the voltage stress on $Q_2$ is much lower than the voltage stress on $Q_1$, very low ON-resistance MOSFET can be found to implement $Q_2$. A 16 m$\Omega$ ON-resistance MOSFET is used, and the conduction loss of $Q_2$ is only 1.7 mW. When the cost is a concern, a MOSFET with a higher ON-resistance can also be used to implement $Q_2$, which will generate more conduction loss. However, it should not have too much impact on the overall loss.

When $P_{in} < P_{LED}$, the duty cycle of $Q_2$ is controlled to be 100%. Therefore, the turn-ON overlap loss with $Q_2$ only occurs when $P_{in} > P_{LED}$. Under this condition, the average drain-to-source voltage of $Q_2$ is only 30 V before $Q_2$ is turned ON, the calculated turn-ON overlap loss is only 20 mW and only 0.4% of the total loss. Also, the output capacitor switching loss with $Q_2$ only occurs when $P_{in} > P_{LED}$ and is calculated to be 6.9 mW. Overall, the losses generated by the operation of $Q_2$ are equal to 1.7 mW + 20 mW + 6.9 mW = 28.6 mW, which is only 0.1% of the output power and can be ignored in the design.

Because $V_{\text{sto}}$ is much higher than $V_{\text{LED}}$, the sum of current $I_{D1\text{\_avg}}$ and $I_{D2\text{\_avg}}$ in the proposed unidirectional energy buffering LED driver is smaller than the average current $I_{D1\text{\_avg}}$ in the previous active filtering LED driver. Consequently, the total conduction loss with $D_1$ and $D_2$ in the proposed LED driver is smaller than the conduction loss with $D_1$ in the previous active filter LED driver. It should note that the total loss generated by the proposed LED driver, without the buck converter operation, is 3.94 W, which already includes the loss generated when transferring the energy from the ac input to the LED load and the storage capacitor. This number is almost equal to, even slightly smaller than, the loss generated by the flyback PFC in the previous active filtering LED driver. Therefore, the process of storing the extra energy in the proposed LED driver can be claimed only go through one power conversion

TABLE II
LOSS BREAKDOWN OF THE PROPOSED UNIDIRECTIONAL ENERGY BUFFERING LED DRIVER

| Sources of loss | Expression for loss | Loss (W) | Percentage |
|---|---|---|---|
| Q1 conduction loss | $P_{Q1\_cond} = I^2_{Q1\_rms} \times R_{Q1\_on}$ | 0.15 | 3.2% |
| Q1 output capacitor loss | $P_{Q1\_cap} = C_{Q_1\_oss} \times V^2_{Q1\_ds} \times F_{sw}$ | 0.02 | 1.7% |
| Q1 turn off overlap loss | $P_{Q1\_off} \approx (V_{Q_1\_ds} \times I_{Q_1\_pk\_rms} \times T_{f\_Q_1} \times F_{sw})/2$ | 0.15 | 4.4% |
| D1 conduction loss | $P_{D_1\_cond} = I_{D_1\_avg} \times V_{D_1\_F}$ | 0.46 | 11.0% |
| Q2 conduction loss | $P_{Q_2\_cond} = I^2_{Q_2\_rms} \times R_{Q_2\_on}$ | 0.0017 | 0.0% |
| Q2 output capacitor loss | $P_{Q1\_cap} = (C_{Q_2\_oss} \times V^2_{Q2\_ds} \times F_{sw})/4$ | 0.014 | 0.3% |
| D2 conduction loss | $P_{D_1\_cond} = I_{D_2\_avg} \times V_{D_2\_F}$ | 0.14 | 3.3% |
| Q2 turn on overlap loss | $P_{Q2\_on} \approx (V_{Q_2\_ds} \times I_{Q_2\_pk} \times T_{r\_30} \times F_{sw})/4$ | 0.02 | 0.4% |
| Input bridge diode conduction loss | $P_{bridge\_cond} = I_{in\_avg} \times V_{DB\_F} \times 2$ | 0.48 | 11.4% |
| Leakage inductance loss | $P_{lk} = \dfrac{1}{2} \times I^2_{Q_1\_pk\_rms} \times L_{lk}$ | 1.39 | 33.2% |
| Transformer core and copper loss | $P_{transformer} = P_{LED} \times K_{tran\_loss}$ | 1.12 | 26.7% |
| Total loss without the Buck converter | | 3.94W | 93.4% |
| Buck converter loss | $P_{Buck\_loss} = (P_{LED}/\pi)(\dfrac{1}{\eta_{buck}} - 1)$ | 0.28 | 6.6% |
| Total loss of the proposed LED driver | | 4.21W | 100% |

TABLE III
LOSS BREAKDOWN OF THE PREVIOUS ACTIVE FILTER LED DRIVER

| Sources of loss | Expression for loss | Loss (W) | Percentage |
|---|---|---|---|
| Q1 conduction loss | $P_{Q1\_cond} = I^2_{Q1\_rms} \times R_{Q1\_on}$ | 0.15 | 3.2% |
| Q1 capacitor loss | $P_{Q1\_cap} = C_{oss} \times V^2_{Q1\_ds} \times f_{pwm}$ | 0.04 | 0.8% |
| Q1 turn off loss | $P_{Q1\_off} = (V_{Q_1\_ds\_rms} \times I_{pk\_rms} \times T_f \times f_{PWM})/2$ | 0.23 | 4.9% |
| D1 conduction loss | $P_{D_1\_cond} = I_{D_1\_avg} \times V_{D_1\_F}$ | 0.68 | 14.5% |
| Input bridge diode conduction loss | $P_{bridge\_cond} = I_{in\_avg} \times V_{DB\_F} \times 2$ | 0.48 | 10.3% |
| leakage inductance loss | $P_{lk} = \dfrac{1}{2} \times I^2_{Q_1\_pk\_rms} \times L_{lk}$ | 1.39 | 30.1% |
| transformer core and copper loss | $P_{transformer} = P_{LED} \times K_{tran\_loss}$ | 1.12 | 24.1% |
| Total loss of Flyback PFC | | 4.08 | 88% |
| Loss from Boost converter | $P_{Buck\_loss} = (P_{LED}/\pi)(\dfrac{1}{\eta_{buck}})(\dfrac{1}{\eta_{boost}} - 1)$ | 0.28 | 6.0% |
| Loss from Buck converter | $P_{Buck\_loss} = (P_{LED}/\pi)(\dfrac{1}{\eta_{buck}} - 1)$ | 0.28 | 6.0% |
| Total loss of previous active filter LED driver | | 4.64 | 100% |

step. Compared to the previous active filter LED driver, the loss generated by transferring the extra energy from the LED load side to the storage capacitor, by the boost converter, is eliminated in the proposed unidirectional energy buffering LED driver, which will help achieve a higher efficiency.

Fig. 16 shows the loss breakdown of the proposed LED driver with a bar chart.

*F. Efficiency*

As discussed in the above-mentioned section, the imbalanced energy only goes through one power conversion step when transferring it from the ac input to the storage capacitor. Therefore, in total, the imbalanced energy experiences two power conversion steps, which is one time less than the previous active filtering and three-port LED drivers. The amount of imbalanced
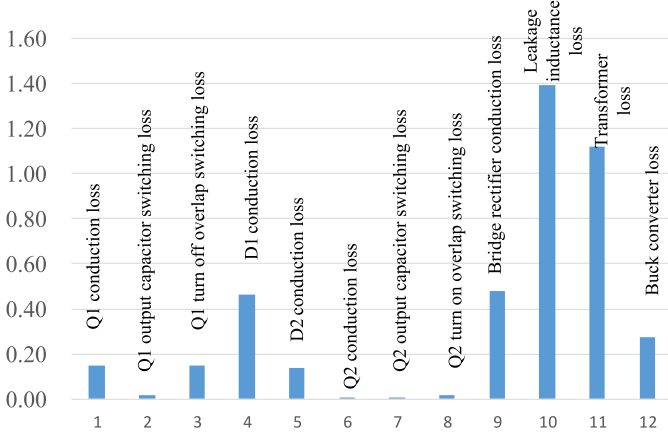
Fig. 16. Loss breakdown of the proposed LED driver.

TABLE IV
EXPERIMENTAL PROTOTYPE SPECIFICATION AND KEY COMPONENTS

| System Specification | |
| --- | --- |
| Input voltage | 89 Vrms – 132 Vrms |
| Maximum output voltage | ~65 V |
| Maximum output current | 0.43 A |
| Maximum output power | 28 W |
| **Circuit Parameter** | |
| Transformer | $N_{pri}$: $N_{sec}$: = 1:1 $L_{pri}$=400 µH, EE16 core |
| Switching frequency | 50 kHz |
| Input Bridge rectifier | GBU606 |
| PFC Controller | PIC16F1578-I/SS |
| MOSFET Q1 | STB13N80k5 (800 V, 12 A) |
| MOSFET Q2 | FDP2532 (150 V, 8 A@Ta=25 C°) |
| Diode D1 | STPSC6H065D1 (650 V, 6 A) |
| Diode D2 | LQA06T300 (400 V, 6 A) |
| Output capacitor | CGA9N3X7S2A106K230KB, 100 V, 10 µF |
| Storage capacitor | 2 x ECW-FD2W335 K 450 V, 3.3 µF |
| High and low sides MOSFET (Buck) | IRF730PBF (400 V 5.5 A) |
| Controller (Buck) | NCP159DR2G |
| Output inductor | DELEVAN-224 (220 µH, 2.0 A) |
| Output capacitor | CGA9N3X7S2A106K230KB, 100 V, 10 µF |

energy can be expressed as

$$P_{\mathrm{imb}} = \frac{\int_{\frac{\pi}{8}}^{\frac{3\pi}{8}} P_{\mathrm{in}}(t)dt}{T_s/2}$$

$$= \frac{\int_{\frac{\pi}{8}}^{\frac{3\pi}{8}} \frac{1}{2} P_{\mathrm{in\_pk}} \times [1 - \cos(4\pi \times f_{\mathrm{line}} \times t)]dt}{T_s/2}$$

$$= \frac{1}{2\pi} P_{\mathrm{in\_pk}} = \frac{1}{\pi} P_{\mathrm{LED}}. \qquad (38)$$

In (38), $P_{\mathrm{inb}}$ represents the amount of imbalanced power. Approximately, the total power losses can be partitioned as the losses generated by the operation of the flyback PFC and the losses generated by the buck converter. The loss generated by the operation of $Q_2$ can be ignored, as proved in the above-mentioned section. Therefore, the efficiency of the proposed LED driver can be expressed as

$$\eta_{\mathrm{LED\_drv}} \approx \frac{P_{\mathrm{LED}}}{\frac{P_{\mathrm{LED}} - P_{\mathrm{imb}}}{\eta_{PFC}} + \frac{P_{\mathrm{imb}}}{\eta_{PFC} \times \eta_{\mathrm{buck}}}}. \qquad (39)$$

To facilitate a comparison between the efficiency of the proposed LED driver and the efficiency of a conventional two-stage LED driver, (39)

$$\eta_{\mathrm{LED\_drv}} = \eta_{\mathrm{PFC}} \times \eta_{\mathrm{eqv}}. \qquad (40)$$

Combining (38), (39), and (40) yields

$$\eta_{\mathrm{eqv}} = \frac{1}{\frac{\left(1 - \frac{1}{\pi}\right)}{1} + \frac{\frac{1}{\pi}}{\eta_{\mathrm{buck}}}}. \qquad (41)$$

Using (41), $\eta_{\mathrm{eqv}}$ is calculated to be 99% when $\eta_{\mathrm{buck}}$ is 97% efficiency, as an example. When the flyback PFC achieves 86% efficiency, the theoretical efficiency of the proposed LED driver is calculated to be 85.1%, which is only 0.9% lower than a conventional single-stage LED driver. The reduction in efficiency is a small price to pay when flicker-free operation and electrolytic capacitor-free design are achieved. On the other side, the efficiency of a flyback PFC plus a buck converter (two stages) design should be much lower. All of the output power needs to be processed by the buck converter in the two-stage design. By comparison, only ~30% output power passes through

the buck converter in the proposed design. Therefore, the proposed design will achieve significant efficiency improvements over the existing two-stage driver. Assuming the buck converter in the two-stage design achieves the same 97% efficiency, the efficiency of the two-stage LED driver will be 86% × 97% = 83.4%, which is 1.7% lower than the proposed LED driver. Also, a conventional two-stage LED driver will still require the use of electrolytic capacitors. Therefore, the proposed LED driving method is an optimal solution to achieve both high efficiency and long lifespan.

## VI. EXPERIMENTAL VERIFICATION

A 28 W experimental prototype had been built and tested to verify the proposed unidirectional current ripple compensation LED driving method. Table IV shows the system specifications and circuit parameters of the experimental prototype.

Fig. 17(a) shows the key line cycle waveforms of the proposed LED driver. The power factor of the ac input was measured to be 0.98. The voltage on the buffer capacitor $V_{\mathrm{sto}}$ changes from a minimum of 70 V to a maximum of 120 V. The 120 Hz ripple LED current is measured to be 21.7 mA rms with fast Fourier transform function in the oscilloscope, which converts to 30.7 mA peak ripple current. Therefore, the 120 Hz ripple current is 7.1% of the average LED current. Fig. 17(b) shows the 120 Hz ripple current reaches 750 mA pk to pk when the current compensation is disabled. The proposed unidirectional current compensator demonstrated flicker-free LED driving performance without utilizing an electrolytic capacitor.

Fig. 18 shows the switching current from the main output, the switching current from the buck converter output, and the LED current. Fig. 19(a) and (b) shows the voltage waveforms of the key switching components currents with $Q_2$ under trailing
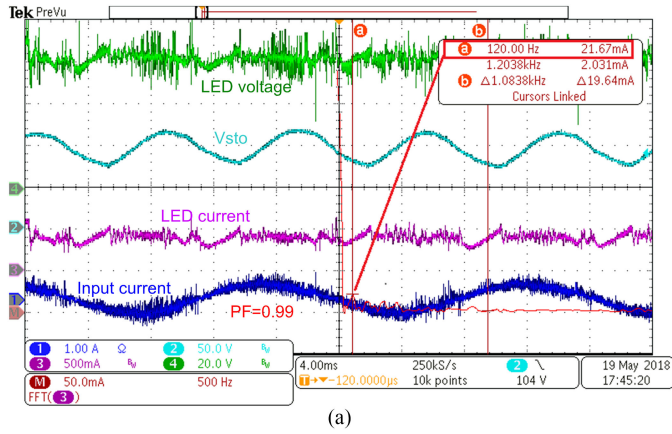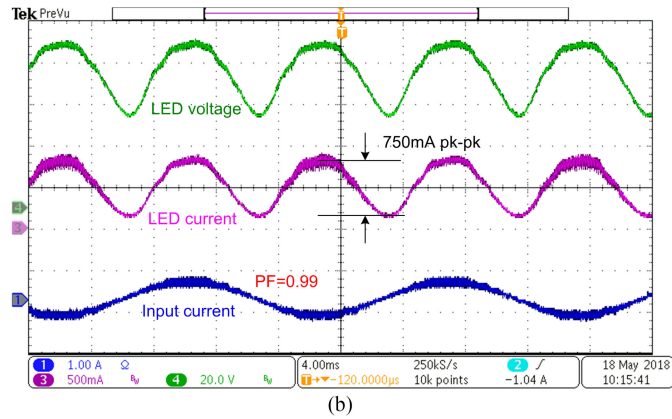
Fig. 17. Key line cycle waveforms of the proposed LED driver I. (a) Unidirectional current compensator is enabled. (b) Unidirectional current compensator is disabled.
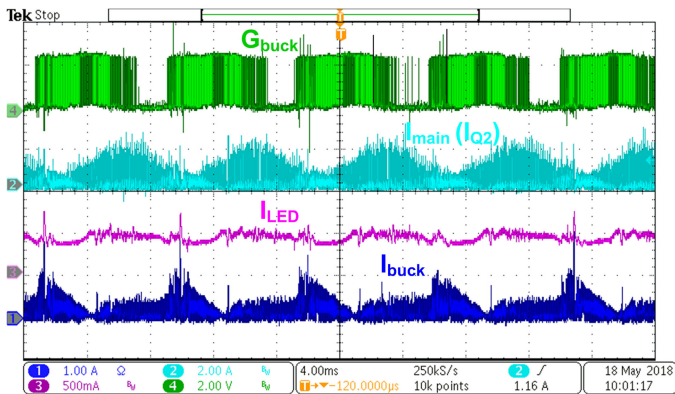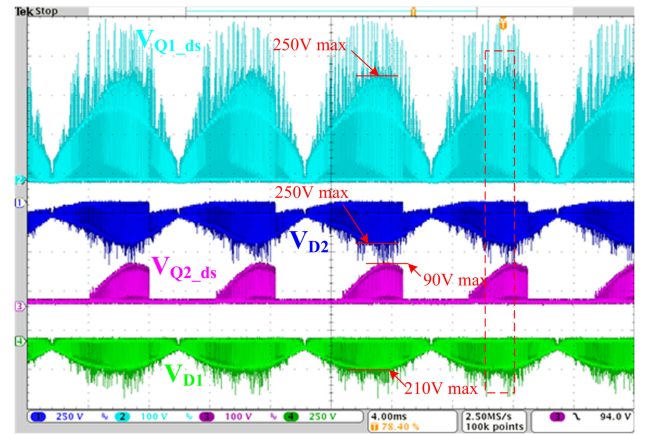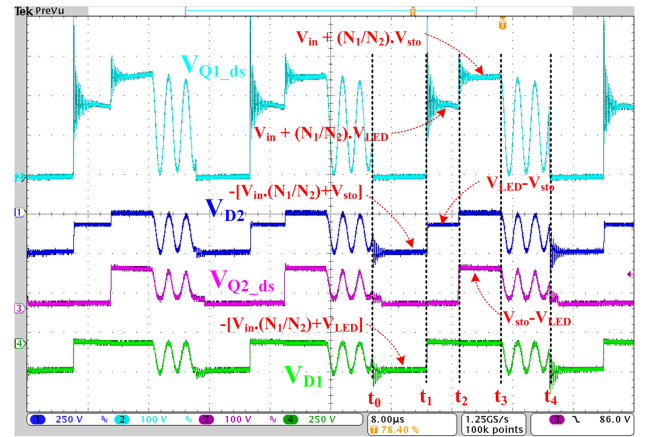


Fig. 18. Key line cycle waveforms of the proposed LED driver.



Fig. 19. Key component voltage waveforms with $Q_2$ under trailing edge modulation. (a) At the line cycle time scale. (b) Zoom-in of (a).

are zero. The diode $D_2$ is reverse biased and the voltage across $D_2$ is equal to $V_{sto}$ minus the LED voltage. $Q_2$ is turned OFF at $t_2$ and the secondary-side current flows in $D_2$. The voltage stress on $Q_1$ becomes the sum of input voltage plus $V_{sto}$ reflected to the primary side. The diode $D_1$ is forward biased so that the voltage stress is zero. The voltage stress on $Q_2$ is equal to $V_{sto}$ minus the LED voltage.

Fig. 20(a) and (b) shows the voltage waveforms of the key switching components with $Q_2$ under leading edge modulation. As expected, the maximum voltage stresses with MOSFETS $Q_1$, $Q_2$, and diodes $D_1$, $D_2$ are the same as they are in Fig. 19. The switching waveforms at the switching cycle time scale are shown in Fig. 20(b). The voltages across these components under each time interval are also annotated.

Fig. 21 shows the switching current waveforms of the key components with $Q_2$ under trailing edge modulation. The maximum current with $Q_1$ is 2.4 A. Under trailing edge modulation, the peak secondary-side current flows in $D_1$ and $Q_2$. Therefore, the peak current with $D_1$ and $Q_2$ is also 2.4 A. The peak current in $D_2$ is 1.6 A when the secondary-side switching current commutes from $D_1$ to $D_2$.

Fig. 22 shows the switching current waveforms of the key components with $Q_2$ under leading edge modulation. The max-

edge modulation. The maximum voltage stresses with MOSFETS $Q_1$, $Q_2$, and diodes $D_1$, $D_2$ are 250 V, 90 V, 210 V, and 250 V, respectively. Fig. 19(b) shows the zoomed-in waveform at a switching cycle time scale. $Q_1$ and $Q_2$ are ON during the time interval $[t_0-t_1]$. Therefore, the voltage stress on $Q_1$ and $Q_2$ is zero. During $[t_1-t_2]$, $Q_1$ is OFF and $Q_2$ remains ON. The voltage stress on $Q_1$ is equal to the input voltage plus the LED output reflected to the primary side. The voltage stresses for $D_1$ and $Q_2$
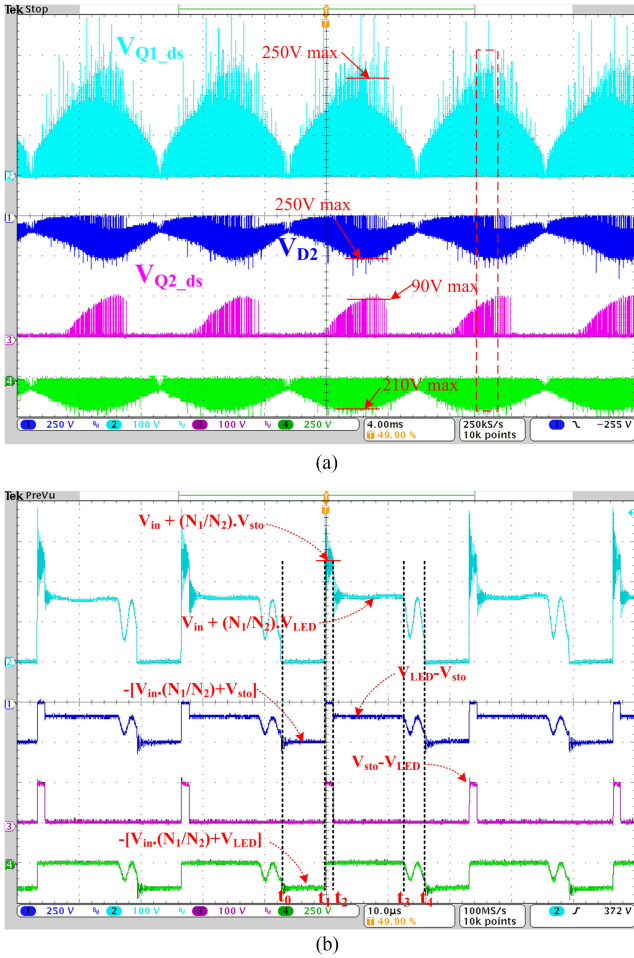
(a)



(b)

Fig. 20. Key component voltage waveforms with $Q_2$ under leading edge modulation. (a) At the line cycle time scale. (b) Zoom-in of (a).

imum current with $Q_1$ is also 2.4 A. Under leading edge modulation, the peak secondary-side current flows in $D_2$. Therefore, the peak current in $D_2$ is also 2.4 A. The peak current in $D_1$ (also $Q_2$) is 1.6 A when the secondary-side switching current commutes from $D_2$ to $D_1$.

The efficiency of the experimental prototype had been measured and compared with the efficiency of a conventional flyback LED driver. These two designs share the same PFC stage to make a fair comparison. Both prototypes achieve their highest efficiency at 350 mA LED load. The maximum efficiency of the proposed LED driver is around 1% lower than the maximum efficiency of the conventional single stage LED driver, as shown in Fig. 23.

Fig. 24 shows the power factor of the proposed LED driver, and Fig. 25 shows the measurement of input harmonic currents. Since the proposed LED driver applies the same PFC technology as a conventional design, a high PF is achieved. At full load, the experimental prototype achieved 0.99 PF, which meets the requirement from EnergyStar. All harmonic currents of interest are also below the limits from IEC-61000-3-2.

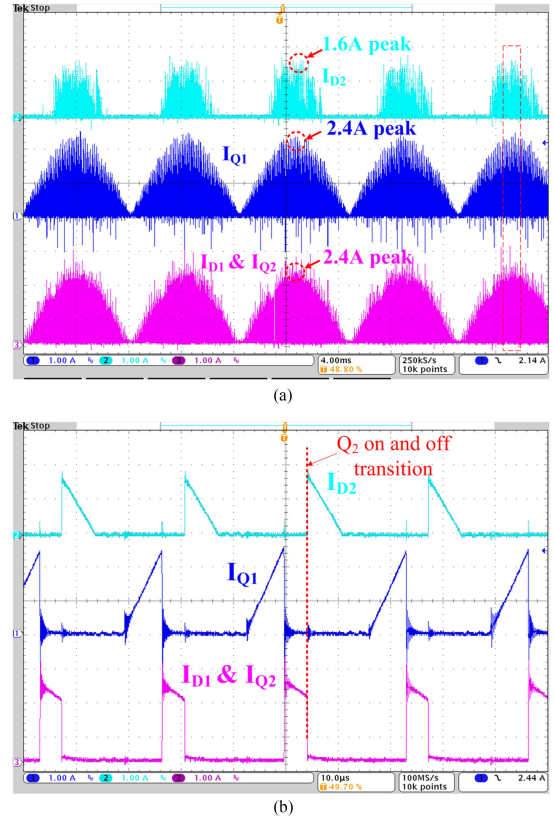The photograph of the experimental prototype is shown in Fig. 26.



(a)



(b)

Fig. 21. Key component current waveforms with $Q_2$ under trailing edge modulation. (a) At the line cycle time scale. (b) Zoom-in of (a).
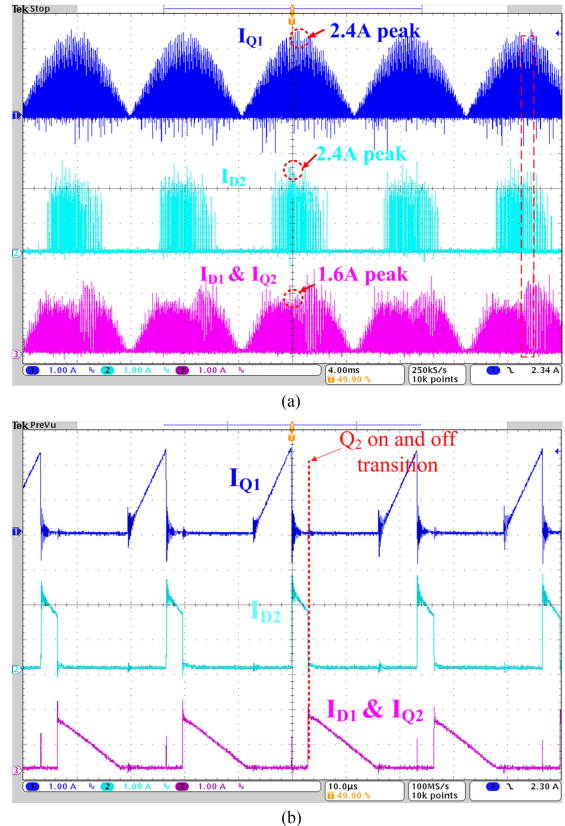


(a)



(b)

Fig. 22. Key components current waveforms with $Q_2$ under leading edge modulation. (a) At the line cycle time scale. (b) Zoom-in of (a).
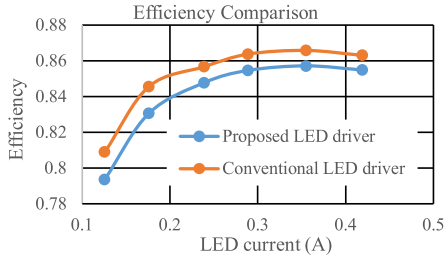
Fig. 23. Efficiency comparison between the proposed unidirectional current ripple compensator LED driver and a conventional LED driver.
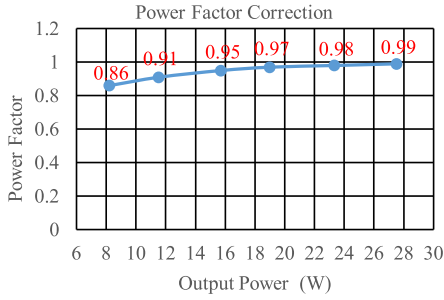


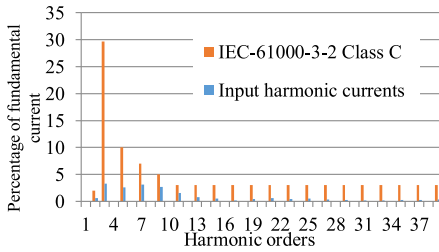Fig. 24. Power factor performance under 110 Vrms input.



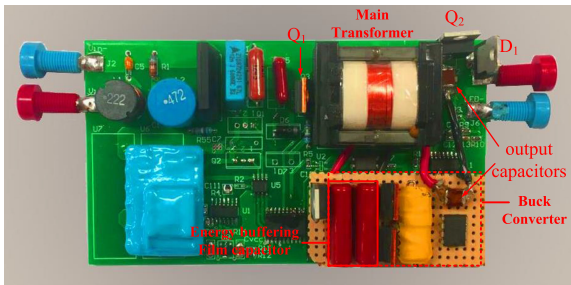Fig. 25. Input harmonic currents versus IEC-61000-3-2 limit under 110 Vrms input, full load.



Fig. 26. Photograph of the experimental prototype.

## VII. CONCLUSION

In this paper, a unidirectional current ripple compensation LED driver has been proposed to achieve electrolytic capacitor-less and flicker-free design. A flyback PFC is used to deliver the energy from the ac input to LED output while achieving a high PFC at the same time. By controlling the MOSFET $Q_2$, the flow of energy can be precisely controlled either delivering to LED output or storing in the energy storage capacitor, in every switching cycle. When $P_{in} > P_{LED}$, the imbalanced energy will be stored in the capacitor $C_{sto}$. When $P_{in} < P_{LED}$,

the reserved energy in $C_{sto}$ is delivered to the output through a buck converter. The advantage of this energy delivery structure is a reduction in the circulating energy compared with previous approaches. In previous active filter and three-port LED drivers, the imbalanced energy (approximately one-third of the total energy) goes through three power conversion steps, which results in a significant loss. In the proposed LED driver, the imbalanced energy experiences only two power conversion steps, resulting in improved efficiency compared with previous designs. A 28 W experimental prototype had been designed and tested. The 120 Hz ripple current is measured to be 11% of the dc LED current. With the optimized energy buffering structure, the efficiency of the proposed LED driver is only 0.9% lower than a conventional single-stage design, which is a significant improvement from the previous electrolytic capacitor-less design. The PF and harmonic currents of the proposed LED driver had also been verified in the experimental prototype, and measured results can meet the requirements both from Energy Star and IEC-61000-3-2. Overall, the measured results highly agree with the analysis and demonstrate a very promising LED driving technology.

## APPENDIX

TABLE V
PARAMETER VALUES USED IN THE ANALYSIS OF LOSS BREAKDOWN

| Description | Used in the proposed LED driver | Used in the previous active filter LED driver |
|---|---|---|
| RMS current of $Q_1$ | $I_{Q1\_rms}$ =0.57 A, | $I_{Q1\_rms}$ =0.57 A, |
| On resistance of $Q_1$ | $R_{Q1\_on}$=0.45 ohm, | $R_{Q1\_on}$=0.45 ohm, |
| Forward voltage drop of $D_1$ | $V_{D1\_F}$=1.57 V | $V_{D1\_F}$=1.57 V |
| Parasitic output capacitor of $Q_1$ | $C_{Q1\_oss}$=50 pF | $C_{Q1\_oss}$=50 pF |
| Drain to source voltage stress of $Q_1$ | $V_{Q1\_ds}$=$V_{in\_rms}$ =110 V | $V_{Q1\_ds}$=$V_{in\_rms}$ =110 V |
| Switching frequency of the PFC | $F_{sw}$=50 kHz | $F_{sw}$=50 kHz |
| RMS value of peak switching current in $Q_1$ | $I_{Q1\_pk\_rms}$= 1.67 A | $I_{Q1\_pk\_rms}$= 1.67 A |
| Average current in $D_1$ | $I_{D1\_avg}$=0.29 A | $I_{D1\_avg}$=0.43 A |
| Average input current in bridge rectifier | $I_{in\_avg}$=0.24 A | $I_{in\_avg}$=0.24 A |
| Forward voltage drop per diode in bridge rectifier | $V_{DB\_F}$=1 V | $V_{DB\_F}$=1 V |
| Turn off fall time of $Q_1$ | $T_{f\_Q1}$=16 ns | $T_{f\_Q1}$=16 ns |
| Efficiency of the Buck converter | $\eta_{buck}$=0.97% | $\eta_{buck}$=0.97% |
| Lump sum of primary side leakage inductance | $L_{lk}$=$L_{pri}$ x 5% = 20 μH | $L_{lk}$=$L_{pri}$ x 5% = 20 μH |
| Forward voltage drop of $D_2$ | $V_{D2\_F}$=1.57 V | |
| Parasitic output capacitor of $Q_2$ | $C_{Q1\_oss}$=650 pF | |
| Drain to source voltage stress of $Q_1$ | $V_{Q2\_ds}$=$V_{sto\_avg}$-$V_{LED}$=30 V | |
| Average current in $D_2$ | $I_{D2\_avg}$=0.09 A | |
| RMS current in $Q_2$ | $I_{Q2\_rms}$=0.33 A | |
| On resistance of $Q_2$ | $R_{Q2\_on}$=16 mohm | |
| Turn on rise time of $Q_2$ | $T_{r\_Q2}$=30 ns | |
| Peak switching current in $Q_2$ | $I_{Q2\_pk}$=1.67 A | |
| Loss coefficient of the Flyback transformer | $K_{tran\_loss}$ = 4% | |
| Efficiency of the Boost converter | | $\eta_{boost}$=0.97% |

## REFERENCES

[1] U.S Department of Energy, "LED lighting," Jul. 2017. [Online]. Available: https://energy.gov/energysaver/led-lighting

[2] "Global LED lighting market size & share worth $54.28 billion by 2022 Zion market research," Aug. 2017. [Online]. Available: https://globenewswire.com/news-release/2017/01/30/911985/0/en/Global-LED-Lighting-Market-will-reach-USD-54-28-Billion-by-2022-Zion-Market-Research.html

[3] B. Lehman and A. J. Wilkins, "Designing to mitigate effects of flicker in LED lighting: Reducing risks to health and safety," *IEEE Power Electron. Mag.*, vol. 1, no. 3, pp. 18–26, Sep. 2014.

[4] Illinois Capacitor Limited, "Aluminum electrolytic capacitors life expectancy," Aug. 2017. [Online]. Available: https://www.illinoiscapacitor.com/pdf/Papers/Life%20expectancy%20of%20Aluminum%20electrolytic%20capacitors.pdf

[5] X. B. Ruan, B. B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less ac–dc drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1820–1825, Jul. 2011.

[6] B. B. Wang, X. B. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less ac–dc drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[7] C. A. Cheng, C. H. Chang, T. Y. Chung, and F. L. Yang, "Design and implementation of a single-stage driver for supplying an LED street-lighting module with power factor corrections," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 956–966, Feb. 2015.

[8] J. C. W. Lam and P. K. Jain, "Isolated ac/dc offline high power factor single-switch LED drivers without electrolytic capacitors," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 3, no. 3, pp. 679–690, Sep. 2015.

[9] J. C. W. Lam and P. K. Jain, "A high power factor, electrolytic capacitor-less ac-input LED driver topology with high frequency pulsating output current," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 943–955, Feb. 2015.

[10] D. Camponogara, D. R. Vargas, M. A. Dalla Costa, J. M. Alonso, J. Garcia, and T. Marchesan, "Capacitance reduction with an optimized converter connection applied to LED drivers," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 184–192, Jan. 2015.

[11] D. Camponogara, G. F. Ferreira, A. Campos, M. A. Dalla Costa, and J. Garcia, "Offline LED driver for street lighting with an optimized cascade structure," *IEEE Trans. Ind. Appl.*, vol. 49, no 6, pp. 2437–2443, Dec. 2013.

[12] P. Fang, Y. J. Qiu, H. Wang, and Y. F. Liu, "A single-stage primary-side-controlled off-line flyback LED driver with ripple cancellation," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4700–4715, Jun. 2017.

[13] Y. Qiu, L. Wang, H. Wang, Y. F. Liu, and P. C. Sen, "Bipolar ripple cancellation method to achieve single-stage electrolytic-capacitor-less high-power LED driver," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 3, no. 3, pp. 698–713, Sep. 2015.

[14] P. Fang and Y. F. Liu, "Energy channeling LED driver technology to achieve flicker-free operation with true single stage power factor correction," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3892–3907, May 2017.

[15] Z. Shan, X. Chen, J. Jatskevich, and C. K. Tse, "An ac-dc LED driver with an additional active rectifier and a unidirectional auxiliary circuit for ac power ripple isolation," *IEEE Trans. Power Electron.*, to be published.

[16] S. Wang, X. B. Ruan, K. Yao, S. C. Tan, Y. Yang, and Z. H. Ye, "A flicker-free electrolytic capacitor-less ac–dc LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.

[17] Q. C. Hu and R. Zane, "Minimizing required energy storage in off-line LED drivers based on series-input converter modules," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2887–2895, Oct. 2011.

[18] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[19] W. Chen and S. Y. R. Hui, "Elimination of an electrolytic capacitor in ac/dc light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012.

[20] H. C. Kim, M. C. Choi, S. Kim, and D. K. Jeong, "An ac–dc LED driver with a two-parallel inverted buck topology for reducing the light flicker in lighting applications to low-risk levels," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3879–3891, May 2017.

[21] B. White, H. Wang, Y. F. Liu, and X. Liu, "An average current modulation method for single-stage LED drivers with high power factor and zero low-frequency current ripple," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 3, no. 3, pp. 714–731, Sep. 2015.

[22] M. Chen, Y. Ni, C. Serrano, B. Montgomery, D. Perreault, and K. Afridi, "An electrolytic-free offline LED driver with a ceramic-capacitor-based compact SSC energy buffer," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, 2014, pp. 2713–2718.

[23] W. B. Zhang and D. Qiu, "A novel valley-fill single-stage boost-forward converter with optimized performance in universal-line range for dimmable LED lighting," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2770–2778, Apr. 2017.

[24] H. Ma, J. S. Lai, Q. Feng, W. Yu, C. Zheng, and Z. Zhao, "A novel valley-fill SEPIC-derived power supply without electrolytic capacitor for LED lighting application," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3057–3071, Jun. 2012.

[25] H. Ma, J. S. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power ac–dc driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.

[26] H. Valipour, G. Rezazadeh, and M. R. Zolghadri, "Flicker-free electrolytic capacitor-less universal input offline LED driver with PFC," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6553–6561, Sep. 2016.

[27] Richtek, "Single-stage high power factor flyback for LED lighting," Hsinchu, Taiwan, May 2014.

[28] Fairchild, "LED application design guide using half-bridge LLC resonant converter for 100W street lighting," San Jose, CA, USA, Nov. 2011.

[29] Texas Instrument, "A new off-line LED lighting driver solution with multi-transformer LLC control," Dallas, TX, USA, Sep. 2011.

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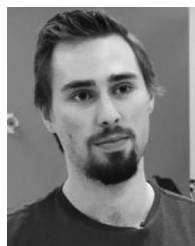
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