A Line Cycle Skipping Method to Improve the Light Load Efficiency and THD of PFC Converters

Christopher Fiorentino, Zhiyuan Hu and Yan-Fei Liu

Department of Electrical and Computer Engineering
Queen's University
Kingston, ON, Canada
c.fiorentino@queensu.ca, zhiyuan.hu@queensu.ca, yanfei.liu@queensu.ca

Abstract— Light load efficiency is becoming a very important performance specification for power supplies. To address the increasing requirements for higher efficiency and lower total harmonic distortion (THD) without increasing the cost or complexity of the design, a Line Cycle Skipping (LCS) method is proposed. This method can be applied to all PFC topologies. A 100W universal line input voltage PFC boost converter prototype is built to demonstrate the effectiveness of the proposed method.

I. INTRODUCTION

With tremendous growth in computer electronics and energy efficient lighting, there has been a lot of focus on the design of power factor correction (PFC) converters for such applications. The energy efficiency and power quality of such converters have become increasingly important. Products that wish to qualify for the Energy Star program must meet or exceed certain efficiency requirements [1, 2]. Also, the total harmonic distortion (THD) of PFC converters must meet the IEC 61000-3-2 standard which sets harmonic current limits for different categories [3]. These standards and regulations are increasingly strict about light load conditions because more and more devices tend to stay in light load for longer periods of time (e.g. computers, TV boxes, etc.); and the poor performance in light load condition counts for a significant percentage of the total power loss [4].

Yet improving the light load performance of PFC converters is the most challenging due to the following reasons: (a) the switching loss, driving loss, and reverse recovery loss of semiconductor components become dominant losses at light load, which is difficult to reduce; (b) due to the difficulties in detecting low-amplitude signals, and possibly the change from CCM to DCM mode, current distortion is much more severe at light load; (c) for boundary conduction mode (BCM), the switching frequency is higher at light load, adding even more losses. Due to these considerations, there have been many methods introduced to improve the light load efficiency and reduce the THD [5-17]. Some research has only addressed the efficiency at the no-load or stand-by condition for PFC converters, and does not address the entire light load range [19-20]. For interleaved PFC topologies, light load efficiency improvements are specific to the topology itself, using phase shedding as the primary means of efficiency improvement [8-10, 14, 17]. One research paper devises a method to improve the light load efficiency for all PFC converters, but at the cost of increasing the THD [18].

Cost is a very important consideration when adopting a method to improve the efficiency and reduce the THD. While adaptive control methods are attractive because of their ability to change control strategies based on the operating conditions, most of these methods require high a cost DSP, FPGA, or ASIC in order to implement the sophisticated techniques [5-8, 12, 16]. A simpler and lower-cost control method would be more attractive and more practical.

In this paper, a Line Cycle Skipping control method is proposed to increase the light load efficiency and reduce the THD at light load by skipping one or more entire line cycles with different patterns. Its advantages include: (a) it is very simple and can be implemented using a low cost microcontroller unit (MCU); (b) it can apply to all PFC topologies; (c) the light load efficiency and THD can be maintained at the peak level as if in medium-heavy load condition, shown in Fig. 1.

The following sections are organized as follows: Section II provides the description, analyses, and design considerations of the proposed Line Cycle Skipping control method; Section III presents experimental results; and Section IV concludes the paper.

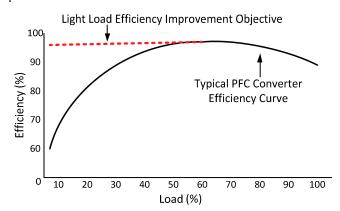


Figure 1. Light load efficiency improvement objective

II. PROPOSED LINE CYCLE SKIPPING METHOD

A. Operating Principle

The idea of the Line Cycle Skipping (LCS) control method is described as follows: at light load, the controller selects to skip one or more line cycles, and then operates for one or one-half line cycle (LC) and draws an amount of current that

corresponds to the peak efficiency power level. This way, the PFC is either operating at peak efficiency or completely shut down; thus even if the average output power is low, the efficiency and THD are the same as at the peak efficiency condition. By applying different skipping patterns, LCS is able to maintain peak efficiency and low THD throughout the entire light load range.

An example case is given in Fig. 2 to explain the two modes of the proposed LCS method. In Method 1, line current is conducted for one complete LC at a power level of 45W and skipped for 2 LCs with a power draw of 0W. The average power over the entire LCS period is 15W. In Method 2, line current is conducted for one positive half LC with a power draw of 45W and skipped for four half LCs drawing no power. The average output power is 9W, and the next LCS period will draw from the negative half LC with the same power draw sequence as before. In Method 2, line current

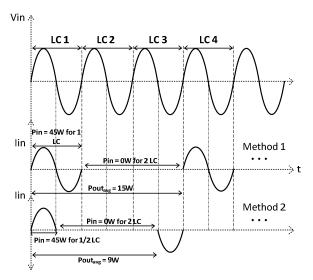


Figure 2. The proposed line cycle skipping methods

must be conducted for an equal amount of positive and negative cycles to avoid introducing a DC bias. If Method 2 were to only skip 1 LC instead of two, it would have the same average power as Method 1.

B. Analyses of Light Load Efficiency and THD Improvement

Equation (1) is the general equation for these methods, which calculates the average input power, $P_{IN,AVG}$, where $P_{IN,AVG,cond}$ and $P_{IN,AVG,skip}$ are the average input power over 1 LC. As seen in (1), the average input power is calculated by summing the average power of each LC conducted by the converter with the average input power of each LC skipped or not conducted by the converter. Finally, this sum is divided by the sum of the LCs conducted and skipped. In the case of Method 2, $Linecycles_{cond}$ will not be an integer number. The average output power can be calculated by multiplying it with the estimated efficiency of the converter, η , to give (2) and effectively (3), both shown below.

$$P_{IN,AVG} = \frac{P_{IN,AVG,cond} + P_{IN,AVG,skip}}{Linecycles_{cond} + Linecycles_{skip}} \tag{1}$$

$$P_{OUT,AVG} = P_{IN,AVG} \times \eta \tag{2}$$

$$P_{OUT,AVG} = \frac{(P_{IN,AVG,cond} + P_{IN,AVG,skip}) \times \eta}{Linecycles_{cond} + Linecycles_{skip}}$$
(3)

The significance of (2) and (3) are highlighted by Fig. 2 because the efficiency at $Pout_{AVG}$ is now equal to the average input power during the conduction period. For example, if peak efficiency is to be maintained for load levels below the power level at the peak efficiency, then that power level is used during the conduction period so that the average output power maintains peak efficiency during the entire load range. Based on this, the light load efficiency of the converter will be significantly increased and closely resemble the achievement objective shown in Fig. 1.

The LCS control method can also greatly reduce the THD of a PFC converter. Equation (4) is the equation for THD for line current conducted by a PFC converter, where I_1 , I_3 , I_5 , I_7 , I_9 , ... are the currents at their respective harmonics. To reduce

$$I_{THD} = \frac{\sqrt{I_3^2 + I_5^2 + I_7^2 + I_9^2 \dots}}{I_1} \tag{4}$$

the THD of a PFC converter, the odd harmonics of the line frequency must be reduced. Ideally, a PFC converter acts like an emulated resistor to change the behavior of the non-linear load into a linear one. Therefore, the power transferred to the load will contain no harmonics. In practice, however, harmonics are generated over that line cycle and are calculated together as the THD. When the PFC converter is turned off, no harmonics are generated because usually no current is drawn from the source.

The contribution of harmonics to (4) only occurs during the period in which the PFC converter is turned on. These harmonics are generated during the conduction period, shown in Fig. 2 where the conduction period for Method 1 conducts 45W for 1 LC and Method 2 conducts 45W for one half-LC. No contribution of harmonics to (4) is generated during the skipping period in either method. The harmonic contribution to (4) for either method would be generated as if the converter was operating at 45W continuously. Therefore, the THD at the average output power observed, 15W and 9W for methods 1 and 2 respectively, is the same value of THD at 45W.

C. Design Considerations

To implement the LCS control mode, a controller only needs to detect a new half LC and be able to conduct sinusoidal line current for the conduction period, as well as not conduct line current for the skipping period. Since the LCS control method is based on the output voltage feedback loop, the proposed method is compatible with all PFC converters that can:

- Detect the zero crossing of the input line voltage
- Detect the output power either directly or indirectly

1) Detecting the zero crossing of the input line voltage

The zero crossing of the line input voltage must be detected in order to determine when a new half-LC has begun. This sensing can be done after the bridge rectifier or by sensing the input line voltage directly, as shown in [20]. This detection must be done even when the PFC is turned off in order to determine how many LCs have been skipped and

when the exact moment the PFC should be turned back on. This is illustrated in Fig. 3, where the conduction period is 1 LC and the skipping period is 2 LCs.

2) Detecting the output power directly or indirectly

The output power must be detected directly or indirectly in order for the LCS control method to determine the number of cycles to conduct and the number of cycles to skip. An indirect method to detect the output power is to determine the duty cycle in fixed frequency control methods (such as average current mode control), or to determine the on-time of the switch, Ton, in variable frequency control methods (such as BCM control), as it relates to input or output current. A calculation can then be done to determine the approximate output power.

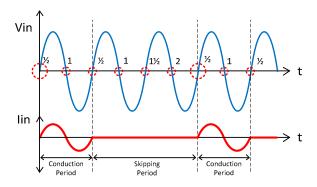


Figure 3. Zero crossing detection and cycle counting of input line voltage for determining conduction period and skipping period

To directly determine the output power, one must sense the average output current or input current as it relates to the output current and output voltage, and then calculate the output power based on these two values. The advantage of the indirect method over the direct method of determining the output power is that no additional components are needed, thereby lowering the cost.

D. Digital Implementation

To implement the LCS control method digitally, the zero crossing of the line input voltage can be easily sensed using an analog to digital converter (ADC) on a MCU. Determining this zero crossing will depend on whether the line voltage is sensed directly or after the bridge rectifier. Using an additional ADC channel, the output voltage must be sensed. This sensing is usually done anyways for output voltage regulation, so the sampled voltage data can be used for both purposes.

The last piece of information needed to implement the LCS control method is the current information. As stated previously, this can be done indirectly, which is preferable because it requires less components than directly sensing, and is insensitive to noise that would otherwise be generated from measuring it directly. The duty cycle or on-time signal sent to the switch(es) will generally correlate with the input and output current information. Using this information, an internal calculation can be done at the end of each LC to calculate the average input or output power, so that peak efficiency can be maintained throughout the entire light load range. Fig. 4

shows the digital control implementation for any PFC converter using a bridge rectifier.

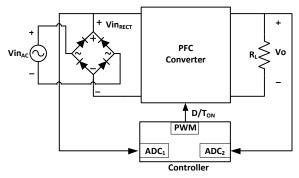


Figure 4. Digital control implementation for PFC converters implementing the LCS method

III. EXPERIMENTAL RESULTS

A 100W universal line input voltage PFC boost converter prototype was built and implemented with a ST7FLIT19B MCU [22] to implement the LCS control method in order to improve the light load efficiency and reduce the THD. Fig. 5 shows the circuit diagram for the prototype. A ST7FLIT19B low cost 8-bit MCU is used for the digital implementation, based off a previous design for a digital ballast [23]. ZCD is achieved through an auxiliary winding in the boost inductor connected to an edge detection pin on the MCU. This allows for a rising or falling edge detection of the inductor voltage waveform to trigger the switch to turn on when the current in the inductor falls to zero. Input voltage is sensed by an ADC on the MCU, which allows for mains voltage detection as well as the detection of a new half LC. A constant on-time PWM is used to achieve BCM without a current reference calculation. This allows for a low cost MCU to be used in this control method, thereby lowering the total cost of the system.

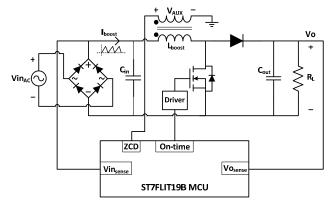


Figure 5. PFC boost converter prototype

Table 1 describes the specifications, components and the values of the components used for the boost converter prototype. Fig. 6 shows the input line voltage and the input line current for the prototype at 50W load operating in conventional BCM with constant on-time. Fig. 7 shows the prototype operating with LCS using Method 1 for an average

Table 1. Prototype specifications

22 kHz	
120, 220 V _{RMS}	
400 Vdc	
100W	
1 mH	
1:12 Turns	
$0.47 \text{ uF} \pm 20\%$	
$120 \text{ uF} \pm 20\%$	
STD10NM60N	
(600V, 8.0A)	
S8KC-13	
(800V, 8.0A)	
GBU6J-BP	
(600V, 6A)	
ST7FLIT19B, 8MHz	
MCP1407-E	

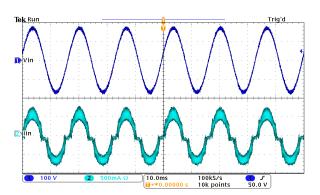


Figure 6. Input voltage and current waveforms at Pin = Po = 50W without LCS

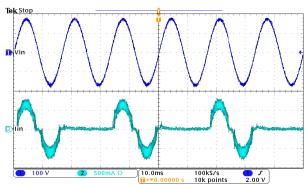


Figure 7. Input voltage and current waveforms at $P_{\rm IN}$ = 50W over the conduction period, $P_{\rm OUT,AVG}$ = 25W for Method 1; 1 LC on, 1 LC off

output power of 25W. Sinusoidal line current is conducted for 1 LC at a power level of 50W. The total average power is 25W. Fig. 8 and Fig. 9 show input voltage and current waveforms using Method 2 for 10W and 5W load respectively.

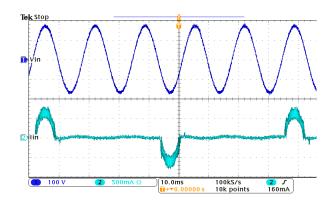


Figure 8. Input voltage and current waveforms at $P_{\rm IN}$ = 50W over the conduction period, $P_{\rm OUT,AVG}$ = 10W for Method 2; 1/2 LC on, 2 LC off

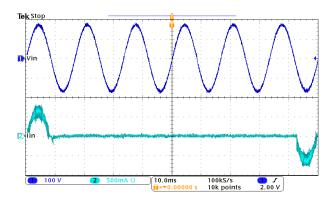


Figure 9. Input voltage and current waveforms at $P_{\rm IN}$ = 55W over the conduction period, $P_{\rm OUT,AVG}$ = 5W for Method 2; 1/2 LC on, 5 LC off

As can be seen in Fig. 10, at $120~V_{RMS}$ input, the light load efficiency has dramatically increased by using the LCS control method. Efficiency gains as high as 7.2% at 10% load can be observed. Efficiency improvements are significant up to 50% load, when the LCS control method is used. The results for THD with and without LCS are shown in Fig. 11. As can be seen in Fig. 11, the THD is dramatically reduced by up to 15.25% at 10% load. Improvements in THD can also be seen when the LCS control method is used up to 50% load.

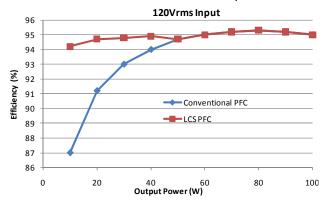


Figure 10. Efficiency results with and without LCS at 120 $V_{\text{RMS}}\,$

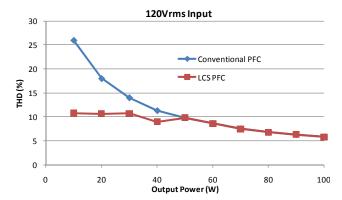


Figure 11. THD results with and without LCS at 120 V_{RMS}

In addition to testing the converter at $120~V_{RMS}$, the prototype was also tested at $220~V_{RMS}$. As can be seen in Fig. 12, the light load efficiency has also dramatically increased by using the LCS control method at $220~V_{RMS}$. Efficiency gains as high as 8.6% at 10% load can be observed. Efficiency improvements are also significant up to 50% load when the LCS control method is used. The results of THD

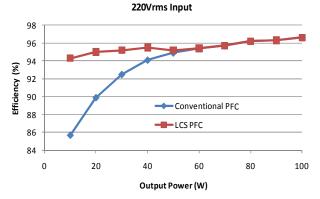


Figure 12. Efficiency results with and without LCS at 220 V_{RMS}

with and without LCS are shown in Fig. 13. As can be seen in Fig. 13, the THD has again dramatically reduced. A reduction of up to 17.3% at 10% load can be observed. Improvements, again, in THD can also be seen when the LCS control method is used up to 50% load.

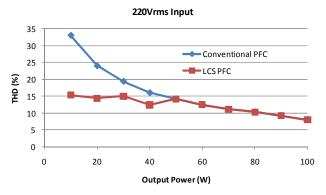
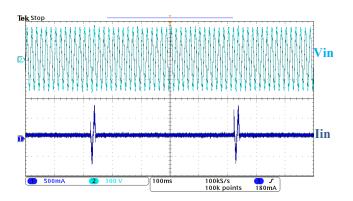


Figure 13. THD results with and without LCS at 220 V_{RMS}

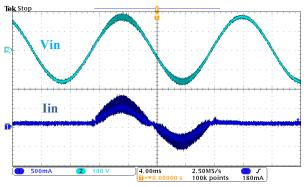
Finally, additional testing at very light load was conducted and includes the controller loss, which has a more pronounced effect at very light load conditions. The power loss due to the MCU is approximately constant during the conduction period and the skipping period. This value is 47.7mW. The driver loss, however, decreases with the amount of LCs skipped. This is due to the fact that the driver is idle during the skipping period. If the driver were to run continuously, as is usually the case in the conventional control method, the power consumption for all load levels would be approximately 51.8mW. Using LCS, results were obtained for 1W, 2W and 5W operating at 120 $V_{\rm RMS}$ input, shown in Table 2 below. The measured waveforms at 1W output are shown in Fig. 14(a) and Fig. 14(b) respectively.

Table 2. Very light load efficiency results at 120Vrms

Output Power	Converter Loss + MCU loss	Driver Loss	Efficiency
1 W	144.2 mW	1.8 mW	87.3%
2 W	214.5 mW	3.5 mW	90.2%
5 W	447.3 mW	8.7 mW	91.6%



(a) LCS for 1W showing two conduction periods



(b) Expanded waveform of (a), showing conduction period

Figure 14. Input voltage and current waveforms at $P_{IN} = 30$ W over the conduction period, $P_{OUT,AVG} = 1$ W for Method 2; 1 LC on, 29 LCs off

IV. CONCLUSION

In this paper, a Line Cycle Skipping method is proposed to increase the light load efficiency and reduce the THD of a universal line input voltage PFC converter. It dramatically improves the light load efficiency by 7.2% and 8.6% at 10% load for 120 V_{RMS} and 220 V_{RMS} respectively. A reduction of THD by 15.25% and 17.3% at 10% load for 120 V_{RMS} and 220 V_{RMS} respectively, can also be observed using the LCS control method. Even at very light load, the LCS method maintains a high efficiency of 87.3% even at 1W operation, while also reducing the MOSFET driver power loss without additional circuitry.

The LCS control method can be applied to any PFC converter that senses the input line voltage and output power either directly or indirectly, where the latter can be achieved without adding cost or complexity. Due to the simplicity of the LCS method, a low cost MCU is used for the implementation of the control method while achieving the objective light load efficiency results and reducing the THD.

REFERENCES

- Energy Star. (2009). ENERGY STAR® Program Requirements for Computers (Version 5.0) [Online]. Available: http://www.energystar.gov
- [2] Energy Star. (2008). ENERGY STAR® Program Requirements for Single Voltage External Ac-Dc and Ac-Ac Power Supplies (Version 2.0) [Online]. Available: http://www.energystar.gov
- [3] EPSMA. (2010). Harmonic Current Emissions Guidelines to the standard EN 61000-3-2. [Online]. Available http://www.epsma.org/ pdf/PFC%20Guide November%202010.pdf
- [4] Climate Savers Computing. (2007). PC Energy Report 2007 United States. [Online] http://www.climatesaverscomputing.org/
- [5] Q. Li, F.C. Lee, M. Xu and C. Wang, "Light Load Efficiency Improvement for PFC", in *Energy Conversion Congress and Exposition*, 2009, pp. 3755-3760.
- [6] S.F. Lim and A. M. Khambadkone, "A multimode digital control scheme for boost PFC with higher efficiency and power factor at light load," in *Applied Power Electronics Conference and Exposition*, 2012, pp. 291-298.
- [7] F.Z. Chen and D. Maksimovic, "Digital Control for Improved Efficiency and Reduced Harmonic Distortion over Wide Load Range in Boost PFC Rectifiers," in *Applied Power Electronics Conference and Exposition*, 2009, pp. 760-766.
- [8] X. Xu, W. Liu and A.Q. Huang, "Two-Phase Interleaved Critical Mode PFC Boost Converter With Closed Loop Interleaving Strategy," *IEEE Trans. Power Electron.*, vol.24, no.12, pp.3003-3013, Dec. 2009

- [9] T. Grote, H. Figge, N. Frohleke, W. Beulen, F. Schafmeister, P. Ide and J. Bocker, "Semi-Digital Interleaved PFC Control with Optimized Light Load Efficiency," in *Applied Power Electronics Conference and Exposition*, 2009, pp.1722-1727
- [10] T. Grote, H. Figge, N. Frohleke, J. Bocker and F. Schafmeister, "Digital control strategy for multi-phase interleaved boundary mode and DCM boost PFC converters," in *Energy Conversion Congress and Exposition*, 2011, pp.3186-3192
- [11] S.F. Lim and A.M. Khambadkone, "Non linear inductor design for improving light load efficiency of boost PFC," in *Energy Conversion Congress and Exposition*, 2009, pp.1339-1346
- [12] S.F. Lim and A.M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," in *Energy Conversion Congress and Exposition*, 2010, pp.1218-1225
- [13] Y.K. Lo, S.C. Yen and C.Y. Lin, "A High-Efficiency AC-to-DC Adaptor With a Low Standby Power Consumption," *IEEE Trans. Ind. Electron.*, vol.55, no.2, pp.963-965, Feb. 2008
- [14] B. Lu, "A novel control method for interleaved transition mode PFC," in Applied Power Electronics Conference and Exposition, 2008, pp.697-701
- [15] J. Hwang and A. Chee, "Improving efficiency of a pre-/post-switching regulator (PFC/PWM) at light loads using green-mode function," in Applied Power Electronics Conference and Exposition, 1998, pp.669-675
- [16] W.S. Wang and Y.Y. Tzou, "Light load efficiency improvement for AC/DC boost PFC converters by digital multi-mode control method," in *Power Electronics and Drive Systems*, 2011, pp.1025-1030
- [17] C. Wang, M. Xu, F.C. Lee and Z. Luo, "Light load efficiency improvement for multi-channel PFC," in *Power Electronics Specialists Conference*, 2008, pp.4080-4085
- [18] Y. Jang and M.M. Jovanovic, "Light-Load Efficiency Optimization Method," *IEEE Trans. Power Electron.*, vol.25, no.1, pp.67-74, Jan. 2010
- [19] K.Y. Lee and Y.S. Lai, "Novel circuit design for two-stage AC/DC converter to meet standby power regulations," *IET Power Electron.*, vol.2, no.6, pp.625-634, Nov. 2009
- [20] B.H Lee, B.W. Ryu, S.W. Choi and G.W Moon, "AC/DC notebook adapter with 22mW no-load power consumption," in *Power Electronics* and ECCE Asia, 2011, pp. 468-473.
- [21] Texas Intruments. (2004). UCC38050 100W Critical Conduction Power Factor Corrected (PFC) Preregulator - Application Note [Online]. Available: http://www.ti.com/lit/an/sluu138a/sluu138a.pdf
- [22] STMicroelectronics. (2008). ST7LITE1xB Datasheet [Online]. Available: http://www.st.com/internet/com/TECHNICAL_RESOURC ES/TECHNICAL_LITERATURE/DATASHEET/CD00081035.pdf
- [23] STMicroelectronics. (2008). AN2640: Intelligent multipower digital ballast for fluorescent lamps [Online]. Available: http://www.st.com/ internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATU RE/APPLICATION_NOTE/CD00173891.pdf