

Fig. 1 HB CSD topology

Block capacitor voltage  $V_{cb}$

Inductor Current  $i_{Lr}$

Input voltage  $V_{in}$

Input Current  $I_{in}$

Duty Cycle

Fig. 2 Key waveforms of the boost PFC converter with the HB CSD

Therefore, the CSD solution for the PFC converters should have no blocking capacitor. The CSDs with discontinuous current are suitable to this application, but its drawback is complex control and without integration as a drive chip, it is hard to use this technology with commercially available drive chips and controller right now. Furthermore, it needs complex control to achieve adaptive gate drive current.

#### B. The Proposed CSD Circuit for Boost PFC Converter

Fig. 3 shows the proposed CSD solution for the PFC application. Fig. 4 shows the key waveforms. Fig. 5 shows the single phase boost PFC stage with the CSD. Compared to Fig. 1,  $S_2$  and  $S_4$  are used to remove the blocking capacitor, which forms a full bridge CSD topology. Since there is no blocking capacitor, the proposed CSD can be suitable for the PFC application, where the duty cycle keeps changing.

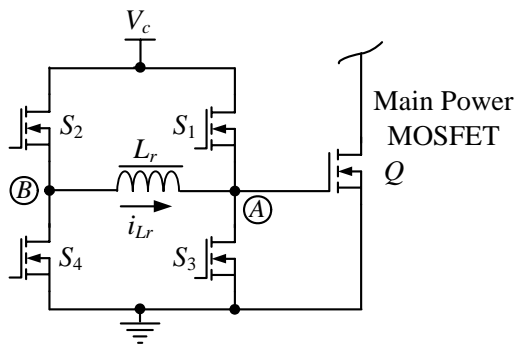


Fig. 3 Proposed CSD Solution for PFC applications

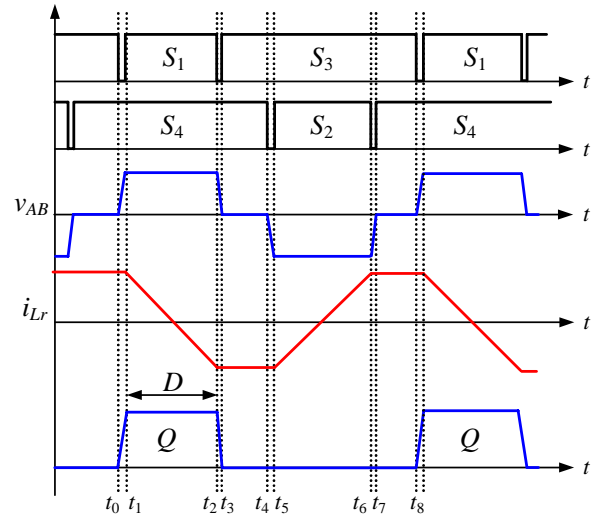


Fig. 4 Key waveforms

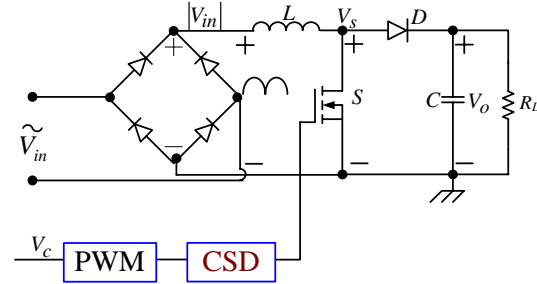


Fig. 5 Proposed CSD solution for the boost PFC converter

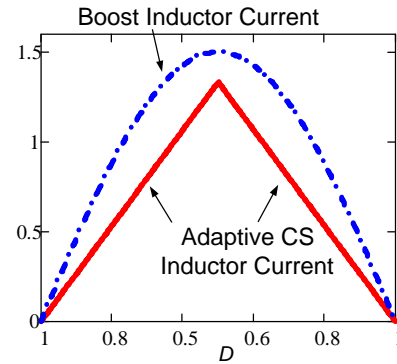


Fig. 6 Inductor current with the duty cycle

Fig. 6 shows the peak current value of the CS inductor, which is used to drive the main power MOSFET. It is observed that the drive current changes with the duty cycle and the value can be chosen when the CS inductor value is decided. It should be also noted that the operation region of adaptive drive current is limited by the duty cycle range. For a boost PFC converter with 120V input and 380V output, the minimum modulated duty cycle is 0.55. According to Fig. 6, when  $0 < D < 0.55$ , the CS inductor current increases with the boost inductor current increasing; when  $0.55 < D < 1$ , the inductor current decreases with the boost inductor current decreasing. This means the drive current is able to behavior adaptively according to the MOSFET switching current.

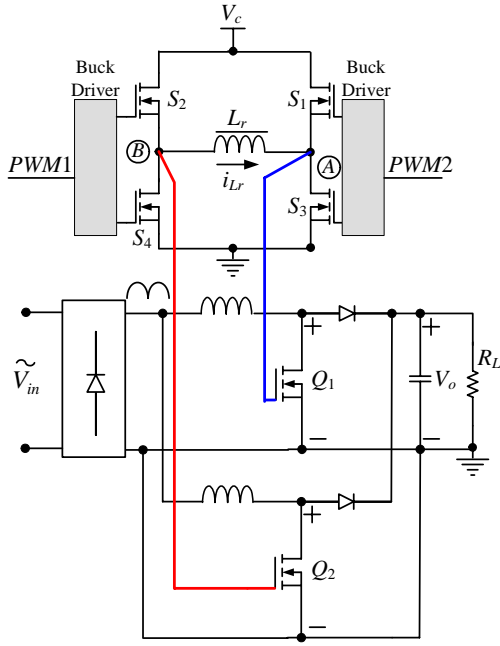


Fig. 7 Interleaving boost PFC converters with the CSD

As seen from Fig. 4,  $S_1$  &  $S_3$  and  $S_2$  &  $S_4$  are complementarily controlled, which is similar to the control of the synchronous buck converters. Therefore, another advantage of this solution is that the commercial off shelf components can be directly used instead of using discrete ones in other CSD circuits [12]-[13]. This is important since the present CSDs were built with many discrete components and no commercial integrated CSD ICs are available now. Moreover, the presented CSD solution with one inductor can actually be directly used to drive two interleaving boost PFC converters as shown in Fig. 7.

### III. LOSS ANALYSIS OF THE FB CSD FOR BOOST PFC CONVERTER

The efficiency of the PFC stage is determined by the power losses of the input diode bridge, the boost inductor, the main switch, and the rectifier diode. The active switch and boost diode are under hard switching conditions with the fixed switching frequency operation. Therefore, the dominant losses are caused by the switching losses in the active switch and boost diode. The loss analysis of a boost PFC converter with the proposed CSD is presented as follows:

#### 1) The loss of the power MOSFET

The losses of the power switch include the conduction loss and switching loss. For a single phase PFC converter, the current which flows through the main switch has a half sinusoidal shape. The switching loss  $P_{sw}$  and conduction loss  $P_{cond}$  are (1) and (2) respectively.

$$P_{sw} = \frac{2 \int_0^{T_{line}} K f_s V_o I_{L4pk} \sin(\omega_L t) (T_r + T_f) dt}{T_{line}} \quad (1)$$

$$P_{cond} = \frac{2 \int_0^{T_{line}} \frac{1}{2} I_{L4pk} \sin(\omega_L t) R_{ds(on)} dt}{T_{line}} \quad (2)$$

where  $\omega_L = 2\pi f_L$ ,  $T_r$  and  $T_f$  are the rising time and the falling time of MOSFET respectively.  $I_{L4pk}$  is the peak of input boost inductor current. The constant  $K$  is typically between 1/6 and 1/2.  $T_{line}$  is line period and  $f_s$  is the switching frequency.

#### 2) The conduction loss of the boost diode

The power losses of the boost diode include the forward conduction loss and the reverse recovery related switching loss. With the SiC diode, the reverse recovery is low, so the power loss of the diode is

$$P_{fd} = \frac{2 \int_0^{T_{line}} \frac{1}{2} I_{L4pk} \sin(\omega_L t) V_{f4fd} dt}{T_{line}} \quad (3)$$

where  $V_{f4fd}$  is the forward voltage drop of the boost diode.

#### 3) The conduction loss of the rectifier bridge

The rectifier bridge has four rectifier diodes, the conduction loss of the rectifier bridge is

$$P_{rd} = \frac{4}{T_{line}} \int_0^{T_{line}} I_{L4pk} \sin(\omega_L t) V_{f4rd} dt \quad (4)$$

where  $V_{f4rd}$  is the forward voltage drop of the rectifier diodes.

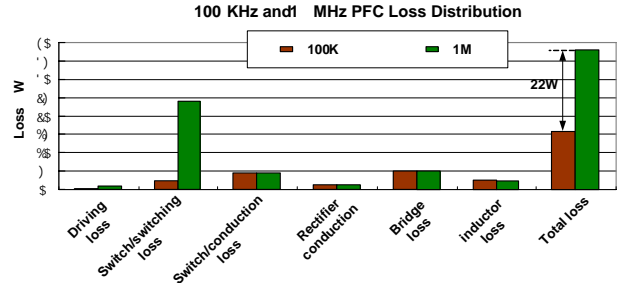


Fig. 8 Loss distribution of the boost PFC converter with 100KHz and 1MHz:  $V_{in}=110V$ ,  $V_o=380V$  and  $P_o=300W$

Fig. 8 shows the loss breakdown of the 300W boost PFC converter with 100kHz and 1MHz. For the boost converter, the 600V/11A CoolMOS™ SPA11N60 from Infineon and the SiC Schottky diode CSD06060 from CREE are used. The input line voltage is 110V and the output voltage is 380V.

From Fig. 8, it is observed that the switching loss is the dominant loss of the PFC while the switching frequency becomes 1MHz, which is as much as ten times of the switching loss in 100KHz. This results in poor efficiency when the boost PFC converter runs at 1MHz. The predicted efficiency of the 100KHz converter is 94.5%, while the efficiency of the 1MHz converter is only 89.1% in comparison.

In order to improve the efficiency, the proposed CSD is employed to reduce the switching loss of the converter. The total power losses of the CSD circuit are listed as below:

#### 1) The CS inductor loss

$$P_{copper} \mid R_{ac} \mid I_{LRMS}^2 \quad (5)$$

$$P_{ind} \mid P_{copper} + P_{core} \quad (6)$$

where  $I_{LRMS}$  is the RMS value of the CS inductor current,  $R_{ac}$  is the AC resistance of the inductor winding,  $P_{copper}$  is the copper loss and  $P_{core}$  is the core loss.

### 2) The mesh resistance loss of the power MOSFET

$$P_{RG} \mid 2 \mid R_G \mid I_{Lpeak}^2 \mid t_{sw} \mid f_s \quad (7)$$

where  $R_G$  is the internal gate mesh resistance,  $t_{sw}$  is the switching time and  $I_{Lpeak}$  is the peak value of the CS inductor current.

### 3) The total conduction loss of $S_1$ - $S_4$

$$P_{cond} \mid 2 \mid R_{DS(on)} \mid I_{Lpeak}^2 \mid \frac{4D41}{3} \quad (8)$$

where  $R_{DS(on)}$  is the on-resistor of the four switches.

### 4) The total gate drive loss of four switches

$$P_{Gate} \mid 4 \mid Q_{gs} \mid V_{gs4s} \mid f_s \quad (9)$$

where  $Q_{gs}$  is the total gate charge of switch and  $V_{gs}$  is the drive voltage of the switch.

From (6), (7), (8) and (9), the total loss of the CSD is

$$P_{drv} \mid P_{ind} + P_{RG} + P_{cond} + P_{Gate} \quad (10)$$

## A Loss Comparison with 110V Input

With the input voltage  $V_{in}=110V$ , output voltage  $V_o=380V$ , 1MHz/300W PFC converter, the loss of the CSD is shown in Fig. 9. In this case, the drive voltage  $V_c$  is 15V, DO3316P-1uH is chosen for the CS inductor and the power MOSFET is SPA11N60.

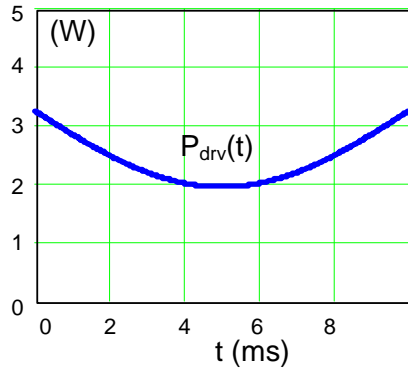


Fig. 9 The loss of CSD circuit in half of line period

With input voltage  $V_{in}=110V$ , output voltage  $V_o=380V$ , the duty cycle of the boost PFC converter is:

$$D/t0 \mid 14 \frac{V_{in} \mid \sin \omega_L t \mid}{V_o} \quad (11)$$

From (2), the gate drive current is given by:

$$i_g / t0 \mid \frac{V_{cc} \left( 14 D / t0 \right)}{2 f_s L_r} \mid \frac{V_{cc} V_{in} \mid \sin \omega_L t \mid}{2 f_s L_r V_o} \quad (12)$$

As an ideal current source driver, the switching loss of the power MOSFET with CSD is

$$P_{sw4csd} / t0 \mid \frac{1}{2} f_s V_o I_L / t0 \left( T_{rcsd} / t0 + T_{fcsd} / t0 \right) \quad (13)$$

$$T_{rcsd} / t0 \mid \frac{Q_{pl} 4 Q_{th} + Q_{gd}}{I_g / t0} \quad (14)$$

$$T_{fcsd} / t0 \mid \frac{Q_{pl} 4 Q_{th} + Q_{gd}}{I_g / t0} \quad (15)$$

where  $Q_{pl}$  is the MOSFET total gate charge at the beginning of the plateau;  $Q_{th}$ , the total gate charge at the threshold and  $Q_{gd}$ , the gate-to-drain charge.  $T_{rcsd}$  is the rising time and  $T_{fcsd}$  is the falling time with CSD.

Fig. 10 illustrates the switching time comparison with the CSD and conventional driver, and the CSD gate drive current  $i_g$ . Between  $t_1$  and  $t_2$ , in half of line period, the switching time with the CSD is much reduced over the voltage driver. At the same time, it is observed that when  $i_g$  increases, the switching time of the CSD drops rapidly, which means significant switching loss reduction.

During  $[0, t_1]$  and  $[t_1, T_{line}/2]$ , it is also noted that the switching time with the CSD is longer than that with the voltage driver. This is because during these intervals, the gate drive current is not large enough to turn on the power MOSFET completely. However, what happens is that during the dead time of two drive switches, the CSD behaviors as a voltage driver with an effective drive current of 0.8A.

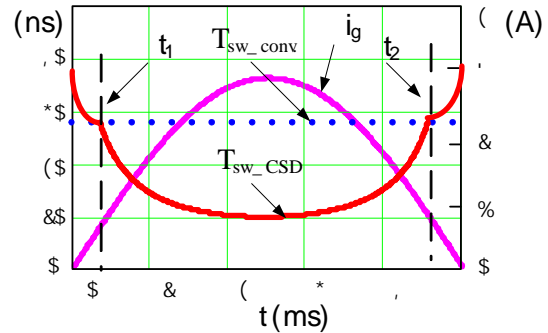


Fig. 10 The switching time with the CSD with the low line voltage in half of line period ( $V_{in}=110V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1uH$ )

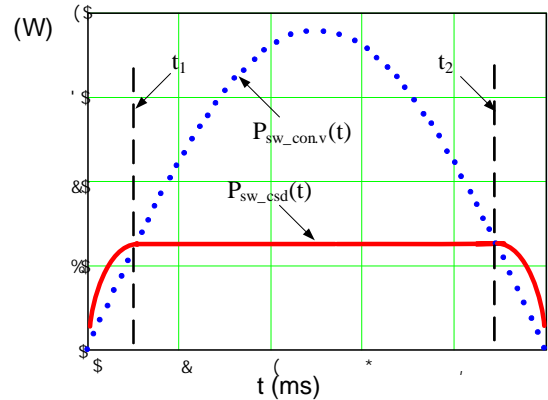


Fig. 11 The actual switching loss with the CSD compared with the conventional gate driver in half of line period ( $V_{in}=110V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1uH$ )

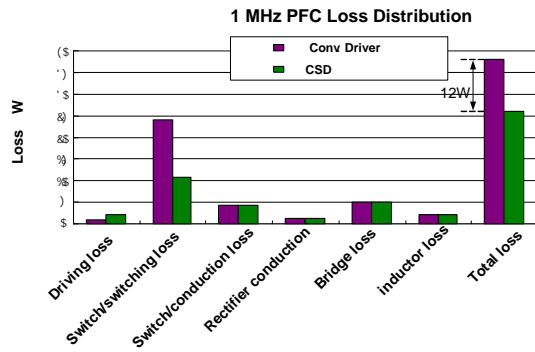


Fig. 12 Loss breakdown between the CSD and the conventional driver at 1MHz ( $V_{in}=110V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1\mu H$ )

Based on Fig. 10, the switching loss comparison is shown in Fig. 11. However, it should be noted that at low line voltage, the input current is low and the switching current is also low. Therefore, the switching loss happens at the low line voltage is limited among the line period. Overall, the CSD can reduce the switching loss much over the conventional voltage driver.

Fig. 12 shows the 1MHz PFC loss distribution comparison. At 110V input, 380V output voltage, the CSD reduces the total loss of 12W, which translates into an efficiency improvement of 3.1% (from 89% to 92.1%).

#### B. Loss Comparison of 220V Input

With  $V_{in}=110V$  and  $V_o=380V$ , during half of line period, the duty cycle of the boost PFC converter is always above 0.5. From (2), the current of the CS inductor is proportional to  $(1-D)$ . Therefore, the curve of the CS gate drive current can be adaptive to the switching current of the power MOSFET in half of line period.

If the input voltage increases to 220V, compared to the 110V condition, the duty cycle of the power MOSFET is not always above 0.5. In order to understand this mode, the detailed analysis is given as follows.

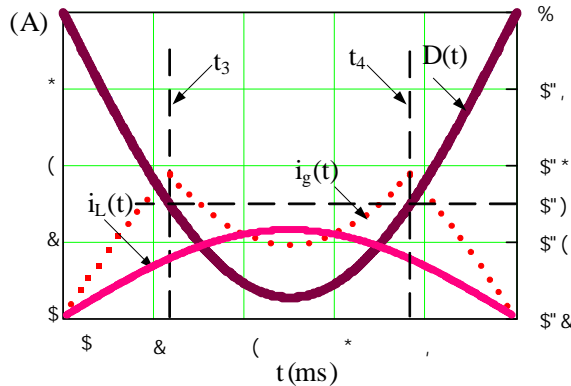


Fig. 13 Duty cycle  $D$ , gate drive current  $i_g$  and boost inductor current  $i_L$  in half of line period ( $V_{in}=220V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1\mu H$ )

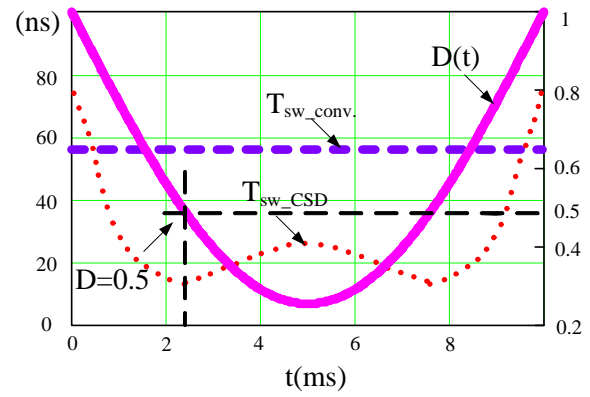


Fig. 14 The switching time with the CSD compared with the conventional driver in half of line period ( $V_{in}=220V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1\mu H$ )

Fig. 13 shows the duty cycle  $D(t)$ , the CS gate drive current  $i_g(t)$  and boost inductor current  $i_L(t)$  during the half of line period. As seen from Fig. 13, between  $t_3$  and  $t_4$ , the gate drive current  $i_g$  drops, and as a result, the switching time of the power MOSFET increases. This is because when  $D < 0.5$ , the CS current will be governed by (1). Fig. 14 shows the switching time with the CSD compared with the conventional driver. According to Fig. 13, although the gate drive current drops during  $[t_3, t_4]$ , and is not adaptive to the switching current, but compared with conventional drivers, the switching time  $T_{sw\_CSD}$  with CSD is still reduced drastically (see Fig. 14).

Based on Fig. 14, Fig. 15 gives the associated switching loss comparison. with  $V_{in}=220V$ . As from Fig. 15, the switching loss reduction with the CSD is less compared to the value with 110V input (see Fig. 11). Fig. 16 shows the loss breakdown between the CSD and the conventional driver with 220V input. The CSD improves the 1MHz PFC efficiency from 93.8% to 95.6% with 220V input.

Fig. 17 gives the efficiency of 1MHz/300W PFC in comparison with different input voltages. At the same time, it is noted that the CSD achieve higher efficiency improvement with lower input line voltage.

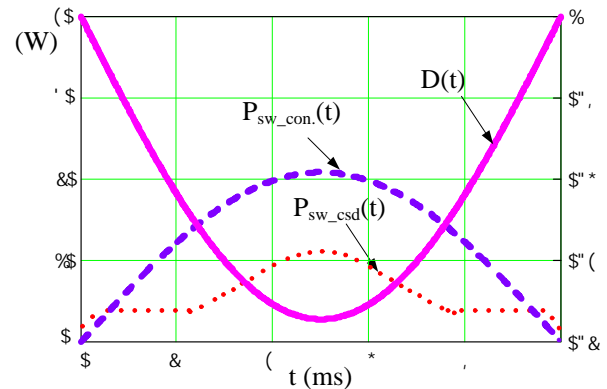


Fig. 15 The actual switching loss with the CSD compared with conventional gate driver in half of line period ( $V_{in}=220V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=1\mu H$ )

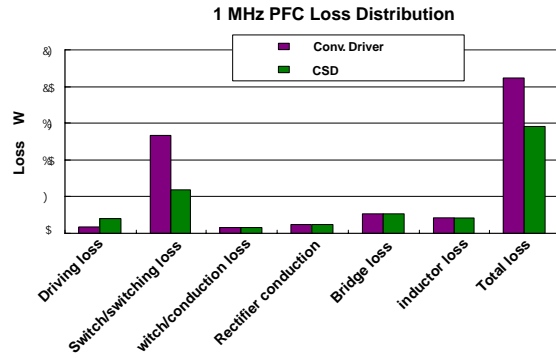


Fig. 16 1MHz PFC loss breakdown between the CSD and the conventional driver with 220V input voltage

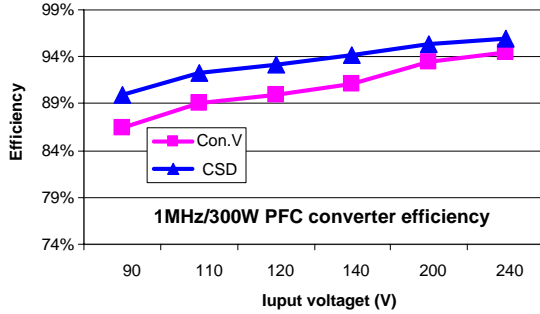


Fig. 17 The efficiency comparison between the CSD and the conventional voltage driver with different line voltages

#### IV. DESIGN OPTIMIZATION

For a boost PFC converter with 110V input and 380V output, in order to achieve optimal design, the idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together [13]. The object function should be a U-shape curve as function of the max drive current  $I_{gmax}$ . The specifications are:  $V_{in}=110V$ ;  $V_o=380V$ ;  $P_o=300W$ ;  $f_s=1MHz$ ;  $V_c=15V$  and power MOSFET: SPA11N60.

First, the switching loss of the power MOSFET as function of the max drive current  $I_{gmax}$  is

$$P_{switching\_loss}/t \Big| \int_0^{T_{line}} f_s V_o (I_{L4pk} / \omega_L t) (T_{s4csd} / t) dt \quad (16)$$

Substituting (13), (14), (15) to (16) yields

$$P/I_{gmax} \Big| \frac{1}{2} f_s V_o I_{L4avg} \frac{\phi/Q_{pl} 4Q_{th} + Q_{gd}}{I_{gmax}} \quad (17)$$

Secondly, from (10), the total loss of CSD as function of the max drive current  $I_{gmax}$  is given as:

$$P_{CSD}/I_{gmax} \Big| P_{copper} \frac{I_{gmax}^2}{I_{g1max}} + P_{core} + P_{RG} \frac{I_{gmax}^2}{I_{g1max}} + P_{Gate} + P_{cond} \frac{I_{gmax}^2}{I_{g1max}} \quad (18)$$

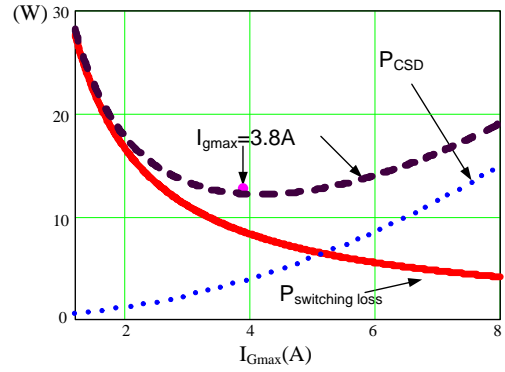


Fig. 18 Objective function  $P(I_{gmax})$  as function of the max current  $I_{gmax}$

Thirdly, in order to find the optimized gate drive current, the objective function is established adding the switching loss and the CS drive circuit loss together as:

$$P/I_{gmax} \Big| P_{scsd4mos}/I_{gmax} + P_{CSD}/I_{gmax} \quad (19)$$

Fig. 18 gives the optimal design curves. It is noted that the optimal gate drive current is 3.8A. Based on the selected gate drive current, the calculated CS inductor from (12)

is  $L_r \Big| \frac{V_{cc} V_{inmax}}{2f_s V_o I_{gmax}} \Big| 0.8uH$ , where  $V_{in}=110V$ ,  $f_s=1MHz$ ,  $V_o=380V$ ,  $P_o=300W$  and  $I_{gmax}=3.8A$ .

Fig. 19 illustrates the loss breakdown between the CSD and conventional driver based on the basis of the optimized CSD. When the input line voltage is 110V, the optimized CSD reduces the total loss of 14W, which translates into an efficiency improvement of 3.5% (from 89% to 92.6%).

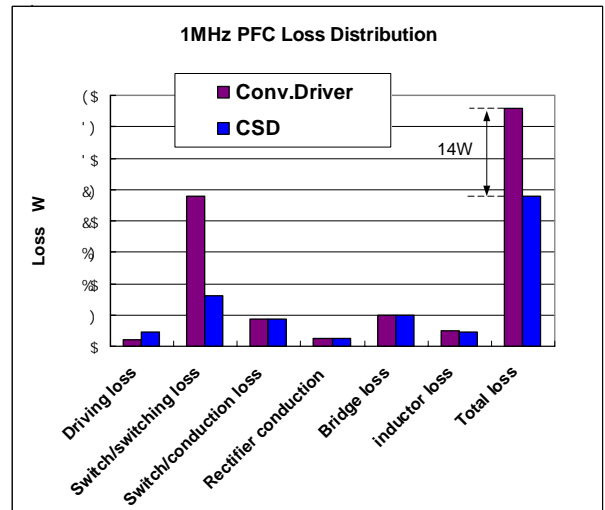


Fig. 19 1MHz PFC loss breakdown comparison based on the optimal design ( $V_{in}=110V$ ,  $V_o=380V$ ,  $V_c=15V$ ,  $P_o=300W$  and  $L_r=0.8uH$ )

## V. BENEFITS OF THE PROPOSED CSD FOR MHz PFC APPLICATIONS

### A. Adaptive Drive Current to Achieve Switching Loss Reduction

The proposed CSD can achieve fast switching speed and reduce the switching losses significantly due to strong drive capability of the current source. Normally, high drive currents lead to lower switching loss. Strong drive current is desired to reduce the switching loss further when the power MOSFET carries high current. Nevertheless, higher drive currents also result in higher circulating loss. However, the present CSD circuits normally use constant drive currents.

Therefore, the adaptive drive current would be able to improve the performance of the CSDs and help to achieve optimal design of the switching loss reduction and gate drive loss reduction. On the contrary, the adaptive current is inherent capability of the presented CSD for the PFC application. Furthermore, no additional control scheme and additional circuitry are needed to achieve this adaptive drive current.

### B. Gate Energy Recovery

The proposed adaptive CSD can also achieve the gate energy recovery of the gate capacitance of the MOSFET. The efficiency of gate energy recovery depends on the loss of the CSD circuit. Normally, high CSD current results in high circulating loss, but faster switching speed and lower switching loss. Because the CSD current varies with the current, the efficiency of the gate energy recovery changes with the operating condition. Moreover, the proposed solution only needs four drive switches and one small external inductor. Due to the complimentary control of the switches, the existing Buck drivers can be directly used and this will reduce the complexity of the control circuit significantly. This neat configuration and implementation will make the CSD technology more efficient in the practical applications.

### C. Size Reduction of the PFC Stage

Compared traditional 100kHz PFC converters, the 1MHz PFC with the adaptive CSD will lead to the 90% reduction of the inductor. Owing to the adaptive drive current of the proposed CSD solution, the switching loss and gate drive loss can be greatly reduced, which leads to the MHz operation of the PFC.

More importantly, the MHz PFC can also achieve great size reduction of the EMI filter. Therefore, with the adaptive CSD, the MHz PFC achieves much higher power density over the conventional solution.

## VI. SIMULATION AND EXPERIMENTAL RESULTS

To verify the proposed solution, an 110V input, 380V/300W output and 1MHz boost PFC converter with the CSD was simulated using the PSPICE software. The specifications are: boost inductor  $L=100\mu\text{H}$ ; output capacitance  $C=220\mu\text{F}$ ; the CSD inductor  $L_r=1\mu\text{H}$ ; the gate

driver voltage  $V_g=8\text{V}$ . A boost PFC prototype with the same specifications is been built.

### Boost Inductor Current

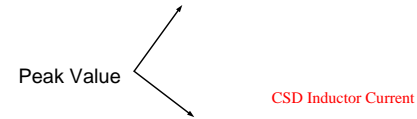


Fig. 20 Key waveforms of the boost PFC converter with the CSD solution

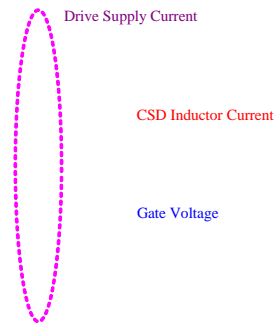


Fig. 21 Zoomed the drive supply current, CS current and gate voltage

Fig. 20 shows the boost inductor current and the CS inductor current. It is observed that the line current is the sinusoidal waveform, which is able to catch up with the input voltage. As the duty cycle changes with the input line voltage, the CS inductor current is able to change simultaneously with fast dynamic response. When the input current reaches its peak value as shown in the dotted area, which means the main MOSFET carries the peak current, the CS inductor current also reaches its peak value adaptively.

Fig. 21 illustrates the zoomed CS inductor current, gate drive voltage and drive supply current. The CS inductor current is a triangle waveform and the peak value varies with the duty cycle. Turn on and turn off transition is only about 20ns and this leads fast switching speed. Also when the gate voltage turns off as shown in the dotted area, the direction of the drive supply current switches, which means the gate energy is returned to the supply voltage rail.

## VII. CONCLUSION

In this paper, the CSD technique is investigated for MHz PFC applications. The proposed CSD solution for the boost PFC converter can achieve fast switching speed and gate energy recovery. These benefits help to improve the switching frequency of the boost PFC converter to MHz over the conventional several kHz PFC converters. This will lead to significantly reduction of the inductors and the size of the EMI filter. The simulation results verified the proposed solution. An 110V input, 380V output and 1MHz/ 300W boost PFC converter has been implemented. The initial test has begun and the experimental results will be reported soon.

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