Letters

A Soft-Switching Transformerless DC−DC Converter With Single-Input Bipolar Symmetric Outputs

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***Abstract*—In this letter, a soft-switching transformerless dc−dc converter with single-input bipolar symmetric outputs (SIBSO) is proposed, which has positive and negative outputs with equal voltage amplitude and can be used in audio amplifier, bipolar symmetric auxiliary power supply application, etc. Based on the proposed bipolar symmetric outputs cells, the SIBSO dc−dc converter only requires two switches forming a half bridge circuit, and zero voltage switching (ZVS) of the two switches can be achieved over full load range. In addition, common ground of input and outputs is realized, which means the floating driver and isolated sensors are not required in the proposed dc−dc converter. The controller and drivers can be powered up by using input power supply through a simple step-down circuit, which reduces not only the cost and volume but also the complexity of the converter. The operation modes and characteristic of the proposed SIBSO dc−dc converter are analyzed. Moreover, parameter design for ZVS operation is presented. Finally, a 60-W 1-MHz switching frequency prototype is built up by using GaN high electron mobility transistors (HEMTs). Experimental results shown that bipolar symmetric outputs are obtained with common ground of input and output, and peak efficiency of 95.8% and power density of 154 W/in^3 are achieved.**

***Index Terms*—Bipolar symmetric outputs, dc−dc converter, soft switching, transformerless.**

I. Introduction

Along with multioutput applications that attract much attention, single-input dual-output dc−dc converter is more and more popular because of the lower cost and smaller volume than that of the two single-output dc−dc converters [1] − [6]. In [1]−[4], single inductor dual-output dc−dc converter is presented by sharing one inductor in two conventional buck dc−dc converters, and two positive outputs are obtained. In [5] and [6], the dual-output dc−dc converters are proposed, and single-input bipolar symmetric output (SIBSO) is realized by setting the output ground as the central node between two output capacitors. Compared to single-input dual positive output dc−dc converter, SIBSO dc−dc converter is widely used in various power electronics applications, including audio amplifier, bipolar symmetric auxiliary power supply, ultrasound medical imaging systems, solar inverter systems, etc. [7]−[16].

As high efficiency and high power density are the development tendency of the SIBSO dc−dc converter, high switching frequency, soft-switching technique, simple topology, and controller become more and more important solutions to improve the performance of the SIBSO converter. However, there are few literatures about SIBSO converter, which achieve both high efficiency and high power density.

Flyback converter is usually used in isolated SIBSO dc−dc converter, and two transformer secondaries are needed to generate bipolar symmetric outputs. However, it is difficult to ensure that the bipolar output voltages are symmetric as the difference of transformer turns and cross-regulation. If the transformer is removed in nonisolated applications, the efficiency and power density can be improved. Furthermore, when the isolated sensors are removed, the cost of the converter can also be reduced. Therefore, transformerless SIBSO dc−dc converter has been developed rapidly in recent years [17]−[22].

In traditional transformerless SIBSO dc−dc converter, two independent nonisolated dc−dc converters are utilized to generate bipolar symmetric outputs, which require two controllers and increase the cost of the converter [17]. In the SIBSO dc−dc converters of [5], [6], [10], and [11], one controller and less switches are used, which reduces the cost and complexity. However, in these converters in which inputs and outputs have different grounds, isolated sensors and drivers are required for controller and floating switches. In contrast, for common-ground SIBSO dc−dc converter in [18]−[22], the isolated auxiliary power supplies are not required for drivers, sensors, and controllers. Thus, the common-ground SIBSO dc−dc converter plays an important role in bipolar bus applications.

In recent years, wide bandgap semiconductor devices such as GaN and SiC are used more and more widely. To achieve high power density and small volume, high switching frequency

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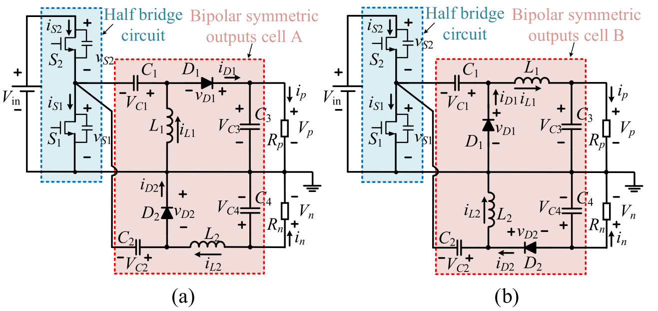


Fig. 1. Proposed soft-switching SIBSO dc–dc converter. (a) SIBSO dc-dc converter with bipolar symmetric outputs cell A. (b) SIBSO dc-dc converter with bipolar symmetric outputs cell B.

operation is a tendency in converters. Thus, the GaN-based or SiC-based soft-switching SIBSO dc–dc converter without snubbers not only increases the efficiency but also can improve the switching frequency and power density [23].

In [5]–[22], the efficiency of the SIBSO dc–dc converters is decreased as large switching loss caused by hard switching. In this letter, novel transformerless SIBSO dc–dc converters are proposed based on the bipolar symmetric output cells. In comparison with the traditional SIBSO dc–dc converter, we have the following.

1) Only two GaN high electron mobility transistors (HEMTs) with half bridge configuration are used.

2) The simple gate driver and auxiliary power supply circuit can be used to reduce the complexity.

3) Common ground of inputs and outputs is achieved.

4) Zero voltage switching (ZVS) of switches are realized over full load range.

Thus, high efficiency and high power density are achieved in the proposed SIBSO dc–dc converters.

The rest of this letter is organized as follows. Section II illustrates operation modes, steady-state characteristic, and the analysis of soft-switching condition. Section III gives the controller and prototype parameters design. Section IV shows the experimental results. Finally Section V concludes the letter.

II. Operation Modes and Characteristic of the Proposed SIBSO DC–DC Converter

A. Operation Modes

Fig. 1(a) shows the proposed SIBSO dc–dc converter, which consists of a half bridge circuit and the proposed bipolar symmetric output cell A. According to the duality principle, the proposed bipolar symmetric output cell A can also be re-formed as the bipolar symmetric output cell B, as shown in Fig. 1(b). As the operation principle of the SIBSO dc–dc converter in Fig. 1(b) is similar to that of the converter in Fig. 1(a), only the converter shown in Fig. 1(a) is analyzed in detail. In bipolar symmetric output cell A, the positive output cell consists of capacitor C_1, C_3, inductor L_1, and diode D_1, and the load R_p is connected to positive output capacitor C_3; the negative output cell consists of capacitor C_2, C_4, inductor L_2, and diode D_2, and

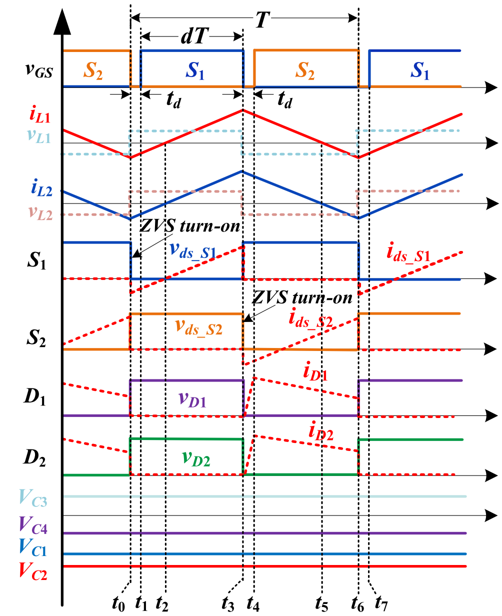


Fig. 2. Key waveforms of the SIBSO dc–dc converter in Fig. 1(a).

the load R_n is connected to negative output capacitor C_4. The reference polarities of voltages and currents are shown in Fig. 1.

The key waveforms of the proposed SIBSO dc–dc converter in Fig. 1(a) are shown in Fig. 2, where t_d is deadtime between the driving signal of switches S_1 and S_2. When the deadtime t_d is neglected, the driving signals of switches S_1 and S_2 are complementary. To simplify the analysis, the following assumptions are made: 1) the active switches are ideal except their output capacitances; 2) the diodes, inductors, and capacitors are ideal; and 3) the capacitances C_1–C_4 are large so that the voltages across them are constant. In steady state, the proposed SIBSO dc–dc converter has six operation modes, as shown in Fig. 3. The red lines represent active circuits, the gray lines represent nonactive circuits, and the real current polarities are shown in Fig. 3.

Mode 1 [t_0–t_1]: Mode 1 is deadtime mode. At time t_0, switch S_2 is turned OFF. As i_{L1} and i_{L2} are negative and can be regarded as constant during this mode, the flowing paths for the freewheeling of currents i_{L2} and i_{L1} are provided by switch S_1.

Mode 2 [t_1–t_2]: At time t_1, switch S_1 is turned ON. As the voltage $v_{ds,S1}$ is zero before turning ON, ZVS turn-ON of switch S_1 can be achieved. In this mode, the voltage across inductor L_1 is V_{C1}, the voltage across inductor L_2 is $V_{C2}-V_{C4}$, and currents i_{L1} and i_{L2} increase from negative to zero.

Mode 3 [t_2–t_3]: In this mode, currents i_{L1} and i_{L2} increase from zero to positive.

Mode 4 [t_3–t_4]: Mode 4 is deadtime mode. At time t_3, switch S_1 is turned OFF. As i_{L1} and i_{L2} are positive and can be regarded as constant during this mode, the flowing paths for the freewheeling of currents i_{L2} and i_{L1} are provided by switch S_2.

Mode 5 [t_4–t_5]: At time t_4, switch S_2 is turned ON. As the voltage $v_{ds,S2}$ is zero before turning ON, ZVS turn-ON of switch

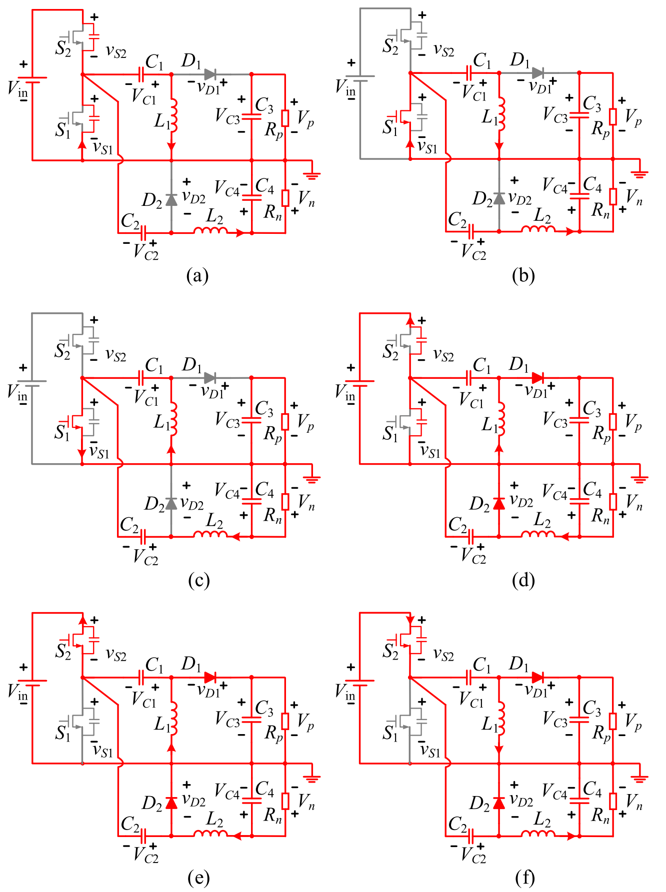


Fig. 3. Operation mode. (a) Mode 1 (t0∼t1). (b) Mode 2 (t1∼t2). (c) Mode 3 (t2∼t3). (d) Mode 4 (t3∼t4).(e) Mode 5 (t4∼t5). (f) Mode 6 (t5∼t6).

S_2 can be achieved. In this mode, the voltage across inductor L_1 is V_{C3}, the voltage across inductor L_2 is$-V_{C4}$, and currents i_{L1} and i_{L2} decrease from positive to zero.

Mode 6 [t_5−t_6]: In this mode, currents i_{L1} and i_{L2} decrease from zero to negative.

B. Voltage Gain and Stress Analysis

As the deadtime is much shorter than the time interval in modes 2, 3, 5, and 6, modes 1 and 4 are neglected. In steady state, volt-second balance of L_1 gives

$$(V_{in} + V_{C1})(1 - d)T + V_{C1}dT = 0. \tag{1}$$

Thus, the voltage across capacitor C_1 is

$$V_{C1} = (d - 1)V_{\text{in}}. \tag{2}$$

Volt-second balance of L_2 gives

$$(V_{C2} - V_{C4})dT - V_{C4}(1 - d)T{=}0. \tag{3}$$

Thus, the voltages across capacitors C_2 and C_4 satisfy

$$V_{C2}d{=}V_{C4}. \tag{4}$$

In modes 5 and 6, when switch S_2 is turned ON, the voltages across capacitors C_1 and C_3 satisfy

$$V_{\text{in}} + V_{C1} = V_{C3} \tag{5}$$

$$V_{C2} + V_{C3} = V_{C1}. \tag{6}$$

From (2), (4)−(6), and modes 2 and 5, the voltages across capacitors C_2, C_3, and C_4 and the voltage stress of diodes and switches can be obtained as

$$\begin{cases} V_{C2} = -V_{\text{in}}, \;\; V_{S1} = V_{\text{in}}, \;\; V_{S2} = V_{\text{in}} \\ V_{C3} = dV_{\text{in}}, \;\; V_{D1} = V_{C3} - V_{C1} = V_{\text{in}} \\ V_{C4} = -dV_{\text{in}}, \;\; V_{D2} = -V_{C2} = V_{\text{in}}. \end{cases} \tag{7}$$

From (2) and (7), the voltages of V_{C1} and V_{C2} in terms of input voltage satisfy

$$G_{C1} = \frac{V_{C1}}{V_{\text{in}}} = d - 1 \text{ and } G_{C2} = \frac{V_{C2}}{V_{\text{in}}} = -1. \tag{8}$$

From (7), the gains of the SIBSO dc−dc converter are

$$G_p = \frac{V_p}{V_{\text{in}}} = \frac{V_{C3}}{V_{\text{in}}} = d \text{ and } G_n = \frac{V_n}{V_{\text{in}}} = \frac{V_{C4}}{V_{\text{in}}} = -d. \tag{9}$$

As shown in (9), it can be known that $|G_p| = |G_n|$; thus, bipolar symmetric outputs are obtained.

C. Analysis of Soft Switching

To ensure ZVS turn-ON of switch S_1 and S_2 in modes 1 and 4, the charge stored in output capacitor of switch should be discharged fully by inductors currents so that $v_{ds,S1}$ and $v_{ds,S2}$ are zero before turning ON. Thus, the following should be satisfied:

$$-[i_{L1,\min} + i_{L2,\min}] \cdot t_d > V_{\text{in}} \cdot C_{\text{oss},s_1} + V_{\text{in}} \cdot C_{\text{oss},s_2} \tag{10}$$

$$[i_{L1,\max} + i_{L2,\max}] \cdot t_d > V_{\text{in}} \cdot C_{\text{oss},s_1} + V_{\text{in}} \cdot C_{\text{oss},s_2}. \tag{11}$$

where $C_{\text{oss},S1}$ and $C_{\text{oss},S2}$ are the output capacitances of switches S_1 and S_2, respectively.

According to ampere-second balance of capacitor C_4, average current I_{C4} is zero in one switching period. Thus, average currents I_{L2} satisfies

$$I_{L2} = \frac{-V_n}{R_n} = \frac{dV_{\text{in}}}{R_n}. \tag{12}$$

According to ampere-second balance of capacitors C_1 and C_3, average currents I_{C1} and I_{C3} are zero in one switching period. Thus, average current I_{L1} satisfies

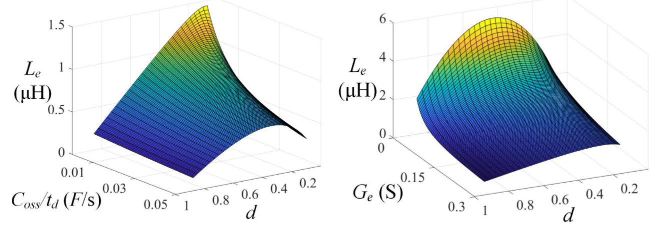
$$I_{L1} = I_{D2} = \frac{V_p}{R_p} = \frac{dV_{\text{in}}}{R_p}. \tag{13}$$

The minimum and maximum currents flowing through inductors L_1 and L_2 are

$$i_{L_1,\min} = I_{L_1} - \frac{-V_{C1}}{2L_1}dT = \frac{dV_{\text{in}}}{R_p} - \frac{V_{\text{in}}(1-d)}{2L_1}dT. \tag{14}$$

$$i_{L_2,\min} = I_{L_2} - \frac{V_{C4} - V_{C2}}{2L_2}dT = \frac{dV_{\text{in}}}{R_n} - \frac{V_{\text{in}}(1-d)}{2L_2}dT. \tag{15}$$

As average current I_{L1} and I_{L2} are positive, $i_{L1,\max}$ is larger than ($-i_{L1,\min}$), and $i_{L2,\max}$ is larger than ($-i_{L2,\min}$), ZVS condition of switch S_1 is more difficult than ZVS condition of switch S_2. If ZVS turn-ON of switch S_1 can be realized,



(a) (b)

Fig. 4. ZVS turn-ON boundary of switch $S1$ in the SIBSO dc−dc converter. (a) ZVS turn-ON boundary against Le, C_{oss}/td and d. (b) ZVS turn-ON boundary against Le, d and Ge.

ZVS turn-ON of switch S_2 can also be realized. Thus, only ZVS condition of switch S_1 is investigated.

Substituting (14) and (15) to (10), ZVS of switch S_1 can be achieved when

$$\left(\frac{1}{L_1}+\frac{1}{L_2}\right) > \frac{\frac{4C_{\text{oss}}}{t_d}+2d\left(\frac{1}{R_n}+\frac{1}{R_p}\right)}{(1-d)dT}. \tag{16}$$

In order to simplify (16), defining that $L_e = L_1L_2/(L_1 + L_2)$ represents equivalent inductance of inductor L_1 in parallel with L_2, and $G_e = 1/R_p + 1/R_n$ represents the sum of the admittance of the positive and negative outputs loads. Therefore, (16) can be rewritten as

$$L_e < \frac{(1-d)dT}{\frac{4C_{\text{oss}}}{t_d}+2dG_e}. \tag{17}$$

According to (17), Fig. 4 shows ZVS turn-ON boundary of switch S_1 in the proposed SIBSO dc−dc converter. When $1/R_n + 1/R_p = 4/15$ S, ZVS turn-ON boundary against L_e, C_{oss}/t_d and d is shown in Fig. 4(a). When $C_{\text{oss}}/t_d = 0.009$ F/s, ZVS turn-ON boundary against L_e, d, and G_e is shown in Fig. 4(b). If the converter operates below the surface in Fig. 4, ZVS turn-ON of switches S_1 and S_2 can be achieved.

III. Controller and Prototype Design of the Proposed SIBSO DC−DC Converter

A. Controller Design

From (9), the bipolar symmetric output voltage gains can be achieved with the assumption that all the devices are ideal. To further improve the symmetry of bipolar output voltages when the parasitic parameters and unbalanced loads are considered, both positive and negative output voltages are fed back and controlled in the proposed SIBSO dc−dc converter.

The block diagram of control loop of the proposed SIBSO dc−dc converter is shown in Fig. 5. As output voltage v_p is positive and output voltage v_n is negative, the value of $(v_p - v_n)$ is equal to $(|v_p| + |v_n|)$. Therefore, the output voltage v_p minus the output voltage v_n, i.e., $(v_p - v_n)$ is selected as feedback variable. Microcontroller TMS320F280049 is used to perform the control strategy in this letter.

From Fig. 5, the positive and negative outputs voltages are detected and scaled down by using resistor divider. The information of $(v_{C3} - v_{C4})$ is fed back to MCU ADC module, and conventional PI control strategy is implemented. Then, the pulsewidth modulation driver signals of switches S_1 and S_2 are generated.

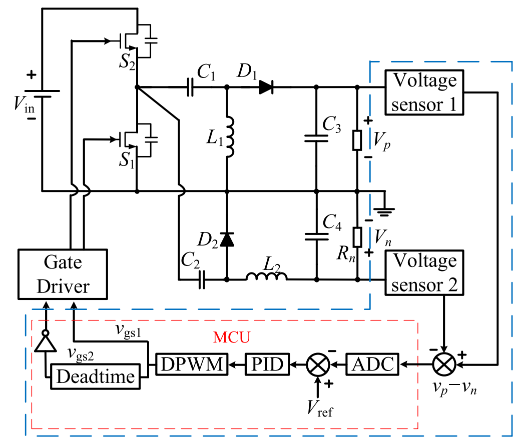


Fig. 5. Control loop of the proposed SIBSO dc−dc converter.

B. Parameter Design of the Prototype

To verify the analysis of the proposed SIBSO dc−dc converter, a 60-W prototype of the converter in Fig. 1(a) is implemented. In the proposed prototype, input voltage range is 20−50 V, and output voltage is ±15 V.

Take the nominal input voltage 48 V as an example. If the maximum positive and negative output powers are both 30 W, the G_e is changing from 0 to 0.27 which represents no load to full load. According to (17), if ZVS turn-ON of S_1 can be achieved at $G_e = 0.27$, ZVS turn-ON of S_1 will always be achieved when G_e is less than 0.27. Therefore, ZVS turn-ON of S_1 and S_2 can be achieved over full load range by designing the inductances L_1 and L_2.

Assuming that the prototype operates at 1 MHz switching frequency with 30-ns deadtime, ±15-V bipolar symmetric outputs are obtained, D_1 and D_2 are selected to SBRT4U60LP with its voltage rating of 60 V, and GaN HEMTs S_1 and S_2 are selected to LMG5200 with voltage rating of 80 V; thus, $T = 1\ \mu$s, $d = 15/48 = 0.31$, $t_d = 30$ ns, $C_{\text{oss}} = 266$ pF, and $G_e = 0.27$. From (17), L_e should satisfy

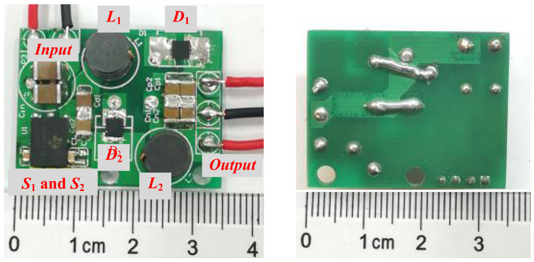
$$\begin{aligned} L_e &< \frac{(1-0.31)\times 0.31\times 10^{-6}}{4\times 266\times 10^{-12}\div 30\div 10^{-9}+2\times 0.31\times 0.27} \\ &= 1.06\ \mu\text{H}. \end{aligned} \tag{18}$$

As $L_e = L_1L_2/(L_1 + L_2)$, if L_1 and L_2 have the same inductances, the inductance of L_1 and L_2 should be smaller than 2.12 μH. Therefore, 2-μH inductors L_1 and L_2 are selected in the proposed prototype.

From [5], assuming the maximum voltage ripple content is 2%, the minimum required values of capacitance is

$$C_{\min} = \frac{P_{\max}T}{2V\times 2}. \tag{19}$$

Thus, capacitances of C_1, C_2 and input capacitor C_{in} are selected with 10 μF, and capacitances of C_3 and C_4 are selected with 20 μF according to (19).

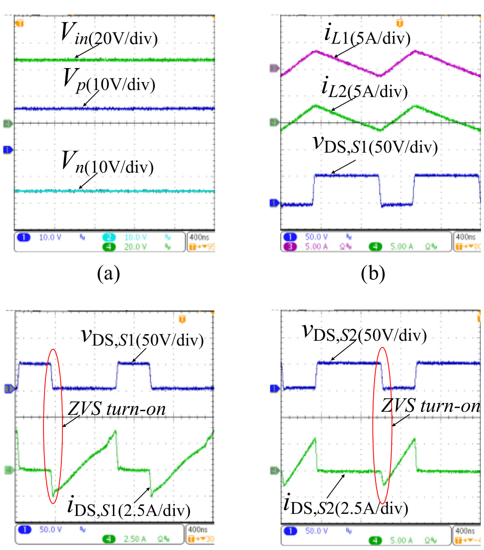


(a) (b)

Fig. 6. Prototype of the proposed SIBSO dc–dc converter. (a) Top. (b) Bottom.

TABLE I
KEY DESIGN SPECIFICATIONS OF THE PROTOTYPE

Input voltage V_{in}	20V~50V (nominal 48V)
Output voltage V_o	±15V
Rated output power	60W (30W positive output and 30W negative output)
Inductors L_1 and L_2	2μH
Capacitors C_1, C_2 and C_{in}	10μF (63V voltage rating)
Capacitors C_3 and C_4	20μF (63V voltage rating)
Switching frequency f_s	1MHz
Deadtime t_d	30ns
GaN switches S_1 and S_2	LMG5200 (integrated with driver)
Diodes D_1 and D_2	SBRT4U60LP

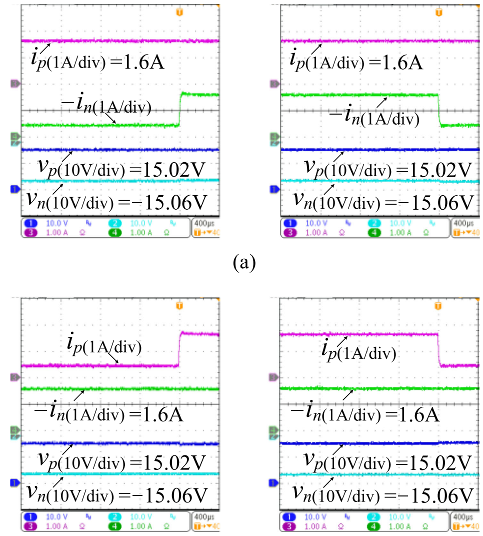


(a) (b) (c) (d)

Fig. 7. Key waveforms of the proposed SIBSO dc–dc converter. (a) waveforms of input and bipolar i_{L1},output voltages v_{in}, v_p and v_n. (b) waveforms of inductors currents i_{L2} and the voltage v_{DS} of S_1. (c) waveforms of v_{DS} and i_{DS} of S_1. (d) waveforms of v_{DS} and i_{DS} of S_2.

IV. Experimental Results

Fig. 6 shows the prototype of the proposed SIBSO dc–dc converter. The proposed SIBSO dc–dc converter has ±15-V outputs and 60-W rated load power, and the volume is L:2.9 cm, W:2.2 cm, H:1.0 cm and the power density of the main circuit is 154 W/in^3. The key design specifications are given in Table I.



(a)

(b)

Fig. 8. Dynamic performance of the proposed SIBSO dc–dc converter. (a) Step negative output load current increase from 0.5 to 1.6 A and decrease from 1.6 to 0.5 A when positive output load current is 1.6 A. (b) Step positive output load current increase from 0.5 to 1.6 A and decrease from 1.6 to 0.5 A when negative output load current is 1.6 A.

TABLE II
LOSS ANALYSIS OF THE PROTOTYPE AT FULL LOAD

P_{S1}	P_{con}	$I_{S1,rms}{}^2 R_{ds(on)}$	0.11W
	P_{off}	$\frac{1}{2} t_f V_{in} (\lvert i_{L1,\max} + i_{L2,\max} \rvert) f_s$	0.33W
P_{S2}	P_{con}	$I_{S2,rms}{}^2 R_{ds(on)}$	0.04W
	P_{off}	$\frac{1}{2} t_f V_{in} (\lvert i_{L1,\min} + i_{L2,\min} \rvert) f_s$	0.09W
P_{D1}		$V_F I_{D1}$	0.59W
P_{D2}		$V_F I_{D2}$	0.59W
P_{L1}	P_{cupper}	$I_{L1,RMS}{}^2 R_{ac,L1}$	0.19W
	P_{core}	$P_v V$	0.43W
P_{L2}	P_{cupper}	$I_{L2,RMS}{}^2 R_{ac,L2}$	0.19W
	P_{core}	$P_v V$	0.43W
$P_{C1}+P_{C2}+P_{C3}+P_{C4}$		$I_{C1,rms}{}^2 R_{ESR,C1} + I_{C2,rms}{}^2 R_{ESR,C2} + I_{C3,rms}{}^2 R_{ESR,C3} + I_{C4,rms}{}^2 R_{ESR,C4}$	0.06W
Total			3.05W

Fig. 7(a) shows the waveforms of input and bipolar output voltages v_{in}, v_p, and v_n, and Fig. 7(b) shows the waveforms of inductor currents i_{L1}, i_{L2} and the voltage v_{DS} of S_1. Fig. 7(c) and (d) shows the waveforms of v_{DS} and i_{DS} of switches S_1 and S_2. From Fig. 7(c) and (d), ZVS turn-ON can be achieved for switches S_1 and S_2. Fig. 8 shows the output voltages and the dynamic performance of the proposed SIBSO dc–dc converter when input voltage is 48 V and output voltages are $V_p = 15.02$ V and $V_n = -15.06$ V. The positive and negative outputs are stable and symmetric when load current step-up or step-down.

Table II presents the loss calculation of the proposed SIBSO dc–dc converter at 60-W full load when input voltage is 48 V and output voltage is ±15 V.

TABLE III
COMPARISON BETWEEN THE PROPOSED SIBSO DC–DC CONVERTER AND THE REFERENCES

References	[5]	[6]	[10]	[11]	[12]	[16]	[20]	This work
Switch	3	4	4	4	1	1	1	2
Diode	0	0	0	0	2	2	2	2
Inductor	2	3	1	2	4	3	4	2
Capacitor	3	3	2	2	5	5	4	4
Input / Output	48V / ±5V	27V / ±24V	1.5V / ±2.5V	120V / ±300V	24V~48V / ±40V	25V~55V / ±350V	96V / ±200V	20V~50V / ±15V
Switching frequency	100kHz	30kHz	2.5MHz	30,50,70kHz	100kHz	20kHz	30kHz	1MHz
Soft switching	No	No	No	No	No	No	No	Yes
Common ground of input and outputs	No	No	No	No	Yes	Yes	Yes	Yes
Voltage Gain	-	$\pm\frac{d_1}{1-d_1}$	$\pm\frac{1}{1-d}$	$\pm\frac{2}{1-d}$	$\pm\frac{d}{1-d}$	$\pm\frac{2+n}{1-d}$	$\pm\frac{d}{1-d}$	$\pm d$
Voltage stress of switch	$V_{in}-V_2$	$\frac{V_{in}}{1-d_1}$	$\frac{V_{in}}{1-d}$	$\frac{2V_{in}}{1-d}$	$\frac{dV_{in}}{1-d}$	$\frac{V_{in}}{1-d}$	$\frac{dV_{in}}{1-d}$	V_{in}
Floating driver	Yes	Yes	Yes	Yes	No	No	No	No
Power density	6.5W/in^3	7.4W/in^3	256W/in^3	27.3W/in^3	-	7.6W/in^3	10.5W/in^3	154W/in^3
Output power	100W	200W	0.225W	2kW	600W	150W	450W	60W
Peak Efficiency	95%	96.1%	83.4%	98.5%	92.7%	96.2%	88.1%	95.8%
Full load efficiency	94%	92%	77%	94%	87.0%	94.6%	85.3%	94.6%

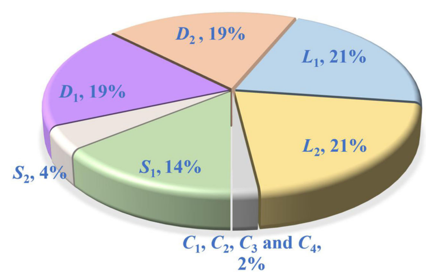
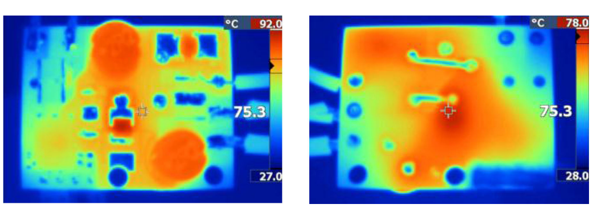


Fig. 9. Loss breakdown of the SIBSO dc–dc converter at full load.



(a) (b)

Fig. 10. Thermal images of the proposed SIBSO dc–dc converter at full load (no thermal compound, heatsink, or fan). (a) Top. (b) Bottom.

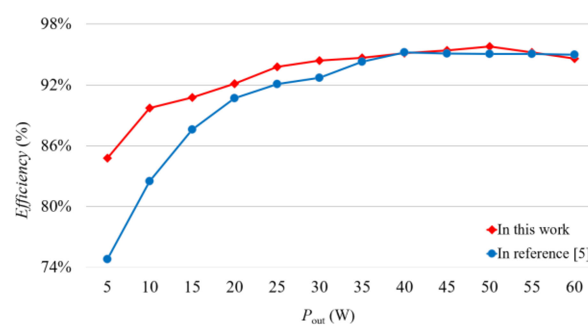


Fig. 11. Measured efficiency.

Fig. 9 shows the loss breakdown of the prototype at full load. The loss of diodes D_1 and D_2 occupies 38% of the total loss. If the diodes are replaced by the active switches, the efficiency of the proposed converter will be further increased.

Thermal images of the proposed SIBSO dc–dc converter at full load without thermal compound, heatsink, or fan is shown in Fig. 10. The temperature of the diode D_2 is 92 °C, and the temperature of the other devices is below 85 °C. From Fig. 9, it can be seen that the loss of diodes D_1 and D_2 is high; thus, the temperature of diodes is high as shown in Fig. 10, which is consistent with the theoretical analysis.

Fig. 11 shows the measured efficiency comparison between the proposed SIBSO dc–dc converter and the work [5] at 48-V input voltage. As the power consumption of auxiliary power supply is less than 140 mW, only main power is considered for the measured efficiency. It can be observed that the highest efficiency is 95.8% at 50-W load, and the full load efficiency is 94.6% in this letter. Although the proposed SIBSO dc–dc converter operates at 1-MHz switching frequency, the efficiency of the proposed prototype is still higher than that in [5] with 100-kHz switching frequency.

Table III gives the comparison between the proposed and the others SIBSO dc-dc converters. In the proposed prototype with 1 MHz switching frequency, only two switches are required and ZVS turn-ON can be achieved. Thus, 154 W/in^3 power density and 94.6% full load efficiency are achieved. Common-ground of input and bipolar symmetric outputs is also achieved in the proposed converter. Therefore, floating driver is not required for the two switches, which reduces the complexity and cost.

V. CONCLUSION

A soft-switching transformerless SIBSO dc–dc converter is proposed in this letter based on symmetric bipolar outputs cell, which only need two switches, two diodes, and two inductors. ZVS turn-ON of two switches can be achieved over full load range. As input and bipolar outputs have common ground in the proposed SIBSO dc–dc converter, common-ground driver can be used instead of using floating driver, which simplifies the driver circuit and reduces the cost. Two GaN HEMTs are used in the proposed SIBSO dc−dc converter and switching frequency is set to 1 MHz. 95.8% peak efficiency, 94.6% full load efficiency, and 154 W/in^3 power density are obtained. Therefore, the proposed SIBSO dc−dc converter is suitable for the applications that need highly symmetric bipolar bus voltages, such as audio amplifier, bipolar symmetric auxiliary power supply, ultrasound medical imaging systems, bipolar dc microgrid, etc.

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