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A New Dual Channel Resonant Gate Drive Circuit for Synchronous Rectifier

Presented By:

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Presentation Overview

1. *Introduction*
   1. *Why you should use resonant gate drive*
   2. *Drawbacks of existing techniques*
2. Proposed Resonant Gate Driver and Operation
3. Loss Analysis
4. Simulation and Experimental Results
5. Conclusions

1. Introduction

- **Application:** low voltage high current DC-DC power supplies
- Trend to increase switching frequency for improvements in:
  + power density
  + dynamic performance
- Drawbacks of increased switching frequency:
  - gate loss
  - switching loss
  - body diode conduction

Important for SRs in MHz range

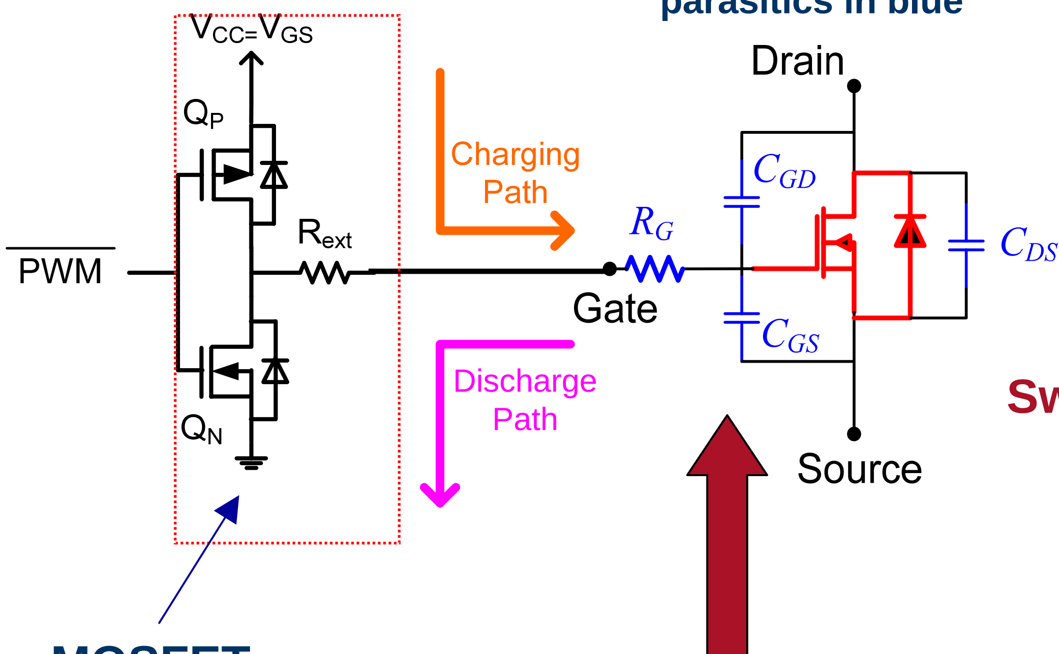
Conventional MOSFET Driver

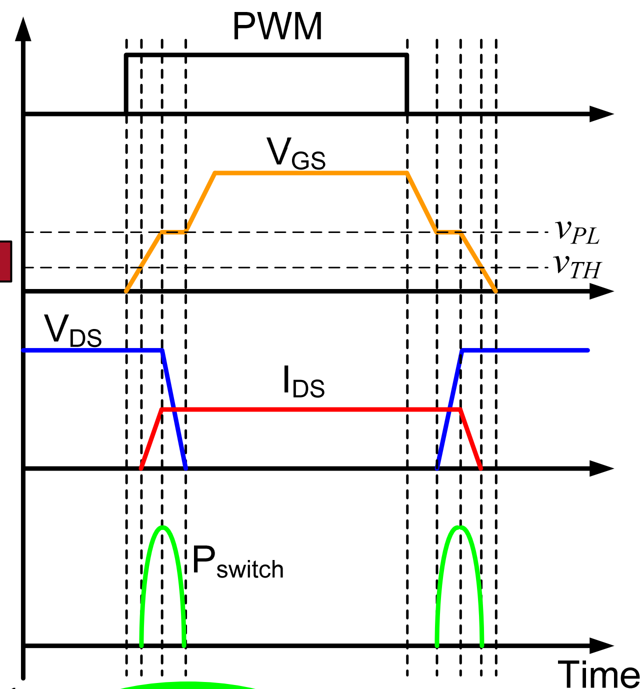
MOSFET Driver

Power MOSFET

parasitics in blue

Hard Switching Waveforms





Switching Loss

MOSFET, or BJT switches

Gate Loss

$$P_{gate} = Q_g V_{GS} f_S$$

$$P_{switch} = \frac{1}{2}(t_{rise} + t_{fall}) V_{DS} I_{DS} f_S$$

$$P_{out} = \frac{1}{2} C_{DS} V_{DS}^2 f_S$$

Techniques for Improvement

Gate Loss Savings

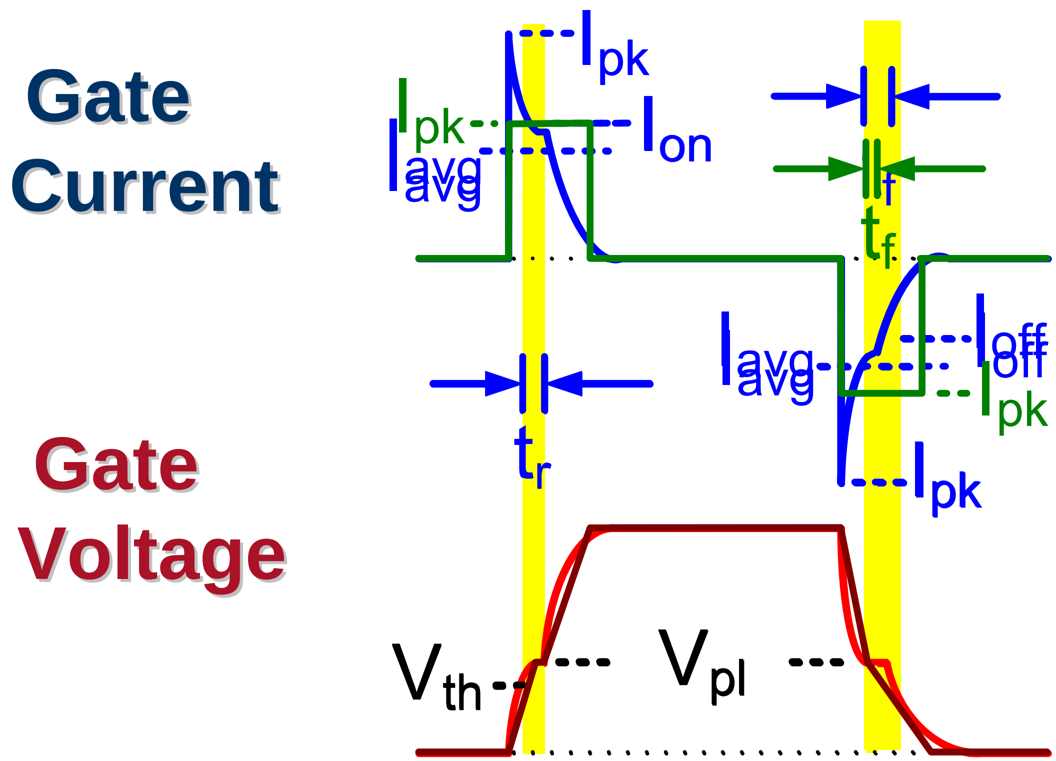
Resonant Gate Drive Techniques

+ Many good (~15) circuits proposed since early 1990s, but generally unused

- Existing methods emphasize gate energy savings, but ignore potential increase in switching speed

CURRENT SOURCE DRIVERS CAN REDUCE SWITCHING LOSS OR BODY DIODE CONDUCTION!

Conventional vs. Resonant Drive
Switching Loss and Body Diode Savings



Voltage source
RC-type charging
limits speed

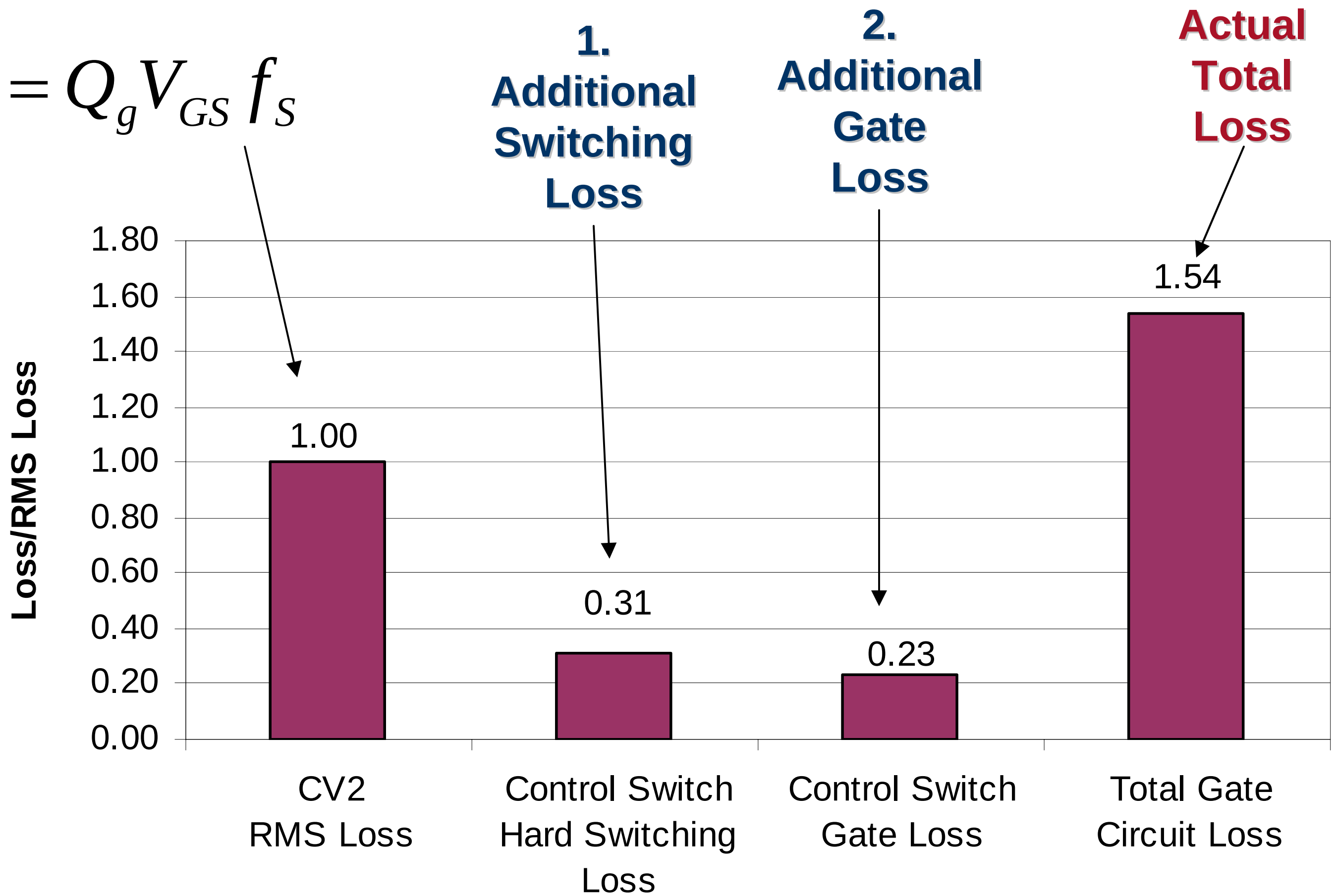
Constant current source
type charging
improves speed!

Additional Conventional Driver Loss

Actual driver loss can be much higher than CV² loss…

e.g. varies by driver, but typically 15-50%

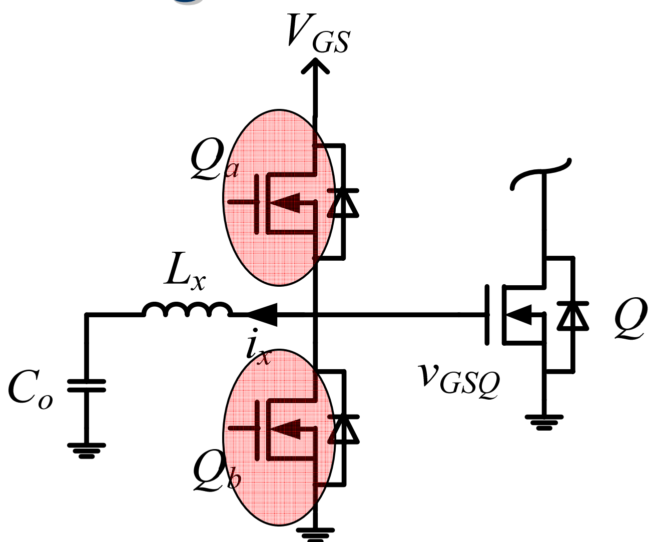
$$P_{gate} = Q_g V_{GS} f_S$$

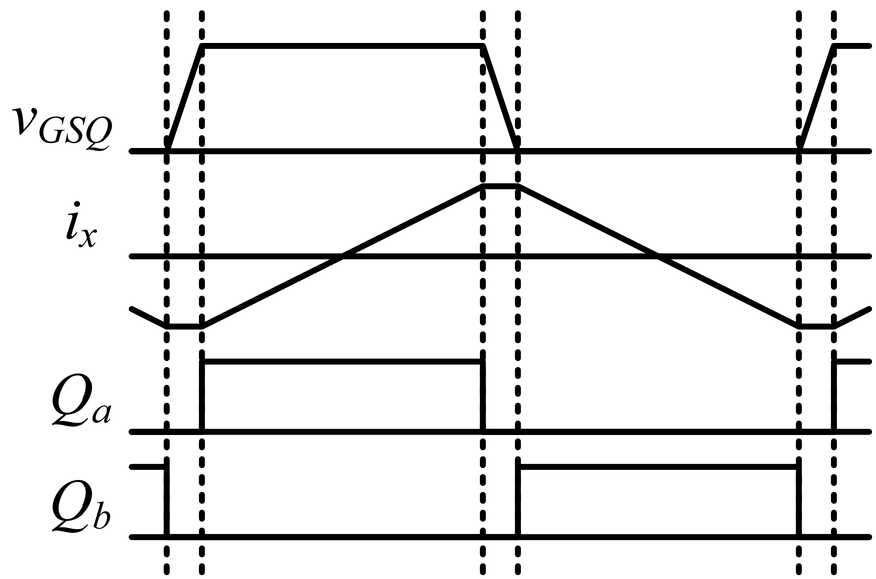


Resonant Gate Drive Review

Existing techniques suffer from several problems:

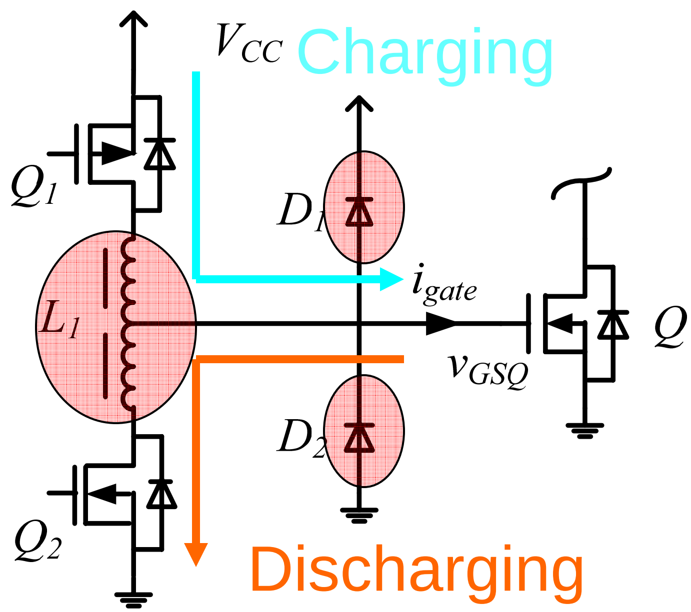
1. **Slow dynamic response (large Co)**
2. **Single MOSFET drive**

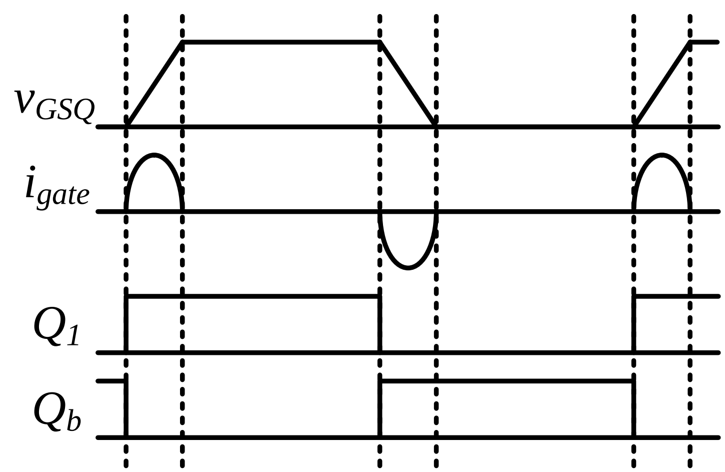




Resonant Gate Drive Review

3. **Bulky transformer, or coupled inductor**
4. **Slow turn-on and/or turn-off**
5. **Gate not actively clamped high and/or low, so false triggering (Cdv/dt) can result**





Presentation Overview

1. Introduction
2. *Proposed Resonant Gate Driver and Operation*
    1. *Circuit and Waveforms*
3. Loss Analysis
4. Simulation and Experimental Results
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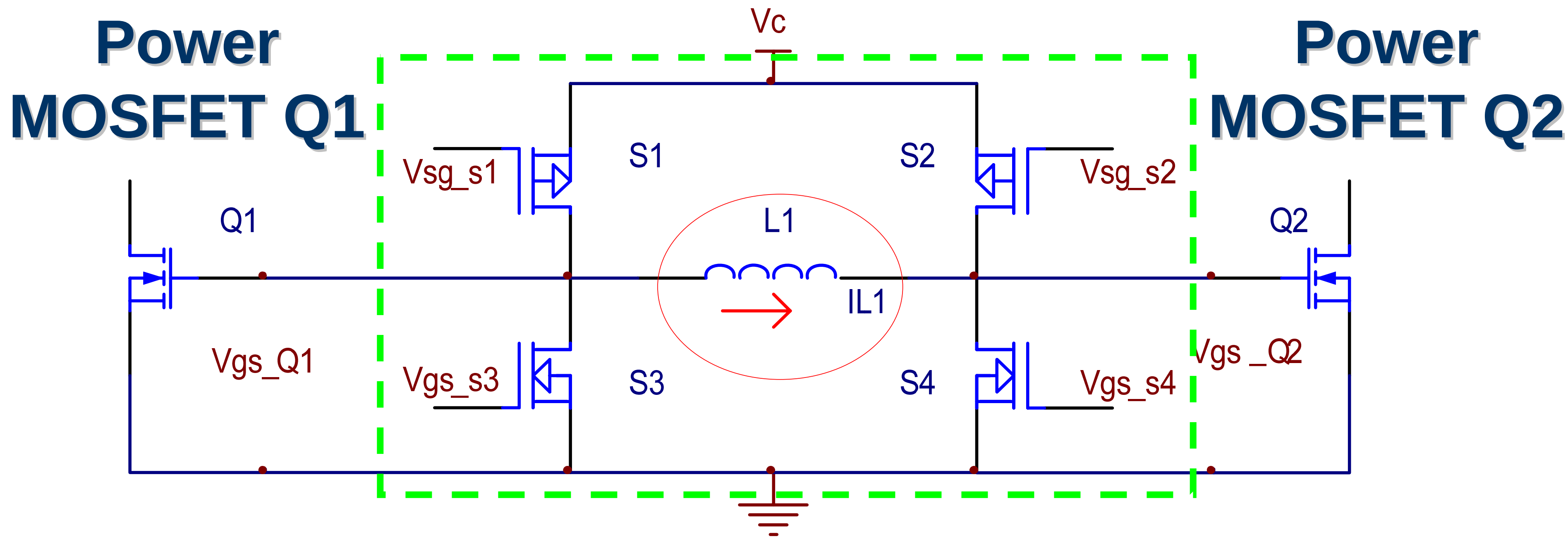
Proposed Resonant Driver

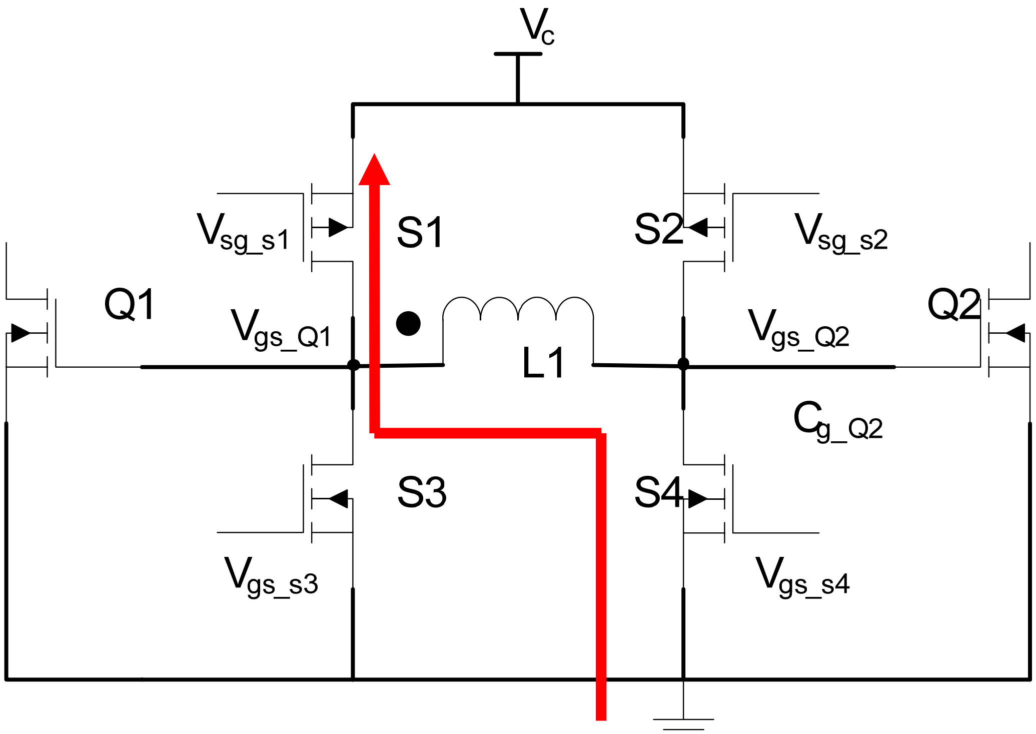


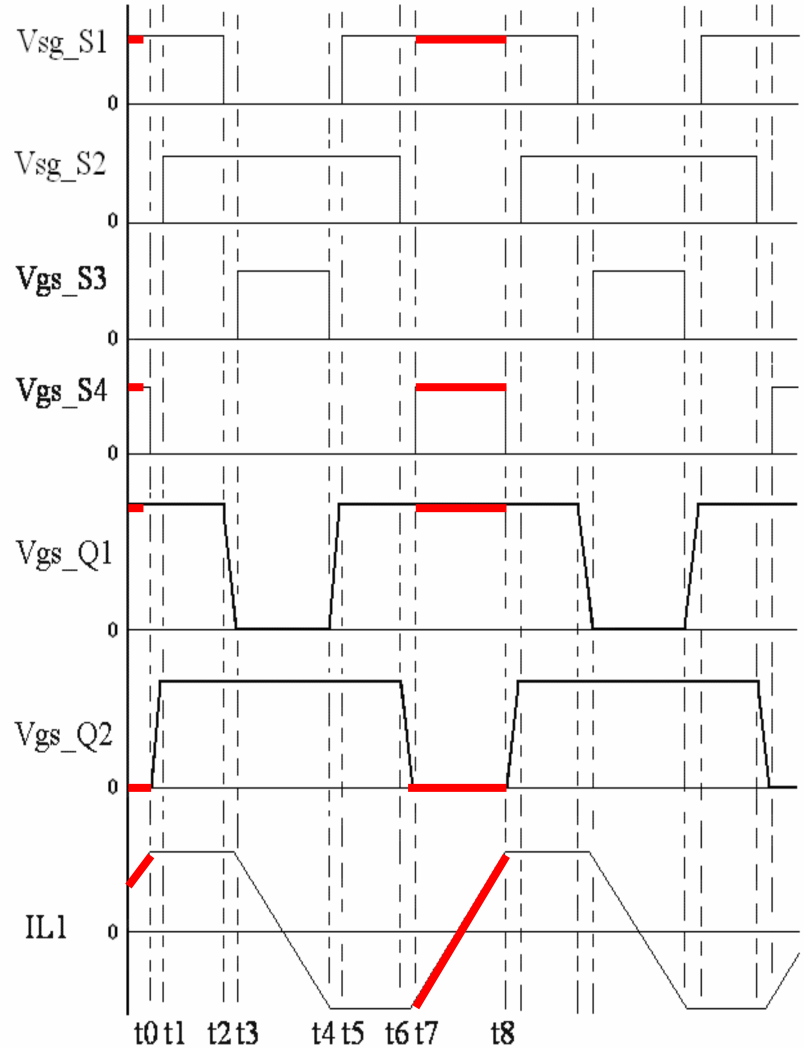
Applications:

1. Synchronous rectifiers in isolated DC-DC
2. Push-pull primary switches
3. Interleaved low-side converters (e.g. Boost)

Principles of Operation

Mode 1 (t < t0 and t7 < t < t8)

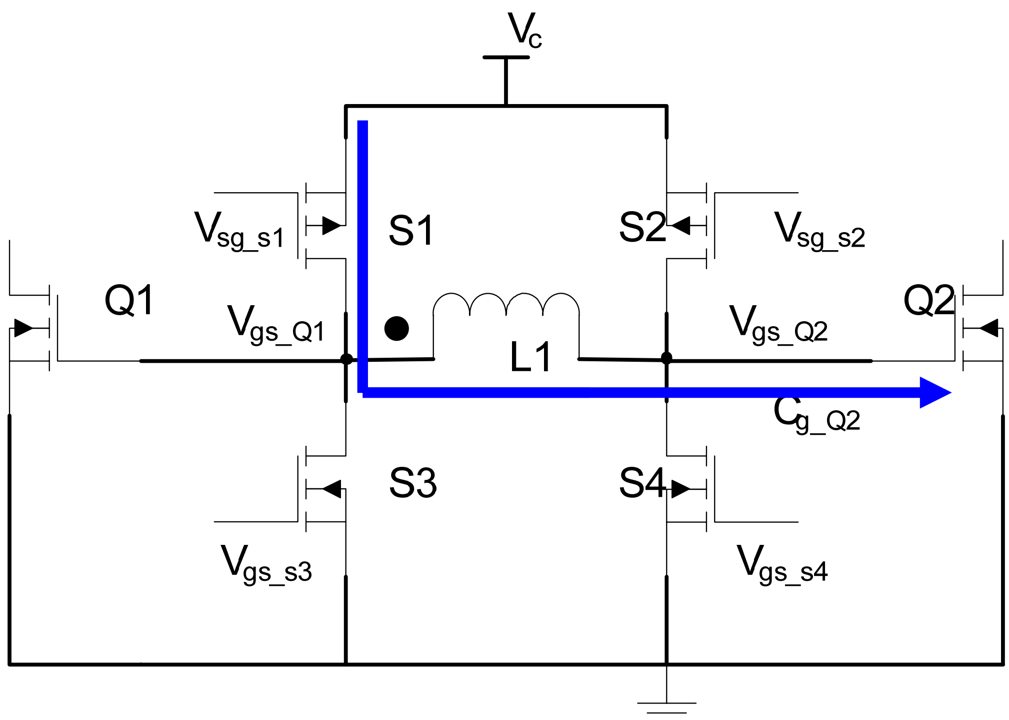


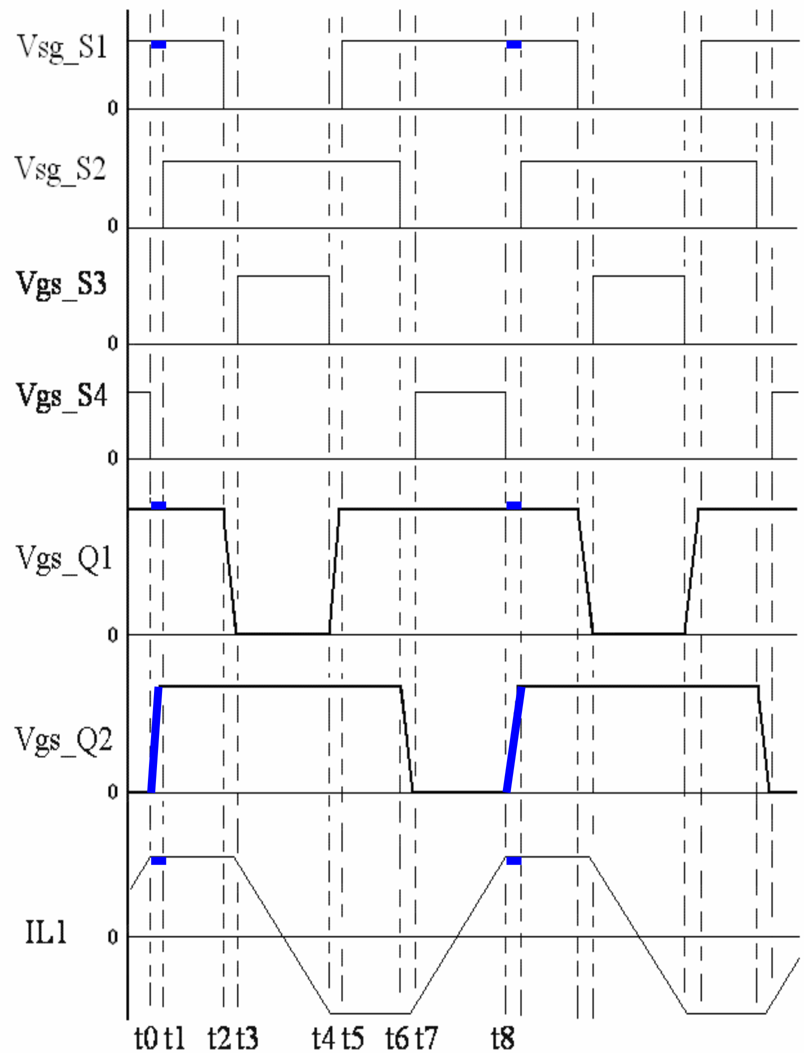


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 2 (t0 < t < t1)

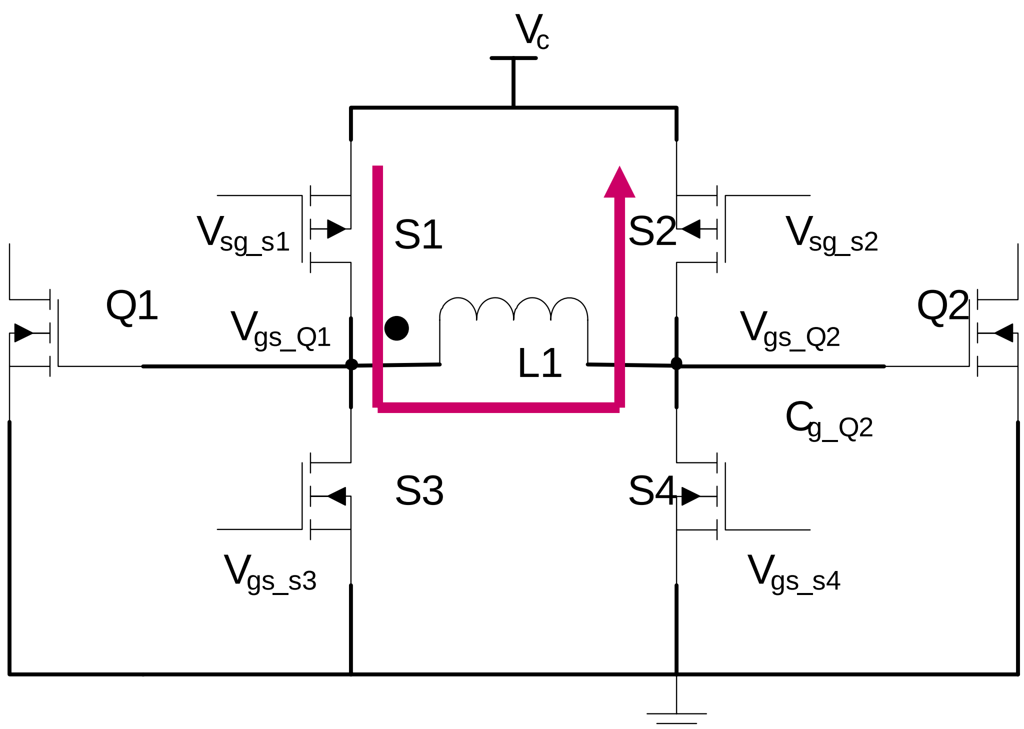


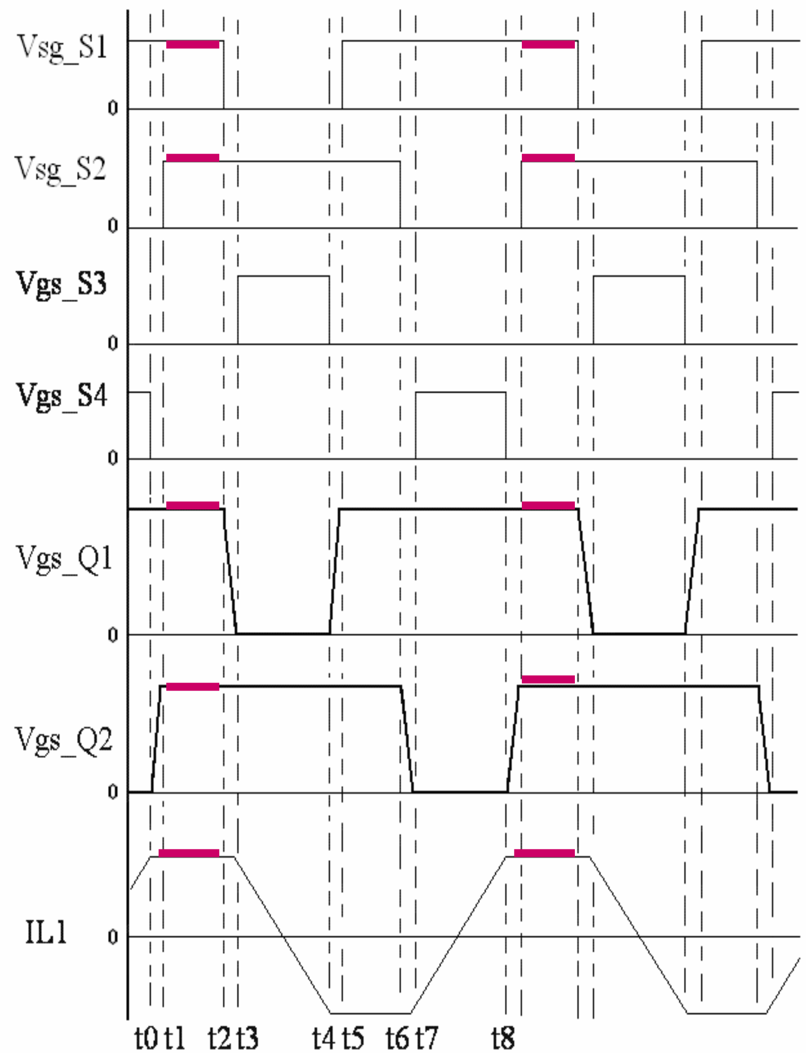


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 3 (t1 < t < t2)

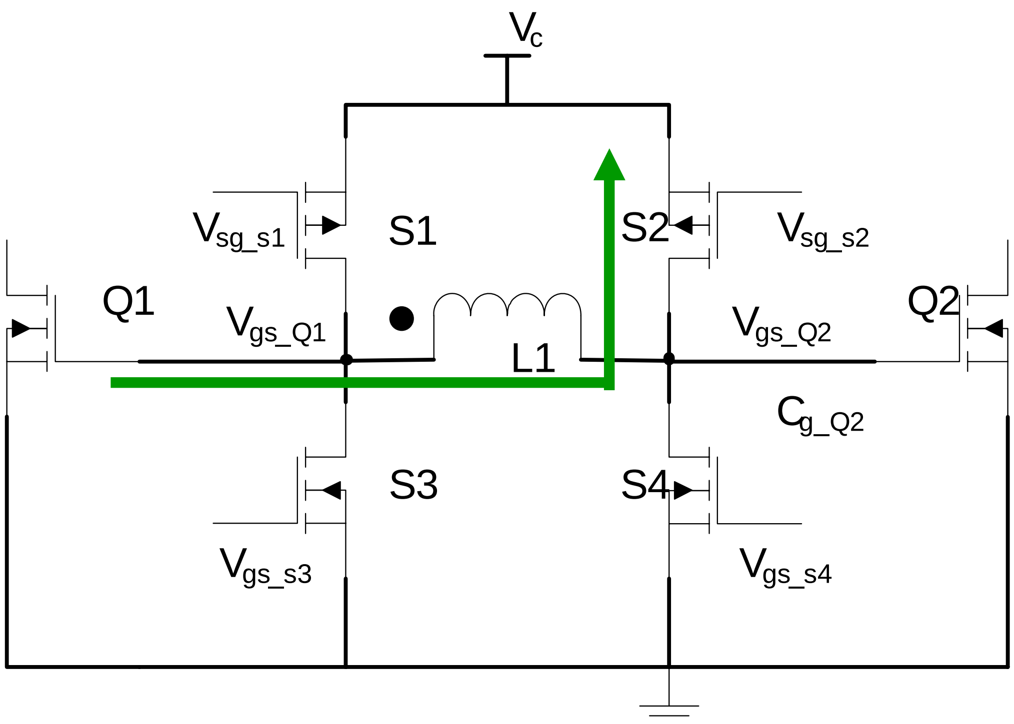


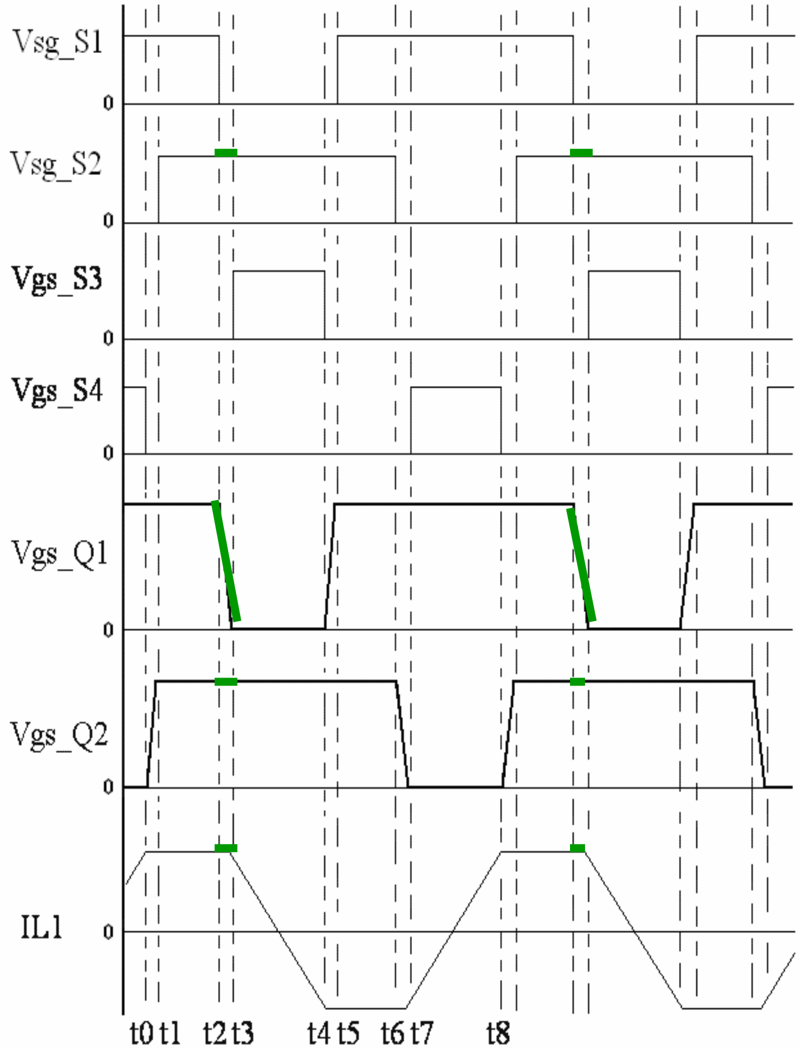


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 4 (t2 < t <t3)

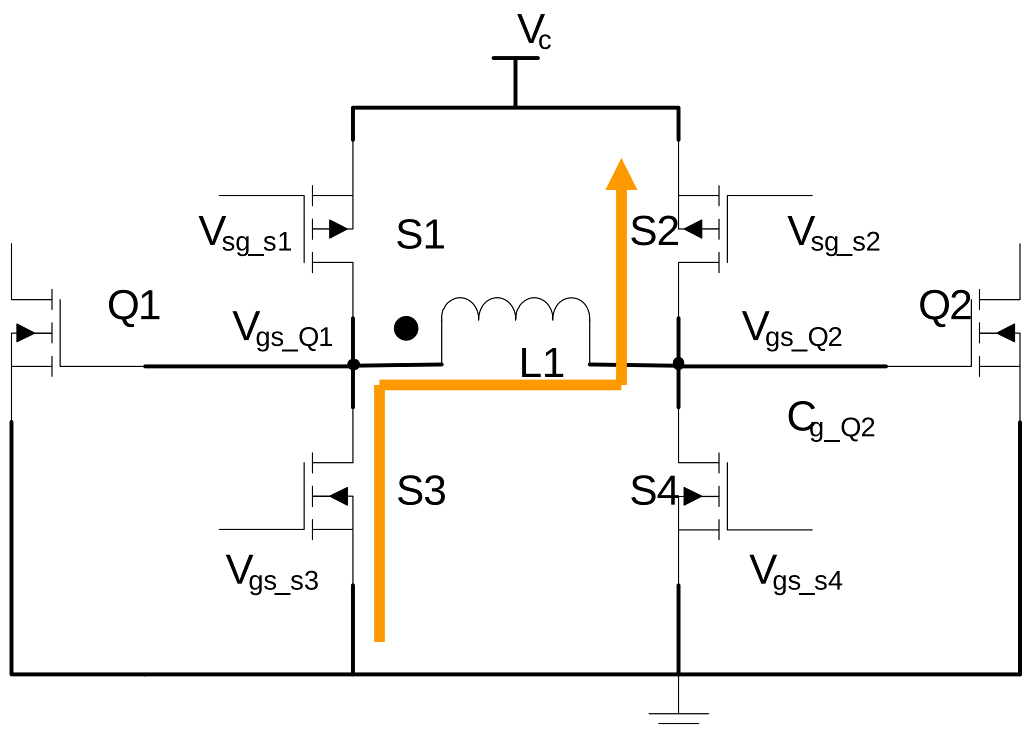


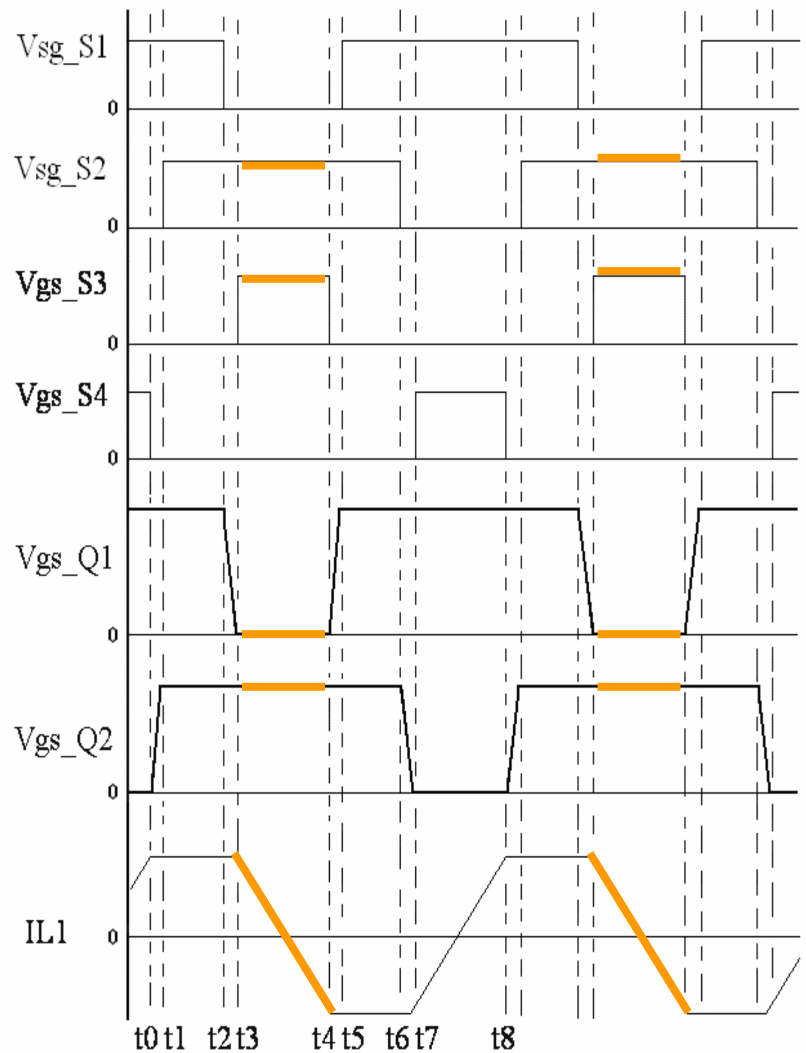


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 5 (t3 < t <t4)

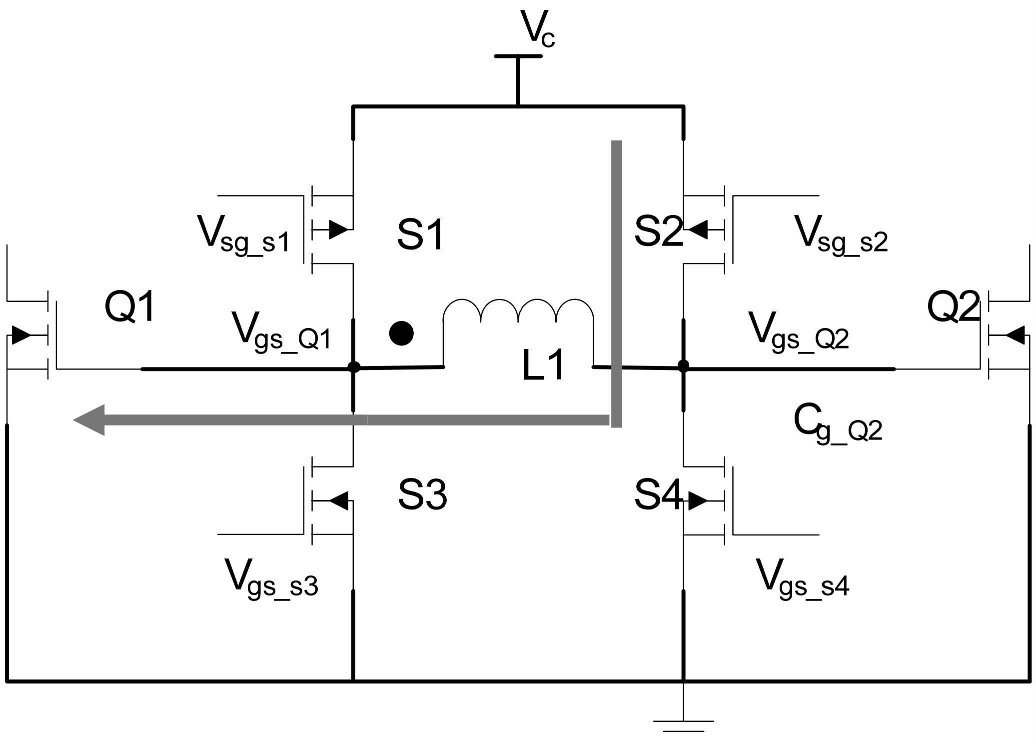


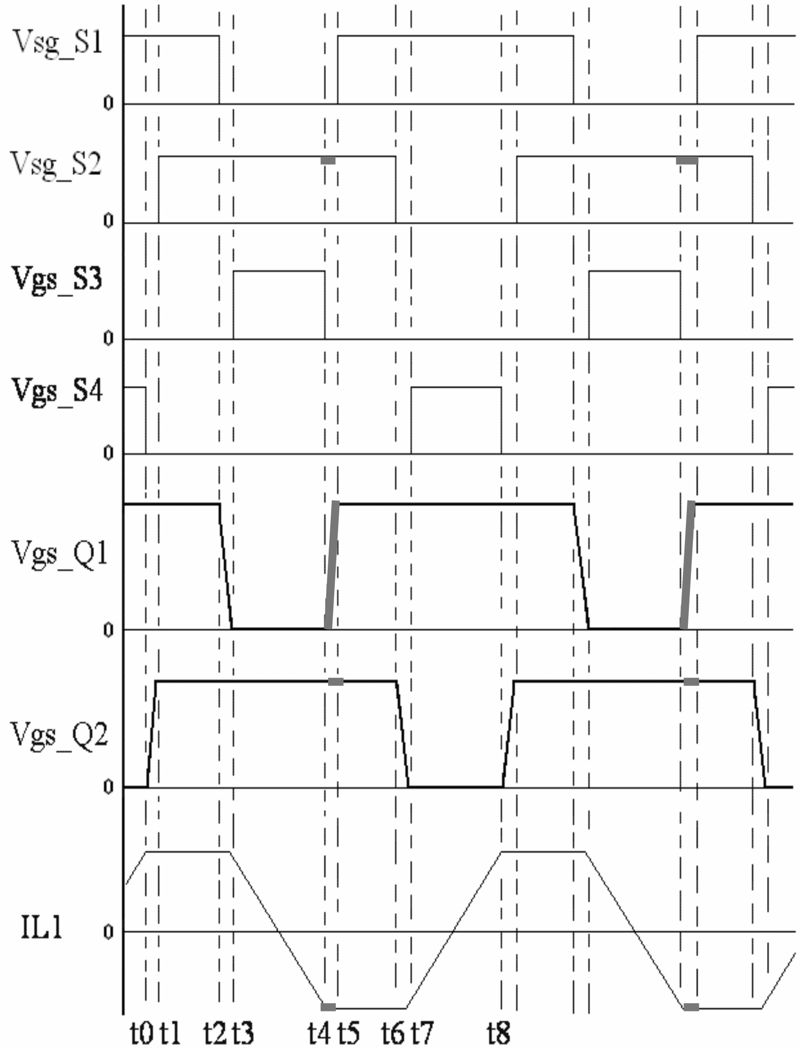


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 6 (t4 < t <t5)

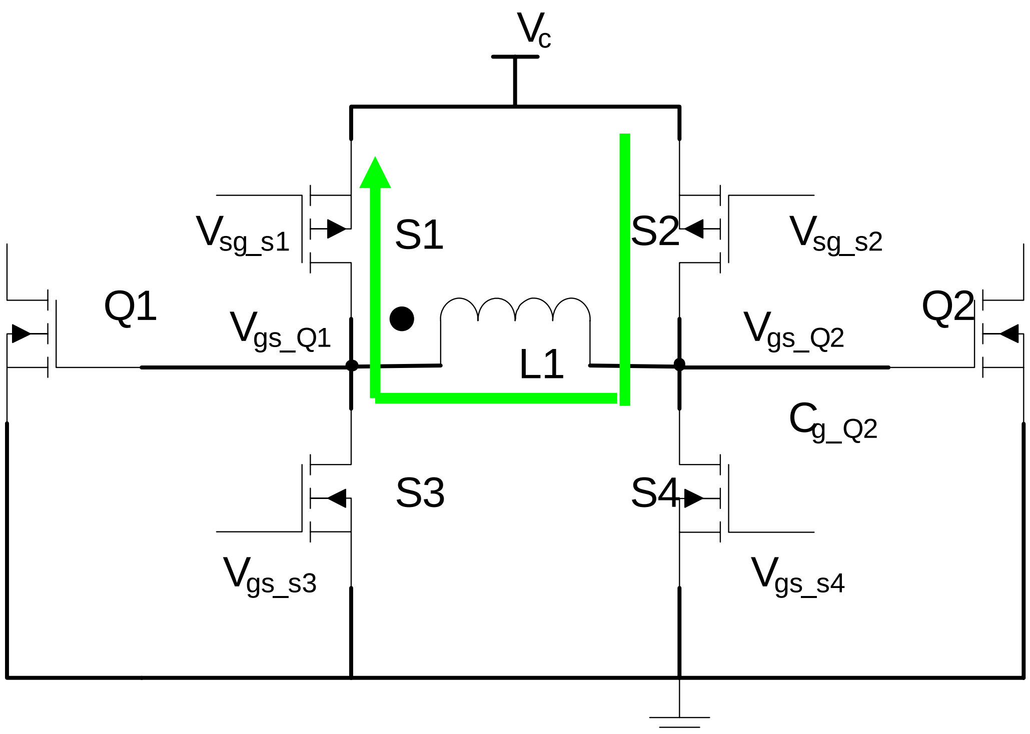


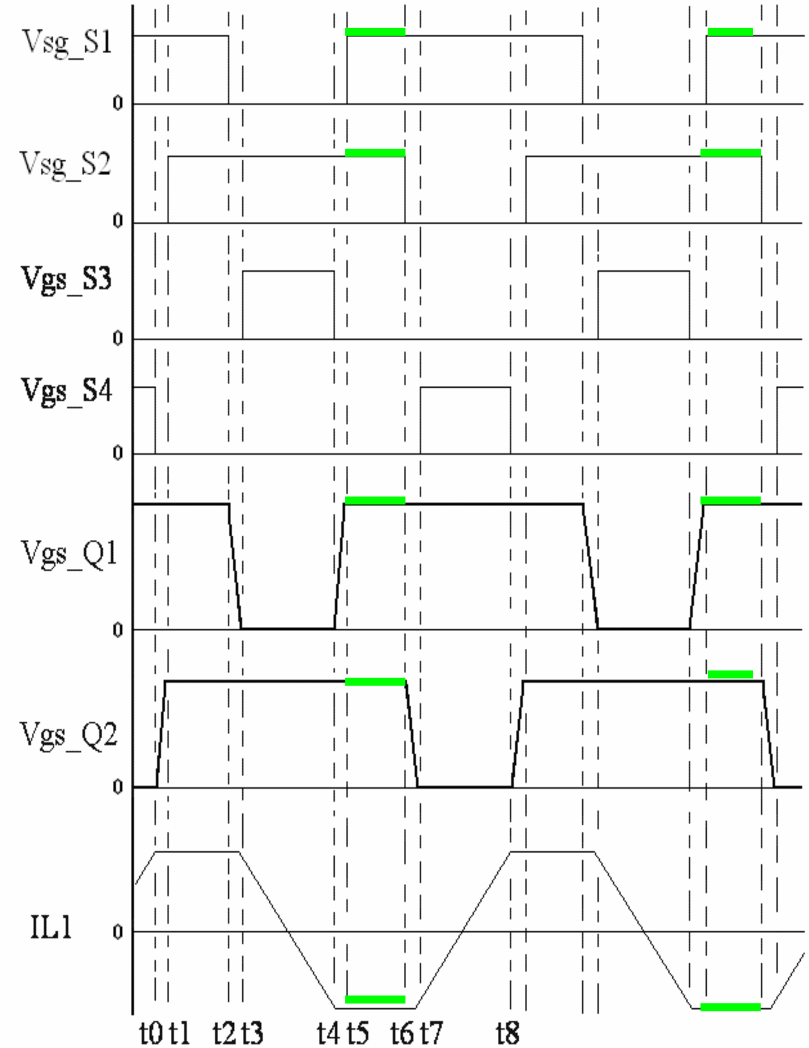


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 7 (t5 < t <t6)

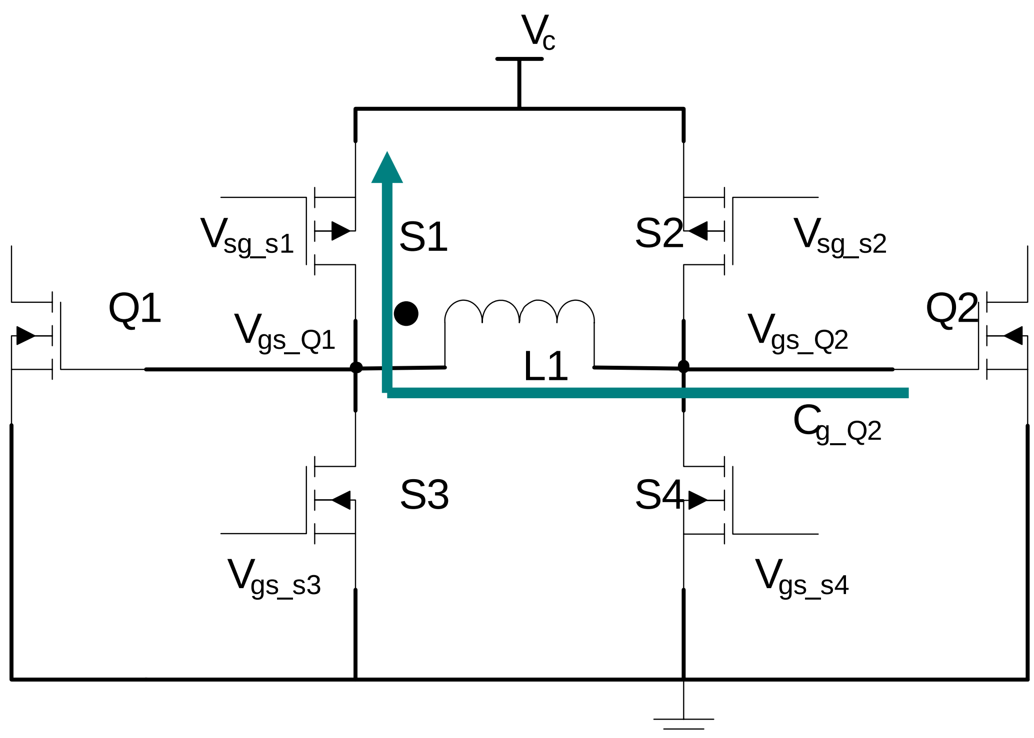


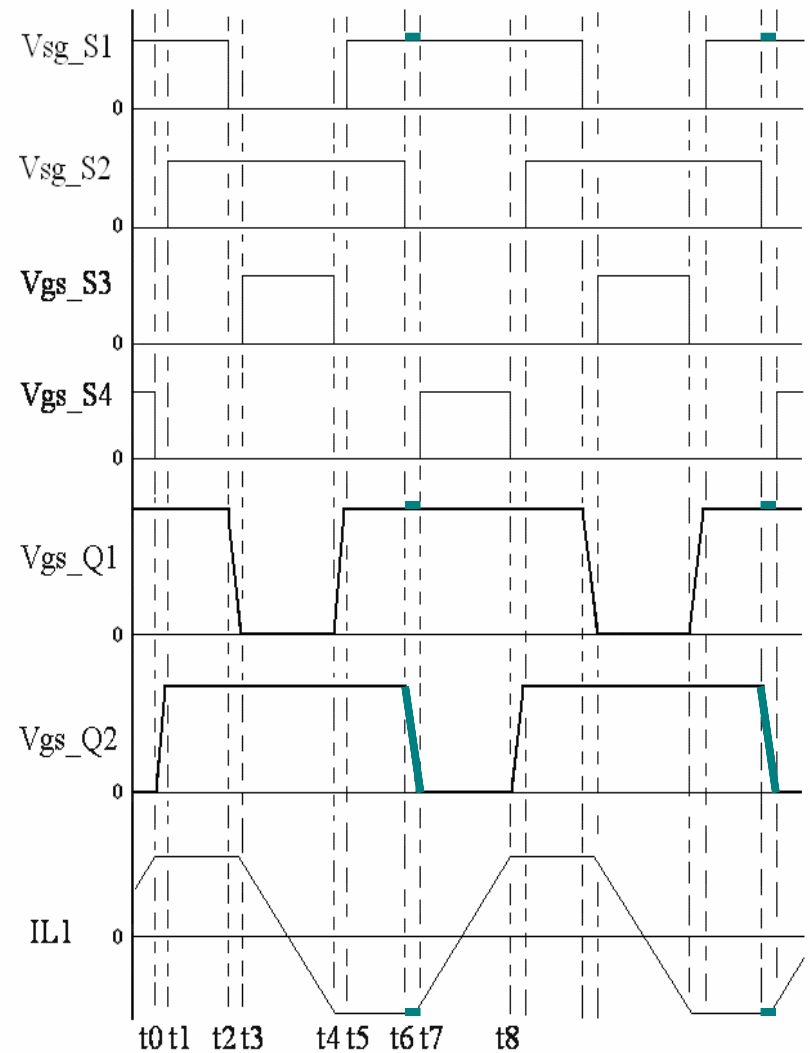


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

Mode 8 (t6 < t <t7)

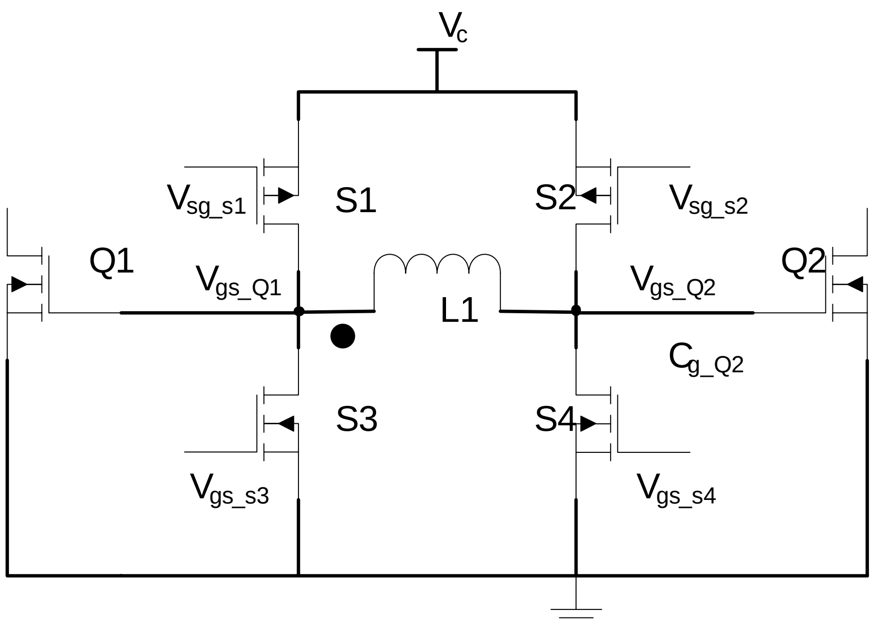


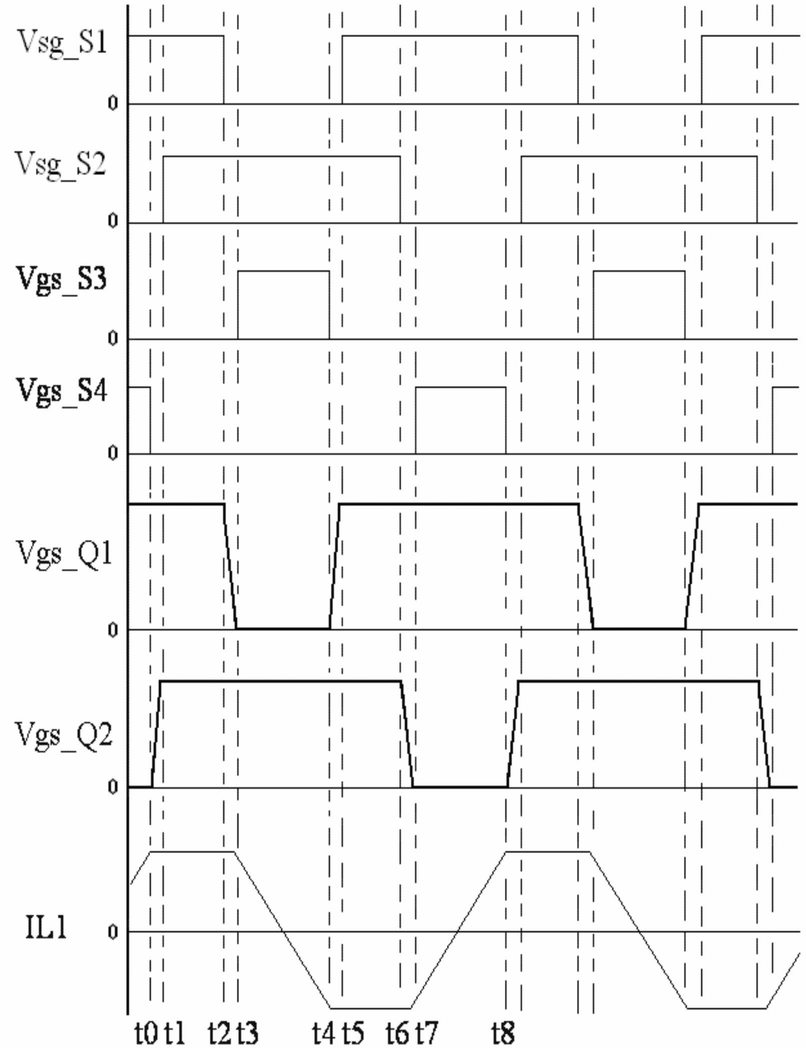


S1-S4 achieve ZVS at turn-on & turn-off

Principles of Operation

- Overlap rectifier timing shown
- Gating can be adjusted for complementary operation





Presentation Overview

1. Introduction
2. Proposed Resonant Gate Driver and Operation
3. ***Loss Analysis***
   1. ***Loss Components***
   2. ***Equations***
   3. ***Analysis Results***
4. Simulation and Experimental Results
5. Conclusions

Loss Components

1.Inductor

$$P_{ind} = P_{copper} + P_{core}$$

2.MOSFET's gate resistance

$$P_{RG} = 4R_G I_{Lpeak}^{\ 2} t_{sw} f_s$$

3.Other resistive

$$P_{cond} = P_{top} + P_{bott} = 2R_{DS(on)} I_{Lpeak}^{\ 2} \frac{4D-1}{3}$$

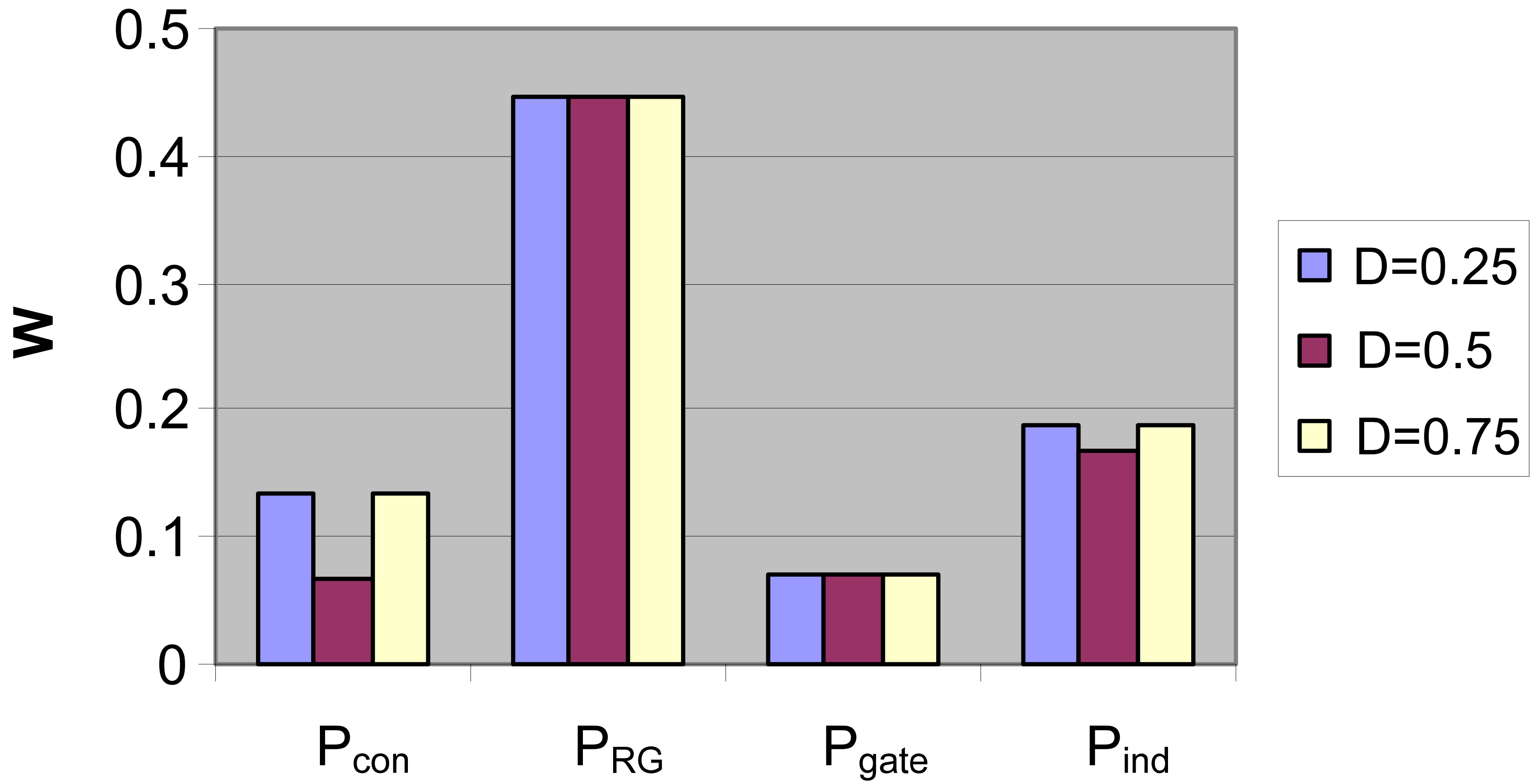
4.Control switch gate

$$P_{Gate} = 4Q_{g\_s} V_{gs\_s} f_s$$

Total

$$P_{DRV} = P_{cond} + P_{RG} + P_{Gate} + P_{ind}$$

Loss Breakdown



Total Gate Drive Loss

- Logic circuit loss: 40mW
- No cross conduction loss

E.g. Two IRF6618, Vgs = 12V, fs = 1MHz, D = 0.5

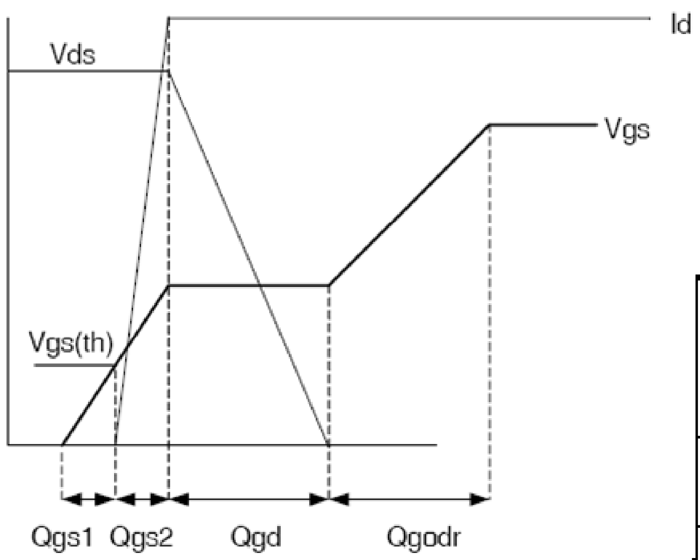
Calculated Loss	Logic Loss	Total Loss
0.752W	0.04W	0.792W

Gate Energy Savings

	Gate Loss	Additional Chip Loss	Total Loss
Conventional Driver	2.232W	0.3W	2.532W
Resonant Driver	0.752W	0.04W	0.792W
Loss Savings	1.48W	0.26W	1.74W

No cross-conduction loss in proposed driver

Turn-off Switching Loss Reduction



Gate Charge Characteristic (IRF7821 datasheet)

$V_{gs} = 12V$ $R_{DRV} = 6\Omega$
$V_{gs(th)} = 2V$ $V_p = 3V$

Drive Current Comparison

	Conventional Drive	Resonant Drive
Peak Current	2 A	1.5 A
Average Charge Current	1.54 A	1.5 A
Average Discharge Current (I_{dis})	0.46 A	1.5 A

Design Considerations

Peak drive current

$$I_{Lpeak} = \frac{Q_g}{t_{sw}}$$

Duty cycle D > 0.5

$$L = \frac{V_{gs}(1-D)T_s}{2I_{Lpeak}}$$

Duty cycle D < 0.5

$$L = \frac{V_{gs}DT_s}{2I_{Lpeak}}$$

Parameters

Parameter	Device Value
Q1, Q2	IRF6618
S1-S4	FDN335N
L1	2.2uH
V_{gs}	12V

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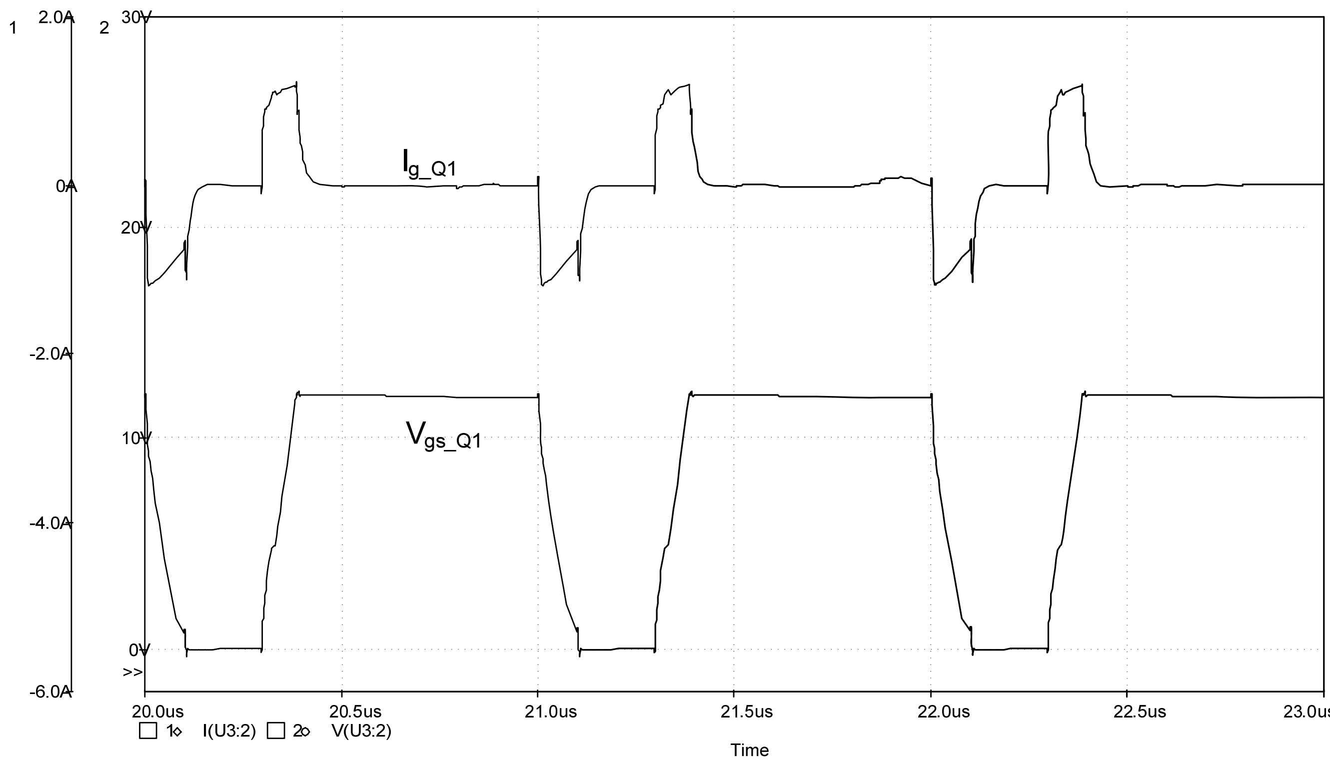
4. *Simulation and Experimental Results*
   1. *Waveforms*
   2. *Driver Loss Savings*
   3. *Switching Loss Savings*
5. Conclusions

Simulation Results



Gate Current

Gate Voltage

- **Constant charge/discharge current**
- **Charge/discharge current at peak I_L**

Boost Experimental Results:

2-Phases, 1MHz, IRF6618, 10TQ040, Vin=5.7V, Vo=11.35V, Vgs=12V

Resonant Driver: S1-S4: FDN335N, Inductor:DS3316P-2.2u

Gate Loss Comparison

	Calculated Drive Loss	Measured Drive Loss
Conventional Drive	2.532 W	2.61 W
Resonant Drive	0.792 W	0.864 W
Loss Savings	1.74 W	1.747 W

Boost Experimental Results:

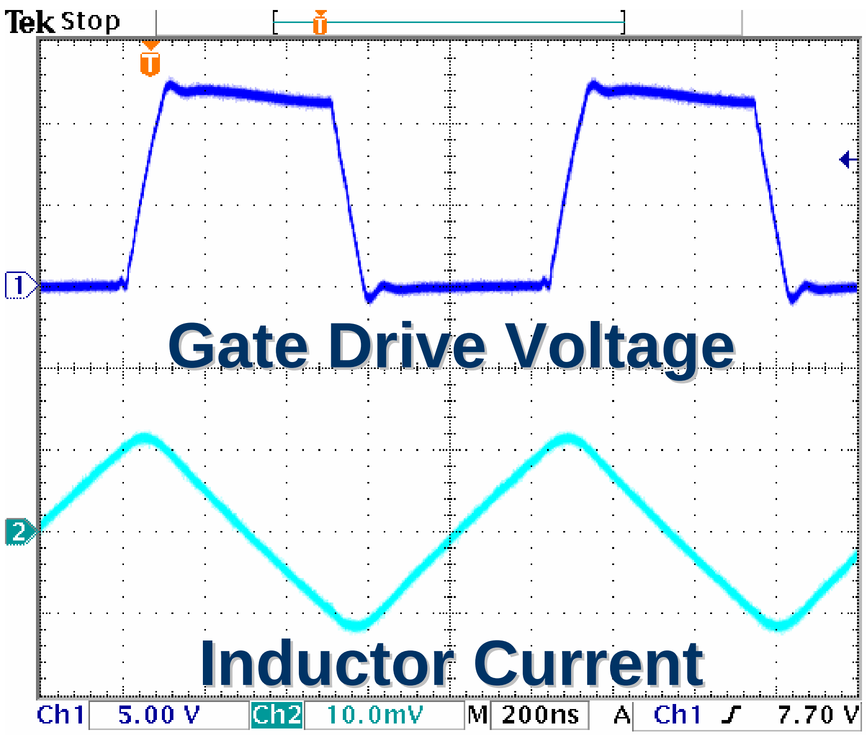
1MHz, IRF6618, 10TQ040, Vin=5.7V, Vo=11.35V, Vgs=12V

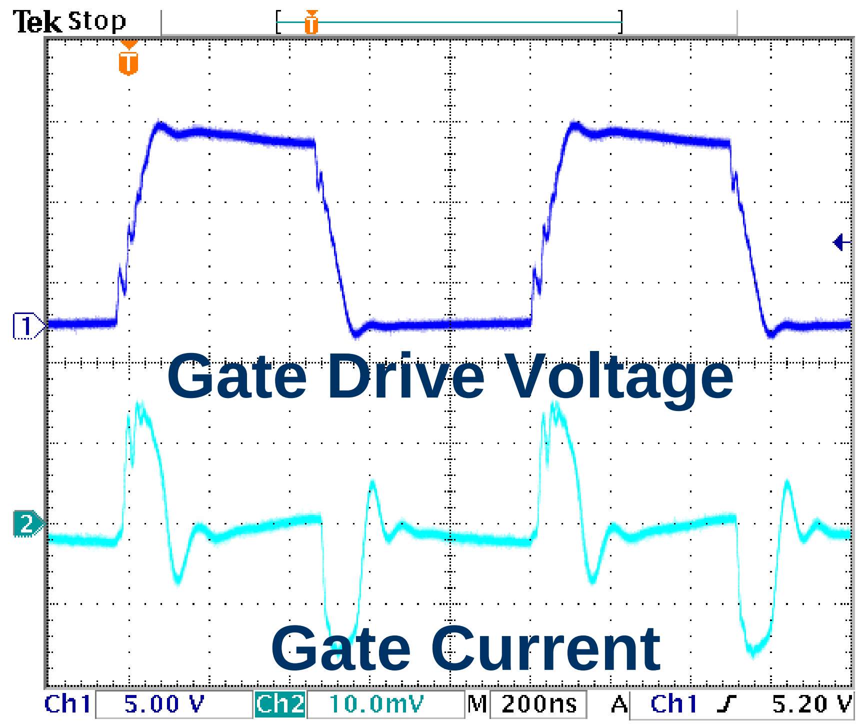
Resonant Driver: S1-S4: FDN335N, Inductor:DS3316P-2.2u

	R_{ext}	I load	Loss: UCC27323	Loss: Resonant	Loss Savings
Case 1	2.5 Ω	0.4 A	2.07 W	1.92 W	0.15 W
Case 2	2.5 Ω	0.8 A	2.78 W	2.32 W	0.46 W
Case 3	1 Ω	0.4 A	1.98 W	1.92 W	0.06 W
Case 4	1 Ω	0.8 A	2.50 W	2.32 W	0.18 W

- Switching loss reduced with faster speed
- Greater savings with heavier load

Measured Typical Waveforms





Gate charge/discharge current is nearly constant

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Conclusions

New Resonant Driver Proposed:

- Gate Energy Recovery
- Switching Loss Reduction
- Body Diode Loss Reduction
- Specific Advantages:
  - Quick turn on & off due to relatively constant inductor current at charge/discharge intervals
  - No Cdv/dt false triggering (low impedance)
  - No cross conduction
  - Simple inductor
- 0.46W savings in Boost test circuit
- Wide range of applications

Thank You For Your Time

Other Resonant Gate Drive Material at:

www.queenspowergroup.com

and

2.6 (Tuesday) and 9.3 (Yesterday)