# A Neutral Point Clamped Multilevel Topology Flow Graph and Space NPC Multilevel Topology

Hongliang Wang, Member, IEEE, Yan-Fei Liu, Fellow, IEEE, Paresh C. Sen, Life Fellow, IEEE

Department of Electrical and Computer Engineering

Queen's University, Kingston, Canada

Hongliang.wang@queensu.ca, yanfei.liu@queensu.ca, senp@queensu.ca

Abstract— Neutral-Point Clamped (NPC), such as diodeclamped, multilevel inverter technology has emerged recently as a very important alternative in the area of high-power mediumvoltage energy control. However, the NPC Multilevel topology also has variable type of structure which cannot be found due to lack of systematic derivation methodology. A new system method, called NPC Flow Graph (NPC-FG), is proposed to derive all the possible topologies in this paper, which sets the basic criteria and special steps to construct topologies. Thirtytwo NPC five-level topologies have been derived. Among them, a new family of Space NPC (S-NPC) multilevel topologies is also proposed by NPC-FG. Additional topologies can be derived based on different criteria to meet special requirement, such as Photovoltaic (PV) application. The proposed method can find all the existing multi-level NPC topologies, as well as new ones, with better performance.

#### I. INTRODUCTION

Multilevel converters (or inverters) have been used for power conversion in high-power applications such as medium voltage grid (2.3KV, 3.3KV, or 6.9KV) to reduce the switch voltage stress, and photovoltaic (PV) application to reduce the filter size and reactive and harmonic compensation in power systems[1][2], As compared with two-level voltage source inverter, the key advantage of multilevel inverter is lower voltage stress, higher efficiency, and smaller filter size, as well as lower common-mode voltage [3].

There are three classical well-known multilevel inverters, neutral-point-clamped (NPC) multilevel inverter [4][5], flying capacitor (FC) multilevel inverter[6], and cascaded H-bridge (CHB) multilevel converter/inverter[7]. The diode-clamped topology prevailed in the 1980s by[4]; the bidirectional switches-clamped or T-type(or NPP) multilevel inverter is illustrated [8][9] and researched for industry application [[10][11][12]. They are also called NPC multilevel inverter in this paper. The NPC multilevel inverter has been widely applied in different applications. To regulate the capacitors voltage, the FC multilevel inverter requires some redundant switching states. The control strategy becomes complicated and the number of capacitors increases with the number of voltage levels increasing. The CHB multilevel inverters use

series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. The H-bridge cell also uses the Multilevel NPC or FC multilevel topologies [13]. The CHB multilevel inverters have been used in several applications fields such as pump, fans, compressors, etc. In addition, they have recently been proposed for other applications like photovoltaic power-conversion system and wind power conversion [14]. Based on three classical multilevel topology or topology cell, many hybrid multilevel topologies have been proposed in high-power application. Combining NPC and CHB [15], [16], [17], and [18], combing FC and CHB [19], combining NPC and FC topology [20], [21], [22], and [23] are introduced in recent years. Thus, the generalized synthesis methodologies for classical NPC, FC and CHB topologies are important.

A generalized multilevel inverter topology is present by [24], which can balance each voltage level by itself regardless of inverter control and load characteristics. The Multilevel NPC inverter, FC multilevel inverters, and CHB multilevel inverter also can be derived from this generalized inverter topology. Moreover, the new multilevel topologies, such as Active NPC (ANPC) multilevel inverter [25], Multilevel Modular Capacitor-Clamped (MMCC) inverter [26] and zigzag multilevel inverter [27] also can be derived using the method proposed in [24].

Many multilevel modulation strategies have also been proposed. The dc-link capacitor voltage balance issue has been analyzed in detail for NPC, FC [28], [29], [30], [31], and [32]. Specifically, the self-voltage-balance topologies in [24] and [33], as well as its special case [34] have demonstrated that the DC-link capacitor voltage can be balanced automatically. is the benefit of your proposed method?)

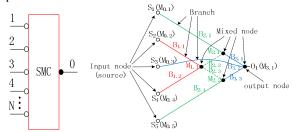
This paper focuses on the NPC topologies, the moudulation method can also use the conventional method. A new system method, called NPC Flow Graph (NPC-FG) is proposed to derive all the topologies of NPC multilevel converters. The elements and basic rule are defined. The example of three-level and five-level NPC-FG is derived to explain the detailed operation. A new family of Space NPC

(S-NPC) multilevel topologies have been derived using the proposed NPC-FG method.

This paper is organized as follows: Section II describes the basic idea of NPC-FG for multilevel converter; Section III introduces an example of NPC three-level topologies based on multilevel topology NPC-FG; Section III introduces an example of NPC five-level topologies based on multilevel topology NPC-FG; Section IV discusses space NPC multilevel topology. Section V gives conclusion. Section VI discusses the future work.

## A. NPC MULTILEVEL TOPOLOGY FLOW GRAPH BASIC ELEMENT OF NPC-FG

Fig.1 shows the basic structure of NPC Flow Graph. Fig.1 (a) shows the general block of one phase leg of N-level. Fig.1 (b) shows a possible connection between the input nodes (S1, S2 ...) and the output node (O). Fig.1 (c) shows the possible implementations of the branches.



(a) One phase leg of N-level (b) node and branch of flow graph
Fig.1 the multilevel topology flow graph

More detailed definition is listed as following:

- 1) Node: A node is a point.
- 2) Branch: A branch is a line segment joining two nodes.
- Input node or source: An input node or source is a node that has only outgoing branches. It is marked as S<sub>0,j</sub>, j=1, 2...N.
- Output node or sink: An output node or sink is a node that has only incoming branches. It is marked as O<sub>1</sub>.
- 5) Outgoing branch: the branch is starting from one mixed node, is called the outgoing branch of this mixed node. For example, the branch B1.1 is the outgoing branch of M0.2.
- 6) Incoming branches: the branch is ended from one mixed node, is called the incoming branch of this mixed node. For example, the branch B1.1 is the incoming branch of M1.1.
- 7) Mixed node: A mixed node is a node that has both incoming and outgoing branches. It is marked as M<sub>i, j</sub>. The input node can be considered as a special mixed node as M<sub>0, j</sub>. The output node is the final mixed node.
- 8) Dotted Branch: for the outgoing branches of mixed node, there are two dotted branches to provide bi-directional current flow. The dotted branch represents diode

- implementation. For example, branches B2.2 and B2.3 are dotted branches.
- 9) Solid branch: for the outgoing branches of mixed node, the solid branch represents switch implementation, which provides bi-directional current flow. For example, branches B1.1 and B1.2 are solid branches.
- 10) Branches Crossing: two branches has a crossing in the space is called branches crossing. For example, the branch B3.2 is crossing branch B1.1 or B1.2 and branch B2.2 or B2.3.

### B. Relization elements of NPC topology

Once the NPC-FG is finished, the new topology can be described by the realization elements and rule. The Fig.2 shows the realization element of incoming branch of NPC-FG.

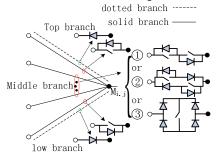


Fig.2 realization element of incoming branch of NPC-FG Some elements are defined as follows.

- Top branch: For the incoming branches of mixed node, the top one branch is defined as top branch. Top branch represents one diode or one switch.
- Low branch: For the incoming branches of mixed node, the low one branch is defined as top branch. Top branch represents one diode or one switch.
- 3) Middle branch: For the incoming branches of mixed node, the branch is between top branch and low branch defined as middle branch. The middle branch represents controlled bi-directional current flow by switches. There are three structures as show in Fig.3 (c). It is note that the middle branch is not always present. And the dotted branch cannot become the middle branch.

### C. Rule

There are several basic rules as follows

- 1) The source notes are the left-side, and the output node is right side.
- 2) All branches are added from left to right.
- 3) Usually, every note only has two dotted branches or one solid branch to provide bi-directional current for outgoing branch in this paper. This rule can be changed according to special requirement, For example, active-NPC(ANPC) topology, two bi-directional current flows are provided to get the redundant state Thus, several

- mixed notes has two solid branches for outgoing branch to provide two solid branches.
- 4) The middle branch doesn't always exist for all mixed notes, and the middle branch only chooses solid branch because of bi-directional controlling current flow.
- 5) Once several branches are crossing each other, two originally mixed notes are connected by several branches; it is prevent to short-circuit of two mixed notes. Two situations are correct as follows, (a) there are two dotted branches of these branches, because there is no current flow between two mixed notes; (b) At least one middle branch is included in these branches, because the middle branch can control the bi-directional current flow.

### D. Steps of NPC-FG

Five-level NPC topologies are made as an example to show how to get NPC-FG and topology. The number of multilevel is N=5. Fig.3 shows one example of five-level NPC topology to explain the steps of multilevel topology flow graph. All steps must satisfy the rule.

- Setting the N source node. Marked M0.j. j=1, 2...5. The figure is shown in Fig.3 (a).
- 2) 1<sup>st</sup> mixed operation. Choosing some source nodes, add outgoing branch using the dotted or solid branch and mark the mixed note M1.j. The minimum note number is 2, and Maximum notes number is N. For example, two

- mixed points M0.2 and M0.4 are choose in fig.3 (b) and they are connected into mixed note M1.1 by the sold branch B1.1 and B1.2.
- 3) 2<sup>nd</sup> mixed operation, choose some mixed nodes or source nodes and add outgoing branch using the dotted or solid branch, and then mark the mixed note M2.j. For example, there are maximum four mixed notes M0.1, M0.3, M0.5, M1.1 can be chosen for mixed operation from fig.3 (b). Three mixed notes M0.1, M0.5 and M1.1 are choose in fig.3(c). They are connected into the mixed notes M2.1 and M2.2 by the solid branches B2.1, B2.4 and dotted branches B2.2, B2.3.
- 4) Repeat the step 3. Stop operation until only one mixed node exists; this mixed node is the output node or sink. Finally, the NPC-FG is finished as shown in fig.3 (d).
- 5) Branch crossing rule checking: without branches crossing, skip the step. If NPC-FG has the branches crossing, do next. For example, the branch B3.2 is crossing several branches, such as B1.1or B1.2, B2.2 or B2.3. The branch B3.2 is the middle branch of M3.1. Thus, it is correct to meet the rule requirement.
- 6) According to the NPC-FG shown in Fig.3 (d). The topology can be shown in fig.3 (e) based on the realization element, which is shown in fig.2.

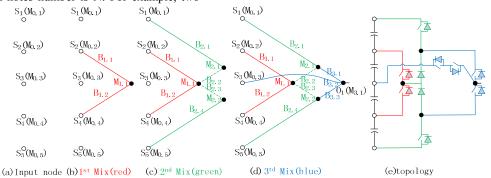
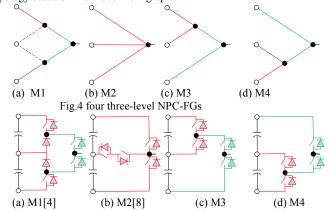


Fig.3 one example of five-level topology based on multilevel flow graph

# II. EXAMPLE OF THREE-LEVEL NPC TOPOLOGIES BASE ON FLOW GRAPH

This section is an example of three-level NPC topologies. There are three source notes. The red line is the 1<sup>st</sup> mixed operation; the green line is the 2<sup>nd</sup> mixed operation. Fig. 4(a), (b) are chosen three source notes in the 1<sup>st</sup> mixed operation. The difference between them is dotted branches are used in fig.4(a) and solid branch is used in fig.4(b). Two source notes are chosen in the 1<sup>st</sup> mixed operation in fig.4(c), (d). Four NPC-FGs are shown in fig.4. Fig.5 shows the four topologies of three-level NPC-FG.



# III. EXAMPLE OF FIVE-LEVEL NPC TOPOLOGIES BASE ON FLOW GRAPH

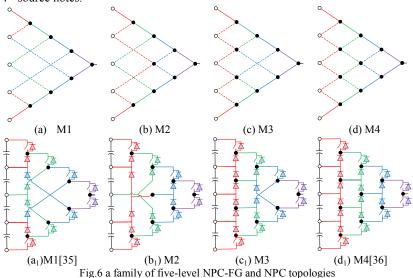
This section is an example of NPC five-level topologies. The source notes number is five. As 1<sup>st</sup>, 5<sup>th</sup> source notes are the top or bottom, thus, only solid branch can be chosen as the outgoing branch of 1<sup>st</sup>, 5<sup>th</sup> source notes. Based on this situation, three families of NPC-FG are introduced in next.

Part A shows the NPC-FG which only dotted branch is used for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes. Part B shows NPC-FG which only solid branch is used for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes. Part C shows NPC-FG which hybrid dotted branch and solid branch are used for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes.

## A. Only using the dotted branch for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes

In this part, only the dotted branch is used, and the middle branch doesn't exist. Fig.4 shows four NPC five-level topologies.Fig.4 (a), (b), (c) and (d) are the four multilevel topology flow graph. Fig.4 (a), (b), (c) show that these NFC-FGs which exist the branch crossing and satisfy the branch crossing rule as two dotted branches crossing.

Fig.4  $(a_1)$ ,  $(b_1)$ ,  $(c_1)$  and  $(d_1)$  are the four multilevel topologies according to the flow graph, which are all the diode-clamping five-level topologies.



# B. Only using the solid branch for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes

In this part, only the solid branch is used. Fig.7 shows four NPC five-level topologies. Fig.7 (e), (f), (g), and (h) are four NPC-FGs. Fig.4 ( $e_1$ ), ( $f_1$ ), ( $g_1$ ), ( $h_1$ ) shows the four multilevel

topologies according to NPC-FG. Fig.7 (h) show the NPC-FG which has branches crossing and satisfies the branch crossing rule as one branch including the crossing branches is the middle branch.

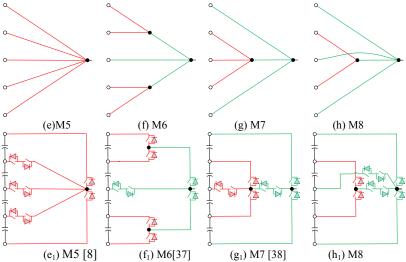
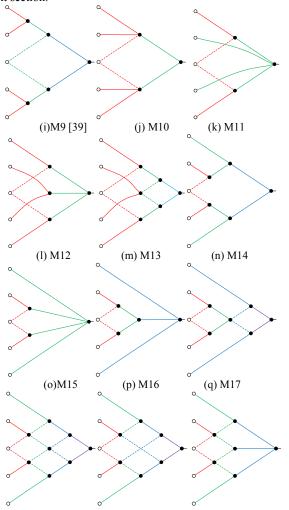


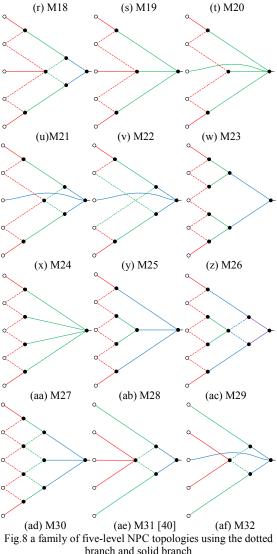
Fig. 7 a family of five-level NPC-FG and topology only using the solid branch

## C. Using dotted branch and solid branch for 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> source notes

In this part, the dotted branch and the solid branch are used for 2nd, 3rd, 4th source notes.Fig.6 shows twenty-four NPC five-level topologies using the solid branch and dotted branch.

Fig.6 (k), (l), (m), (s), (w), (x), (y), (af) show that these NFC-FG which exist the branch crossing. Fig.6 (l), (m), (s) satisfy the branch crossing rule as there are two dotted branches between two mixed notes. Fig. 6 (k), (w), (x), (y), (af) satisfy the branch crossing rule as there is a middle branch. Like these NPC-FGs, a corresponding topologies, are called Space NPC (S-NPC) multilevel topologies, which are shown in next section.

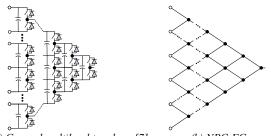




branch and solid branch

### IV. SPACE MULTILEVEL NPC TOPOLOGIES (S-NPC)

Fig.9 (a) shows the general multilevel topology [9]. Its NPC-FG can be get as shown in fig.9 (b). Several mixed nodes have two solid branches, which mean two bi-directional current flows. Thus, the ANPC multilevel topology can derive from it. But, it has not the branch crossing of NPC-FG. The space multilevel topology doesn't be derived from the general multilevel topology.



(a) General multilevel topology [7] (b) NPC-FG
Fig.9 general multilevel topology and its NPC-FG
According to NPC-FG of fig.7 (h), fig.8 (k), (l), (m), (w),
(x), (y), (af), eight S-NPC topologies are shown in fig.10.

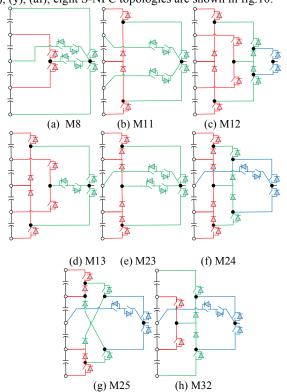


Fig. 10 S-NPC five-level topologies from NPC-FG

### V. CONCLUSION

A new systematic method, called NPC-FG (Please spell out the NPC-FG) is proposed to derive all possible topologies for multilevel NPC converters. The basic element, rule and steps are built to create NPC-FG. Three-level and five-level NPC-FG have been used as two examples to illustrate procedure to create the new topologies. The corresponding topologies can be derived from it. All present NPC topologies have been derived from NPC-FG and many new topologies have also been derived. More importantly, the new S-NPC topologies are proposed using the branch crossing rule from

the new topologies, which extend the general NPC topology methodology. The NPC-FG can be extended to use hybrid multilevel topologies which include the NPC cell.

#### References

- [1] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *Ind. Appl. IEEE Trans.*, vol. 33, no. 1, pp. 202–208, 1997.
- [2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. W. Bin Wu, J. Rodriguez, M. a. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [3] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.
- [4] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, 1981.
- [5] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6. pp. 2930–2945, 2007.
- [6] F. Richardeau, P. Baudesson, and T. A. Meynard, "Failures-tolerance and remedial strategies of a PWM multicell inverter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 905–912, 2002.
- [7] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.
- [8] J. Holtz, "Selbstgefuhrte wechselrichter mit treppenformiger ausgangss- pannung für grose leistung und hohe frequenz," *Siemens Forschungs- und Entwicklungsberichte*, vol. 6, no. 3, pp. 164–171, 1977.
- [9] N. Matsiii, "PWM control and input characteristics of threephase multi-level AC/DC converter," *Power Electron. Spec. Conf. 1992. PESC '92., 23rd Annu. IEEE*, no. 1, 1992.
- [10] J. Dixon and L. Morán, "High-level multistep inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 330–337, 2006.
- [11] V. Guennegues, B. Gollentz, F. Meibody-Tabar, S. Rael, and L. Leclere, "A converter topology for high speed motor drive applications," in *Power Electronics and Applications*, 2009. EPE '09. 13th European Conference on, 2009, pp. 1–8.
- [12] B. Wu, High-Power Converters and ac Drives. 2005.
- [13] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 412–420, 2011.
- [14] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, 2013.
- [15] Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output

- voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, 2007.
- [16] I. Etxeberria-Otadui, A. Lopez-de-Heredia, J. San-Sebastian, H. Gaztañaga, U. Viscarret, and M. Caballero, "Analysis of a H-NPC topology for an AC traction front-end converter," in 2008 13th International Power Electronics and Motion Control Conference, EPE-PEMC 2008, 2008, pp. 1555– 1561.
- [17] V. Guennegues, B. Gollentz, L. Leclere, F. Meibody-Tabar, and S. Raël, "Selective harmonic elimination PWM applied to H-bridge topology in high speed applications," in POWERENG 2009 2nd International Conference on Power Engineering, Energy and Electrical Drives Proceedings, 2009, pp. 152–156.
- [18] C. M. Wu, W. H. Lau, and H. Chung, "A five-level neutral-point-clamped H-bridge PWM inverter with superior harmonics suppression: a theoretical analysis," ISCAS'99. Proc. 1999 IEEE Int. Symp. Circuits Syst. VLSI (Cat. No.99CH36349), vol. 5, 1999.
- [19] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-Bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3505–3512, 2012.
- [20] L. A. Serpa, P. M. Barbosa, P. K. Steimer, and J. W. Kolar, "Five-level virtual-flux direct power control for the active neutral-point clamped multilevel inverter," in *PESC Record* - *IEEE Annual Power Electronics Specialists Conference*, 2008, pp. 1668–1674.
- [21] M. Narimani, B. Wu, G. Cheng, and N. Zargari, "A new nested neutral point clamped (NNPC) converter for medium-voltage (MV) power conversion," in *Conference Proceedings - IEEE Applied Power Electronics Conference* and Exposition - APEC, 2014, pp. 2372–2377.
- [22] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1907–1918, 2013.
- [23] Y. Kashihara and J. I. Itoh, "Performance evaluation among four types of five-level topologies using Pareto front curves," 2013 IEEE Energy Convers. Congr. Expo. ECCE 2013, pp. 1296–1303, 2013.
- [24] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.
- [25] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, 2005.
- [26] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor Clamped DC-DC Converter," Conf. Rec. 2006 IEEE Ind. Appl. Conf. Forty-First IAS Annu. Meet., vol. 2, 2006
- [27] F. Zhang, S. Yang, F. Z. Peng, and Z. Qian, "A zigzag cascaded multilevel inverter topology with self voltage balancing," Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, pp. 1632–1635, 2008.
- [28] S. J. Watkins and L. Zhang, "Influence of multilevel sinusoidal PWM schemes on the performance of a flying-

- capacitor inverter," in *Power Electronics, Machines and Drives, 2002. International Conference on (Conf. Publ. No. 487)*, 2002, pp. 92–97.
- [29] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, 2000.
- [30] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, 2005.
- [31] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, 2008.
- [32] C. F. C. Feng, J. L. J. Liang, and V. G. Agelidis, "A novel voltage balancing control method for flying capacitor multilevel converters," *IECON'03. 29th Annu. Conf. IEEE Ind. Electron. Soc. (IEEE Cat. No.03CH37468)*, vol. 2, 2003.
- [33] A. Chen and X. He, "Research on hybrid-clamped multilevel-inverter topologies," *IEEE Trans. Ind. Electron.*, vol. 53, no. 6, pp. 1898–1907, 2006.
- [34] H. Wang, "A half-bridge five-level topology and its application," CN102624270, 2012.
- [35] R. H. Baker, "Bridge converter circuit," US 4270163, 1981.
- [36] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 711–718, 2000.
- [37] H. Wang, X. Yue, H. Ni, and W. Zhao, "a five-level topology and its application," CN102427304, 2011.
- [38] H. Wang, "A T-T five-level circuit and its application," 2012.
- [39] R. Chibani, E. M. Berkouk, and G. Manesse, "PWM current rectifier-five NPC level inverter cascade. Application to the PM synchronous machine," 1999 IEEE Africon. 5th Africon Conf. Africa (Cat. No.99CH36342), vol. 2, 1999.
- [40] H. Wang, "a T-I five-level circuit and its application," CN102710161, 2012.