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High Performance Digital Control Algorithms for DC-DC Converters Based on the Principle of Capacitor Charge Balance

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Presentation Outline



- **Introduction**
- **Concept of Capacitor Charge Balance**
- **Load Current Transient**
- **Input Voltage Transient**
- **Experimental Results**
- **Conclusion**

1. Introduction



- VRMs must adhere to increasingly stringent dynamic performance criteria
- Alter topology (increase size of output capacitor)
 - **Disadvantages:**
 - Increased cost
 - Increased real-estate
- Increase switching speed
 - **Disadvantages:**
 - Decrease efficiency

Controller Improvement

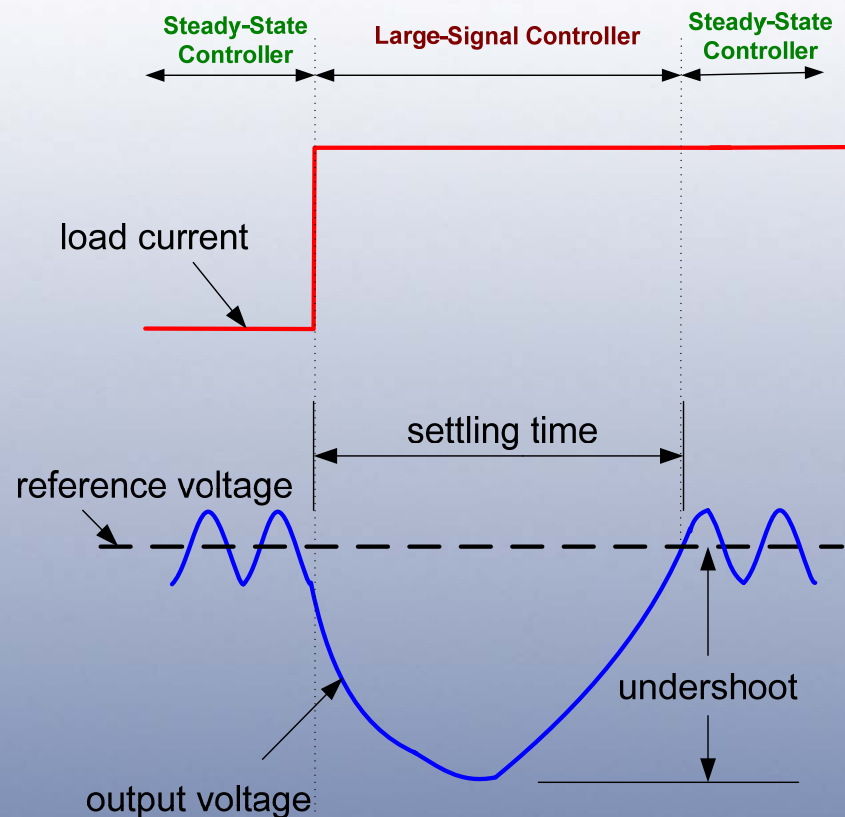


- **Improve control method**
 - **Advantages:**
 - **Significantly less expensive than topology modification**
 - **Typically no effect on efficiency**

Steady State vs. Transient



- **Conventional controllers**
 - Designed using frequency-domain small-signal model
 - Zero-steady state error
 - Widest bandwidth with sufficient phase margin
 - Model insufficient for large-signal time-domain transients
- **Alternative controller**
 - Separate control methods for steady and transient states
 - Well suited for digital implementation



Digital Controllers



Advantages:

- **Re-programmability**
 - No hardware modification needed for altered topology
- **Reliability**
 - Tolerance and non-idealities of analog control components
- **System Integration**
 - Higher integration with digital circuits
- **Simplicity**
 - For controls requiring complicated arithmetic

Analog to Digital: New Implementation, Old Problems

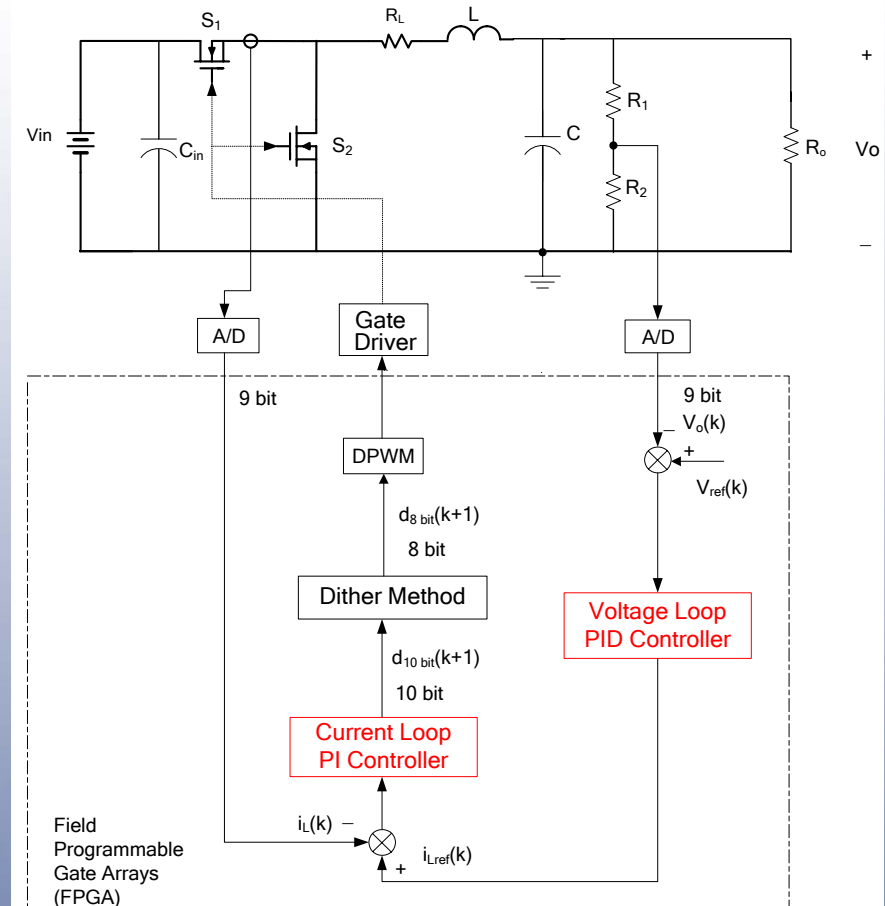


Majority of research:

- Conventional analog designs copied
- Still suffers from slow compensation networks

Novel methods:

- Digital control simplifies complicated arithmetic
- Can be used to develop new non-linear control strategies

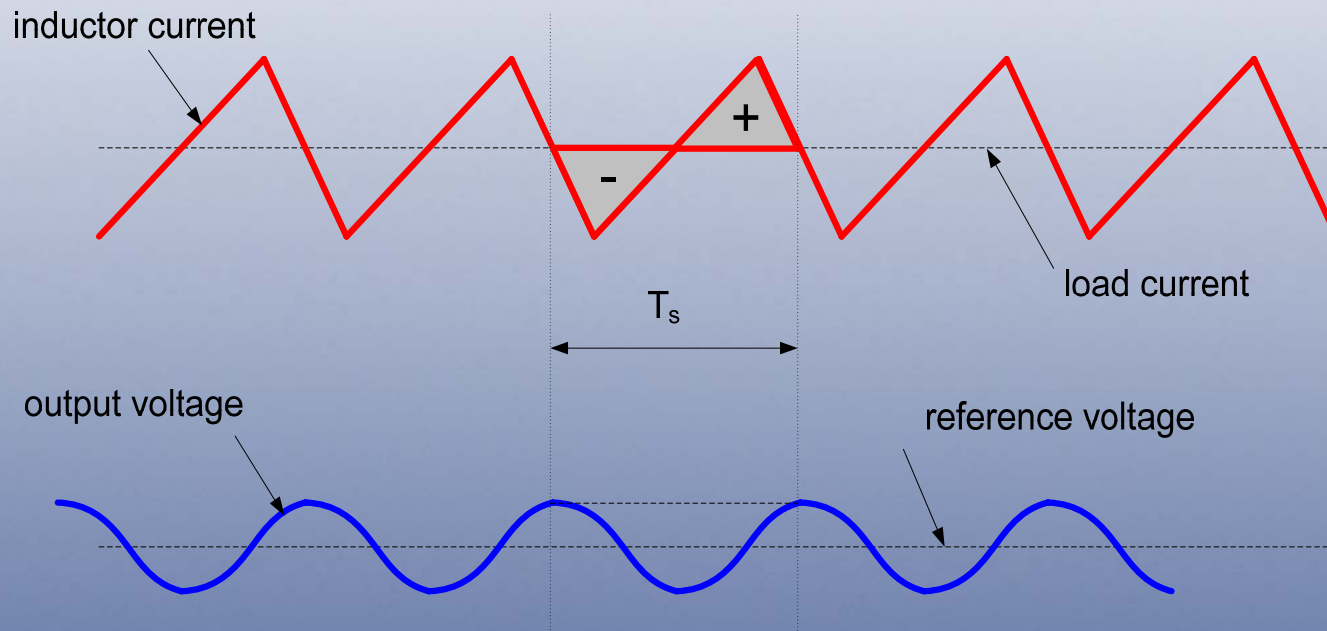
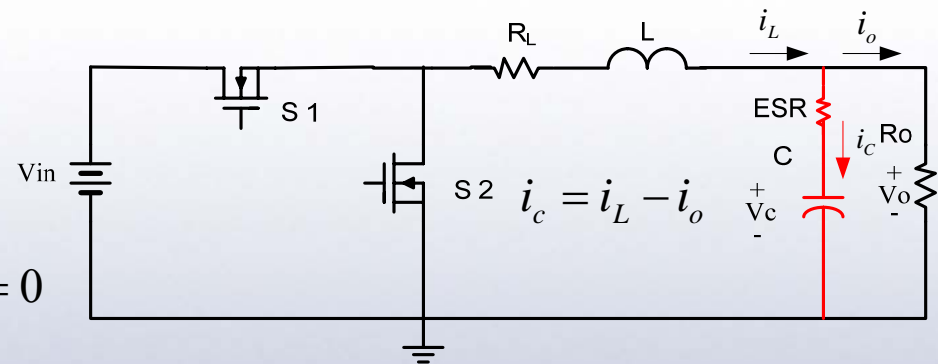


Digital Current Mode Controller

2. Capacitor Charge Balance

- Used extensively in steady-state analysis of DC-DC converters

$$v_c(T_s) - v_c(0) = \frac{1}{C} \cdot i_{c_{avg}} = 0 \rightarrow \frac{1}{T_s} \int_0^{T_s} i_c(t) dt = 0$$



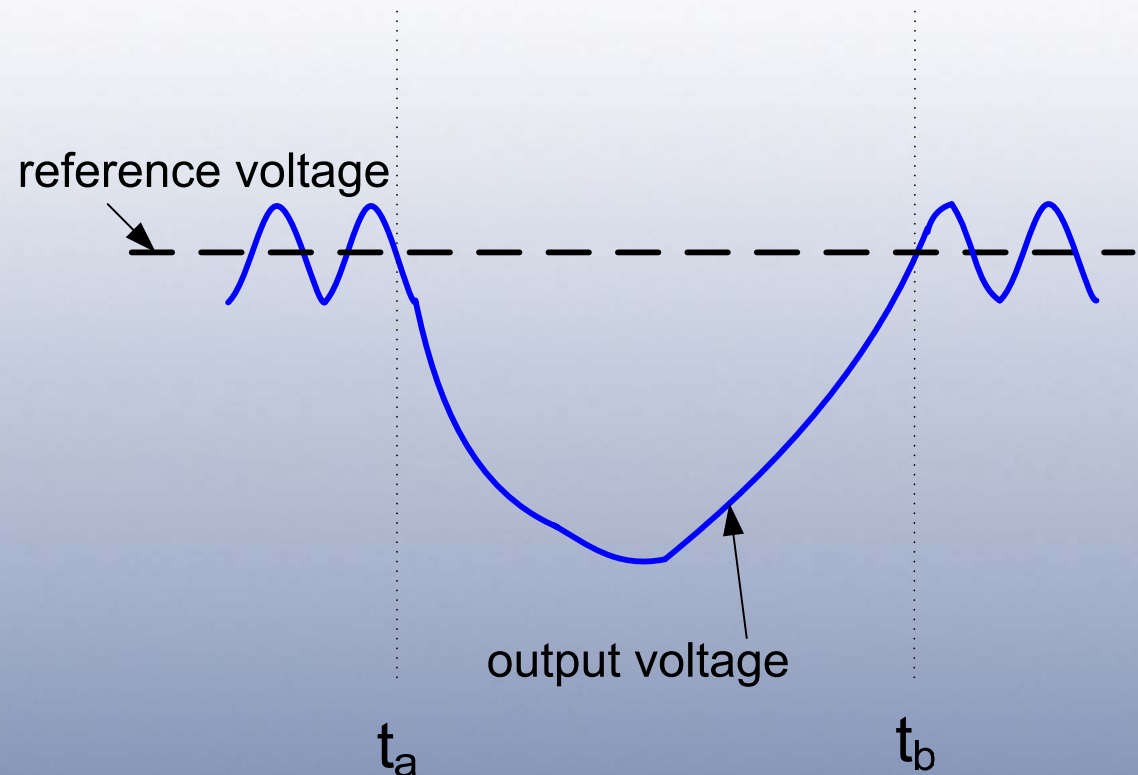
Capacitor Charge Balance

- **Extend principle to transient**

$$v_c(t_b) - v_c(t_a) = \frac{1}{C} \cdot i_{c_{avg}} = 0$$

$$\frac{1}{t_b - t_a} \int_{t_a}^{t_b} i_c(t) dt = 0$$

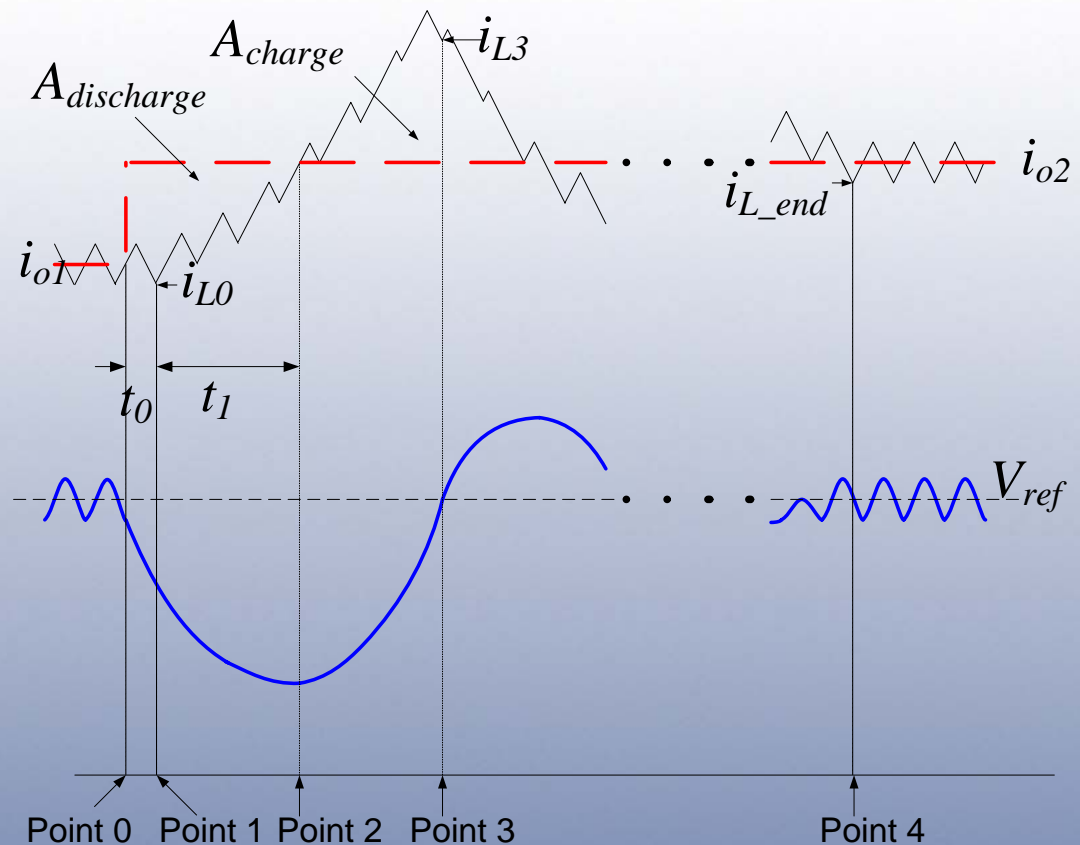
- **Voltage recovers to original value when net charge balanced**
- **Goal: Balance charges when inductor current reaches steady state value in shortest possible time**



3. Load Current Transient

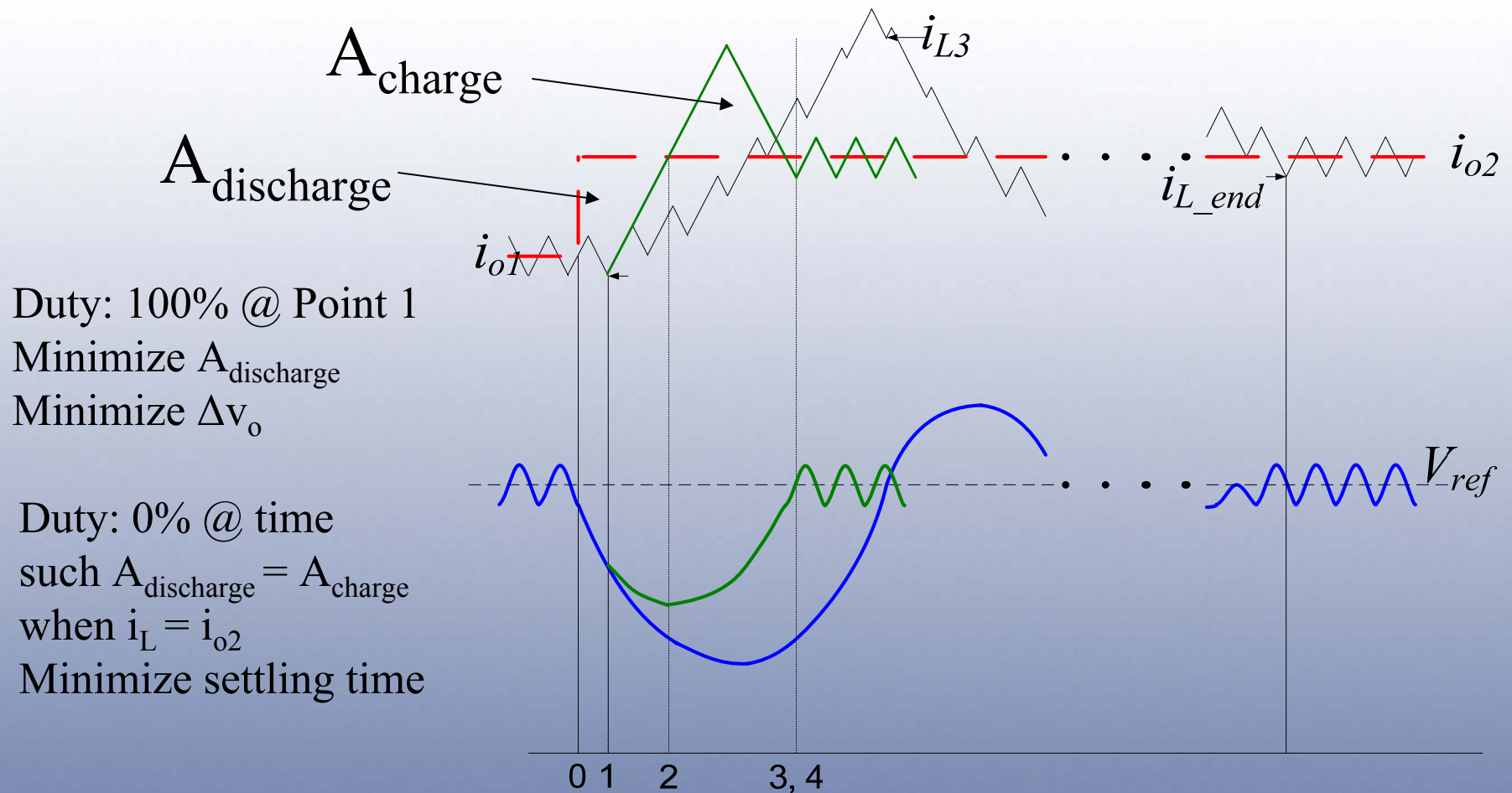
- Point 0: Load current step
- Point 1: Controller slowly increases duty
- Point 2: Inductor current equal load current
- Point 3: Output voltage recovered
 - Inductor current > Load current
- Point 4: Converter “recovered”

How can we improve this response?



Conventional Control Method

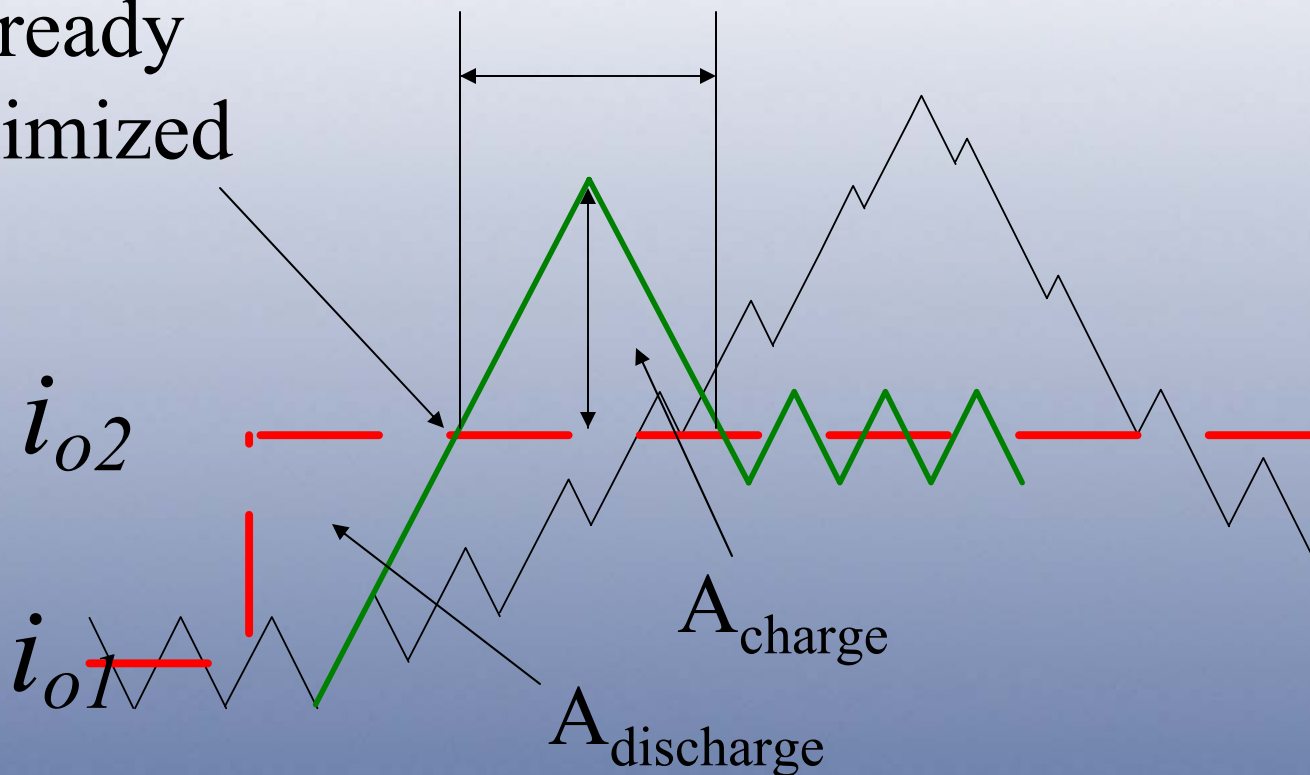
Load Current Transient Optimized



Minimize Transient Time

minimize re-charge
time by maximizing i_{Lpeak}

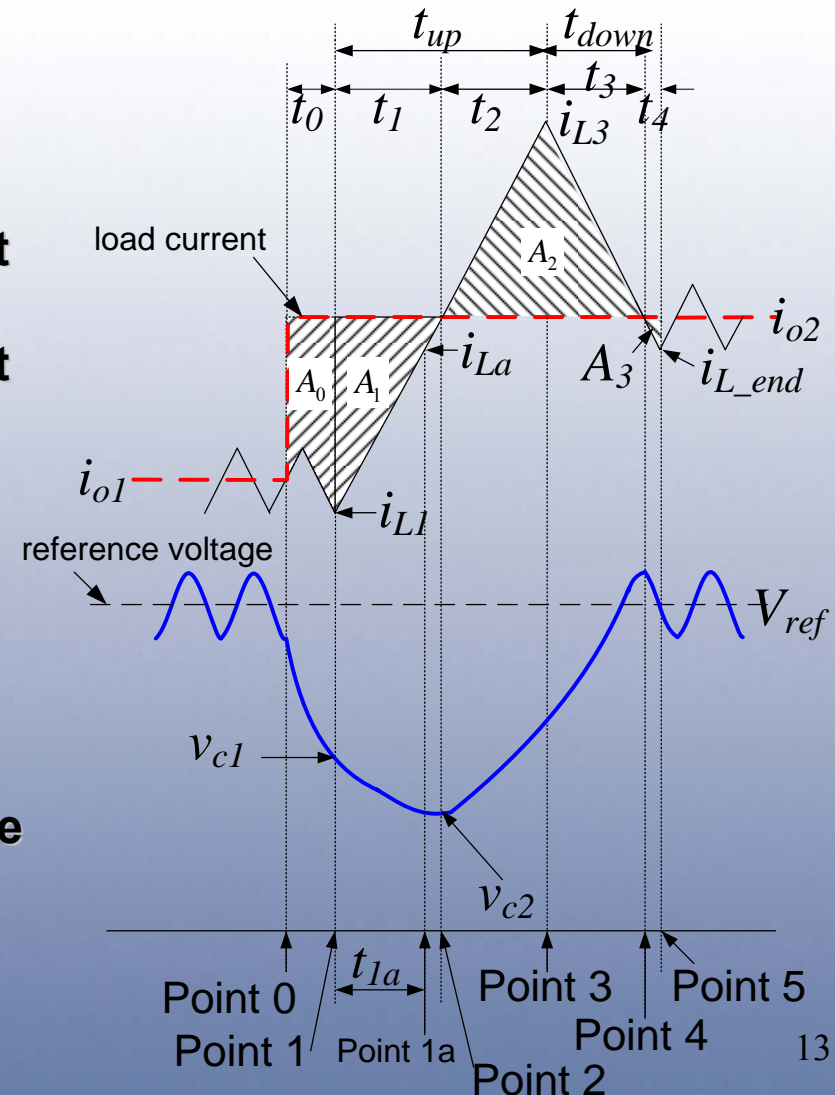
t_1 already
minimized



Load Current Transient Algorithm

- Six key steps after sensing large signal transient condition:**

1. Estimate the new load current i_{o2}
2. Calculate the inductor current rising and falling slew rates
3. Calculate the capacitor discharge portion A_0
4. Calculate t_1 and the capacitor discharge portion A_1
5. Calculate t_4 and the capacitor discharge portion A_3
6. Calculate the capacitor charge portion A_2 and the time periods t_2 and t_3

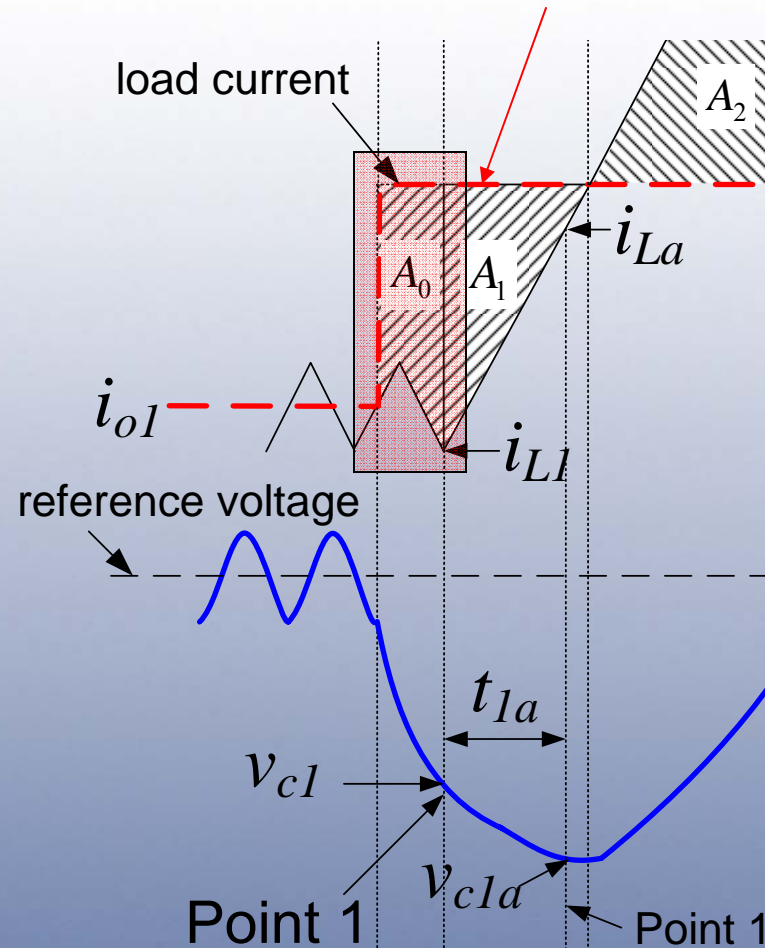


Estimate New Load Current & Estimate A_0

- i_{o2} and A_0 can be estimated by observing the output voltage response and knowing C and ESR

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{La}) - \frac{C \cdot (v_{0a} - v_{o1}) - C \cdot (i_{La} - i_{L1}) \cdot ESR}{t_{1a}}$$

$$A_0 = C \cdot (V_{ref} - v_{o1} + (i_{L1} - i_{o2}) \cdot ESR)$$



Calculate A_1 , A_3 , t_1 , t_3

- A_1 , A_3 , t_1 , t_3 can be simply calculated geometrically by knowing the slew rates of the inductor current

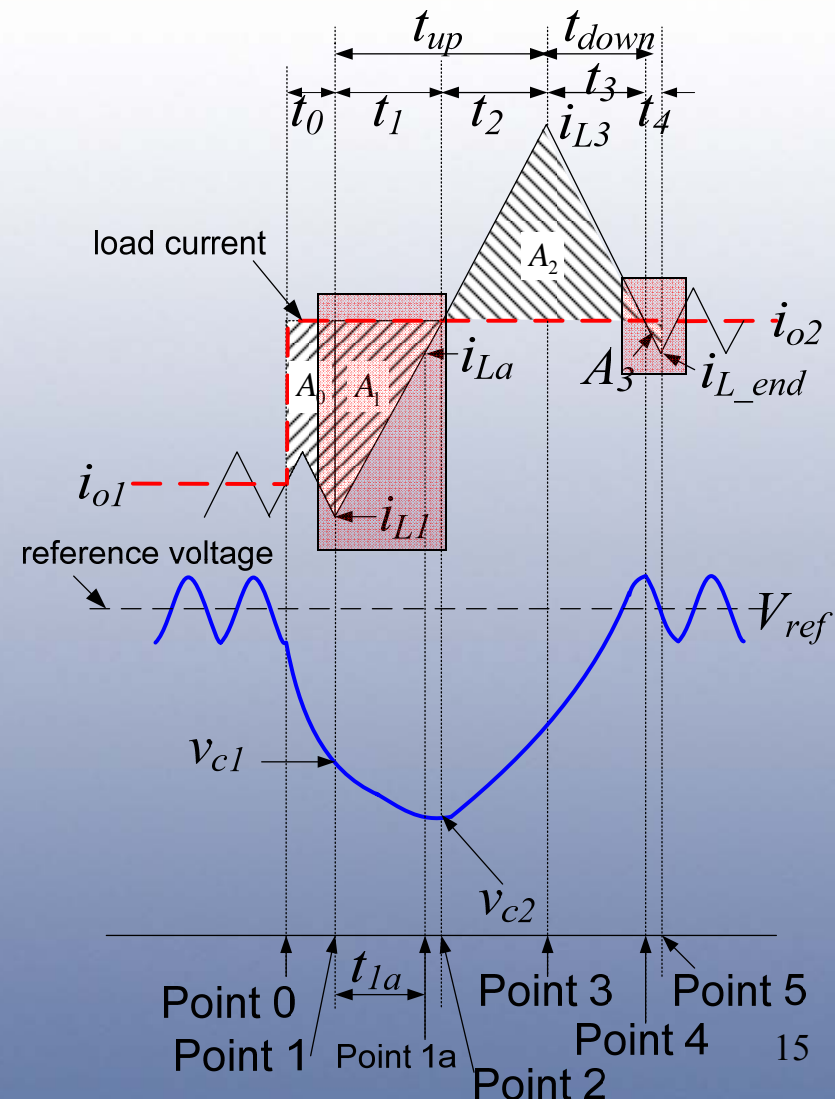
$$t_1 = (i_{o2} - i_{L1}) / \left(\frac{v_{in} - v_o'}{L} \right)$$

$$A_1 = \frac{1}{2} * t_1 * (i_{o2} - i_{L1})$$

$$t_4 = (i_{o2} - i_{L_end}) / \left(\frac{L}{v_o'} \right)$$

$$A_3 = \frac{1}{2} * t_4 * (i_{o2} - i_{L_end})$$

9/3/2006



Balance the Charges

$$A_{\text{discharge}} = A_{\text{charge}}$$

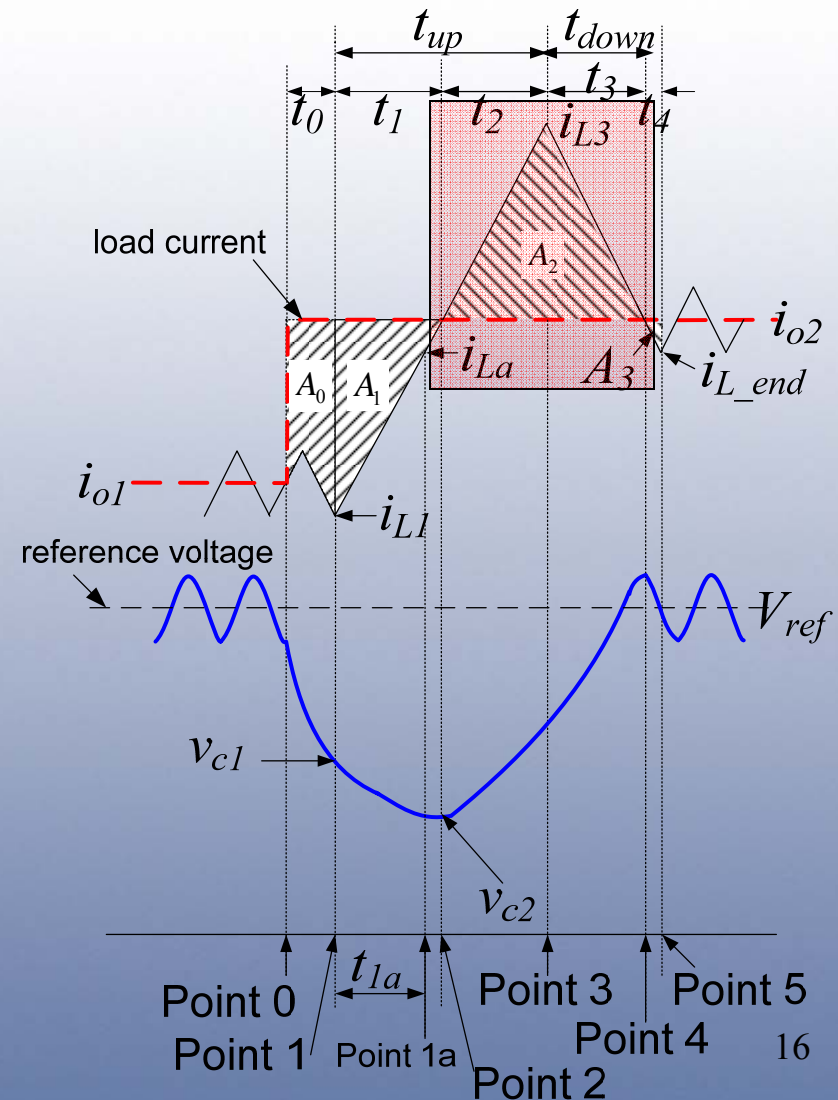
$$A_0 + A_1 + A_3 = A_2$$

- Can now calculate A_2 , t_2 , t_3
- The optimal path is calculated

$$t_2 = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2} \frac{v_{in}}{v_o'} \frac{v_{in} - v_o'}{L}}}$$

$$t_3 = \frac{v_{in} - v_o'}{v_o'} t_2$$

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Other Considerations



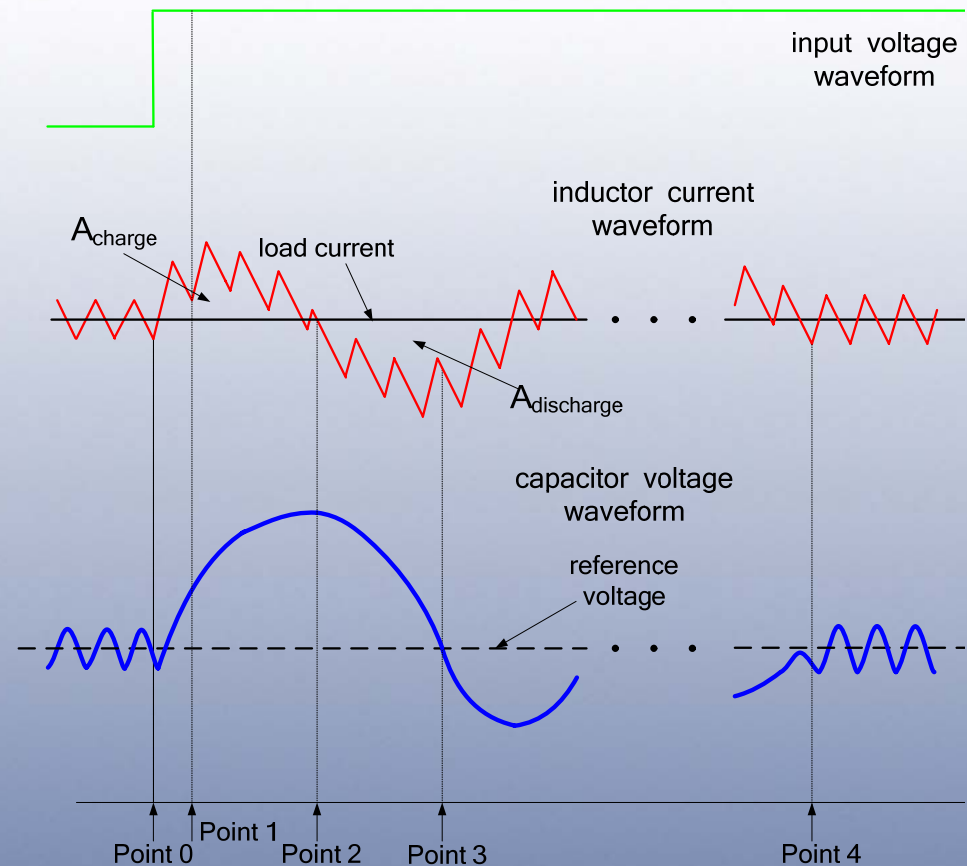
- The aforementioned derived equations are designed for a positive load current step
 - For a negative load current step, the derivation is similar
- Before completion, algorithm calculates the new steady state duty cycle d and inductor current i_L to be passed to the PID current-mode controller
 - Allows for a smooth transition

4. Input Voltage Transient

Digital Current-mode PID controller: Poor Audiosusceptibility

- **Point 0: Input voltage change**
- **Point 1: Controller slowly decreases duty**
- **Point 2: Inductor current equal load current**
- **Point 3: Output voltage recovered**
 - Inductor current < Load current
- **Point 4: Converter “recovered”**

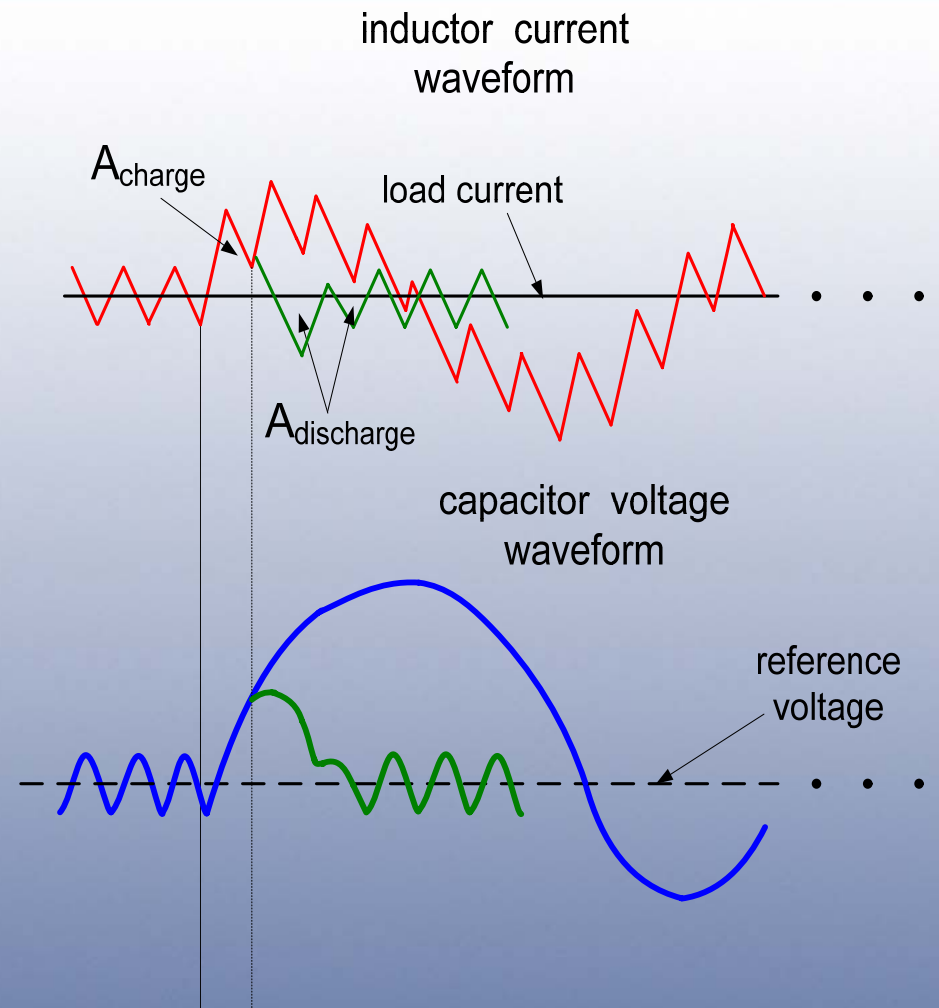
How can we improve this response?



Input Voltage Transient Optimized

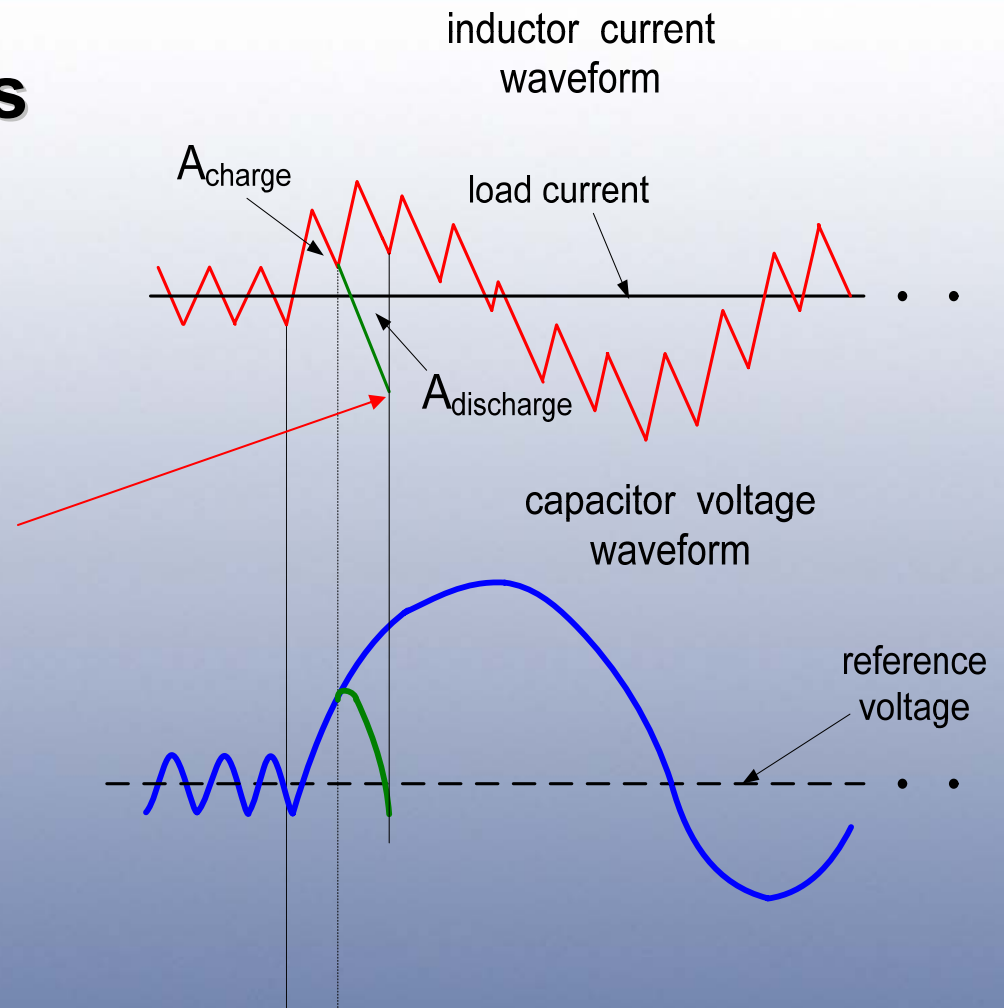


- **Directly detect input voltage transient**
- **Calculate two duty cycles that will balance charges when inductor current reaches steady state value**
- **Minimizes voltage overshoot and settling time**



Why 2 cycles?

- **Not enough degrees of freedom in one cycle to:**
 - **Balance charges**
AND
 - **Ensure inductor current = steady state value**



Input Voltage Transient Algorithm

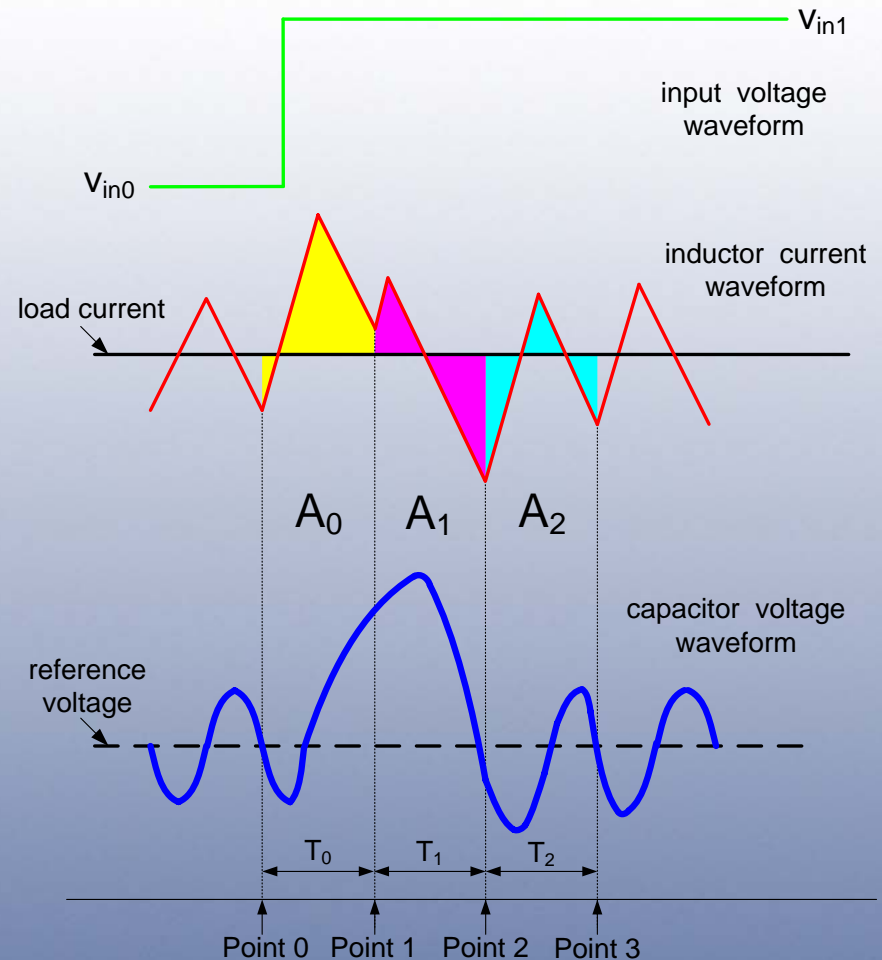


- Charge Portion A_0 (Yellow T_0)
 - Net charge before algorithm activates
- Charge Portion A_1 (Pink T_1)
- Charge Portion A_2 (Cyan T_2)

Goal of Algorithm:

Ensure inductor current at steady-state value at Point 3

$$A_0 + A_1 + A_2 = 0 \text{ at Point 3}$$



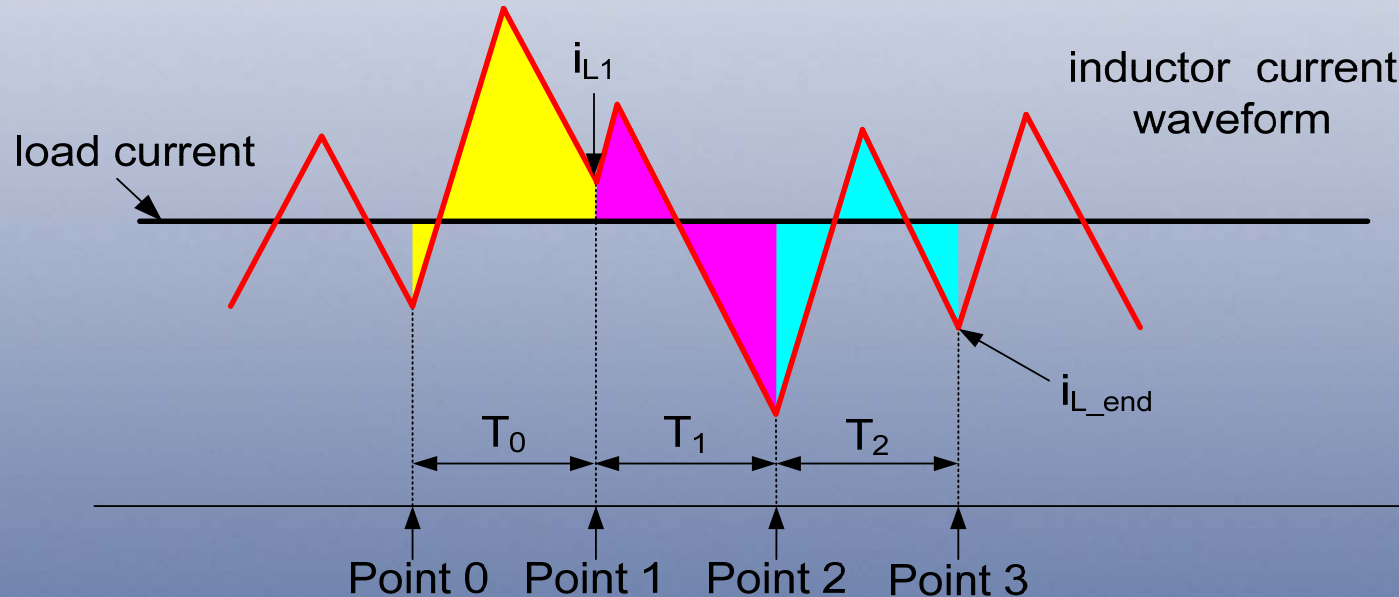
Input Voltage Transient Algorithm



- i_{L_end} known
Relationship between
 i_{L1} , i_{L_end} , d_1 and d_2

$$i_{L_end} - i_{L1} = (d_1 v_{in1} - v_o') \frac{T_s}{L} + (d_2 v_{in1} - v_o') \frac{T_s}{L}$$

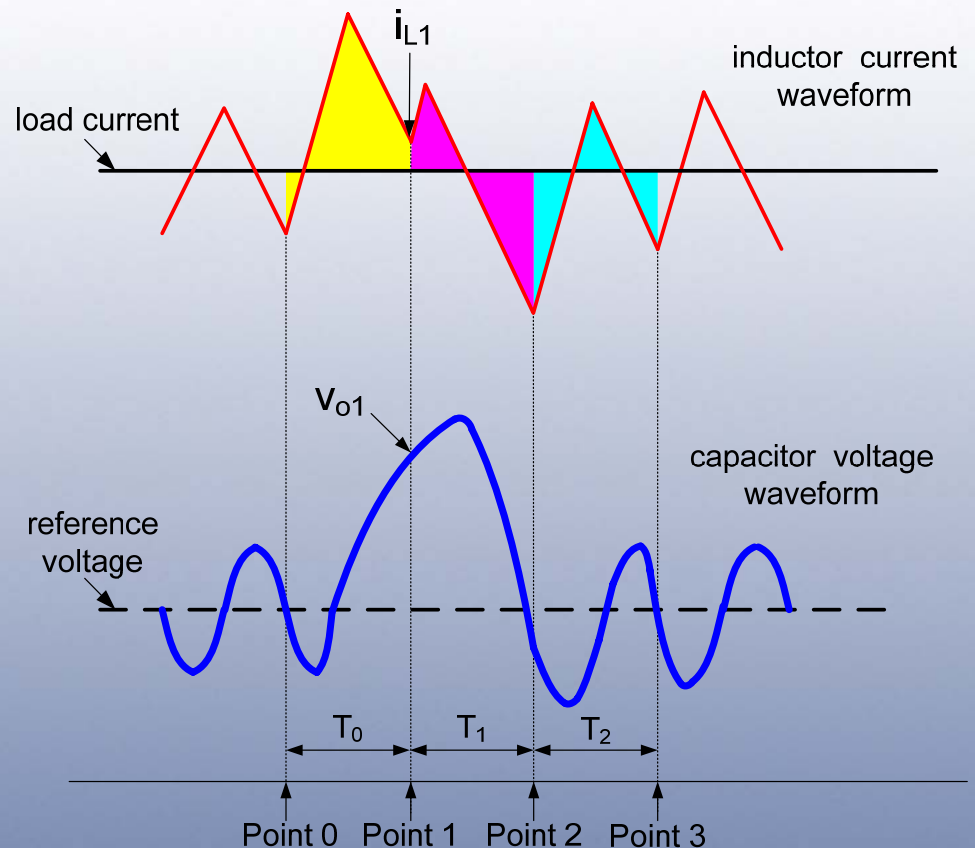
$$k = d_1 + d_2 = \frac{(i_{L_end} - i_{L1}) \cdot \frac{L}{T_s} + 2 \cdot v_o'}{v_{in1}}$$



Charge Area A_0

As before, A_0 is estimated by observing the variation of output voltage from *Point 0* to *Point 1*

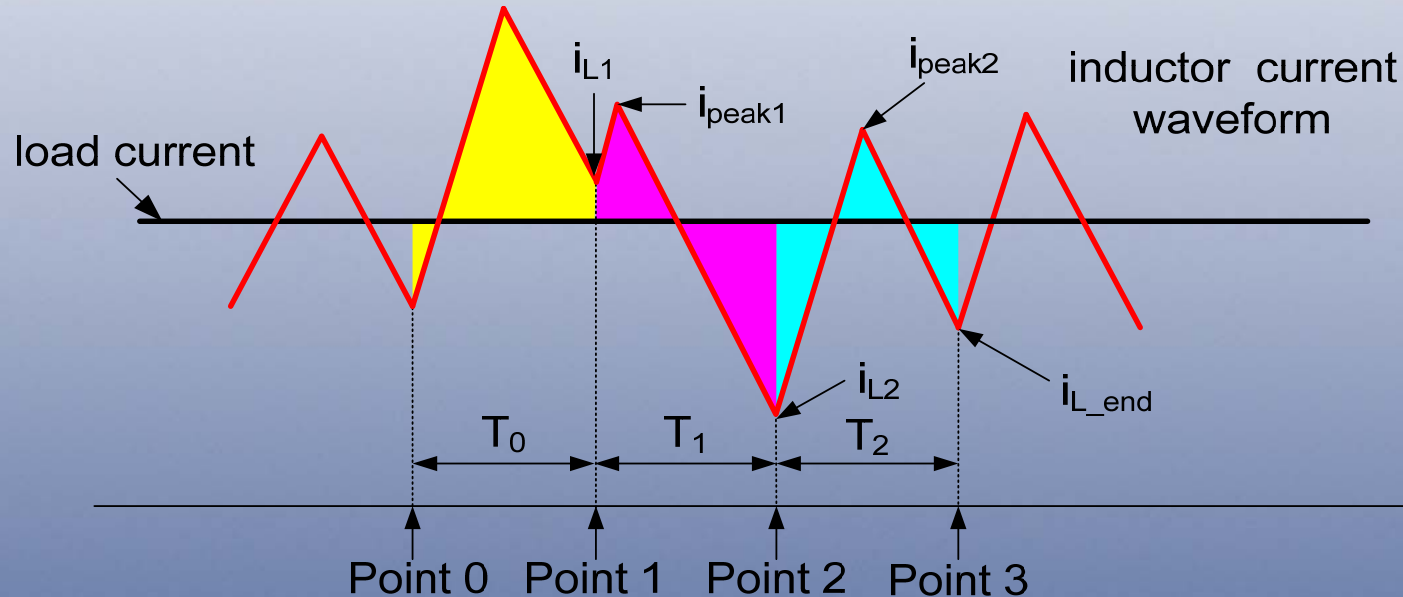
$$\begin{aligned}
 A_0 &= C \cdot (v_{C1} - v_{C0}) \approx C \cdot (v_{C1} - V_{ref}) \\
 &= C \cdot (v_{o1} - i_{C1} \cdot ESR - V_{ref}) \\
 &= C \cdot (v_{o1} - (i_{L1} - i_o) \cdot ESR - V_{ref})
 \end{aligned}$$



A_1 and A_2

$$A_1 = \frac{1}{2} d_1 T_s \cdot [(i_{L1} - i_{L2}) + (i_{peak1} - i_{L2})] + \frac{1}{2} (1 - d_1) T_s \cdot (i_{peak1} - i_{L2}) - (i_o - i_{L2}) T_s$$

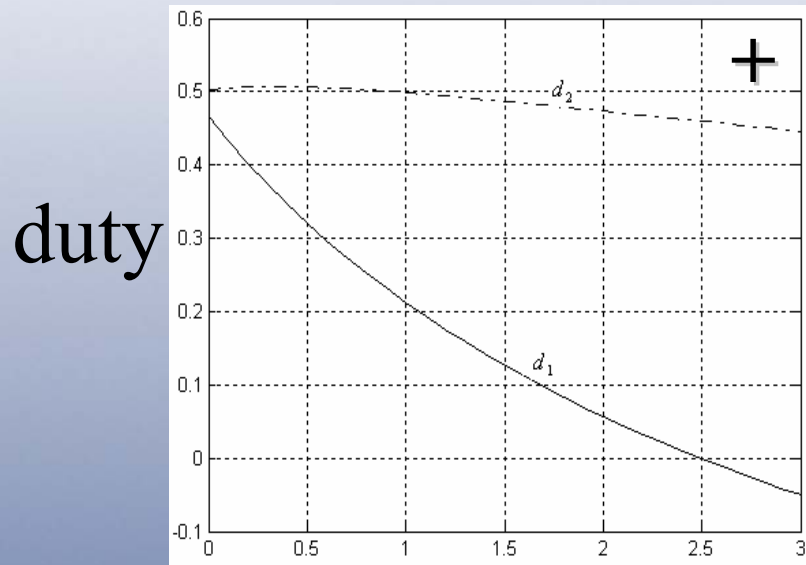
$$A_2 = \frac{1}{2} d_2 T_s \cdot (i_{peak2} - i_{L2}) + \frac{1}{2} (1 - d_2) T_s \cdot [(i_{peak2} - i_{L2}) + (i_{L_end} - i_{L2})] - (i_o - i_{L2}) T_s$$



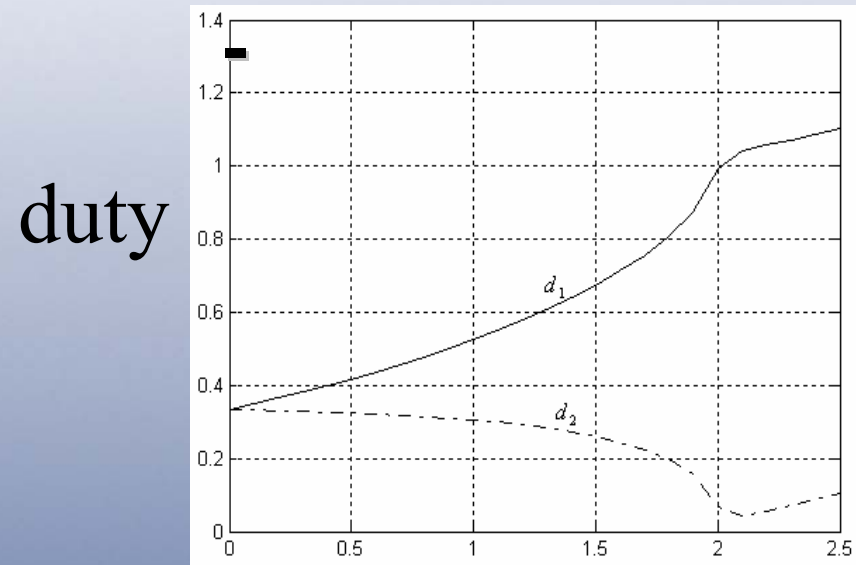
Duty Cycles

$$d_1 = \frac{1}{2} \left[(1+k) - \sqrt{(1+k)^2 + \frac{4L}{v_{in1} \cdot T_s} (i_{L1} - 2i_o + i_{L_end} - \frac{1}{2} k^2 v_{in1} \frac{T_s}{L} + \frac{A_{charge0}}{T_s})} \right]$$

$$d_2 = k - d_1$$



Positive ΔV_{in}



Negative ΔV_{in}

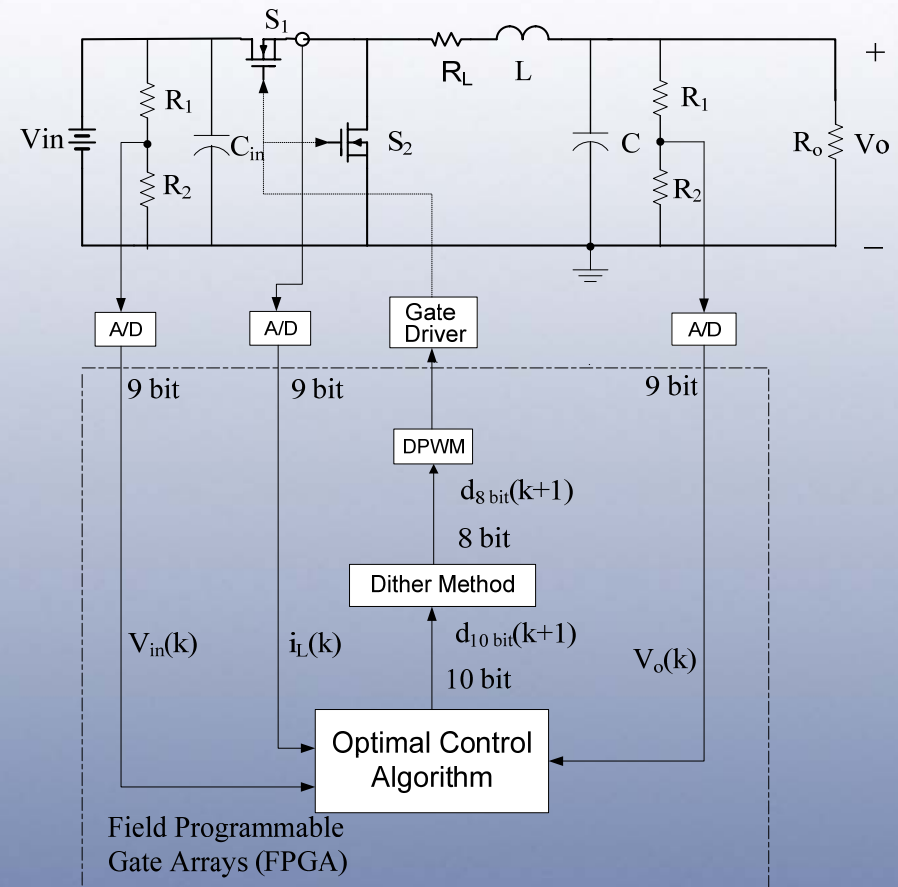
Other Considerations



- The aforementioned derived equations are designed for a positive load current step
 - For a negative load current step, the derivation is similar
- Before completion, algorithm calculates the new steady state duty cycle d to be passed to the PID current-mode controller
 - Allows for a smooth transition
- “Slow” input voltage variations

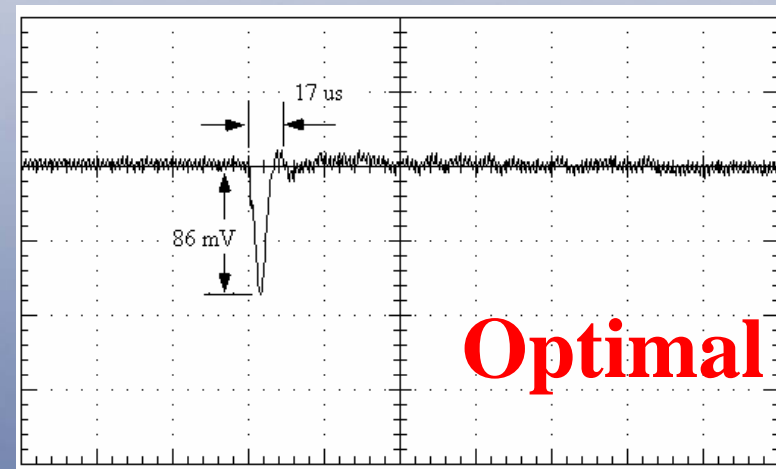
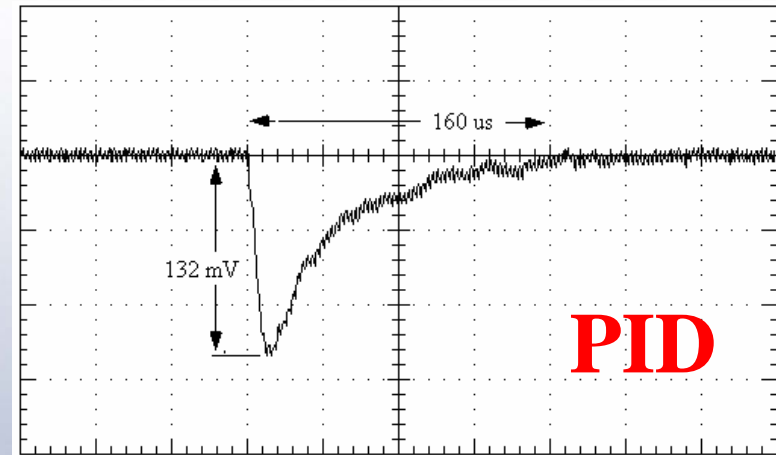
5. Experimental Results

- **Prototype:**
 - $L = 1\mu\text{H}$
 - $C = 235\mu\text{F}$
 - $\text{ESR} = 1\text{m}\Omega$
 - $R_L = 2\text{m}\Omega$
 - $f_s = 400\text{kHz}$
- **Current-mode PID controller:**
 - $f_o = 70\text{ kHz}$
 - Phase margin: 50°



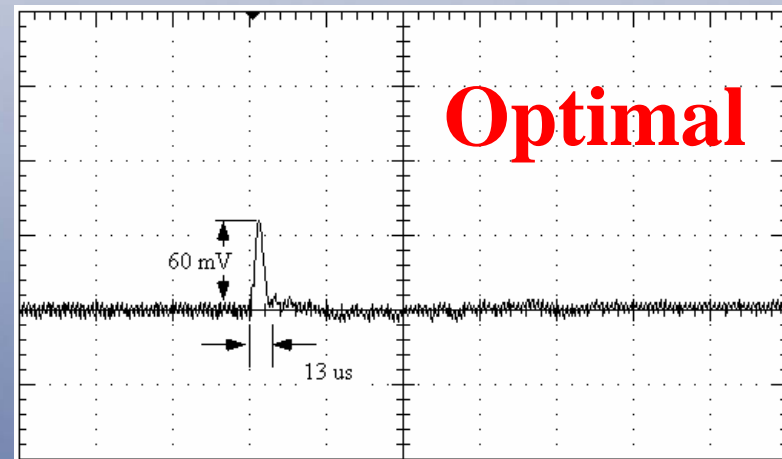
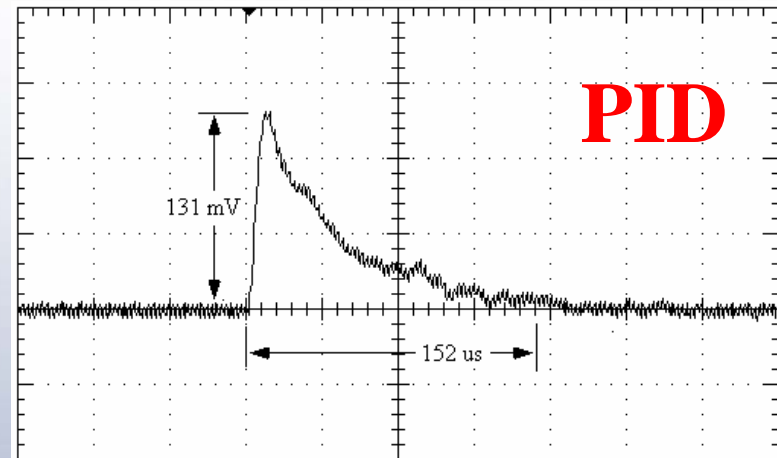
Load Current Step Response

- $V_{in} = 5V$, $V_{out} = 2.5V$
- Load Current: $5A \rightarrow 10A$
- X-axis: $40\mu s/div$
- Y-axis: $50mV/div$
- Undershoot: 35% reduction
- Settling Time: 89% reduction



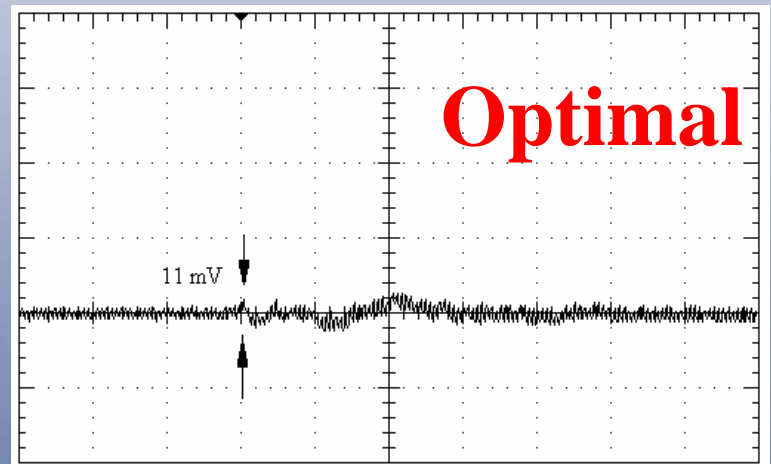
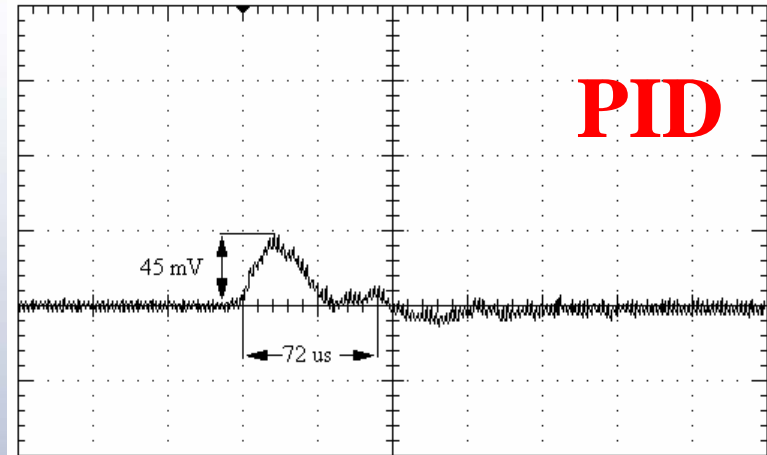
Load Current Step Response

- $V_{in} = 5V$, $V_{out} = 2.5V$
- Load Current: $10A \rightarrow 5A$
- X-axis: $40\mu s/div$
- Y-axis: $50mV/div$
- Overshoot: 54% reduction
- Settling time: 91% reduction



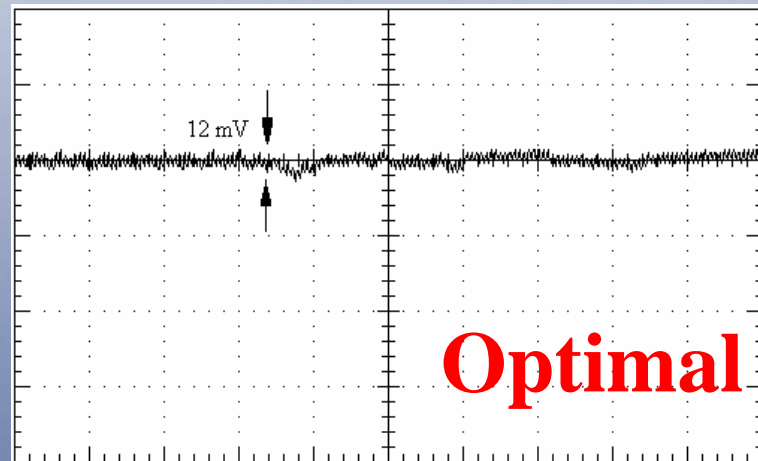
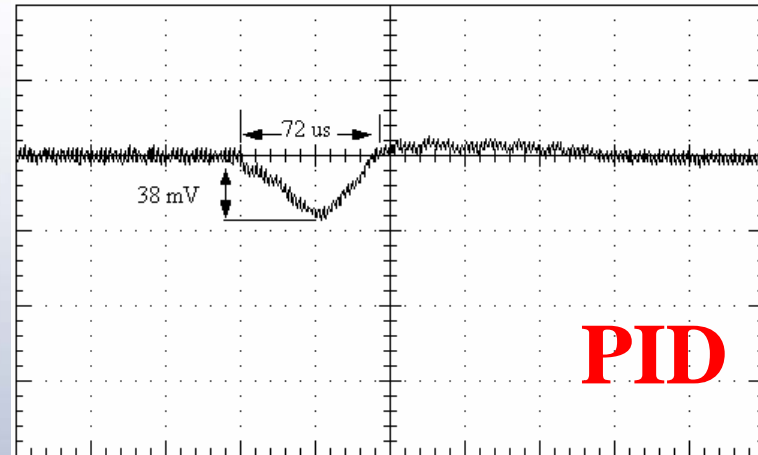
Input Voltage Step Response

- Load Current = 5A
- Input Voltage: 5V \rightarrow 7.5V
- X-axis: 40us/div
- Y-axis: 50mV/div
- Overshoot: 75% reduction
- Settling time: 83% reduction



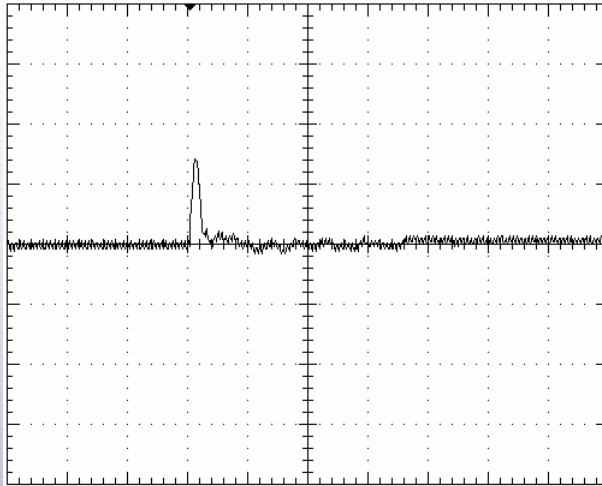
Input Voltage Step Response

- Load Current = 5A
- Input Voltage: 7.5V \rightarrow 5V
- X-axis: 40us/div
- Y-axis: 50mV/div
- Undershoot: 68% reduction
- Settling time: 83% reduction

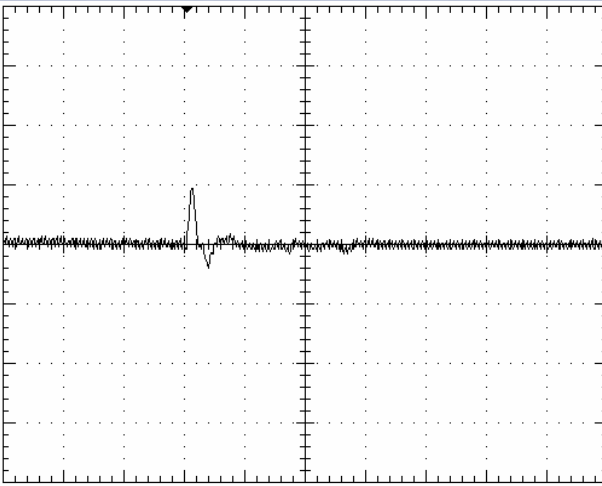


Tolerance Sensitivity

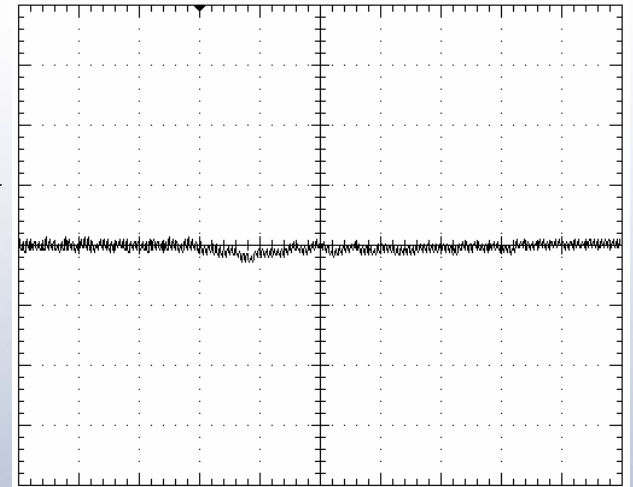
$C = -20\%$
 $I_o =$
 $10A \rightarrow 5A$



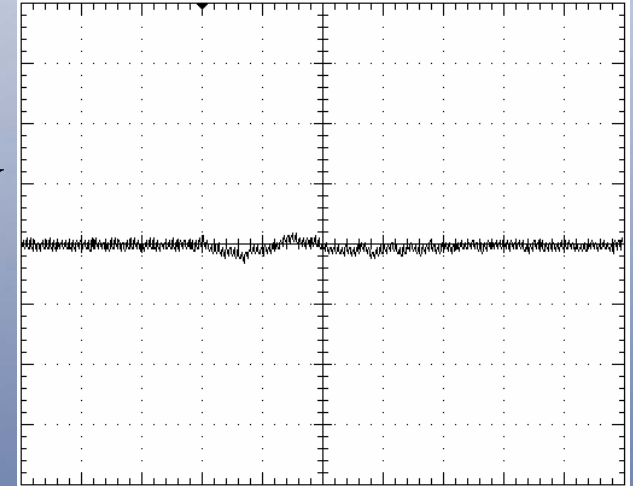
$L = -20\%$
 $I_o =$
 $10A \rightarrow 5A$



$C = -20\%$
 $V_{in} =$
 $7.5V \rightarrow 5V$



$L = -20\%$
 $V_{in} =$
 $7.5V \rightarrow 5V$



6. Conclusion



- **By focusing on balancing capacitor charges during transient periods, dynamic response can be optimized**
- **Experimental results show substantial improvement over conventional methods**
- **Low sensitivity to parameter tolerance**

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