Single-stage LED Driver Achieves Electrolytic Capacitor-less and Flicker-free Operation with Unidirectional Current Compensator

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***Abstract*—AC-connected LED drivers experience imbalanced energy between input and output in a half line cycle. To achieve flicker-free operation the imbalanced energy needs to be buffered, often by energy-dense electrolytic capacitors. However, electrolytic capacitors are also well-known for their short lifespan. These capacitors are the limiting factor of an LED drivers' lifespan. High voltage film capacitors and a Buck converter have been used in the proposed LED driver to buffer the imbalanced energy. When Pin> PLED the extra energy is transferred from the AC input directly to the high voltage film capacitors. When Pin< PLED energy is transferred from the high voltage film capacitors to the output by the Buck converter. The imbalanced energy goes through two power conversion steps in the proposed LED driver, which is one time less than other comparable electrolytic capacitor-less designs, enabling higher efficiency to be achieved. A 28W Flyback topology based experimental prototype had been built and tested to verify the proposed design.**

***Index Terms*—Energy buffering, Electrolytic capacitor-less, flicker-free operation, AC-connected LED driver, high power factor.**

I. Introduction

Light Emitting Diodes (LEDs) are a great technological advancement in the lighting industry and have the potential to fundamentally change the future of lighting. They offer numerous advantages over conventional incandescent, neon and fluorescent lighting devices; most notably their extended lifespan, reduced energy consumption, and low maintenance requirements. The potential energy savings offered by LED lighting is phenomenal. It is estimated that LED lighting could save 348 trillion watts hours of electricity per year by 2027, which equates to the power generated by 44 large power plants, and more than 30 billion USD at today's electricity prices [1]. LED lighting fixtures are rapidly expanding into many applications as their price continues to fall. The global LED lighting market hit 26.09 billion USD in 2016 and is expected to reach 54.28 billion USD by 2022, with an annual growth rate as high as 13% between 2017 and 2022 [2].

An LED driver is the interface between a power source and an LED load, and is required to achieve proper operation. The LED driver is a critical component in an LED lighting fixture and ultimately determines the cost, size, reliability and light quality. Advancements in LED driving technology has a great impact on the widespread adoption of LED lighting. Although using LED lighting offers significant advantages, the design of LED drivers can be very challenging. This is especially true when dealing with an AC-connected LED driver, where a great deal of rigorous industry standards and regulations kick in. For example, EnergyStar requires power factor correction (PFC) implementation with AC-connected LED drivers. They should have a PF higher than 0.7 for residential usage and 0.9 for commercial usage. In addition, there is also IEC61000-3-2 that imposes limitations on input harmonic currents. To meet these requirements, active power factor correction technology is usually implemented with AC-connected LED drivers. As a result, the input power becomes a time varying waveform and there is an imbalanced energy between input and output in a half line cycle, as shown in Fig. 1. The imbalanced energy leads to many technical challenges that are a driving force behind today's LED lighting research.

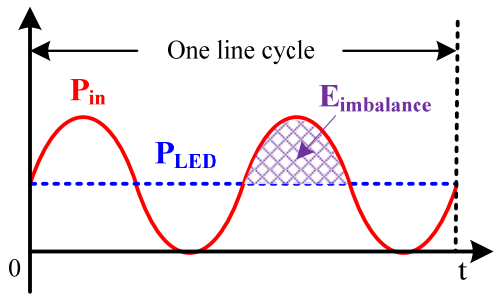

Fig. 1. Energy imbalance between input and output in an AC-connected LED driver

In a conventional LED driver, the imbalanced energy is buffered by electrolytic capacitors, which are connected at the output of a PFC stage. This also leads to the generation of a double-line-frequency ripple voltage at the PFC output. For a single stage LED driver, the PFC is the only power stage and, therefore, the ripple voltage is directly applied to its LED load.

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The ripple voltage will produce a significant double-line-frequency ripple current as an LED load has very low intrinsic resistance. The ripple current presents itself as light fluctuation – commonly called flicker. Although double-line-frequency flicker is usually not visible, it has been linked to several serious health issues, such as headaches, fatigue and even seizures [3]. Two-stage LED drivers are often used to achieve flicker-free operation. In a two-stage driver the ripple voltage from a PFC output is filtered by a second stage converter. This converter removes the double-line-frequency ripple, providing a DC LED voltage at the output of the second stage converter to achieve flicker-free operation. The two main drawbacks of two-stage LED drivers are extra power loss from the second power stage, which generally results in lower efficiency, and higher component count. For example, in a two-stage design with the first stage being a Flyback PFC and the second stage being a Buck converter, the extra loss generated by the Buck converter will reduce the overall efficiency. It is possible to achieve high efficiency with a two-stage design, such as a Boost PFC and an LLC converter, however, due to the high expensive component count this solution is usually adopted for much higher power applications [27], [28] where the cost is not a critical concern.

In addition to avoiding flicker, extending the lifespan of LED drivers is also paramount. Electrolytic capacitors are often used in conventional designs to buffer the double-line-frequency imbalanced energy. The drawback of using electrolytic capacitor is their limited lifespan. Although the life of electrolytic capacitors can vary based on the operating temperature and ripple current, it is usually in the range of 1,000 ~ 10,000 hours [4]. The electrolyte gradually dissipates in electrolytic capacitors and capacitance will be reduced over time. LEDs, however, are semiconductor chips that can achieve several decades of lifespan. Therefore, it is critical to eliminate electrolytic capacitors in LED driver designs to achieve significant lifespan extension of LED lighting fixtures.

A variety of LED driving methods had been proposed attempting to reduce flicker, improve efficiency, reduce cost and eliminate electrolytic capacitors. These previous LED driving methods can be broadly categorized as follows:

1) Input harmonic currents injection methods [5] & [6]. Higher order harmonic currents are added to the fundamental AC input current to reduce the imbalanced energy in a half line cycle. Using this technique, the double-line-frequency ripple voltage at the output of a single-stage LED driver can be reduced as well as flicker.

2) Two-stage integrating methods [7]-[9]. The first stage PFC and the second stage DC-DC converter are combined to share power components. These technologies can reduce cost, but sharing components introduces additional constraints on design and operation which may be unsuitable in certain applications.

3) Ripple voltage cancellation methods [10]-[15]. An opposite ripple voltage is generated and used to cancel the double-line-frequency ripple voltage produced by the main PFC stage of an LED driver. A DC LED voltage can be produced and applied to an LED load to achieve flicker-free LED driving.

4) Active filtering and three-port methods [16]-[18]. The imbalanced energy between the AC input and the LED output are buffered by the film capacitors. A bi-directional DC-DC converter is used to transfer the imbalanced energy between the main circuit and the film capacitors.

5) And other LED driving methods that do not fall into the above categories, such as the output current shaping LED driver [19], the two parallel inverted Buck converter average current modulation LED driver [20], the averaged LED current modulation method [21], the stacked switch capacitor LED driver [22], the valley-fill LED driver[23]-[25] and the one and a half stage LED driver [26]. The topology presented in [26], also shown in Fig. 2, may look similar to the topology proposed in this paper, however, it is operated in a very different way. For the topology in [26] in every switching cycle, the energy from the AC input is delivered to the main output capacitor C_o and the storage capacitor C_{sto}. For this topology the energy transfer process between the two paths is not controllable. In other words, the energy that needs to be buffered cannot be controlled, leaving a significant double-line-frequency output ripple voltage on the LED load, as evidenced in the paper. On the contrary, a key feature of the proposed LED driver, which is illustrated in Fig. 5, is that the amount of energy being delivered to either C_o or C_{sto} can be well controlled by operating two switches, S1 and S2. Therefore, precise energy buffering can be achieved so that the instantaneous output power is always a constant.

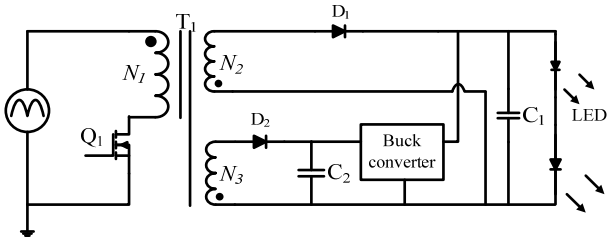

Fig. 2 LED driving method proposed in [26]

In this paper, a unidirectional current ripple compensator LED driver is proposed to eliminate electrolytic capacitors as well as achieve high power factor, flicker-free LED driving. This converter also offers superior efficiency compared to previous electrolytic capacitor-less design. A 28W experimental prototype had been built and tested to verify the operating principles. The remainder of this paper is arranged as follows. The concept of the proposed LED driver is derived in Section II. The circuit implementation and detailed operating principle are discussed in Section III. The control strategy is discussed in Section IV and the design analysis is discussed in Section V. Experimental results are discussed in Section VI and the paper is concluded in Section VII.

II. Idea Of Unidirectional Current Ripple Compensator

Fig. 3 shows the key power waveforms of two existing energy buffering LED drivers. The input power, Pin, is a time-varying waveform with its average being equal to the LED output power, PLED. The buffered power, P_{buffer}, which is handled by the bi-directional converters in Fig. 3(b) & (c), is the difference between P_{in} and P_{LED}. Fig. 3(b) shows the

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implementation of an active filtering LED driver. A bi-directional DC-DC converter is paralleled to the LED load to process imbalanced energy and buffers it with the storage capacitor C_{sto}. Fig. 3 (c) shows the implementation of a three-port LED driver. A dedicated port is used to interfacing with the bi-directional converter to achieve energy buffering. Although the above two methods utilize different circuit implementations and control strategies, in both cases the imbalanced energy must go through no less than three power conversion steps.

When $P_{in} > P_{LED}$, the imbalanced energy is transferred from the AC input to the DC output by the main PFC in the active filter LED driving method, experiencing the first power conversion step. The energy is then transferred from the DC output to the storage capacitor, C_{sto}, by the bi-directional DC-DC converter; this is the second power conversion step. When Pin < PLED, the imbalanced energy is transferred back from C_{sto} to the LED load by the bidirectional DC-DC converter, experiencing the third power conversion step. In three-port LED drivers the process is similar. C_{sto} is built with a Film capacitor to achieve extended lifespan. The drawback of active filter LED driving or three-port LED driver methods is the generation of significant power loss when buffering imbalanced energy. As described above, the imbalanced energy experienced three power conversion steps with the active filtering LED driving method. As a result, the efficiency of an active filtering LED driver or three port LED driver is much lower than a conventional single-stage LED driver. This reduction in efficiency is also evidenced in [16].

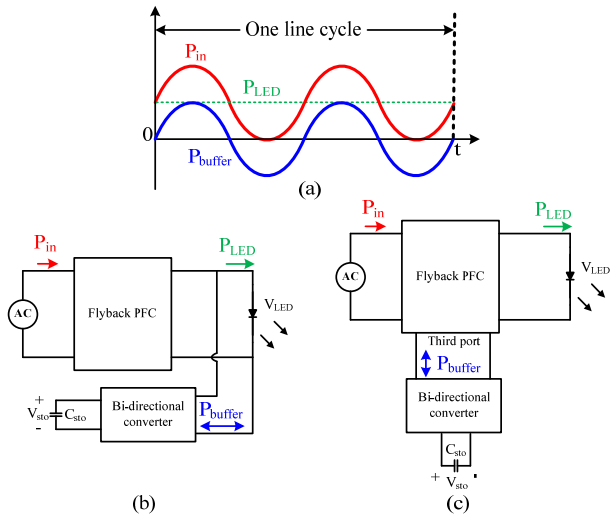

Fig. 3 Previous energy buffering LED driver without electrolytic capacitor, (a) key power waveforms, (b) active filtering LED driver [16], [17], (c) three-port LED driver [18]

The proposed unidirectional current ripple compensator LED driver aims to achieve reduced power conversion loss with the imbalanced energy by restructuring the energy buffering process. The concept of the proposed LED driver is shown in Fig. 4 and the key waveforms in a line cycle are shown in Fig. 5. A Flyback PFC is used at the first stage to achieve a high power factor. Two switches, S_1 and S_2, are used to control the energy flow. When $P_{in} < P_{LED}$, the switch S1 is turned on while S2 is off. In this way, the power delivered to the LED load from AC input, P1, is equal to the input power. At the same time, additional energy will be transferred from C_{sto} to the LED load by the DC-DC converter to make up the difference between Pin and P_{LED}. When $P_{in} > P_{LED}$, by controlling the on time of S1 and S_2 in one switching cycle, the instantaneous AC input power can be split into P1 and P2 with precision. The control circuit design will ensure that P1 = PLED during this condition while the excess energy, P2 = Pin - PLED, from the AC input will be stored in Csto. Under steady state, the energy stored in Csto during $P_{in} > P_{LED}$ is equal to the amount it releases when $P_{in} < P_{LED}$.

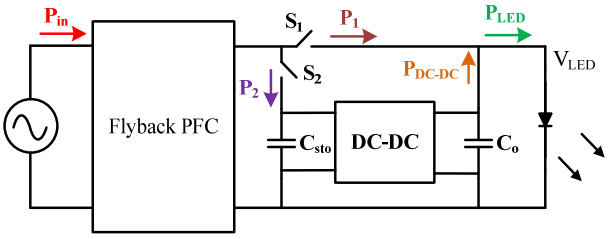

Fig. 4 Concept of the proposed unidirectional ripple current compensation LED driver

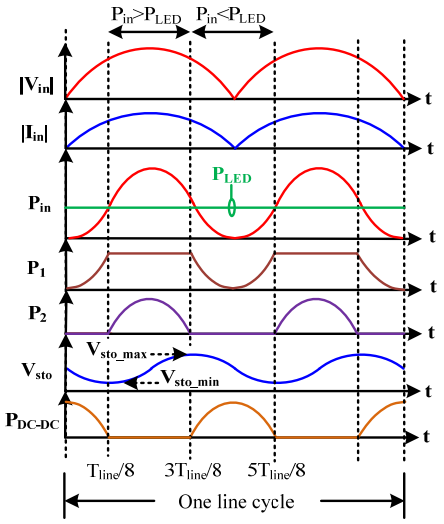

Fig. 5 Key line cycle waveforms of the proposed unidirectional current ripple compensation LED driver

The above description reveals that the imbalanced energy experiences only two power conversion steps in the proposed LED driver. By directly attaching C_{sto} to the main Flyback PFC, the extra energy is directly transferred from the AC input to C_{sto}, when $P_{in} > P_{LED}$, without the extra power conversion process with a bi-directional converter. One less power conversion step is achieved with the imbalanced energy as compared to active filtering LED drivers. The process of transferring energy back from C_{sto} to LED load is the same with the proposed LED driver and the active filtering LED drivers. It should note that the DC-DC converter is unidirectional in the proposed LED driver.

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III. Circuit Implementation And Operating Principle

Fig. 6 shows the circuit implementation of the proposed unidirectional current ripple compensation LED driver. The LED driver includes a main Flyback PFC, a Buck converter and one energy channeling MOSFET, Q_2. In Fig. 4, two switches are needed in the conceptual design to achieve power splitting. By carefully designing the storage capacitor voltage V_{sto}, one MOSFET in the design can be removed while achieving energy splitting. More specifically, to achieve this, the voltage V_{sto} needs to be always higher than V_{LED}. If this condition is met, then when the MOSFET Q_2 is off, the current in the secondary side of the transformer T_1 only flows in D_2, during which energy is delivered the storage capacitor C_{sto}. When Q_2 is turned on, the secondary side current flows in Q_2 and D_1. The voltage across the winding N_{sec} is clamped at V_{LED} (with ignoring the forward voltage drop on D_1 and the voltage difference between the drain and the source terminals of Q_2). Therefore, if $V_{sto} > V_{LED}$, the diode D_2 is reverse biased and blocking any current flow. As shown in Fig. 5, there is a significant ripple voltage on V_{sto} at double line frequency. The average voltage of V_{sto} can be controlled by a voltage loop that will be explained in section IV. By selecting a proper capacitor C_{sto}, the ripple voltage amplitude on V_{sto} can be controlled, which will be explained in section V. The goal is to keep V_{sto_min} higher than V_{LED} to ensure D_2 remains correctly biased. The Flyback PFC shapes the input current to achieve a high power factor and draws energy from the AC input. The Buck converter provides the power difference when $P_{in} < P_{LED}$.

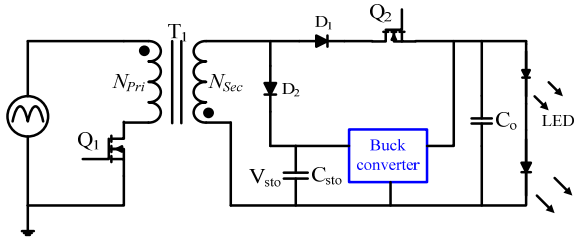

Fig. 6 Circuit implementation of the unidirectional ripple current compensation LED driver

A. Line Cycle Operation

First, the line cycle operation of the proposed LED driver will be discussed and the key waveforms in Fig. 5 will also be derived. Since a high power factor is achieved with proposed LED driver, the input current follows the input voltage. The rectified input voltage, $|V_{in}(t)|$, and the rectified the input current, $|I_{in}(t)|$, can be expressed as:

$$|V_{in}(t)| = V_{in\_pk} \times |\sin(2\pi \times f_{line} \times t)| \tag{1}$$

and

$$|I_{in}(t)| = I_{in\_pk} \times |\sin(2\pi \times f_{line} \times t)| \tag{2}$$

Where f_{line} represents the mains frequency, V_{in_pk} and I_{in_pk} represent the peak input voltage and peak input current amplitude, respectively. Therefore, the input power, Pin(t), can be expressed as:

$$\begin{aligned} P_{in}(t) &= V_{in\_pk} \times \sin(2\pi \times f_{line} \times t) \times I_{in\_pk} \times \sin(2\pi \times f_{line} \times t) \\ &= \frac{1}{2} P_{in\_pk} \times [1 - \cos(4\pi \times f_{line} \times t)] \end{aligned} \tag{3}$$

As indicated in Eq. (3), the input power, P_{in}, is a sinusoidal waveform with a DC bias being equal to half the peak value. Assuming no power loss, the LED output power, P_{LED}, will be equal to the averaged input power and it is a constant. The capacitor C_{sto} is used to buffer the energy difference between the AC input and the LED output. Because the imbalanced energy is buffered by the storage capacitor and leads to voltage change on V_{sto}, the relationship between the imbalanced energy, $E_{imbalance}$, and the voltage change on V_{sto} , ΔV_{sto} , can be expressed as:

$$\begin{aligned} E_{imbalance} &= \frac{1}{2} C_{sto} (V_{sto\_max}^2 - V_{sto\_min}^2) \\ &= C_{sto} (\frac{V_{sto\_max} + V_{sto\_min}}{2})(V_{sto\_max} - V_{sto\_min}) \\ &= C_s \times V_{sto\_avg} \times (\Delta V_{sto}) \end{aligned} \tag{4}$$

In Eq.(4), V_{sto_avg} represents the averaged value of V_{sto} in a half line cycle. The imbalanced energy in a half line cycle can also be calculated as:

$$E_{imbalance} = \frac{1}{\pi} P_{LED} \times \frac{T_{line}}{2} \tag{5}$$

Therefore, once V_{sto_avg} and C_{sto} are determined in a design, the voltage change ΔV_{sto} , as well as the minimum and maximum V_{sto} can be calculated.

From $T_{line}/8$ to $3T_{line}/8$, the input power is higher than the LED output power. The difference between P_{in} and P_{LED}, P_2, is used to charge the storage capacitor C_{sto} and the voltage V_{sto} rises in this period. The instantaneous voltage V_{sto} (t), V_{sto_min}, C_{sto}, P_{in} (t) and P_{LED}, have the following relationship:

$$\begin{aligned} &\frac{1}{2} \times C_{sto} [V_{sto}(t)^2 - V_{sto\_min}^2] \\ &= \int_{\frac{T_{fline}}{8}}^{t} [P_{in}(t) - P_{LED}] dt \\ &\text{When } \frac{T_{line}}{8} < t < \frac{3T_{line}}{8} \end{aligned} \tag{6}$$

During $3T_{line}/8$ to $5T_{line}/8$, P_{in} is lower than P_{LED}. S_1 is fully on so that the P_{in} is equal to P_1. Energy is taken from C_{sto} and the DC-DC converter delivers the difference in power between P_{in} and P_{LED} to the output. Therefore, the voltage V_{sto} falls during this interval. The relationship between V_{sto} (t), V_{sto_max}, C_{sto}, P_{in} (t) and P_{LED}, can be expressed as:

$$\begin{aligned} &\frac{1}{2} \times C_{sto} [V_{sto}(t)^2 - V_{sto\_max}^2] = \int_{\frac{3T_{fline}}{8}}^{t} [P_{in}(t) - P_{LED}(t)] dt \\ &\text{When } \frac{3T_{line}}{8} < t < \frac{5T_{line}}{8} \end{aligned} \tag{7}$$

Combing Eq. (3), (6) and (7), the voltage V_{sto} can be expressed as:

$$V_{sto}(t) = \begin{cases} \sqrt{\dfrac{2 \times \int_{\frac{T_{fline}}{8}}^{t} (\frac{1}{2} P_{in\_pk} \times [1 - \cos(4\pi \times f_{line} \times t)]) dt}{C_{sto}} + V_{sto\_min}^2} & \dfrac{T_{line}}{8} < t < \dfrac{3T_{line}}{8} \\ \sqrt{V_{sto\_max}^2 - \dfrac{2 \times \int_{\frac{3T_{fline}}{8}}^{t} (\frac{1}{2} P_{in\_pk} \times [1 - \cos(4\pi \times f_{line} \times t)]) dt}{C_{sto}}} & \dfrac{3T_{line}}{8} < t < \dfrac{5T_{line}}{8} \end{cases} \tag{8}$$

The power $P_1(t)$, $P_2(t)$ and $P_{DC\text{-}DC}(t)$ can be written as:

$$P_1(t)=\begin{cases} P_{LED} & \frac{T_{line}}{8}<t<\frac{3T_{line}}{8} \\ P_{in}(t) & \frac{3T_{line}}{8}<t<\frac{5T_{line}}{8} \end{cases} \quad (9)$$

and

$$P_2(t)=\begin{cases} P_{in}(t)-P_{LED} & \frac{T_{line}}{8}<t<\frac{3T_{line}}{8} \\ 0 & \frac{3T_{line}}{8}<t<\frac{5T_{line}}{8} \end{cases} \quad (10)$$

and

$$P_{DC-DC}(t)=\begin{cases} 0 & \frac{T_{line}}{8}<t<\frac{3T_{line}}{8} \\ P_{LED}-P_{in}(t) & \frac{3T_{line}}{8}<t<\frac{5T_{line}}{8} \end{cases} \quad (11)$$

The above line cycle operation provides an overview of the proposed unidirectional current ripple compensation LED driver. It is possible to use different topologies to achieve the above discussed operation. The switching operation that is specifically for the proposed LED driver circuit is discussed below.

B. Switching Operation

The Flyback PFC in the proposed LED driver is operated under constant on time, fixed switching frequency, discontinues conduction mode (DCM) to achieve high power factor correction [27]. The design of the Buck converter is very generic. To simplify the discussion, the Buck converter is represented as a function unit and its switching operation is not of interest. The switching operations to achieve energy buffering will be discussed in detail and separately for $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$.

When $P_{in} > P_{LED}$

When $P_{in} > P_{LED}$, the Buck converter is not active. One switching cycle is divided into four time intervals, $[t_0\text{-}t_1]$, $[t_1\text{-}t_2]$, $[t_2\text{-}t_3]$ and $[t_3\text{-}t_4]$. Fig. 7 shows the switching operation of each time interval and Fig. 8 shows the key switching waveforms.

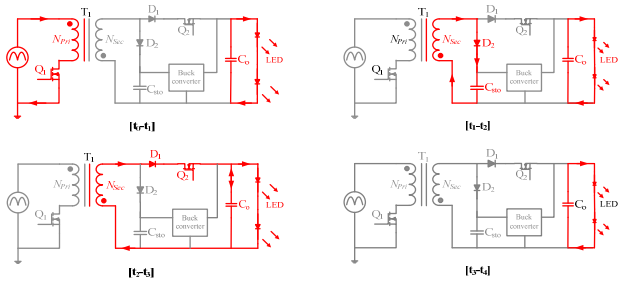

Fig. 7 Switching operation of the LED driver when Pin > PLED (Q2 under leading edge modulation)

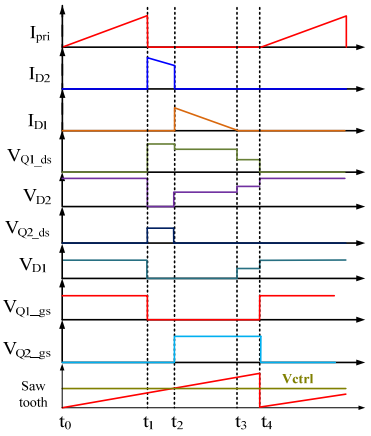

Fig. 8 Key switching waveforms of the proposed LED driver when Pin > PLED (Q2 under leading edge modulation)

Time interval $[t_0\text{-}t_1]$

One switching cycle starts at time t_0 when Q_1 is turned on. The switching current in winding N_{pri}, I_{pri}, starts increasing from zero. Due to the opposite orientation between the winding N_{pri} and N_{sec}, the diode D_1 and D_2 are reversely biased while the body diode of Q_2 is forward biased. The voltage across the diode D_1 and D_2 can be expressed as:

$$V_{D_1(P_{in}>P_{LED})}[t_0-t_1]=V_{LED}+V_{in}\times\frac{N_{sec}}{N_{pri}} \quad (12)$$

and

$$V_{D2(P_{in}>P_{LED})}[t_0-t_1]=V_{sto}+V_{in}\times\frac{N_{sec}}{N_{pri}} \quad (13)$$

This interval ends at time t1 when the main MOSFET Q1 is turned off. The switching current in Q1 at time t1 can be expressed as:

$$I_{Q_1\_t_1(P_{in}>P_{LED})}=\frac{V_{in}\times(t_1-t_0)}{L_{pri}} \quad (14)$$

The averaged input current in this switching cycle can be expressed as:

$$I_{in\_avg}=\frac{I_{Q_1\_t_1(P_{in}>P_{LED})}\times(t_1-t_0)}{2\times T_s}=\frac{V_{in}\times(t_1-t_0)^2}{2\times T_s\times L_{pri}} \quad (15)$$

Eq. (15) indicates that the average input current follows the input voltage when $(t_1\text{-}t_0)$ and the switching cycle, T_s, are constant in a half line cycle.

Time interval $[t_1\text{-}t_2]$

As Q_1 is turned off at time t_1, the magnetic current commutes from the primary side winding to the secondary side winding. The MOSFET Q_2 is still off so that the magnetic current flows in diode D_2. The energy stored in the transformer is transferred to the capacitor C_{sto}. The voltage across the winding N_{sec} is clamped at V_{sto} and reflected to the primary side. The voltage across the drain to source of Q_1 can be expressed as:

$$V_{Q_1(P_{in}>P_{LED})}[t_1-t_2]=V_{in}+V_{sto}\times\frac{N_{pri}}{N_{sec}} \quad (16)$$

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When D_2 is conducting, the voltage at the anode of diode D_1 is equal to V_{sto} (ignoring the voltage drop of D_2). Since V_{sto} is higher than V_{LED}, which is ensured by the design, the diode D_1 is therefore forward biased while the body diode of Q_2 is reverse biased. The voltage across the drain to source of Q_2 can be expressed as:

$$V_{Q_2(P_{in}>P_{LED})}[t_1 - t_2] = V_{sto} - V_{LED} \quad (17)$$

This interval ends at t_2 when the MOSFET Q_2 is turned on.

Time interval [t_2-t_3]

The voltage on the secondary side winding is clamped at V_{LED} after Q_2 is on. Since V_{LED} is lower than V_{sto}, the diode D_2 becomes reverse biased and the switching current in D_2 is zero. The voltage across the diode D_2 can be expressed as:

$$V_{D_2(P_{in}>P_{LED})}[t_2 - t_3] = V_{sto} - V_{LED} \quad (18)$$

The voltage on the secondary side winding is reflected to the primary side winding and the voltage on Q_1 during this time interval can be expressed as:

$$V_{Q_1(P_{in}>P_{LED})}[t_2 - t_3] = V_{in} + V_{LED} \times \frac{N_{pri}}{N_{sec}} \quad (19)$$

Eq. (16) and Eq. (19) express the voltage stress on Q_1 during the time interval [t_1-t_2] and [t_2-t_3], respectively. Since V_{sto} is higher than V_{LED}, Q_1 has higher voltage stress during the time interval [t_1-t_2].

During [t_2-t_3], the switching current in winding N_{sec} continues its flow in D_1 and Q_2 and the Flyback transformer releases its remaining energy to the LED load. The switching current in winding N_{sec} drops to zero at time t_3, which ends this time interval.

Time interval [t_3-t_4]

To achieve DCM operation, there is a small-time interval [t_3-t_4] when there is no active switching operation. The switching cycle ends at t_4.

One can also apply leading edge modulation to Q_2 to achieve the same function. Fig. 9 shows the operation when with applying trailing edge modulation to Q_2. Q_2 is turned on before Q_1 is turned off. The secondary side current flows in D_1 and Q_2 when Q_1 is turned off. After Q_2 is turned off, the remaining current is directed to flow in D_2. Fig. 10 shows the critical switching waveforms when applying trailing edge modulation to Q_2. The current stresses for D_1, Q_2, D_2 are different under two modulation schemes. When leading edge modulation is applied to Q_2, the peak secondary side current goes through the diode D_2. By contrast, when trailing edge modulation is applied to Q_2, the peak secondary side current goes through the diode D_1 and Q_2. Under trailing edge modulation, there is no turn on loss with Q_2 since the body diode of Q_2 is forward biased when Q_2 is turned on. Switching loss occurs during turn off of Q_2 when the current in Q_2 is not zero. Under leading edge modulation, there is no turn off loss with Q_2 since the current is already zero when Q_2 is turned off. The switching loss occurs during turn on of Q_2 when the switching current is not zero.

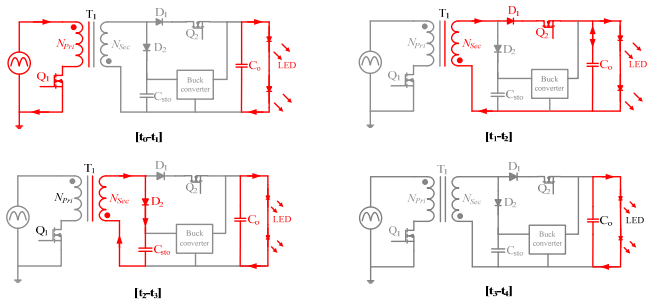

Fig. 9 Switching operation of the LED driver when Pin > PLED (Q2 under trailing edge modulation)

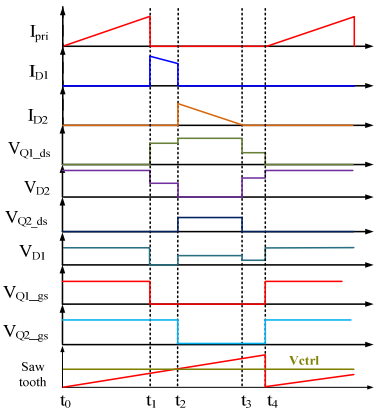

Fig. 10 Key switching waveforms of the proposed LED driver when Pin > PLED (Q2 under trailing edge modulation)

When $P_{in} < P_{LED}$

Fig. 11 shows the switching operation during each time interval when $P_{in} < P_{LED}$ and Fig. 12 shows the key switching waveforms. One switching cycle is further divided into three time intervals [t_0-t_1], [t_1-t_2] and [t_2-t_3]. The MOSFET Q_2 is always on so that $P_{in} = P_1$. The Buck converter is activated, and energy is transferred from C_{sto} back to the LED load. Since $P_{in} < P_{LED}$, the control loop will automatically generate a 100% duty cycle for Q_2. Therefore, the switching operation during $P_{in} < P_{LED}$ can be understood as a special case of the switching operation under $P_{in} > P_{LED}$ and will not be repeated.

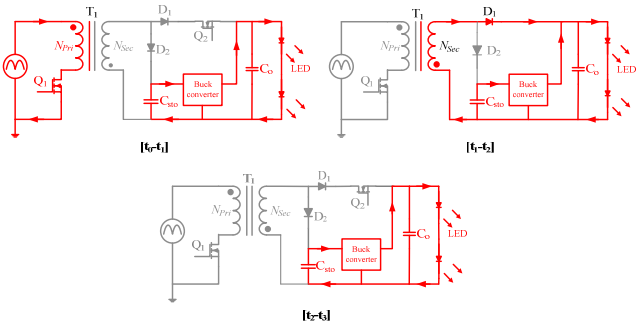

Fig. 11 Switching operation of the proposed unidirectional current ripple compensation L ED driver when Pin < PLED

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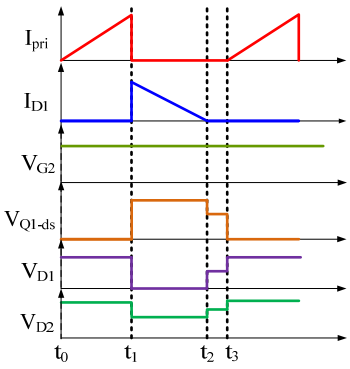

Fig. 12 Key switching waveforms of the proposed unidirectional current ripple compensation LED driver when $P_{in} < P_{LED}$

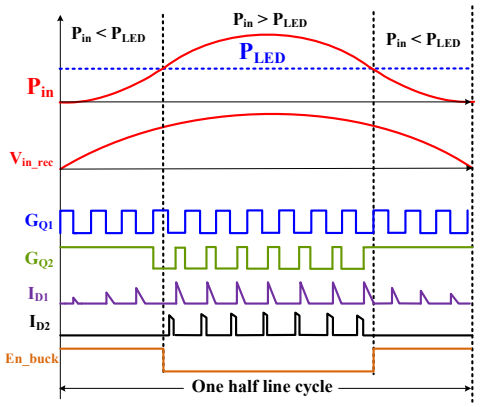

Fig. 13 Switching operation over a half line cycle

Switching operation over half line cycle

As the switching operation during $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ had been discussed, the switching operation under the scale of a half line cycle is illustrated in Fig. 13.

IV. Control Scheme

Fig. 14 shows the control scheme of the proposed unidirectional current ripple compensation LED driver. There are two current regulation loops and one voltage regulation loop in the system to regulate the LED current and the voltage of the storage capacitor, V_{sto}. Although the goal is to buffer the imbalanced energy in every switching cycle, the control is achieved by sensing and regulating currents and voltages.

The current in diode D_1 is sensed and averaged in every switching cycle. The averaged current in D_1, I_{D1_avg}, is then compared with the LED current reference, I_{LED_ref}. If I_{D1_avg} is larger than I_{LED_ref}, the compensated error voltage V_{c2} will be reduced. A reduced V_{c2} will generate a smaller duty cycle for Q_2, which will reduce I_{D1_avg}. When $P_{in} > P_{LED}$, the duty cycle of Q_2 will be controlled to achieve $I_{D1\_avg} = I_{LED\_ref}$. When $P_{in} < P_{LED}$, because I_{D1_avg} is always less than I_{LED_ref}, the feedback loop will turn Q_2 on. When it is detected that the duty cycle of Q_2 is 100%, the Buck converter will be activated. The difference between I_{LED_ref} and I_{D1_avg}, $I_{LED\_ref} - I_{D1\_avg}$, becomes the output current reference of the Buck converter. The current feedback loop of the Buck converter ensures that the current generated by the Buck converter is equal to its reference. Therefore, the current delivered to the LED load under both $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$ can be precisely controlled.

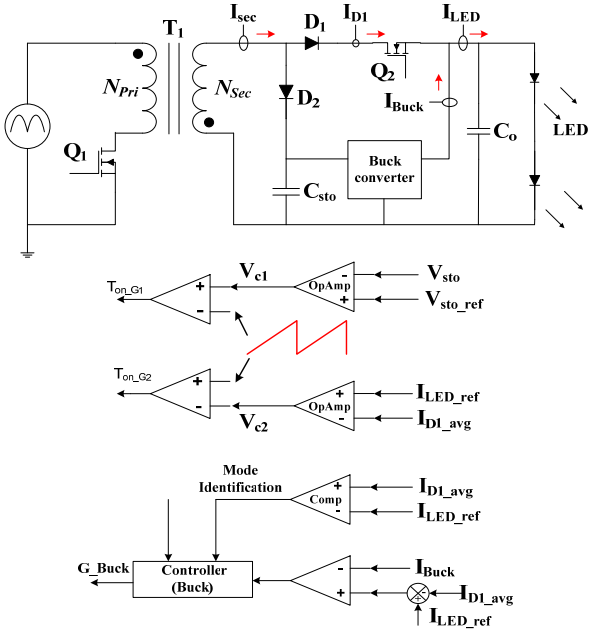

Fig. 14 Control scheme of the proposed unidirectional current ripple compensation LED driver

The average voltage of V_{sto} is controlled as well to serve two purposes. First, net-zero energy storage with C_{sto} can be achieved by controlling the average voltage of Vsto. In a half line cycle, it is expected that the net energy stored in C_{sto} is zero. In this way, the averaged input power is equal to the LED output power. To achieve this, V_{sto_avg} is compared with the reference voltage V_{sto_ref}. The compensated error, V_{c1}, determines the on time of Q_1, which controls the input power. Whenever Vsto_avg is not equal to V_{sto_ref}, V_{c1} will be changed by the feedback loop to change the input power. As a chain reaction, Vsto_avg will be adjusted to follow V_{sto_ref} again. For example, if the net stored energy with C_{sto} is above zero, V_{sto_avg} will start growing and eventually become higher than V_{sto_ref}. Once this happens, the compensated error signal Vc1 will be decreased. A decreased V_{c1} would generate a smaller on time for Q_1, which reduces the input power. As the output power remains unchanged, a reduction in input power will reduce the net energy stored in C_{sto}. The feedback loop will continue exert this effect and the net energy storage in C_{sto} will eventually become negative in a half line cycle. Then, V_{sto} will start decreasing and eventually be brought down to V_{sto_avg}. It is noted that with constant on time in a half line cycle, together with DCM operation, power factor correction is achieved automatically, which also indicated by Eq. (15). In addition, V_{sto} should be controlled to maintain a proper operation. Since there is a significant double-line-frequency ripple voltage on V_{sto}, one

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needs to make sure that V_{sto_min} is always higher than V_{LED}. The reference voltage for V_{sto_avg} should be designed high enough to maintain this condition, which is achieved by the V_{sto_avg} voltage control loop, as shown in Fig. 14 as well.

V. Design Analysis

In this section, the design parameters will be analyzed to provide a design guideline. The component voltage and current stresses, the design of V_{sto_avg} and the selection of C_{sto}, as well as the selection of the switching frequency for the proposed LED driver will be discussed.

A. Component voltage stress

The voltage stress for each component, as described in Section II, is summarized in TABLE 1. The voltage stresses of the components are determined by the input voltage, the voltage of the storage capacitor voltage V_{sto} and the LED output voltage. Under 110Vrms input voltage, 65V LED output voltage, N_{pri}: N_{sec} = 1: 1, and the storage capacitor voltage V_{sto} swinging from 105V to 185V, the maximum voltage of Q_1, D_1, D_2 and Q_2 are 318V, 318V, 220V and 120V, respectively as plotted in Fig. 15.

TABLE 1 Expression of the voltage stress of each component

Q_1	$V_{in}(t)+V_{sto}(t)\times\frac{N_{pri}}{N_{sec}}$
D_1	$V_{in\_pk}\times\frac{N_{sec}}{N_{pri}}+V_{LED}$
D_2	$V_{sto}(t)+V_{in}(t)\times\frac{N_{sec}}{N_{pri}}$
Q_2	$V_{sto}-V_{LED}$

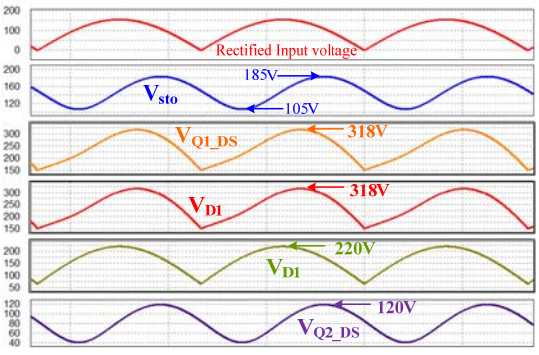

Fig. 15 Plot of component voltage stresses with the proposed LED driver over half line cycle (the simulation is based on the following parameter: V_{in}=110Vrms, V_{LED}=65V, P_{LED}=28W, V_{sto_min}=105V, V_{sto_max}=185V, N_{pri}: N_{sec}= 1:1)

B. Component current stress

In every switching cycle, at time t_1, the energy stored in the Flyback transformer, E_{Tran_t1}, can be expressed as:

$$E_{Tran\_t1}(t') = \frac{1}{2}L_{pri}\times I^2_{pri\_t_1}(t') \quad (20)$$

Where in Eq. (20), L_{pri} represents the inductance of primary side winding, T_s represents the switching period, and $I_{pri\_t1}(t)$ represents the primary side switching current at time t_1 in a switching cycle. The symbol "(t')" indicates that I_{pri_t1} is a time-varying parameter at line cycle scale. Therefore, the instantaneous input power can be expressed as:

$$P_{in}(t') = \frac{E_{Tran\_t_1}}{T_s} = \frac{L_{pri}\times I^2_{pri\_t_1}(t')}{2\times T_s} \quad (21)$$

In Eq. (21), T_s represents one switching period. Rearranging Eq. (21) yields:

$$I_{pri\_t_1}(t') = \sqrt{\frac{P_{in}\times 2\times T_s}{L_{pri}}} \quad (22)$$

The switching current in the secondary side winding at time t_1 can be expressed as:

$$I_{sec\_t_1}(t') = \frac{N_{pri}}{N_{sec}}\times\sqrt{\frac{P_{in}\times 2\times T_s}{L_{pri}}} \quad (23)$$

Replacing P_{in} with P_{in_max} in Eq. (22) & (23), the maximum switching current in the primary side winding and the secondary side winding, in a half line cycle, can be calculated as:

$$I_{pri\_max} = I_{Q_1\_max} = \sqrt{\frac{4P_{LED}\times T_s}{L_{pri}}} \quad (24)$$

$$I_{sec\_max} = I_{D_2\_max} = \frac{N_{pri}}{N_{sec}}\times I_{pri\_max} = \sqrt{\frac{4P_{LED}\times T_s}{L_{sec}}} \quad (25)$$

With the design specification provided in TABLE 4, the maximum switching current in Q_1 and D_2 is calculated to be 2.36A. When $P_{in} > P_{LED}$, the magnetic current starts conducting in D_1 at time t_2. The energy stored in the transformer at time t_2, E_{Tran_t2}, can be expressed as:

$$E_{Tran\_t_2(P_{in}>P_{LED})} = \frac{1}{2}L_{sec}\times I^2_{D_1\_t_2(P_{in}>P_{LED})} \quad (26)$$

As the remaining energy in the transformer will be transferred to the LED load, therefore

$$\frac{E_{L\_sec\_t_2(P_{in}>P_{LED})}}{T_s} = P_{LED} \quad (27)$$

Combining Eq. (26) and (27) yields:

$$I_{D_1\_t_2(P_{in}>P_{LED})} = \sqrt{\frac{2P_{LED}\times T_s}{L_{sec}}} \quad (28)$$

It can be understood that, when $P_{in} > P_{LED}$, the switching current in D_1 at t_2 is the maximum current of D_1. Therefore,

$$I_{D_1\_max} = I_{Q_2\_max} = \sqrt{\frac{2P_{LED}\times T_s}{L_{sec}}} \quad (29)$$

I_{D1_max} is calculated to be 1.67 A with the specification and parameters from TABLE 4.

C. Storage capacitor C_{sto} selection

The average voltage of V_{sto}, V_{sto_avg}, is closely related to the selection of C_{sto}. Combining Eq. (4) and (5), the relationship between C_{sto} and the voltage V_{sto_avg} can be expressed as:

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$$C_{sto} = \frac{P_{LED} \times T_{line}}{2\pi \times V_{sto\_avg} \times (\Delta V_{sto})} \quad (30)$$

At the same time, there is another constraint that needs to be maintained at all time:

$$V_{sto\_min} = V_{sto\_avg} - \frac{\Delta V_{sto}}{2} > V_{LED} \quad (31)$$

For example, if V_{sto_avg} is selected to be 150V and the LED voltage is 60V, the peak-to-peak ripple voltage of V_{sto}, ΔV_{sto}, should be limited to be less than 180V. In this way, V_{sto_min} is always higher than 60V. Among V_{sto_avg}, ΔV_{sto} and C_{sto}, one can first determine values for two parameters, based on the design, and then calculate the third one. V_{sto_avg} can be regulated by the control loop as discussed in section V. Once the allowable V_{sto} is determined, the capacitor C_{sto} can be calculated by Eq. (30).

As shown in TABLE 1, the voltage stresses of Q_1, D_2, Q_2 are related to V_{sto}. A higher voltage of V_{sto} will result in higher voltage stresses on these components. The maximum voltage stress allowed on these components will, therefore, affect the selection of C_{sto}.

D. Achieving DCM operation

Flyback PFC is operated under DCM constant on time (for Q_1) to achieve a high PFC. It can be well understood, when P_{in}=2P_{LED}, the time span (t_3-t_0) will be stretched to the maximum. Therefore, to achieve DCM operation, one needs to make sure T_s is larger than (t_3-t_1) when P_{in} = 2P_{LED} with the given circuit parameters. When the input voltage reaches its maximum in a half line cycle, the primary side switching current also reaches the maximum. The relationship between them can be expressed as:

$$I_{pri\_max} = \frac{V_{in\_max} \times (t_1 - t_0)}{L_{pri}} \quad (32)$$

Combing Eq. (24) and (32) yields:

$$(t_1 - t_0) = \frac{\sqrt{4 \times T_s \times P_{LED} \times L_{pri}}}{V_{in\_max}} \quad (33)$$

When P_{in} = P_{LED}, the relationship between the peak switching current in D_1 and the timespan (t_2-t_3) can be expressed as:

$$I_{D1\_max} = \frac{V_{LED} \times (t_3 - t_2)}{L_{sec}} \quad (34)$$

Combing Eq. and (33) yields:

$$(t_3 - t_2) = \frac{\sqrt{2 \times T_s \times P_{LED} \times L_{sec}}}{V_{LED}} \quad (35)$$

The secondary side winding releases energy to the capacitor C_{sto} during the time interval [t_1-t_2]. The current change on the secondary side winding during [t_1-t_2], the voltage V_{sto} and the secondary side inductance L_{sec}, have the following relationship:

$$\frac{V_{sto} \times (t_2 - t_1)_{max}}{L_{sec}} = I_{sec\_max} - I_{D1\_max} \quad (36)$$

Combining Eq.(25) and (36) yields:

$$(t_2 - t_1)_{max} = \frac{(\sqrt{\frac{4 \times T_s \times P_{LED}}{L_{pri}}} - \sqrt{\frac{2 \times T_s \times P_{LED}}{L_{sec}}}) \times L_{sec}}{V_{sto}} \quad (37)$$

The above derivation assumes that DCM operation has already been achieved and needs to be verified. In other words, one needs to ensure that the sum of [t_0-t_1], [t_1-t_2] and [t_2-t_3] is less than the predefined switching period. As an example, one can define T_s to be 20μs. With the circuit parameters from TABLE 4, (t_1-t_0) and (t_3-t_2) are calculated to be 6.1μs, 10.3μs, respectively. When P_{in}=2P_{LED}, V_{sto} is at the vicinity of the averaged value, 150V. Using V_{sto}=150V in Eq. (37), (t_2-t_1) is calculated to be 1.85μs. Therefore, (t_3-t_0) is equal to 18.2μs and is less than the predefined 20μs switching period. If, somehow, the initial assumption of DCM operation is not met, one can reselect the switching period. On the other side, if one aims to operate at a specific switching period (or frequency) for better EMI signature or efficiency, the circuit parameters, such as L_{pri}, V_{in_max}, L_{sec}, can be reselected to change the time (t_1-t_0), (t_2-t_1), (t_3-t_2), as indicated by (33), (35) and (37).

At the same time, it is not desirable to make T_s much larger than (t_3-t_0). Eq. (24), (25) and (29) indicate that a lower current stresses can be achieved with Q_1, D_1, Q_2 and D_2 when T_s is smaller. Therefore, T_s should be selected to be the smallest value that achieves DCM, with some acceptable margin.

E. Loss breakdown

One major advantage of the proposed LED driver is a reduction of the power conversion loss. In this section, a breakdown of the proposed unidirectional energy buffering LED driver as well as the previous active filtering LED driver will be presented. The MOSFET Q_2 is under leading edge modulation in this analysis.

The loss breakdown of the proposed unidirectional energy buffering LED driver and the previous active filter LED driver are presented in TABLE 2 and TABLE 3. The parameters used for loss calculations are derived or obtained from the datasheets is presented in Appendix. One should note that the design of the Buck converters is identify in two designs. Therefore, analyzing the detail loss from each component inside the Buck converter is not necessary. The efficiency of the Buck converter and Boost converter are estimated in TABLE 2 and TABLE 3.

When looking into both designs from the primary side, the operation of the Flyback PFC is the same. Therefore, the conduction and switching losses with Q_1 are the same in both designs. The leakage inductance loss and the transformer loss are also the same in both designs.

The loss generated by the operation of Q_2 is presented in TABLE 2. Because the voltage stress on Q_2 is much lower than the voltage stress on Q_1, very low on-resistance MOSFET can be found to implement Q_2. A 16 mohm on-resistance MOSFET is used, and the conduction loss of Q_2 is only 1.7mW. When the cost is a concern, a MOSFET with a higher on-resistance can also be used to implement Q_2, which will generate more

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TABLE 2 Loss breakdown of the proposed unidirectional energy buffering LED driver

Sources of loss	Expression for loss	Loss (W)	Percentage
Q1 conduction loss	$P_{Q1\_cond} = I_{Q1\_rms}^2 \times R_{Q1\_on}$	0.15	3.2%
Q1 output capacitor loss	$P_{Q1\_cap} = C_{Q_1\_oss} \times V_{Q1\_ds}^2 \times F_{sw}$	0.02	1.7%
Q1 turn off overlap loss	$P_{Q1\_off} \approx (V_{Q_1\_ds} \times I_{Q_1\_pk\_rms} \times T_{f\_Q_1} \times F_{sw})/2$	0.15	4.4%
D1 conduction loss	$P_{D_1\_cond} = I_{D_1\_avg} \times V_{D_1\_F}$	0.46	11.0%
Q2 conduction loss	$P_{Q_2\_cond} = I_{Q_2\_rms}^2 \times R_{Q_2\_on}$	0.0017	0.0%
Q2 output capacitor loss	$P_{Q1\_cap} = (C_{Q_2\_oss} \times V_{Q2\_ds}^2 \times F_{sw})/4$	0.014	0.3%
D2 conduction loss	$P_{D_1\_cond} = I_{D_2\_avg} \times V_{D_2\_F}$	0.14	3.3%
Q2 turn on overlap loss	$P_{Q2\_on} \approx (V_{Q_2\_ds} \times I_{Q_2\_pk} \times T_{r\_30} \times F_{sw})/4$	0.02	0.4%
Input bridge diode conduction loss	$P_{bridge\_cond} = I_{in\_avg} \times V_{DB\_F} \times 2$	0.48	11.4%
Leakage inductance loss	$P_{lk} = \frac{1}{2} \times I_{Q_1\_pk\_rms}^2 \times L_{lk}$	1.39	33.2%
Transformer core and copper loss	$P_{transformer} = P_{LED} \times K_{tran\_loss}$	1.12	26.7%
Total loss without the Buck converter		3.94W	93.4%
Buck converter loss	$P_{Buck\_loss} = (P_{LED}/\pi)(\frac{1}{\eta_{buck}} - 1)$	0.28	6.6%
Total loss of the proposed LED driver		4.21W	100%

TABLE 3 Loss breakdown of the previous active filter LED driver

Sources of loss	Expression for loss	Loss (W)	Percentage
Q1 conduction loss	$P_{Q1\_cond} = I_{Q1\_rms}^2 \times R_{Q1\_on}$	0.15	3.2%
Q1 capacitor loss	$P_{Q1\_cap} = C_{oss} \times V_{Q1\_ds}^2 \times f_{pwm}$	0.04	0.8%
Q1 turn off loss	$P_{Q1\_off} = (V_{Q_1\_ds\_rms} \times I_{pk\_rms} \times T_f \times f_{PWM})/2$	0.23	4.9%
D1 conduction loss	$P_{D_1\_cond} = I_{D_1\_avg} \times V_{D_1\_F}$	0.68	14.5%
Input bridge diode conduction loss	$P_{bridge\_cond} = I_{in\_avg} \times V_{DB\_F} \times 2$	0.48	10.3%
leakage inductance loss	$P_{lk} = \frac{1}{2} \times I_{Q_1\_pk\_rms}^2 \times L_{lk}$	1.39	30.1%
transformer core and copper loss	$P_{transformer} = P_{LED} \times K_{tran\_loss}$	1.12	24.1%
Total loss of Flyback PFC		4.08	88%
Loss from Boost converter	$P_{Buck\_loss} = (P_{LED}/\pi)(\frac{1}{\eta_{buck}})(\frac{1}{\eta_{boost}} - 1)$	0.28	6.0%
Loss from Buck converter	$P_{Buck\_loss} = (P_{LED}/\pi)(\frac{1}{\eta_{buck}} - 1)$	0.28	6.0%
Total loss of previous active filter LED driver		4.64	100%

conduction loss. However, it should not have too much impact on the overall loss.

When $P_{in} < P_{LED}$, the duty cycle of Q_2 is controlled to be 100%. Therefore, the turn-on overlap loss with Q_2 only occurs when $P_{in} > P_{LED}$. Under this condition, the average drain to source voltage of Q_2 is only 30V before Q_2 is turned on, the calculated turn-on overlap loss is only 20mW and only 0.4% of the total loss. Also, the output capacitor switching loss with Q_2 only occurs when $P_{in} > P_{LED}$ and is calculated to be 6.9mW. Overall, the losses generated by the operation of Q_2 is equal to 1.7mW + 20mW+ 6.9mW = 28.6mW, which is only 0.1% of the output power and can be ignored in the design.

Because V_{sto} is much higher than V_{LED}, the sum of current, I_{D1_avg} and I_{D2_avg} in the proposed unidirectional energy buffering LED driver are smaller than the average current I_{D1_avg} in the previous active filtering LED driver. Consequently, the

total conduction loss with D_1 and D_2 in the proposed LED driver is smaller than the conduction loss with D_1 in the previous active filter LED driver. It should note that the total loss generated by the proposed LED driver, without Buck converter operation is 3.94W, which already includes the loss generated when transfers energy from the AC input to the LED load and the storage capacitor. This number is almost equal to, even slightly smaller than, the loss generated by the Flyback PFC in the previous active filtering LED driver. Therefore, the process of storing the extra energy in the proposed LED driver can be claimed only go through one power conversion step. Compared to the previous active filter LED driver, the loss generated by transferring the extra energy from the LED load side to the storage capacitor, by the boost converter, is eliminated in the proposed unidirectional energy buffering LED driver, which will help achieve higher efficiency.

Fig. 16 shows the loss breakdown of the proposed LED driver with bar Chart.

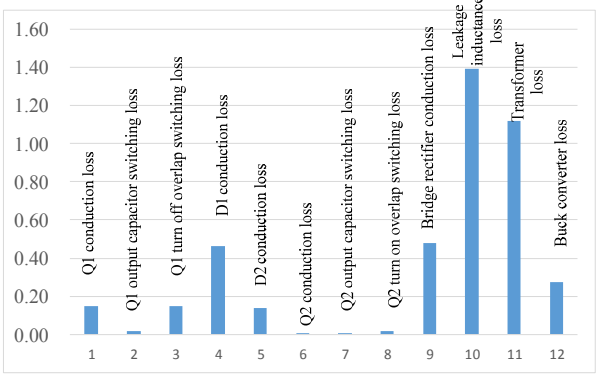

Fig. 16 Loss breakdown of the proposed LED driver

F. Efficiency

As discussed in the above section, the imbalanced energy only goes through one power conversion step when transfers it from the AC input to the storage capacitor. Therefore, in total, the imbalanced energy experiences two power conversion steps, which is one time less than the previous active filtering and three port LED drivers. The amount of imbalanced energy can be expressed as:

$$P_{imb} = \frac{\int_{\frac{\pi}{8}}^{\frac{3\pi}{8}} P_{in}(t)dt}{T_s/2} = \frac{\int_{\frac{\pi}{8}}^{\frac{3\pi}{8}} \frac{1}{2}P_{in\_pk} \times [1-\cos(4\pi \times f_{line} \times t)]dt}{T_s/2} = \frac{1}{2\pi}P_{in\_pk} = \frac{1}{\pi}P_{LED} \quad (38)$$

In Eq. (38), P_{inb} represents the amount of imbalanced power. Approximately, the total power losses can be partitioned as the losses generated by the operation of the Flyback PFC and the losses generated by the Buck converter. The loss generated by the operation of Q_2 can be ignored, as proofed in the above section. Therefore, the efficiency of the proposed LED driver can be expressed as:

$$\eta_{LED\_drv} \approx \frac{P_{LED}}{\frac{P_{LED}-P_{imb}}{\eta_{PFC}} + \frac{P_{imb}}{\eta_{PFC} \times \eta_{Buck}}} \quad (39)$$

To facilitate a comparison between the efficiency of the proposed LED driver and the efficiency of a conventional two-stage LED driver, Eq.(39):

$$\eta_{LED\_drv} = \eta_{PFC} \times \eta_{eqv} \quad (40)$$

Combining Eq. (38), (39) and (40) yields:

$$\eta_{eqv} = \frac{1}{\frac{(1-\frac{1}{\pi})}{1} + \frac{\frac{1}{\pi}}{\eta_{Buck}}} \quad (41)$$

Using (41), η_{eqv} is calculated to be 99% when η_{Buck} is 97% efficiency, as an example. When the Flyback PFC achieves 86% efficiency, the theoretical efficiency of the proposed LED driver is calculated to be 85.1%, which is only 0.9% lower than a conventional single-stage LED driver. The reduction in efficiency is a small price to pay when flicker-free operation and electrolytic capacitor-free design are achieved. On the other side, the efficiency of a Flyback PFC plus a Buck converter (two stages) design should be much lower. All of the output power needs to be processed by the Buck converter in the two-stage design. By comparison, only ~ 30% output power passes through the Buck converter in the proposed design. Therefore, the proposed design will achieve significant efficiency improvements over the existing two-stage driver. Assuming the Buck converter in the two-stage design achieves the same 97% efficiency, the efficiency of the two-stage LED driver will be 86% × 97% = 83.4%, which is 1.7% lower than the proposed LED driver. Also, a conventional two-stage LED driver will still require the use of electrolytic capacitors. Therefore, the proposed LED driving method is an optimal solution to achieve both high efficiency and long lifespan.

VI. Experimental Verification

A 28W experimental prototype had been built and tested to verify the proposed unidirectional current ripple compensation LED driving method. TABLE 4 shows the system specifications and circuit parameters of the experimental prototype.

TABLE 4 The experimental prototype specification and key components

System Specification	
Input voltage	89Vrms – 132Vrms
Maximum output voltage	~65V
Maximum output current	0.43A
Maximum output power	28W
Circuit Parameter	
Transformer	N_{pri}: N_{sec}: = 1:1 L_{pri}=400μH, EE16 core
Switching frequency	50kHz
Input Bridge rectifier	GBU606
PFC Controller	PIC16F1578-I/SS
MOSFET Q1	STB13N80k5 (800V, 12A)
MOSFET Q2	FDP2532 (150V, 8A@Ta=25C°)
Diode D1	STPSC6H065D1 (650V, 6A)

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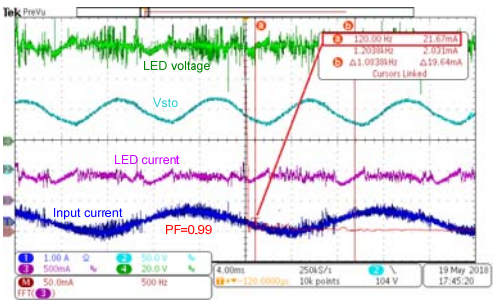
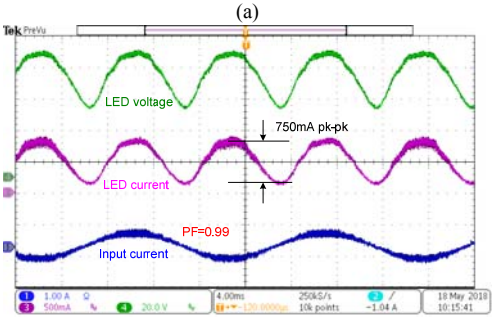
Diode D2	LQA06T300 (400V, 6A)
Output capacitor	CGA9N3X7S2A106K230KB, 100V, 10μF
Storage capacitor	2 x ECW-FD2W335K 450V, 3.3μF
High and low sides MOSFET (Buck)	IRF730PBF (400V 5.5A)
Controller (Buck)	NCP159DR2G
Output inductor	DELEVAN-224 (220μH, 2.0A)
Output capacitor	CGA9N3X7S2A106K230KB, 100V, 10μF

Fig. 17(a) shows the key line cycle waveforms of the proposed LED driver. The power factor of the AC input was measured to be 0.98. The voltage on the buffer capacitor, V_{sto}, changes from a minimum of 70V to a maximum of 120V. The 120Hz ripple LED current is measured to be 21.7mA rms with FFT function in the oscilloscope, which converts to 30.7mA peak ripple current. Therefore, the 120Hz ripple current is 7.1% of the average LED current. Fig. 17(b) shows the 120Hz ripple current reaches 750mA pk to pk when the current compensation is disabled. The proposed unidirectional current compensator demonstrated flicker-free LED driving performance without utilizing an electrolytic capacitor.



(a)



(b)

Fig. 17 Key line cycle waveforms of the proposed LED driver I , (a) unidirectional current conpensator is enabled (b) unidirectional current conpensator is disabled

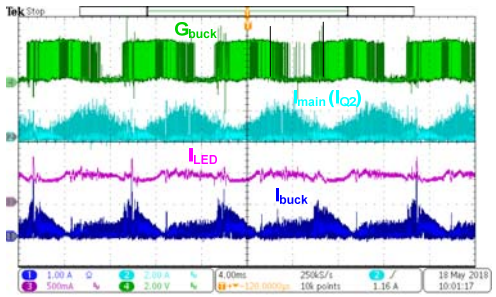
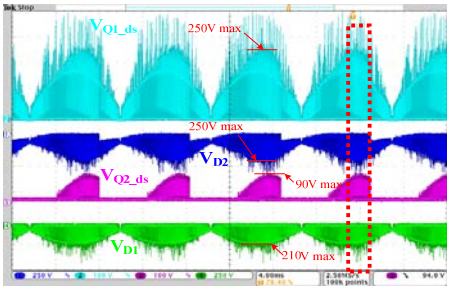
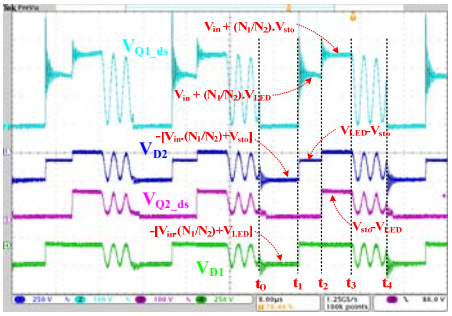


Fig. 18 Key line cycle waveforms of the proposed LED driver

Fig. 18 shows the switching current from the main output, the switching current from the Buck converter output and the LED current. Fig. 19 (a) and (b) shows the voltage waveforms of the key switching components currents with Q_2 under trailing edge modulation. The maximum voltage stresses with MOSFET Q_1, Q_2, diode D_1 and D_2 are 250V, 90V, 210V and 250V, respectively. Fig. 19(b) shows the zoomed in waveform at switching cycle time scale. Q_1 and Q_2 are on during the time interval $[t_0\text{-}t_1]$. Therefore, the voltage stress on Q_1 and Q_2 are zero. During $[t_1\text{-}t_2]$, Q_1 is off and Q_2 is remaining on. The voltage stress on Q_1 is equal to the input voltage plus the LED output reflected to the primary side. The voltage stresses for D_1 and Q_2 are zero. The diode D_2 is reverse biased and the voltage across D_2 is equal to the V_{sto} minus the LED voltage. Q_2 is turned off at t_2 and the secondary side current flows in D_2. The voltage stress on Q_1 becomes the sum of input voltage plus the V_{sto} reflected to the primary side. The diode D_1 is forward biased so that the voltage stress is zero. The voltage stress on Q_2 is equal to V_{sto} minus the LED voltage.



(a)



(b)

Fig. 19 Key component voltage waveforms with Q2 under trailing edge modulation, (b) zoom in of (a)

Fig. 20 (a) and (b) shows the voltage waveforms of the key switching components with Q_2 under leading edge modulation. As expected, the maximum voltage stresses with MOSFET Q_1, Q_2, diode D_1 and D_2 are the same as they are in Fig. 19. The switching waveforms at switching cycle time scale is shown in Fig. 20 (b). The voltages across these components under each time interval are also annotated.

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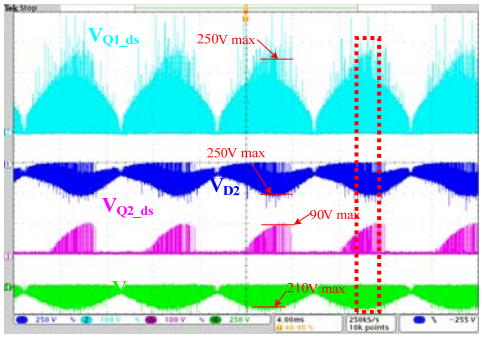
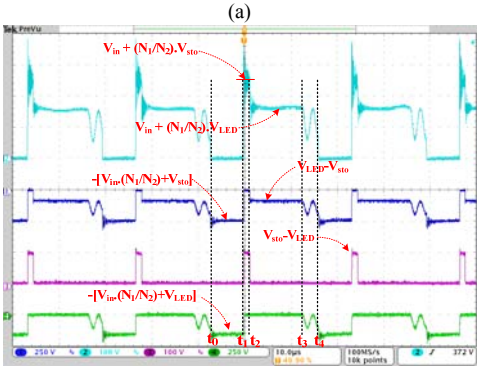


(a)

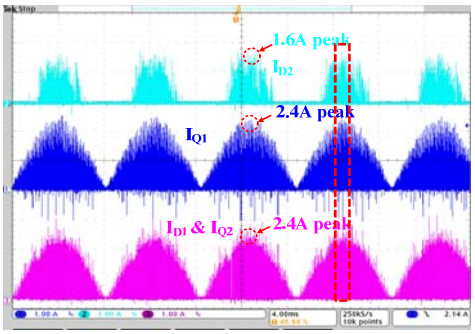


(b)

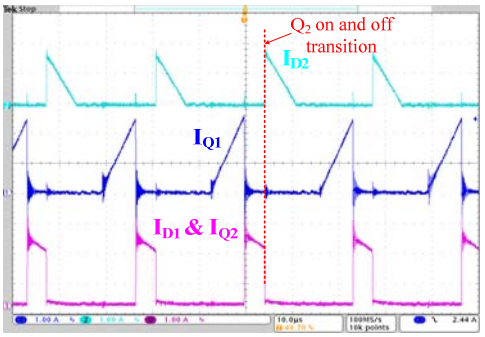
Fig. 20 Key component voltage waveforms with Q_2 under leading edge modulation, (a) at line cycle time scale, (b) zoom in of (a)

Fig. 21 shows the switching current waveforms of the key components with Q_2 under trailing edge modulation. The maximum current with Q_1 is 2.4A. Under trailing edge modulation, the peak secondary side current flows in D_1 and Q_2. Therefore, the peak current with D_1 and Q_2 are also 2.4A. The peak current in D_2 is 1.6A when the secondary side switching current commutes from D_1 to D_2.

Fig. 22 shows the switching current waveforms of the key components with Q_2 under leading edge modulation. The maximum current with Q_1 is also 2.4A. Under leading edge modulation, the peak secondary side current flows in D_2. Therefore, the peak current in D_2 is also 2.4A. The peak current in D_1 (also Q_2) is 1.6A when the secondary side switching current commutes from D_2 to D_1.

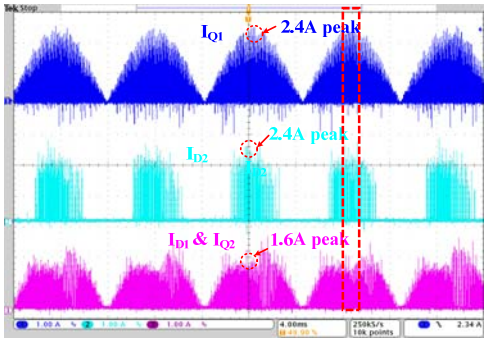


(a)

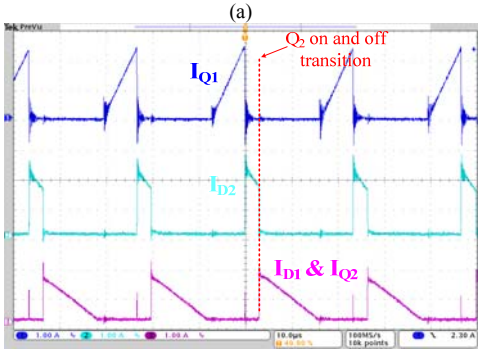


(b)

Fig. 21 Key component current waveforms with Q_2 under trailing edge modulation, (a) at line cycle time scale, (b) zoom in of (b)



(a)



(b)

Fig. 22 key components current waveforms with Q_2 under leading edge modulation, (a) at line cycle time scale, (b) zoom in of (a)

The efficiency of the experimental prototype had been measured and compared with the efficiency of a conventional Flyback LED driver. These two designs share the same PFC stage to make a fair comparison. Both prototypes achieve their highest efficiency at 350mA LED load. The maximum efficiency of the proposed LED driver is around 1% lower than the maximum efficiency of the conventional single stage LED driver, as shown in Fig. 23.

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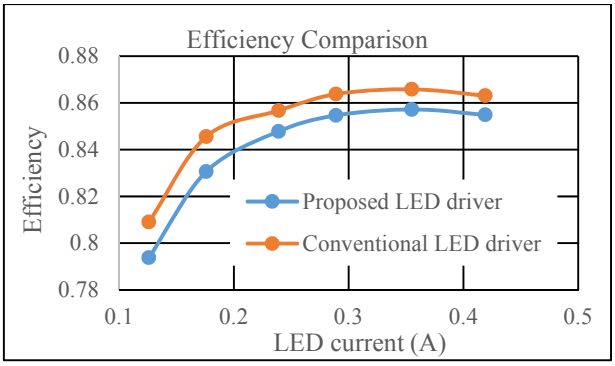

Fig. 23 Efficiency comparison between the proposed unidirectional current ripple compensator LED driver and a conventional LED driver

Fig. 24 shows the power factor of the proposed LED driver and Fig. 25 shows the measurement of input harmonic currents. Since the proposed LED driver applies the same PFC technology as a conventional design, a high PF is achieved. At full load, the experimental prototype achieved 0.99PF, which meets the requirement from EnergyStar. All harmonic currents of interest are also below the limits from IEC-61000-3-2.

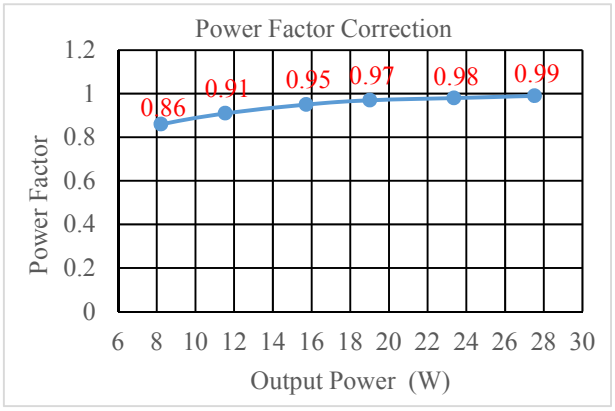

Fig. 24 Power factor performance under 110Vrms input

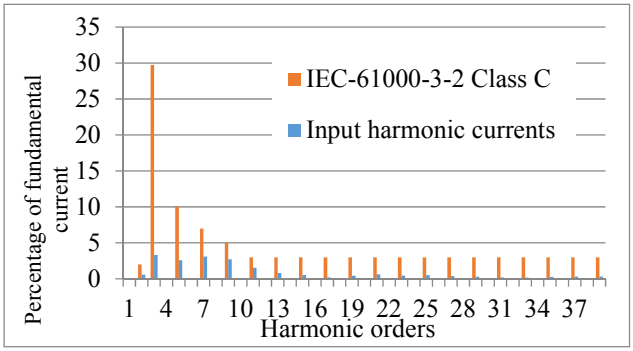

Fig 25 Input harmonic currents versus IEC-61000-3-2 limit under 110Vrms input, full load

The photo of the experimental prototype is shown in Fig 26.

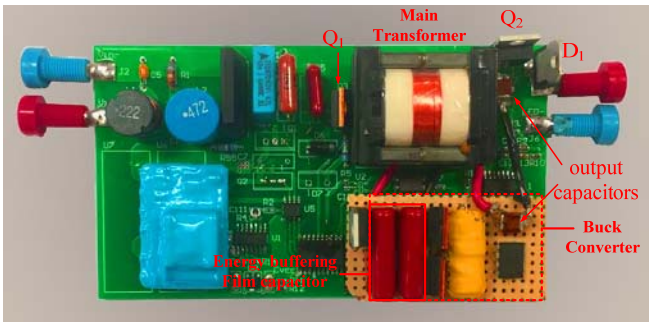

Fig. 26 Photo of the experimental prototype

VII. Conclusion

In this paper, an unidirectional current ripple compensation LED driver has been proposed to achieve electrolytic capacitor-less and flicker-free design. A Flyback PFC is used to deliver energy from the AC input to LED output while achieving a high power factor correction at the same time. By controlling the MOSFET Q_2, the flow of energy can be precisely controlled either delivering to LED output or storing in the energy storage capacitor, in every switching cycle. When $P_{in} > P_{LED}$, the imbalanced energy will be stored in the capacitor, C_{sto}. When $P_{in} < P_{LED}$, the reserved energy in C_{sto} is delivered to the output through a Buck converter. The advantage of this energy delivery structure is a reduction in the circulating energy compared with previous approaches. In previous active filter and three-port LED drivers, the imbalanced energy (approximately one third of total energy) goes though three power conversion steps, which results in significant loss. In the proposed LED driver, the imbalanced energy experiences only two power conversion steps, resulting in improved efficiency compared with previous designs. A 28W experimental prototype had been designed and tested. The 120Hz ripple current is measured to be 11% of the DC LED current. With the optimized energy buffering structure, the efficiency of the proposed LED driver is only 0.9 % lower than a conventional single-stage design, which is a significant improvement from previous electrolytic capacitor-less design. The PF and harmonic currents of the proposed LED driver had also been verified in the experimental prototype, and measured results can meet the requirements both from Energy Star and IEC-61000-3-2. Overall, the measured results highly agree with the analysis and demonstrate a very promising LED driving technology.

APPENDIX

TABLE 5 Parameter values used in the analysis of loss breakdown

Description	Used in the proposed LED driver	Used in the previous active filter LED driver
RMS current of Q_1	I_{Q1_rms} =0.57A,	I_{Q1_rms} =0.57A,
On resistance of Q_1	R_{Q1_on}=0.45ohm,	R_{Q1_on}=0.45ohm,
Forward voltage drop of D_1	V_{D1_F}=1.57V	V_{D1_F}=1.57V
Parasitic output capacitor of Q_1	C_{Q1_oss}=50pF	C_{Q1_oss}=50pF
Drain to source voltage stress of Q_1	V_{Q1_ds}=V_{in_rms} =110V	V_{Q1_ds}=V_{in_rms} =110V
Switching frequency of the PFC	F_{sw}=50kHz	F_{sw}=50kHz
RMS value of peak switching current in Q_1	$I_{Q1\_pk\_rms}$= 1.67A	$I_{Q1\_pk\_rms}$= 1.67A
Average current in D_1	I_{D1_avg}=0.29A	I_{D1_avg}=0.43A
Average input current in bridge rectifier	I_{in_avg}=0.24A	I_{in_avg}=0.24A
Forward voltage drop per diode in bridge rectifier	V_{DB_F}=1V	V_{DB_F}=1V
Turn off fall time of Q_1	T_{f_Q1}=16ns	T_{f_Q1}=16ns
Efficiency of the Buck converter	η_{buck}=0.97%	η_{buck}=0.97%
Lump sum of primary side leakage inductance	L_{lk}=L_{pri} x 5% = 20μH	L_{lk}=L_{pri} x 5% = 20μH
Forward voltage drop of D_2	V_{D2_F}=1.57V	
Parasitic output capacitor of Q_2	C_{Q1_oss}=650pF	
Drain to source voltage stress of Q_1	V_{Q2_ds}=V_{sto_avg}-V_{LED}=30V	
Average current in D_2	I_{D2_avg}=0.09A	
RMS current in Q_2	I_{Q2_rms}=0.33A	
On resistance of Q_2	R_{Q2_on}=16mohm	
Turn on rise time of Q_2	T_{r_Q2}=30ns	
Peak switching current in Q_2	I_{Q2_pk}=1.67A	
Loss coefficient of the Flyback transformer	K_{tran_loss} = 4%	
Efficiency of the Boost converter		η_{boost}=0.97%

REFERENCES

[1] U.S department of energy. LED Lighiting. [online]. Available: https://energy.gov/energysaver/led-lighting [2017, July]

[2] Global LED Lighting Market Size & Share Worth $54.28 Billion by 2022 Zion Market Research [online]. Available:https://globenewswire.com/news-release/2017/01/30/911985/0/en/Global-LED-Lighting-Market-will-reach-USD-54-28-Billion-by-2022-Zion-Market-Research.html [2017, Aug]

[3] B. Lehman, A.J. Wilkins, "Designing to Mitigate Effects of Flicker in LED Lighting: Reducing risks to health and safety," in IEEE Power Electronics Magazine, Vol 1, No 3, September 2014. pp. 18-26.

[4] Illions Capacitor Limited. Aluminum Electrolytic Capacitors Life expectancy [online]. https://www.illinoiscapacitor.com/pdf/Papers/Life%20expectancy%20of%20Aluminum%20electrolytic%20capacitors.pdf [2017, Aug]

[5] X.B. Ruan, B.B. Wang, K. Yao, S. Wang, "Optimum Injected Current Harmonics to Minimize Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers" IEEE Transactions on Power Electronics, Vol.26, No.7, 2011, pp.1820,1825

[6] B.B. Wang, X.B. Ruan, K. Yao, M. Xu, "A Method of Reducing the Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers," IEEE Transactions on Power Electronics, Vol.25, No.3, March 2010, pp.592,601

[7] C.A. Cheng, C.H. Chang, T.Y. Chung and F.L. Yang, "Design and Implementation of a Single-Stage Driver for Supplying an LED Street-Lighting Module With Power Factor Corrections," IEEE Transactions on Power Electronics, Vol.30, No.2, Feb. 2015, pp.956,966

[8] J. C. W. Lam and P. K. Jain, "Isolated AC/DC Offline High Power Factor Single-Switch LED Drivers Without Electrolytic Capacitors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 3, No. 3, pp. 679-690, September 2015.

[9] J. C. W. Lam and P. K. Jain, "A High Power Factor, Electrolytic Capacitor-Less AC-Input LED Driver Topology With High Frequency Pulsating Output Current," in IEEE Transactions on Power Electronics, Vol. 30, Vo. 2, pp. 943-955, Feburary 2015.

[10] D.Camponogara, D.R.Vargas, M.A.Dalla Costa, J.M.Alonso, J.Garcia and T.Marchesan, "Capacitance reduction with an optimized converter connection applied to LED drivers," in IEEE Transactions on Industrial Electronics, Vol. 62, No.1, pp.184-192, January 2015.

[11] D.Camponogara, G.F.Ferreira, A. Campos, M.A. Dalla Costa and J. Garcia, "Offline LED Driver for Street Lighting With an Optimized Cascade Structure," in IEEE Transactions on Industry Applications, Vol.49, No 6, pp.2437-2443, December 2013.

[12] P. Fang, Y. j. Qiu, H. Wang and Y. F. Liu, "A Single-Stage Primary-Side-Controlled Off-line Flyback LED Driver With Ripple Cancellation," in IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4700-4715, June 2017.

[13] Y. Qiu, L. Wang, H. Wang, Y. F. Liu and P. C. Sen, "Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-Capacitor-Less High-Power LED Driver," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 698-713, Sept. 2015.

[14] P. Fang and Y. F. Liu, "Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation With True Single Stage Power Factor Correction," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3892-3907, May 2017.

[15] Z. Shan, X. Chen, J. Jatskevich (GAE) and C. K. Tse, "An AC-DC LED Driver with an Additional Active Rectifier and a Unidirectional Auxiliary Circuit for AC Power Ripple Isolation," in IEEE Transactions on Power Electronics, Early Access

[16] S. Wang, X.B. Ruan, K. Yao, S.C. Tan, Y. Yang and Z.H Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver" IEEE Transactions on Power Electronics, Vol.27, No.11, 2012, pp.4540,4548

[17] Q.C. Hu and R. Zane, "Minimizing Required Energy Storage in Off-Line LED Drivers Based on Series-Input Converter Modules" IEEE Transactions on Power Electronics, Vol.26, No.10, 2011, pp.2887,2895

[18] P. T. Krein, R. S. Balog and M. Mirjafari, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port," in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp. 4690-4698, November. 2012.

[19] W. Chen and S.Y.R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current," in IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1598-1607, March 2012.

[20] H. C. Kim, M. C. Choi, S. Kim and D. K. Jeong, "An AC–DC LED Driver With a Two-Parallel Inverted Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3879-3891, May 2017.

[21] B. White, H. Wang, Y. F. Liu and X. Liu, "An Average Current Modulation Method for Single-Stage LED Drivers With High Power Factor and Zero Low-Frequency Current Ripple," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 714-731, Sept. 2015.

[22] M. Chen, Y. Ni, C. Serrano, B. Montgomery, D. Perreault and K. Afridi, "An electrolytic-free offline LED driver with a ceramic-capacitor-based compact SSC energy buffer," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014

[23] Wang, B. Zhang and D. Qiu, "A Novel Valley-Fill Single-Stage Boost-Forward Converter With Optimized Performance in Universal-Line Range for Dimmable LED Lighting," in IEEE Transactions on Industrial Electronics, vol. 64, no. 4, pp. 2770-2778, April 2017

[24] H. Ma, J. S. Lai, Q. Feng, W. Yu, C. Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3057-3071, June 2012.

[25] H. Ma, J. S. Lai, C. Zheng and P. Sun, "A High-Efficiency Quasi-Single-Stage Bridgeless Electrolytic Capacitor-Free High-Power AC–DC Driver for Supplying Multiple LED Strings in Parallel," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5825-5836, Aug. 2016

[26] H. Valipour, G. Rezazadeh and M. R. Zolghadri, "Flicker-Free Electrolytic Capacitor-Less Universal Input Offline LED Driver With PFC," in IEEE Transactions on Power Electronics, vol. 31, no. 9, pp. 6553-6561, Sept. 2016.

[27] Richtek. "Single-Stage High Power Factor Flyback for LED Lighting" [online]. May 2014.
[28] Fairchild. "LED Application Design Guide Using Half-Bridge LLC Resonant Converter for 100W Street Lighting" [online]. Nov 2011.
[29] Texas Instrument. "A New Off-Line LED Lighting Driver Solution with Multi-Transformer LLC Control". [online]. Sep 2011.

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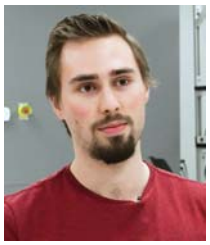

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