Seven-Switch Five-Level Active Neutral-Point Clamped Converter and Optimal Modulation Strategy

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Abstract—The five-level active-neutral-point-clamped (ANPC) converters are newly hybrid topologies which have the advantages of traditional neutral-point-clamped (NPC) and flying-capacitor (FC) multilevel converters. A novel seven-switch five-level ANPC (7S-5L-ANPC) inverter topology is proposed, which reduces the number of active semiconductor switches over traditional 5L-ANPC inverter topologies. It is capable of operating under any power factor conditions. The special modulation strategy for 7S-5L-ANPC is proposed and simulation shows only reactive current is flowing through the seventh switch. Thus, low current rating switch can be selected for the seventh switch. The proposed 7S-5L-ANPC inverter is very suitable for unity and high power factor applications such as photovoltaic (PV) application. A 1KW single-phase inverter prototype is built to verify the validity and flexibility of the proposed topology and modulation.

I. INTRODUCTION

Multilevel converters (or inverters) have been used for power conversion in high-power applications such as medium voltage grid (2.3KV, 3.3KV, or 6.9KV) to reduce the switch voltage stress, and photovoltaic (PV) application to reduce the filter size [1, 2]. Compared to two-level voltage source inverters, the advantages of multilevel inverters are lower voltage stress, higher efficiency, smaller filter size and lower common-mode voltage [3].

There are three traditional multilevel topologies [4-8]: the neutral-point-clamped (NPC) type [4, 5], flying-capacitor (FC) type [6], and cascaded H-bridge (CHB) type [7-8]. Many five-level NPC topology has been derived in [9]. NPC type generates the voltage levels from the neutral point voltage by adopting diodes. The drawback is the increased number of switching devices when voltage level increases. FC type outputs the voltage level by summing the flying-capacitor voltage. However, higher voltage level leads to more flying-capacitors and the complexity of control strategy to balance the voltages of each flying-capacitor is then increased. The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell [10]. Similarly, to have more output levels, more cells are needed. This will lead to impracticality of this type of topology since more DC sources are required.

Active-neutral-point-clamped (ANPC) which is one of the multilevel topology has been proposed in Refs [11-15]. Three 5L-ANPC topologies are shown in Fig.1. The ANPC type converter combines the features of NPC and FC topology. The ANPC topologies is receiving more and more attentions nowadays because of high efficiency and multi-level output. In this paper, a novel seven-switch five-level ANPC (7S-5L-ANPC) inverter topology is proposed. Compared to traditional ANPC topologies, the proposed topology reduces the number of active semiconductor switches. In addition, a low current rating switch can be chosen for the seventh switch. This paper is organized as follows: Section II describes working principles of proposed topology; Section III discusses the modulation strategy of 7S-5L-ANPC topologies; Section IV and V show the simulation and experimental results and Section VI gives the conclusion.
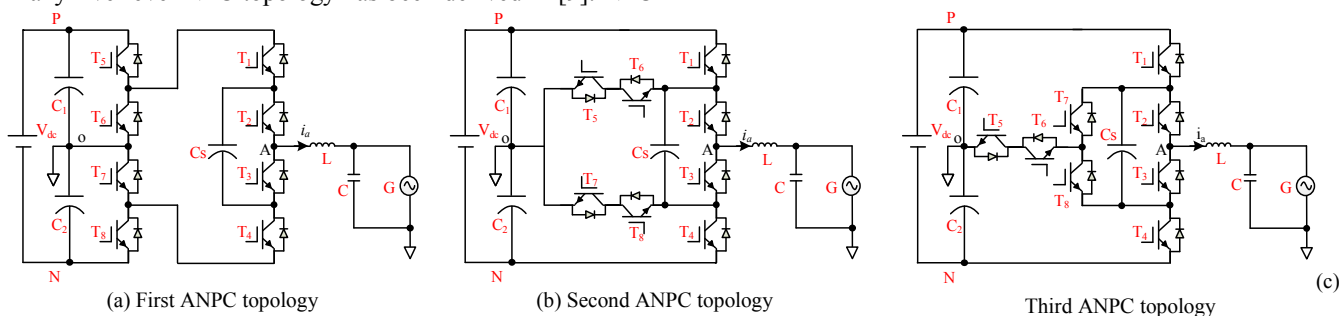

(a) First ANPC topology (b) Second ANPC topology (c) Third ANPC topology

Fig. 1. Five-level ANPC topology

II. THE PROPOSED 7S-5L-ANPC INVERTER

A. Introduction of 7S-5L-ANPC Inverter

For PV grid-connection application, the output current and grid voltage are in phase. For this reason, some reactive power current paths can be ignore. Then, some active switches can be replaced by diodes in order to increase the efficiency. Because of this, a novel 5-level ANPC inverter is proposed. It consists of 7 switches (T_1 to T_7), 2 independent-diodes (D_{F1}, D_{F2}) and 1 flying-capacitor (C_S). The configuration of 7-switches-5-level ANPC (7S-5L-ANPC) inverter is shown in Fig.2.
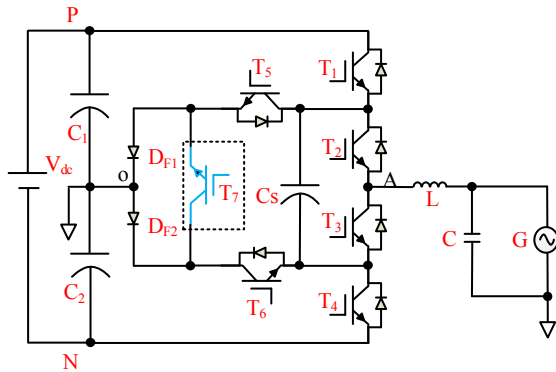

Fig. 2. Proposed 7S-5L-ANPC inverter

Based on half bridge inverter, this topology is very suitable for both single-phase and three-phase transformer-less PV system application because of no leakage current generation. In addition, only two series-connected bulk capacitors, C_1 and C_1, are connected to DC-link in which NPC type and FC type need four in series. So the difficulty of balancing DC capacitor voltages is greatly reduced. Compared to traditional 5L-ANPC which needs 8 switches and other types of 5-level inverter which need more, the proposed 5L-ANPC inverter only has 7 active switches and 2 discrete diodes. And from the analysis in the following section, it can be obtained that under appropriate modulation method, only reactive current will flow through the seventh switch T_7, which means under unity power factor and high

power factor applications, the current through T_7 is very small. Thus switch with low current rating can be selected for T_7. It can be concluded that the main advantage of 7S-5L-ANPC over traditional ANPC and other types of 5-level inverter topology is the reduced number of active semiconductors.

The seventh switch T_7 is employed under reactive power operation. The current stress of T_7 is decided by power factor $cos\theta$. A smaller IGBT without anti-diode or MOSFET can be used for T_7. The specific modulation strategy will be discussed in the following section.

B. Operation of 7S-5L-ANPC Topology

Define the input DC voltage as V_{dc}. The proposed 7S-5L-ANPC outputs five voltage levels which are $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$ (+2 level, +1 level, 0 level, -1 level and -2 level). The five voltage levels are achieved by summing the flying-capacitor voltage and DC capacitor voltage. Two DC-link capacitors in series are to provide $\pm V_{dc}/2$ voltage levels. The voltage of flying-capacitor is controlled to be kept at $V_{dc}/4$ to provide $\pm V_{dc}/4$ voltage levels.

As a result, there are eight switching states for 7S-5L-ANPC inverter topology: A, B, C, D, E, F, G and H, outputting $+V_{dc}/2$, $+V_{dc}/4$, $+V_{dc}/4$, +0, -0, $-V_{dc}/4$, $-V_{dc}/4$ and $-V_{dc}/2$ respectively. The specific switching states and current path are shown in Fig.3. Red line is the active power branch, and Green line is the reactive power branch. The switching pattern, voltage of flying-capacitor and output voltage are presented in Table I.

From Table I, it is observed that for $+V_{dc}/4$, 0 and $-V_{dc}/4$ output voltage levels, each level owns a pair of redundant switching states. When the switching pattern is $\pm V_{dc}/4$, the flying capacitor is in charge mode or discharge mode according to the direction of output current.

Without switch T_7, switching states C, D, E and F can only provide single current flowing path due to the presence of diode, which sacrifice the reactive power current path. Therefore, under reactive power operation (e.g. $cos\theta < 0.95$): in switching states C, D, E and F, T_7 is switched on to provide bi-directional current path.

TABLE I. SWITCHING STATES OF 7S-5L-ANPC INVERTER

Switching state	Switch number							Output voltage V_{Ao}	Flying capacitor C_S	
	T_1	T_2	T_3	T_4	T_5	T_6	T_7		$i_a>0$	$i_a<0$
A	1	1	0	0	0	1	0	$+V_{dc}/2$	--	--
B	1	0	1	0	0	1	0	$+V_{dc}/4$	Charge	Discharge
C	0	1	0	0	0	1	1	$+V_{dc}/4$	Discharge	Charge
D	0	0	1	0	0	1	1	+0	--	--
E	0	1	0	0	1	0	1	-0	--	--
F	0	0	1	0	1	0	1	$-V_{dc}/4$	Discharge	Charge
G	0	1	0	1	1	0	0	$-V_{dc}/4$	Charge	Discharge
H	0	0	1	1	1	0	0	$-V_{dc}/2$	--	--

(a) Mode A

(b) Mode B

(c) Mode C

(d) Mode D

(e) Mode E

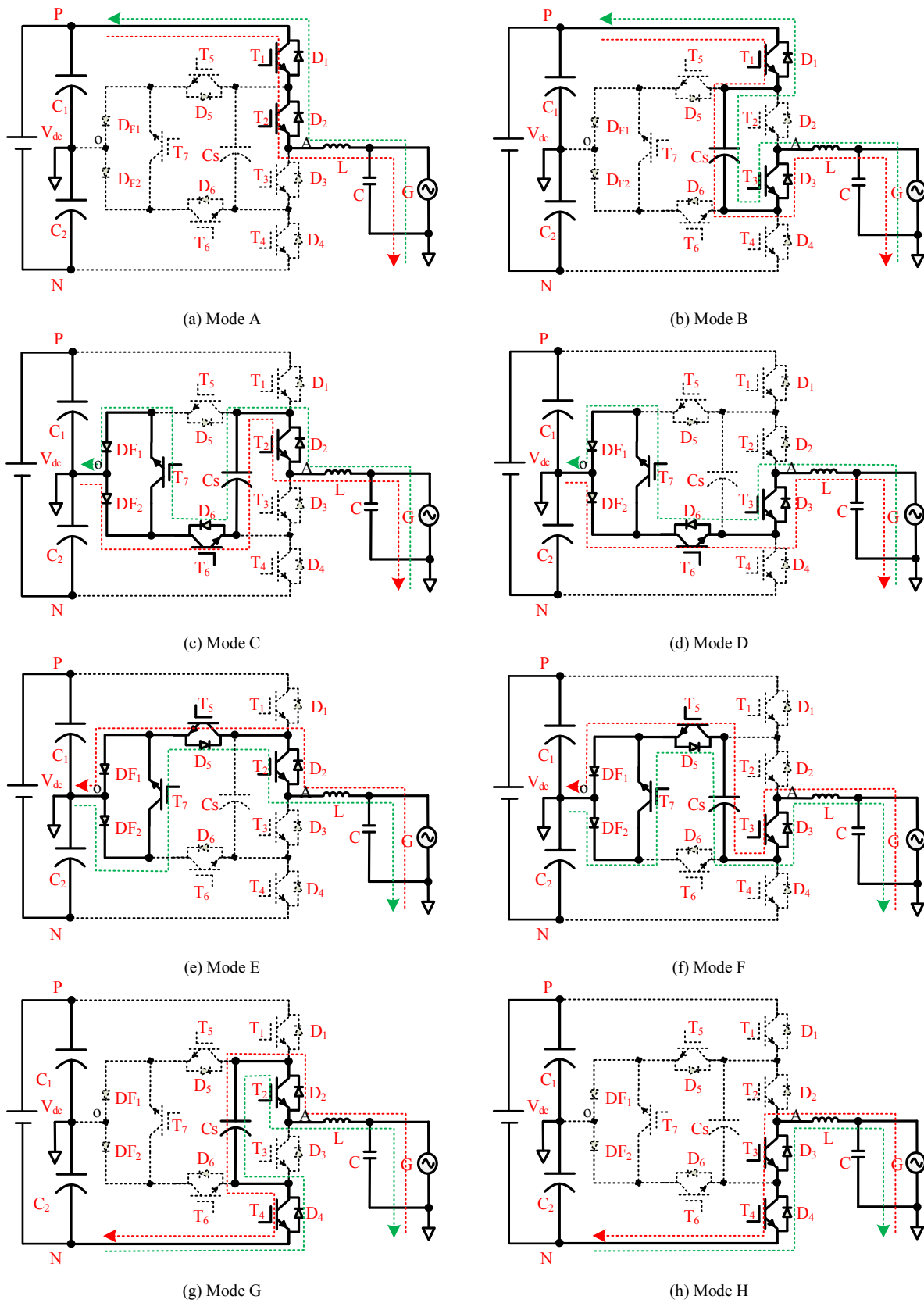(f) Mode F

(g) Mode G

(h) Mode H

Fig. 3. Eight switching states and current-flow path for 7S-5L-ANPC

III. MODULATION STRATEGY

This section investigates the modulation method for proposed 7S-5L-ANPC inverter. Same as traditional ANPC topologies, the new topology has eight switching states. However, the existence of three pairs of redundant switching modes will result in diverse modulation strategies. Therefore, appropriate switching states selection is very important because it leads to reduced switching and conduction losses.

A. Optimized zero output voltage states selection

For two redundant switching states D and E which provide zero output voltage, combination of two discrete diodes D_{F1}, D_{F2} and switch T_7 allows bi-directional current flowing path. Consequently, both modes can be used during positive, negative or whole grid period. Thus, four possible combinations of zero output modes are available for modulation. Four conditions are: (1) mode D for positive reference cycle, and mode E for negative cycle; (2) mode E for positive reference cycle, and mode D for negative cycle; (3) mode D for all zero output switching states; (4) mode E for whole reference period. Among four different situations, the currents through T_7 are different. In optimal situation, only reactive current is passing through T_7 and one discrete diode while all active current is flowing through complementary diode. In situation 1, it is only reactive current is going through switch T_7. In situation 2, all active current is passing through T_7. In situations 3 and 4, half active and reactive current is flowing through T_7. Consequently, mode D for positive grid period and mode E for negative grid cycle is the best combination for proposed 7S-5L-ANPC inverter. Simulation verification is provided in the following section.

Additionally, under situation 1, switch T_5 and T_6 will be turned on and off at line frequency. This results in the reduced switching loss. In conclusion, mode D should be used in positive grid cycle, which is called positive freewheeling state. Similarly, mode E is called negative freewheeling state and used during negative grid cycle.

B. Modulation method for 7S-5L-ANPC inverter

Fig.4 shows the diagram of modulation method for 7S-5L-ANPC inverter. There are four zones according to whether the output current and voltage are in same direction: zone 1 and 3 are reactive power zone; zone 2 and 4 belong to active power zone. In PV application, the power factor is usually larger than 0.9. An example of power factor $cos\theta > \sqrt{3}/2$ is used in our case.
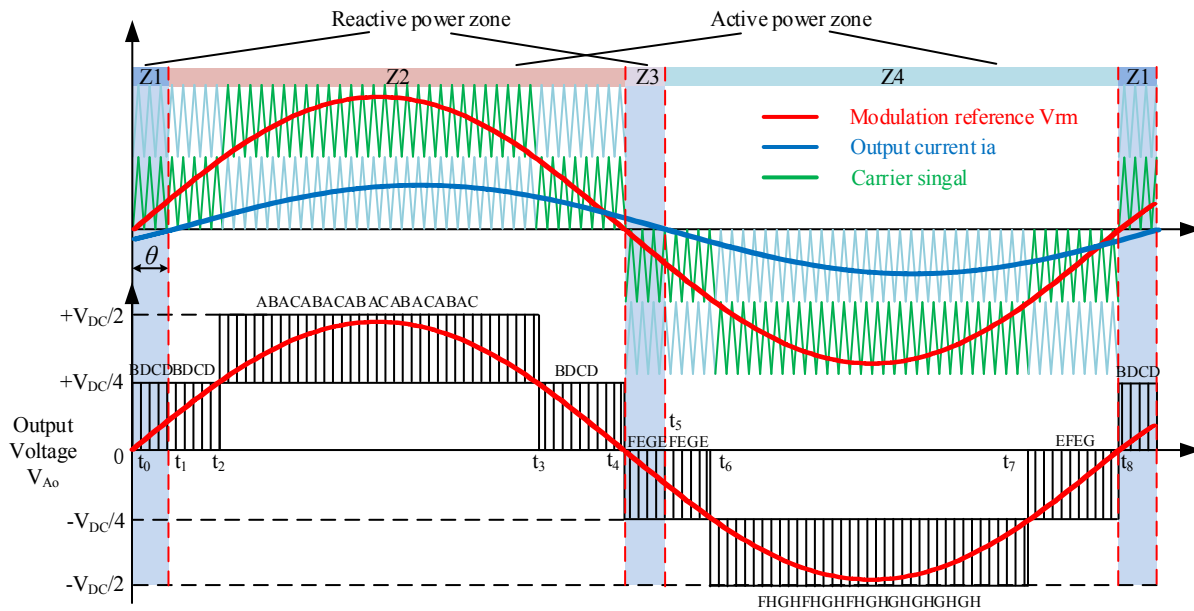

Fig. 4. PWM modulation of 7S-5L-ANPC inverter ($cos\theta > \sqrt{3}/2$)

As shown in Fig.4, the reference is compared to four carrier signals, generating five level outputs. Phase Disposition (PD) PWM modulation method (all carrier signals are in phase) [16-17] is adopted because of its lower THD (total harmonic distortion, THD).

From t_0 to t_2 and t_3 to t_4, reference voltage signal is between $+V_{dc}/4$ and 0. When reference is larger than carrier signal, the inverter outputs $+V_{dc}/4$ (+1 level), which can be achieved by states B and C. Although the redundant switching states (B, C) generate the same output voltage level, their effect on the flying-capacitor is opposite to each other. This gives an opportunity to regulate the voltage across flying-capacitor. One way is to adopt the redundant switching states alternately. Consequently, over a grid period or longer, the charging time and discharging time of flying-capacitor is the same. The flying capacitor can achieve voltage self-balancing. Additionally, this

alternation will decrease the flying-capacitor voltage ripple to lowest. Therefore, smaller capacitor can be used for flying-capacitor. When reference is less than carrier signal, the inverter gives +0 output, which is achieve by positive freewheeling state D. As a result, the switching state sequence of (B, D, C, D) is generated.

From t_2 to t_3, the output reference voltage is between $+V_{dc}/4$ and $+V_{dc}/2$. Mode A is required to generate $+V_{dc}/2$ output level. Modes B and C can be selected alternately to provide $+V_{dc}/4$ output. In this way, sequence of (B, A, C, A) guarantees output voltage and flying-capacitor voltage balancing.

Similarly, when reference signal is negative, it also compares to two carrier signals. When outputting $-V_{dc}/4$ voltage levels, redundant switching states (F, G) are employed alternately to keep flying-capacitor balanced. Consequently, during t_4 to t_6 and t_7 to t_8, switching state sequence (F, E, G, E) is acquired; from t_6 to t_7, switching state sequence (F, H, G, H) is adopted.

As discussed before, in reactive power zones: Z1 (t_0 to t_1) and Z3 (t_4 to t_5), the output voltage and current are in opposite directions. For example, in reactive power zone Z1, the current is negative, which is the green line in Fig.3 (b), (c) and (d). So in modes C and D, the current is no longer flowing through discrete diode D_{F2}; instead, it passes through switch T_7 and another discrete diode D_{F1}. Similarly, in Z3, the output current is flowing through T_7 and D_{F2}. In other cases, no current will go through T_7. Therefore, current rating of switch T_7 can be selected according to the system requirement. If the system is working under unity power factor, then the current through T_7 is closed to zero; under high power factor ($\cos\theta > \sqrt{3}/2$), small current will pass through T_7 so that a low current rating semiconductor can be selected; in low power factor case, T_7 can be selected to be the same as T_5 and T_6 due to the same voltage and current ratings. According to this, it can be concluded that the proposed 7S-5L-ANPC inverter is very suitable for PV application.

## IV.   SIMULATION VERIFICATION

To verify the selected zero output states combination is the optimal selection, simulation tests are carried out in two cases: one is under active power operation, the other is reactive power operation. Simulation parameters are shown in Table II.

TABLE II.   SYSTEM PARAMETERS

Input voltage	400V	Grid voltage	110V$_{RMS}$
DC capacitor	2000µF	Grid frequency	60Hz
Flying capacitor	310µF	Output current	4.6A$_{RMS}$
Output filter inductor	1.6mH	Switching frequency	15kHz

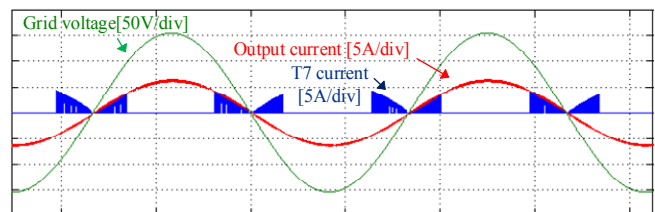### A. Active Power operation ($\cos\theta = 1$)

Under unity power factor, the simulation waveforms of inverter output voltage, flying-capacitor voltage, grid voltage, output current and T_7 current under four switching conditions are shown in Fig.5.
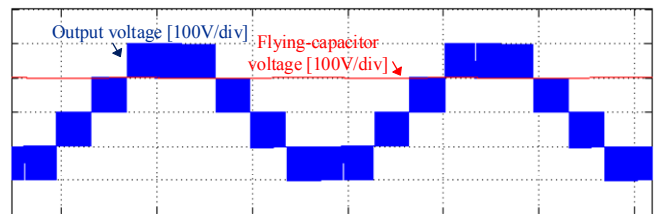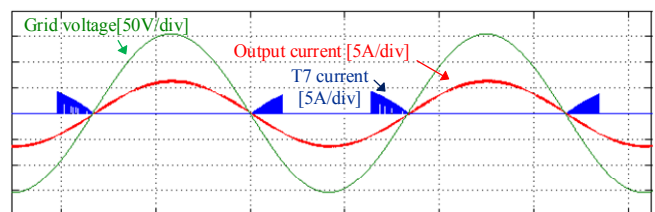

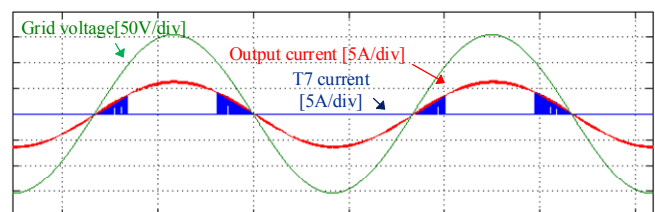(a)Inverter output voltage and flying-capacitor voltage
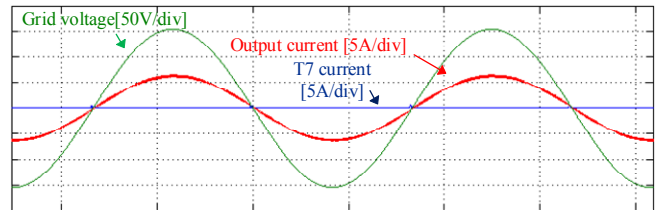
(b)Situation 1: mode D for positive grid cycle and E for negative grid cycle

(c)Situation 2: mode E for positive grid cycle and D for negative grid cycle

(d)Situation 3: mode D for whole grid cycle
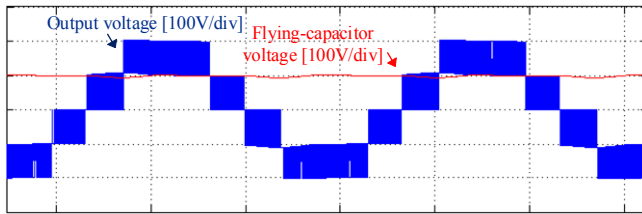

(e)Situation 4: mode E for whole grid cycle

Fig. 5. Active power operation: simulation waveforms of inverter output voltage, flying-capacitor voltage, grid voltage, output current and T_7 current under four switching conditions

Fig.5 (a) shows the five-level bridge voltage and flying-capacitor voltage. As can be seen, the flying-capacitor is capable of obtaining self-balancing at 100V, and the measured ripple voltage is 2V (2%).

The waveforms of currents through T_7 in four different zero switching states combinations are shown in Fig.5 (b) to (e) respectively. In Fig.5 (b), the system is working under situation 1 (mode D for positive grid cycle and E for negative grid cycle): the T_7 current is almost zero, which means no active current is flowing through T_7. Therefore, zero switching states combination in situation 1 is the optimal one among four combinations.

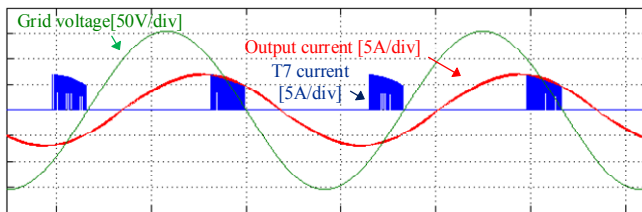### B. Reactive Power operation ($cos\theta = 0.9$)

Under reactive power operation: $cos\theta = 0.9$, simulation waveforms of inverter output voltage, flying-capacitor voltage, grid voltage, output current and T_7 current under four switching conditions are shown in Fig.6.
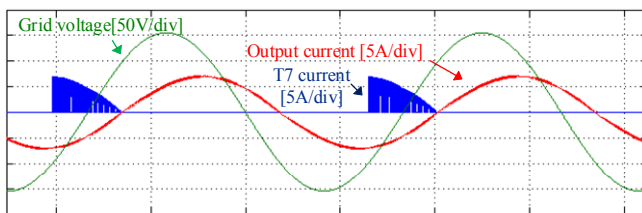

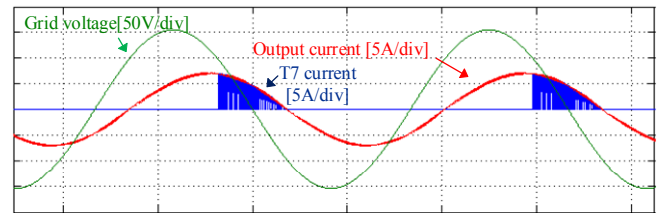(a)Inverter output voltage and flying-capacitor voltage
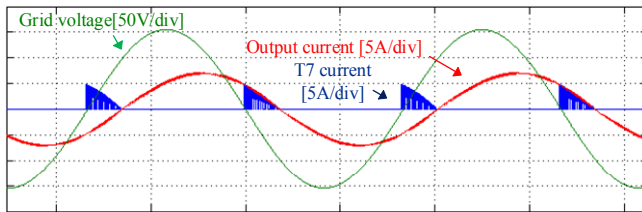
(b)Situation 1: mode D for positive grid cycle and E for negative grid cycle

(c)Situation 2: mode E for positive grid cycle and D for negative grid cycle

(d)Situation 3: mode D for whole grid cycle

(e)Situation 4: mode E for whole grid cycle

Fig. 6. Reactive power operation $cos\theta = 0.9$: simulation waveforms of inverter output voltage, flying-capacitor voltage, grid voltage, output current and T_7 current under four switching conditions

Fig.6 (a) shows the five-level inverter output voltage and FC voltage, which are closed the waveforms in active power operation. The ripple voltages of flying-capacitor in this case is 5V (5%).

Fig.6 (b) to (e) shows the output current, grid voltage and T_7 currents in four situations. According to the analysis in section III, we know that in optimal situation, only reactive current is passing through T_7. Under reactive power condition, there is phase shift between grid voltage and output current. When current and voltage are in opposite direction, the system is entering reactive power zone. In situation 1, which is shown in Fig.6 (b), it is observed that only reactive current is going through switch T_7 (current is flowing through T_7 only in reactive power zones Z1 and Z3). In situation 2, all active current is passing through T_7, which is not desirable. In situations 3 and 4, half active and reactive current is flowing through T_7, which is also not what we need. With simulation results under active and reactive power conditions, it is concluded that mode D for positive grid period and mode E for negative grid cycle is the best combination for proposed 7S-5L-ANPC inverter.

V. EXPERIMENTAL RESULTS

To demonstrate the ability of proposed topology and its modulation strategy. A 500W single-phase 7S-5L-ANPC inverter grid-connection experimental prototype is built, as shown in Fig.7. The system includes main circuit, DSP and FPGA control board, DC source, output filter and measuring instruments. The control board employs a combination of the Texas Instruments TMS320F28335 control card and the Altera Cyclone IV EP4CGX22 FPGA card to provide powerful real-time mathematical calculations and control functions. The experimental parameters are the same as parameters used in simulation, shown in Table II.
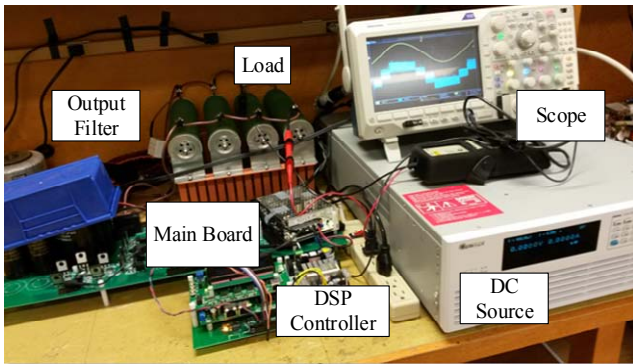
Fig. 7. Experimental prototype

The experimental tests are carried out in two cases: active power operation and reactive power operation.

A. Active Power operation

Fig.8 and Fig.9 show the experimental results under unity power factor condition. Fig.8 shows inverter output voltage, grid voltage, flying-capacitor voltage and output current: channel 1 is the output bridge voltage; channel 2 is $110V_{RMS}$ grid voltage; channel 3 is the flying-capacitor voltage, which is balanced at 100 volts; channel 4 is the output current, which is sinusoidal without distortion and in phase with grid voltage.

Fig.9 shows two DC-link capacitors voltages, flying-capacitor voltage and output current: channel 1 is lower DC-link capacitor voltage and channel 2 is upper DC-link capacitor voltage, which both have a line-frequency fluctuation. The measured flying-capacitor ripple voltage is 3V (3%) and DC-link capacitor ripple voltage is 8V (4%).
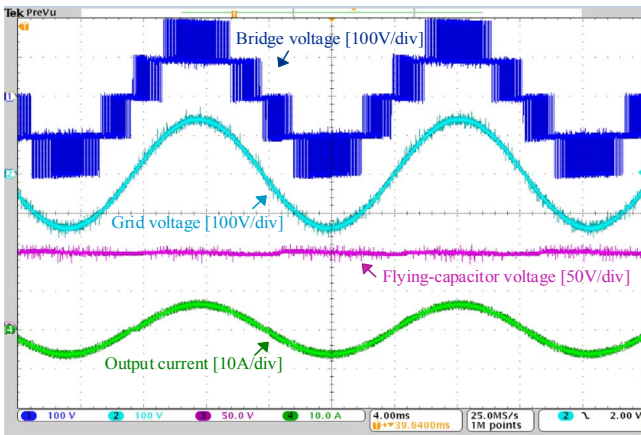

Fig. 8. Experimental results under unity power factor condition: waveforms of inverter bridge voltage, grid voltage, flying-capacitor voltage and output current
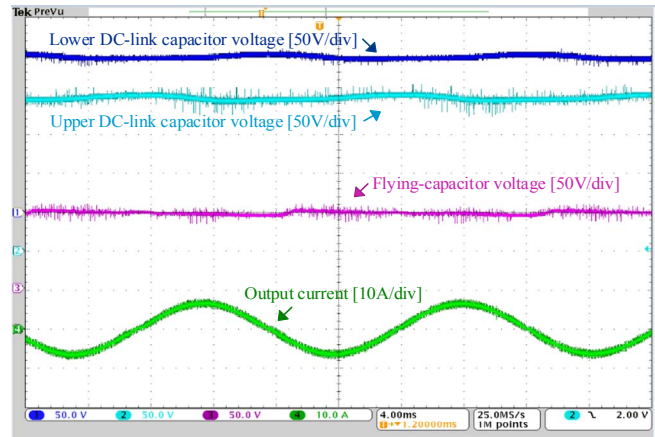

Fig. 9. Experimental results under unity power factor condition: waveforms of lower DC-link capacitor votlage, upper DC-link capacitor voltage, grid voltage and output current

B. Reactive Power operation ($cos\theta = 0.9$)

To testify the proper system operation under reactive power condition, experimental works are carried out. The power factor is 0.9. Experimental results are shown in Fig.10 and Fig.11.

Fig.10 shows inverter output voltage, grid voltage, flying-capacitor voltage and output current. It is observed that the waveform of inverter output voltage V_{Ao} is closed to the waveform in active power condition. The flying-capacitor voltage is also balanced at 100 volts, and measured ripple voltage is 6V (6%). Under 0.9 power factor, the output current and grid voltage has a 25 degree phase shift. In this situation, the inverter still produces good quality current waveform without distortion.

Fig.11 shows two DC-link capacitors voltages, flying-capacitor voltage and output current. The DC-link capacitors voltages waveforms in this situation are almost the same as ones under active power condition. The measured DC-link capacitor ripple voltage is 8V (4%).
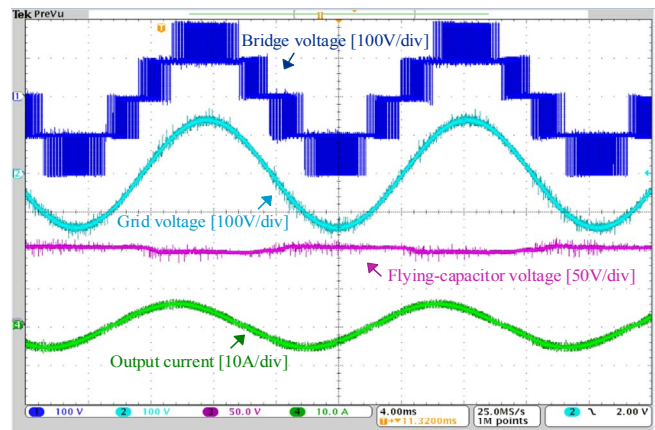
Fig. 10. Experimental results under reacitve power operation $cos\theta = 0.9$: waveforms of inverter bridge voltage, grid voltage, flying-capacitor voltage and output current
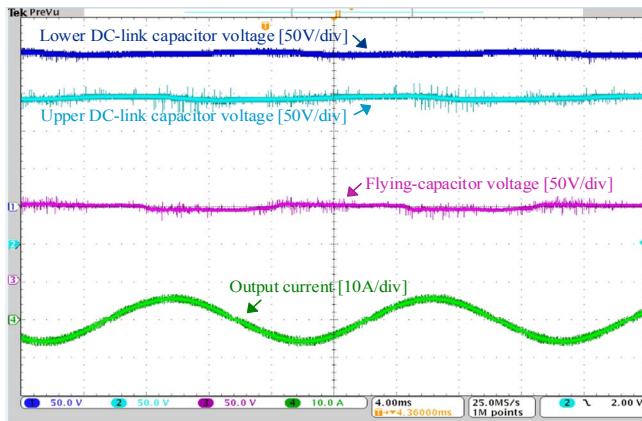

Fig. 11. Experimental results under unity power factor $cos\theta = 0.9$: waveforms of lower DC-link capacitor votlage, upper DC-link capacitor voltage, grid voltage and output current

From the experimental results achieved in two situations, it can be concluded that the with proposed modulation strategy applied on proposed 7S-5L-ANPC inverter, the system is capable of outputting good quality AC current. The flying-capacitor voltage is self-balanced. The ripple voltages of FC voltage and DC-link capacitor voltage are kept within a reasonable range. The effectiveness of proposed topology and modulation method is verified.

VI. CONCLUSION

A novel 7S-5L-ANPC inverter topology with fewer active semiconductor switches is proposed. Compared to traditional five-level ANPC topologies. Only seven active switches are employed. Switch with low current rating can be selected for the seventh switch T_7 because only reactive current is flowing through it. The basic working principles and modulation strategy are explained in this paper. The simulation and experimental results demonstrated the effectiveness of proposed topology and modulation method

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