LED Driver Achieves Electrolytic Capacitor-Less and Flicker-Free Operation with an Energy Buffer Unit

Peng Fang, *Member, IEEE*, Bo Sheng, *Member, IEEE*, Sam Webb, *Student Member, IEEE,* Yan Zhang, *Member, IEEE*, Yan-Fei.Liu, *Fellow, IEEE*

***Abstract*—Electrolytic capacitors are often needed to provide the high-density energy storage required by AC powered LED drivers, however, they are also well known for their short lifespans. Eliminating electrolytic capacitors in AC-DC LED driver design has become a very important target to improve LED driver technology. In this paper, a cycle-by-cycle energy buffering LED driver has been proposed to achieve electrolytic capacitor-less flicker-free operation. An energy buffering unit (EBU), with high voltage film capacitors being the energy storage device, is introduced in the design to buffer the imbalanced energy in every switching cycle. The switching current can be controlled to meet high power factor correction requirement while maintaining DC LED output current at the same time. Compared to previous electrolytic capacitor-less designs, this technology can reduce circulating power and, therefore, power conversion loss. A 15W experimental prototype had been built and tested to verify the proposed LED driving method.**

***Index Terms*—Cycle by cycle energy buffering, Electrolytic Capacitor-less design, LED Driver, Flicker-free operation**

I. Introduction

LED lighting has been steadily increasing in popularity, owing largely to its high efficacy, long lifespan, and environmentally-friendly operation. It is replacing fluorescent lighting and becoming the primary artificial lighting sources in many applications. Although having inherent advantages over fluorescent lighting, there are several technical challenges that need to be overcome to fully take advantage of LED lighting, particularly with the AC powered LED driver. In an AC connected driver, the notorious double-line-frequency flicker, which can cause numerous health issues, will occurs unless the driver is properly designed to eliminate it. Therefore, the key to realizing the full benefits of LED lighting lies in LED driver designs. Also, LED drivers heavily determine the size, efficiency, and cost of LED lighting fixtures, playing a critical role in LED lighting deployment.

EnergyStar requires power factor correction (PFC) to be implemented for lighting devices higher than 5W. The power factor must be higher than 0.9 for commercial usages and 0.7 for residential usages [1], which results in a time-varying input power with a double-line-frequency ripple, as shown in Fig. 1. On the other side, achieving flicker-free LED driving requires constant output power. Therefore, energy buffering for double-line-frequency imbalanced energy is required. Conventional single-stage LED driver uses the simplest form of energy buffering, by paralleling bulky electrolytic capacitors at its output. Part of the ripple power is buffered by the storage capacitor while the remaining escapes to the LED load and, therefore, generates double-line-frequency flicker. Only an infinitely large storage capacitor can buffer 100% of the ripple power using this technique. Thus, double-line frequency flicker is always present with single-stage LED driver based design. The recommended low-risk flicker level should be less than 0.08×fflicker percent of the average [3], which is equivalent to 10% for 120Hz flicker (under 60Hz mains) and 8% for 100Hz flicker (under 50Hz mains), respectively. Commercially available single-stage LED drivers usually exceed the recommended safe level.

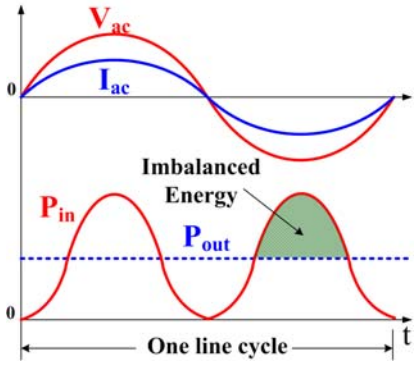


Fig. 1 Energy imbalance between AC input power and expected LED output power with grid-connected LED drivers

Double-line-frequency flicker raises health-related concerns. Although usually not visible, it can be picked up by retina that leads to visual fatigue and other problems [4], [5]. Conventional two-stage LED drivers can naturally achieve flicker-free LED driving. The additional DC-DC stage in a two-stage design can filter the double-line-frequency ripple power. The drawback is additional loss from the extra power stage and higher cost due to the additional components.

A variety of LED driving methods have been investigated to achieve flicker-free LED driving performance while maintaining high efficiency, and low cost. Some focus on novel control strategies while others focus on power topologies. For

Peng Fang is with University of Minnesota, Duluth, MN 55813 USA (fangp@d.umn.edu). He was with Queen's University, Kingston, ON, K7M 3 N6, Canada, from 2011 to 2018.
Yan, Zhang is with Xi'an Jiao Tong University, Xi'an, Shangxi, China. (zhangyanjtu@163.com)
Bo Sheng, Sam Webb and Yan-Fei Liu are with Queen's University, Kingston, ON, K7M 3 N6, Canada. (bo.sheng@queensu.ca, 11sdw4@queensu.ca , yanfei.liu@queensu.ca)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

instance, the harmonic current injection method had been proposed to reduce imbalanced energy in a half line cycle [6]. Similar methods include input or output current shaping [7]-[9]. They can lessen the severity of flicker but cannot completely remove it. There are also two-stage integration methods [10]-[12] that share components between the first and the second power stages, leading to a reduction in component count and lower cost. However, optimal operation is difficult to achieve because of extra constraints from component sharing. Ripple cancellation methods [14]-[18] have also been proposed to achieve flicker-free operation. An opposite ripple voltage is produced to cancel the double-line-frequency ripple voltage from main PFC circuit. A DC LED voltage and LED current can be produced to achieve flicker-free operation. This method can achieve very good efficiency and reduce requirement on storage capacitors. It is possible to achieve electrolytic capacitor-less design, but only for high LED output voltage applications [17].

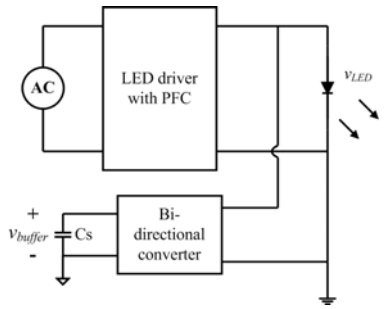


Fig. 2 General implementation of active filtering LED driver [21]

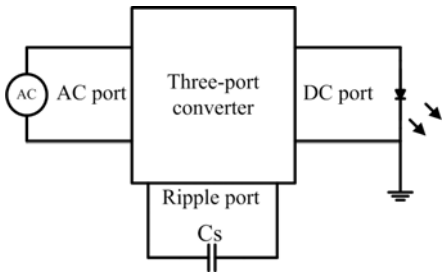


Fig. 3 Generic implementation of three-port electrolytic capacitor-free LED driver [23]

In addition to eliminating flicker, one other important research area for LED drivers is eliminating electrolytic capacitors. Electrolytic capacitors are often used as high-density energy storage device, buffering the double-line-frequency imbalanced energy. However, it compromises system life. Like other semiconductor devices, LEDs can last for decades. On the other side, the lifespan of electrolytic capacitors is an order of magnitude less [19]. Therefore, eliminating them in LED driver designs becomes paramount.

High voltage film capacitors have sometimes been used as storage capacitors to replace electrolytic capacitors. By allowing a large double-line-frequency ripple voltage on the high voltage film capacitor, small capacitors, usually in the range of a few microfarads, can be used. Designs come in different forms under this basic concept. There are active filter methods [20]-[22] that parallel a bidirectional DC-DC converter to a LED load, as shown in Fig. 2. The bi-directional converter serves as an infinite capacitor. When Pin > PLED, the bi-directional converter transfers extra energy to the film capacitor; When Pin < PLED, the energy is transferred back to the LED load from the film capacitors. In general, active filter LED drivers generate quite sizeable loss. The half line cycle imbalanced energy, which is around 1/3 of the total delivered energy, goes through three power convesion steps. Firstly, when $P_{in} > P_{LED}$, the imbalanced energy is transferred from AC input side to DC output side. Secondly, it is then transferred from DC output side to the storage capacitors. Thirdly, when $P_{in} < P_{LED}$, the energy in the storage capacitor is transferred back to the LED output. Because of excessive power circulation, the projected efficiency is much lower than a conventional single-stage LED driver, and this is evidenced in [21]. Similarly, there are also three-port power decoupling methods [23]-[27] that dedicate a third port for ripple power, as shown in Fig. 3.

A cycle by cycle current energy buffering Flyback LED driver has been proposed in this paper. It can be considered as an alternative three-port LED driver, but with completely different operating principle. The method treats imbalanced energy at switching frequency level, resulting in the following benefits:

(1) The imbalanced energy experiences one less circulation through the system. When $P_{in} > P_{LED}$, the imbalanced energy is directly transferred from the AC input to the storage capacitors. The imbalanced energy only experiences one power conversion step during this process instead of two times in active filtering and previous three port LED drivers, which results in a higher efficiency.

(2) The maximum energy that needs to be stored in the main Flyback transformer, in every switching cycle, is half the amount that of conventional designs and other three-port LED drivers. With the proposed design, the maximum energy that needs to be stored in the Flyback transformer is constant in every switching cycle and proportional to the LED output power. On the contrary, with conventional or other electrolytic capacitor-less design, the maximum energy that needs to be stored in the Flyback transformer is proportional to the peak input power, which is double the amount of the LED output power. Therefore, a smaller magnetic core can be used for the main Flyback transformer and the current stress for power components is reduced, allowing for lower current rated devices to be used.

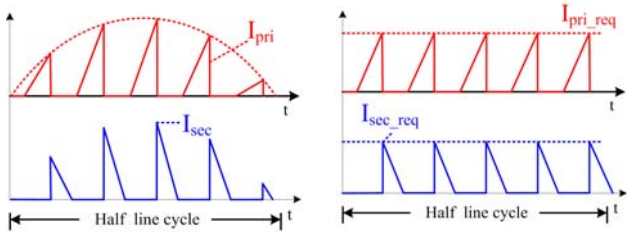
(3) Primary side control can be easily implemented with the proposed LED driver. The signals required to build the LED current regulation loop can be sensed at the primary side. Eliminating the need for a secondary side control circuit can achieve reduced design complexity and cost.

The remaining part of this paper is organized as follows. Section II presents the design concept and operating principle of the proposed LED driver. Section III discusses the component requirement. Control scheme is discussed in section IV and the loss analysis is provided in Section V. The design procedure and consideration are discussed in Section VI. The simulation and experimental result are presented in Section VII and finally, the paper is concluded in Section IX.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

II. Design Concept And Operating Principle

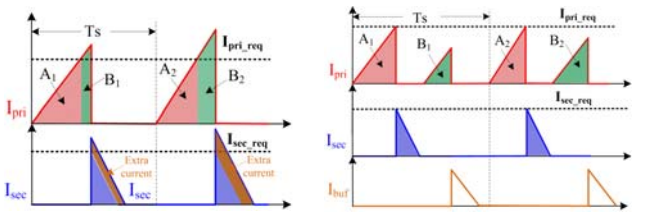
For a conventional single-stage LED driver, power factor correction and DC LED output power cannot be achieved at the same time. A Flyback LED driver operating under discontinues current conduction mode (DCM) is used as an example to illustrate this point. Fig. 4(a) shows the primary side and the secondary side switching current, I_{pri} and I_{sec}, of a conventional Flyback LED driver when power factor correction is performed. Fig. 4(b) shows the required primary side and secondary side switching current that can deliver constant LED output current. As shown, performing power factor correction requires the peak primary side switching current to follow the input voltage. On the contrary, delivering constant LED output power requires identical secondary side switching current in every switching cycle. Therefore, the switching current waveforms need to be changed to bridge the different requirements of these two.



(a) (b)

Fig. 4 Primary side and secondary side switching current waveforms, (a) conventional Flyback LED driver with PFC implementation, (b) expected waveforms to achieve constant LED current output

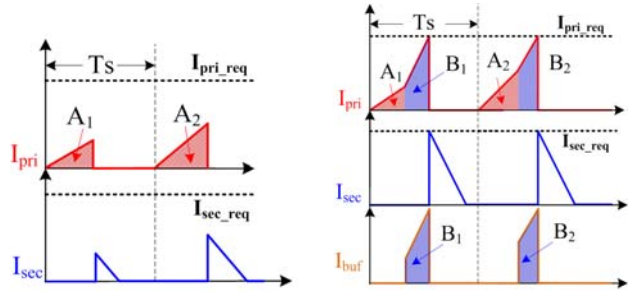
Fig. 5 shows two different patterns of switching current when $P_{in} > P_{LED}$. Fig. 5(a) shows the switching current in a conventional design. When power factor correction is performed, the peak primary side switching current is higher than Ipri_req, which is the amount required from LED output. Fig. 5(b) shows the conceptual change on the switching current. The current drawn from AC input happens in two occasions and the area A1(or A2) and B1(or B2) are used to represent them. When the primary side switching current hits I_{pri_req}, the primary side current is ended as the switch controlling it is turned off. The magnetic current commutes to the secondary side and the extra amount of current is delivered to the LED output. When Isec becomes zero, more primary side current is drawn from AC input, as represented by area B1, to meet the requirement from power factor correction. The area B1 in Fig. 5(b) is equal to the area B1 in Fig. 5(a). Therefore, the total current drawn from AC input depicted in Fig. 5(b) is the same as it is depicted in Fig. 5 (a). After the second portion of primary side current, the energy stored in the transformer is used to charge another conceptual load instead of feeding the LED output. The remaining energy is represented by the magnetic current, I_{buf}.



(a) (b)

Fig. 1 Illustration of switching current when $P_{in} > P_{LED}$, (a) conventional design waveforms, (b) conceptual waveforms achieve energy buffering

Fig. 6 shows two different patterns of switching current when $P_{in} < P_{LED}$. Fig. 6(a) represents the waveforms in a conventional design. The primary side switching current is terminated when enough current is drawn from AC input, as represented by area A1, for power factor correction. In this condition, the peak primary side switching current is still lower than Ipri_req, the amount required for constant LED output current. Fig. 6(b) shows a conceptual change on the switching current. After enough current is drawn from AC input, also represented by area A1, the remaining primary side switching current is supplied by a conceptual source and is also represented by I_{buf}. As the current drawn from AC input is the same in both cases, the power factor correction performance is maintained. The primary side switching current stops when it hit Ipri_req. The extra current supplied by the conceptual source also means extra energy supplied by the conceptual source.



(a) (b)

Fig. 6 Illustration of switching current when $P_{in} < P_{LED}$, (a) conventional design waveforms, (b) conceptual waveforms achieve energy buffering

A storage capacitor can serve as the voltage source when $P_{in} < P_{LED}$. It can also serve as the load when $P_{in} > P_{LED}$. Therefore, in every switching cycle, the imbalanced energy is buffered by the energy storage capacitor. To achieve the above current repatterning concept, an interfacing circuit needs to be designed between the storage capacitor and a conventional LED driver and the proposed LED driver is shown in Fig. 7.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

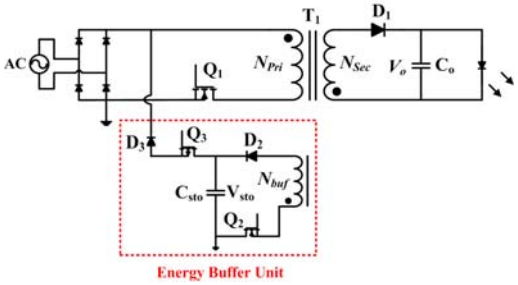


Fig. 7 The proposed cycle by cycle energy buffering LED driver

The power stage is based on the Flyback topology with an extra energy buffer unit (EBU) to achieve high power factor and constant current output in every switching cycle. When $P_{in} < P_{LED}$, the additional energy is supplied from the storage capacitor, C_{sto}, to the LED load. When $P_{in} > P_{LED}$, the extra energy is stored into C_{sto}. The output capacitor C_o is implemented by a 10μF ceramic capacitor in the experimental prototype to filter the switching frequency ripple. The storage capacitor, C_{sto}, is implemented with a 2 x 3.3μF, 450V film capacitor. The switching operations during $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ are different and they will be discussed separately.

A. Operation when $P_{in} < P_{LED}$

The LED driver is operated under discontinues conduction mode (DCM) with four distinct time intervals, [t_0-t_1], [t_1-t_2], [t_2-t_3], [t_3-t_4] in one switching cycle. The critical switching waveforms are shown in Fig. 8.

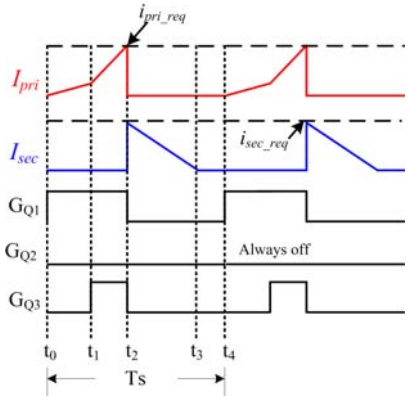


Fig. 8 Key switching waveforms of the proposed LED driver when $P_{in} < P_{LED}$

During [t_0-t_1]

Fig. 9(a) illustrates the circuit operation during the time interval [t_0-t_1] when $P_{in} < P_{LED}$. The MOSFET Q_1 is turned on at t_0 and current is drawn from the AC input. Because the primary side winding, N_{pri}, is oriented in Flyback mode with respect to the secondary side windings, N_{sec}, and buffer winding, N_{buf}, the diode D_1, D_2 are reverse biased. During this time interval, Q_2 and Q_3 are off. The body diode of Q_2 is forward biased. The voltage on D1 can be expressed as:

$$V_{D1\_(P_{in}<P_{LED})}[t_0 - t_1] = V_o + V_{in} \times \frac{N_{pri}}{N_{sec}} \qquad (1)$$

The voltage on diode D2 can be expressed as:

$$V_{D2\_(P_{in}<P_{LED})}[t_0 - t_1] = V_s + V_{in} \times \frac{N_{buf}}{N_{pri}} \qquad (2)$$

The voltage, Vsto, is designed to be higher than Vin_rec when $P_{in} < P_{LED}$. Therefore, the diode D_3 is forward biased, and the body diode of Q_3 is reverse biased. The voltage across Q_3 can be expressed as:

$$V_{Q3\_(P_{in}<P_{LED})}[t_0 - t_1] = V_{sto} - V_{in\_rec} \qquad (3)$$

This interval ends at time t1 when the switching current drawn from the AC input reaches the level required for power factor correction.

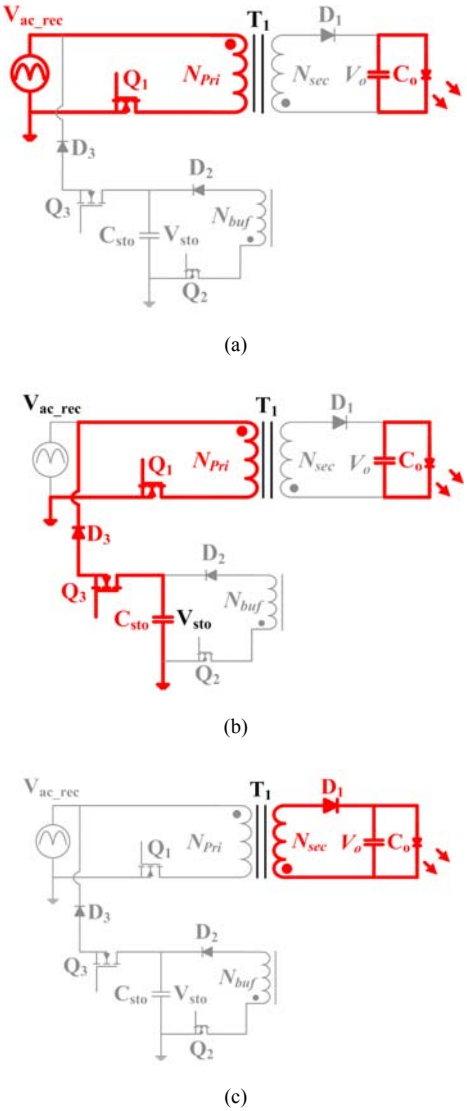


Fig. 9 Switching operation when $P_{in} < P_{LED}$, (a) during [t_0-t_1], (b) during [t_1-t_2], (c) during [t_2-t_3]

During [t_1-t_2]

Fig. 9(b) illustrates the circuit operation during the time interval [t_1-t_2]. The MOSFET Q_3 is turned on at t_1 and Q_1 is remaining on. Because V_{sto} is higher than V_{in_rec}, the input

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

bridge rectifier is reversed biased, and there is no more current drawn from the AC input during this time interval. C_{sto} provides the switching current in primary side winding instead. No AC input current during $[t_1\text{-}t_2]$ is desirable as enough AC current had been drawn for power factor correction during $[t_0\text{-}t_1]$. D_1 and D_2 are still reverse biased, and Q_2 is forward biased. As the voltage on the primary side winding becomes Vsto, the voltages on diode D_1 and D_2 during this time interval also change and become:

$$V_{D1\_(P_{in}<P_{LED})}[t_1-t_2]=V_o+V_s\times\frac{N_{pri}}{N_{\sec}} \quad (4)$$

$$V_{D2\_(P_{in}<P_{LED})}[t_1-t_2]=V_s+V_s\times\frac{N_{buf}}{N_{pri}} \quad (5)$$

This time interval ends at time t_2 when the primary side switching current hits Ipri_req, which represents the current level required for delivering a constant LED output current. Ipri_req is automatically generated by a feedback loop that will be discussed in Section V. Both Q_1 and Q_3 are turned off at t_2.

During $[t_2\text{-}t_3]$

Fig. 9(c) illustrates the circuit operation during the time interval $[t_2\text{-}t_3]$. As Q_1, Q_3 are turned off at t_2 and Q_2 is still off, the magnetic current is forced to commute from the winding N_{pri} to the winding N_{sec}. The voltage on the secondary side winding is clamped at V_o with ignoring the forward voltage drop on D_1. The voltage on the secondary side winding is reflected to the primary side winding and the buffer winding. The voltage across the primary side winding can be expressed as:

$$V_{Npri\_(P_{in}<P_{LED})}[t_2-t_3]=V_o\times\frac{N_{pri}}{N_{\sec}} \quad (6)$$

The voltage on Q_1 can, therefore, be expressed as:

$$V_{Q1\_(P_{in}<P_{LED})}[t_2-t_3]=V_{in\_rec}+V_o\times\frac{N_{pri}}{N_{\sec}} \quad (7)$$

The voltage across winding N_{buf} can be expressed as:

$$V_{Nbuf\_(P_{in}<P_{LED})}[t_2-t_3]=V_o\times\frac{N_{buf}}{N_{\sec}} \quad (8)$$

In the proposed LED driver, V_{sto} is designed to be always smaller than the voltage on the buffer winding during $[t_2\text{-}t_3]$ given by Eq. (8). Therefore, the diode D_2 is forward biased while the body diode of Q_2 is reverse biased. The voltage on Q_2 can be expressed as:

$$\begin{aligned}&V_{Q2\_(P_{in}<P_{LED})}[t_2-t_3]\\&=V_{Nbuf\_(P_{in}<P_{LED})}[t_2-t_3]-V_{sto}\\&=V_o\times\frac{N_{buf}}{N_{\sec}}-V_{sto}\end{aligned} \quad (9)$$

The status of D_3 and Q_3 is the same as it is in the interval $[t_0\text{-}t_1]$. The magnetic current in winding N_{sec} starts decreasing at t_2 and becomes zero at t_3, which ends this time interval.

During $[t_3\text{-}t_4]$

An idle interval $[t_3\text{-}t_4]$ is followed to achieve DCM operation. No active switching operation happens in this interval.

B. Operation when $P_{in} > P_{LED}$

When $P_{in} > P_{LED}$, the extra energy is transferred from the AC input to the storage capacitor Csto in every switching cycle. Fig. 10 shows the key switching waveforms with one switching cycle being divided into five time intervals, $[t'_0\text{-}t'_1]$, $[t'_1\text{-}t'_2]$, $[t'_2\text{-}t'_3]$, $[t'_3\text{-}t'_4]$ and $[t'_4\text{-}t'_5]$.

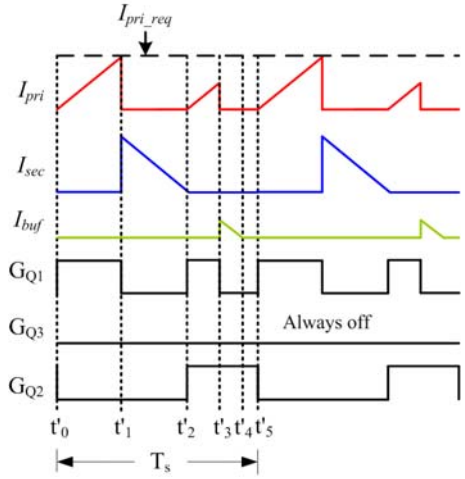


Fig. 10 Key switching waveforms of the proposed LED driver when $P_{in} > P_{LED}$

During $[t'_0\text{-}t'_1]$

Fig. 11(a) shows the circuit operation during the time interval $[t'_0\text{-}t'_1]$ when $P_{in} > P_{LED}$. It is the same as Fig. 9(a) when $P_{in} < P_{LED}$. Therefore, (1) and (2) can be reused to describe voltage stresses of D_1 and D_2. The voltages on Q_3 and D_3 are depended on the instantons value of V_{in_rec} and V_{sto}. Both V_{in_rec} and V_{sto} change in a half line cycle and the situation can change between $V_{in\_rec} > V_{sto}$ and $V_{in\_rec} < V_{sto}$. The voltage on Q_3 and D_3 can be expressed as:

$$V_{D3\_(P_{in}>P_{LED})}[t'_0-t'_1]=\max\{(V_{in\_rec}-V_{sto}),0\} \quad (10)$$

and

$$V_{D3\_(P_{in}>P_{LED})}[t'_0-t'_1]=\max\{(V_{sto}-V_{\max}),0\} \quad (11)$$

As Q_3 is always off when $P_{in} < P_{LED}$, the voltage stresses of Q_3 and D_3 remain unchanged in the entire switching cycle. At t_1, the primary side winding reaches I_{pri_req} and Q_1 is turned off. One should note that the current drawn from the AC inpt is not sufficient to perform power factor correction yet at t_1. More current will be drawn from AC input during the time interval $[t'_2\text{-}t'_3]$.

During $[t'_1\text{-}t'_2]$

Fig. 11(b) shows the circuit operation during the time interval $[t'_1\text{-}t'_2]$ when $P_{in} > P_{LED}$. It is the same as Fig. 9(b). Therefore, (7) and (9) can be reused to describe voltage stress

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

for each component. This interval ends at t'_2 when the secondary side current drops to zero.

During [t'_2-t'_3]

Fig. 11(c) shows the circuit operation during the time interval [t'_2-t'_3] when $P_{in} > P_{LED}$. Q_1 is turned on again at t_2 to draw more current from AC input. The voltage stresses of the components in [t'_2-t'_3] are the same as they are in [t'_0-t'_1]. This time interval ends at t_3 when the exact amount of current required for power factor correction is drawn from AC input.

During [t'_3-t'_4]

Fig. 11(d) shows the circuit operation during the time interval [t'_3-t'_4] when $P_{in} > P_{LED}$. Since Q_1 is turned off at t_4 and the Q_2 is already on, the magnetic current commutes from winding N_{pri} to winding N_{buf}. The magnetic current does not flow in secondary side winding because of the following relationship in the design:

$$V_{sto} \times \frac{N_{sec}}{N_{buf}} < V_o \tag{12}$$

When the magnetic current flows in winding N_{buf}, the voltage on the winding is clamped at V_{sto}. The term on the left side of the "less than" sign of (12) is equal to the voltage reflected to the secondary side winding at the time. Therefore, the LED output voltage during [t'_3-t'_4] is higher than the secondary side winding voltage and the diode D_1 is reverse biased to block current. The voltage across D_1 can be expressed as:

$$V_{D1\_(P_{in}>P_{LED})}[t_3 - t_4] = V_o - V_{sto} \times \frac{N_{sec}}{N_{buf}} \tag{13}$$

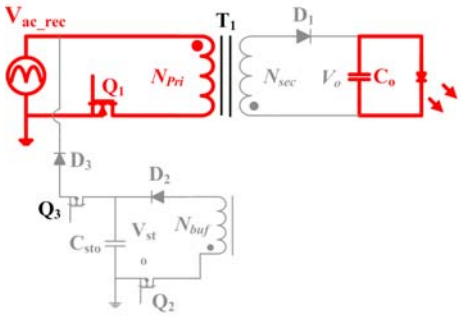
The voltage on the buffer winding is also reflected to the primary side winding, and the voltage on Q_1 can be expressed as:

$$V_{Q1\_(P_{in}>P_{LED})}[t_3 - t_4] = V_{in} + V_{sto} \times \frac{N_{pri}}{N_{buf}} \tag{14}$$

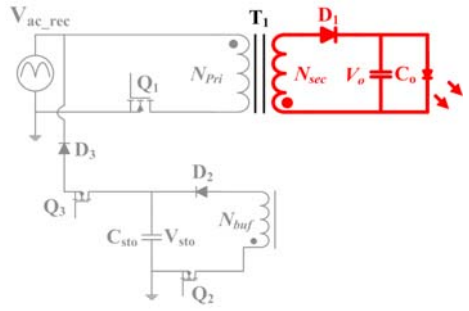
This time interval ends at t_4 when the magnetic current in winding N_{buf} decreases to zero.

During [t'_4-t'_5]

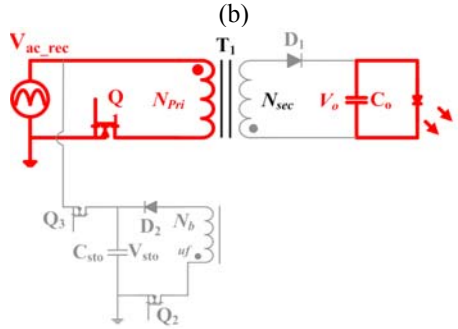
A small idle time interval [t'_4-t'_5] is used to achieve DCM operation. No active switching operation happens in this interval.



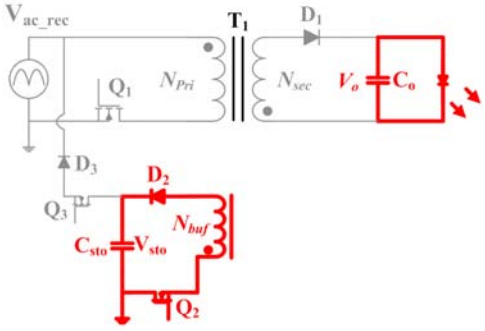
(a)



(b)



(c)



(d)

Fig. 11 Switching operation when Pin > PLED, (a) during [t'_0-t'_1], during [t'_1-t'_2], during [t'_2-t'_3], during [t'_3-t'_4]

C. Overall operation in a half line cycle

Since the switching operations under both $P_{in}<P_{LED}$ and $P_{in}>P_{LED}$ have been discussed, the overall view of the operation in a half line cycle is illustrated in Fig. 12.

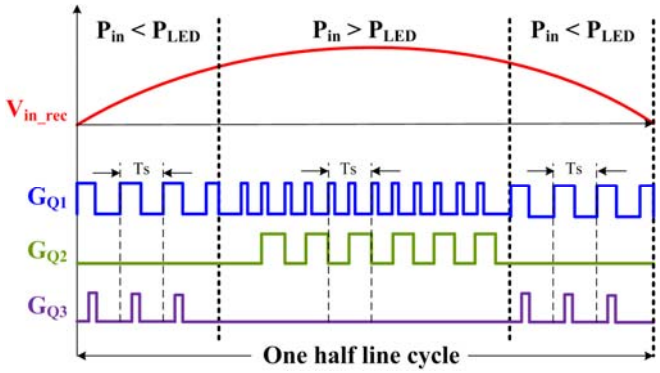


Fig. 12 Switching operation over a half line cycle

The above discussion also reveals that the imbalanced energy had only gone through two power conversion steps. When $P_{in} > P_{LED}$, the imbalanced energy is transferred from AC input side to the storage capacitor, directly. When $P_{in} < P_{LED}$, it

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

is then transferred from the energy storage capacitor to the LED output side. One less power conversion step is required with the proposed LED driver as compared to active filter and previous three-port LED drivers.

III. Component Requirement Analysis

A. Component Voltage Stress

As the expressions of the component voltage stresses have been derived in each time interval, the maximum voltage stress expression for them in a half line cycle are summarized and shown in TABLE 1. The maximum voltage stresses for them are calculated/simulated in the right column according to the circuit parameters from TABLE 3.

TABLE 1 Maximum voltage stress of each component under 110Vrms Input

Q_1	$V_{sto\_max}+V_o\times\frac{N_{pri}}{N_{sec}}$	350V
D_1	$V_{sto\_max}\times\frac{N_{sec}}{N_{pri}}+V_o$	117V
Q_2	$V_o\times\frac{N_{buf}}{N_{sec}}-V_{sto\_min}$	130V
D_2	$\max\left[V_{in\_rec}(t)\times\frac{N_{buf}}{N_{pri}}+V_{sto}(t)\right]$	310V
Q_3	$\max\left[V_{sto}(t)-V_{in\_rec}(t)\right]$	150V
D_3	$\max\left[V_{in\_rec}(t)-V_{sto}(t)\right]$	10V

B. Component Current Stress

The switching current in Q_1 peaks at t_2 when $P_{in} < P_{LED}$. It is equal to I_{pri_req} that is generated by the feedback loop. The switching current in Q_1 peaks two times at t_1 and t_3, respectively, when $P_{in} > P_{LED}$. The peak current at t_1 is also equal to I_{pri_req} while is smaller at t_3 except, when $P_{in}=2P_{LED}$, the peak current at t_1 and t_3 are equal. Therefore, the maximum current stress of Q_1 in a half line cycle is equal to the I_{pri_req}. There is current in D_3 and Q_3 during $[t_1\text{-}t_2]$ when $P_{in} < P_{LED}$. The maximum current stress for D_3 and Q_3 is I_{pri_req} as well. In every switching current, the energy delivered to the LED load, E_{sec}, can be expressed as:

$$E_{LED}=\frac{1}{2}\times I_{pri\_req}^2\times L_{pri} \tag{15}$$

At the same time, E_{LED} can also be expressed as:

$$E_{LED}=I_{LED}\times V_o\times T_s \tag{16}$$

Combining Eq. (15) and Eq. (16) yields:

$$I_{pri\_req}=\sqrt{\frac{2\times P_{LED}\times T_s}{L_{pri}}} \tag{17}$$

Eq. (17) describes the relationship between I_{pri_req} and I_{LED}. Once the circuit parameters, I_{LED}, V_o, T_s and L_{pri} are determined, I_{pri_req} can be calculated. I_{pri_req} is calculated to be 1A at 15W output power with the circuit parameter from TABLE 3. The maximum current stress with D_1 can be expressed as:

$$I_{D1\_max}=I_{sec\_pk}=I_{pri\_req}\times\frac{N_{pri}}{N_{sec}} \tag{18}$$

The maximum current of D_1 is calculated to be 3A. The maximum current in D_2 and Q_2 occurs when $P_{in} = 2P_{LED}$. Under this situation, the primary side current at t_3 is equal to I_{pri_eq} as well. Therefore,

$$I_{D2\_max}=I_{Q2\_max}=I_{LED\_req\_pri}\times\frac{N_{pri}}{N_{buf}} \tag{19}$$

The maximum current with D_2 and Q_2 is calculated to be 1A.

It is worth mentioning again that the proposed LED driver allows the use of a smaller core for the transformer and low current rating components. In every switching cycle, the peak secondary side current is the same and corresponds to a constant output power, P_{LED}. In a conventional design or previous active filtering LED drivers, the maximum power delivered to the secondary side is equal to $2P_{LED}$. Therefore, the maximum energy that must be stored in the transformer in the proposed design is only half the amount of these previous designs, which permits using a smaller transformer core and low current rating components.

C. Storage Capacitor Requirement

The high voltage film capacitor C_{sto} is used to buffer the imbalanced energy in a half line cycle. The value of C_{sto} is determined by the amount of imbalanced energy and the designed voltage range for V_{sto}. The relationship among the imbalanced energy, E_{buffer}, the minimum voltage of V_{sto}, and the maximum voltage of V_{sto} can be expressed as:

$$\begin{aligned}E_{buffer}&=\frac{1}{2}C_{sto}\times(V_{sto\_max}^2-V_{sto\_min}^2)\\&=C_{sto}\times V_{sto\_avg}\times V_{sto\_pp\_rip}\end{aligned} \tag{20}$$

Where

$$V_{sto\_avg}=\frac{V_{sto\_max}+V_{sto\_min}}{2} \tag{21}$$

And

$$V_{sto\_pp\_rip}=V_{sto\_max}-V_{sto\_min} \tag{22}$$

V_{sto_avg} represents the average voltage of V_{sto} and $V_{sto\_pp\_rip}$ represents the double-line-frequency peak to peak ripple voltage of V_{sto}. Rearranging Eq. (22) yields:

$$C_{sto}=\frac{E_{imbalance}}{V_{sto\_avg}\times V_{sto\_pp\_rip}} \tag{23}$$

At the same time, E_{buffer} can also be expressed as:

$$E_{buffer}=\frac{1}{\pi}P_{LED}\times\frac{1}{2}\times T_{line} \tag{24}$$

Combining Eq. (23) and (24)yields:

$$C_{sto}=\frac{P_{LED}\times T_{line}}{2\pi\times V_{sto\_avg}\times V_{sto\_pp\_rip}} \tag{25}$$

Eq.(25) reveals that the capacitance of C_{sto} is reversely proportional to the average voltage V_{sto_avg} and the peak to peak ripple amplitude $V_{sto\_pp\_rip}$. When a higher average voltage V_{sto_avg} and / or a larger ripple amplitude $V_{sto\_pp\_rip}$ is designed in the proposed LED driver, C_{sto} can be reduced to achieve

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

TABLE 2 STORAGE CAPACITOR REQUIREMENT COMPARISON BETWEEN DIFFERENT LED DRIVING SOLUTIONS

Topology	Storage Capacitor Requirement
Single-stage Flyback LED driver	**Voltage rating**: can be decided based on the LED voltage **Capacitance**: High. Determined by the requirement of flicker level. Electrolytic capacitors are required to implement the storage capacitor. Example: 1mF electrolytic capacitors are used on a 12W, 41V LED driver [30]. The normalized capacitance per wattage is 83uF/W.
Two-stage Flyback + Buck LED driver	**Voltage rating**: can be decided based on LED voltage. The Bus voltage is usually designed to be the LED voltage plus a reasonable voltage margin for proper Buck converter operation. For example, 63V voltage rated capacitors can be used when the maximum LED voltage is 50V. **Capacitance**: High. Determined by the acceptable Bus voltage ripple. Usually implemented by electrolytic capacitors. Example: 1mF, 63V, electrolytic capacitors are used in a 30W, 45V, two-stage LED driver design [31]. The normalized capacitance per wattage is 33uF/W.
Proposed cycle by cycle energy buffering LED driver	**Voltage rating**: High. The storage capacitors are biased at high voltage (usually 100V to 300V voltage) and allow a high peak to peak double line frequency voltage ripple. The voltage rating of the storage capacitor is not linked to the LED voltage. **Capacitance**: Low. A few microfarads to enable film capacitor implementation. Eq.(25) can be used to calculate the required capacitor. Example: 2 x 3.3μF, 300V film capacitors are used in the proposed LED driver. The normalized capacitance per wattage is 0.44uF/W in the proposed design.
Previous active filter LED driver	The rule to select the storage capacitor is the same as the proposed LED driver.

(b) gate driving logic when $P_{in} < P_{LED}$, (c) gate driving logic when $P_{in} > P_{LED}$, (d) operation flow of the proposed LED driver in a switching cycle

electrolytic capacitor-free design. The energy storage capacitors requirement of the proposed LED driver will be compared to the requirement of other LED driving technologies and the result is summarized in TABLE 2.

IV. CONTROL STRATEGY

Fig. 13 (a) shows the control diagram of the proposed energy buffering LED driver and Fig. 13(b) & (c) give the example gate driving logic for both $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$. There are two control loops, LED current loop and Vsto voltage loop in the system.

In the Vsto voltage loop, the averaged voltage of Vsto, V_{sto_avg}, is compared with its reference, V_{sto_ref}. The compensated error, V_{s_comp} multiples the scaled input voltage, $V_{in\_rec\_s}$, and the result becomes the reference of the AC input current. The average input current is obtained by taking I_{pri_sns}, for integration in every switching cycle. The result, Iin_avg, is compared with I_{in_ref}. Once I_{in_avg} hits I_{in_ref}, no more current will be drawn from AC input. Therefore, power factor correction is achieved. The voltage feedback loop determines the AC input current to achieve Vsto_avg regulation.

Fig. 13 (b) illustrates the corresponding gate driving signal when $P_{in} > P_{LED}$. At time t_0, Q_1 is turned on. I_{in_avg} is the integrated result of I_{pri_sns}. I_{pri_sns} hits I_{pri_req} at time t_1 while I_{in_avg} is still lower than I_{in_ref}. The control system identifies Pin>PLED. Q_1 is turned off at time t_1 and magnetic current commutes from primary side to secondary side. At time t_2, the secondary side current drops to zero and generates a signal ZCD. During [t_1-t_2], I_{in_avg} is constant as there is no current from AC input. Q_1 is turned on again at t_2 and I_{pri_sns} starts rising from zero. Q_2 is also turned on at t_2. I_{in_avg} continues increasing until t_3, when I_{in_avg} hits I_{in_ref}. Q_1 is turned off at t_3 while Q_2 remains on. The magnetic current commutes from primary side to auxiliary side.

Fig. 13 (c) illustrate the corresponding gate driving signals when $P_{in} < P_{LED}$. At time t_0, Q_1 is turned on. I_{in_avg} is the integrated result of I_{pri_sns}. I_{in_avg} hits I_{in_ref} at t_1 while I_{pri_sns} is still lower than I_{pri_req}. The control system identifies $P_{in} < P_{LED}$. Therefore, Q_3 is turned on at t_2 and no more current will be drawn from AC input. The primary side switching current keeps increasing until t_3, when I_{pri_sns} hits I_{pri_req}. Both Q_1 and Q_3 are turned off then and the switching current commutes to secondary side.

It is worth mentioning that the proposed LED driving method enables primary side current regulation. Under steady state, the peak secondary side current in every switching cycle is described by (18). The secondary side current conduction time, which corresponds to (t_3-t_2) in Fig. 8 and (t'_2-t'_1) in Fig. 10, can be sensed by detecting winding voltages. Therefore, the averaged secondary side current in one switching cycle can be expressed as:

$$I_{LED} = \frac{I_{sec\_pk} \times T_{dis}}{2 \times T_s} \tag{26}$$

Where T_{dis} is equal to (t_2-t_1) in Fig. 8 and (t'_3-t'_2) in Fig. 10. Combining Eq. (18) and (26) yields:

$$I_{LED} = \frac{I_{LED\_req\_pri} \times T_{dis} \times N_{pri}}{2 \times T_s \times N_{sec}} \tag{27}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

Once I_{pri_req} and T_{dis} are available, the LED current can be estimated without additional sensing on the secondary side. [28] and [29] have the details of primary side circuit sensing technology and will not be further discussed in this paper.

Fig. 14 illustrates the high level power flow of the proposed cycle by cycle energy buffering LED driver. When $P_{in} < P_{LED}$, the storage capacitor will supply the amount of power, $P_{LED} - P_{in}$, to the LED load. When $P_{in} > P_{LED}$, the extra power from the AC input, $P_{in}-P_{LED}$, will be directed to be stored in the storage capacitor.

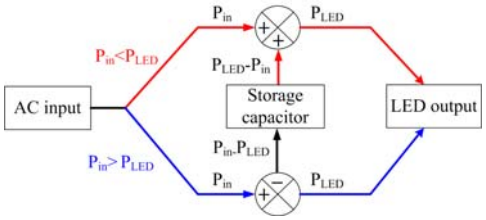


Fig. 14 Power flow of the proposed cycle by cycle energy buffering LED driver

V. Loss Analysis

In this section, a loss analysis of the proposed cycle by cycle energy buffering LED driver, as well as the previous active filtering, LED driver will be performed. To fairly compare the losses from both designs, the parameters of MOSFETs and diodes used in the analysis are standardized. In this way, the analysis has a much less dependence on the components parameter, and the result can strongly reflect the advantages/disadvantages of each design from the perspective of power circuit topology and operation condition. For the proposed cycle by cycle energy buffering LED driver, the following losses had been identified.

For MOSFET Q_1, under both $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ operating condition, there are conduction loss during $[t_0\text{-}t_1]$, output capacitor switching loss at t_0. When $P_{in} < P_{LED}$, there is turn off overlap switching loss at t_2. When $P_{in} > P_{LED}$, there is turn off overlap switching loss at t_1 and t_3.

For MOSFET Q_2, there is only conduction loss during $[t_3\text{-}t_4]$ when $P_{in} > P_{LED}$. One should note that the body diode of Q_2 is forward biased before it is turned on. Therefore, there is no turn on overlap switching loss and output capacitor switching loss. There is no turn off switching loss with Q_2 as well since the switching current in it is already zero before Q_2 is turned off.

For MOSFET Q_3, there is turn on overlap switching loss and output capacitor switching loss at t_1 when $P_{in} < P_{LED}$. There is no turn off switching loss with Q_3 since its switching current is already zero before Q_3 is turned off (turn off Q_1 at t_2 terminates the switching current).

For diode D_1, there are conduction losses during $[t_2\text{-}t_3]$ when $P_{in} < P_{LED}$ and during $[t_1\text{-}t_2]$ when $P_{in} > P_{LED}$.

For diode D_2, there is conduction loss during $[t_3\text{-}t_4]$ when $P_{in} > P_{LED}$.

For diode D_3, there is conduction loss during $[t_1\text{-}t_2]$ when $P_{in} < P_{LED}$.

There are also losses from the equivalent lump leakage inductance at the primary side. The leakage inductance, between the primary side main winding and the secondary side main winding, is estimated to be 4% of the primary side main winding inductance, due to relatively poor coupling caused by galvanic isolation. The leakage inductance, between the primary side main winding and the buffering winding, is estimated to be 2% of the primary side main winding inductance as galvanic isolation is not required and good coupling can be achieved. When $P_{in} < P_{LED}$, there is energy built up in the leakage inductor as the primary side switching current grows during $[t_0\text{-}t_1]$. When Pin > PLED, there is energy built up in the leakage inductor as the primary side switching grows during $[t_0\text{-}t_1]$ and $[t_2\text{-}t_3]$, respectively. These energies are dissipated in a snubber circuit as loss.

For the Flyback transformer, there is core and copper loss. A detailed estimation of this loss requires very complex analysis, however, with a reasonably good design, the total loss from the transformer is estimated to be 2% of the power it will handle.

The detailed loss breakdown of the proposed cycle by cycle energy buffering LED driver is shown in TABLE 4 in the appendix as well as presented in bar chart below.

Also, the detailed loss breakdown for the previous active filter LED driver is performed, and the result is shown in TABLE 5 as well as the bar chart in Fig. 15 and Fig. 16 below.

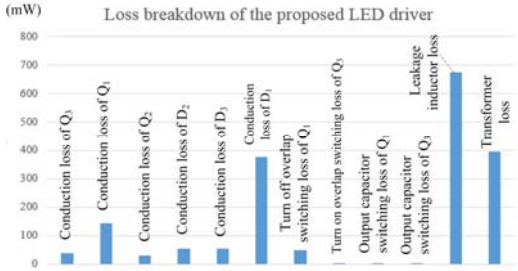


Fig. 15 Loss breakdown of the proposed cycle by cycle energy buffering LED driver

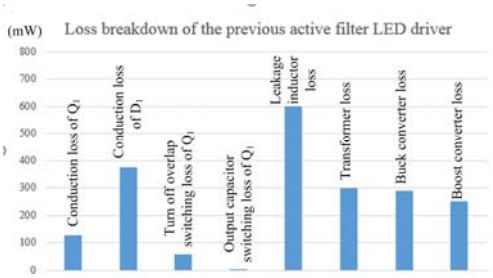


Fig. 2 Loss breakdown of the previous active filtering LED driver

To estimate the power losses from the Buck (release imbalanced energy) and Boost (store imbalanced energy) converters in the previous active filtering LED driver, the following assumption is made.

1. The switching frequency of the Buck and Boost converters is also 25kHz, which benchmark the switching frequency of the proposed LED driver.

2. The inductor used in the Buck and Boost converter is 1.2mH, which is equal to the inductance value of the primary side winding of the Flyback transformer in the proposed LED driver. In this way, the magnetic components used in both designs are at a comparable level and can be assumed to have the same level of power loss.

The total loss generated by the proposed cycle by cycle energy buffering LED driver and the previous active filtering LED driver are calculated/estimated to be 1815mW and 2006mW, respectively for 15W output power. It should note that the majority of losses, in both designs, are from diode conduction loss, leakage inductance loss, transformer loss. Because of low frequency (25kHz) operation, the related switching loss is not significant. In addition to the quantitative analysis on the loss breakdown, the loss difference between these two designs can also be understood from the perspective of energy process steps.

TABLE 3 THE EXPERIMENTAL PROTOTYPE SPECIFICATION AND KEY COMPONENTS

System Specification	
Input voltage	89Vrms – 132Vrms
Maximum output voltage	~60V
Maximum output current	0.25A
Maximum output power	15W
Circuit Parameter	
Transformer	Npri: Nsec: Nbuf = 3:1:3 Lpri=1.2mH, EE16 core
Switching frequency	25KHz
Controller	dsPIC33FJ32GS606
MOSFET Q1	STP5N60M2, 600V, 3.7A
MOSFET Q2, Q3	FQP3N30, 300V, 3.2A
Diode D1, D2, D3	LQA03TC600, 600V, 3A
Output capacitor	CGA9N3X7S2A106K230K B, 100V, 10μF

The proposed LED driver requires one less power conversion step with the imbalanced energy.

Although there are several additional components in the proposed LED driver as compared to a standard single-stage and two-stage LED driver, some of them do not add too much to the overall loss and even help reduce loss. For example, when $P_{in} > P_{LED}$, the imbalanced energy is transferred from the AC input to the storage capacitor. Compared to a standard Flyback converter including a MOSFET, a diode and a Flyback Transformer, there is an additional MOSFET Q_2 involved in the energy transfer in the proposed design. However, there is only conduction loss with Q_2, and the calculated loss is only 30mW, which is equal to roughly 0.2% of the total output power. On the contrary, the imbalanced energy needs to go through a complete Boost power conversion process in the previous active filter LED drivers to complete energy storage. One more power conversion step means more diode conduction loss and inductor loss, which contributes significantly to the total loss. The loss saved with the proposed LED driver, over the previous active filtering LED driver, is around 190mW, which is equivalent to ~1.2% higher efficiency for 15W output power designs.

VI. DESIGN PROCEDURES AND CONSIDERATION

In this section, an example design procedure is provided as a design guideline. Design considerations on switching frequency, transformer inductance, turns ratio and storage capacitors selection are included.

(1) Determine the switching frequency. For example, the switching frequency is designed to be 25kHz for the experimental prototype to minimize switching loss.

(2) Select the turns ratio N_{pri}: N_{sec}: N_{buf}. The turn's ratio determines the voltage stresses of the components. For example, N_{pri}: N_{sec}: N_{buf} is designed to be 3: 1: 3 in the experimental prototype.

(3) Determine the inductance of the primary side winding. L_{pri} should be selected to meet the requirement of DCM operation while, at the same time, minimize idle time in one switching cycle, to achieve lowest possible current stresses. In the experimental prototype, Ipri is designed to be 1.2mH.

4) Select the capacitor C_{sto} and the voltage range for Vsto. With P_{LED} = 15W, V_{sto_avg} is chosen to be 140V and $V_{sto\_pp\_rip}$ to be 60V, the required capacitor C_{sto} is calculated to be 5.7μF with Eq. (27), Two 3.3μF, film capacitors are used in the experimental prototype. On the other side, one should note that the voltage stresses of other components are also related to V_{sto}, as shown in TABLE 1. Therefore, the voltage range for V_{sto} should be properly selected.

5) Select the output capacitors. Because constant output current is delivered to the output in every switching cycle, the output capacitor C_o is only responsible for filtering the switching frequency ripple. Therefore, small capacitance ceramic capacitors can be selected for the design. A 10μF, 100V ceramic capacitor is used in the experimental prototype.

6) Calculate the voltage and current stresses of each power semiconductor components and select parts accordingly.

The above steps provide an example procedure to design the proposed LED driver. Like any other designs, it can always start the design procedure in a different order. For example, one can set the maximum voltage stresses and current stresses of components in the beginning and then design other parameters that around this objective.

VII. SIMULATION AND EXPERIMENTAL RESULT

To verify the operating principle of the proposed LED driver, a 15W simulation model and experimental prototype had been built, simulated, and tested. The circuit parameter is shown in TABLE 3.

Fig. 17 shows the simulated and measured primary side switching current waveforms. A rather flat peak primary side switching current is shown in the simulated result, which completely agrees with the analysis. Due to sensing circuit limitation and delay, the measured primary side peak switching current has a small level of variation in the measured waveform. Also because of noise, mis-triggers occur and results in several spikes and dips scattered in a half line cycle period.

Fig. 18 shows the simulated secondary side switching current and the LED current at line frequency time scale. The peak secondary side switching current is a constant in a half line cycle. Therefore, the averaged secondary side current, which is also equal to the LED current, is a constant in a half line cycle and flicker-free LED driving performance is achieved.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

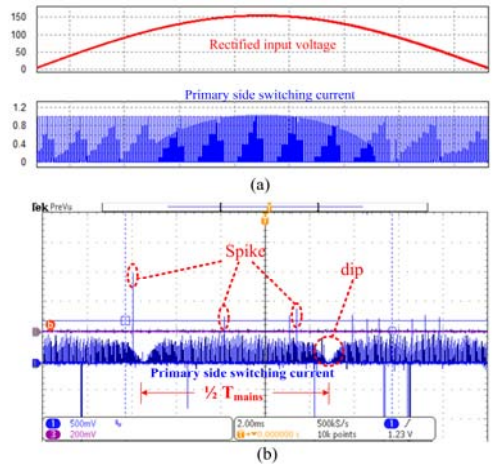


Fig. 17 Primary side switching current, (a) simulated result (PSIM 11.0), (b) measured waveform

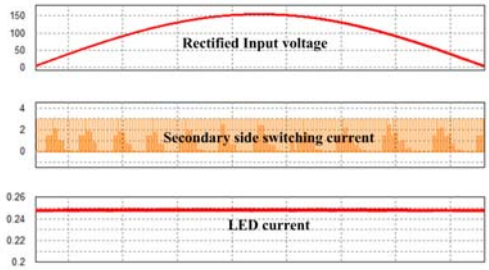


Fig. 18 Simulated key waveforms at line cycle time scale (PSIM 11.0)

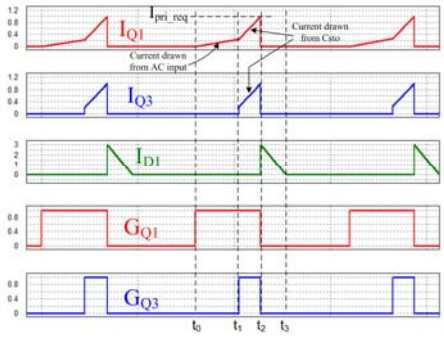


Fig. 19 Simulated key switching waveforms when Pin < PLED (PSIM 11.0)

Fig. 19 shows the key switching waveforms when $P_{in} < P_{LED}$. The MOSFET Q_1 is turned on at the beginning of a switching cycle. During $[t_0\text{-}t_1]$, the switching current in the Q_1 is drawn from AC input. At time t_1, enough current is drawn from AC input required by performing power factor correction. The MOSFET Q_3 is turned on at t_1. During $[t_1\text{-}t_2]$, the switching current in Q_1 is drawn from the storage capacitor C_{sto}. Therefore, energy is transferred from C_{sto} to the transformer and eventually to the LED output after the primary side switching current is terminated. The MOSFET Q_2 is always off during this operating condition. The measured waveforms are shown in Fig. 20 and agrees with simulated waveforms (the switching current is sensed by resistor and presented in voltage form).

Fig. 21 shows the simulated key switching waveforms when $P_{in} > P_{LED}$. The MOSFET Q_1 is turned on during $[t_0\text{-}t_1]$ and the primary side current in Q_1 is drawn from the AC input. At t_1, the primary side switching current hits I_{pri_req}, the level required by LED output. Q_1 is turned off to end the primary side switching current and the magnetic current commutes to the secondary side winding. During $[t_1\text{-}t_2]$, the magnetic current flows in the secondary side winding and delivered to the LED load. The secondary side current drops to zero at t_2 and Q_1 is turned on again. The MOSFET Q_2 is also turned on at t_2. During $[t_2\text{-}t_3]$, more current is drawn from the AC input. At t_3, the total current drawn from AC input reaches the level required by performing power factor correction and Q_1 is turned off again. The magnetic current commutes from the primary side winding to the buffer winding. The extra energy in the transformer is then transferred to the capacitor C_{sto}. The MOSFET Q_3 is always off during this operation condition. Fig. 22 shows the measured waveforms and it highly agrees with simulated result.

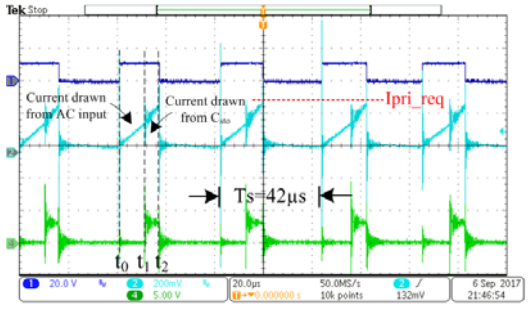


Fig. 3 Key switching waveforms when $P_{in} < P_{LED}$

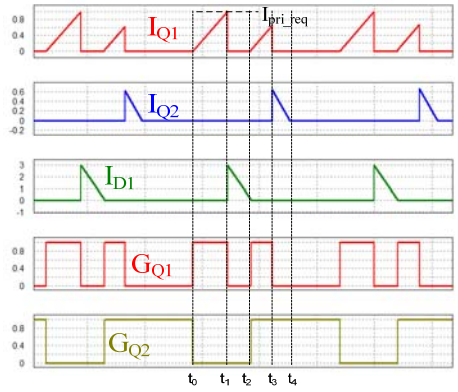


Fig. 4 Simulated key switching waveforms when $P_{in} > P_{LED}$ (PSIM 11.0)

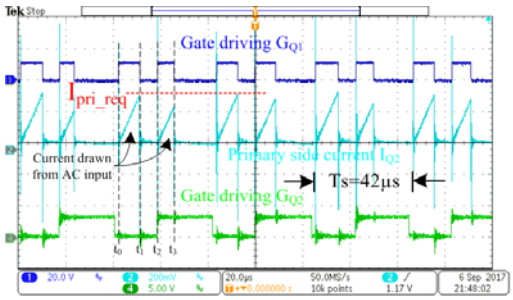


Fig. 22 Key switching waveforms when $P_{in} > P_{LED}$

Fig. 23 shows the key waveforms of line frequency operation, which includes the AC input current, the LED voltage, the LED current and the storage capacitor voltage Vsto. The LED voltage is almost a constant. FFT function is used to measure 120Hz ripple LED current to avoid misreading due to switching noise. The RMS ripple LED current at 120Hz is 10.67mA,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

which corresponds to 15mA peak ripple and is 6% of the average LED current. The voltage on the storage capacitor, V_{sto}, changes from 120V as the minimum to 170V as the maximum in a half line cycle, to buffer the imbalanced energy. It is worth mentioning that, due to sensing circuit limitation, the peak of the switching current I_{pri} varies a bit in a half line cycle, which results in a less than ideal output current waveform. A better output current waveform can be achieved with an improved sensing circuit design; the simulation waveform in Fig. 18 verifies that.

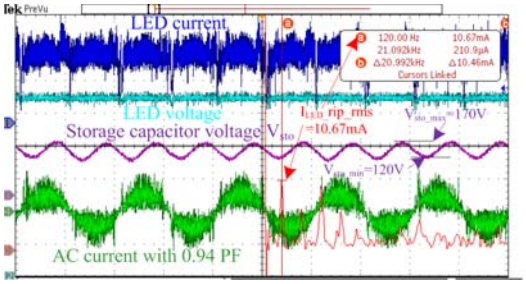


Fig. 23 Key waveforms in double line frequency operation

Fig. 24 compares the efficiency of the proposed LED driver and a comparable conventional single-stage LED driver. At full load, the efficiency of the proposed LED driver is 1.9% lower than the efficiency of a conventional Flyback LED driver, which is a very small price to pay when flicker-free and electrolytic capacitor free operation have been achieved.

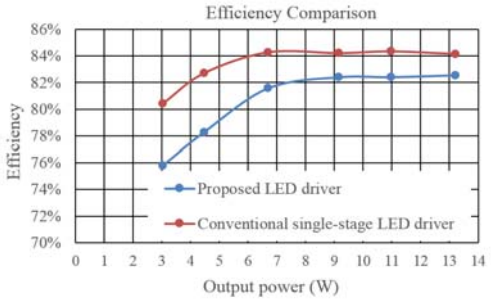


Fig. 24 Efficiency comparison between the proposed LED driver and a conventional LED driver under 110Vrms input

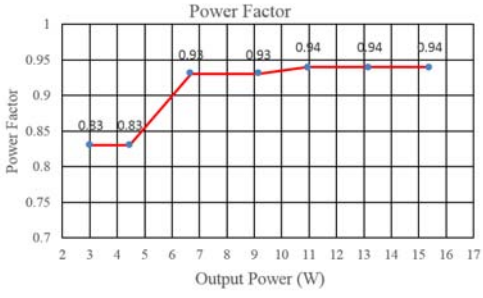


Fig. 25 Power factor performance under 110Vrms input, full load

Fig. 25 shows the power factor of the proposed LED driver. At full load, the experimental prototype achieves 0.94PF, which meets the requirement from EnergyStar.

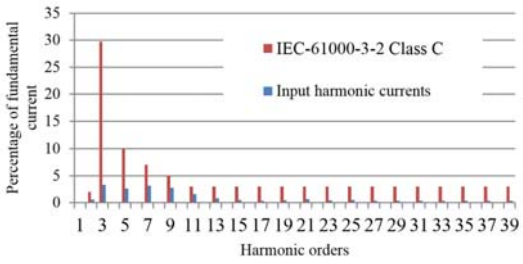


Fig. 26 Input harmonic currents versus IEC-61000-3-2 limit under 110Vrms input, full load

Fig. 26 shows the measurement of input harmonic currents. All harmonic currents of interest are below the limits from IEC-61000-3-2. The photo of the experimental prototype is shown in Fig. 27.

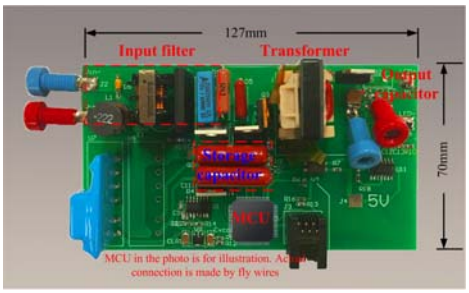


Fig. 5 Photo of the experimental prototype

VIII. Conclusion

Eliminating electrolytic capacitors in LED driver designs is critical to extending the lifetime of LED lighting fixtures. An alternative three-port LED driver - cycle by cycle energy buffering LED driver has been proposed in the paper to achieve electrolytic-less and flicker-free operation. By directly controlling the switching current, the following improvements are made with the proposed LED driver over previous three-port LED drivers. First, the imbalanced energy in a half line cycle experiences one less power conversion step, which reduces conversion loss and improves overall efficiency. Second, the maximum energy that needs to be stored in the transformer in the proposed design is half the amount of conventional and other electrolytic capacitor-less designs, which allows the use of a smaller magnetic core. Third, primary side current regulation can be easily implemented, which can reduce design complexity on controller circuit. A potential integrated primary side controller can be implemented based on this method. A 15W experimental prototype had been built and tested to verify the operating principle. 0.94PF has been achieved and each order of harmonic currents are measured, and they are all below the limit from IEC-61000-3-2. The efficiency of the proposed LED driver is only 1.9 % lower than a conventional single-stage LED driver at full load, which is a low price to pay when achieving flicker-free operation and electrolytic capacitor-less design. Two 3.3μF film capacitor have been used in the prototype to buffer double-line-frequency imbalanced energy. The 120Hz ripple current is measured to be 6% of the average LED current. Overall, the experimental result demonstrates a very good LED driving performance compared

with existing options, and a high degree of agreement with the analysis presented.

APPENDIX

For MOSFET, the following parameters are used in the loss calculation.

C_{Q_oss}: MOSFET parasitic output capacitance 13pF
R_{Q_on}: On resistance of MOSFET 1.4 ohm
T_{Q_f}: MOSFET Turn off fall time 15ns
T_{Q_r}: MOSFET turn on rise time 15ns

For diode, the following parameter is used in the loss calculation

VD_F: Diode forward voltage drop 1.5V

The switching frequency is 25kHz. The loss breakdown of the proposed cycle by cycle energy buffering LED driver and the previous active filtering LED driver are shown in TABLE 4 and TABLE 5.

TABLE 4 LOSS BREAKDOWN OF THE PROPOSED CYCLE BY CYCLE ENERGY BUFFERING LED DRIVER

	Calculation formula	Result (mW)	Parameters
P_{Q1_cond}	$P_{Q1\_cond}=I_{Q1\_rms}^2\times R_{Q\_on}$	134	$\boldsymbol{P_{Q1\_cond}}$: Conduction loss of Q_1 $\boldsymbol{I_{Q1\_rms}}$: RMS current in Q_1 0.32A
P_{Q1_cap1}	$P_{Q1\_cap1}=\frac{1}{4}C_{Q1\_oss}\times V_{Q1\_ds\_on1}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_on1}=(V_{in\_rec})_{avg}$ when $P_{in}<P_{LED}$	~0	$\boldsymbol{P_{Q1\_cap1}}$: Output capacitor switching loss of Q_1 when $P_{in}<P_{LED}$ $\boldsymbol{V_{Q1\_ds\_on1}}$: Drain to source voltage of Q_1 before turn on when $P_{in}<P_{LED}$ ~60V (average)
P_{Q1_off1}	$P_{Q1\_off1}=\frac{1}{2}\times V_{Q_1\_ds\_off1}\times I_{Q1\_pk1}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_off1}=V_{sto\_avg}+\frac{N_{pri}}{N_{sec}}\times V_{LED}$	20.6	$\boldsymbol{P_{Q1\_off1}}$: Q_1 turn off switching loss of when $P_{in}<P_{LED}$ $\boldsymbol{I_{Q1\_pk1}}$: Peak switching current in Q_1 when $P_{in}<P_{LED}$ 1A $\boldsymbol{V_{Q1\_ds\_off1}}$: Drain to source voltage of Q_1 after turning off when $P_{in}<P_{LED}$ ~320V
P_{Q1_cap2}	$P_{Q1\_cap1}=\frac{1}{4}C_{Q1\_oss}V_{Q1\_ds\_on2}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_on1}=(V_{in\_rec})_{avg}$ when $P_{in}>P_{LED}$	~0	$\boldsymbol{V_{Q1\_ds\_on1}}$: Drain to source voltage of Q_1 before turn on when $P_{in}>P_{LED}$ ~130V
P_{Q1_off2}	$P_{Q1\_off2}=\frac{1}{2}\times V_{Q_1\_ds2}\times I_{Q_1\_pk2}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_off2}=V_{in\_rec\_avg}+\frac{N_{pri}}{N_{sec}}\times V_{LED}$	6.1	$\boldsymbol{P_{Q1\_off2}}$: 1st turn off overlap switching loss of Q_1 when $P_{in}>P_{LED}$ $\boldsymbol{V_{Q1\_ds\_off2}}$: Drain to source voltage of Q_1 after turn off when $P_{in}>P_{LED}$ ~280V $\boldsymbol{I_{Q1\_pk2}}$: 1st peak switching current in Q_1 when $P_{in}>P_{LED}$ 1A
P_{Q1_off3}	$P_{Q1\_off3}=\frac{1}{2}\times V_{Q_1\_ds\_off2}\times I_{Q_1\_pk3}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	4.3	$\boldsymbol{P_{Q1\_off3}}$: 2nd turn off overlap switching loss of Q_1 when $P_{in}>P_{LED}$ $\boldsymbol{I_{Q1\_pk3}}$: 2nd peak switching current in Q_1 when $P_{in}>P_{LED}$ 0.5A (the peak switching current changes from 0A to 1A)
P_{D1_cond}	$P_{D_1\_cond}=I_{D_1\_avg}\times V_{D\_F}$	375	$\boldsymbol{P_{D1\_cond}}$: D_1 conduction loss $\boldsymbol{I_{D1\_avg}}$: Average current in D_1 0.25A
P_{Q2_cond}	$P_{Q_2\_cond}=R_{Q\_on}\times I_{Q_2\_rms}^2$	30	$\boldsymbol{P_{Q2\_cond}}$: Conduction loss of D_2 $\boldsymbol{I_{Q2\_rms}}$: RMS current in Q_2 0.15A
P_{D2_cond}	$P_{D_2\_cond}=I_{D_2\_avg}\times V_{D\_F}$	55	$\boldsymbol{P_{D2\_cond}}$: Q_2 conduction loss $\boldsymbol{I_{D2\_avg}}$: RMS current in Q_2 0.04A
P_{Q3_on}	$P_{Q_3\_on}=\frac{1}{2}\times V_{Q_3\_ds\_on}\times I_{Q_3\_pk}\times t_{Q\_r}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_3\_ds\_on}=(V_{sto}-V_{in\_rec})_{avg}$	8.8	$\boldsymbol{P_{Q3\_on}}$: Turn on overlap switching loss with Q_3 $\boldsymbol{V_{Q3\_ds\_on}}$: Drain to source voltage of Q_3 before turn on ~70V $\boldsymbol{I_{Q3\_pk}}$: Peak switching current in Q_3 0.17A
P_{Q3_cond}	$P_{Q_3\_cond}=R_{Q\_on}\times I_{Q_3\_rms}^2$	39	$\boldsymbol{P_{D3\_cond}}$: Conduction loss of D_3 $\boldsymbol{I_{Q3\_rms}}$: RMS current in Q_3 0.16A
P_{D3_cond}	$P_{D_3\_cond}=I_{D_3\_avg}\times V_{D\_F}$	52	$\boldsymbol{P_{D3\_cond}}$: Conduction loss of D_3 $\boldsymbol{I_{D3\_avg}}$: RMS current in Q_3 0.04A
P_{Q3_cap}	$P_{Q1\_cap}=\frac{1}{4}C_{Q\_oss}\times V_{Q_3\_ds\_on}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	0.3	$\boldsymbol{P_{Q3\_cap}}$: Q_3 output capacitor switching loss
P_{lk1}	$P_{lk1}=\frac{1}{2}I_{Q_1\_pk2}^2\times L_{lk1\_est}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	300	$\boldsymbol{P_{lk1}}$: Leakage inductor loss when $P_{in}<P_{LED}$ $\boldsymbol{L_{lk1\_est}}$: Estimated leakage inductance between the primary side main winding and the second side main winding 4% x L_{pri} = 48μF
P_{lk2}	$P_{lk2}=\frac{1}{2}I_{Q_1\_pk2}^2\times L_{lk1}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	300	$\boldsymbol{P_{lk2}}$: Leakage inductor loss generated by the first primary pulse current when $P_{in}<P_{LED}$
P_{lk3}	$P_{lk3}=\frac{1}{2}I_{Q_1\_pk3}^2\times L_{lk2}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	75	$\boldsymbol{P_{lk3}}$: Leakage inductor loss generated by the second primary pulse current when $P_{in}<P_{LED}$ $\boldsymbol{L_{lk2}}$: Leakage inductance between the primary side main winding and the buffer winding 24μF
P_{tran_est}	$P_{tran}=P_{LED}\times(1+\frac{1}{\pi})\times 2\%$	395	$\boldsymbol{P_{tran\_est}}$: Estimated sum of core and copper losses of the Flyback transformer 2% P_{LED} = 0.3W
Total		1815	

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2876337, IEEE Transactions on Power Electronics

TABLE 5 LOSS BREAKDOWN OF PREVIOUS ACTIVE FILTERING LED DRIVER

	Calculation formula	Result (mW)	Parameters
P_{Q1_cond}	$P_{Q1\_cond}=I_{Q\_rms}^2\times R_{Q\_on}$	134	$\boldsymbol{P_{Q1\_cond}}$: Conduction loss of Q_1 $\boldsymbol{I_{Q1\_rms}}$: RMS current in Q_1 0.3A
P_{Q1_cap}	$P_{Q1\_cap}=\frac{1}{4}C_{Q\_oss}V_{Q1\_ds\_on}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_on}=(V_{in\_rec})_{avg}$	1	$\boldsymbol{P_{Q1\_cap1}}$: Output capacitor switching loss of Q_1 $\boldsymbol{V_{Q1\_ds\_on}}$: Drain to source voltage of Q_1 before turn on ~100V
P_{Q1_off}	$P_{Q1\_off}=\frac{1}{2}\times V_{Q\_ds\_off}\times I_{Q1\_pk}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_off}=(V_{in\_rec})_{avg}+\frac{N_{pri}}{N_{sec}}\times V_{LED}$	13	$\boldsymbol{P_{Q1\_off}}$: Q_1 turn off switching loss of $\boldsymbol{I_{Q1\_pk}}$: Peak switching current in Q_1 1A (rms) $\boldsymbol{V_{Q1\_ds\_off}}$: Drain to source voltage of Q_1 after turn off ~280V
P_{D1_cond}	$P_{D_1\_cond}=I_{D_1\_avg}\times V_{D_1\_F}$	375	$\boldsymbol{P_{D1\_cond}}$: D_1 conduction loss $\boldsymbol{I_{D1\_avg}}$: Average current in D_1 0.25A
P_{lk}	$P_{Q1\_cond}=\frac{1}{2}I_{Q1\_pk}^2\times L_{lk}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	600	$\boldsymbol{P_{lk}}$: Leakage inductor loss $\boldsymbol{L_{lk\_est}}$: Estimated leakage inductance between the primary side main winding and the second side main winding 4% x L_{pri} = 48μF
P_{tran}	$P_{tran}=P_{LED}\times 2\%$	300	$\boldsymbol{P_{tran\_est}}$: Estimated sum of core and copper losses of the Flyback transformer 2% P_{LED} = 0.3W
P_{QBuck_cond}	$P_{Q_{Buck}\_cond}=I_{Q_{Buck}\_rms}^2\times R_{Q\_on}$	49	$\boldsymbol{P_{QBuck\_cond}}$: MOSFET conduction loss in the Buck converter $\boldsymbol{I_{QBuck\_rms}}$: RMS current in the MOSFET of the Buck converter 0.187A
P_{QBuck_off}	$P_{Q1\_off}=\frac{1}{2}\times V_{QBuck\_ds\_off}\times I_{QBuck\_pk}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{QBuck\_ds\_off}=(V_{sto})_{avg}$	7.7	$\boldsymbol{P_{QBuck\_off}}$: MOSFET switching loss in the Buck converter $\boldsymbol{I_{QBuck\_pk}}$: Peak current in the MOSFET 0.59A $\boldsymbol{V_{QBuck\_ds\_off}}$: Drain to source voltage across the MOSFET before turn off ~140V
P_{QBuck_cap}	$P_{Q1\_cap}=\frac{1}{2}\times C_{Q\_oss}V_{Qbuck\_ds\_on}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Qbuck\_ds\_on}=(V_{sto})_{avg}-V_{LED}$	1.6	$\boldsymbol{P_{QBuck\_cap}}$: MOSFET output capacitor switching loss in the Buck converter $\boldsymbol{V_{QBuck\_ds\_on}}$: Drain to source voltage across the MOSFET before turn on ~80V
P_{Dbuck_cond}	$P_{DBuck\_cond}=I_{D_{Buck}\_avg}\times V_{D\_F}$	138	$\boldsymbol{P_{DBuck\_cond}}$: Diode conduction loss in the Buck converter $\boldsymbol{I_{DBuck\_avg}}$: Average current in the diode 0.09A
$P_{inductor\_Buck}$	$P_{inductor\_Buck}=P_{Buck}\times 2\%$	95.5	$\boldsymbol{P_{Buck}}$: Buck converter output power $\boldsymbol{P_{inductor\_Buck}}$: Estimated loss of inductor in the Buck converter 2% x P_{Buck}
P_{Qboost_cond}	$P_{Q_{Boost}\_cond}=I_{Q_{Boost}\_rms}^2\times R_{Q\_on}$	51.6	$\boldsymbol{P_{QBoost\_cond}}$: MOSFET conduction loss in the Boost converter $\boldsymbol{I_{QBoost\_rms}}$: RMS current in the MOSFET of the Boost converter 0.192A
P_{Qboost_off}	$P_{QBoost\_off}=\frac{1}{2}\times V_{QBoost\_ds\_off}\times I_{QBoost\_pk}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{QBoost\_ds\_off}=V_{LED}$	3.3	$\boldsymbol{P_{QBoost\_off}}$: MOSFET switching loss in the Boost converter $\boldsymbol{I_{QBoost\_pk}}$: Peak current in the MOSFET 0.59A $\boldsymbol{V_{QBoost\_ds\_off}}$: Drain to source voltage across the MOSFET after turn off 60V
P_{Qboost_cap}	$P_{Q1\_cap}=\frac{1}{2}C_{QBoost\_oss}\times V_{QBoost\_ds\_on}^2\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{QBoost\_ds\_on}=(V_{sto})_{avg}$	0.3	$\boldsymbol{P_{QBoost\_cap}}$: MOSFET output capacitor switching loss in the Boost converter $\boldsymbol{V_{QBuck\_ds\_on}}$: Drain to source voltage across the MOSFET before turn on ~140V
P_{DBoost_cond}	$P_{DBoost\_cond}=I_{D_{Boost}\_avg}\times V_{D\_F}$	102	$\boldsymbol{P_{QBoost\_cond}}$: MOSFET output capacitor switching loss in the Boost converter $\boldsymbol{I_{DBoost\_avg}}$: Average current in the diode 0.068A
$P_{inductor\_Boost}$	$P_{Inductor\_Boost}=P_{Boost}\times 2\%$	95.5	$\boldsymbol{P_{Boost}}$: Boost converter output power $\boldsymbol{P_{inductor\_Boost}}$: Estimated loss of inductor in the Boost converter 2% x P_{Boost}
Total		2006	

REFERENCES

[1] ENERGY STAR Program Requirements for Solid State Lighting Luminaires, Version 1.1, December 19, 2008.

[2] IEC, IEC61000–3–2 - Electromagnetic Compatibility (EMC), in Part 3: Limits—Section 2: Limits for Harmonic Current Emissions (equipment input current < 16 A, per phase), 1991

[3] B. Lehman, A.J. Wilkins, "Designing to Mitigate Effects of Flicker in LED Lighting: Reducing risks to health and safety," in IEEE Power Electronics Magazine, Vol 1, No 3, September 2014. pp. 18-26.

[4] B. Lehman, A. Wilkins, S. Berman, M. Poplawski and N. J.Miller, "Proposing measures of flicker in the low frequencies for lighting applications," in Energy Conversion Congress and Exposition, Phoenix, AZ, Sept 2011.

[5] "IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers, IEEE Standard 1789-2015, Jun. 5, 2015.

[6] X.B. Ruan, B.B. Wang, K. Yao and S. Wang, "Optimum Injected Current Harmonics to Minimize Peak-to-Average Ratio of LED Current for Electrolytic Capacitor Less AC–DC Drivers" in IEEE Transactions on Power Electronics, Vol. 26, No. 7, pp.1820-1825, July 2011.

[7] G. G. Pereira, M. A. Dalla Costa, J. M. Alonso, M. F. De Melo and C. H. Barriquello, "LED Driver Based on Input Current Shaper Without Electrolytic Capacitor," in IEEE Transactions on Industrial Electronics, vol. 64, no. 6, pp. 4520-4529, June 2017.

[8] D. G. Lamar, J. Sebastian, M. Arias and A. Fernandez, "On the Limit of the Output Capacitor Reduction in Power-Factor Correctors by Distorting the Line Input Current," in IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1168-1176, March 2012.

[9] F.H. Zhang, J.J.Ni and Y.J.Yu, "High Power Factor AC–DC LED Driver With Film Capacitors," in IEEE Transactions on Power Electronics, Vol. 28, No. 10, pp. 4831-4840, October 2013.

[10] C.A. Cheng, C.H. Chang, T.Y. Chung and F.L. Yang, "Design and Implementation of a Single-Stage Driver for Supplying an LED Street-Lighting Module With Power Factor Corrections," in IEEE Transactions on Power Electronics, Vol. 30, No. 2, pp. 956-966, February 2015.

[11] J. C. W. Lam and P. K. Jain, "Isolated AC/DC Offline High Power Factor Single-Switch LED Drivers Without Electrolytic Capacitors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 3, No. 3, pp. 679-690, September 2015.

[12] J. C. W. Lam and P. K. Jain, "A High Power Factor, Electrolytic Capacitor-Less AC-Input LED Driver Topology with High Frequency Pulsating Output Current," in IEEE Transactions on Power Electronics, Vol. 30, Vo. 2, pp. 943-955, February 2015.

[13] H. Ma, J. S. (. Lai, C. Zheng and P. Sun, "A High-Efficiency Quasi-Single-Stage Bridgeless Electrolytic Capacitor-Free High-Power AC–DC Driver for Supplying Multiple LED Strings in Parallel," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5825-5836, Aug. 2016.

[14] P. Fang, Y. F. Liu and P. C. Sen, "A Flicker-Free Single-Stage Offline LED Driver With High Power Factor," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 654-665, Sept. 2015.

[15] P. Fang, Y. j. Qiu, H. Wang and Y. F. Liu, "A Single-Stage Primary-Side-Controlled Off-line Flyback LED Driver With Ripple Cancellation," in IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4700-4715, June 2017.

[16] P. Fang and Y. F. Liu, "Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation with True Single Stage Power Factor Correction," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3892-3907, May 2017.

[17] Y. Qiu, L. Wang, H. Wang, Y. F. Liu and P. C. Sen, "Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-Capacitor-Less High-Power LED Driver," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 698-713, Sept. 2015.

[18] D.Camponogara, G.F.Ferreira, A. Campos, M.A. Dalla Costa and J. Garcia, "Offline LED Driver for Street Lighting With an Optimized Cascade Structure," in IEEE Transactions on Industry Applications, Vol.49, No 6, pp.2437-2443, December 2013.

[19] E. Rifa, "Electrolytic capacitors application guide," Appl. Note, Evox Rifa AB, Gr¨anna, Sweden, 2001.

[20] Q.C. Hu and R. Zane, "Minimizing Required Energy Storage in Off-Line LED Drivers Based on Series-Input Converter Modules," in IEEE Transactions on Power Electronics, Vol. 26, No. 10, pp.2887-2895, October 2011.

[21] S. Wang, X.B. Ruan, K. Yao, S.C. Tan, Y. Yang and Z.H. Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver" in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp.4540-4548, November 2012.

[22] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou and E. C. Tatakis, "Investigation of Parallel Active Filters' Limitations for Power Decoupling on Single-Stage/Single-Phase Microinverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1096-1106, Sept. 2016.

[23] P. T. Krein, R. S. Balog and M. Mirjafari, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port," in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp. 4690-4698, November. 2012.

[24] M. Hadi Zare, M. Mohamadian and R. Beiranvand, "A Single-Phase Grid-Connected Photovoltaic Inverter Based on a Three-Switch Three-Port Flyback With Series Power Decoupling Circuit," in IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 2062-2071, March 2017.

[25] C. Y. Liao, W. S. Lin, Y. M. Chen and C. Y. Chou, "A PV Micro-inverter With PV Current Decoupling Strategy," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6544-6557, Aug. 2017.

[26] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen and I. Batarseh, "A Single-Stage Microinverter Without Using Eletrolytic Capacitors," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2677-2687, June 2013.

[27] W. Chen and S.Y.R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver with High Input Power Factor and Constant Output Current," in IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1598-1607, March 2012.

[28] Y.C. Li and C.L. Chen, "A Novel Primary-Side Regulation Scheme for Single-Stage High-Power-Factor AC–DC LED Driving Circuit," in IEEE Transactions on Industrial Electronics, Vol. 60, No. 11, pp.4978-4986, November 2013.

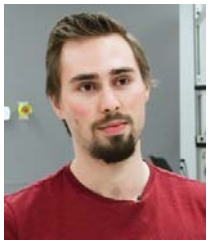
[29] X.G. Xie, J. Wang, C. Zhao, Q. Lu and S.R. Liu, "A Novel Output Current Estimation and Regulation Circuit for Primary Side Controlled High Power Factor Single-Stage Flyback LED Driver," in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp. 4602-4612, November 2012.

[30] Power Integration. "14 W TRIAC Dimmable, High Efficiency >85%, Non-Isolated Buck Converter, Power Factor Corrected (>0.95) LED Driver Using LYTSwitchTM LYT4313E" [online]. 2013

[31] Texas Instruments. "AN-2150 LM3450A Evaluation Board" [online]. 2013

Peng Fang (S'11-M'16) received his M.Sc. degree from the Department of Electrical and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, in 2007. He obtained his Ph.D. degree in the Department of Electrical and Computer Engineering from Queen's University, Canada in 2016. From 2007 to 2011, he worked at ASM Pacific Technology, Hong Kong, as a power electronics engineer, where he led the designs of power converters and power amplifiers. After he graduated from Queen's University, he continued his research in the same research lab as post-doctoral research fellow, from 2016 to 2018. Since 2018, he has been an Assistant Professor with the Department of Electrical Engineering, University of Minnesota, Duluth. He has two granted U.S patents and another four U.S patents in pending. His research interests include LED driver, EV charger, wireless power transfer, smart grid and ultra-high frequency power converter design.

Bo Sheng (S'17) received his M.S degree from the Department of Electrical and Computer Engineering, Shanghai University of Electric Power, in 2016. He is working toward his Ph.D. degree at Queen's university. His areas of interest include high efficiency resonant DC/DC converters.



Samuel Webb (S'17) received his B.S degree from the Department of Electrical and Computer Engineering, Queen' university, Canada, in 2016. He is working toward his Ph.D. degree in the same university. His areas of interest include extremely high efficiency DC/DC converters for point-of-load applications.

ZHANG Yan received the Ph.D. degree in the major of Electrical Engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2014. Then he has been working as a teaching faculty, and he is currently an associate professor in the school of Electrical Engineering in XJTU. From early 2016 to 2017, he was a Postdoctoral Research Fellow in the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada. His research interests include topology, model and control of power electronic systems, high efficiency resonant dc-dc converters, and power-electronics applications in renewable energy and distributed generation. Dr. ZHANG has presided over research projects includes National Natural Science Foundation, China Postdoctoral Science and Province Foundation, Power Electronics Science and Education Development Program of Delta Environmental & Educational Foundation, State key lab Foundation. He has published more than 30 papers technical papers in peer-reviewed journals and conference proceedings and holds 4 China issued invention patents.

Yan-Fei Liu (M'94–SM'97-F'13) received his Bachelor and Master's degree from the Department of Electrical Engineering from Zhejiang University, China, in 1984 and 1987 and PhD degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, in Ottawa, Canada from 1994 to 1999. Since 1999, he has been with Queen's University, where he is currently a Professor with the Department of Electrical and Computer Engineering. His current research interests include digital control technologies for high efficiency, fast dynamic response dc–dc switching converter and ac–dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He has authored over 230 technical papers in the IEEE Transactions and conferences and holds 25 U.S. patents. He is also a Principal Contributor for two IEEE standards. He is a Fellow of Canadian Academy of Engineering and received Modeling and Control Achievement Awards from IEEE Power Electronics Society. He received Premier's Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997.