Optimal Design of Current Source Gate Driver for a Buck Voltage Regulator Based on a New Analytical Loss Model

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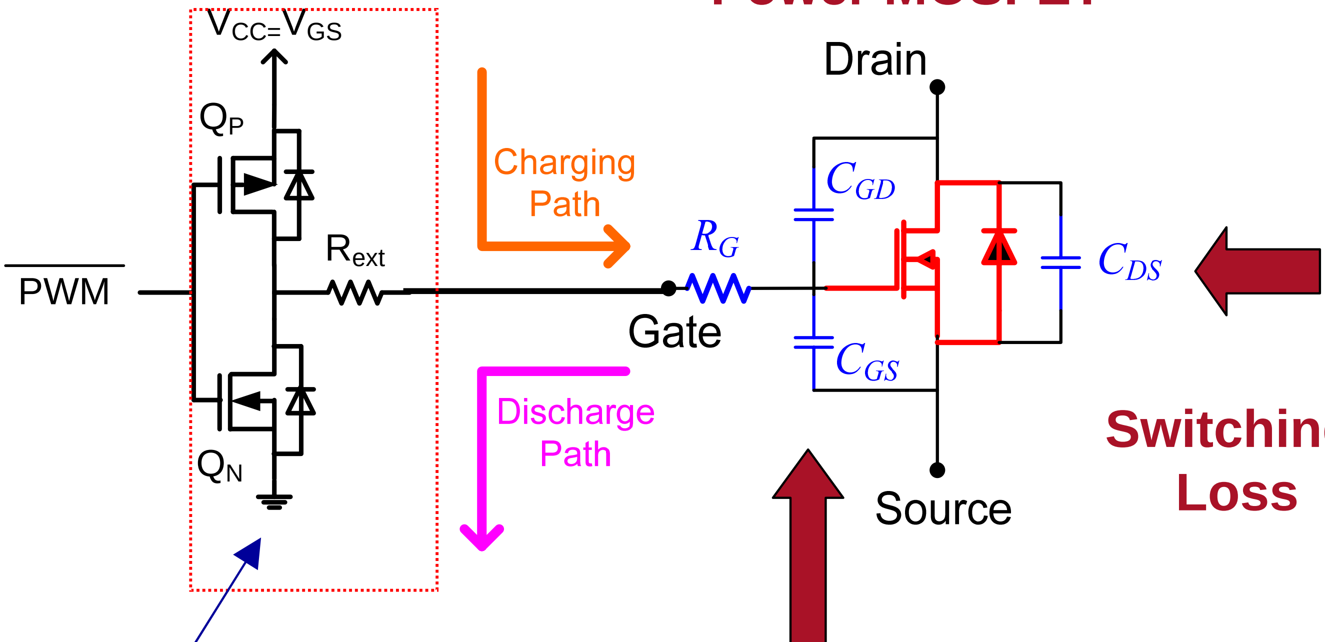
Outline

- Introduction
- Proposed MOSFET Loss Model with Current-Source Driver
- Optimal Design of Current-Source Driver for a Buck VR
- Experimental Results
- Conclusion

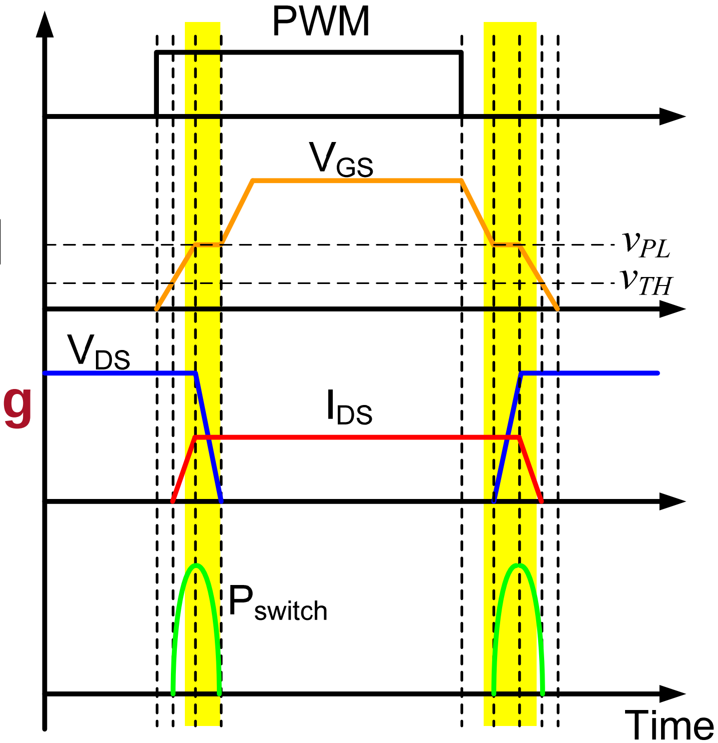
Voltage-Source MOSFET Driver

MOSFET Driver

Power MOSFET



Hard Switching Waveforms



Switching Loss

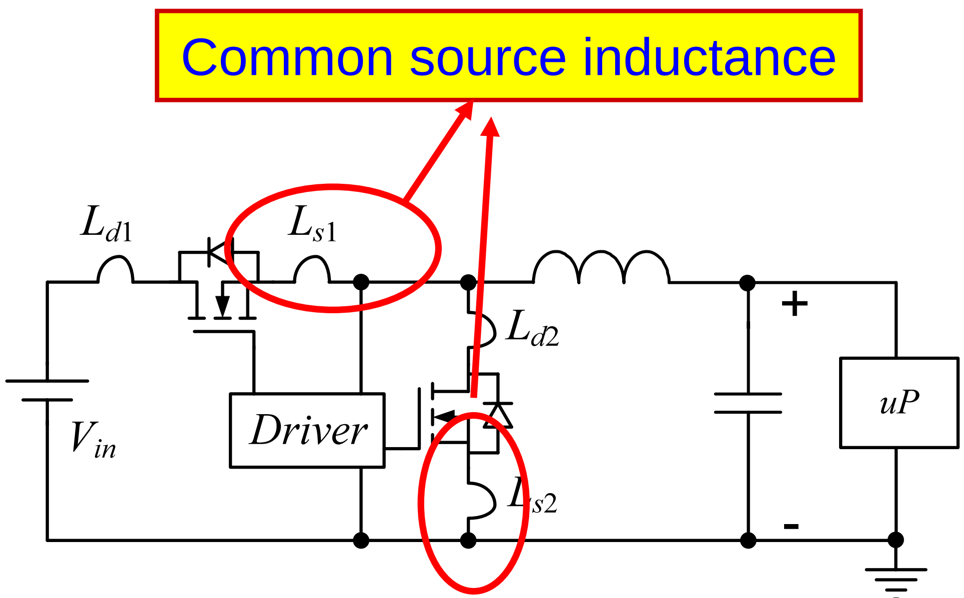
MOSFET, or BJT transistors

Gate Loss

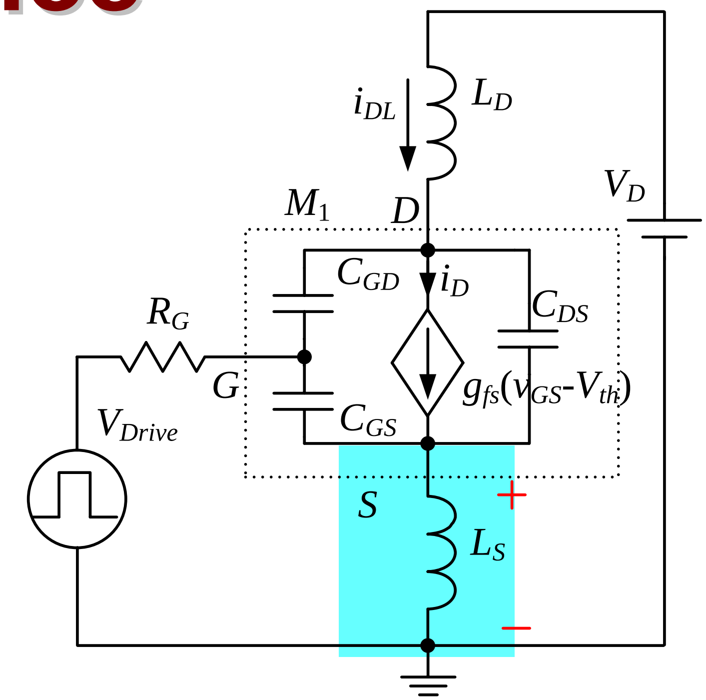
$$P_{gate} = Q_g V_{GS} f_S$$

$$P_{switching} \approx \frac{V_{DS} \cdot I_D}{2} \cdot (t_{rise} + t_{fall}) \cdot f_s$$

Switching Loss: Common Source Inductance



Buck VR with parasitic inductors



Equivalent circuit of MOSFET switching transition

* Y. Ren, M. Xu, J. Zhou and F.C. Lee, "Analytical loss model of power MOSFET," IEEE Trans. Power Electron., vol. 21, No. 2, pp. 310 - 319, Mar. 2004

* Y. Xiao, H. Shah, T.P. Chow and R.J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in Proc. IEEE APEC, 2004, vol. 1, pp. 516-521

Gate Drive Techniques

Limitations of voltage source driver:

- No gate charge energy recovered
- High switching loss due to common source inductance

Resonant gate driver techniques:

- ✓ Many good drive topologies proposed since 1990s, to emphasize gate energy recovery
- ✓ Gate charge current starts from zero

Current-source gate driver

- ✓ Constant gate charge current
- ✓ Gate energy recovery
- ✓ **Significant switching loss savings**

Research Motivation

- Mathematical analysis of effect of the parasitic inductance on the current-source driver
- Accurate prediction of the switching loss saving by a current-source driver considering the parasitic inductance
- Optimal design of a current-source driver to achieve maximum efficiency improvement

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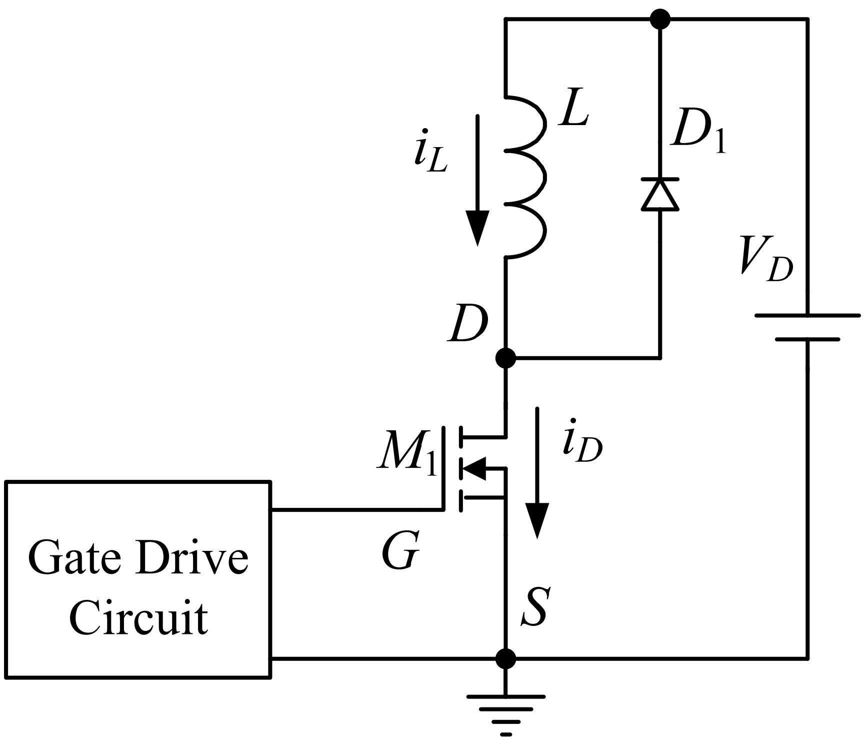
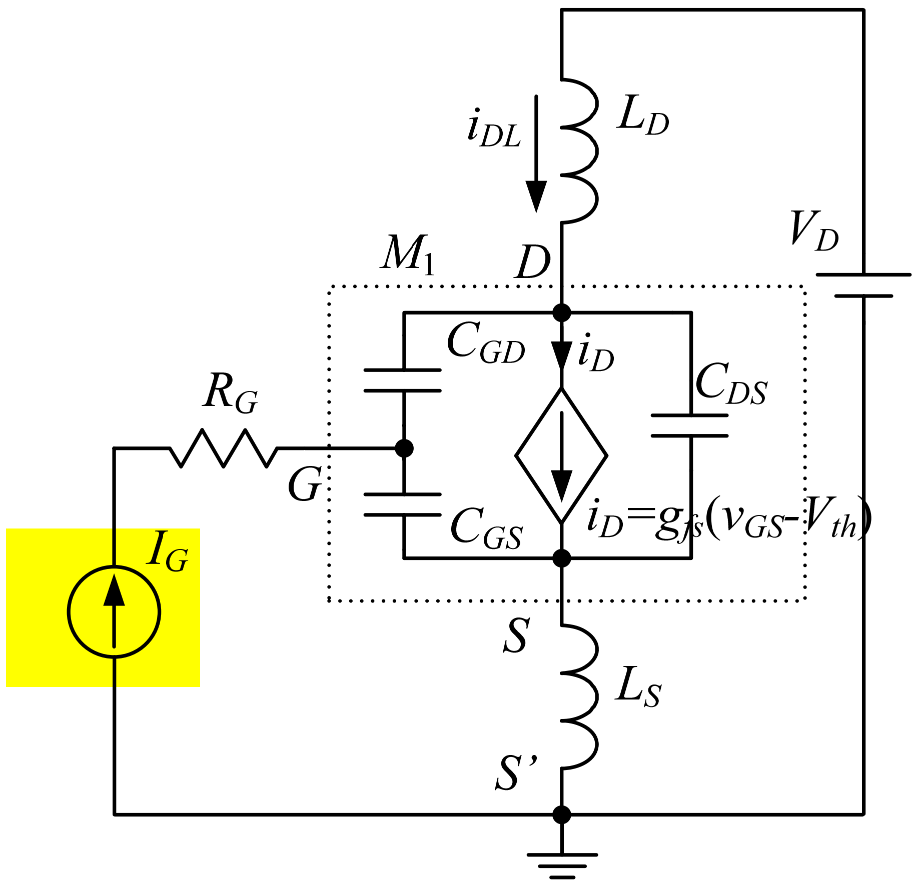
Circuits and Basic Assumption



Circuit with a clamped inductive load



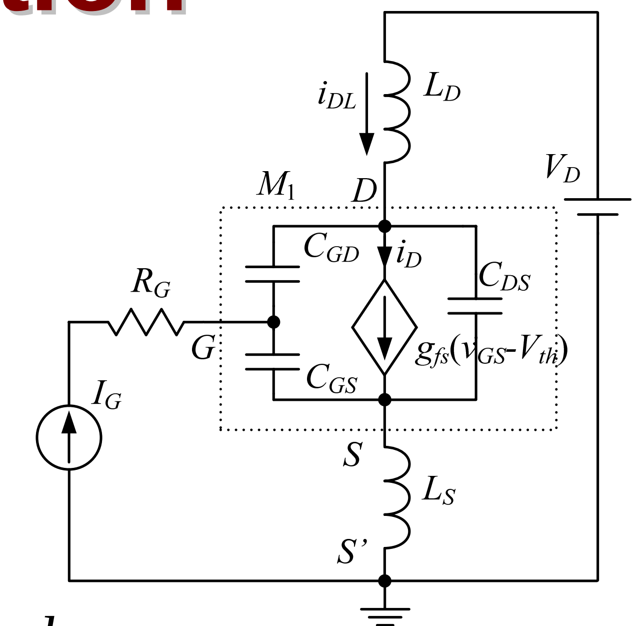
Equivalent circuit of MOSFET switching transition

Analytical Modeling of Main Switching Transition

$$I_G = C_{GD}\frac{dv_{GD}}{dt} + C_{GS}\frac{dv_{GS}}{dt} \qquad v_{GD} = v_{GS} - v_{DS}$$

$$I_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt}$$

$$\frac{dv_{DS}}{dt} = \frac{C_{GS} + C_{GD}}{C_{GD}} \cdot \frac{dv_{GS}}{dt} - \frac{I_G}{C_{GD}}$$



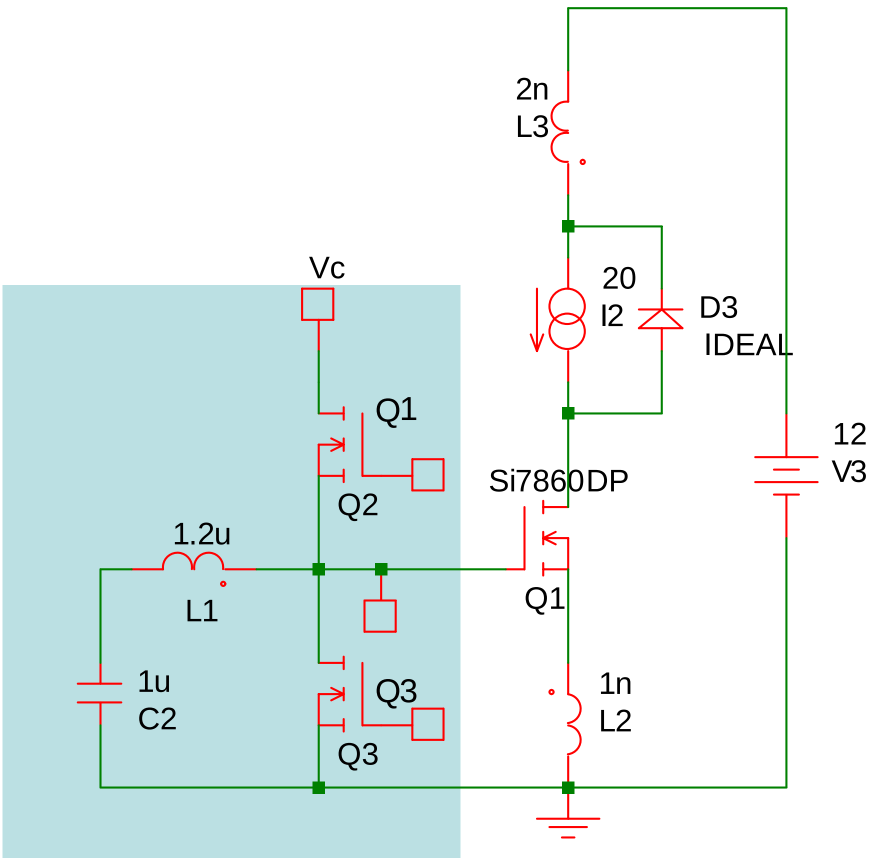
Equivalent circuit of MOSFET switching transition

$$v_{DS} = V_D - (L_D + L_s)(C_{GS}\frac{d^2 v_{GS}}{dt^2} + C_{DS}\frac{d^2 v_{DS}}{dt^2} + g_{fs}\frac{dv_{GS}}{dt})$$

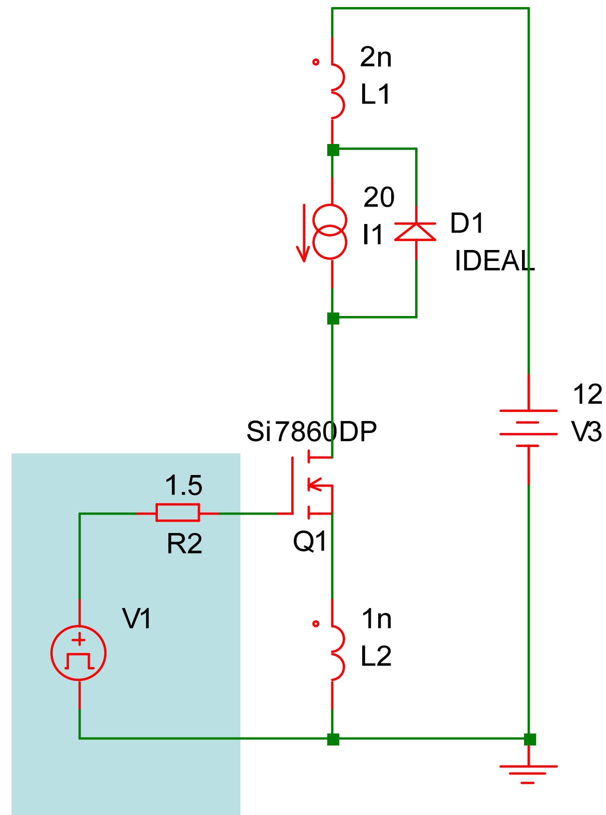
$$\frac{dv_{DS}}{dt} = -(L_D + L_s)(g_{fs}\frac{d^2 v_{GS}}{dt^2} + \frac{C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS}}{C_{GD}} \cdot \frac{d^3 v_{GS}}{dt^3})$$

$$\boxed{A\frac{d^3 v_{GS}(t)}{dt^3} + B\frac{d^2 v_{GS}(t)}{dt^2} + C\frac{dv_{GS}(t)}{dt} = I_G}$$

Simulation Comparison: Current-Source Drive vs. Voltage Drive

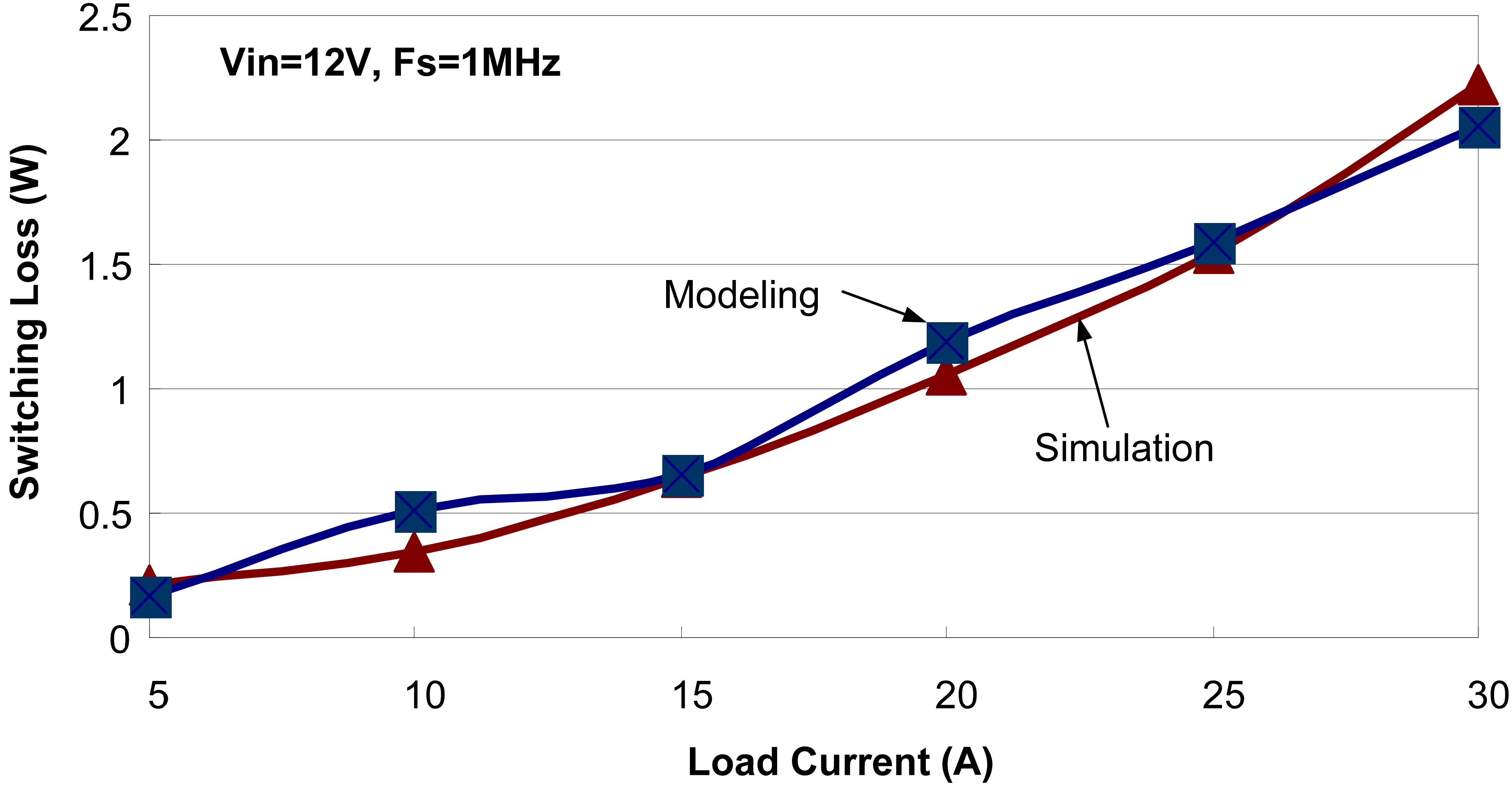


Current-Source Drive



Voltage-Source Drive

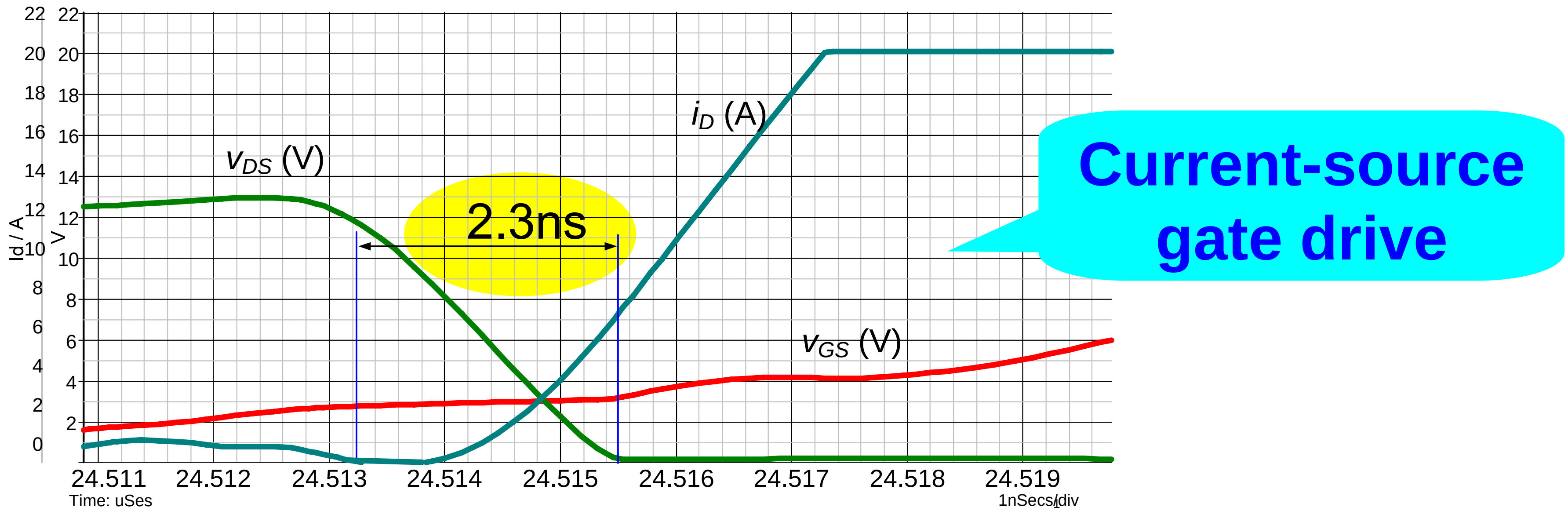
Modeling and Simulation Results

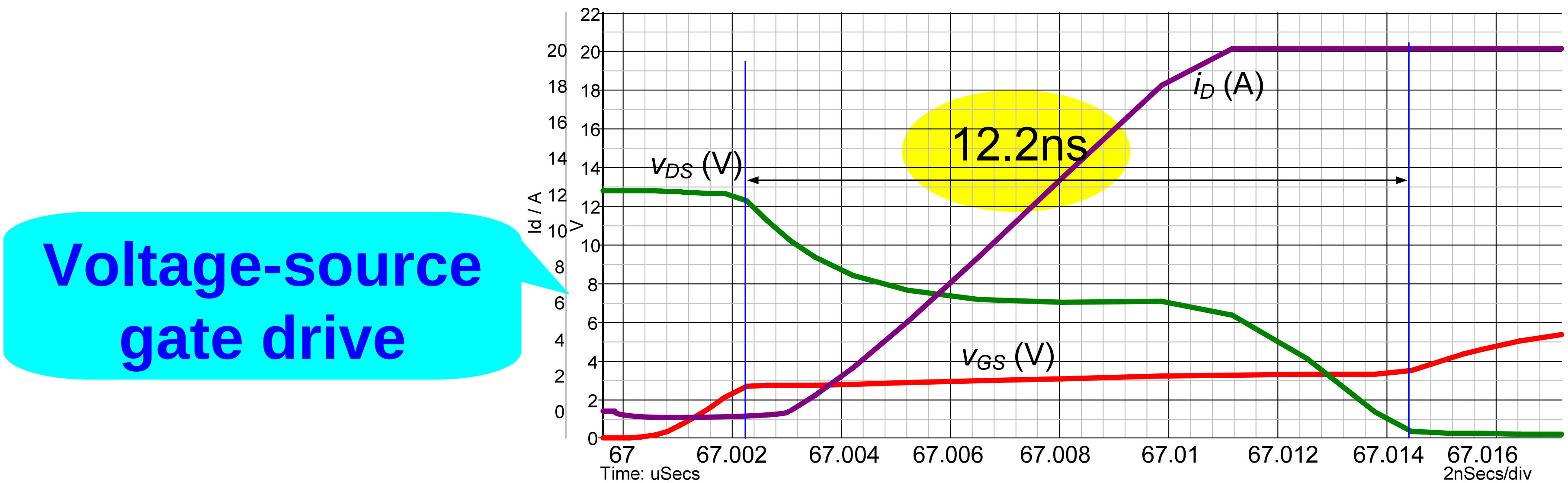


V_D=12V, I_L=20A, fs=1MHz, Ls=1nH, L_D=2nH

Si7860AD SPICE model by Vishay

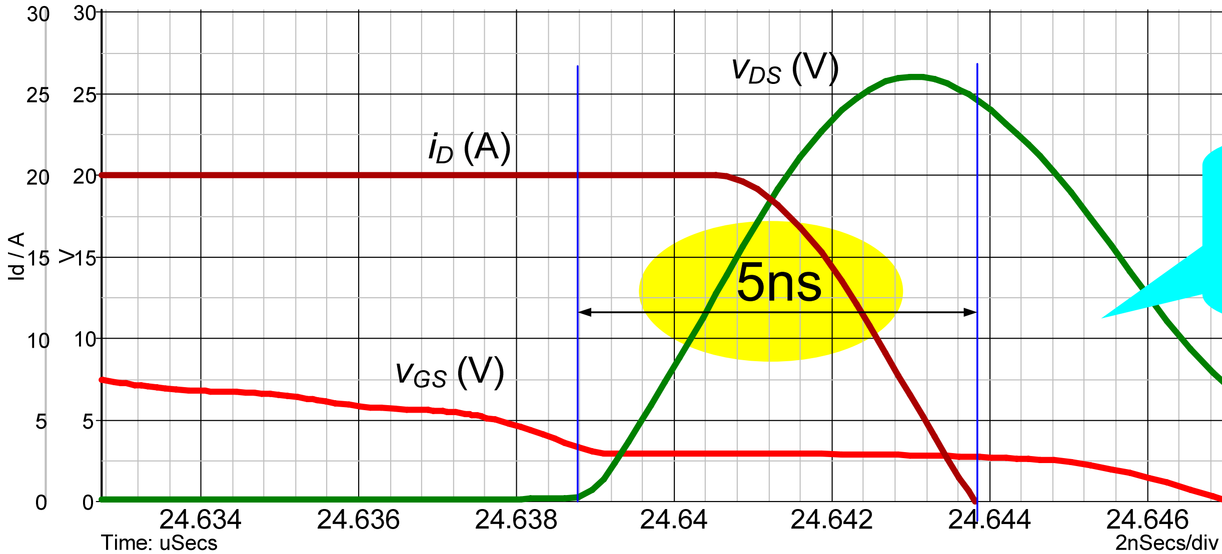
Reduced Turn-On Transition Time:



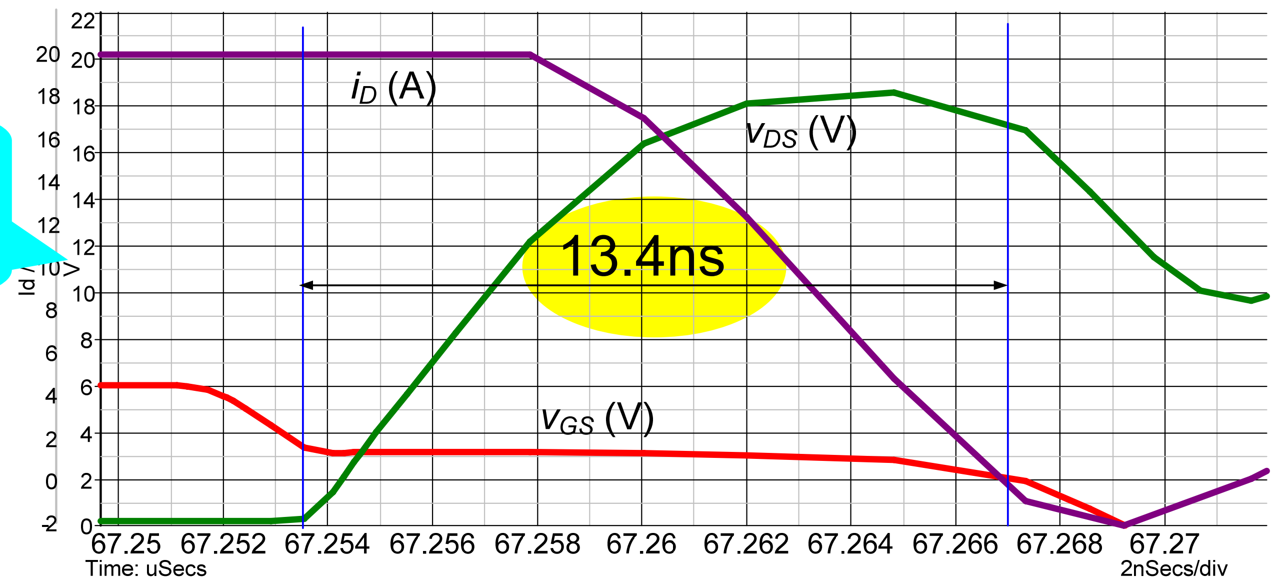


V_{in}=12V, I_o=20A, f_s=1MHz, L_s=1nH, L_D=2nH, R_G=1.5ohm

Reduced Turn-Off Transition Time:



Current-source gate drive



Voltage-source gate drive

V_{in}=12V, I_o=20A, f_s=1MHz, L_s=1nH, L_D=2nH, R_G=1.5ohm

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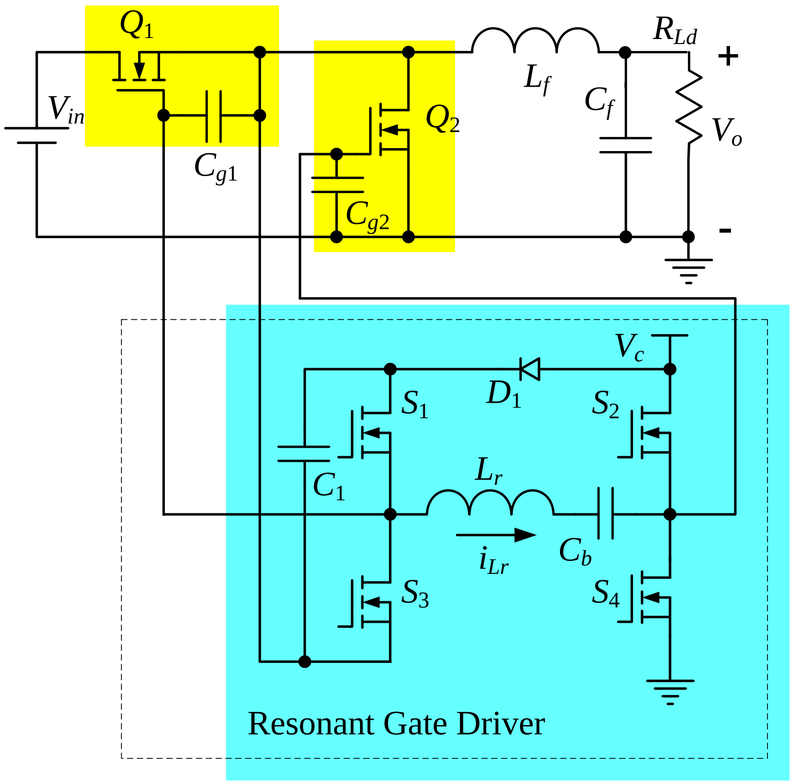
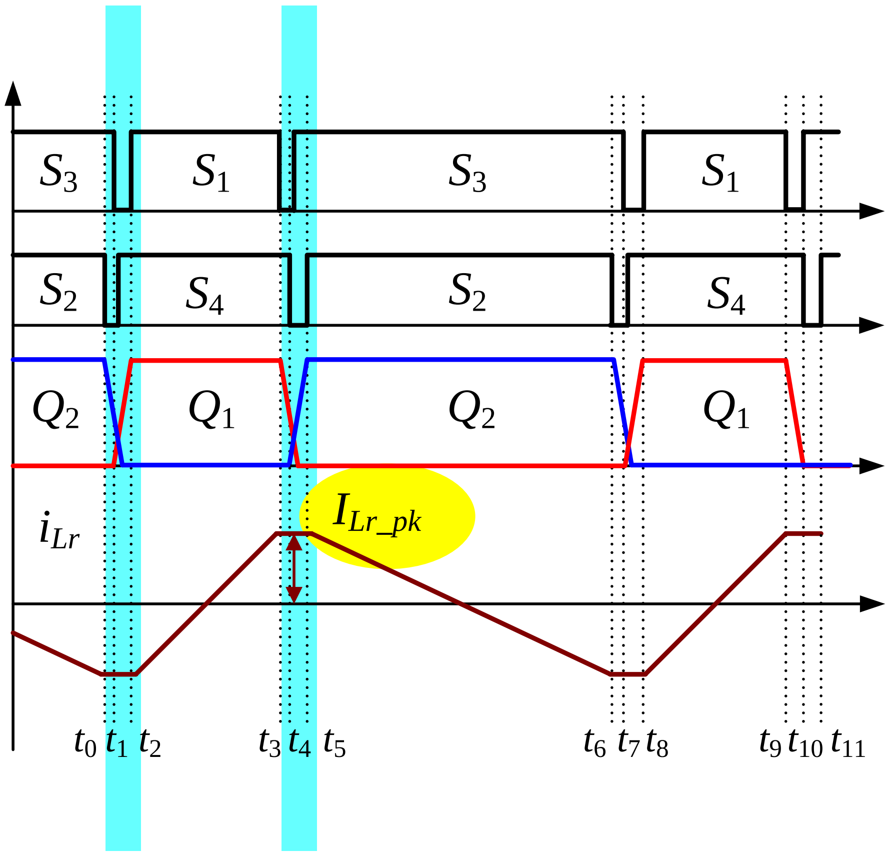
Buck VR with Current-Source Driver*

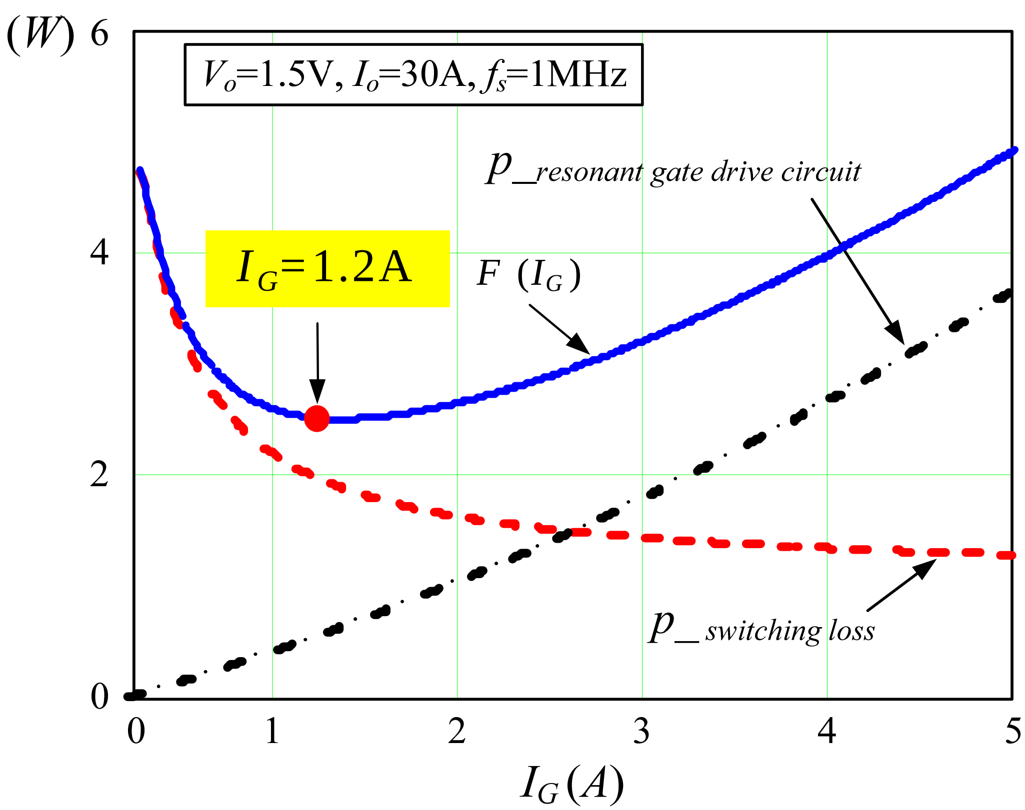




Key waveforms

* Z. Yang, S. Ye and Y. Liu, "A new resonant gate drive circuit for synchronous buck converter," in Proc. IEEE APEC, 2006, pp. 52-58

Gate Charge Current I_G Selection



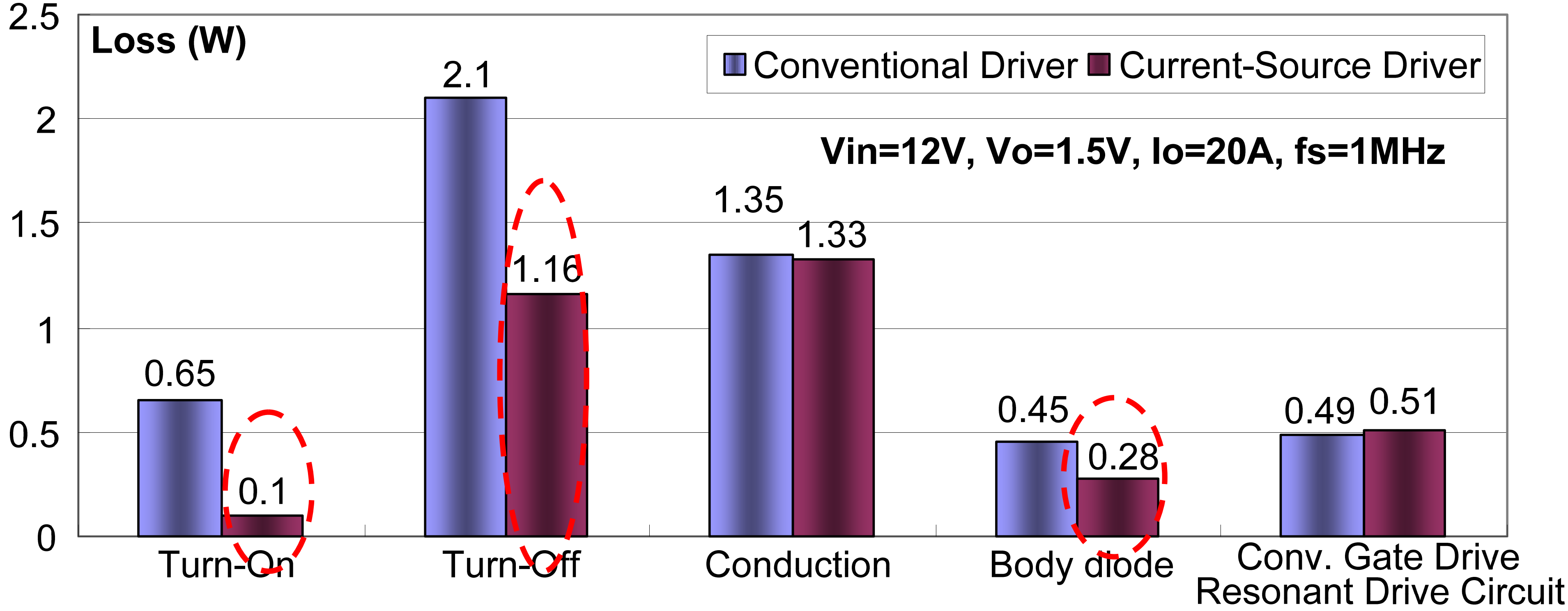
1. Switching loss as function of driven current using **proposed loss Model**

2. Total drive circuit loss as function of I_G

3. Add switching loss and gate driver circuit loss

$$F(I_G) = P_{circuit}(I_G) + P_{switching}(I_G)$$

Loss Comparison: Conventional Driver vs. Current-Source Driver



V_{in}=12V; I_o=20A; f_s=1MHz; Control FET: Vishay Si7860DP ;Syn FET: Vishay Si7336ADP; Drive switches *S*1-*S*4: Fairchild FDN335N

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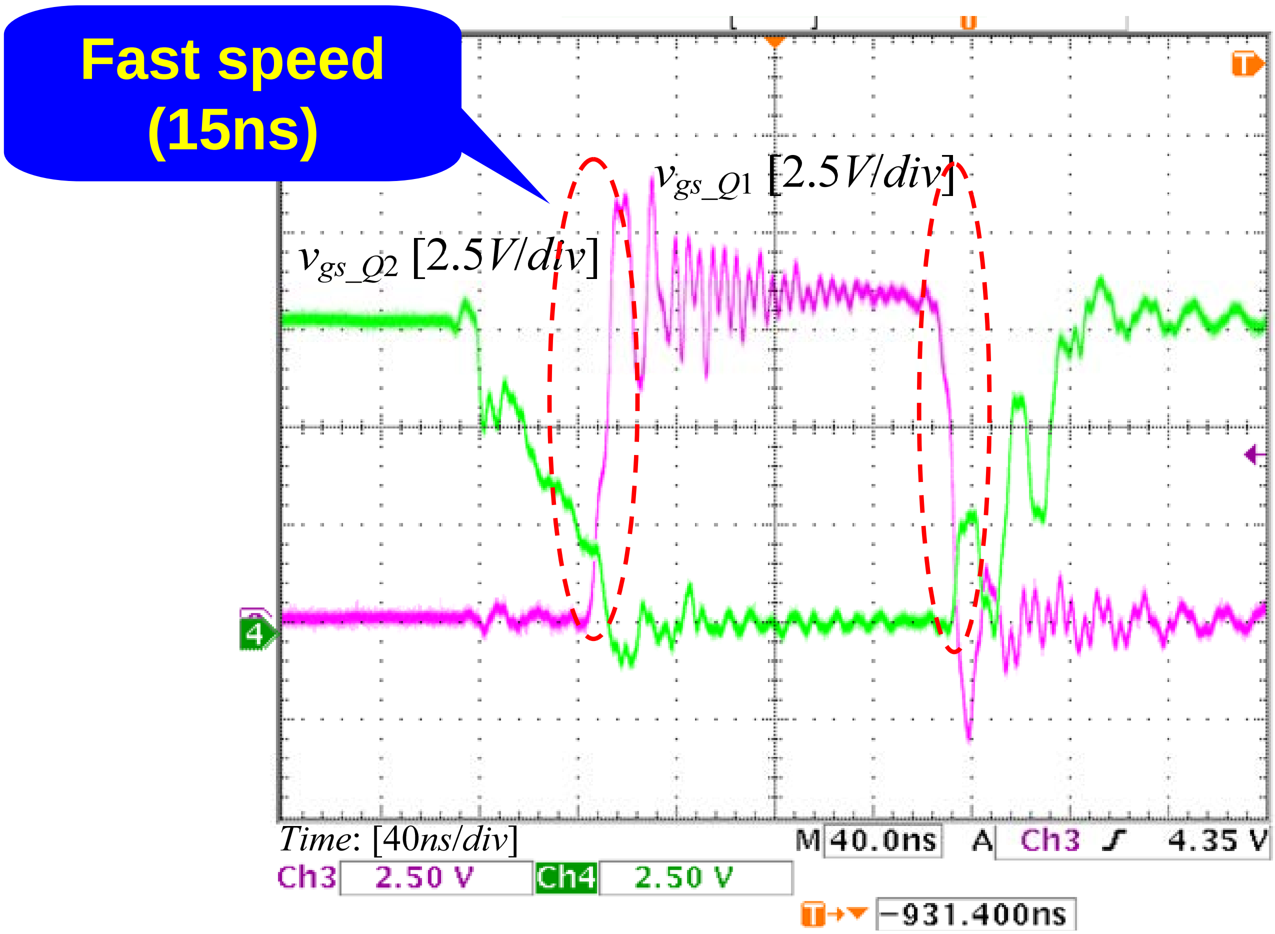
Experimental Prototype

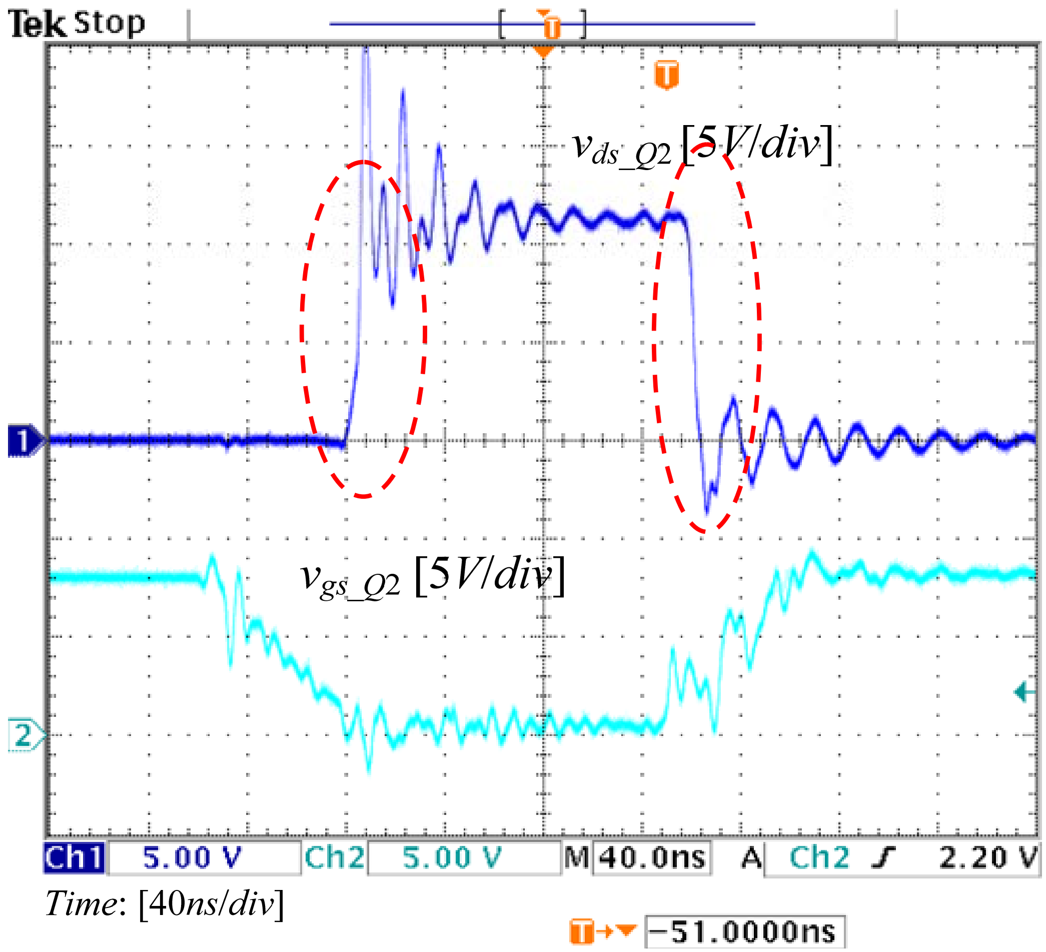
- V_{in}=12V; V_o=1.5V; I_o=30A; f_s=1MHz
- Resonant driver voltage V_c=8V
- Six-layer 2 oz copper
- Control FET: Vishay Si7860DP
- Synchronous FET: Vishay Si7336ADP
- Drive switches: Fairchild FDN335N
- Output filter inductance: 330nH (IHLP-5050CE-01, Vishay)
- Resonant inductor: L_r=1.5uH

Fast Switching Speed



Gate drive signals (control FET and synchronous FET)

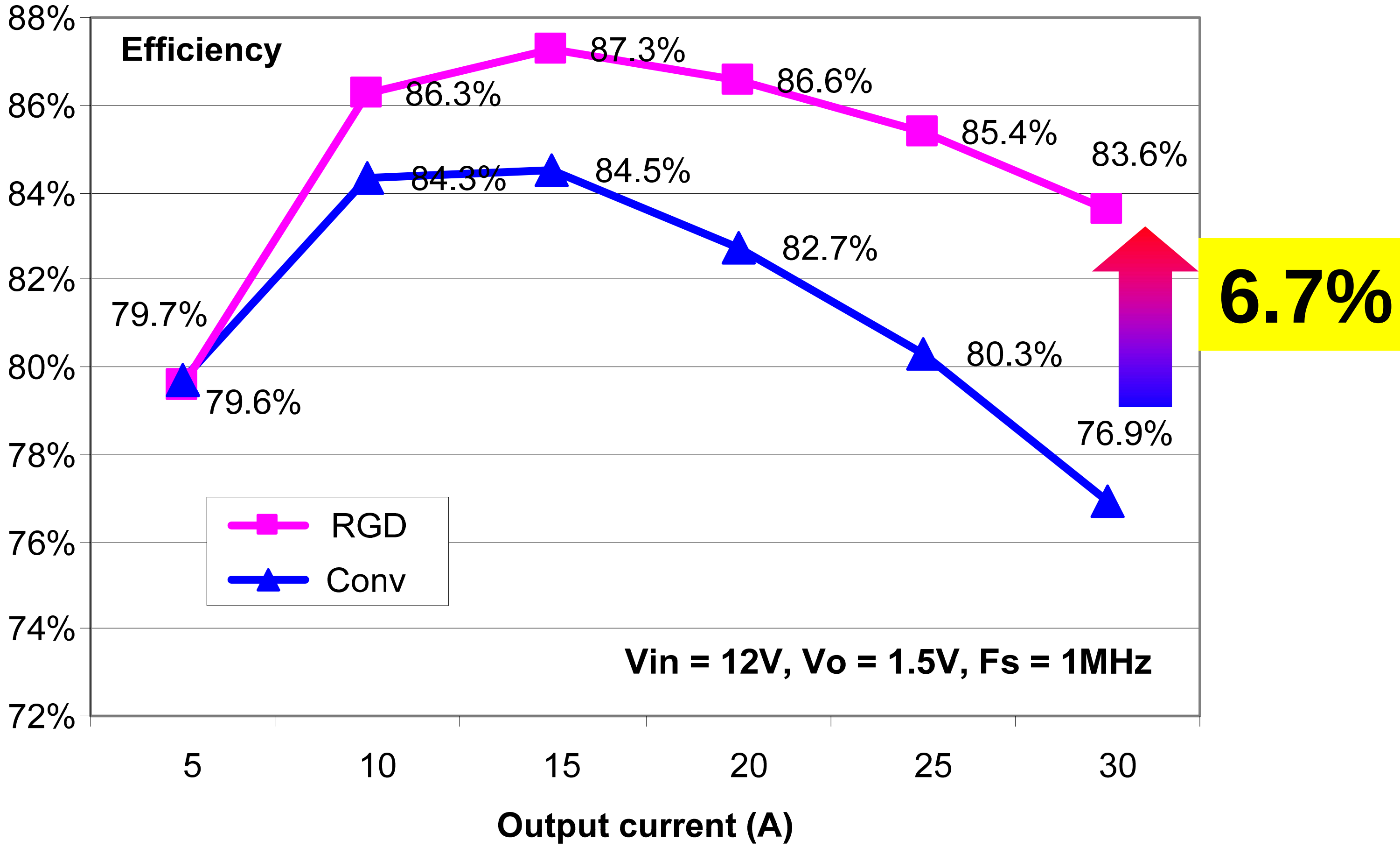
Reduced Body-Diode Conduction



Time: [40*ns*/*div*]

Drain-source voltage and gate drive signal (synchronous FET)

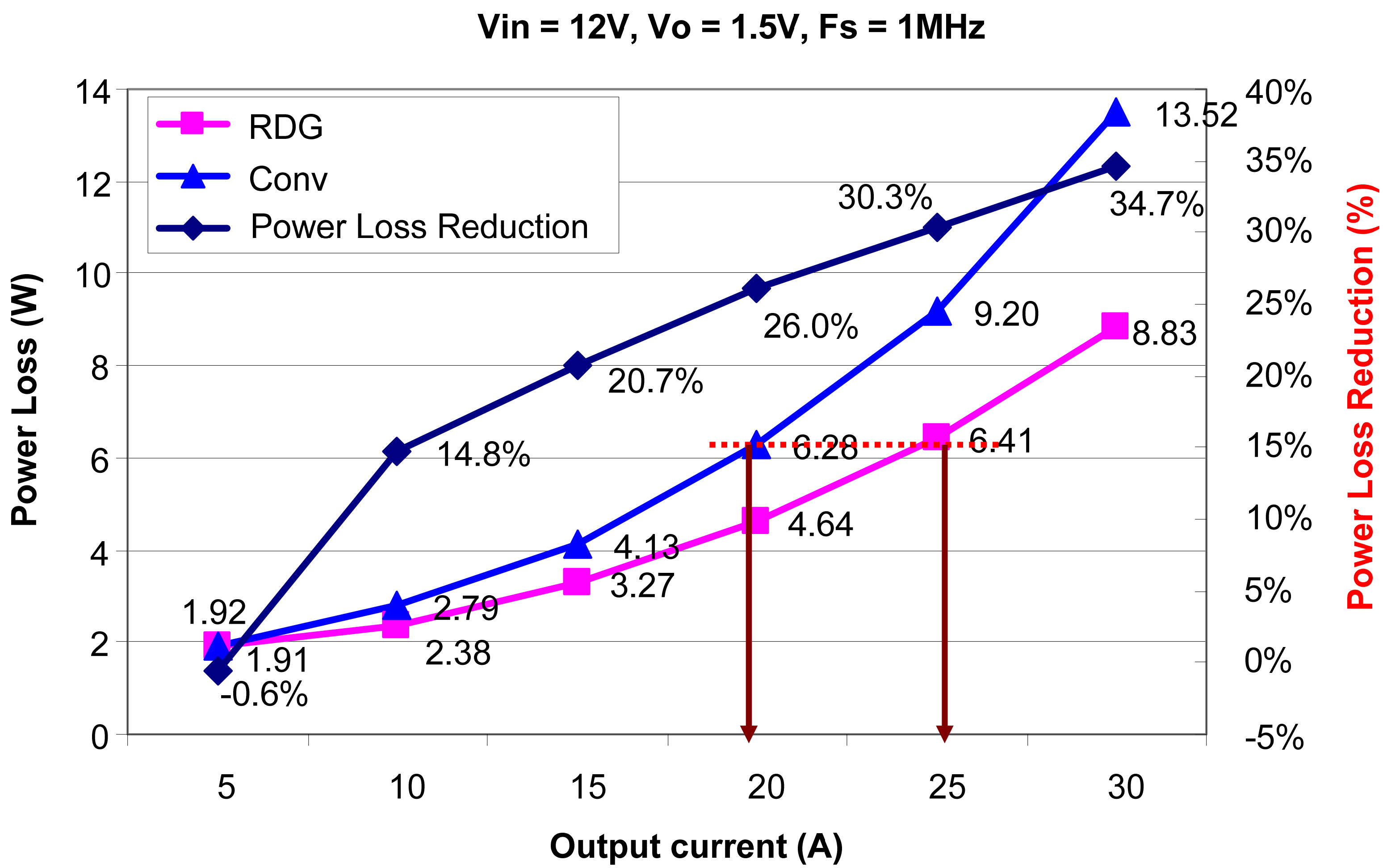
Efficiency Improvement



Top: optimized current-source driver

Bottom: conventional driver (Conv.) Predictive Drive UCC 27222 (TI)

Loss Reduction



Extra Phase Saved: Total VR output current=100A

5 Phases with conventional driver (100A/20A)

4 Phases with current-source driver (100A/25A)

Efficiency Comparison of State of the Art VRs

Input voltage: 12V and switching frequency: 1MHz			
VR Topologies	Efficiency	Current/ Phase	Output voltage
Tapped-inductor buck converter	84%	12.5A	1.5V
Toshiba buck Multi Chip Module (TB7001FL)	85%	20A	1.5V
Current-source driver	87%	12.5A	1.5V
	86.6%	20A	1.5V
Soft-switching phase-shift buck converter	82%	17.5A	1.3V
Self-driven soft-switching multiphase converter	84.9%	25A	1.3V
Current-source driver	86%	17.5A	1.3V
	84.3%	25A	1.3V

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Conclusion

- A new MOSFET loss model with current-source gate driver is proposed
- Optimal design method for a Buck VR with current-source gate driver is proposed
- A significant efficiency improvement is achieved: **86.6%** efficiency (3.9% improvement)@1.5V/20A/1MHz; **83.6%** efficiency (6.7% improvement) @1.5V/30A/1MHz; Extra phase is saved for 1.5V/100A
- High performance and cost-effectiveness approach

Thank You For Your Time

Other Current-source Gate Drive Material at:

www.QueensPowerGroup.com