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A Resonant Gate Drive Circuit with Reduced MOSFET Switching and Gate Losses

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Presentation Overview

1. *Introduction*
   1. *Why you should use resonant gate drive*
   2. *Drawbacks of existing techniques*
2. Proposed Resonant Gate Driver and Operation
3. Logic Implementation
4. Design Procedure
5. Loss Analysis
6. Simulation and Experimental Results
7. Conclusions

1. Introduction

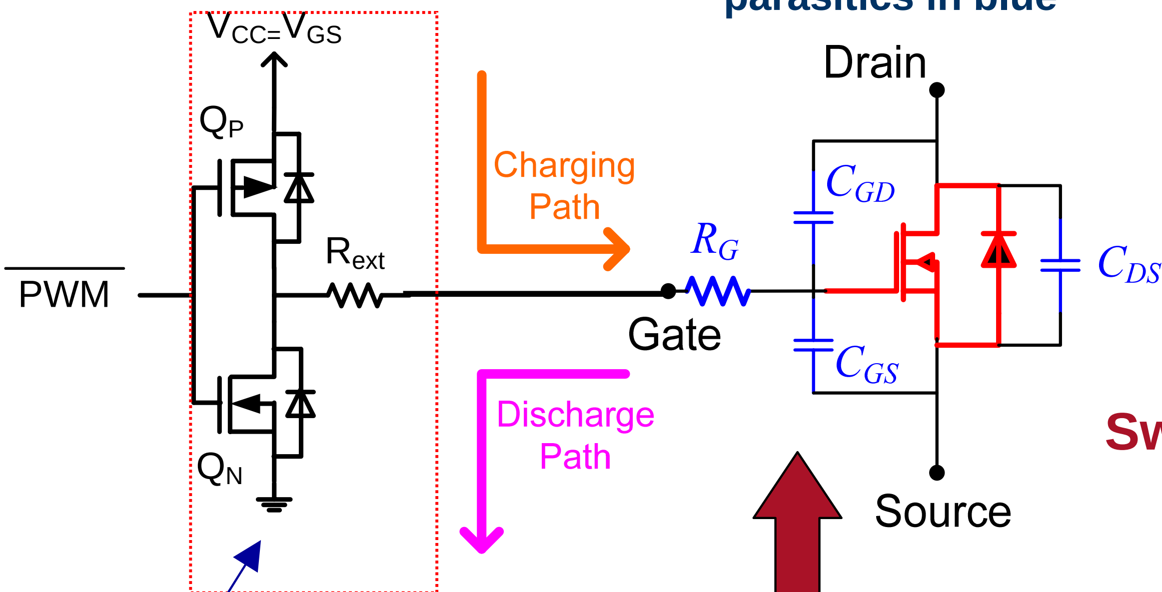
- **Application:** low voltage high current DC-DC power supplies
- Trend to increase switching frequency for improvements in:
  - \+ power density
  - \+ dynamic performance
- Drawbacks of increased switching frequency:
  - \- gate loss
  - \- switching loss

Conventional MOSFET Driver

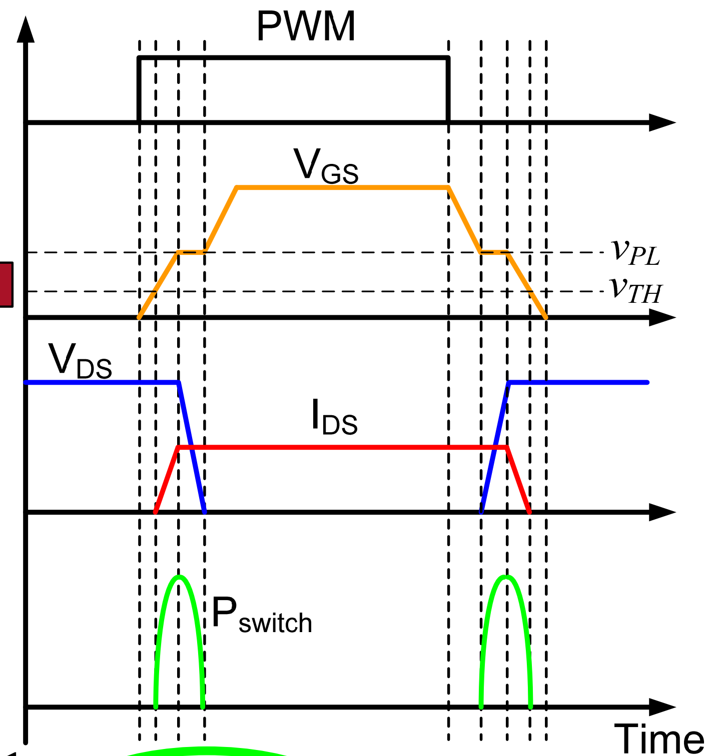
MOSFET Driver

Power MOSFET

parasitics in blue



Hard Switching Waveforms



MOSFET, or BJT switches

Switching Loss

Gate Loss

$$P_{gate} = Q_g V_{GS} f_S$$

$$P_{switch} = \frac{1}{2}(t_{rise} + t_{fall}) V_{DS} I_{DS} f_S$$

$$P_{out} = \frac{1}{2} C_{DS} V_{DS}^2 f_S$$

Switching Loss Savings

Soft-Switching and Resonant Techniques

+ Well established and generally, have good performance
- Additional components
- Additional conduction loss
- Don't reduce turn-off loss

Another Solution: Decrease switching time!

- Recall, switching loss proportional to rise time and fall time

Gate Loss Savings

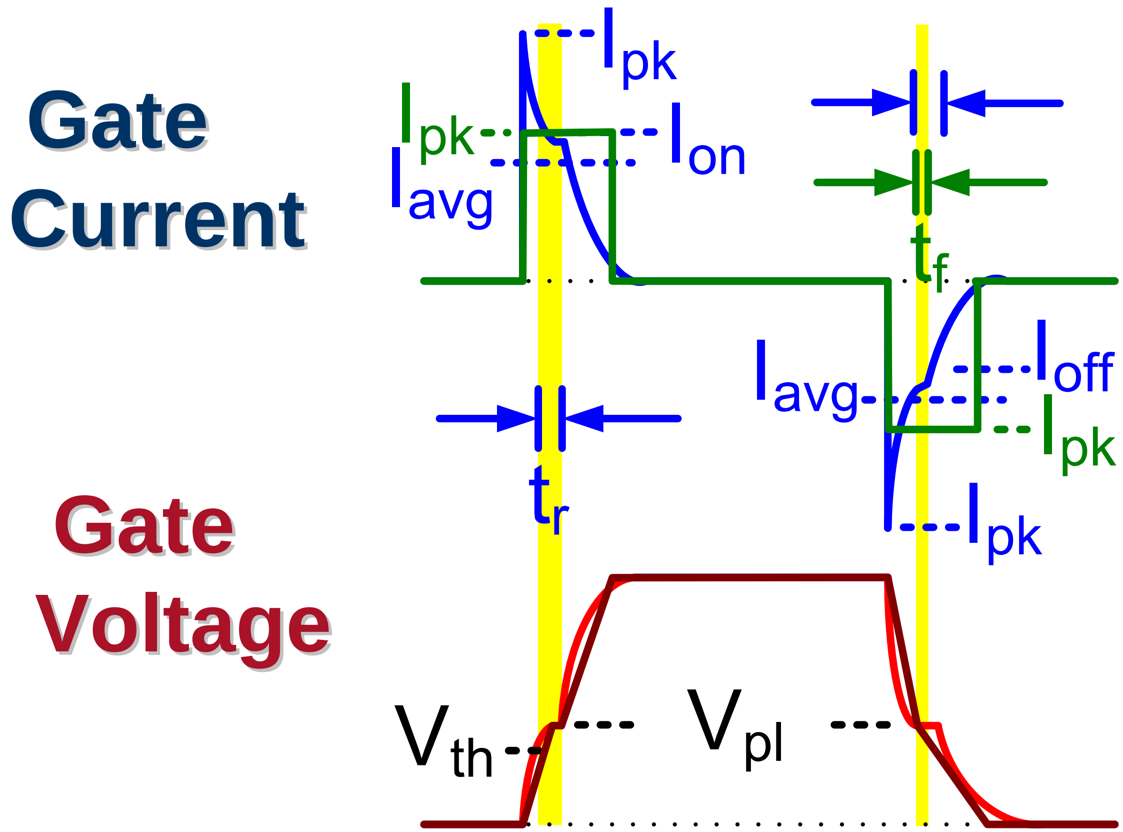
Resonant Gate Drive Techniques

+ Many good (~15) circuits proposed since early 1990s, but generally unused

- Existing methods emphasize gate energy savings, but ignore potential switching loss savings

CURRENT SOURCE DRIVERS CAN REDUCE TURN-ON AND TURN-OFF LOSS!

Conventional vs. Resonant Drive Switching Loss Savings



Voltage source RC-type charging limits speed

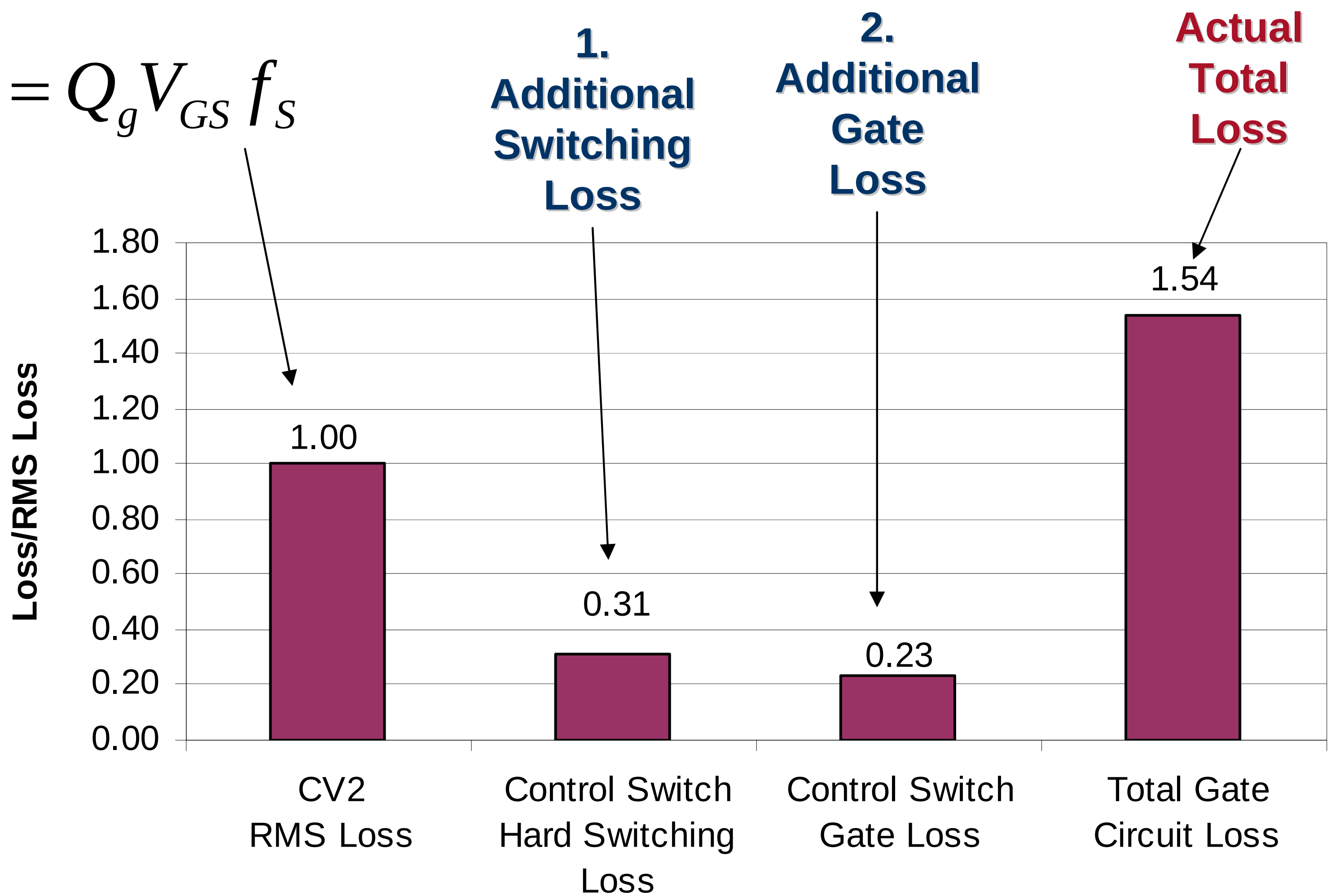
Constant current source type charging improves speed!

Additional Conventional Driver Loss

Actual driver loss can be much higher than CV^2 loss…

e.g. varies by driver, but typically 15-50%

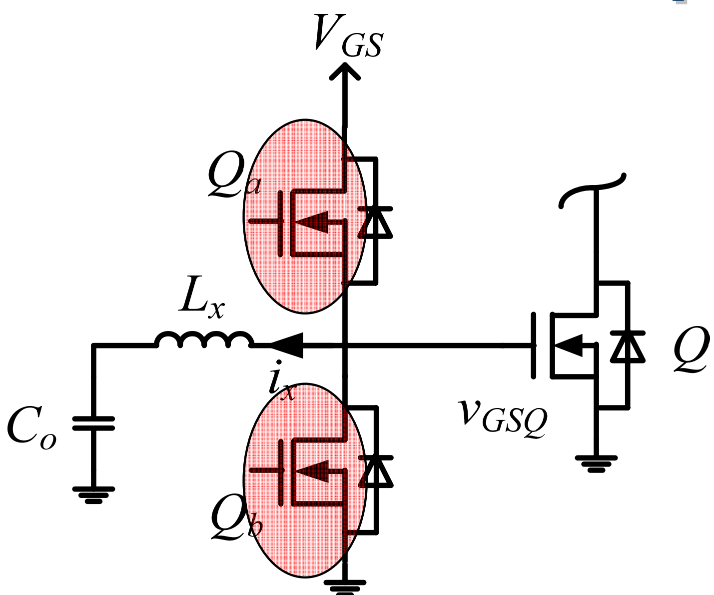
$$P_{gate} = Q_g V_{GS} f_S$$

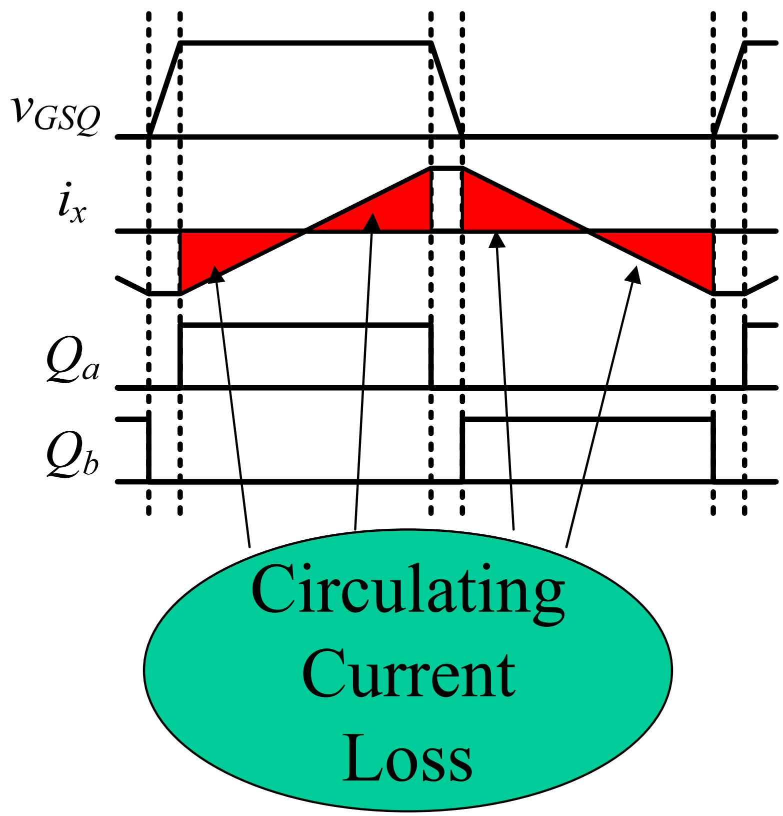


Resonant Gate Drive Review

Existing techniques suffer from at least one of five problems:

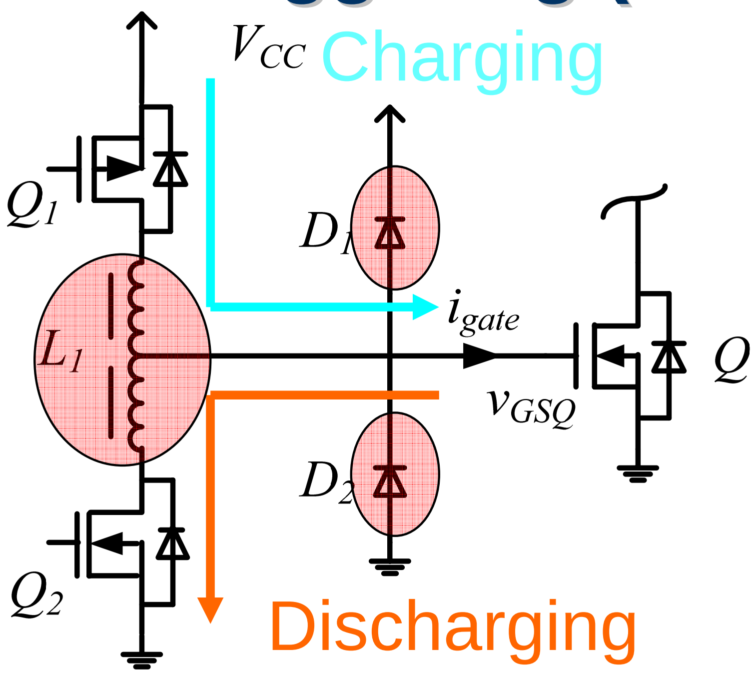
1. Circulating current conduction loss [2]
2. Peak current dependent on duty cycle [2]

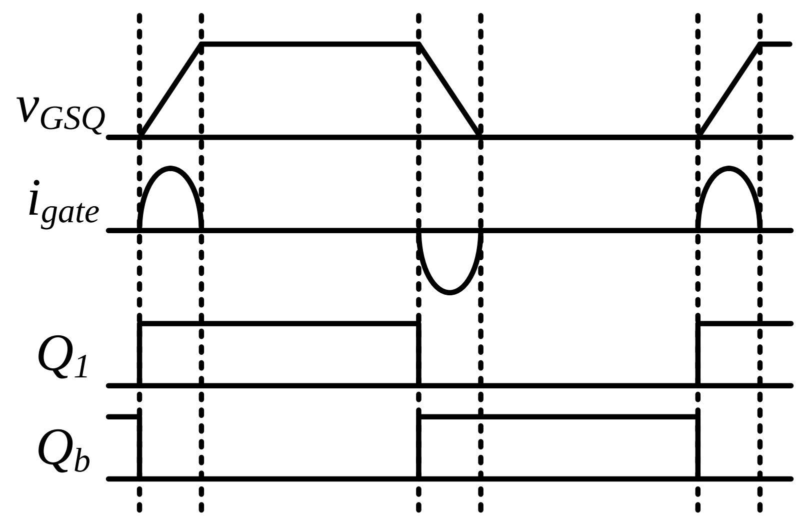




Resonant Gate Drive Review

3. Large inductance [2], bulky transformer, or coupled inductor [3]-[7]
4. Slow turn-on and/or turn-off [3]-[9]
5. Gate not actively clamped high and/or low, so false triggering (Cdv/dt) can result [3]-[7], [9]





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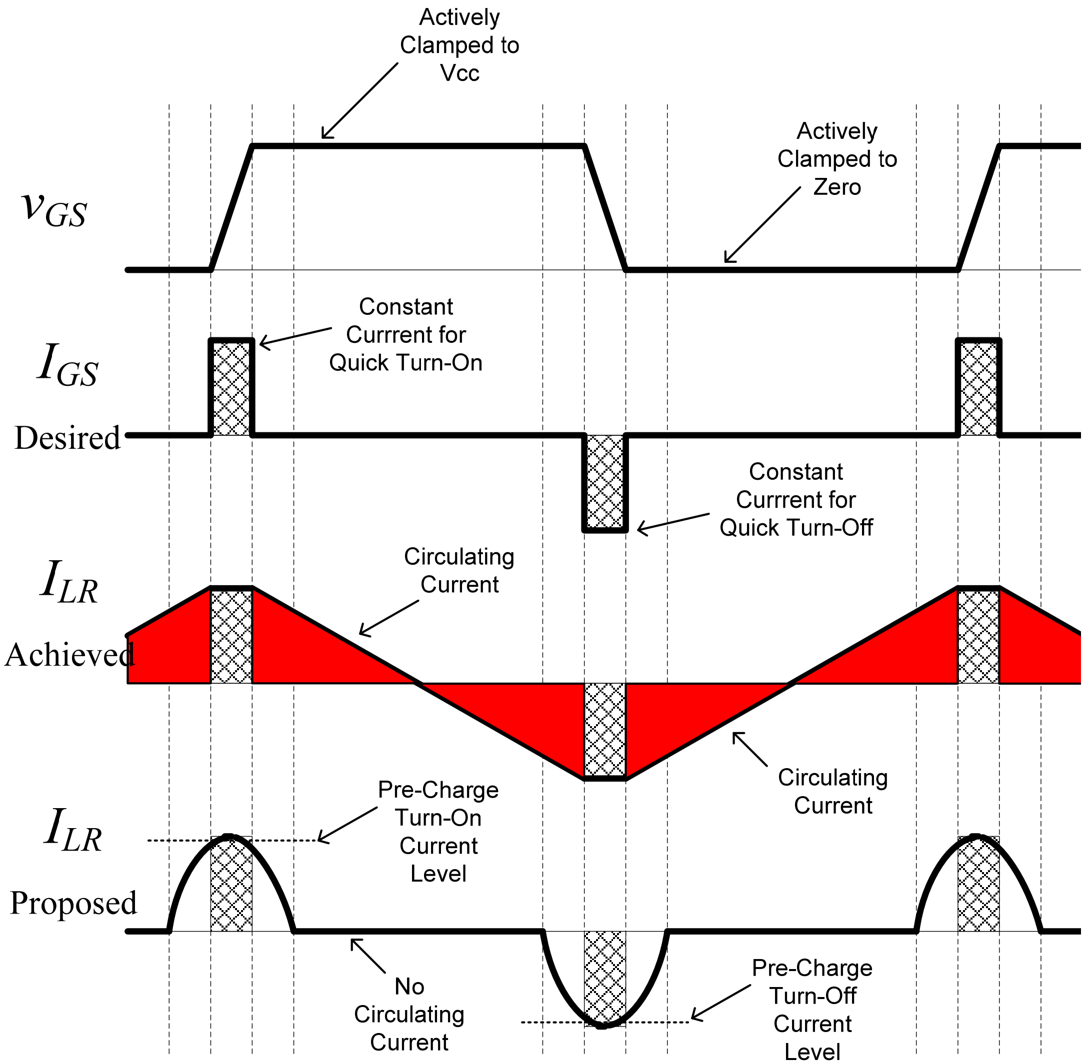
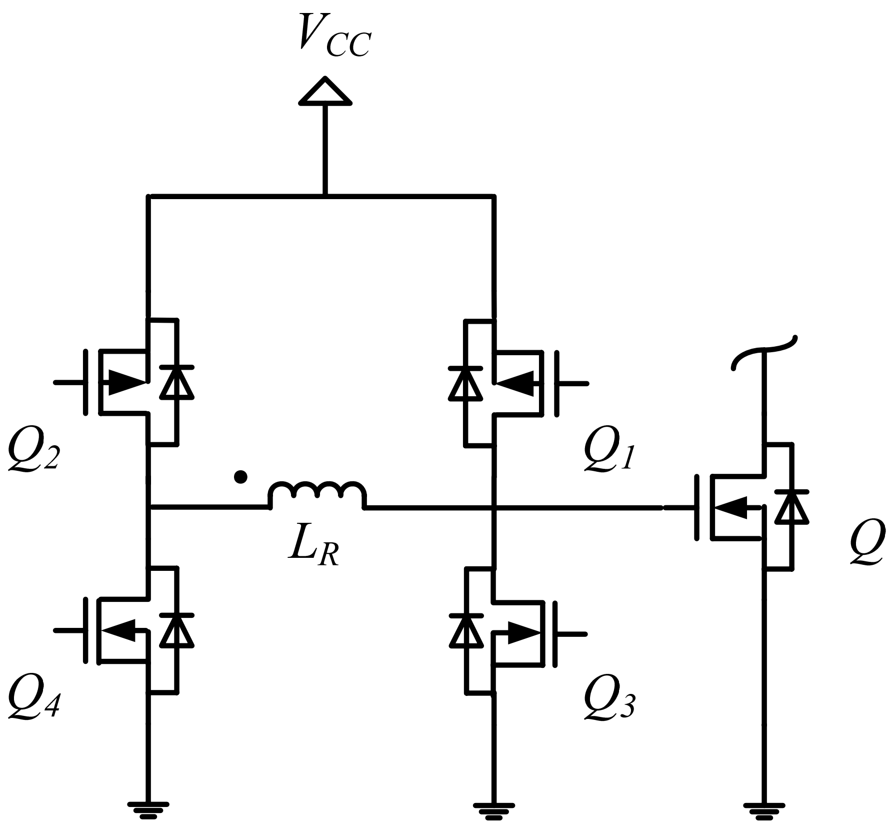
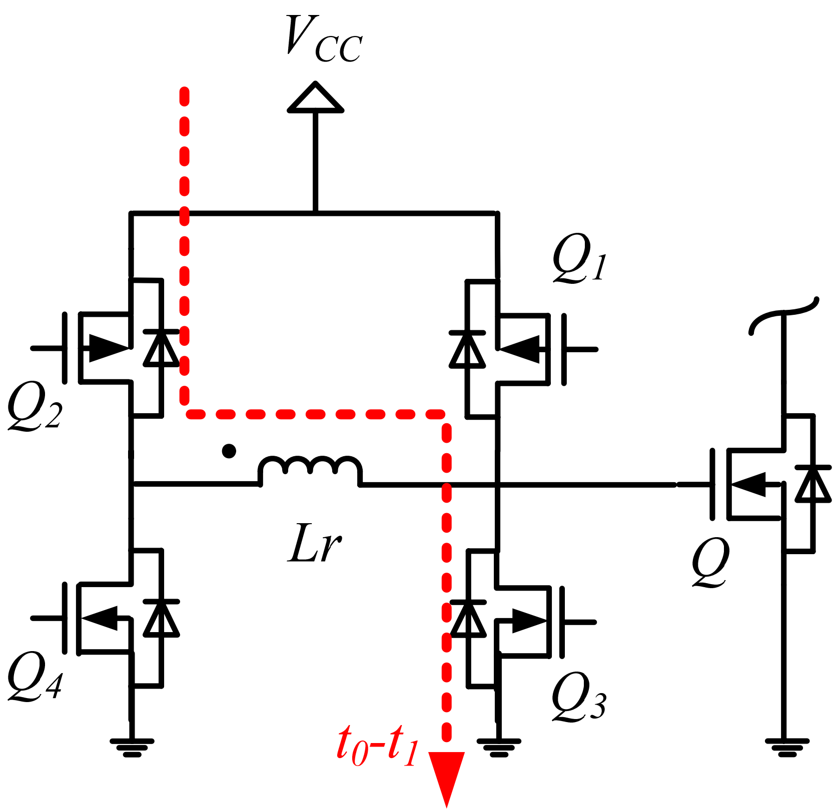
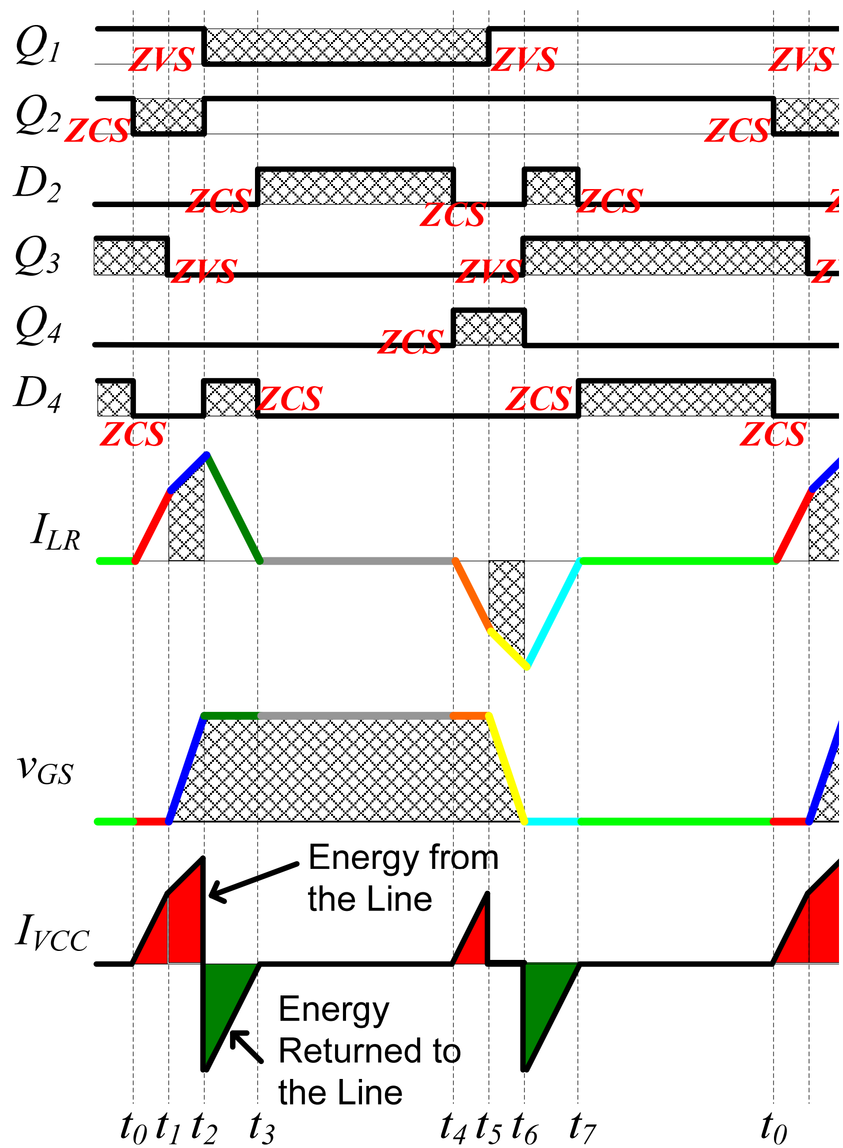
Proposed Driver Evolution





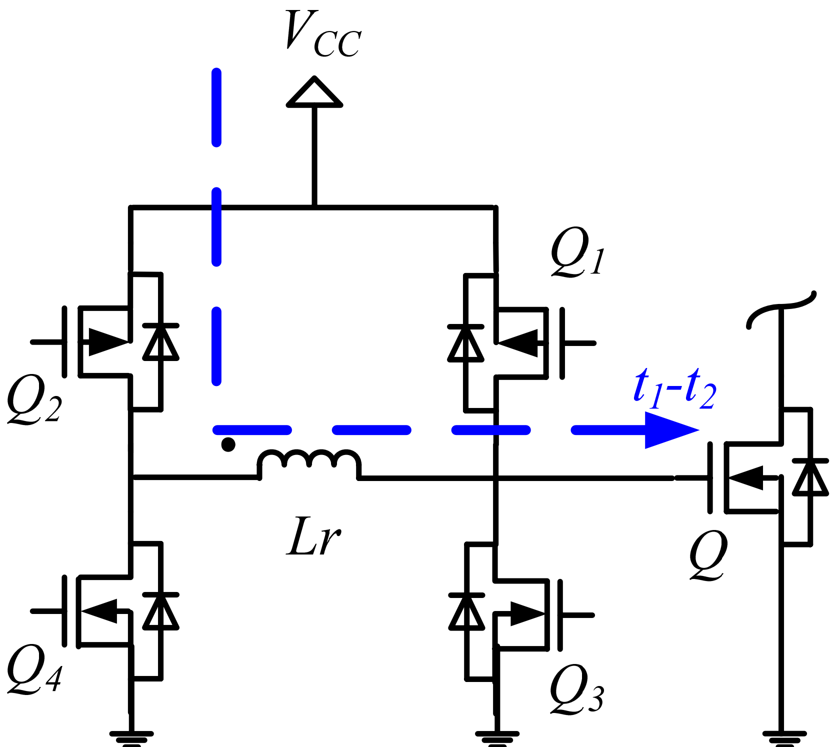
Turn-On Sequence





Switches Can Also Be Used Instead of Diodes

Turn-On Sequence



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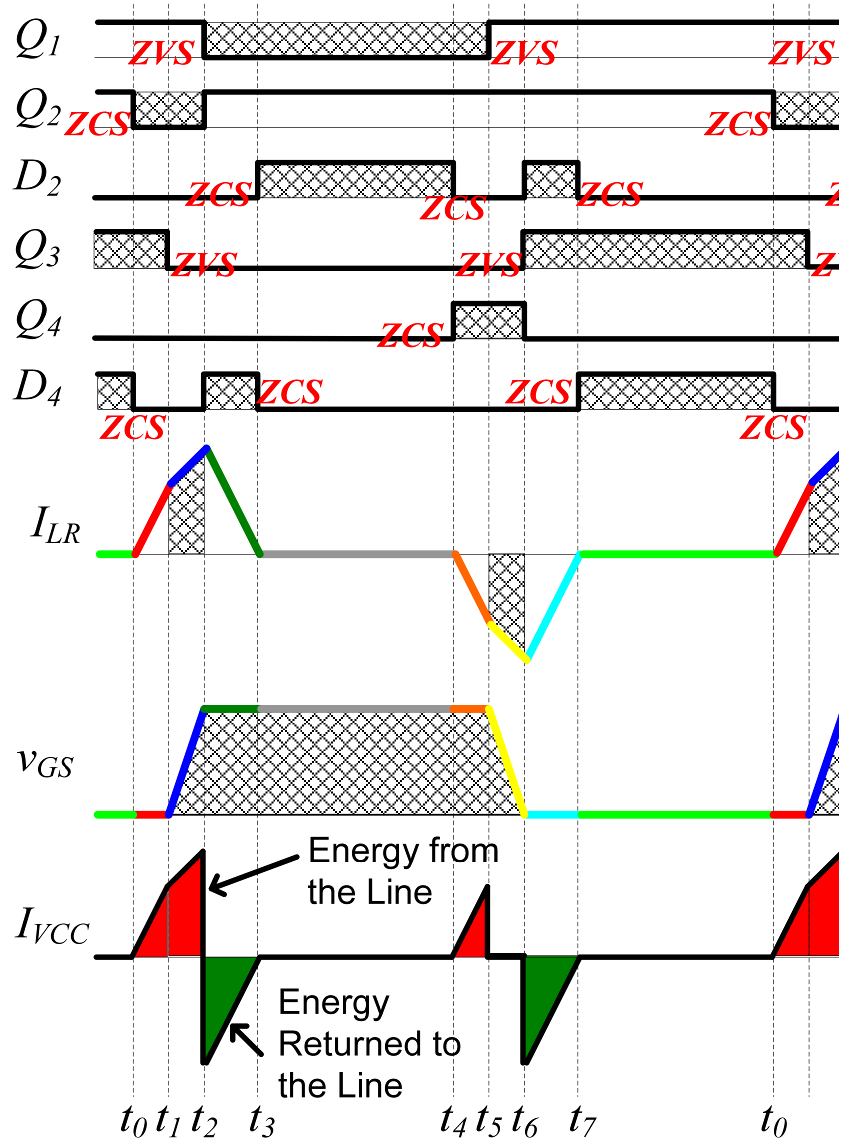

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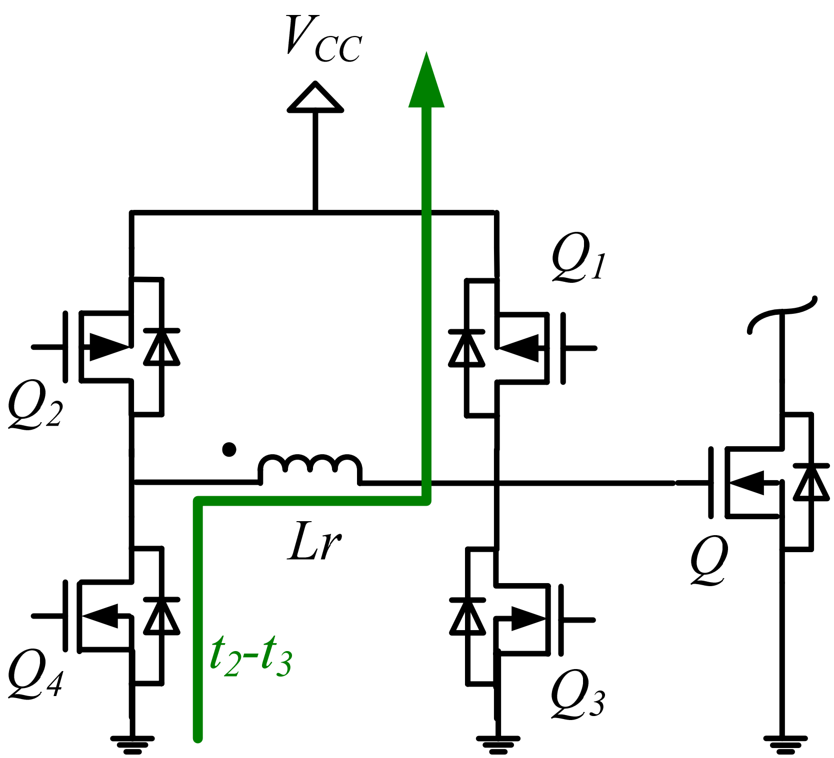

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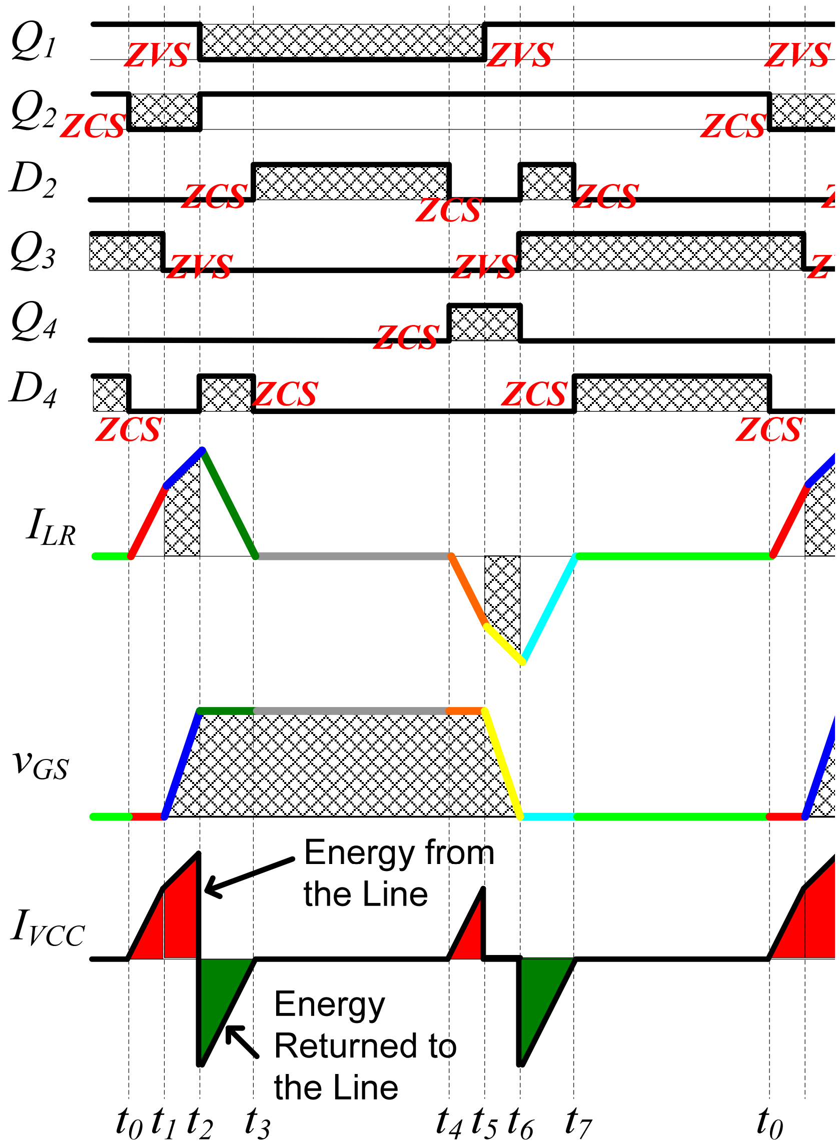
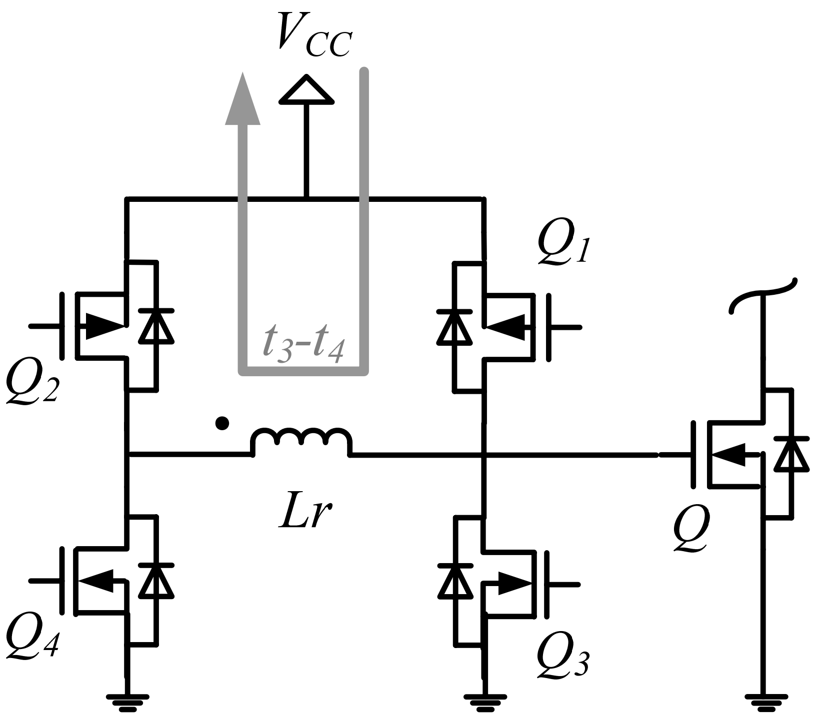


Turn-On Sequence



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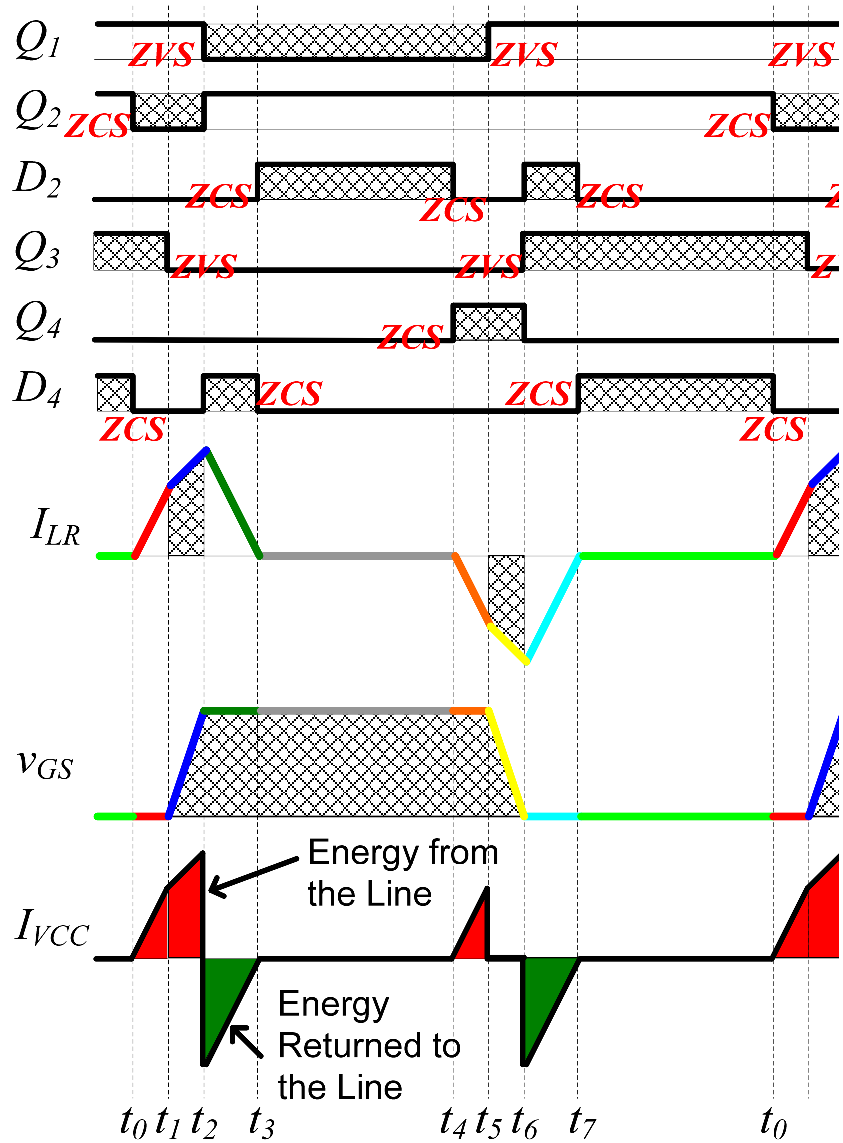
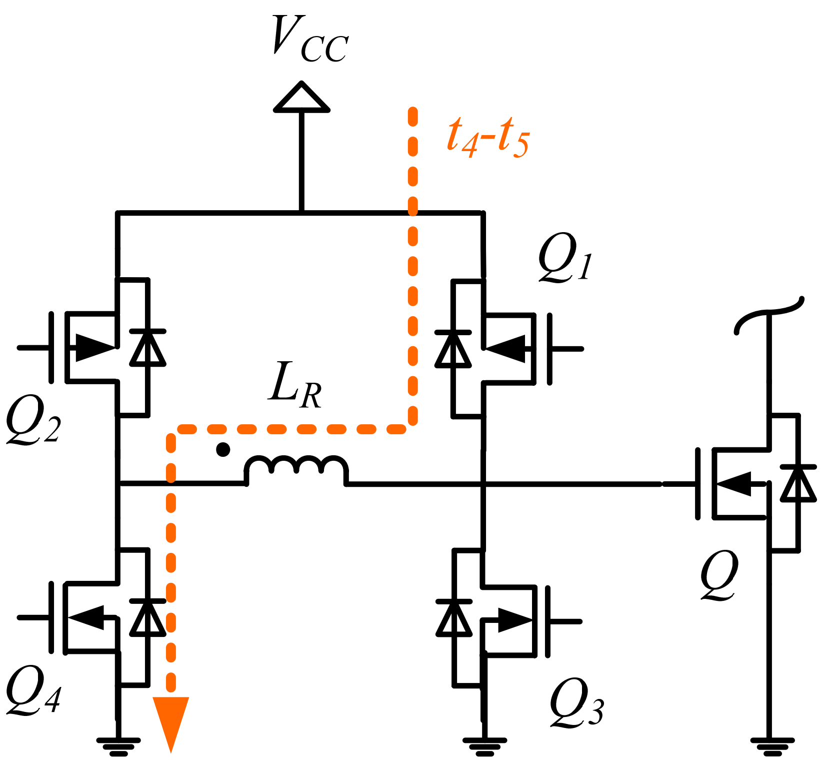
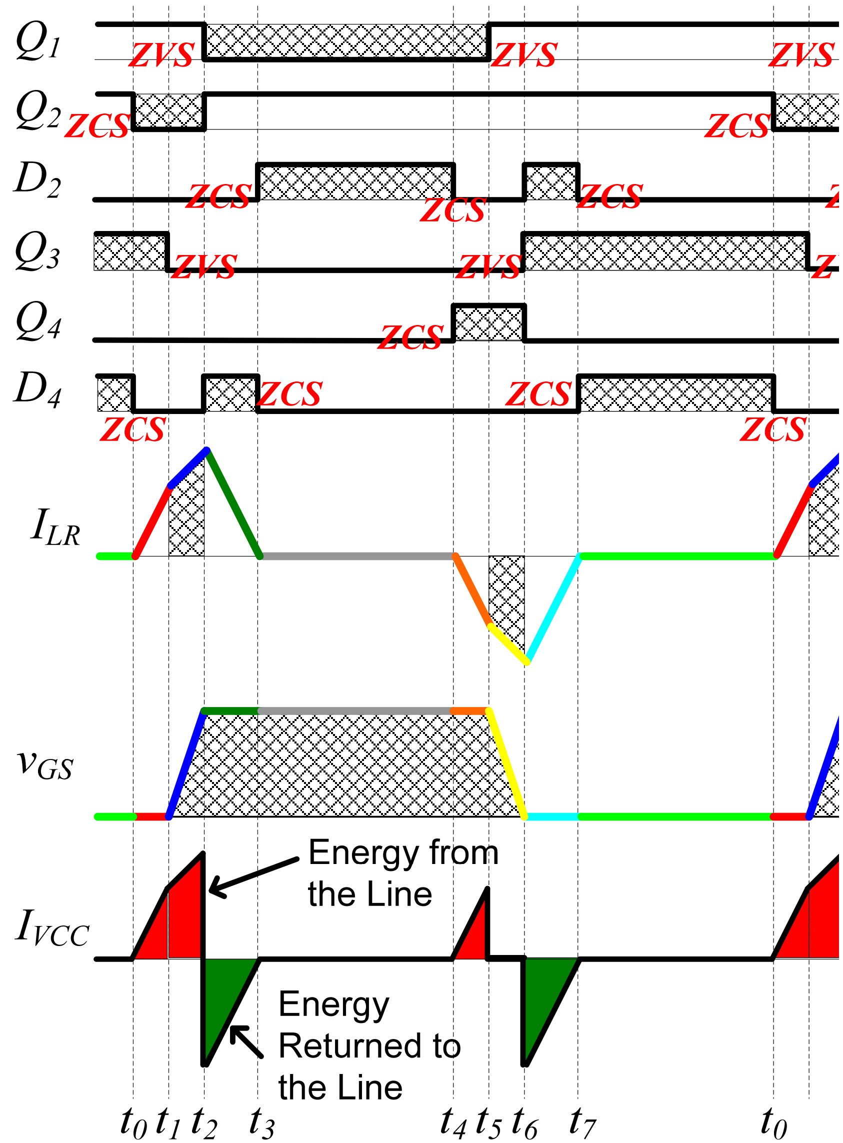


Turn-Off Sequence





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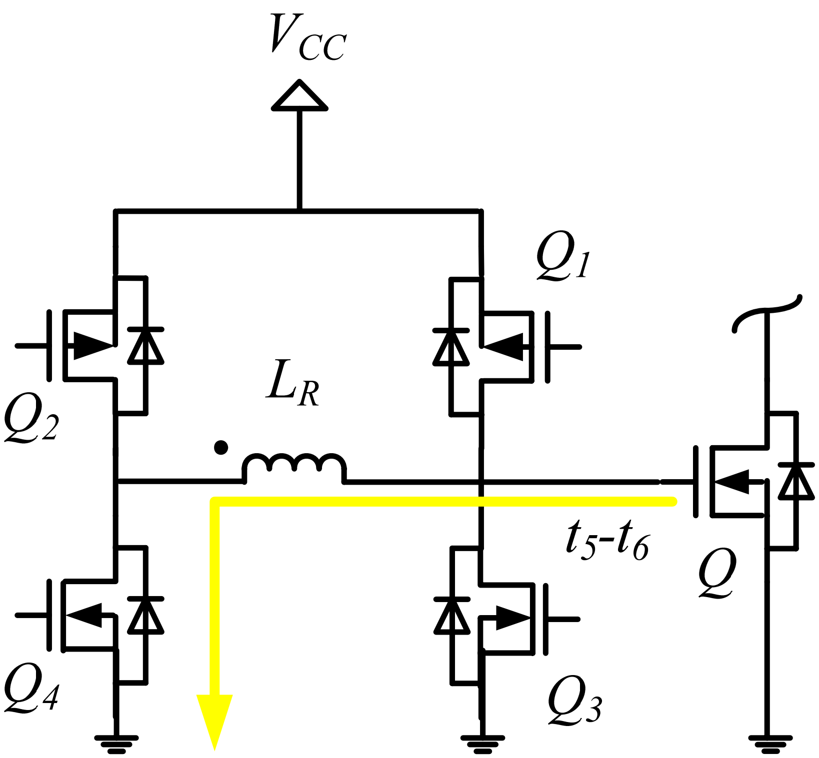
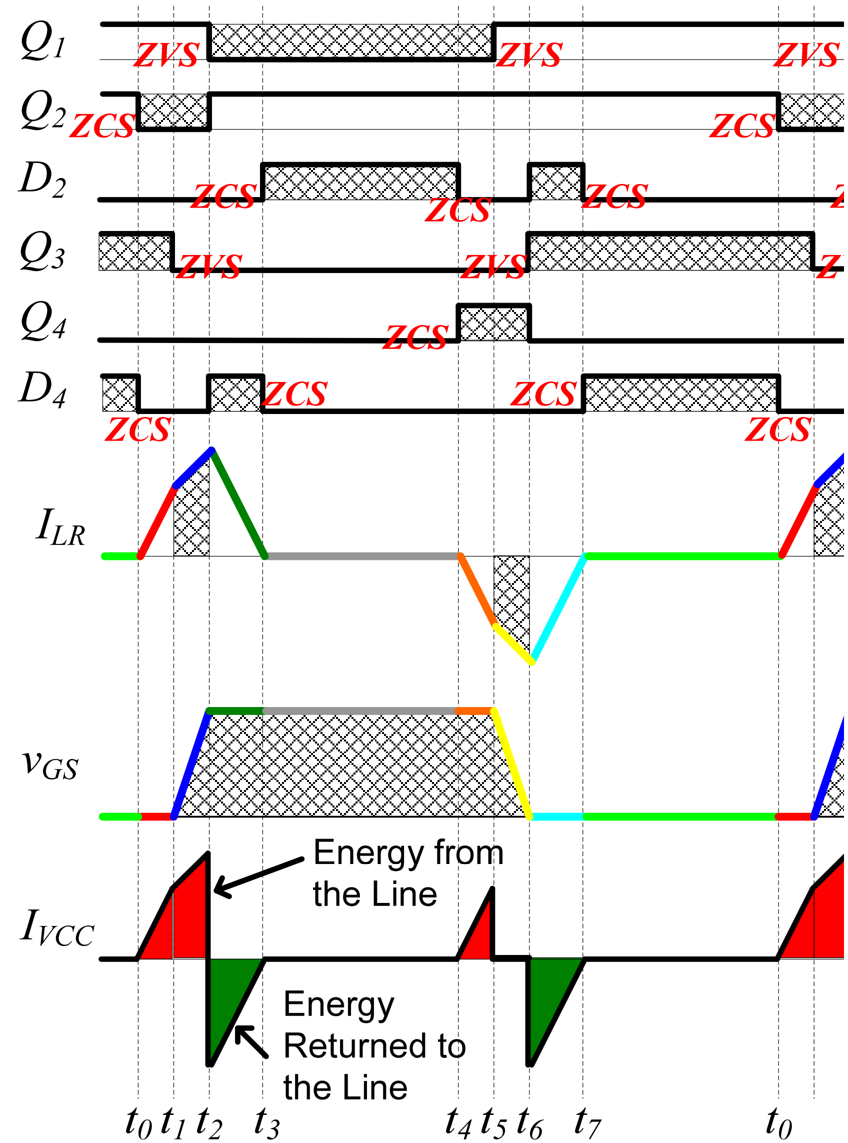
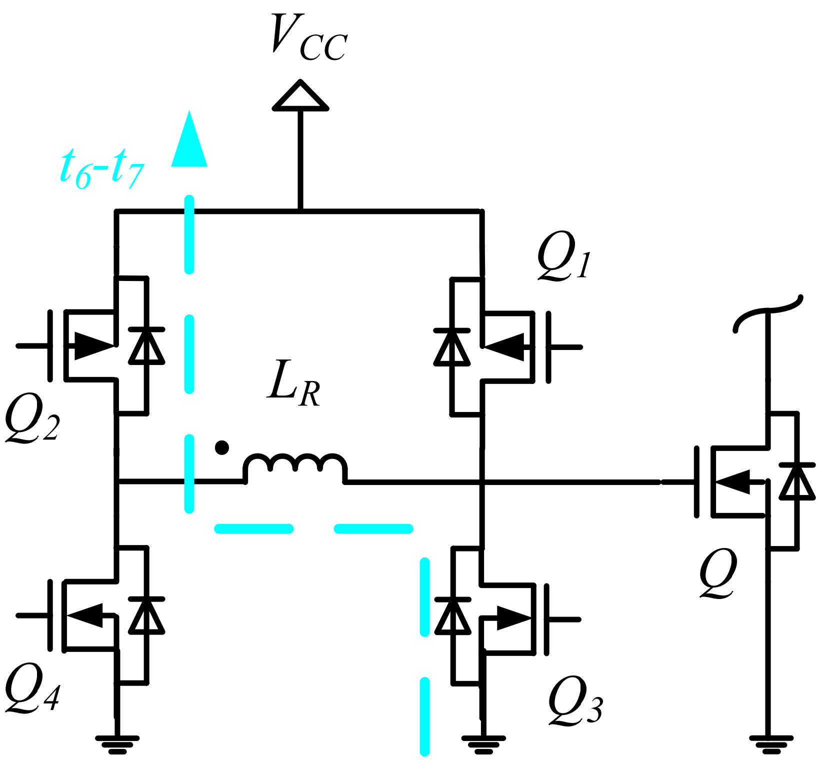
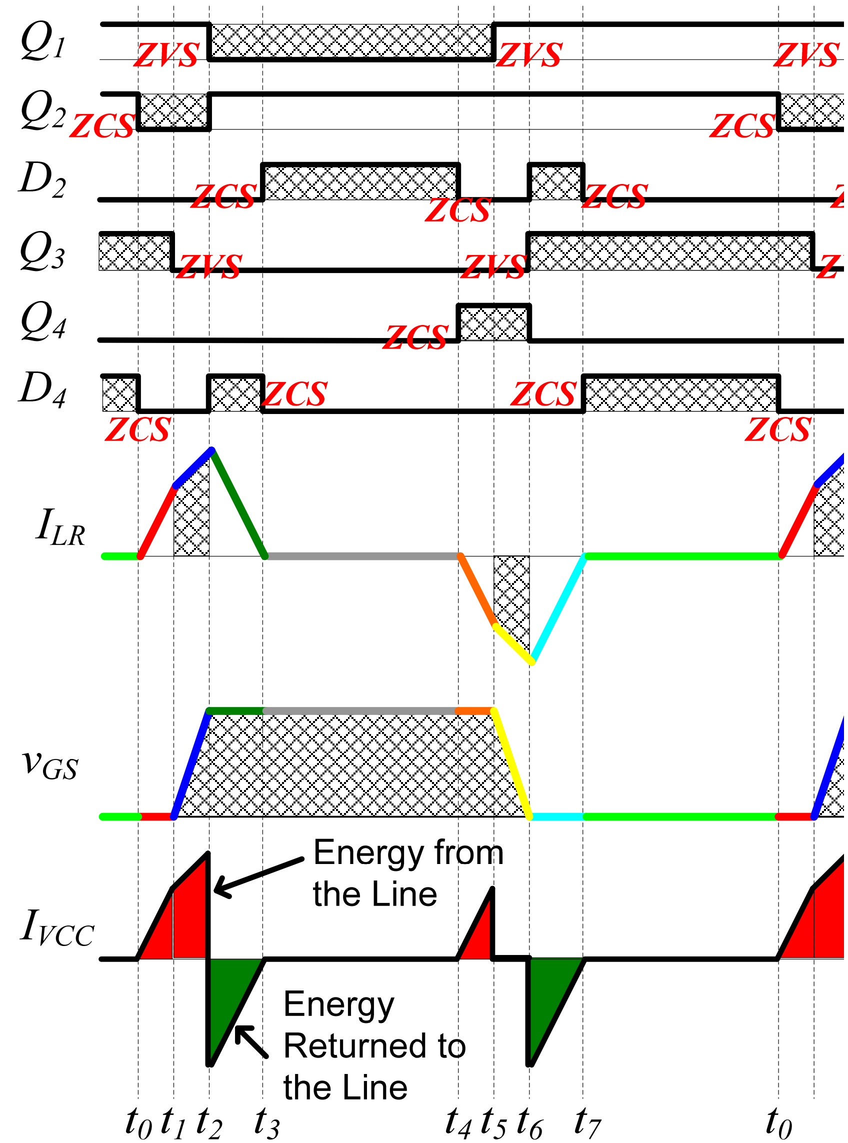


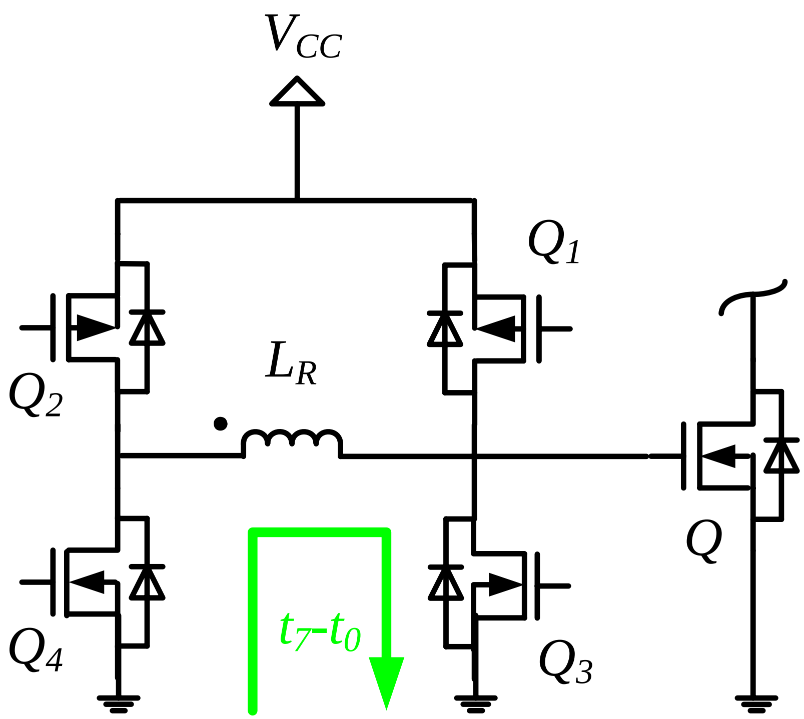


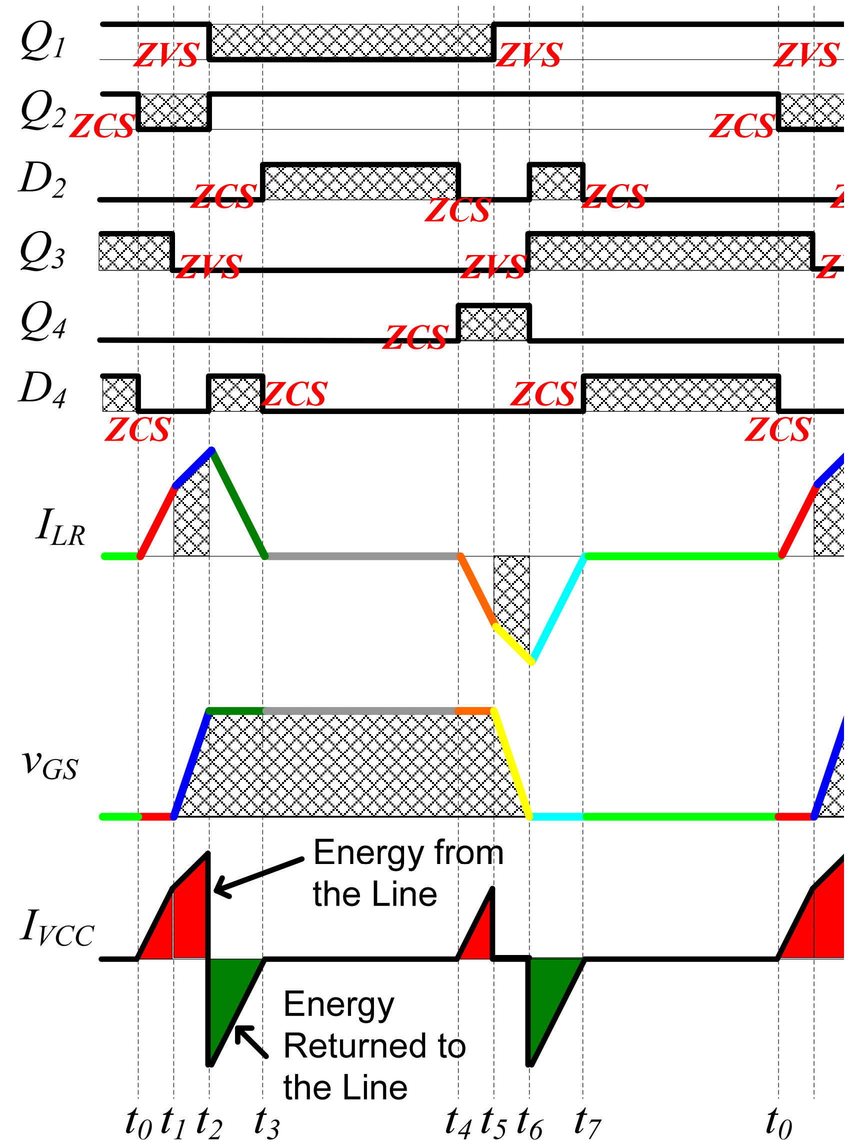
Turn-Off Sequence





Turn-Off Sequence





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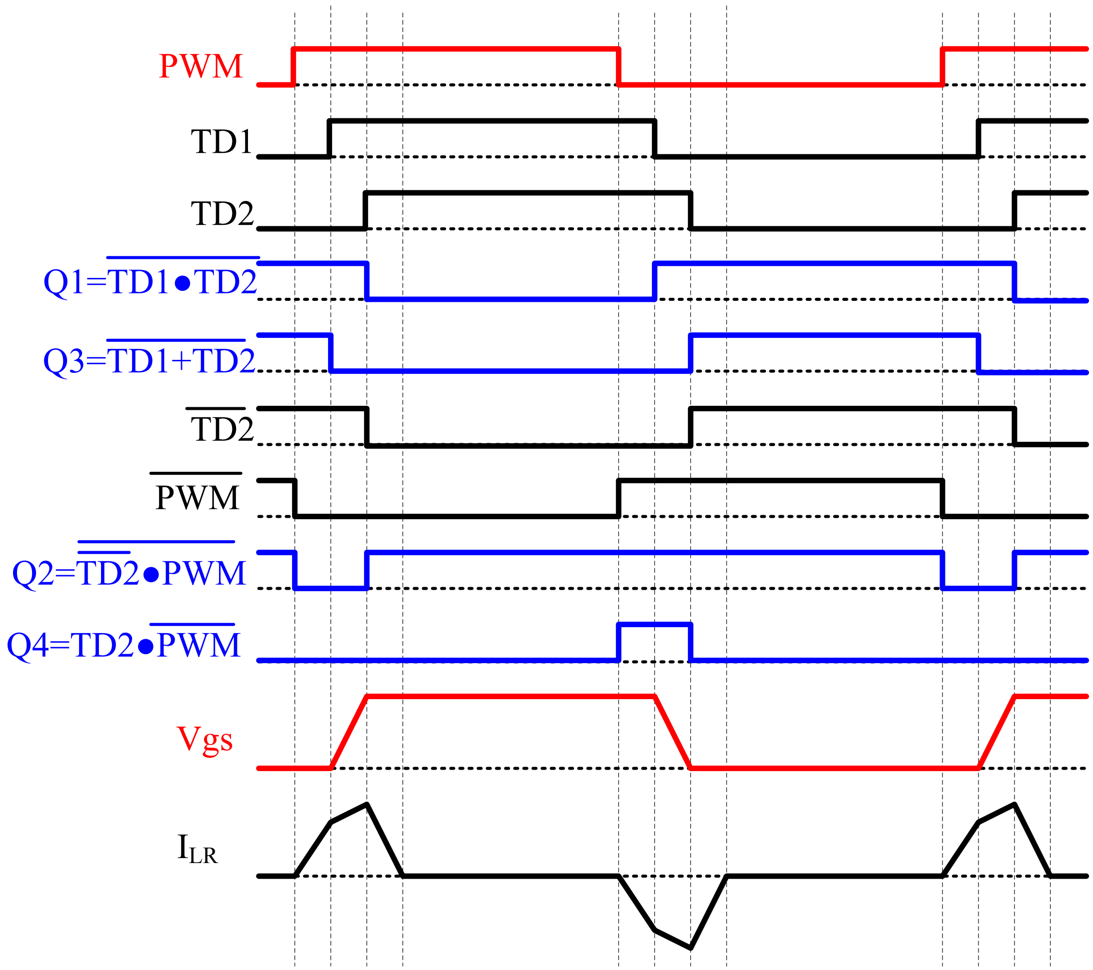
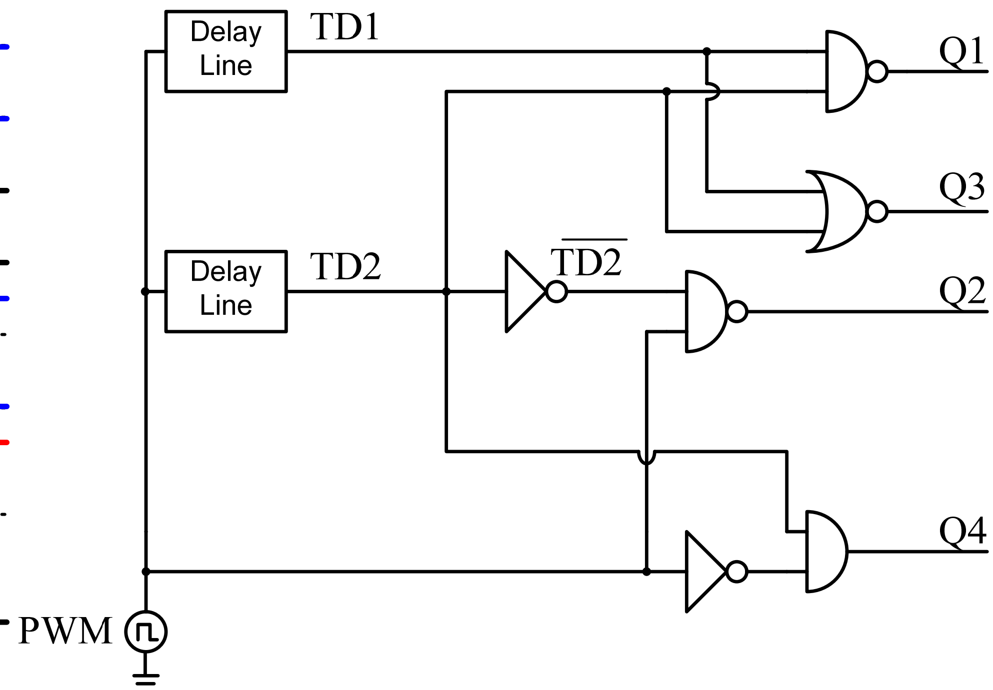
Logic Implementation



6 logic components
2 delay elements



Implementation can be discrete with Fairchild Ultra High Speed (UHS) gates, or using a CPLD, or ultimately integrated into the driver IC

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4. ***Design Procedure***
   1. ***Design steps***
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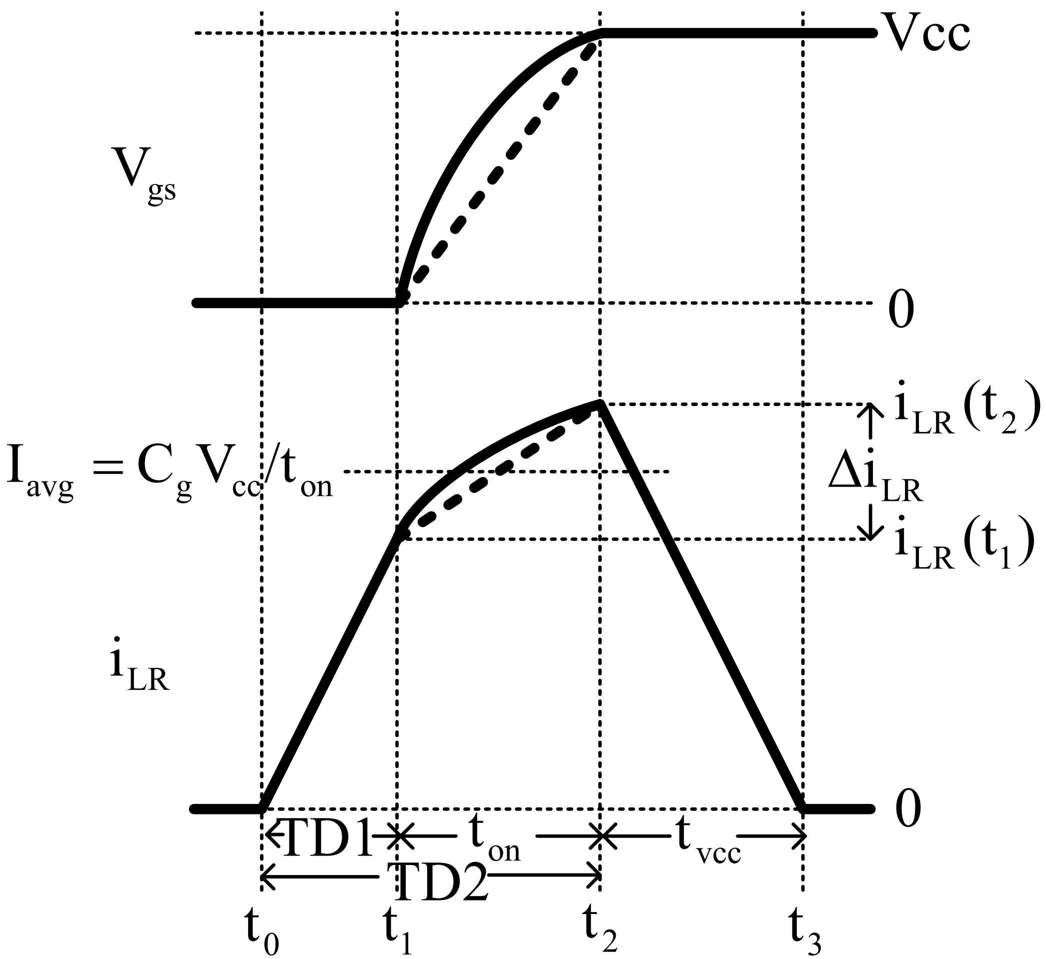
Design Procedure

Needed For Implementation:

1) Resonant Inductance, L_R
2) Delay Time, TD1
3) Delay Time, TD2

Design Procedure



Assumptions:

1) **Rds=Rg=0**
2) **Piecewise linear approximation**

3 Equations:

$$V_{cc} = L_R \frac{i_{LR}(t_1)}{TD1} \qquad \textbf{(a)}$$

$$\Delta i_{LR} = \frac{V_{cc}}{2} \frac{t_{on}}{L_R} \qquad \textbf{(b)}$$

$$i_{LR}(t_1) = \frac{Q_g}{t_{on}} - \frac{\Delta i_{LR}}{2} \qquad \textbf{(c)}$$

Design Procedure

1. **Choose switches;** 20V, 2A pk, low Qg & Rds<250mΩ e.g. Fairchild NDS351AN and FDN352AP
2. **Set ton;** on time
3. **Set TD1;** turn-on pre-charge time
4. **Calculate Δi_{LR};** solving (a)-(c)
5. **Calculate L_R;** using (b)

3 Unknowns in (a)-(c):

Δi_{LR}, L_R, $i_{LR}(t_1)$

$$V_{cc} = L_R \frac{i_{LR}(t_1)}{TD1} \quad \textbf{(a)}$$

$$\Delta i_{LR} = \frac{V_{cc}}{2} \frac{t_{on}}{L_R} \quad \textbf{(b)}$$

$$i_{LR}(t_1) = \frac{Q_g}{t_{on}} - \frac{\Delta i_{LR}}{2} \quad \textbf{(c)}$$

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5. *Loss Analysis*
    1. Equations covered in paper
    2. Loss components
    3. Analysis results
6. Simulation and Experimental Results
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Loss Analysis

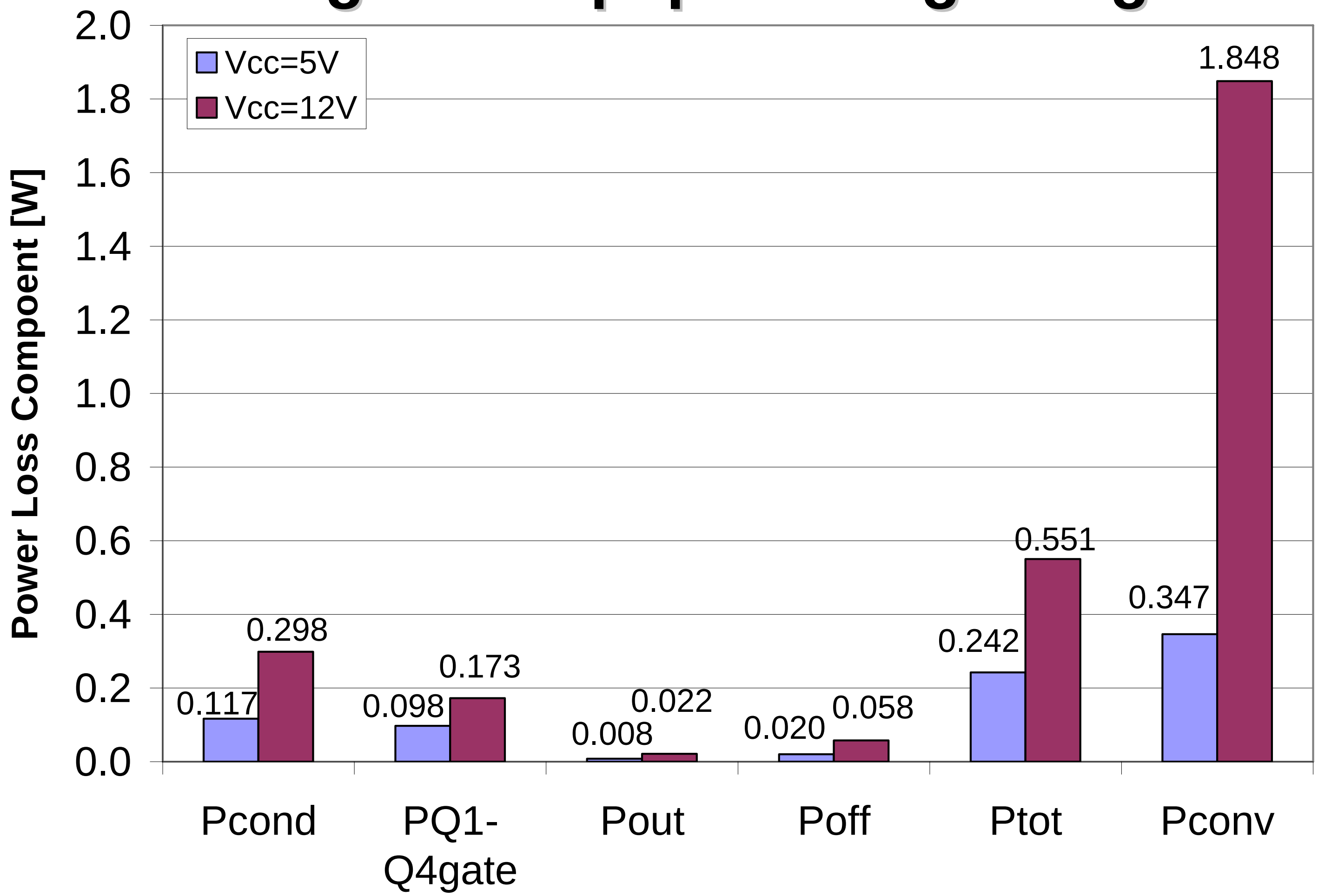
Straightforward Calculations:

1. Conduction loss in Q1-Q4, and Rg during 3 turn-on intervals and 3-turn-off intervals
2. Gate loss in Q1-Q4
3. CV^2 output loss in Q2 and Q4 at turn-on (small)
4. Turn-off loss in Q2 and Q4 (small)
5. Inductor core loss and logic loss (negligible)

Loss Breakdown

Theoretical gate energy recovery at 1MHz

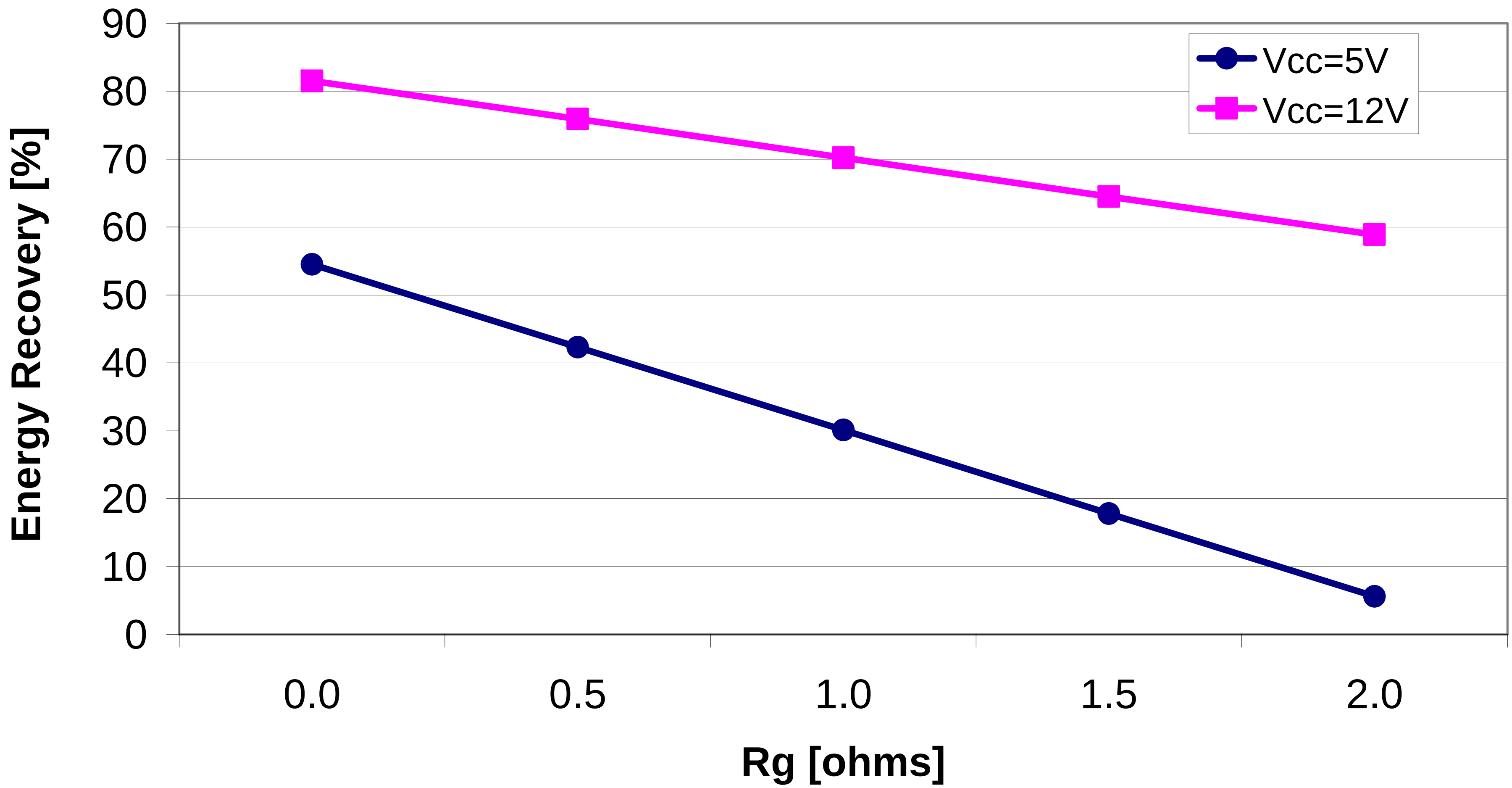
(parameters given in paper using design example)



Impact of Rg

Theoretical gate energy recovery at 1MHz

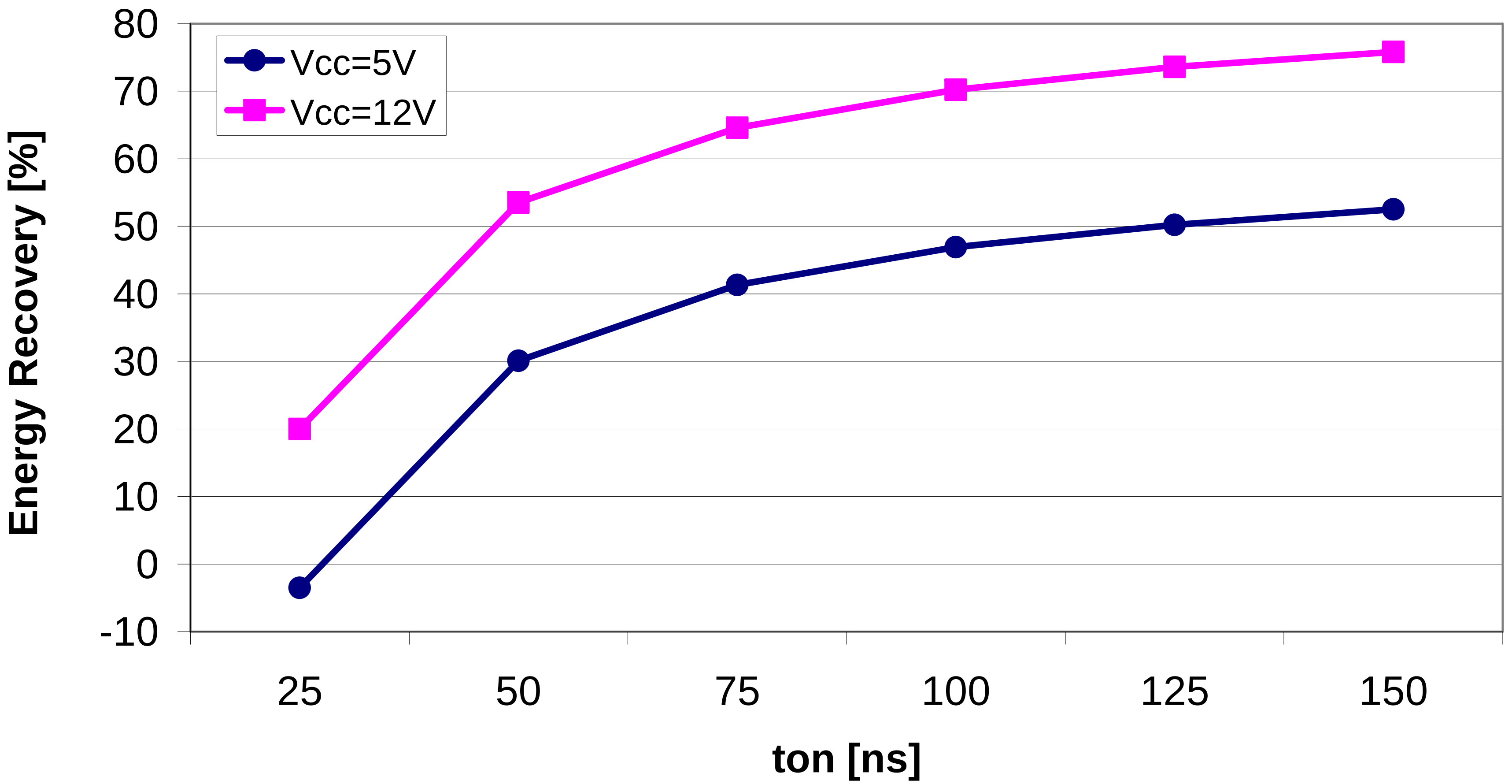
(parameters given in paper)



Recovery vs. Speed Tradeoff

Theoretical gate energy recovery at 1MHz

(parameters given in paper)



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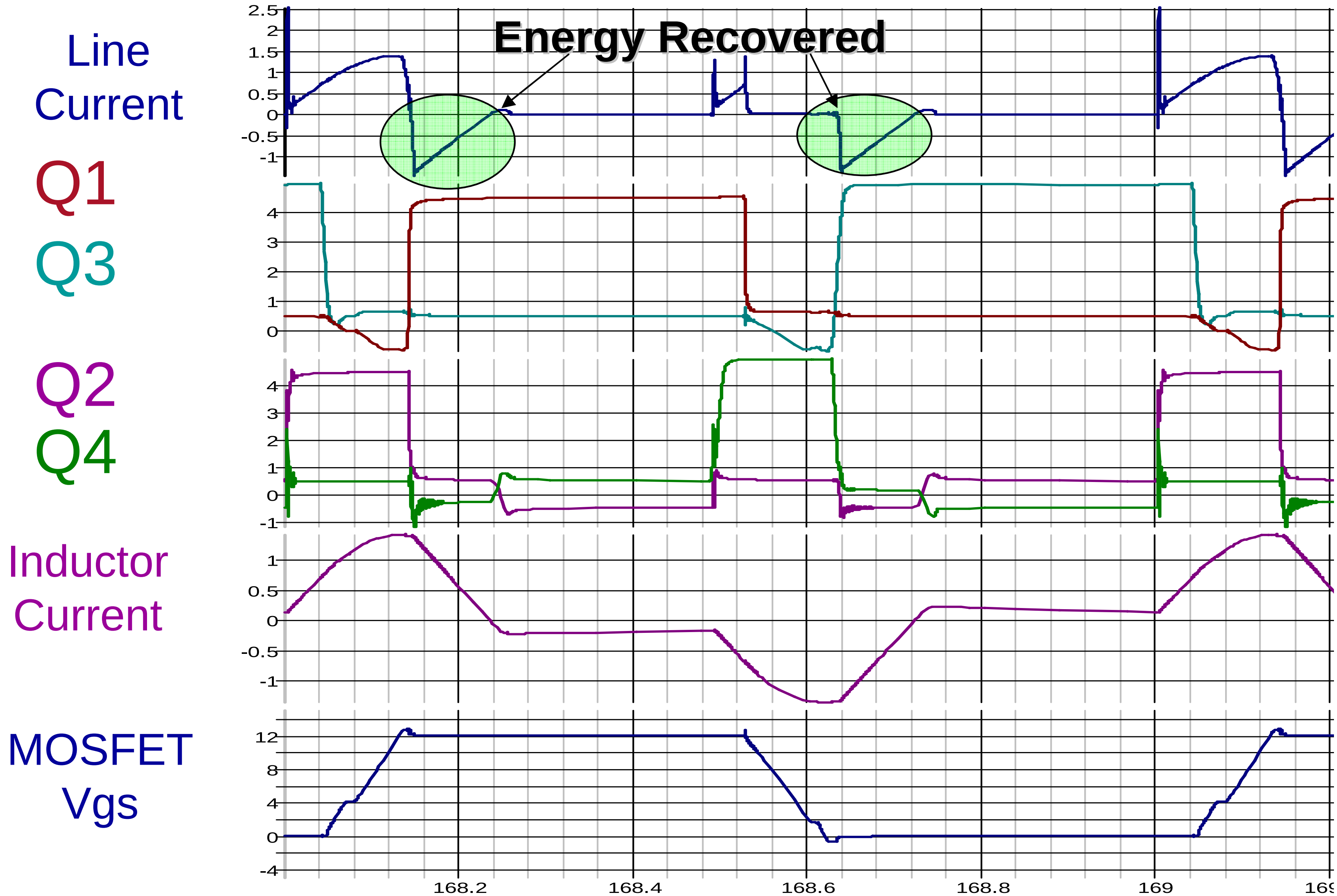
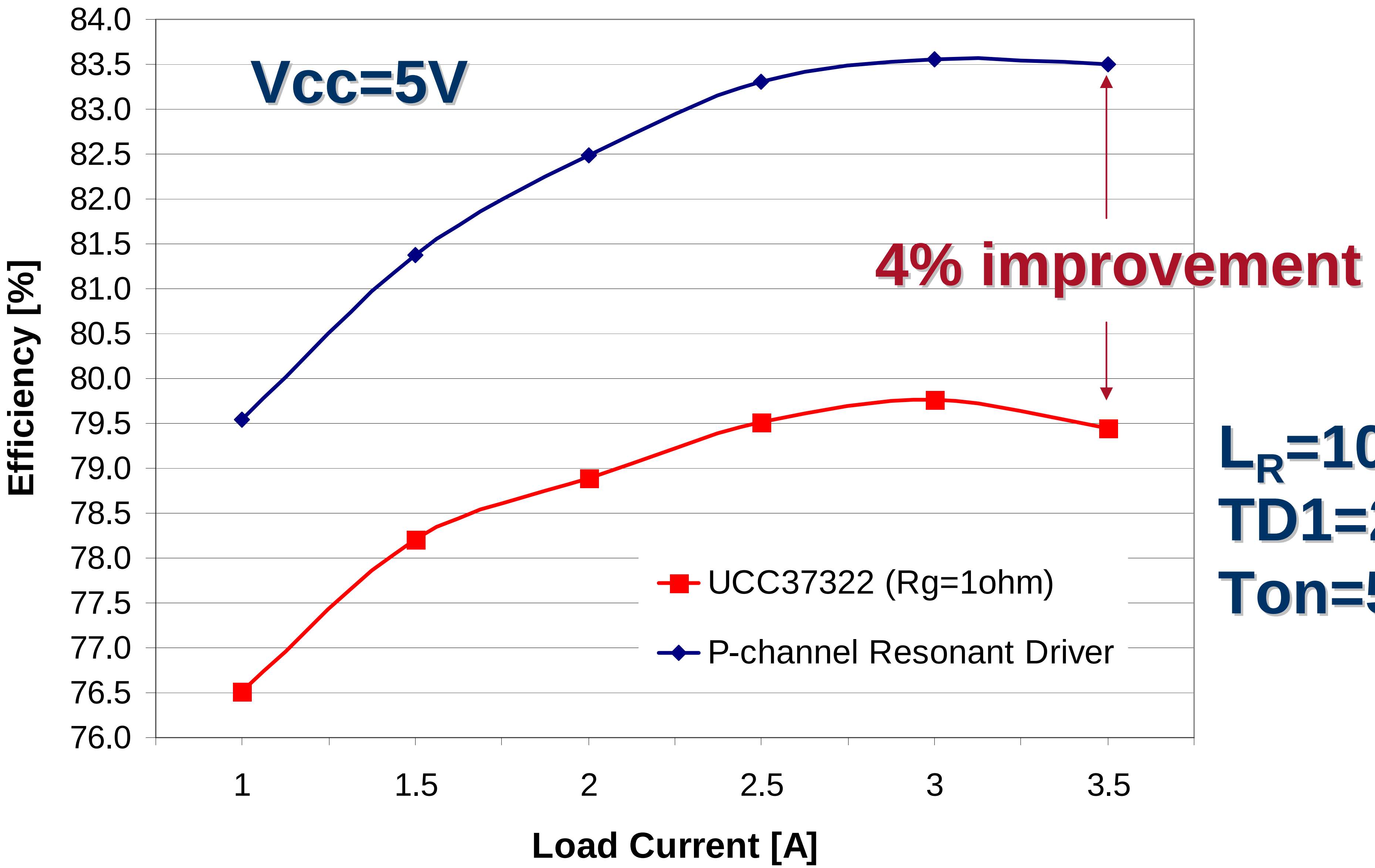
SIMETRIX Simulation Results:

1MHz, IRF6618, L_R=800nH, TD1=40ns, ton=100ns



Boost Experimental Results:

1MHz, IRF6618 (x2), 10TQ035 Diode, Vin=5V, Vo=10V



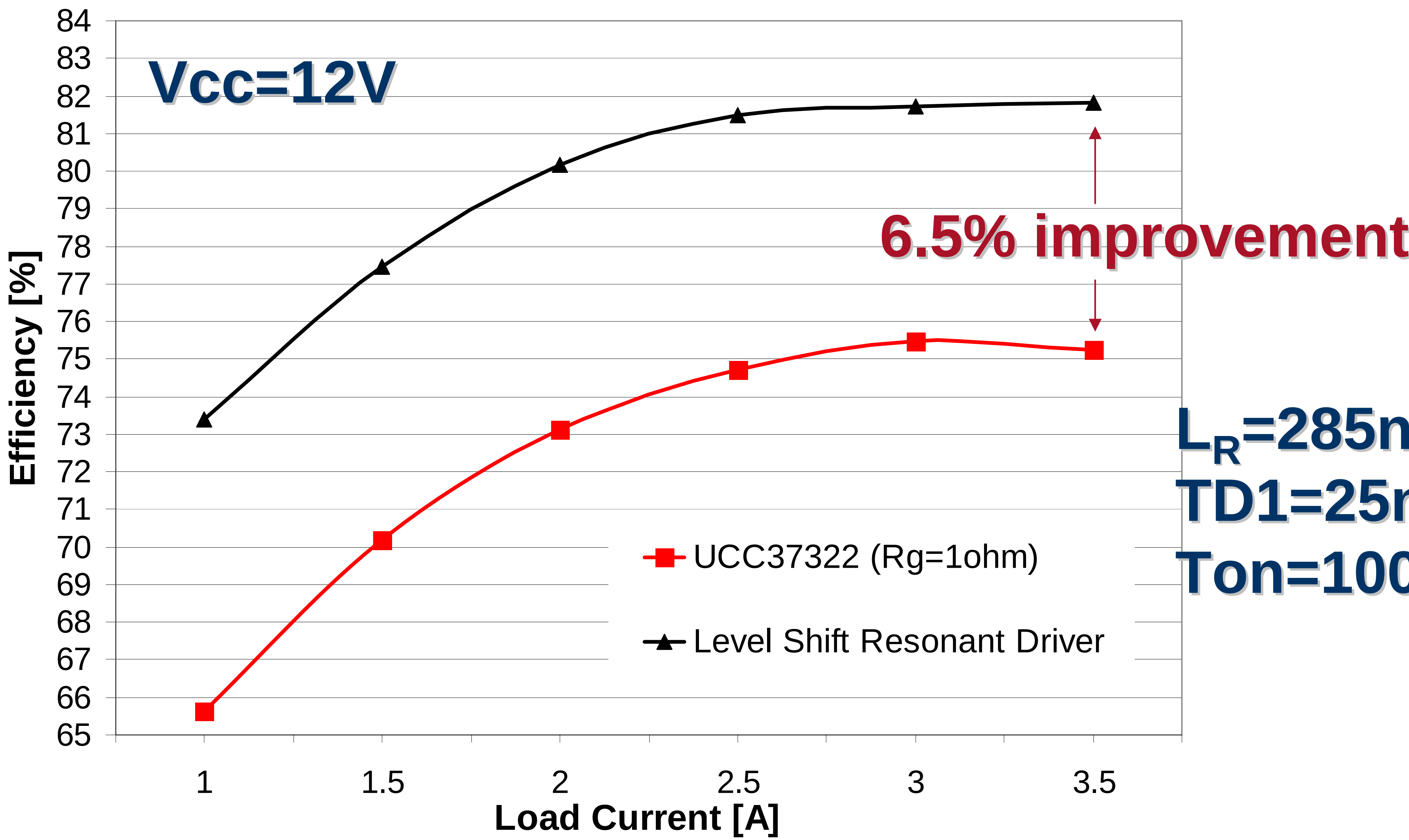
L_R=105nH

TD1=20ns

Ton=55ns

Boost Experimental Results:

1MHz, IRF6618 (x2), 10TQ035, Vin=5V, Vo=10V



L_R=285nH

TD1=25ns

Ton=100ns

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Conclusions

New Resonant Driver Proposed:

- Gate Energy Recovery
- Switching Loss Reduction
- Specific Advantages:
  - Very small inductor (e.g. 100nH @ 1MHz)
  - Peak current independent of duty cycle
  - Low circulating current (discontinuous I_{LR})
  - Quick turn on & off due to inductor pre-charge current during TD1
  - No Cdv/dt false triggering (low impedance)
- 4% efficiency improvement at 5V drive and 6.5% at 12V drive

Thank You For Your Time

Other Resonant Gate Drive Material at:

www.queenspowergroup.com