

# LCLC Converter with Optimal Capacitor Utilization for Hold Up Mode Operation

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**Abstract**—In data center and telecommunication power supplies, the front-end DC-DC stage is required to operate with a wide input voltage range to provide hold up time when AC input fails. Conventional LLC converter serving as the DC-DC stage is not suitable for this requirement, as the normal operation efficiency (at 400 V input) will be penalized once the converter is designed to achieve high peak gain (wide input voltage range). This paper examined the operation of the LCLC converter and revealed that the LCLC converter could be essentially equivalent to a set of LLC converters with different magnetizing inductors that are automatically adjusted for different input voltages. In nominal 400 V input operation, LCLC converter behaves like an LLC converter with large magnetizing inductor, thus the resonant current is small. In hold-up period, when the input voltage reduces, the equivalent magnetizing inductor will reduce together with switching frequency reducing, thus the converter achieves high peak gain. In this paper, a new design methodology is also proposed to achieve optimal utilization of the two resonant capacitors for high power application. To verify the effectiveness of the LCLC converter for hold up operation, comprehensive analysis has been conducted; a detailed step by step design example based on capacitor voltage stress is introduced; an experimental LCLC prototype optimized at 400 V, with input voltage range of 250 V – 400 V and 12 V / 500 W as output has been presented.

**Index Terms**— LLC; multi-element resonant; hold up; high voltage gain; wide input voltage range

## I. INTRODUCTION

THE rapid growth of power consumption in server and data center power systems has been driving the performance improvement of the power supply in recent years [1], [2]. In a server power supply, the front end converter connects the AC grid and outputs 12 V DC (or emerging 48 V). The 12 V DC bus is then connected to the motherboard inside the server to power the point of load converter for CPUs and other parts. Fig. 1 shows the typical structure of the front

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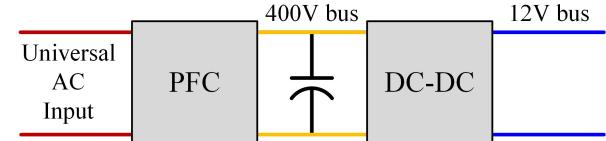


Fig. 1. Structure of the front end converter

end AC to DC converter in the data center power system. A power factor correction (PFC) stage rectifies the AC line into 400 V DC, which is further converted by a DC-DC stage into 12 V [3]–[5].

A critical issue for data center power supply is the hold up problem illustrated in Fig. 2. When the AC line fails, the 400 V bus voltage reduces continuously as the energy storage capacitor discharges. The DC-DC stage converter is then required to operate with a bus voltage that is lower than the designed level (i.e. 400 V), so that a period of time can be saved for the UPS to react. In this way, the load or the end converters will not ‘feel’ the interrupt on the AC side. Usually, the hold-up period lasts for several tens of milliseconds [5]. If the operation range of the DC-DC converter is extended, the capacitor value used on the 400 V bus can be reduced, then the cost will drop and size will reduce significantly. Therefore, improving the operational input voltage range, i.e. the voltage gain of the DC-DC converter, is the solution to the hold-up issue.

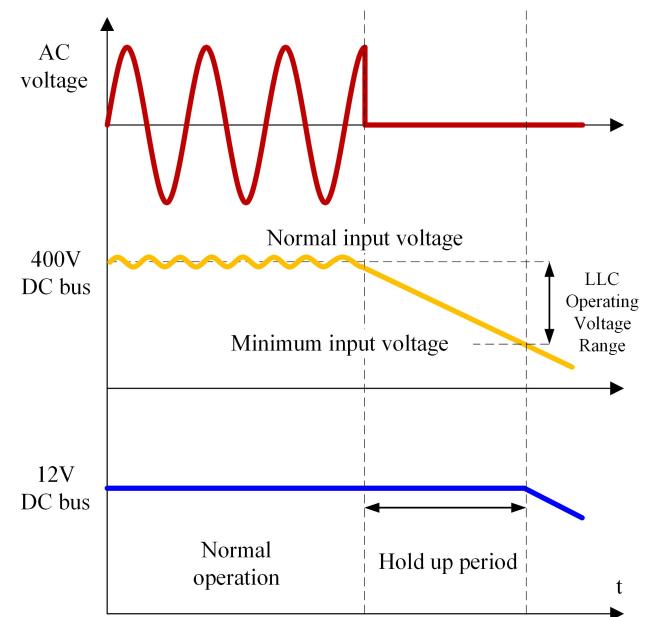


Fig. 2. Hold-up problem process

LLC resonant converter is widely used as the DC-DC stage due to its high efficiency as a result of the inherent zero voltage switching (ZVS) for the primary MOSFETs and zero current switching (ZCS) for the secondary rectifiers [3]–[7]. However, designing LLC converter with hold up ability could compromise its high performance in normal operation. It is widely acknowledged that if the LLC converter is designed to achieve high voltage gain, a small magnetizing inductor value should be used. Such design could lead to severe conduction loss in the primary side for normal operation at 400 V input [8], [9]. Therefore, to solve the hold-up problem, LLC converter should be improved to meet the following requirements:

- (1) to achieve high efficiency for the nominal 400 V input operation;
- (2) to increase the operational input voltage range.

To achieve high efficiency at 400 V operation, from the point view of parameter design, the transformer turns-ratio needs to be properly designed to ensure that the converter operates at resonant frequency for 400 V input. Besides, the magnetizing inductor value should be optimized to reduce the current stress in the resonant tank as much as possible while maintaining ZVS for the half bridge (HB) MOSFETs. At last, for 12 V output applications, on the secondary side, synchronous rectifiers (SR) should be used instead of diode rectifiers, as the forward voltage drop of diodes would be a deal breaker of the whole efficiency [10]–[12].

To meet the hold up time requirement, quite a few methods have been proposed. Before the age of LLC converters, a baby boost converter is used for asymmetrical half bridge converters to achieve hold up operation [13]. Similarly, a baby boost converter can reduce the burden of the LLC stage, although LLC converters are step-up converters with hold up ability by its own nature. However, the additional power stage will reduce the efficiency at nominal 400 V operation. Besides, the two stage configuration is complicated, and, consequently, costly.

Another method solves the hold up problem by utilizing auxiliary windings on the secondary side of the main transformer for both PWM converter [14], and LLC converters [15]. Generally speaking, as long as the input voltage reduces below the designed range, the switch-controlled auxiliary windings will take over the secondary side power transfer. Increased transformer turns-ratio helps achieve higher output-to-input voltage gain during the hold-up period. The independent circuit designs between nominal 400 V operation and hold-up mode operation can maintain 400 V input operation uninfluenced. However, usually the main transformer is the most bulky and lossy part of a converter, thus adding extra windings makes it even more difficult to optimize the transformer from both efficiency and power density improvement point of view.

By driving the half-bridge MOSFETs with asymmetric pulse-width modulation (APWM) rather than conventional frequency modulation (FM), LLC converter can improve voltage gain without any additional components [16]. This method, however, suffers from limited peak gain enhancement. Besides, once the resonant tank is designed, the maximum gain that APWM control could achieve is also determined. Thus, in order to satisfy the voltage gain

requirement, the resonant parameters design might not be optimized for 400 V operation.

A critical insight was revealed in [17] that if the resonant tank can be charged with more energy during one switching cycle, LLC converter achieves higher gain. To charge the resonant tank more, the secondary windings are short circuit for a certain period of time in every switching cycle. The downside of this method is that quite a few components need to be added in the power train on the secondary side, which causes size increasing and efficiency reducing.

Based on [17], a few improving methods propose to adopt either Boost PWM discontinuous current mode (DCM) control [18] or phase shift control on LLC topology [19], [20]. The common principle of these methods is that, in each switching cycle, the resonant tank will be short circuit on either primary side or secondary side by auxiliary switches for a period of time, so that the resonant inductor can be energized more quickly, hence store and transfer more power. The nominal 400 V efficiency remains uninfluenced as compared to a conventional LLC optimized for 400 V input voltage. However, during hold-up period, the converter is operating at DCM, thus both primary and secondary components have significantly higher current stress as compared to 400 V operation, which potentially calls for overdesign in terms of component selection. Besides, these methods use full-bridge rectifier with diodes, thus are not suitable in low output voltage applications.

In [21], [22], the authors have proposed LLC converter with auxiliary switch on the primary side to reduce the current stresses, and solves the SR problem. The potential drawback is that the auxiliary switch achieves no soft switching, which limits the maximum switching frequency.

Four-element resonant topologies have been studied and reported to achieve better performance than LLC converter in various aspects, e.g. the startup process, current limiting ability and load regulation. In this paper, LCLC resonant topologies will be revisited from increasing the voltage gain point of view [23]. In 400 V normal operation, the LCLC converter is equivalent to an LLC converter with a large magnetizing inductor, so that the magnetizing current that is circulating on the primary side will be low, and 400 V efficiency is high. For hold-up operation, when the input voltage reduces, the magnetizing inductor reduces along with the switching frequency, thus the output-to-input voltage gain increases, and the operational input voltage range is extended. Unlike the aforementioned LLC converter with PWM control, LCLC converter can be implemented with existing controller that is designed for conventional LLC converter, which reduces the overall developing time and cost. Besides, LCLC converter works with SR, thus it is beneficial for low output voltage applications. Moreover, LCLC converter utilizes pure passive components, avoiding cumbersome sensing and sudden operation changes, thus it is specifically suitable for high power applications which requires high reliability.

This paper is organized as follows: Section II describes the operation principle of LCLC converter from DC voltage gain point of view; Section III discusses a design methodology based on capacitor voltage stresses; Section IV demonstrates the experimental results; and Section V concludes the paper.

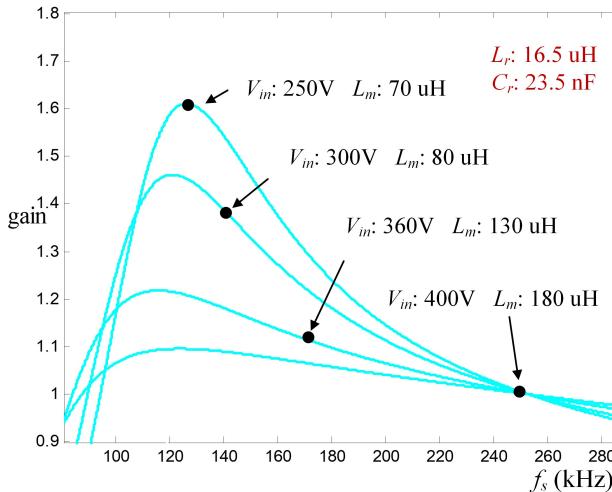


Fig. 3. Desired LLC with different  $L_m$  for hold up operation ( $L_r = 16.5 \mu\text{H}$ ,  $C_r = 23.5 \text{ nF}$ )

## II. PRINCIPLE ANALYSIS OF LCLC CONVERTER FROM DC GAIN POINT OF VIEW

The discussion in this section can be separated in three parts: part A will discuss the desired performance of the LLC converter in hold up applications; part B will discuss the operation of the LCLC converter, and prove that the LCLC converter meet the desired performance; part C will discuss the differences in magnetics component design as compared to LLC converter.

### A. Desired performance for hold up operation and LLC limitation

In data center applications, high voltage gain is required to satisfy the wide input voltage range and/or hold up requirements. The limitation of conventional LLC converter is that it can only be optimized for one specific input voltage level or a narrow input voltage range near the resonant point. In the optimized parameters for normal 400 V operation, magnetizing inductor value is usually large, so the losses in the primary-side switches and the magnetic components are low. On the other hand, to achieve high voltage gain, the magnetizing inductor value should be small. Then, enough current can be generated to compensate the voltage difference between the source and sink of the resonant tank. This is the well-known contradiction between high voltage gain and high efficiency performances in terms of parameter design for LLC converter.

The limitation described above also implies the desired characteristic of LLC converter in the hold up application – a magnetizing inductor  $L_m$  that changes for different input voltages. Specifically, for normal input at 400 V, the  $L_m$  should be of high value; and for low input voltages, the  $L_m$  should be of low value.

According to frequency modulation, the switching frequency is changing along with the input voltage in the same direction. Then, the desired characteristic of the magnetizing inductor could be interpreted as changing together with the switching frequency in the same direction. In other words, the large  $L_m$  at high switching frequency, and vice versa.

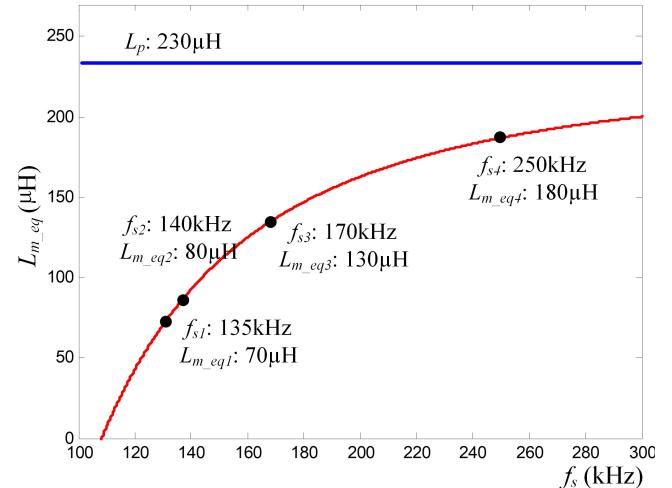


Fig. 4. Equivalent  $L_{m\_eq}$  changing with  $f_s$  ( $L_p = 230 \mu\text{H}$ ,  $C_p = 9.4 \text{ nF}$ )

Fig. 3 shows the desired LLC performance for hold up operation with different  $L_m$  and fixed  $L_r$  and  $C_r$ . The  $L_r$  of 16.5  $\mu\text{H}$  and  $C_r$  of 23.5  $\text{nF}$  are from Table II for illustration purposes. When the input voltage is at 400 V, the switching frequency is at resonant point of 250 kHz, and the magnetizing inductor is high at 180  $\mu\text{H}$ . As the input voltage reduces to 250 V, the switching frequency reduces to 130 kHz. Then the magnetizing inductor also reduces (to 70  $\mu\text{H}$  in this case), so the voltage gain is increased from 1.1 to 1.6, which in turn accommodates the reduced input voltage.

This desired auto-changing magnetizing inductor  $L_m$  can be implemented by a pair of series connected inductor  $L_p$  and capacitor  $C_p$  on the parallel branch of the resonant tank. From the point view of impedance, a capacitor behaves like a negative inductor whose value changes with frequency in a reverse quadratic manner. For given  $L_p$  and  $C_p$  values, the equivalent magnetizing inductor  $L_{m\_eq}$  at different switching frequency can be calculated by (1).

$$L_{m\_eq}(f_s) = L_p - \frac{1}{(2\pi f_s)^2 C_p} \quad (1)$$

From (1), it could be concluded that the performance of the  $L_{m\_eq}$  is exactly as the desired – large at high frequency and small at low frequency, as long as the total impedance of  $L_p$  and  $C_p$  remain as inductive. Fig. 4 shows the  $L_{m\_eq}$  value changing with switching frequency with  $L_p$  of 230  $\mu\text{H}$  and  $C_p$  of 9.4  $\text{nF}$  (from TABLE II).

### B. LCLC converter operation principle

The LCLC converter topology is shown in Fig. 5, in which  $L_r$  and  $C_r$  are the series resonant inductor and capacitor, and  $L_p$  and  $C_p$  are parallel inductor and capacitor.  $V_{in}$  is the input DC voltage,  $V_o$  is the output DC voltage, and  $n$  is the transformer turns ratio.

As compared with LLC converter,  $C_p$  is added on the parallel branch. The value of  $C_p$  should be selected in such way that the resonant frequency of  $L_p$  and  $C_p$  is lower than the entire switching frequency range. Then the impedance of  $L_p$  and  $C_p$  branch will always be inductive, and the LCLC converter can always be equivalent to LLC converters at different switching frequencies (input voltages). For normal 400 V operation at

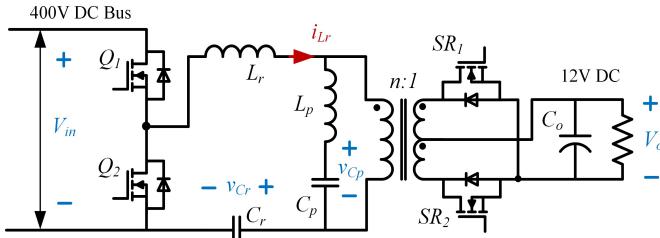


Fig. 5. LCLC converter topology with center tapped transformer and SR

high switching frequency near the resonant point, the equivalent  $L_m$  is large, and high efficiency could be achieved. With switching frequency reducing, the equivalent  $L_m$  will reduce. As a result, LCLC converter achieves higher gain when input voltage is low.

The conventional FHA method is still valid for analyzing the LCLC converter and calculate the voltage gain. Fig. 6 shows the FHA model, in which  $v_{in}$  is the fundamental component of the input square-wave AC voltage seen by the resonant tank, and the RMS value of  $v_{in}$  equals to  $\frac{2\sqrt{2}}{\pi} V_{in}$ .  $v_o$  is the reflected AC output voltage, and the RMS value of  $v_o$  is  $\frac{2\sqrt{2}}{\pi} n V_o$ .  $R_{ac}$  is the equivalent load resistor in the resonant tank, and there is  $R_{ac} = \frac{8n^2}{\pi^2} \cdot \frac{V_o^2}{P_o}$ .

By the analyzing the FHA circuit of the LCLC converter in frequency domain, the voltage gain can be then calculated with  $G = v_{in} / v_o$ . Alternatively, the voltage gain can be calculated with the conventional LLC voltage gain equation as shown in (2) by replacing the variable  $L_m$  with the equivalent  $L_{m\_eq}$  that is calculated by (1) at different switching frequencies. In (2),  $Q$  is the quality factor defined as  $Q = \sqrt{L_r / C_r} / R_{ac}$ .

$$G = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_{m\_eq}} - \frac{L_r}{L_{m\_eq}} \left(\frac{f_r}{f_s}\right)^2\right)^2 + \left(Q \left(\frac{f_s}{f_r} - \frac{f_r}{f_s}\right)\right)^2}} \quad (2)$$

Fig. 7 shows a typical gain curve versus switching frequency of LCLC converter. Conventional frequency modulation can still be used. The parallel resonant frequency  $f_p$  of  $L_p$  and  $C_p$  should be designed lower than the series resonant frequency  $f_r$ , and the operation range should be limited between resonant point  $f_r$  and peak gain point  $f_{min}$ , such that the voltage gain is monotonically changing with switching frequency, and ZVS for HB FETs and ZCS for SR FETs can be achieved. It should be noted that the voltage gain is zero at the parallel resonant frequency  $f_p$ , as the transformer primary side is short circuit.

Fig. 8 shows that the LCLC gain curve (in solid red) fits the desired gain curves (in light blue) of LLC converters with different  $L_m$  values. The parameters are from TABLE II.

At nominal of 400 V, the converter operates at the series resonant frequency 250 kHz. The corresponding gain is unity. The equivalent  $L_{m\_eq}$  is 180  $\mu$ H. As compared to conventional LLC converter with  $L_m$  of 70  $\mu$ H (for the same gain

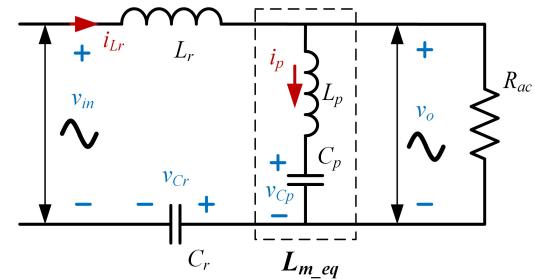


Fig. 6. First Harmonic Approximation of LCLC converter

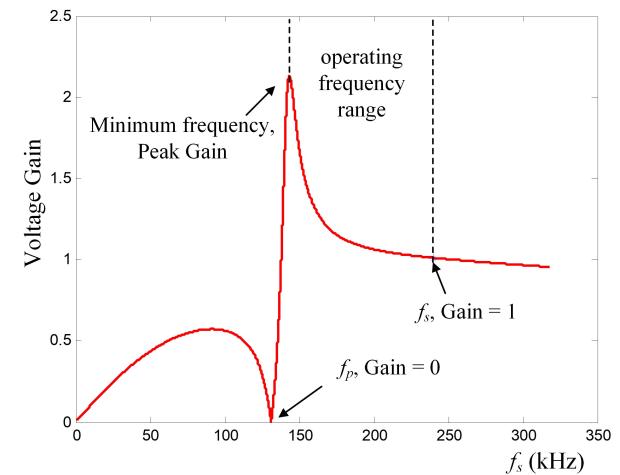


Fig. 7. Typical gain curve of LCLC converter

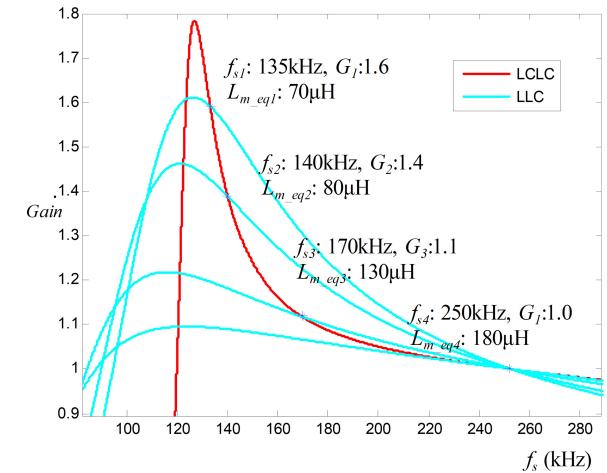


Fig. 8. LCLC gain curve fits the LLC gain curves at specific operating points ( $L_r = 16.5 \mu$ H,  $C_r = 23.5 \text{nF}$ ,  $L_p = 230 \mu$ H,  $C_p = 9.4 \text{nF}$ )

performance), this more than 2.5 times larger magnetizing inductor will significantly reduce the current in the resonant tank, so the conduction and switching loss in the MOSFETs as well as the core loss and copper loss in the magnetic components would be significantly reduced.

The equivalent  $L_m$  will reduce together with the switching frequency if the input voltage drops. At 135 kHz, the equivalent  $L_m$  is 70  $\mu$ H. With this set of parameters, peak voltage gain is increased to more than 1.6 from 1.1 with  $L_m$  of 180  $\mu$ H, so that the designed minimum input voltage could be as low as 250 V.

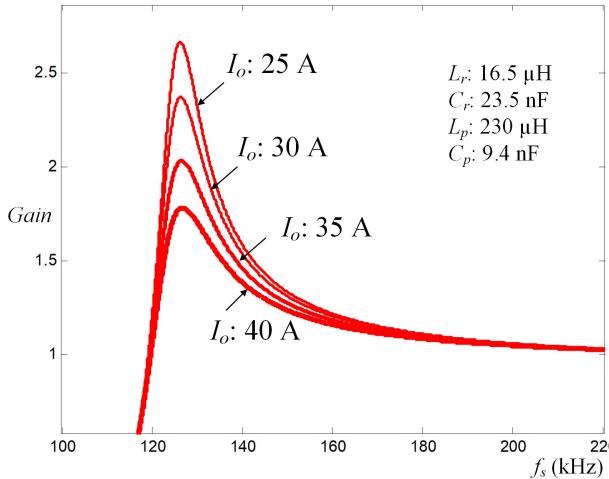


Fig. 9. LCLC gain curve at different load condition

Fig. 9 shows the LCLC converter voltage gain changing with load current. As can be observed, the behavior is very similar to the conventional LLC converter. A noticeable difference is that while LLC converter has lower peak gain frequency for lighter load, LCLC converters' peak gain frequencies converge to one point for different loads. This could be attributed to the parallel resonant frequency of  $L_p$  and  $C_p$ . This characteristic will be beneficial for some applications that require the converter to operate as current source, i.e. always operate at the peak gain point.

In terms of operation modes, LCLC converter is same as LLC converters, because LCLC converter can be equivalent to LLC converters over the entire operation range. In each switching cycle, the circuit behaviors during the switch conducting period and dead time are exactly same for LCLC converter and its equivalent LLC converters. Besides, the switching logic and the control are also the same. Thus, existing controller for LLC converter can be directly used.

Although LCLC converter can be understood and designed from the equivalent LLC point of view, special attention should be paid to the parallel capacitor  $C_p$ . In Fig. 6, it is observed that the parallel branch of  $L_p$  and  $C_p$  has fixed voltage stress of  $v_o$ . As the total impedance is inductive (as  $L_{m\_eq}$ ), at given switching frequency, the parallel branch can be viewed as a current source, and the peak value  $i_{p\_pk}$  can be determined by (3), in which  $L_{m\_eq}$  is given by (1).

$$i_{p\_pk} = \frac{v_o}{2\pi f_s L_{m\_eq}} = \frac{4}{\pi} n V_o \frac{2\pi f_s C_p}{(2\pi f_s)^2 L_p C_p - 1} \quad (3)$$

Then, the voltage stress on  $C_p$  can be calculated by (4).

$$v_{Cp\_pk} = i_{p\_pk} \frac{1}{2\pi f_s C_p} = \frac{4}{\pi} n V_o \frac{1}{(2\pi f_s)^2 L_p C_p - 1} \quad (4)$$

Fig. 10 shows the voltage stresses on different capacitor value of  $C_p$  changing with switching frequency. At low input voltage region, i.e. low switching frequency, the voltage stress increases sharply, because both the current stress and the capacitor impedance increase with the switching frequency reducing, and their product grows in a reverse quadratic relationship. Thus, during the design, the peak voltage stress at minimum input voltage should be carefully designed.

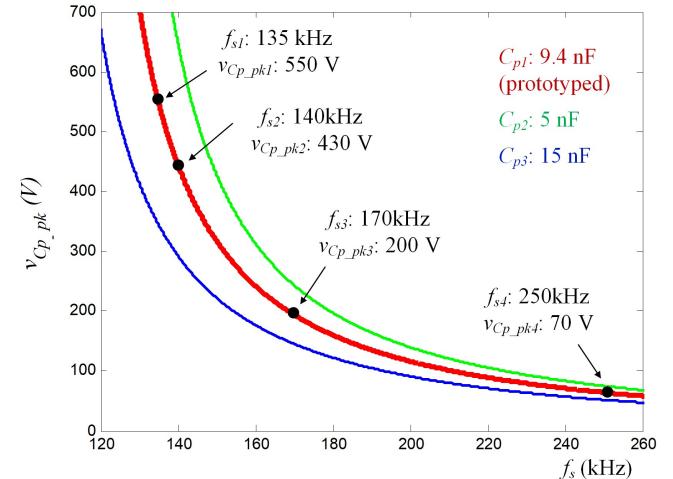


Fig. 10. Voltage stress on  $C_p$  at different switching frequencies

In Fig. 10, the voltage stress of three capacitor values are also compared. The red line shows the calculated peak voltage stress for the parameter design in TABLE II. All three designs have same peak voltage gain, i.e. same  $L_{m\_eq}$  of  $70 \mu\text{H}$  at minimum frequency of 135 kHz. It has been analyzed that larger  $L_p$  is preferred to reduce circulation loss. To achieve so, smaller  $C_p$  should be used. However, it is observed in Fig. 10 that smaller  $C_p$  will have larger peak voltage stress, which could limit the choice and require trade-off in practical designs. More details will be revealed in a Section III.

#### C. $L_p$ and $C_p$ implementation and magnetics design considerations

In conventional LLC converters, the  $L_p$  is usually afforded by the magnetizing inductor  $L_m$  of the transformer. Such design could reduce the size and weight of the total magnetic components to the minimum. In LCLC converter, the  $L_p$  and  $C_p$  should be external. As shown in the prototype picture in Fig. 13, the total space consumed by the external  $L_p$  and  $C_p$  is  $3.2 \text{ cm} * 3 \text{ cm} * 5 \text{ cm}$ , which is less than 10% of the total volume measuring as  $10 \text{ cm} * 10 \text{ cm} * 5 \text{ cm}$ . This size increase is believed affordable.

For LLC used in low power applications, e.g. below 500 W, magnetic integration is usually a preferred choice. However, if the power is higher, magnetic integration is not always desired. It is already an accepted practice in the industry to use separate cores when the efficiency performance becomes the primary target. The reason is that the conduction loss takes an overwhelming part, while the core loss is relatively minor in high current application. By employing an external  $L_p$ , the transformer primary current is separated for two conductors, thus the primary conduction loss will be reduced. In most cases, the conduction loss reduction will outnumber the additional core loss of  $L_p$ . Thus, an external  $L_p$  is not necessarily unprofitable. Besides, since a separate  $L_p$  is used, the air gap on the transformer can be removed. This generates no additional core loss, but removes the fringing loss caused by the air gap.

Therefore, LCLC converter trades for higher performance with affordable size compromise. With the external  $L_p$ , an ungapped transformer can be used in the LCLC converter, which is expected to be of smaller size and/or higher performance over the conventional LLC transformers. This

advantage is even more competitive for planar transformers, which suffer from limited window size and generally heavier conduction loss.

### III. LCLC CONVERTER DESIGN METHODOLOGY BASED ON CAPACITOR VOLTAGE STRESS

Extensive design methods have been proposed for LLC converter in different applications [24]–[30]. These optimal design methods place no limit on capacitor voltage stress, which in practice may bring about iterative capacitor calibrations, especially in high power applications. It has been observed that the AC voltage stress on the resonant capacitor can be as high as 1 kV in 500 W and above applications. High voltage stress on the capacitor not only increases the cost, but also reduces the reliability. Especially when  $C_p$  is added, it is essential to balance the voltage stresses on both capacitors to achieve optimal capacitor utilization. Based on this criterion, a design methodology based on the capacitor voltage stress is proposed in this paper. The design method considers primarily two equivalent LLC converters – equivalent LLC design for minimum input voltage (250 V) based on voltage gain requirement; and equivalent LLC design for normal operation (400 V) evaluated from the efficiency point of view. The design logic is described below and the design flow chart is shown in Fig. 11.

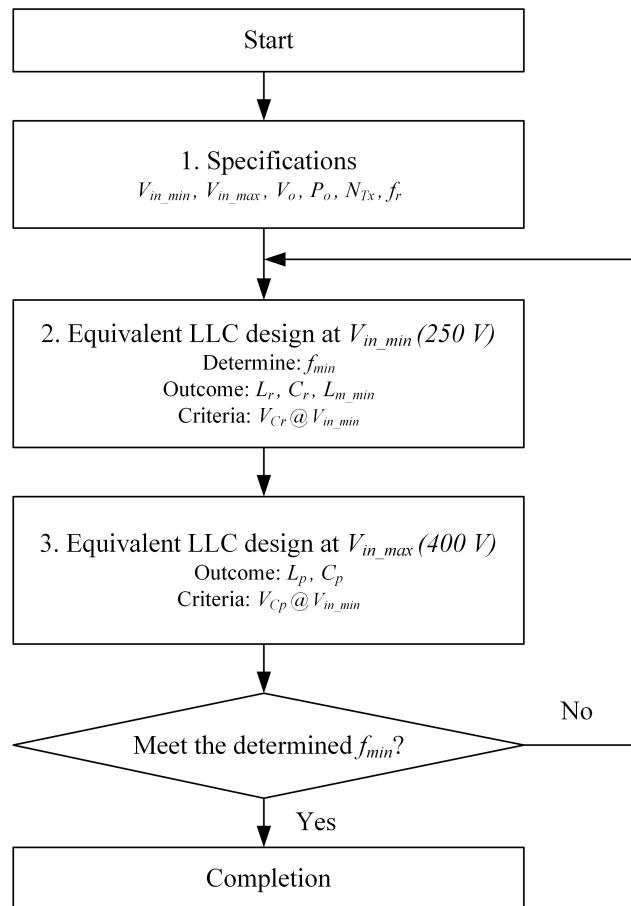


Fig. 11. Design flow chart of proposed design method based on capacitor voltage stress

*1. Specification.* In this step, the input voltage range should be specified – including the maximum input voltage  $V_{in\_max}$ , at which the converter normally operates, and minimum input voltage  $V_{in\_min}$  during the hold up process. The transformer turns-ratio  $n$  should be selected based on the  $V_{in\_max}$  and the rated output voltage  $V_o$ , so that the converter will operate at the specified resonant frequency  $f_r$  for normal operation. The relationship can be determined by  $n = V_{in\_max} / (2V_o)$  for half bridge in this case.

*2. Equivalent LLC design for  $V_{in\_min}$  (250 V).* According to frequency modulation, the switching frequency for minimum input voltage  $V_{in\_min}$  is the minimum frequency  $f_{min}$ , at which the converter will achieve the peak voltage gain. In this design procedure, the selection of  $f_{min}$  will require the designer's engineering judgement. Then the value of minimum  $C_r$ , and corresponding  $L_r$  and equivalent magnetizing inductor  $L_{m\_min}$  for  $V_{in\_min}$  could be determined based on the  $C_r$  voltage stress.

*3. Equivalent LLC design for  $V_{in\_max}$  (400 V).* The  $L_r$  value and  $C_r$  value should remain the same as that in the last step. Equivalent  $L_m$  should be increased for  $V_{in\_max}$  so as to reduce the current stress in the resonant tank. The maximum equivalent  $L_{m\_max}$  is limited by the  $C_p$  voltage stress.

To help demonstrate the design methodology, a detailed design example is given in the following part.

#### A. Specification

The design is based on a 250 V-400 V input, 12 V/500 W output application. Theoretically, the turns-ratio of the transformer should be 16.7:1 ( $n = V_{in\_max} / (2V_o) = 400 \text{ V} / (2 * 12 \text{ V})$ ) to ensure that the normal operation at 400 V is at the resonant point. In real world, the turns-ratio is chosen as 17:1, so that the voltage gain is slightly above unity, and the secondary rectifiers will have ZCS operation.

The series resonant frequency  $f_r$  should be chosen based on the designer's engineering judgement to optimize the efficiency at 400 V normal operation. The consideration of  $f_r$  selection should include but not limited to the magnetic components design and fabrication, thermal design, and trade-off of the conduction loss and switching loss in the switching device, and so on. In this design example, the series resonant frequency is chosen at 250 kHz according to the experience by the authors concerning the above-mentioned aspects.

#### B. Selection of minimum switching frequency for 250 V

LCLC converter follows the same frequency modulation as conventional LLC converter, i.e., switching frequency reduces along with input voltage reducing. Thus, the switching frequency at 250 V operation should be the minimum switching frequency  $f_{min}$  for the entire input voltage range 250 V-400 V. For aggressive designs, the  $f_{min}$  could be chosen at the ZVS and ZCS boundary where the resonant tank critically achieves the peak voltage gain (1.6 in this case). In this scenario, the resonant tank will have the maximum current stress, and the series capacitor  $C_r$  will have the maximum voltage stress. In practical designs, a reasonable margin should be considered for the input voltage, so that the entire range will have ZVS operation.

The selection of the minimum switching frequency  $f_{min}$  should follow similar strategy as the selection of the resonant frequency  $f_r$ , especially the magnetic component design and

EMI design should be primarily considered. A widely acknowledged empirical value of  $f_{min}$  is between 0.5 to 0.8 times  $f_r$ .

In this design example, 150 kHz as minimum switching frequency is selected as the starting point for 250 V input. The actual  $f_{min}$  might have some deviation from this 150 kHz but can be compensated by one or two iterations. Voltage margin is not considered in this step, because FHA tends to underestimate the voltage gain, thus some margin is automatically left there.

#### C. $C_r$ selection based on voltage stress at $f_{min}$

For 250 V operation, at the selected of 150 kHz, the converter achieves peak voltage gain, and the resonant tank is pure resistive. Thus, the current on the primary side is critically in phase with the input square-wave voltage. That is to say, in half switching cycle, the resonant current will charge the resonant capacitor  $C_r$  from its minimum value to its maximum value [31]–[33]. The charging process is illustrated in Fig. 12.

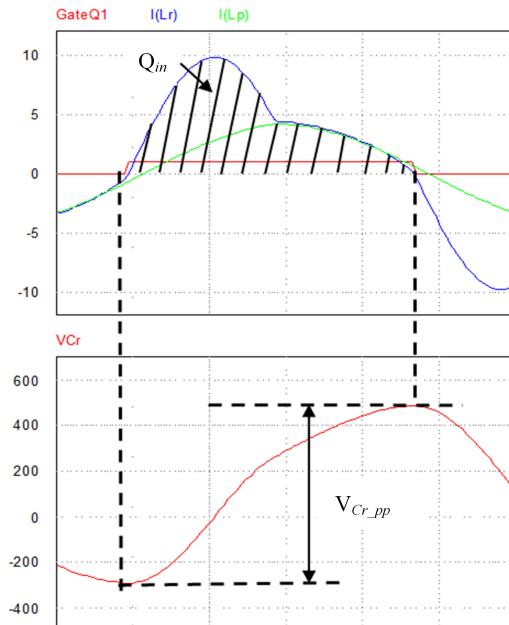


Fig. 12.  $C_r$  charging waveform at minimum frequency

Assuming 100% efficiency, the total charge  $Q_{in}$  in one switching cycle could be calculated by (5), in which  $V_{in\_min}$  is the minimum input voltage;  $P_o$  is the average output power;  $f_{min}$  is the minimum switching frequency.

$$E_{cycle} = V_{in\_min} Q_{in} = \frac{P_o}{f_{min}} \quad (5)$$

For a given capacitor value  $C_r$ , the voltage stress  $V_{Cr}$  can be calculated by (6) where  $V_{Cr\_pk}$  and  $V_{Cr\_pp}$  are the peak value and the peak-to-peak value of the capacitor voltage. It should be noted that this equation is true only at the peak gain point, where the resonant tank is pure resistive.

$$V_{Cr\_pk} = \frac{V_{Cr\_pp}}{2} = \frac{Q_{in}}{2C_r} \quad (6)$$

Combining (5) and (6), the minimum  $C_r$  value can be obtained in (7) with specifying the maximum voltage stress  $V_{Cr\_pk}$  on the capacitor  $C_r$ .

$$C_{r\_min} = \frac{P_o}{2V_{Cr\_pk} \cdot V_{in\_min} \cdot f_{min}} \quad (7)$$

In this design, substitute in (7) with  $P_o$  as 500 W,  $V_{in\_min}$  as 250 V,  $f_{min}$  of 150 kHz, and considering that the maximum AC peak voltage ratings ( $V_{Cr\_pk}$ ) for off-the-shelf film capacitors are around 350 V at 150 kHz [34], the minimum  $C_r$  value can be calculated as  $C_r = \frac{500W}{2 * 350V * 250V * 150 * 10^3 kHz} = 19nF$ .

In the case that the output power is low, the calculated minimum  $C_{r\_min}$  value from (7) will be small. The  $C_r$  value designed by other methods is usually larger than the calculated minimum value. This automatically implies that the capacitor voltage stress is not a concern for low power applications. For high power applications, however, conventional design methods would suggest smaller  $C_r$  than the minimum value, despite the excessive voltage stress. In this case, the calculated minimum value should be accepted as  $C_r$ , because if a larger  $C_r$  value is used, the corresponding  $L_r$  and  $L_p$  will be smaller. This is generally opposed to the practice of reducing the resonant current.

#### D. $L_r$ selection based on $f_r$ at 400 V

Considering the resonant frequency determined in Step A, once the resonant capacitor is selected, the resonant inductor can be obtained in (8). In this design,  $f_r$  is 250 kHz, and  $C_r$  is 19 nF. Thus, the corresponding  $L_r$  is 21  $\mu$ H.

$$L_r = \frac{1}{(2\pi f_r)^2 C_r} \quad (8)$$

#### E. $C_p$ selection based on voltage stress at $f_{min}$

Similar to  $C_r$  selection, the critical criterion for  $C_p$  selection is the voltage  $V_{Cr}$ . Generally speaking, a combination of small  $C_p$  and large  $L_p$  should be used to maximize 400 V efficiency.

As shown in the FHA model in Fig. 6,  $L_p$  and  $C_p$  can be equivalent to an inductor  $L_{m\_eq}$ . The equivalent inductor  $L_{m\_min}$  at 250 V input should be solved so to get the current stress on  $C_p$ . Substituting into (2) with  $G = nV_o / V_{in} = 1.6$ ,  $L_r$  of 21  $\mu$ H,  $f_s$  of 150 kHz,  $f_r$  of 250 kHz, and also with  $Q = \sqrt{L_r / C_r} / R_{ac}$ , in which  $R_{ac} = \frac{8n^2}{\pi^2} \cdot \frac{V_o^2}{P_o}$ ,  $n = 17$ ,  $V_o$  of 12 V and  $P_o$  of 500 W, the  $L_{m\_min}$  can be solved. In this case  $L_{m\_min}$  is 57  $\mu$ H.

It should be noted that, the calculation error of  $L_{m\_min}$  is the major source of error in this design routine. Due to the absence of high-order harmonics, the predicted voltage gain at  $f_{min}$  by the FHA method is lower than the actual gain. Then, to reach the same gain requirement, FHA will suggest lower  $L_{m\_min}$ , which will further impact the selection of  $C_p$  and  $L_p$ . A fine tune process will be introduced in a later part.

Based on the FHA model, the current in the parallel branch can be calculated in (9), in which  $I_{p\_pk\_fmin}$  is the peak value of the parallel current at  $f_{min}$ ;  $L_{m\_min}$  is the equivalent magnetizing inductance at  $f_{min}$ .

$$I_{p\_pk\_fmin} = \frac{4}{\pi} n V_o \cdot \frac{1}{2\pi f_{min} L_{m\_min}} \quad (9)$$

The AC peak voltage stress for given  $C_p$  value can be calculated by (10), in which  $V_{Cp\_pk\_fmin}$  is the peak value of the  $C_p$  voltage stress at  $f_{min}$ ;  $X_{Cp}$  is the impedance of  $C_p$  at  $f_{min}$ .

$$V_{Cp\_pk\_fmin} = I_{p\_pk\_fmin} X_{Cp} = \frac{I_{p\_pk\_fmin}}{2\pi f_{min} C_p} \quad (10)$$

Then combining (9) and (10), the minimum  $C_p$  value is given in (11).

$$C_{p\_min} = \frac{n V_o}{\pi^3 f_{min}^2 L_{m\_min} V_{Cp\_pk\_fmin}} \quad (11)$$

In this design example, substitute in to (11) with  $n = 17$ ,  $V_o$  of 12 V,  $f_{min}$  of 150 kHz, and 57  $\mu$ H as  $L_{m\_min}$  and 350 V as peak voltage stress, the minimum  $C_p$  value is 14.6 nF.

#### F. $L_p$ selection based on $L_{m\_min}$ at $f_{min}$

For a given  $C_p$ , there is one and only one  $L_p$  that pairs with it, so that the equivalent  $L_{m\_min}$  is as determined in Step E at the minimum frequency. The  $L_p$  value can be calculated by (1). With 57  $\mu$ H as  $L_{m\_min}$ , 150 kHz as  $f_{min}$ , and 14.6 nF as  $C_p$ , in this example,  $L_p$  is 134  $\mu$ H.

#### G. Fine Tune of the parameters with PSIM simulation

As widely acknowledged, the accuracy of FHA degrades when the switching frequency is away from the resonant point. Specifically, in this case, a smaller-than-actual  $L_{m\_min}$  value is predicted, which leads to a larger  $C_p$  and smaller  $L_p$  selection. The reverse correlation of  $L_{m\_min}$  and  $C_p$  has been shown in (11). The error, however, can be easily corrected by simulation software, which has a much more accurate prediction of voltage gain.

The calculation of  $C_r$  and  $L_r$  results from the time domain equations and/or at resonant frequency, thus the accuracy is high. In this case, the  $C_r$  and  $L_r$  values from Step C and Step D are used in PSIM to find the  $L_{m\_min}$  value. If a margin for the minimum input voltage is intended, it should be performed in this stage. In this design example,  $L_{m\_min}$  value of 85  $\mu$ H at  $f_{min} = 135$  kHz is found a reasonable setup, which provides a 20 V input voltage margin, so that actual  $V_{in\_min}$  is 230 V. It should be noted that since the  $V_{in\_min}$  and the  $f_{min}$  are changed, the  $C_r$  value should also have a fine adjustment based on (7). In this case,  $C_r$  value is calibrated to 23 nF and  $L_r$  value is calibrated accordingly to 16  $\mu$ H.

Then with the fine-tuned  $L_{m\_min}$  value of 85  $\mu$ H, also substitute in to (11) with  $n = 17$ ,  $V_o$  of 12 V,  $f_{min}$  of 135 kHz, and 400 V peak voltage stress at 135 kHz, the calibrated  $C_p$  value is 10.6 nF. The corresponding  $L_p$  is 216  $\mu$ H, which can be calculated by (1).

TABLE I shows the parameter design comparison between the FHA prediction and the PSIM calibrated results. As can be observed, the design of  $L_r$  and  $C_r$  values are rather true from the FHA while the  $L_p$  and  $C_p$  have some deviation. Although FHA can provide a good pre-dimensioning of the four resonant parameters, a calibration process is still considered as necessary to provide a more realistic design result.

TABLE I. PARAMETER DESIGN COMPARISON BETWEEN FHA AND SIMULATION CALIBRATED RESULTS

	FHA Prediction	PSIM Calibration
$L_r$	21 $\mu$ H	17 $\mu$ H
$C_r$	19 nF	23 nF
$L_p$	134 $\mu$ H	216 $\mu$ H
$C_p$	14.6 nF	10.6 nF

#### H. Practical considerations of capacitor value

Besides the design considerations of the resonant frequency and minimum frequency selection as well as the minimum input voltage margin, the selection of capacitor values should also be practical. The 4.7 nF FKP-series film capacitor from WIMA appears to be a good balance of capacitance and voltage rating. In this design, total 23.5 nF consisting of 5 paralleled 4.7 nF capacitors are used as  $C_r$ , and total 9.4 nF consisting of 2 paralleled 4.7 nF capacitors are used as  $C_p$ . The final LCLC resonant tank design is shown in TABLE II.

TABLE II. PARAMETER DESIGN OF LCLC CONVERTER

	$L_r$	$L_p$	$C_p$
$C_r$	23.5 nF	$C_p$	9.4 nF
$f_r$	250 kHz	$f_{min}$	135 kHz

## IV. EXPERIMENT RESULTS

To verify the effectiveness of the LCLC topology and the design method, a prototype as shown in Fig. 13 is built to operate at 250 V-400 V input and 12 V/500 W rated load. Detailed design specification is shown in TABLE III. Due to the leakage inductance of the main transformer, the actual switching frequency is slightly lower than the designed one.

In the prototype, synchronous rectifiers are used to reduce the secondary rectifiers loss. Since LCLC converters have the same operation as that of conventional LLC converter, a generic SR controller (IR11682S) for LLC converter is used. The controller will detect the conduction timing of the body diode and then turn on the SR accordingly. Besides, a RCD delay circuit is used to offset the impact of the MOSFET package inductance, and help the controller capture the proper turn off timing [34].

TABLE III. DESIGN SPECIFICATION AND POWER TRAIN PARAMETERS OF LCLC CONVERTER

$V_{in}$	250 V-400 V
$V_o / I_o$	12 V / 42 A
$P_o$	500 W
$C_o$	860 $\mu$ F (330 $\mu$ F E-cap * 2 + 100 $\mu$ F ceramic * 2)
$T_x$ turns ratio	17:1
$L_r$	16.5 $\mu$ H
$C_r$	23.5 nF (4.7 nF * 5)
$L_p$	230 $\mu$ H
$C_p$	9.4 nF (4.7 nF * 2)
$L_{lkg}$	5 $\mu$ H
Designed 400V $f_s$	250 kHz
Designed 250V $f_s$	135 kHz

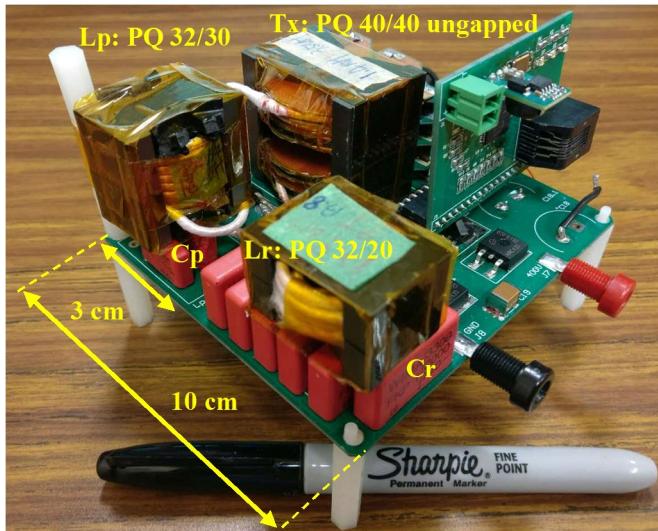


Fig. 13. Picture of the prototype

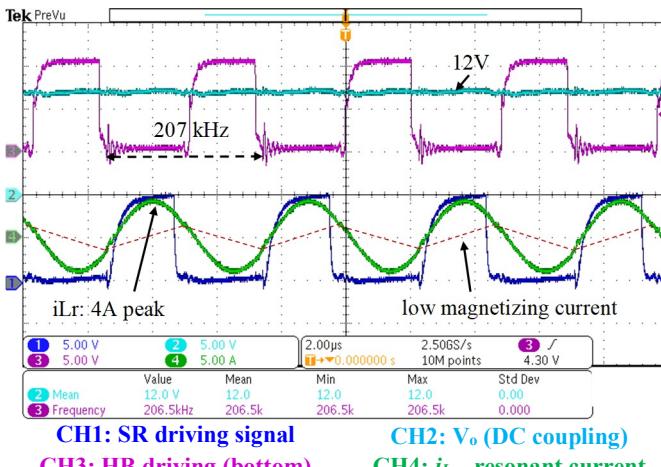


Fig. 14. 400 V input, 12 V/40 A output steady state waveform

Fig. 14 shows the steady state waveforms under 12 V/40 A full load condition at 400 V input, at which the equivalent  $L_m$  is 180  $\mu$ H. As can be observed, the magnetizing current is  $\sim 1.5$  A, which is a relatively small value. Thus, high efficiency at nominal 400 V can be achieved.

Fig. 15 shows the steady state waveforms under 12 V/40 A full load condition at 250 V input. At 250 V, the switching frequency reduces to 140 kHz, which has good agreement with the designed value. The magnetizing current peak value reaches 3.5 A, which implies the equivalent  $L_m$  is reduced to accommodate the low input voltage.

Fig. 16 shows the output voltage response to the input voltage drop under full load of 40 A. The output voltage can be maintained at 12 V even when the input voltage reduces to 220 V.

Fig. 17 shows the steady state waveforms under 12 V/20 A half load condition at 400 V input. Similar to the full load case, the equivalent magnetizing inductor is around 180  $\mu$ H (even larger because switching frequency higher), and the magnetizing current is very small (1.5 A).

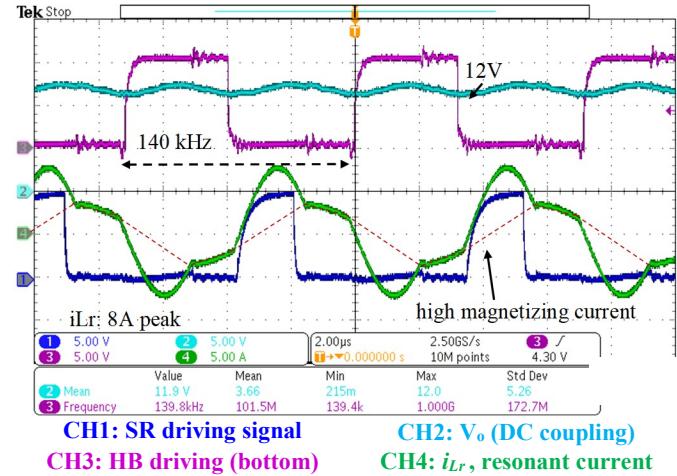


Fig. 15. 250 V input, 12 V/40 A output steady state waveform

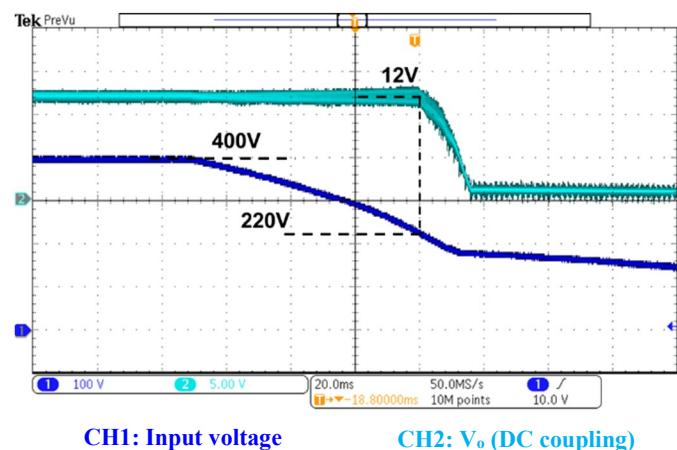


Fig. 16. Hold-up test under full load

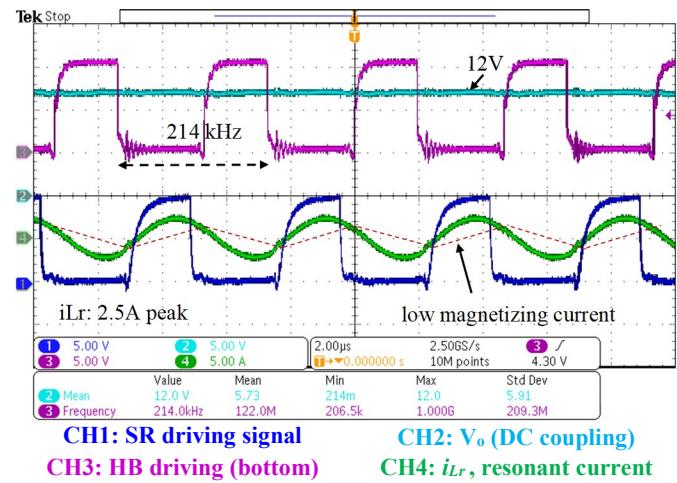


Fig. 17. 400 V input, 12 V/20 A output steady state waveform

Fig. 18 shows the steady state waveforms under 12 V/20 A full load condition at 250 V input. The switching frequency reduces to 140 kHz, and the equivalent  $L_m$  is 70  $\mu$ H, so that the magnetizing current increase to 3.5 A.

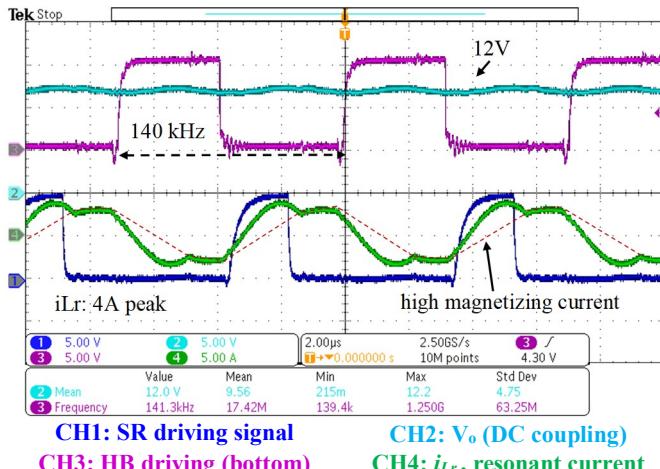


Fig. 18. 250 V input, 12 V/20 A output steady state waveform

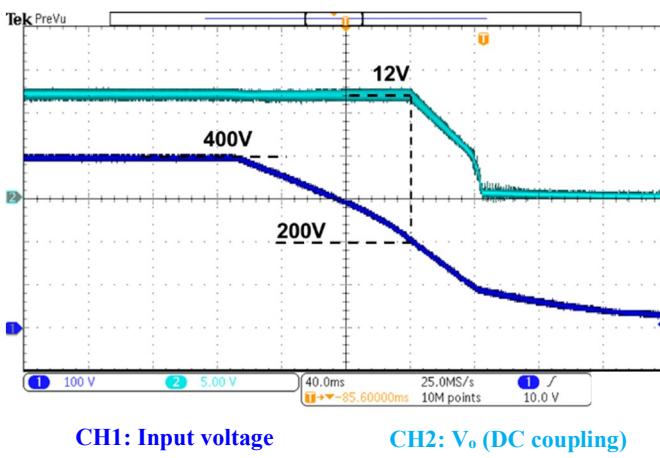


Fig. 19. Hold-up test under half load

Fig. 19 shows the output voltage response to the input voltage drop under half load. The output voltage does not lose regulation until the input voltage reduces to 200 V.

Fig. 20 shows the efficiency comparison between LCLC converter and a conventional LLC converter with same input voltage range from 250 V-400 V. The LLC converter magnetizing inductor is designed as 70  $\mu$ H, which is the same as the equivalent  $L_p$  value for LCLC converter at 250 V. As can be observed, at 400 V, the efficiency of LCLC (solid blue) is generally 1% higher than the conventional LLC (solid red), thanks to the larger equivalent  $L_p$  of 180  $\mu$ H. The front-end system is expected to benefit from this improvement, because the converter will operate for dominantly long time at 400 V. At 250 V, the LCLC converter efficiency (dashed blue) marginally trails the LLC converter (dashed red) by 0.2%, generally due to the additional loss on  $C_p$ . If the converter is designed for operating over a wide input range with equal chance at different input voltages, LCLC converter can still benefit from the higher average efficiency over the conventional LLC converter.

Fig. 21 shows the measured efficiency at different input voltages: 250 V, 300 V, 350 V and 400 V. The highest efficiency achieved is 96.4% at 400 V input, 60% load. For 400 V input full load, the achieved efficiency is 96.2%. As the

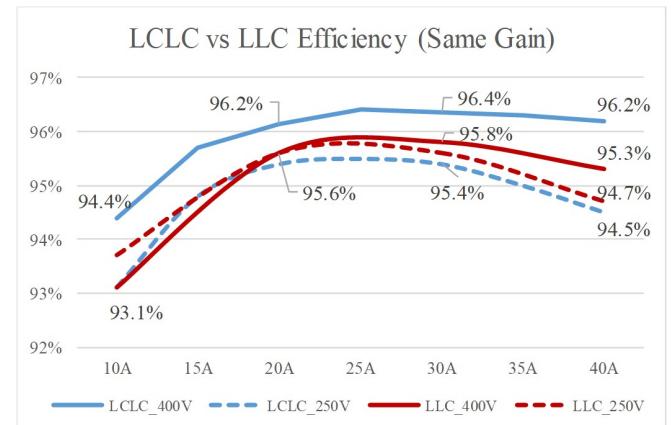


Fig. 20. Efficiency comparison of LCLC and LLC for 250 V and 400 V

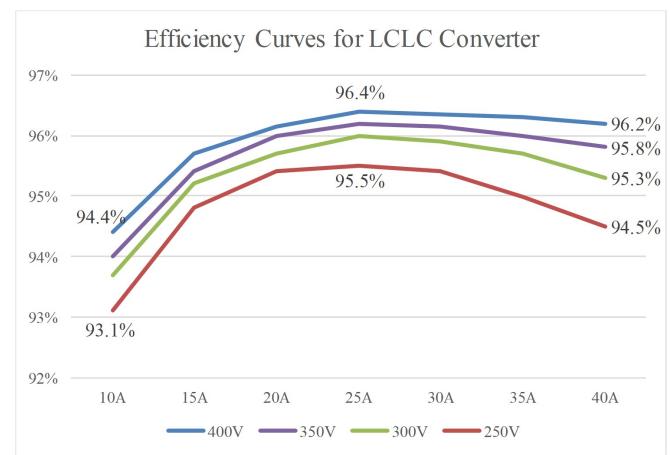


Fig. 21. Efficiency curves of different input voltage level v.s. load

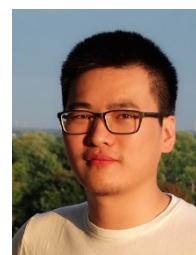
input voltage reduces, the equivalent  $L_m$  is reduced, and the conduction loss increases, the efficiency is thus slightly degraded. For 250 V condition, the highest efficiency is 95.5% at 60% load. For full load, the measured efficiency is 94.3%.

## V. CONCLUSION

In this paper, LCLC resonant topology is examined and explained from the voltage gain improvement point of view. The LCLC topology achieves high efficiency for 400 V input as well as high voltage gain to satisfy the hold-up requirement. Besides, LCLC converter enjoys high reliability, simple control and low cost, because no active component is added, and generic LLC controller can be directly used. A design methodology focusing on the capacitor voltage stress is proposed to achieve optimal capacitor utilization in high power applications. A 250 V-400 V input, 500 W prototype has been built to verify LCLC converter operation and the parameter design. The experiment results justify the feasibility and effectiveness of topology and the design method. With the LCLC converter prototype, the size increase is 10% as compared to the magnetics-integrated configuration, while there is no size increase when compared to core-separate configuration. A 1% of efficiency improvement is achieved for 400 V operation. This is believed a significant reduction of power consumption and emission for applications like datacenters.

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author of 20 technical papers published in IEEE journals and conferences and has 6 US/PCT patents pending.

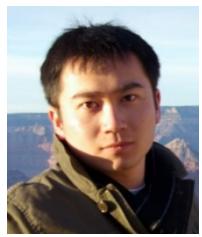


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His current research interests include multilevel topology, High-gain topology, parallel technology and Virtual Synchronous Generator (VSG) technology for photovoltaic application and micro-grids application; resonant converters and server power supplies, and LED drivers. He has authored over 60 technical papers in journals and conferences. He is the inventor/co-inventor of 41 China issued patents, 2 US issued patents, 11 US patents pending and 9 PCT patents pending.

Dr. Wang is currently a senior member of China Electro-Technical Society (CES), a senior member of China Power Supply Society (CPSS). He serves as a member of CPSS Technical Committee on Standardization; a member of CPSS Technical Committee on Renewable Energy Power Conversion, a China Expert Group Member of IEC Standard TC8/PT 62786, a Vice-Chair of IEEE Kingston Section, a Session Chair of ECCE 2015 and ECCE2017, a TPC member of ICEMS2012.



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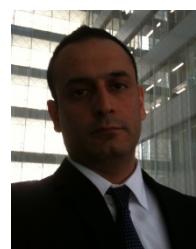
He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, in Ottawa, Canada from 1994 to 1999. Since 1999, he has been with Queen's University, where he is currently a Professor with the Department of Electrical and Computer Engineering. His current research interests include digital control technologies for high efficiency, fast dynamic response dc–dc switching converter and ac–dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He has authored over 230 technical papers in the IEEE Transactions and conferences and holds 25 U.S. patents. He is also a Principal Contributor for two IEEE standards. He is a Fellow of Canadian Academy of Engineering and received Modeling and Control Achievement Awards from IEEE Power Electronics Society. He received Premier's Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997.

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