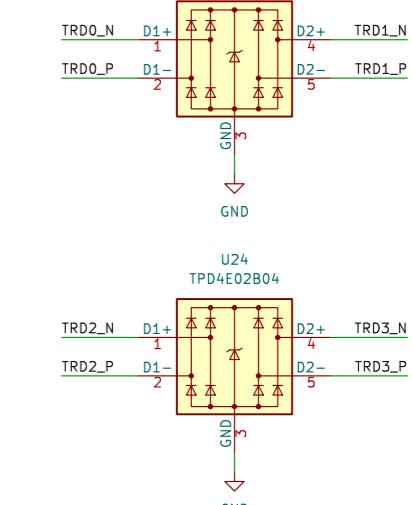
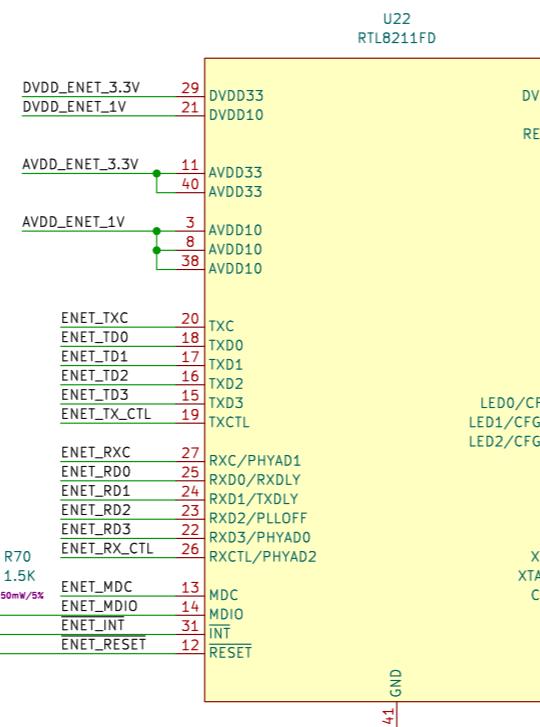
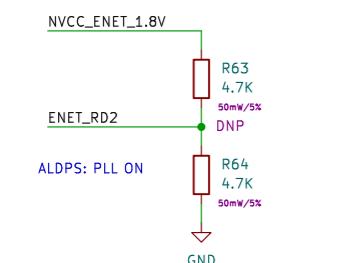
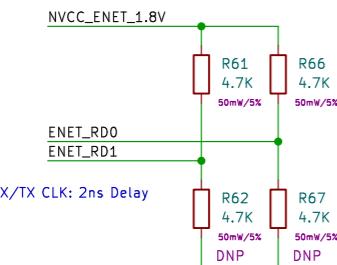
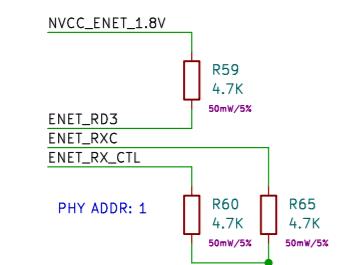
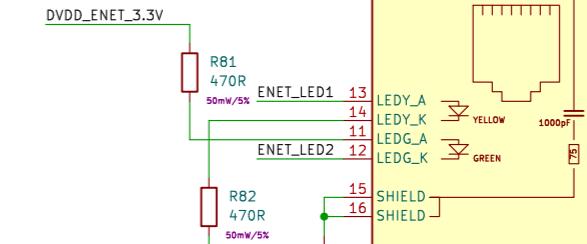
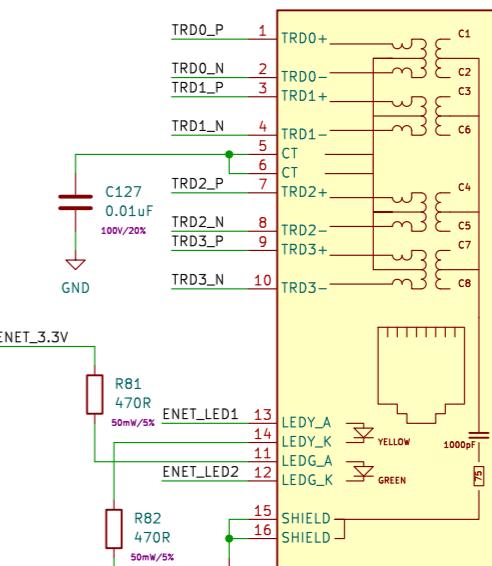
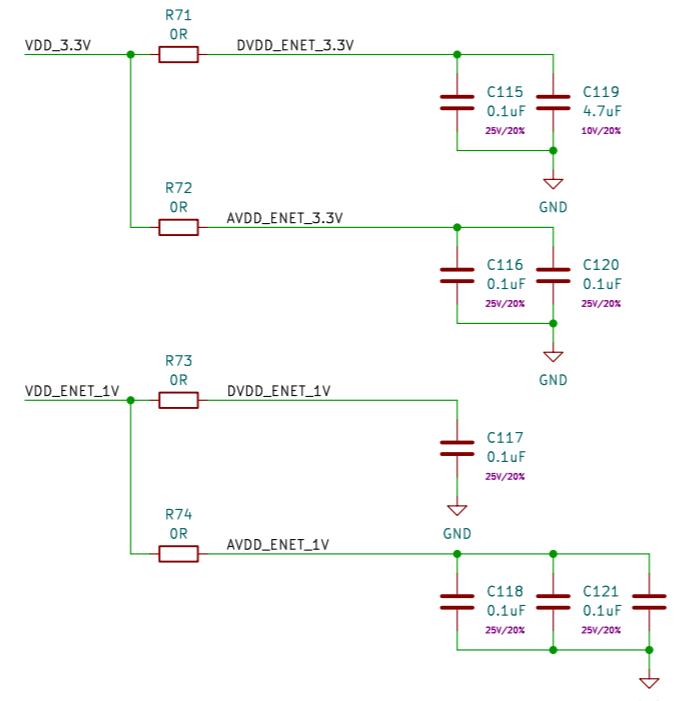
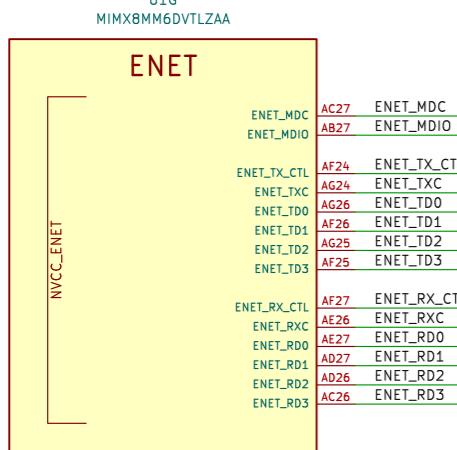


VDD\_3.3V  
 VDD\_1.8V  
 NVCC\_ENET\_1.8V  
 ENET\_INT  
 ENET\_RESET



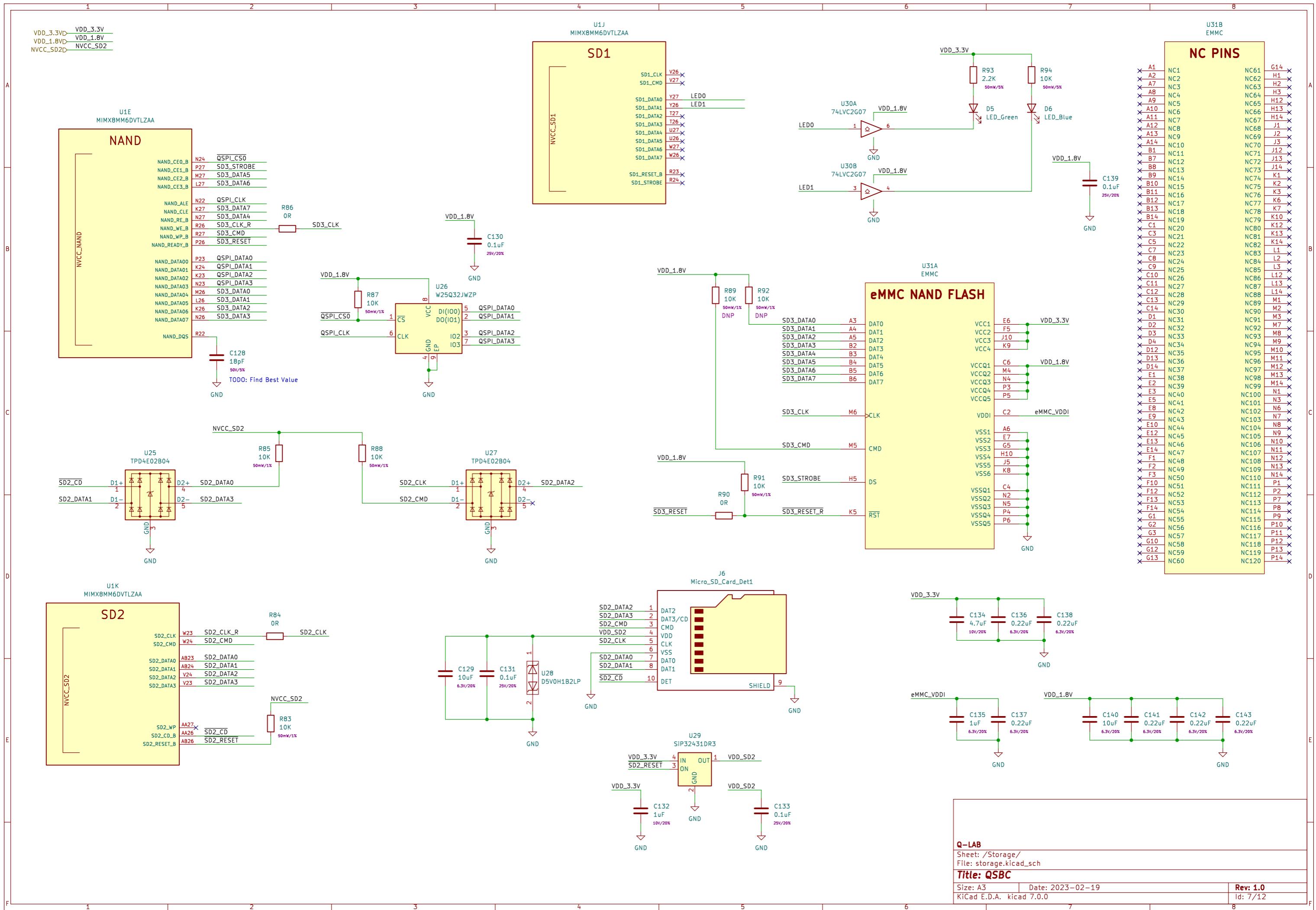
### Q-LAB

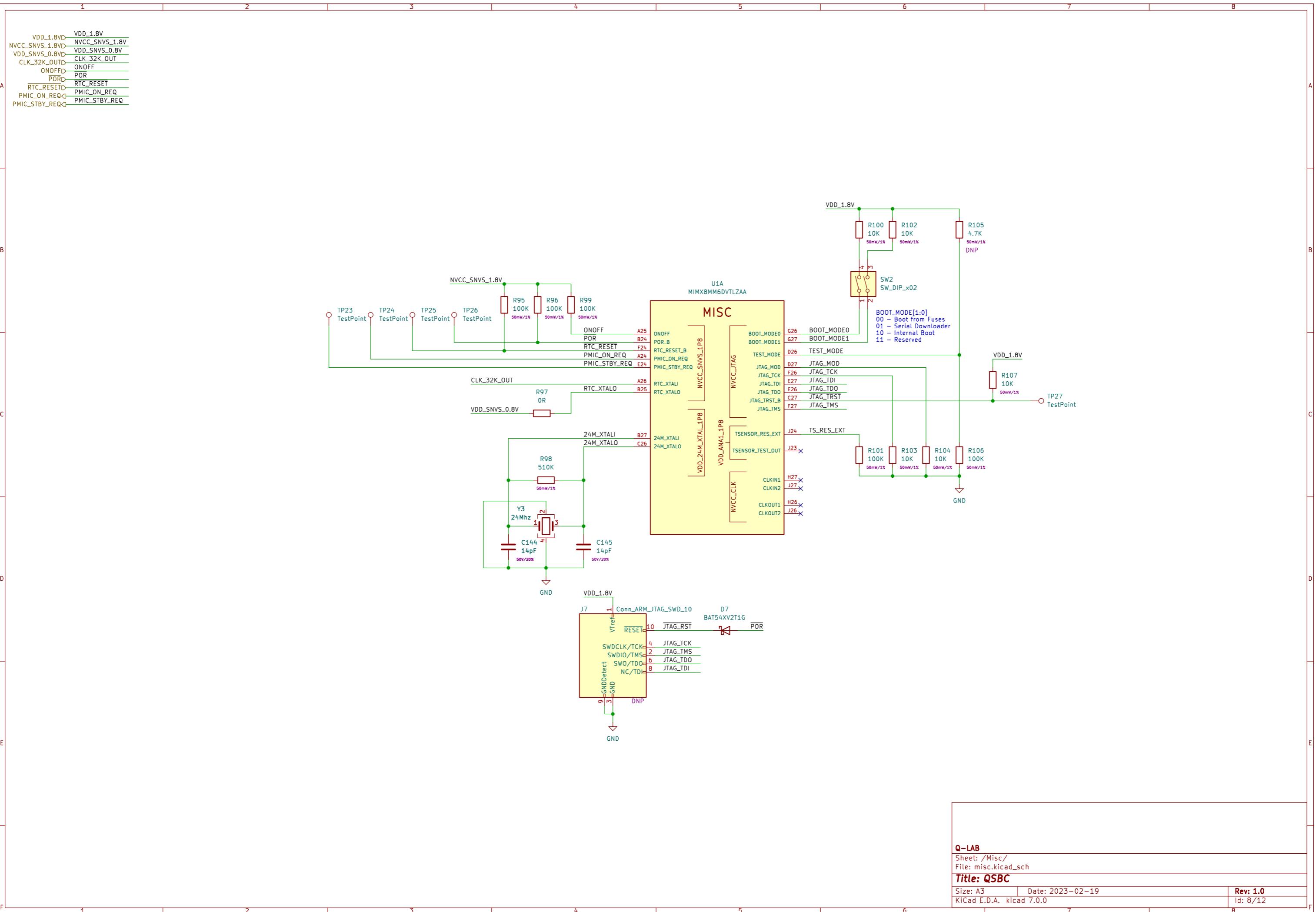
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File: ethernet.kicad\_sch

Title: QSBC

Size: A3 Date: 2023-02-19  
KiCad E.D.A. kicad 7.0.0

Rev: 1.0  
Id: 6/12





VDD\_3.3V  
 VDD\_1.8V  
 M2\_RESET  
 M2\_WAKE  
 WDOG  
 INA\_ALERT  
 USB1\_INT  
 USB1\_VBUS\_EN  
 USB1\_VBUS\_FLT  
 USB2\_VBUS\_EN  
 USB2\_VBUS\_FLT  
 UART2\_RXD  
 UART2\_TXO  
 UART2\_RTS  
 UART2\_CTS  
 UART1\_RXD  
 UART1\_RXI  
 UART1\_TXO  
 UART1\_RTS  
 UART1\_CTS  
 I2C4\_SDA  
 I2C4\_SCL  
 ENET\_INT  
 ENET\_RESET  
 SD2\_SELECT  
 SD2\_VSELECT  
 DS186\_EN  
 DS186\_INT  
 DS186\_INTD

### ECSPI

ECSP11\_MISO  
 ECSP11\_MOSI  
 ECSP11\_SCLK  
 ECSP11\_SS0  
 ECSP12\_MISO  
 ECSP12\_MOSI  
 ECSP12\_SCLK  
 ECSP12\_SS0

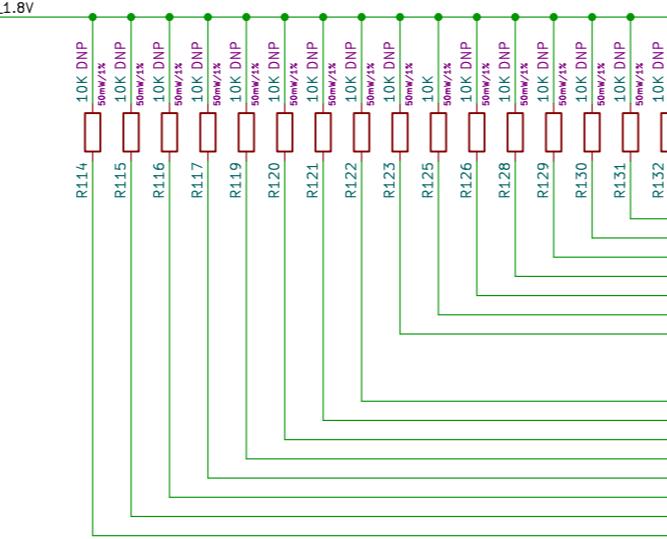
A7  
 B7  
 D6  
 B6  
 AB  
 B8  
 E6  
 A6

UART4\_CTS  
 M2\_WAKE  
 DS186\_EN  
 UART4\_RTS

### GPIO

GPIO1\_I000 AG14 ENET\_INT  
 GPIO1\_I001 AF14 ENET\_RESET  
 GPIO1\_I002 AG13 WDOG  
 GPIO1\_I003 AF13 INA\_ALERT  
 GPIO1\_I004 AG12 PMIC\_INT  
 GPIO1\_I005 AF12  
 GPIO1\_I006 AG11  
 GPIO1\_I007 AF11  
 GPIO1\_I008 AG10  
 AF10 SD2\_SELECT  
 GPIO1\_I009 AD10 USB2\_VBUS\_FLT  
 GPIO1\_I010 AC10 USB2\_INT  
 GPIO1\_I011 AB10 USB2\_VBUS\_EN  
 GPIO1\_I012 AD9 USB1\_VBUS\_FLT  
 GPIO1\_I013 AC9 USB1\_INT  
 GPIO1\_I014 AB9 USB1\_VBUS\_EN  
 GPIO1\_I015 AB9

TODO: USB\*\_VBUS\_FLT should be on USB PHY OC pad



### SAI

SAI1\_MCLK  
 SAI1\_RXFS  
 SAI1\_TXC  
 SAI1\_RXD0  
 SAI1\_RXD1  
 SAI1\_RXD2  
 SAI1\_RXD3  
 SAI1\_RXD4  
 SAI1\_RXD5  
 SAI1\_RXD6  
 SAI1\_RXD7  
 SAI1\_MCLK  
 SAI1\_RXFS  
 SAI1\_TXC  
 SAI1\_RXD0  
 SAI1\_RXD1  
 SAI1\_RXD2  
 SAI1\_RXD3  
 SAI1\_RXD4  
 SAI1\_RXD5  
 SAI1\_RXD6  
 SAI1\_RXD7  
 SAI2\_MCLK  
 SAI2\_RXFS  
 SAI2\_TXC  
 SAI2\_RXD0  
 SAI2\_RXD1  
 SAI2\_RXD2  
 SAI2\_RXD3  
 SAI2\_RXD4  
 SAI2\_RXD5  
 SAI2\_RXD6  
 SAI2\_RXD7  
 SAI3\_MCLK  
 SAI3\_RXFS  
 SAI3\_TXC  
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 SAI3\_RXD1  
 SAI3\_RXD2  
 SAI3\_RXD3  
 SAI3\_RXD4  
 SAI3\_RXD5  
 SAI3\_RXD6  
 SAI3\_RXD7  
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 SAI4\_RXFS  
 SAI4\_TXC  
 SAI4\_RXD0  
 SAI4\_RXD1  
 SAI4\_RXD2  
 SAI4\_RXD3  
 SAI4\_RXD4  
 SAI4\_RXD5  
 SAI4\_RXD6  
 SAI4\_RXD7

Board Revision Straps  
 SA15\_RXD[3:1]  
 001 - Rev 1.0

AD15  
 AB15  
 AC15  
 AD18  
 AC14  
 VDD\_1.8V

AD13  
 AC13

AD6  
 AC6

AF6  
 AF6

AG8  
 AG7  
 AF7

AF7  
 AF7

AF8  
 AF9  
 AF9

AD19  
 AD23

AD22  
 AC22

AC19  
 AB22

AC24  
 AC24

UART1\_RXI  
 UART1\_RTS

UART1\_RXO  
 UART1\_CTS

TODO: UART1\_RXO Should be on SAI2\_RXFS

AC19  
 AB22

AC24  
 AC24

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 UART1\_RTS

UART1\_RXO  
 UART1\_CTS

TODO: UART1\_RXO Should be on SAI2\_RXFS

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TODO: UART1\_RXO Should be on SAI2\_RXFS

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 AC24

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 UART1\_RTS

UART1\_RXO  
 UART1\_CTS

TODO: UART1\_RXO Should be on SAI2\_RXFS

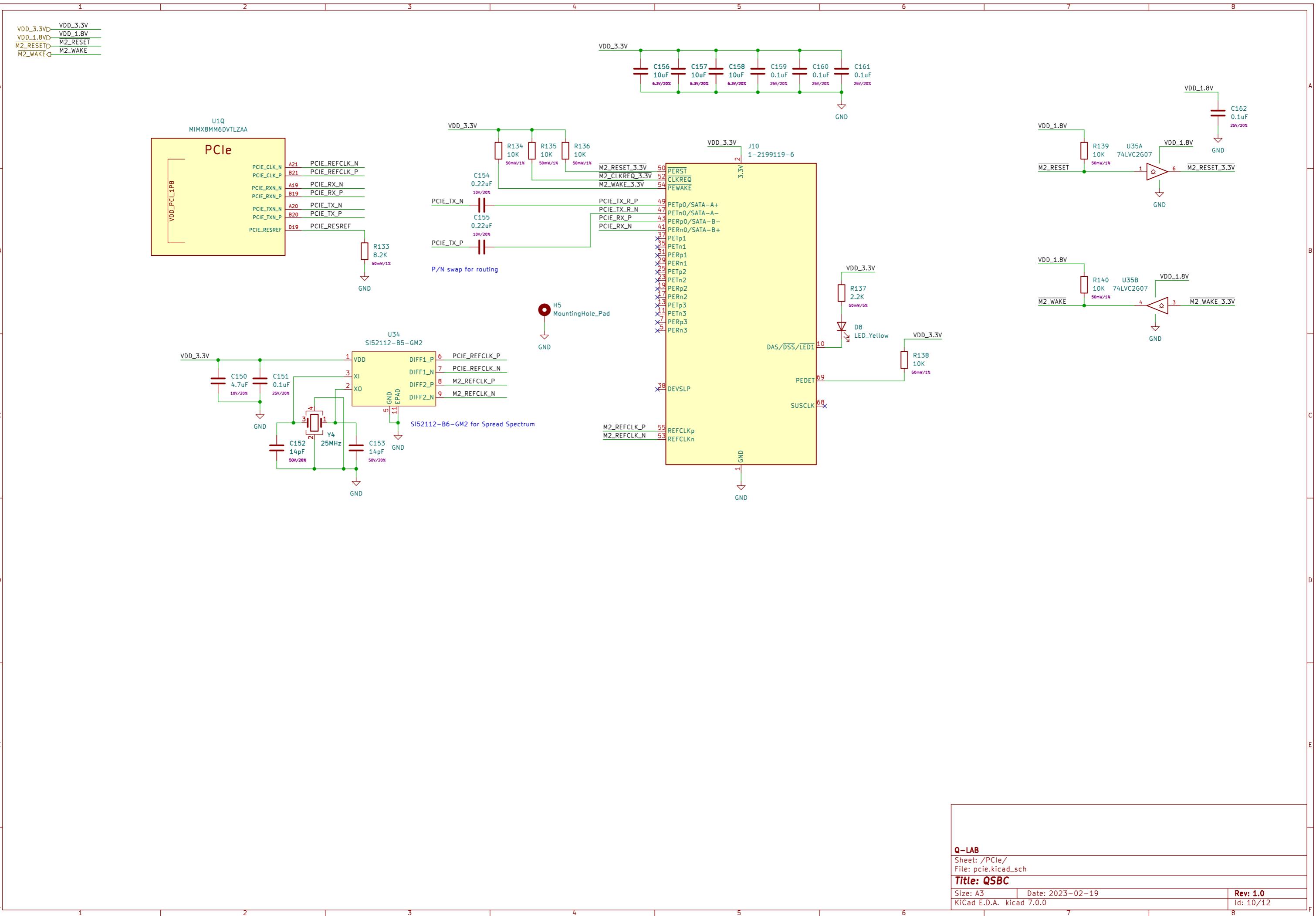
AC19  
 AB22

AC24  
 AC24

UART1\_RXI  
 UART1\_RTS

UART1\_RXO  
 UART1\_CTS

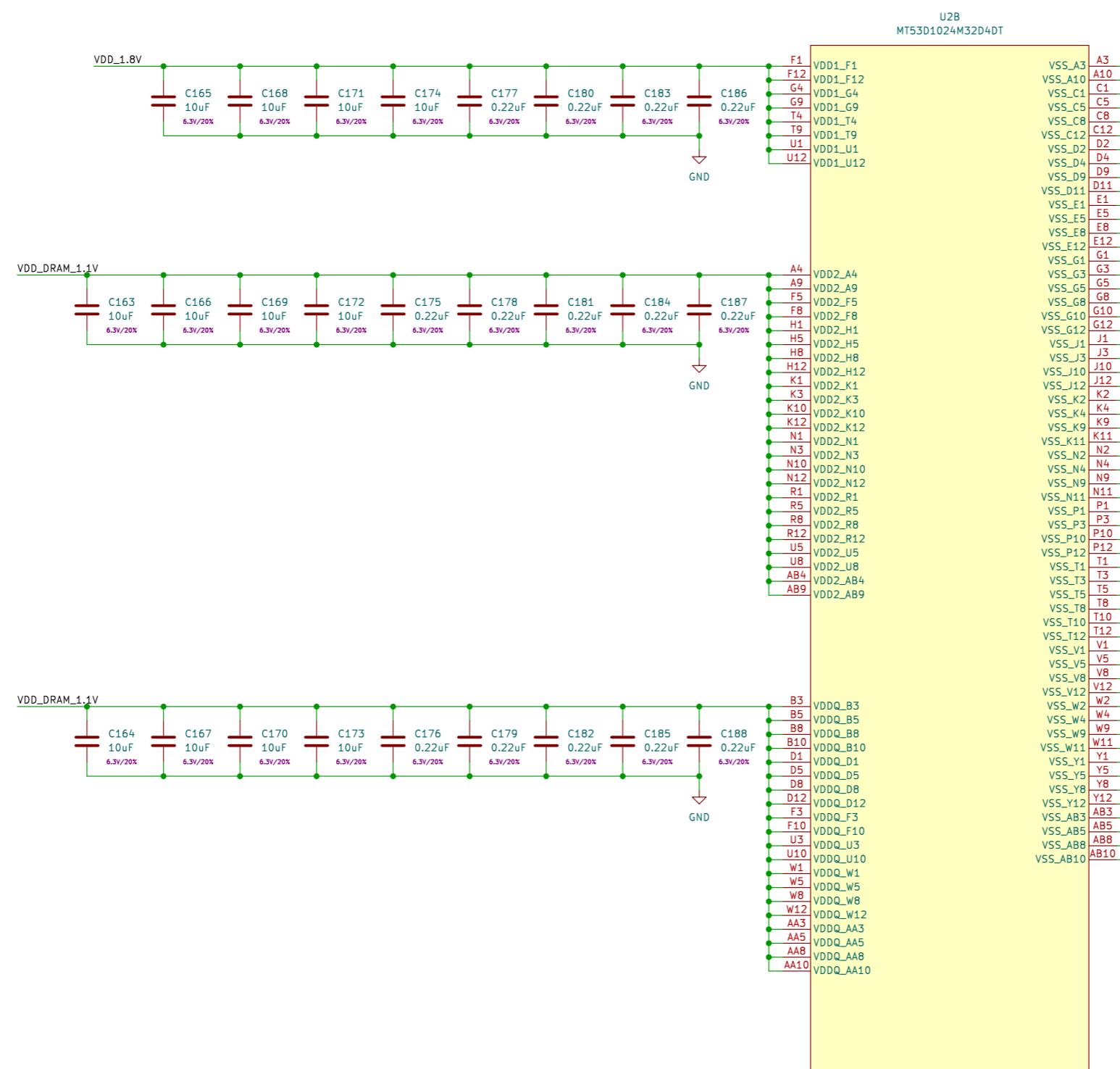
TODO: UART1\_RXO Should be on SAI2\_RXFS



1 2 3 4 5 6 7 8

VDD\_1.8V  
VDD\_DRAM\_1.1V

A



Q-LAB

Sheet: /DDR Power/  
File: ddr\_power.kicad\_sch

Title: QSBC

Size: A3 Date: 2023-02-19  
KiCad E.D.A. kicad 7.0.0

Rev: 1.0  
Id: 11/12

1 2 3 4 5 6 7 8

