# Hardware Acceleration on FPGA of an Integrated Sensing and Communication OFDM Chain

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## Objective

Both communication and RADAR systems exploit the same frequency spectrum, but for different purposes. The first aims to transmit unknown data, the second aims to detect targets. As they share processing steps, why not combine them in a single system? **How to achieve a sufficient level of performance to be able to process data in real-time?**

## Context

In recent years, the concept of integrated sensing and communication systems (ISAC) has gained attention. **Combining data transmission and target detection** into a single system, would enable to:

- exploit the frequency spectrum more efficiently;
- reduce the number of hardware needed.

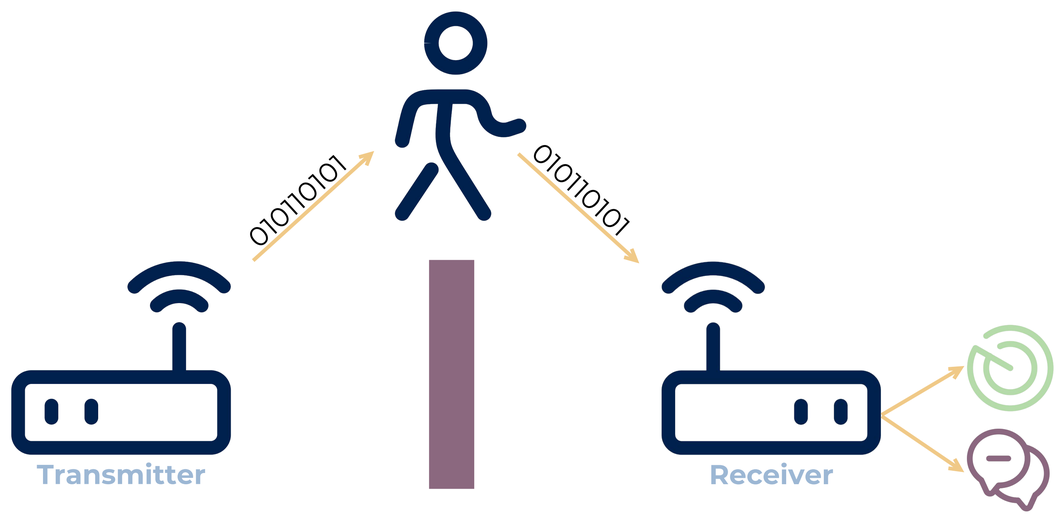


Figure 1:ISAC system considered in this work

New standards, like the upcoming 802.11bf, are being defined to support sensing capabilities in Wi-Fi networks. Based on **Orthogonal Frequency Division Multiplexing (OFDM) modulation**, Wi-Fi Sensing can be used to detect the presence of people, monitor their movements, or even perform fall detection.

## Experimental setup

Proof of concept of ISAC exists, with an **experimental setup** developed at UCLouvain. Based on a software implementation, it first captures the received signal, then **process data offline**. It uses the Universal Software Radio Peripheral (USRP) devices from Ettus Research to transmit and receive signals.

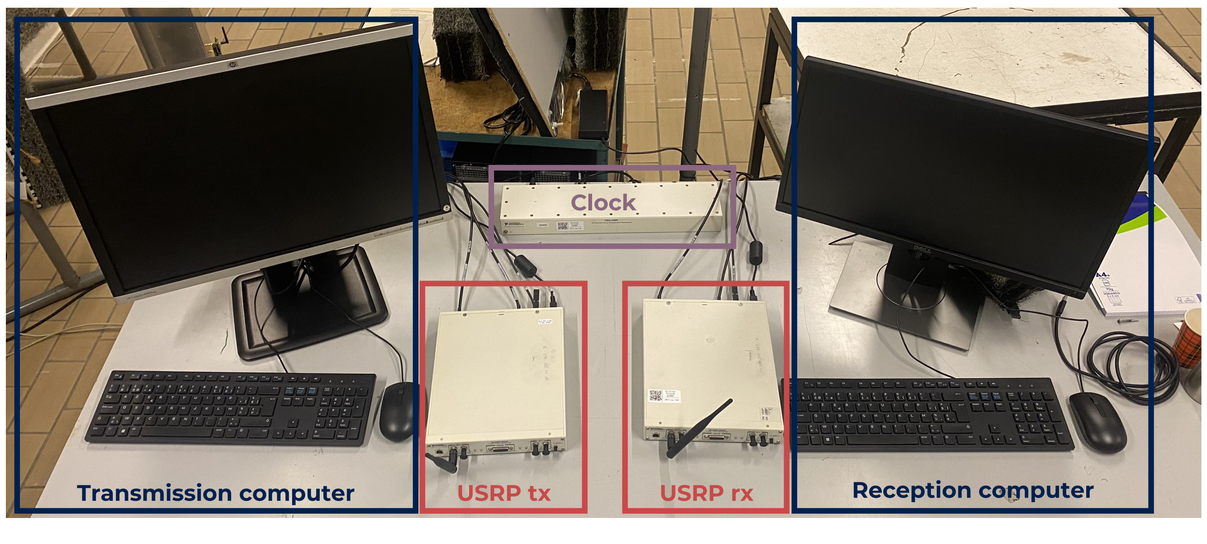


Figure 2:USRP-based experimental setup

## Methodology

USRP devices embed **Field-Programmable Gate Arrays (FPGAs)** that can be programmed to accelerate the processing of the data. By implementing several blocks of the OFDM receiver chain on the FPGA, it is possible to speed up the processing and **target real-time data processing**.

To ensure an efficient implementation, it is necessary to:

- analyze the complexity of each stage;
- optimize the processing pipeline;
- implement the most time-consuming blocks on hardware.

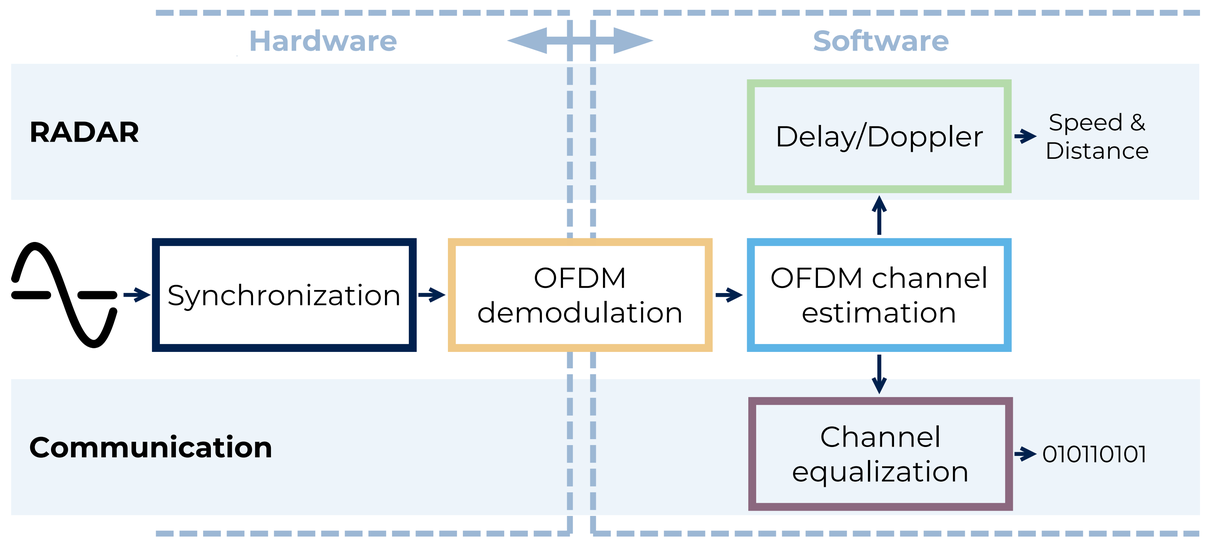


Figure 3:OFDM receiver chain

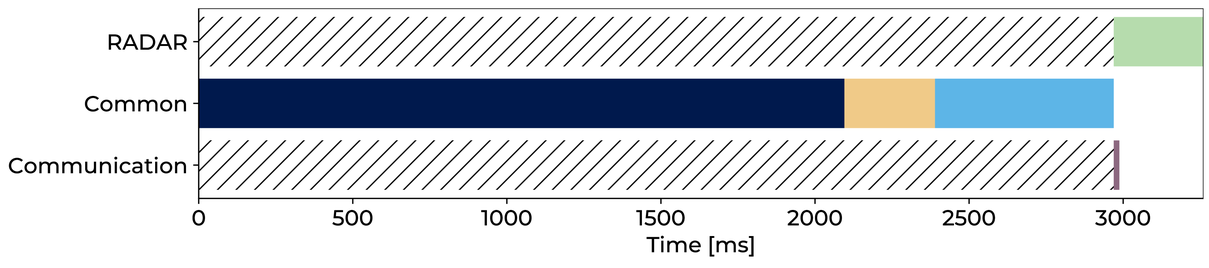


Figure 4:Time taken by each block of the receiver chain for a 2048 OFDM symbols packet

Internally, the FPGA of the USRP devices is composed of several blocks that can be interconnected to create a custom processing chain. Ettus Research developed the **RFNoC** (RF Network on Chip) framework to facilitate the development of FPGA-based signal processing chains and enable the integration of custom processing blocks.

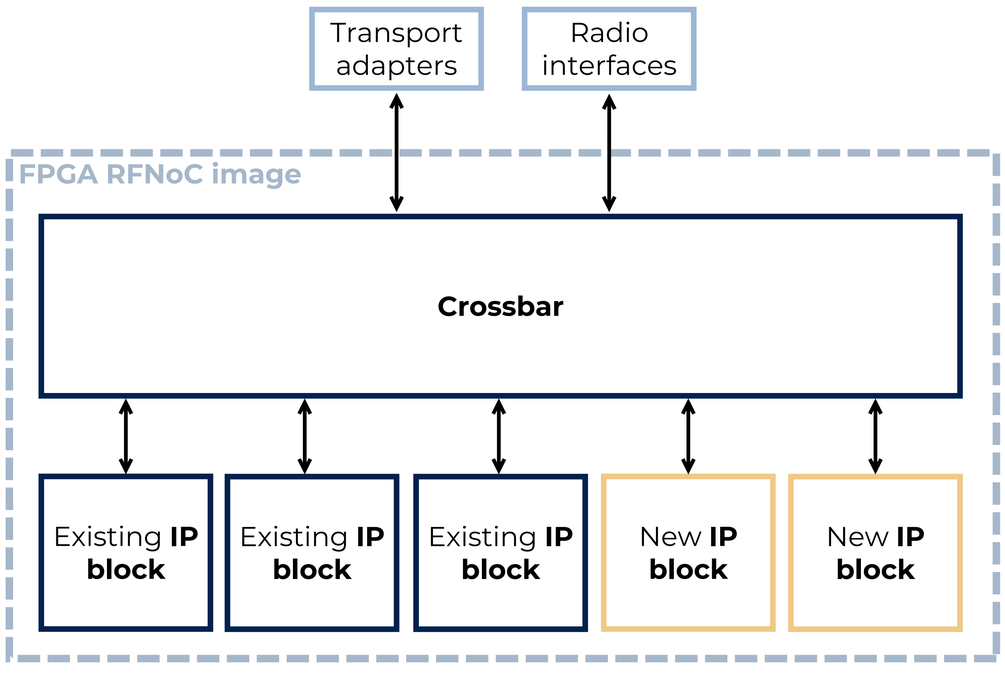


Figure 5:RFNoC framework vizualisation