TFE25-462: Meeting 3

Programming USRP X310 with UHD and RFNoC

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Setup overview

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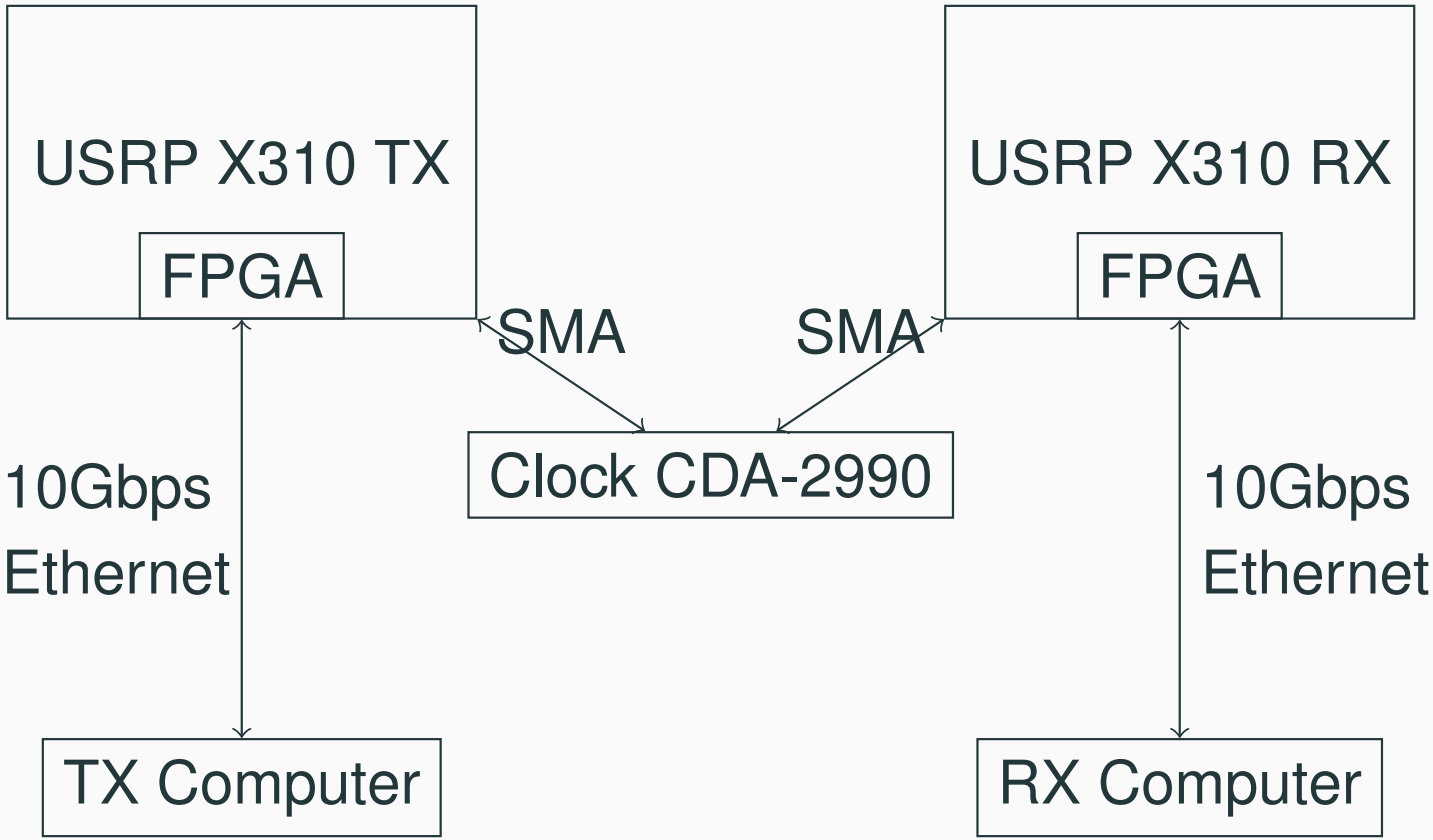

Figure 1: Setup block diagram

USRP Components and programming overview

USRP Overview

- Two denominations:
  - **USRP X310** in the Ettus Research product line.
  - **USRP 2944R** in the National Instruments product line.
- It includes on the Xilinx Kintex-7 FPGA.
- It can be programmed using the UHD driver and RFNoC provided by Ettus Research (see later)
- Needs AMD Xilinx Vivado to compile the FPGA image.

USRP Block Diagram

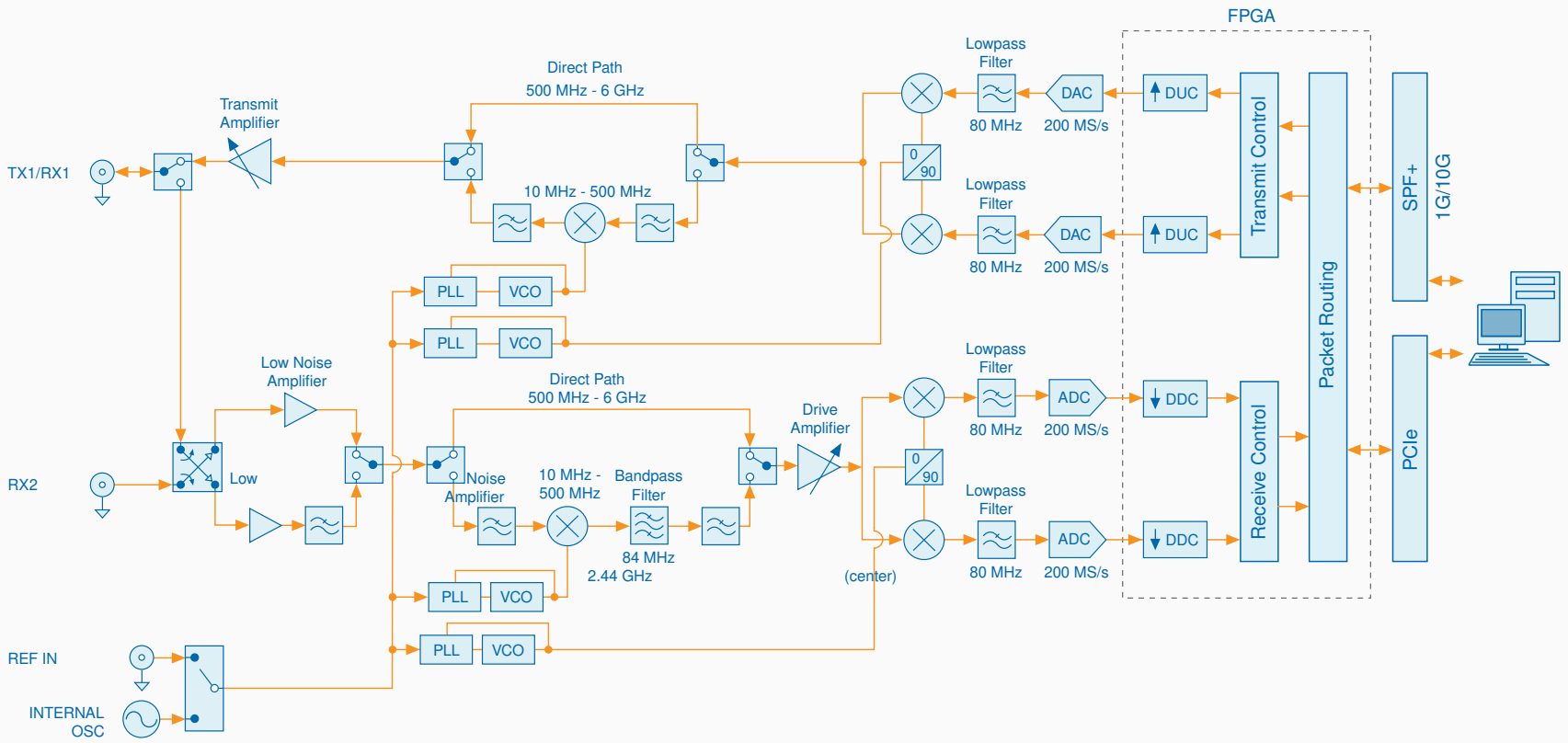

Figure 2: USRP X310 Block Diagram

UHD Overview

- UHD stands for **USRP Hardware Driver**.
- It is an open-source, cross-platform driver for USRP devices.
- It is written in C++ and provides a C API.
- It is used to control the USRP device and stream data to and from it.
- It is used to program and manage the FPGA image.

RFNoC Overview

- RFNoC stands for **RF Network on Chip**.
- It is a framework that allows to create FPGA blocks that can be connected together.
- It comes with a set of blocks that are already implemented and can be used.
- It is includes in the UHD driver since version 3.15, and cannot be disabled since version 4.0.

RFNoC Block Diagram

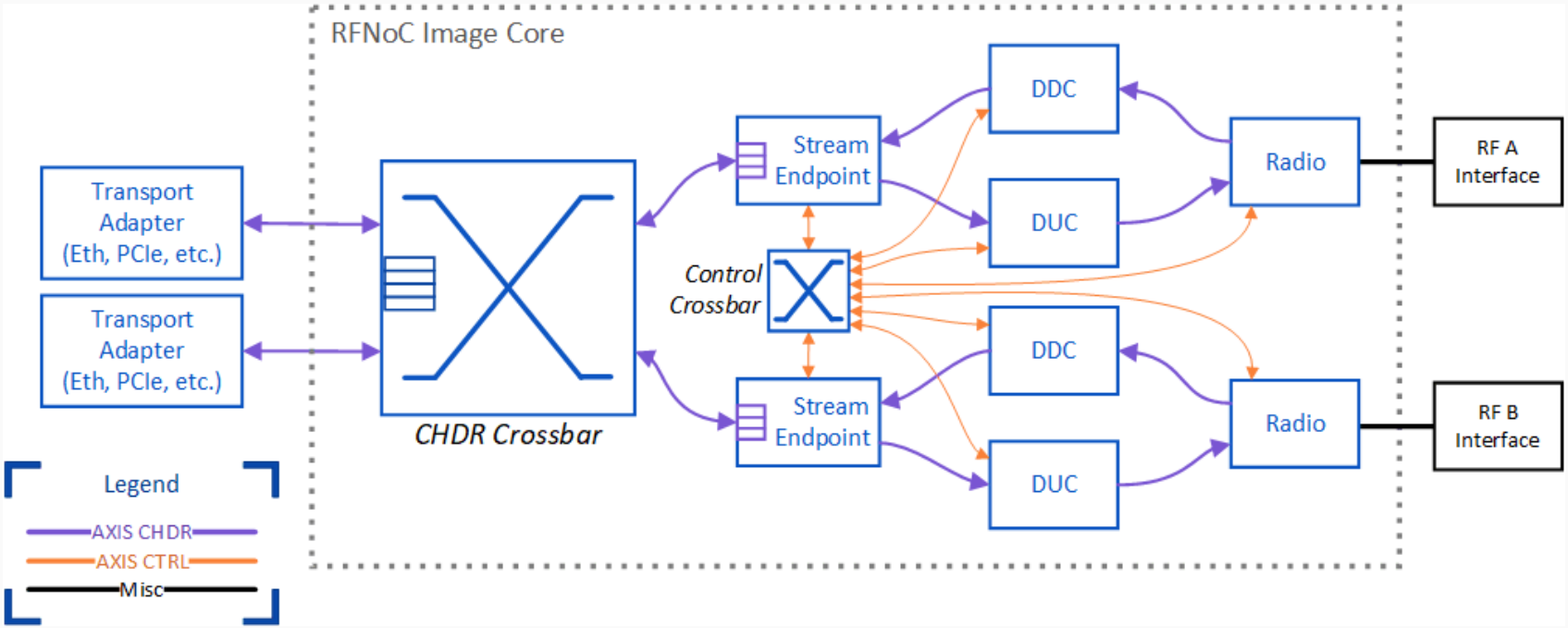

Figure 3: RFNoC Block Diagram

Tool chain and programming environment

Tool chain proposed by Ettus Research

- Ettus suggest the following tool chain to program the USRP X310:
- It includes:
  - **UHD**: to control the USRP device and stream data.
  - **RFNoC**: to create FPGA blocks and connect them.
  - **Xilinx Vivado** 2021.1 with AR76780 patch: to compile the FPGA image.
  - Optional **GNU Radio**: to create the signal processing flow.
- Ubuntu 20.04 recommended, with a lot of dependencies.
- All on the same computer.

Toolchain in practice

- What we have now:
  - **UHD 4.1.0.5** installed on RX computers.
  - **Vivado 2022.1** installed on workstation.
- What we need to do:
  - Install UHD on workstation to be able to compile the FPGA image (and all its dependencies)
  - Update UHD on RX computers to the latest version (have common version on all computers).
  - Check if the AR76780 patch is needed for Vivado 2022.1.

Next steps

Next steps

1. Install / Update software on all computers.
2. Update the FPGA image on the USRP X310 with the latest one.
3. Check toolchain
4. Continue with RFNoC tutorials to compile and run the examples.
5. Start developing the custom blocks needed for this TFE.

INFO poster session

- The poster session will take place on **December 4**.
- Deadline on **November 27** to send the poster.
- Purpose:
  - Present the work achieved so far.
  - Present topic and plan for this year.