
Name **SID #**

EEM16/CSM51A (Fall 2017)

Logic Design of Digital Systems

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Design lab 2 Hints and FAQs | **Assigned Wednesday Nov. 8, 2017 due 4pm Wednesday Nov. 22, 2017**

2 Lab assignment 2

2.2 Input de-serializer

2.2(a). An example timing diagram demonstrating what the output values may look like is shown in Fig. 1 below. For this example, `` `THRESHOLD = 2 ``: durations spanning more than 2 rising edges of the clock count as "long", while durations spanning 2 rising edges or fewer do not. The red XXX values are unspecified; you can assign values during those times however you'd like.

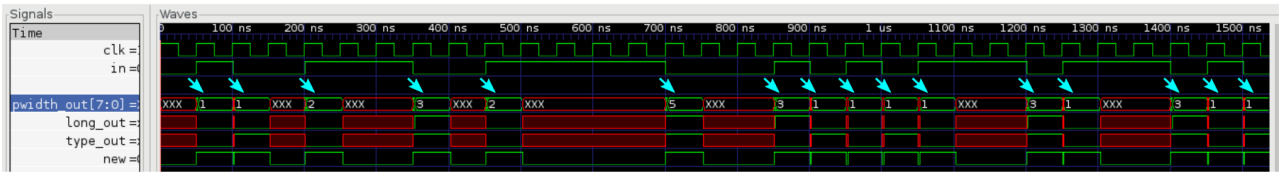

Figure 1: Example timing diagram for Lab 2 problem 2.2(a)

2.2(b). You may create additional commands if they would be helpful. For example, you may want to add a command UPDATE: replace the value in the lowest register with the input value.

Also, you may use procedural Verilog (e.g. a `case` statement) here, provided it obeys the rules to resolve into combinational logic.

2.2(c). You may or may not need all of the outputs generated in problem 2.2(a). You may also use procedural Verilog here, provided it obeys the rules to resolve into combinational logic.