
Name **SID #**

EEM16/CSM51A (Fall 2017)

Logic Design of Digital Systems

Prof. Ankur Mehta : mehtank@ucla.edu

Problem set 3 | **Assigned Monday Nov. 6, 2017**
Show all work. | **due 4pm Monday Nov. 13, 2017**

Instructions

This homework is to be done individually. You may consult with others to share thoughts and ideas, but all of your submitted work must be yours alone. Be sure to indicate with whom you've collaborated and in what manner.

You may use any tools or refer to published papers, books, or course notes. You're allowed to make use of online tools such as Logisim, WolframAlpha, etc., provided you properly cite them in the space below.

You must submit this cover sheet plus all pages of your solutions based on the procedure below. Please write clearly and neatly — if we cannot easily decipher what you have written, you will get zero credit.

Submission procedure

You need to submit your solution online at Gradescope:

`https://gradescope.com/`

Please see the following guide from Gradescope for submitting homework. You will need to upload a PDF and mark where each question is answered.

`http://gradescope-static-assets.s3-us-west-2.amazonaws.com/help/submitting_hw_guide.pdf`

Collaborators

Identify with whom you've collaborated and in what manner, if any.

Online resources

Identify which online tools you've used, if any.

1 SR latch (8+2 pts)

Consider the non-combinational circuit seen below, known as an SR latch, with inputs S, R and outputs Q, Q'. Assume both NOR gates have identical contamination and propagation delays t_{CD}, t_{PD} respectively, and note that the two diagonal wires do not connect to each other.

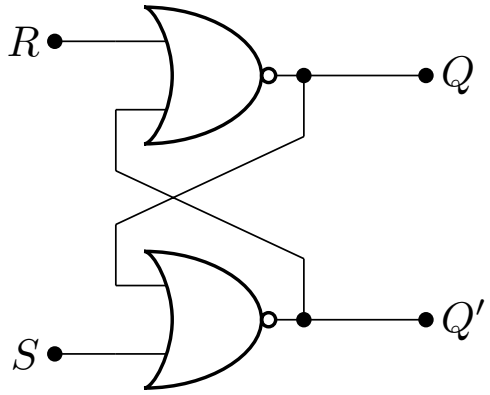

Figure 1: SR latch

1.0(a). (4 pts) Assume an initial condition for all $t < 0$ of $S = R = Q = 0; Q' = 1$, and $t_{CD} = 1, t_{PD} = 2$. Draw a complete timing diagram for the following sequence of levels:

- @$t = 0$: $S \to 1$
- @$t = 5$: $S \to 0$
- @$t = 10$: $R \to 1$
- @$t = 15$: $R \to 0$

1.0(b). (4 pts) This is called an SR latch because a high value on the S input *sets* the output Q to 1, while a high value on the R input *resets* the output Q to 0; Q' is the inverse of (NOT) Q. (What happens when both S and R are low?) Define a dynamic discipline for this latch to ensure exactly this behavior.

1.0(c). (EXTRA CREDIT 2 pts) Recall from lecture that the D latch takes two inputs D, G; the output Q follows D when G is high, and holds its value when G is low. Build a D latch from an SR latch and any additional CMOS gates, and draw the resulting gate diagram.

2 Multiplier (15+3 pts)

Consider two 4-bit unsigned inputs $A = A_3A_2A_1A_0, B = B_3B_2B_1B_0$. Recall that their product can be written as the sum of partial products:

$$AB = B_3 \cdot A \cdot 2^3 + B_2 \cdot A \cdot 2^2 + B_1 \cdot A \cdot 2^1 + B_0 \cdot A \cdot 2^0 = B_3 \cdot (A \cdot 2^3) + B_2 \cdot (A \cdot 2^2) + B_1 \cdot (A \cdot 2^1) + B_0 \cdot (A \cdot 2^0).$$

2.0(a). (5 pts) Assume A and B have been loaded into D-registers. Sequentially generate each partial product by generating the lowest order partial product, then shifting A and B appropriately to load into their respective registers for the next clock cycle. Draw this circuit, built with any CMOS gates or muxes, along with the two D-registers. What width do these registers need to be?

2.0(b). (5 pts) Add to the above an accumulator, storing the running sum of the partial products in another D-register. You may use a ripple carry adder block.

2.0(c). (2 pts) Add to the above a one-bit output indicating when the complete product has been generated. You may use any CMOS gates or muxes.

2.0(d). (3 pts) Write out the timing constraints that must be met for this sequential system to be valid, in terms of t_{CD} and t_{PD} of each module in your circuit along with t_{SETUP} and t_{HOLD} of the D-registers.

2.0(e). (EXTRA CREDIT 3 pts) Add to the above a one-bit reset input and two 4-bit inputs for A and B, zeroing out the accumulator as well as loading A and B into their respective registers when the reset input is high. You may use any CMOS gates or muxes.

3 Vowel decoder (15 pts)

The relative frequencies of the vowels in the english language are (approximately) as follows[1]:

- `A` = 20%
- `E` = 32%
- `I` = 17%
- `O` = 19%
- `U` = 7%
- `Y` = 5%

3.0(a). (2 pts) Come up with a variable-width Huffman encoding for these vowels, as well as an n-bit fixed-width binary encoding *(what is n?)*. Make sure the n-bit label n'b0 is not assigned to any value in the fixed-width encoding.

3.0(b). (3 pts) Draw a state diagram for a Moore FSM decoder that has a one-bit input stream of Huffman-encoded vowels, and generates the n-bit binary encoded output when a complete variable-width code has been received, or n'b0 otherwise.

3.0(c). (3 pts) Draw a state diagram for a Mealy FSM decoder that has a one-bit input stream of Huffman-encoded vowels, and generates the n-bit binary encoded output when a complete variable-width code has been received, or n'b0 otherwise.

3.0(d). (2 pts) Draw the state transition table for the Mealy decoder of part 3.0(c), labeling each state with a binary value.

3.0(e). (5 pts) Implement the Mealy decoder of part 3.0(c) using a D-register to hold the current state, a D-register to gate the input, and muxes to generate the next state and output values.

4 Your turn (12 pts)

It's often said that you don't truly understand a subject until you can teach it. What was a topic that you struggled with so far in this class? Write and solve a pset problem that sheds light on this particular topic.

[1] `https://en.wikipedia.org/wiki/Letter_frequency#Relative_frequencies_of_letters_in_the_English_language`