Verilog Getting Started (v170428)

1. Software: There are many different ways to run this. Details for each is provided in different sections below.

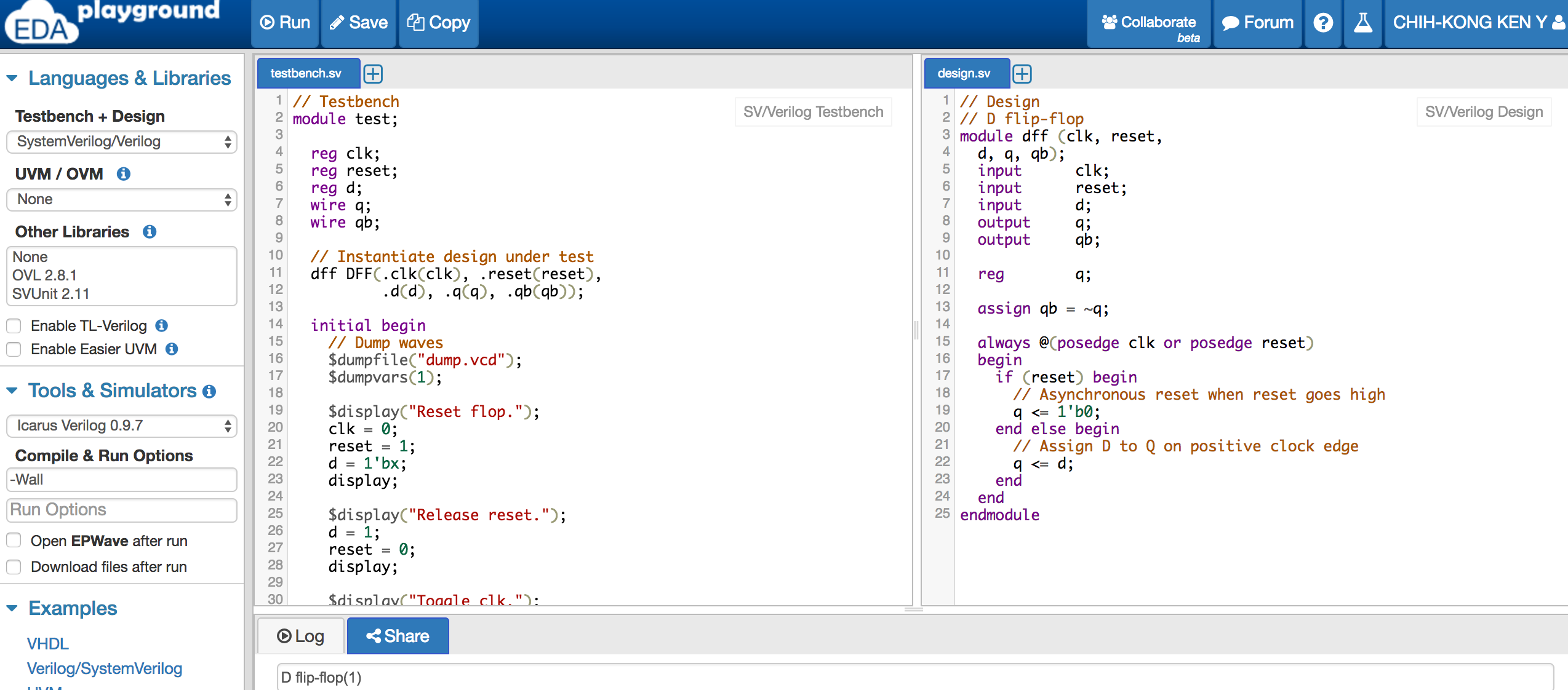
* Web interface: <https://www.edaplayground.com/>
* (Optional) Download: The version we are using is from <http://iverilog.icarus.com/> v0.9.7
* Instructions for downloading and installing for all kinds of platforms can be found in a nice wiki site: <http://iverilog.wikia.com/wiki/Installation_Guide>
* For Windows, a nice executable exists: <http://bleyer.org/icarus/>
* Unfortunately, this packaging does not exist for Macs. I can provide a virtual machine for you to run… albeit a little slower.

1. Guides and resources: There are tons of guides on Verilog and all says basically the same thing

* <http://www.doulos.com/knowhow/verilog_designers_guide/>

1. Using EDA Playground

* **Log in**: you can use your Google account to log in. This will enable you to save and download your work. If you choose, you can create a separate username but it is not necessary. *This step is very important. Because this is a web interface, periodically, there can be a connection issue and an error such as* ***“failed to connect to server”*** *may appear. Refreshing will reconnect but you may lose your work if you do not have an account.*



* Settings:
* LHS: Choose SystemVerilog/Verilog (we wont be using the SystemVerilog)
  + Don’t enable TL-Verilog, or any verification methodologies (OVM or UVM)
* LHS: Choose Icarus Verilog 0.9.7
* LHS: Run Option of “Open EPWave after run” will display the timing waveforms, and “Download files after run” will save your files locally (for submission).
* Examples:Verilog/SystemVerilog contain a D flip-flop example design. Load that design (as shown above).
* Convention in Verilog is to use at least 2 files, a testbench, and a design. The files are generally named with an extension of .v or a .sv. We will use .v in this class. To demark a testbench, we usually end the filename with .tb.
  + LHS: Select the dialog box: “Open EPWave after run”
  + TopLHS: Run the design by clicking on the “Run” button and a new window with the simulation result will pop up.
* To use **your own filenames** instead of the provided “testbench.sv” and “design.sv”,
  + Locate **Compile and Run Options**
  + After –Wall, type in your complete filename such as dassign1\_1.v and dassign1\_1.tb.
  + The simulation will include those files (you can leave the testbench.sv and design.sv blank)

1. Packaging the submission

* Download your files
* LHS: Select the dialog box: “Download files after run”
* Make sure that your file names match the desired format for the submission for proper grading. The design assignments will contain the appropriate details.