Lab 1 DSD F16

1. Continue the Tutorial Project from Xilinx and finish all parts of the tutorial:

   Note whether you have the NEXYs4 DDR or the NEXYs . Refer to the Constaint *.XDC file for your board. This is only a problem when you assign the pins. One of the steps in the tutorial has you assign the pin in the TCL Command Window, make sure to use the right pin for the right board.

   Today should generate bi t file and program the device.

2. If you have extra time, load in a new Verilog file or modify old one and implement the following:

   a. 3 input Nand Gate

   b. 3 input Nor gate

   c. 3 input XOR

Implement with combinational statements and use both logical and bitwise operators.

Answer the following questions:

1. What window do you use to work through the steps in the design flow?
   The Flow Navigator

2. How do you see the schematic?
   RTL Analysis -> Open Elaborated Design

3. What drives the timing signals in the waveform window?
   The input changes and the inherent propagation delays within the logic itself. You can add propagation delays for simulation purposes with "#time".

4. What is the Chip and board we are using for our DSD Labs
   Artix-7 FPGA on the Nexys 4 board

5. What language was out test bench written in?
   Verilog

6. What do we call the thing being simulated in test bench
   Design Under Test (DUT)

7. After you load the bit file into the NEXYS4 Board, what happens when you press the program button? Explain:

The bit file is loaded into FPGA and configures itself based on the design. Once configured it executes the programed logic.