



## 1. Description

### 1.1. Project

Project Name	vfdn_autopp_controller
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	04/21/2022

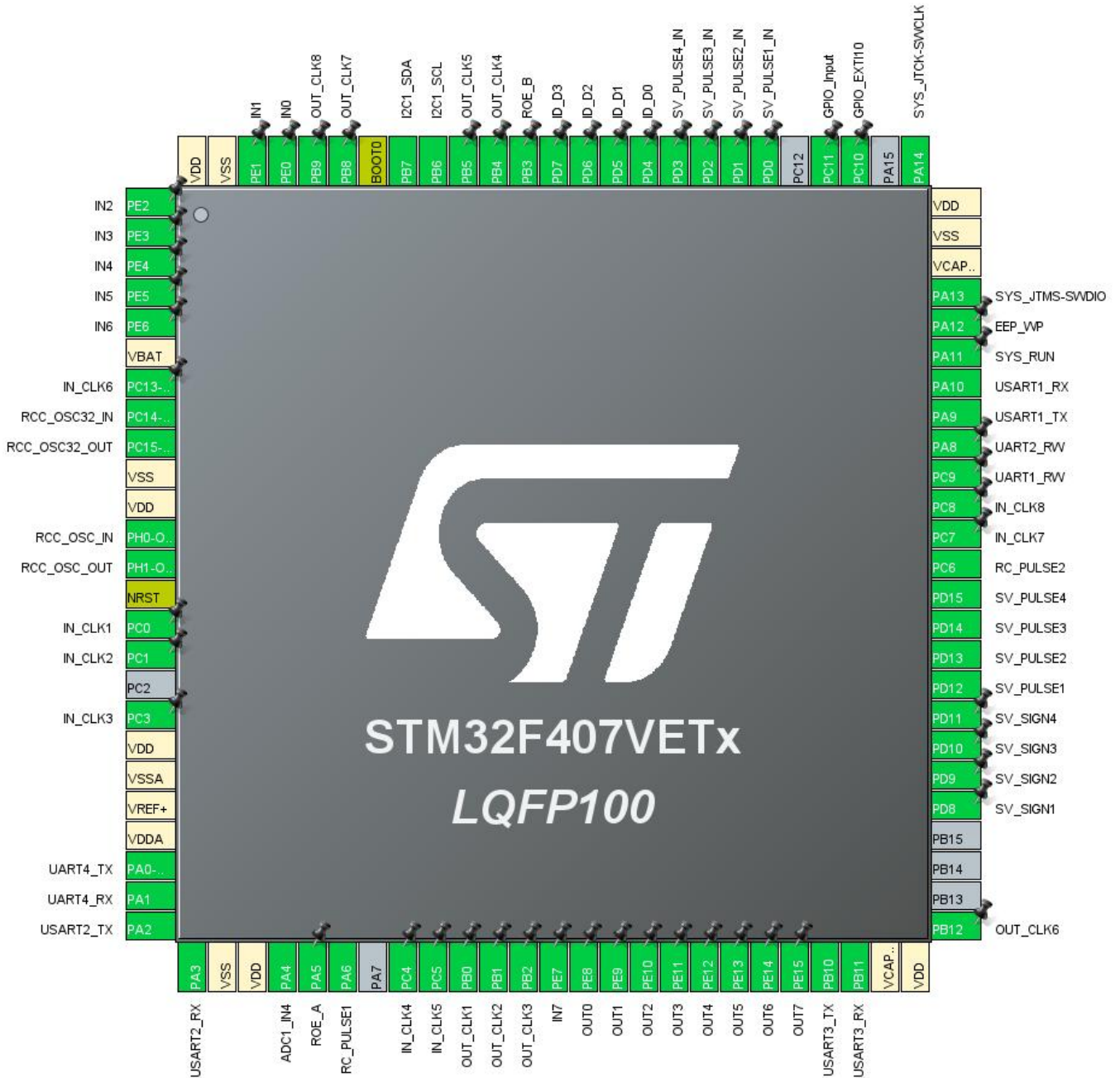
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	IN2
2	PE3 *	I/O	GPIO_Input	IN3
3	PE4 *	I/O	GPIO_Input	IN4
4	PE5 *	I/O	GPIO_Input	IN5
5	PE6 *	I/O	GPIO_Input	IN6
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Output	IN_CLK6
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	IN_CLK1
16	PC1 *	I/O	GPIO_Output	IN_CLK2
18	PC3 *	I/O	GPIO_Output	IN_CLK3
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	UART4_TX	
24	PA1	I/O	UART4_RX	
25	PA2	I/O	USART2_TX	
26	PA3	I/O	USART2_RX	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	GPIO_EXTI5	ROE_A
31	PA6	I/O	TIM3_CH1	RC_PULSE1
33	PC4 *	I/O	GPIO_Output	IN_CLK4
34	PC5 *	I/O	GPIO_Output	IN_CLK5
35	PB0 *	I/O	GPIO_Output	OUT_CLK1
36	PB1 *	I/O	GPIO_Output	OUT_CLK2
37	PB2 *	I/O	GPIO_Output	OUT_CLK3
38	PE7 *	I/O	GPIO_Output	IN7

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PE8 *	I/O	GPIO_Output	OUT0
40	PE9 *	I/O	GPIO_Output	OUT1
41	PE10 *	I/O	GPIO_Output	OUT2
42	PE11 *	I/O	GPIO_Output	OUT3
43	PE12 *	I/O	GPIO_Output	OUT4
44	PE13 *	I/O	GPIO_Output	OUT5
45	PE14 *	I/O	GPIO_Output	OUT6
46	PE15 *	I/O	GPIO_Output	OUT7
47	PB10	I/O	USART3_TX	
48	PB11	I/O	USART3_RX	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	OUT_CLK6
55	PD8 *	I/O	GPIO_Output	SV_SIGN1
56	PD9 *	I/O	GPIO_Output	SV_SIGN2
57	PD10 *	I/O	GPIO_Output	SV_SIGN3
58	PD11 *	I/O	GPIO_Output	SV_SIGN4
59	PD12	I/O	TIM4_CH1	SV_PULSE1
60	PD13	I/O	TIM4_CH2	SV_PULSE2
61	PD14	I/O	TIM4_CH3	SV_PULSE3
62	PD15	I/O	TIM4_CH4	SV_PULSE4
63	PC6	I/O	TIM8_CH1	RC_PULSE2
64	PC7 *	I/O	GPIO_Output	IN_CLK7
65	PC8 *	I/O	GPIO_Output	IN_CLK8
66	PC9 *	I/O	GPIO_Output	UART1_RW
67	PA8 *	I/O	GPIO_Output	UART2_RW
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11 *	I/O	GPIO_Output	SYS_RUN
71	PA12 *	I/O	GPIO_Output	EEP_WP
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	GPIO_EXTI10	
79	PC11 *	I/O	GPIO_Input	
81	PD0	I/O	GPIO_EXTI0	SV_PULSE1_IN
82	PD1	I/O	GPIO_EXTI1	SV_PULSE2_IN

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
83	PD2	I/O	GPIO_EXTI2	SV_PULSE3_IN
84	PD3	I/O	GPIO_EXTI3	SV_PULSE4_IN
85	PD4 *	I/O	GPIO_Input	ID_D0
86	PD5 *	I/O	GPIO_Input	ID_D1
87	PD6 *	I/O	GPIO_Input	ID_D2
88	PD7 *	I/O	GPIO_Input	ID_D3
89	PB3 *	I/O	GPIO_Input	ROE_B
90	PB4 *	I/O	GPIO_Output	OUT_CLK4
91	PB5 *	I/O	GPIO_Output	OUT_CLK5
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Output	OUT_CLK7
96	PB9 *	I/O	GPIO_Output	OUT_CLK8
97	PE0 *	I/O	GPIO_Input	IN0
98	PE1 *	I/O	GPIO_Input	IN1
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	vfdn_autopp_controller
Project Folder	D:\work\V2_211230
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_I2C1_Init	I2C1
5	MX_RTC_Init	RTC
6	MX_TIM2_Init	TIM2
7	MX_TIM3_Init	TIM3
8	MX_TIM4_Init	TIM4
9	MX_TIM8_Init	TIM8
10	MX_UART4_Init	UART4
11	MX_USART1_UART_Init	USART1



Rank	Function Name	Peripheral Instance Name
12	MX_USART2_UART_Init	USART2
13	MX_USART3_UART_Init	USART3

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	DS8626_Rev8

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

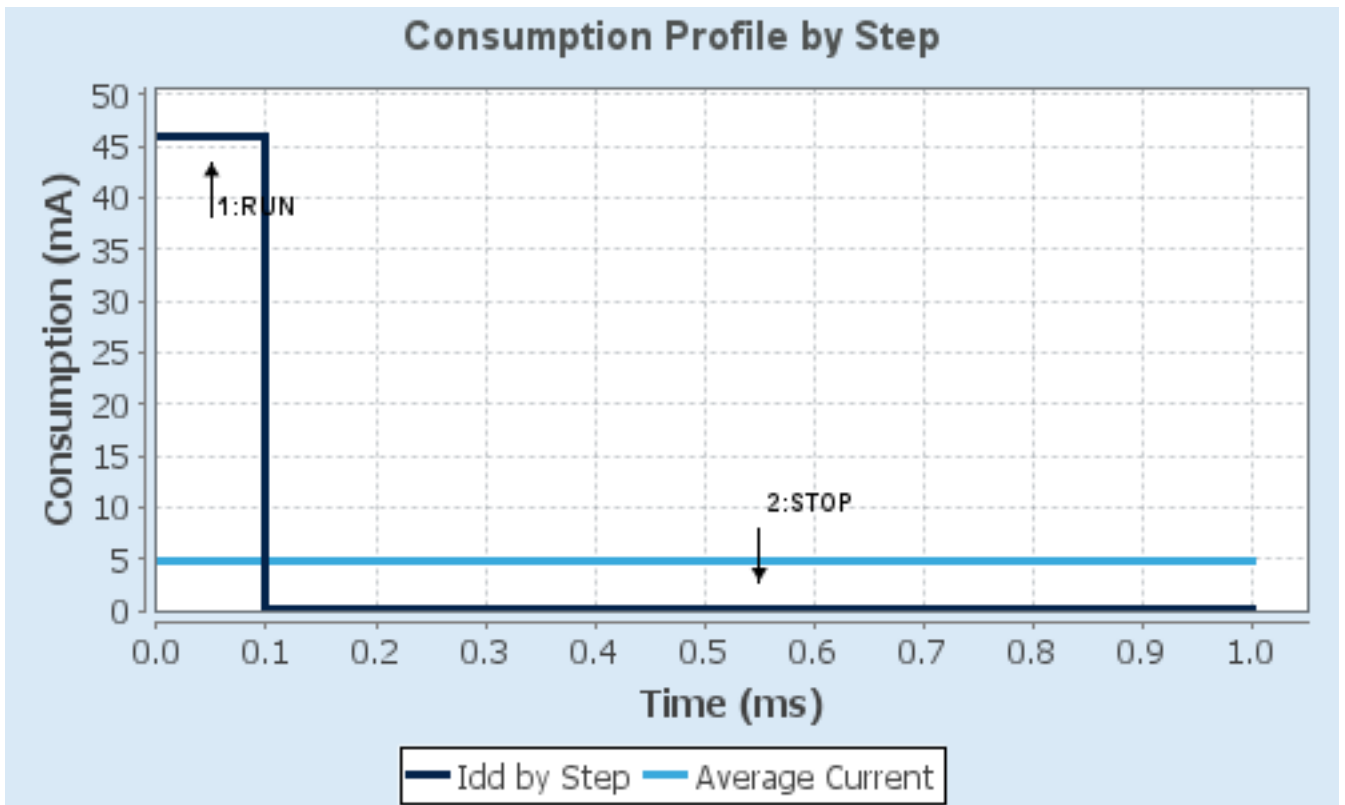
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	168 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	280 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	210.0	0.0
<b>Ta Max</b>	98.47	104.96
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

**mode: IN4**

#### 7.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler

**PCLK2 divided by 8 \***

Resolution

12 bits (15 ADC Clock cycles)

Data Alignment

Right alignment

Scan Conversion Mode

Disabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Disabled

End Of Conversion Selection

EOC flag at the end of single channel conversion

##### **ADC\_Regular\_ConversionMode:**

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 4

Sampling Time

3 Cycles

##### **ADC\_Injected\_ConversionMode:**

Number Of Conversions

0

##### **WatchDog:**

Enable Analog WatchDog Mode

false

### 7.2. I2C1

**I2C: I2C**

#### 7.2.1. Parameter Settings:

##### **Master Features:**

I2C Speed Mode

Standard Mode

I2C Clock Speed (Hz)

100000

##### **Slave Features:**

Clock No Stretch Mode

Disabled

Primary Address Length selection

7-bit

Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

### 7.3. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

#### 7.3.1. Parameter Settings:

##### **System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

##### **RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

##### **Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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### 7.4. RTC

**mode: Activate Clock Source**

**mode: Activate Calendar**

#### 7.4.1. Parameter Settings:

##### **General:**

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

##### **Calendar Time:**

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None

Store Operation                      Storeoperation Reset

**Calendar Date:**

Week Day	<b>Wednesday *</b>
Month	<b>December *</b>
Date	1
Year	<b>21 *</b>

## 7.5. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 7.6. TIM2

**Clock Source : Internal Clock**

### 7.6.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

## 7.7. TIM3

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

### 7.7.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>71 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.8. TIM4

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.8.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>71 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	<b>Low *</b>

### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable



CH Polarity **Low \***

### PWM Generation Channel 3:

Mode PWM mode 1  
Pulse (16 bits value) 0  
Output compare preload Enable  
Fast Mode Disable  
CH Polarity **Low \***

### PWM Generation Channel 4:

Mode PWM mode 1  
Pulse (16 bits value) 0  
Output compare preload Enable  
Fast Mode Disable  
CH Polarity **Low \***

## 7.9. TIM8

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

### 7.9.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value) 0  
Counter Mode Up  
Counter Period (AutoReload Register - 16 bits value ) 65535  
Internal Clock Division (CKD) No Division  
Repetition Counter (RCR - 8 bits value) 0  
auto-reload preload Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)  
Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### Break And Dead Time management - BRK Configuration:

BRK State Disable  
BRK Polarity High

#### Break And Dead Time management - Output Configuration:

Automatic Output State Disable  
Off State Selection for Run Mode (OSSR) Disable  
Off State Selection for Idle Mode (OSSI) Disable  
Lock Configuration Off

### PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## 7.10. UART4

### Mode: Asynchronous

#### 7.10.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.11. USART1

### Mode: Asynchronous

#### 7.11.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.12. USART2

### Mode: Asynchronous

#### 7.12.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.13. USART3

### Mode: Asynchronous

#### 7.13.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

\* User modified value

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	High *	RC_PULSE1
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	High *	SV_PULSE1
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	High *	SV_PULSE2
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	High *	SV_PULSE3
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	High *	SV_PULSE4
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	High *	RC_PULSE2
UART4	PA0-WKUP	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN2
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN3
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN4
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN5
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN6
	PC13- ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CLK6
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN_CLK1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN_CLK2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN_CLK3
	PA5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	<b>n/a</b>	ROE_A
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN_CLK4
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN_CLK5
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT_CLK1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT_CLK2
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT_CLK3
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	IN7
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT0
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT1
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT2
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT3
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT4
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT5
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT6
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT7
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	OUT_CLK6
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	SV_SIGN1
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	SV_SIGN2
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	SV_SIGN3
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>High</b> *	SV_SIGN4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	IN_CLK7
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	IN_CLK8
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	UART1_RW
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	UART2_RW
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	SYS_RUN
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	EEP_WP
	PC10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SV_PULSE1_IN
	PD1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SV_PULSE2_IN
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SV_PULSE3_IN
	PD3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SV_PULSE4_IN
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_D0
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_D1
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_D2
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_D3
	PB3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ROE_B
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	OUT_CLK4
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	OUT_CLK5
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	OUT_CLK7
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	OUT_CLK8
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN0
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IN1

## 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line0 interrupt	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
TIM2 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
UART4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FPU global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
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Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line0 interrupt	false	true	true
EXTI line1 interrupt	false	true	true
EXTI line2 interrupt	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM2 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
UART4 global interrupt	false	true	true

\* User modified value



## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA	ADC1 ✓	RTC ✓	I2C1 ✓			
GPIO ✓		TIM2 ✓	UART4 ✓			
NVIC ✓		TIM3 ✓	USART1 ✓			
RCC ✓		TIM4 ✓	USART2 ✓			
SYS ✓		TIM8 ✓	USART3 ✓			

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00037051.pdf">http://www.st.com/resource/en/datasheet/DM00037051.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00031020.pdf">http://www.st.com/resource/en/reference_manual/DM00031020.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00046982.pdf">http://www.st.com/resource/en/programming_manual/DM00046982.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00037591.pdf">http://www.st.com/resource/en/errata_sheet/DM00037591.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00025071.pdf">http://www.st.com/resource/en/application_note/DM00025071.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00040802.pdf">http://www.st.com/resource/en/application_note/DM00040802.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00040808.pdf">http://www.st.com/resource/en/application_note/DM00040808.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00046011.pdf">http://www.st.com/resource/en/application_note/DM00046011.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00050879.pdf">http://www.st.com/resource/en/application_note/DM00050879.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00072315.pdf">http://www.st.com/resource/en/application_note/DM00072315.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073853.pdf">http://www.st.com/resource/en/application_note/DM00073853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00081379.pdf">http://www.st.com/resource/en/application_note/DM00081379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00115714.pdf">http://www.st.com/resource/en/application_note/DM00115714.pdf</a>
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