## Using LLVM and MLIR

Quinn Pham

Adapted from slides by Braedy Kuzma, Caio Salvador Rohwedder, and Nelson Amaral

# Building

# Your Machine

#### 2.11. Installing MLIR

In the VCalc assignment and your final project you will be working with MLIR and LLVM. Due to the complex nature (and size) of MLIR we did not want to include it as a subproject. In fact, you may even want to defer the installation until you're about to start your assignment. Here are the steps to get MLIR up and running.

1. Checkout LLVM to your machine

```
$ cd $HOME
$ git clone https://github.com/llvm/llvm-project.git
$ cd llvm-project
$ git checkout llvmorg-16.0.6
```

2. Build MLIR (more details are available here)

```
$ mkdir build
$ cd build
$ cmake -G Ninja ../llvm \
    -DLLVM_ENABLE_PROJECTS=mlir \
    -DLLVM_BUILD_EXAMPLES=ON \
    -DLLVM_TARGETS_TO_BUILD="Native" \
    -DCMAKE_BUILD_TYPE=Release \
    -DLLVM_ENABLE_ASSERTIONS=ON
$ ninja check-all -j<number of threads>
```

```
export MLIR_INS="$HOME/llvm-project/build/"
export MLIR_DIR="$MLIR_INS/lib/cmake/mlir/" # Don't change me.
export PATH="$MLIR_INS/bin:$PATH" # Don't change me
```

https://cmput415.github.io/415-docs/setup/index.html

# Lab Machines

#### 5.1. Using Prebuilt Resources

Set up on the CSC machines is a lot simpler because all of the resources are managed for you. Therefore, all you need to do is to add the provided definitions to your ~/.bashrc .

# C415 Predefinitions
source "/cshome/cmput415/415-resources/415env.sh"

This should enable you to build manually using the command line. You should log out and back in so that the changes can take effect.

## MLIR

#### MLIR Language Reference

MLIR (Multi-Level IR) is a compiler intermediate representation with similarities to traditional three-address SSA representations (like LLVM IR or SIL), but which introduces notions from polyhedral loop optimization as first-class concepts. This hybrid design is optimized to represent, analyze, and transform high level dataflow graphs as well as target-specific code generated for high performance data parallel systems. Beyond its representational capabilities, its single continuous design provides a framework to lower from dataflow graphs to high-performance target-specific code.

This document defines and describes the key concepts in MLIR, and is intended to be a dry reference document - the rationale documentation, glossary, and other content are hosted elsewhere.

MLIR is designed to be used in three different forms: a human-readable textual form suitable for debugging, an in-memory form suitable for programmatic transformations and analysis, and a compact serialized form suitable for storage and transport. The different forms all describe the same semantic content. This document describes the human-readable textual form.

- High-Level Structure
- Notation
  - Common syntax
  - Top level Productions
  - Identifiers and keywords
- Dialects
  - Target specific operations
- Operations
  - Builtin Operations
- Blocks
- Regions

#### **MLIR Language Reference**

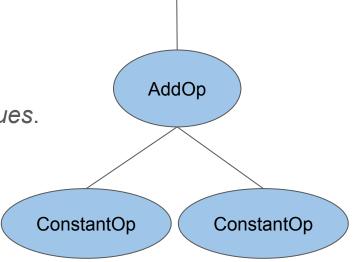
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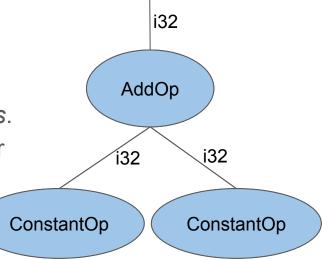
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 MLIR is based on a graph-like data structure of nodes, called *Operations*, and edges, called *Values*.

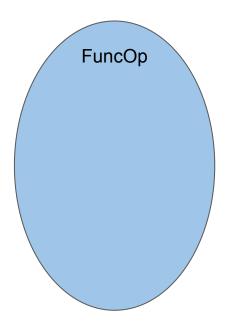


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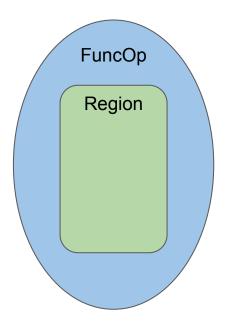
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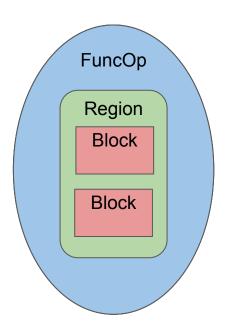
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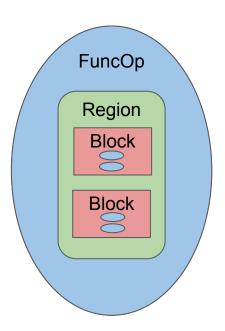
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- Operations contain Regions.



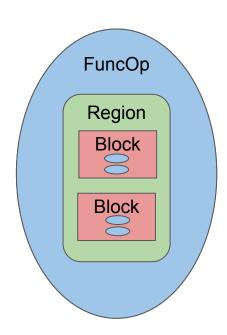
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- Regions contain <u>Blocks</u>.



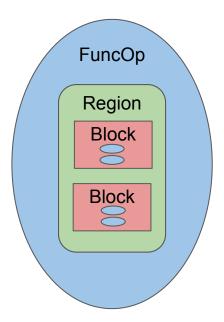
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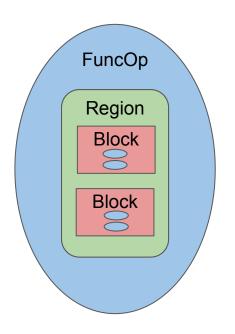
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- Each Value is the result of exactly one Operation or Block Argument, and has a *Value Type*.
- Operations contain Regions.
- Regions contain Blocks.
- Blocks contain operations.
- Operations are ordered within their containing block and Blocks are ordered in their containing region.

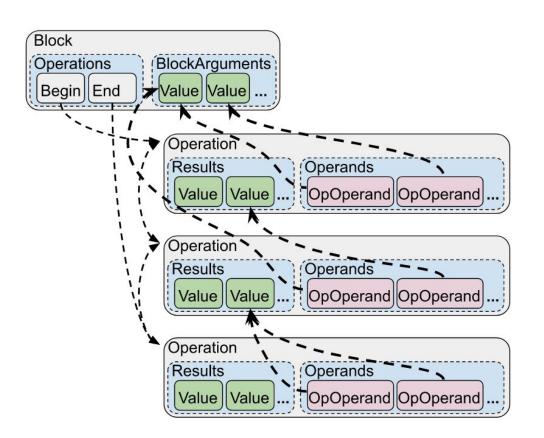


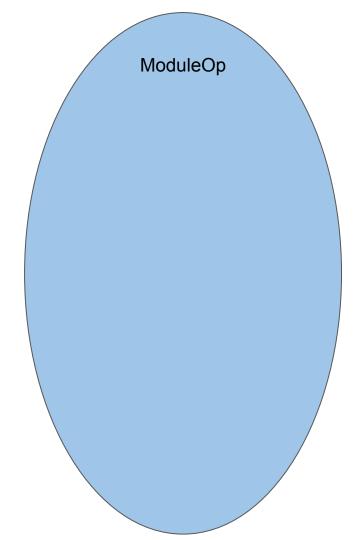
## Operations in a Block

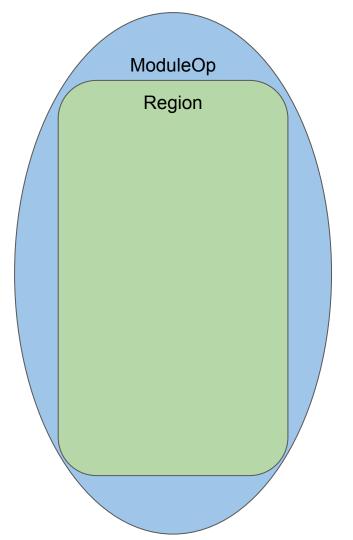


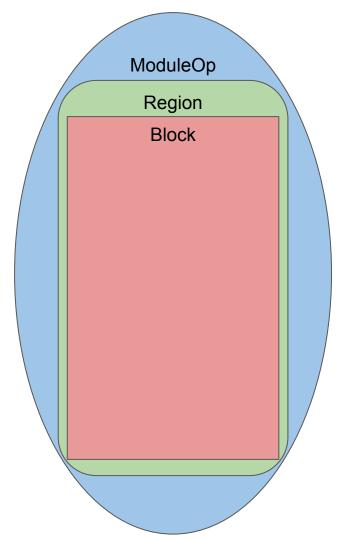
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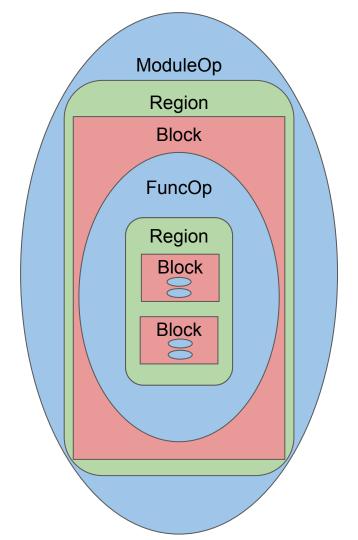












## LLVM Dialect MLIR

#### **Dialects**

This section contains documentation for core and contributed dialects available from the MLIR repository. The description for each dialect includes content automatically generated from the dialect's Definition Specification (ODS).

#### **Dialects Docs**

- 'acc' Dialect
- 'affine' Dialect
- · 'amdgpu' Dialect
- 'amx' Dialect
- · 'arith' Dialect
- · 'arm\_neon' Dialect
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- · 'async' Dialect
- 'bufferization' Dialect
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- 'index' Dialect
- 'irdl' Dialect
- · 'linalg' Dialect
- 'llvm' Dialect
- · 'math' Dialect

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#### 'llvm' Dialect

This dialect maps <u>LLVM IR</u> into MLIR by defining the corresponding operations and types. LLVM IR metadata is usually represented as MLIR attributes, which offer additional structure verification.

We use "LLVM IR" to designate the intermediate representation of LLVM and "LLVM dialect" or "LLVM IR dialect" to refer to this MLIR dialect.

Unless explicitly stated otherwise, the semantics of the LLVM dialect operations must correspond to the semantics of LLVM IR instructions and any divergence is considered a bug. The dialect also contains auxiliary operations that smoothen the differences in the IR structure, e.g., MLIR does not have phi operations and LLVM IR does not have a constant operation. These auxiliary operations are systematically prefixed with mlir, e.g. llvm.mlir.constant where llvm. is the dialect namespace prefix.

- . Dependency on LLVM IR
- Module Structure
  - Data Layout and Triple
  - Functions
  - PHI Nodes and Block Arguments
  - Context-Level Values
  - o Globals
  - Linkage
  - Attribute Pass-Through
- Types
  - Built-in Type Compatibility
  - Additional Simple Types
  - Additional Parametric Types
  - Vector Types
  - Structure Types
  - Unsupported Types
- Operations
  - llvm.ashr (LLVM::AShrOp)
  - llvm.add (LLVM::AddOp)

#### llvm.add (LLVM::AddOp) ¶

Syntax:

```
operation ::= `llvm.add` $lhs `,` $rhs custom<LLVMOpAttrs>(attr-dict) `:`
type($res)
```

Traits: AlwaysSpeculatableImplTrait, Commutative, SameOperandsAndResultType

Interfaces: ConditionallySpeculatable, InferTypeOpInterface, NoMemoryEffect (MemoryEffectOpInterface)

Effects: MemoryEffects::Effect{}

#### Operands: ¶

| Operand | Description  |
|---------|--|
| lhs     | integer or LLVM dialect-compatible vector of integer |
| rhs     | integer or LLVM dialect-compatible vector of integer |

#### Results: ¶

| Result | Description  |
|--------|--|
| res    | integer or LLVM dialect-compatible vector of integer |

https://mlir.llvm.org/docs/Dialects/LLVM/



LLVM Home | Documentation » Reference » LLVM Language Reference Manual

#### LLVM Language Reference Manual

- Abstract
- Introduction
  - Well-Formedness
- Identifiers
- · High Level Structure
  - Module Structure
  - Linkage Types
  - Calling Conventions
  - Visibility Styles
  - DLL Storage Classes
  - Thread Local Storage Models
  - Runtime Preemption Specifiers
  - Structure Types
  - o Non-Integral Pointer Type
  - Global Variables
  - Functions
  - o Aliases
  - o IFuncs
  - Comdats
  - Named Metadata
  - Parameter Attributes



#### · Instruction Reference

- · Terminator Instructions
  - · 'ret' Instruction
  - · 'br' Instruction
  - · 'switch' Instruction
  - · 'indirectbr' Instruction
  - 'invoke' Instruction
  - 'callbr' Instruction
  - · 'resume' Instruction
  - 'catchswitch' Instruction
  - 'catchret' Instruction
  - 'cleanupret' Instruction
  - 'unreachable' Instruction

#### Unary Operations

- 'fneg' Instruction
- Binary Operations
  - · 'add' Instruction
  - · 'fadd' Instruction
  - 'sub' Instruction
  - · 'fsub' Instruction
  - 'mul' Instruction
  - · 'fmul' Instruction
  - THUL INSTRUCTION
  - 'udiv' Instruction
     'sdiv' Instruction
  - · 'fdiv' Instruction
  - IUIV IIISUUCUOII
  - 'urem' Instruction
  - 'srem' Instruction
  - 'frem' Instruction

#### 'add' Instruction ¶

#### Syntax:

#### Overview:

The 'add' instruction returns the sum of its two operands.

#### Arguments:

The two arguments to the 'add' instruction must be integer or vector of integer values. Both arguments must have identical types.

#### Semantics:

The value produced is the integer sum of the two operands.

If the sum has unsigned overflow, the result returned is the mathematical result modulo  $2^n$ , where n is the bit width of the result.

Because LLVM integers use a two's complement representation, this instruction is appropriate for both signed and unsigned integers.

nuw and nsw stand for "No Unsigned Wrap" and "No Signed Wrap", respectively. If the nuw and/or nsw keywords are present, the result value of the add is a poison value if unsigned and/or signed overflow, respectively, occurs.

#### Example:

```
<result> = add i32 4, %var ; yields i32:result = 4 + %var
```

https://llvm.org/docs/LangRef.html#add-instruction

#### **Builtin Dialect**

The builtin dialect contains a core set of Attributes, Operations, and Types that have wide applicability across a very large number of domains and abstractions. Many of the components of this dialect are also instrumental in the implementation of the core IR. As such, this dialect is implicitly loaded in every MLIRContext, and available directly to all users of MLIR.

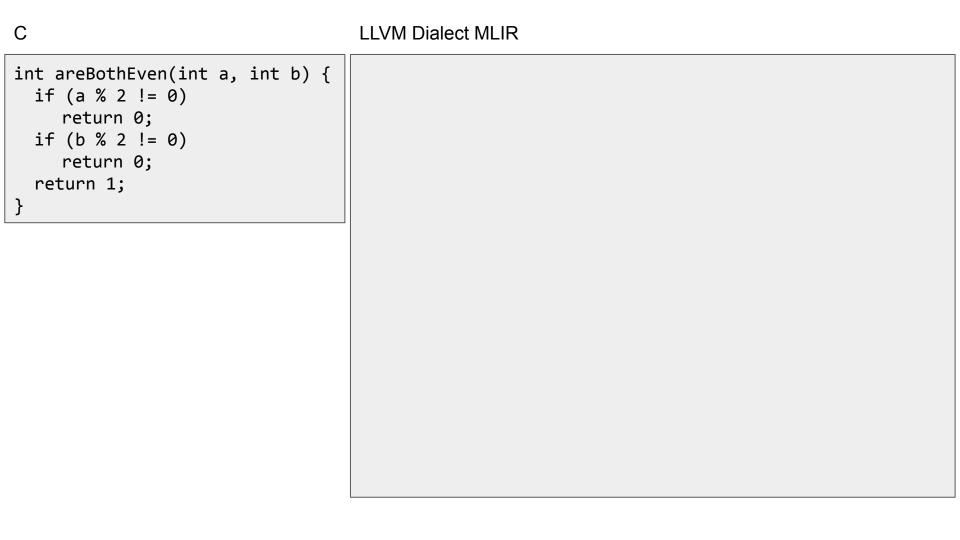
Given the far-reaching nature of this dialect and the fact that MLIR is extensible by design, any potential additions are heavily scrutinized.

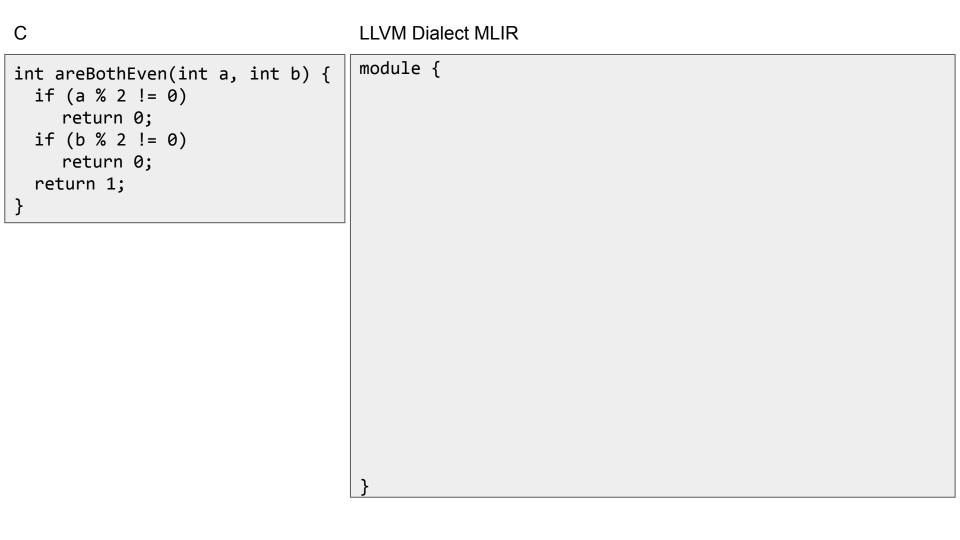
#### Attributes

- AffineMapAttr
- ArrayAttr
- DenseArrayAttr
- DenselntOrFPElementsAttr
- DenseResourceElementsAttr
- DenseStringElementsAttr
- DictionaryAttr
- FloatAttr
- IntegerAttr

# Example

```
int areBothEven(int a, int b) {
  if (a % 2 != 0)
    return 0;
  if (b % 2 != 0)
    return 0;
  return 1;
}
```





```
LLVM Dialect MLIR
                                  module {
int areBothEven(int a, int b) {
                                    llvm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
 if (a % 2 != 0)
                                       %0 = llvm.mlir.constant(0 : i32) : i32
    return 0;
                                       %1 = 11vm.mlir.constant(1 : i32) : i32
  if (b % 2 != 0)
                                       %2 = 11vm.mlir.constant(2 : i32) : i32
    return 0;
                                      %3 = 11vm.srem %arg0, %2 : i32
  return 1;
                                      %4 = llvm.icmp "ne" %3, %0 : i32
                                       llvm.cond br %4, ^bb1, ^bb2
                                    ^bb1:
                                    ^bb2:
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```

```
C
```

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                                      llvm.cond br %4, ^bb1, ^bb2
                                    ^bb1:
                                      llvm.return %0 : i32
                                    ^bb2:
                                      %5 = llvm.srem %arg1, %2 : i32
                                      %6 = llvm.icmp "ne" %5, %0 : i32
                                      11vm.cond br %6, ^bb3, ^bb4
                                    ^bb3:
                                      11vm.return %0 : i32
                                    ^bb4:
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C
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                                       llvm.cond br %4, ^bb1, ^bb2
                                    ^bb1:
                                       llvm.return %0 : i32
                                    ^bb2:
                                      %5 = llvm.srem %arg1, %2 : i32
Handwritten translation.
                                       %6 = llvm.icmp "ne" %5, %0 : i32
As far as I know, there
                                       11vm.cond br %6, ^bb3, ^bb4
is no complete reliable C
                                    ^bb3:
front end for MLIR.
                                       11vm.return %0 : i32
                                    ^bb4:
                                       llvm.return %1 : i32
```

```
module {
  11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
     %0 = llvm.mlir.constant(0 : i32) : i32
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     %3 = 11vm.srem %arg0, %2 : i32
     %4 = llvm.icmp "ne" %3, %0 : i32
     llvm.cond br %4, ^bb1, ^bb2
  ^bb1:
     11vm.return %0 : i32
  ^bb2:
     %5 = llvm.srem %arg1, %2 : i32
     %6 = llvm.icmp "ne" %5, %0 : i32
     11vm.cond br %6, ^bb3, ^bb4
  ^bb3:
     11vm.return %0 : i32
 ^bb4:
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define i32 @areBothEven(i32 %0, i32 %1) {
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                                                      %3 = 11vm.srem %arg0, %2 : i32
                                                      %4 = llvm.icmp "ne" %3, %0 : i32
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                                                  ^bb1:
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                                                  ^bb3:
                                                      11vm.return %0 : i32
                                                  ^bb4:
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```

```
module {
define i32 @areBothEven(i32 %0, i32 %1) {
                                                  11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
 %3 = srem i32 \%0, 2
                                                      %0 = llvm.mlir.constant(0 : i32) : i32
                                                      %1 = llvm.mlir.constant(1 : i32) : i32
                                                      %2 = llvm.mlir.constant(2 : i32) : i32
                                                      %3 = 11vm.srem %arg0, %2 : i32
                                                      %4 = llvm.icmp "ne" %3, %0 : i32
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                                                  ^bb1:
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                                                  ^bb2:
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                                                      %6 = llvm.icmp "ne" %5, %0 : i32
                                                      11vm.cond br %6, ^bb3, ^bb4
                                                  ^bb3:
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 %3 = srem i32 \%0, 2
                                                      %0 = llvm.mlir.constant(0 : i32) : i32
 %4 = icmp ne i32 %3, 0
                                                      %1 = llvm.mlir.constant(1 : i32) : i32
                                                      %2 = llvm.mlir.constant(2 : i32) : i32
                                                      %3 = 11vm.srem %arg0, %2 : i32
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                                                      %6 = llvm.icmp "ne" %5, %0 : i32
                                                      11vm.cond br %6, ^bb3, ^bb4
                                                   ^bb3:
                                                      11vm.return %0 : i32
                                                  ^bb4:
                                                      llvm.return %1 : i32
```

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                                                   11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
 %3 = srem i32 \%0, 2
                                                      %0 = llvm.mlir.constant(0 : i32) : i32
 %4 = icmp ne i32 %3, 0
                                                      %1 = llvm.mlir.constant(1 : i32) : i32
 br i1 %4, label %5, label %6
                                                      %2 = llvm.mlir.constant(2 : i32) : i32
5:
                                                      %3 = 11vm.srem %arg0, %2 : i32
                                                      %4 = llvm.icmp "ne" %3, %0 : i32
6:
                                                      llvm.cond br %4, ^bb1, ^bb2
                                                   ^bb1:
                                                      llvm.return %0 : i32
                                                   ^bb2:
                                                      %5 = llvm.srem %arg1, %2 : i32
                                                      %6 = llvm.icmp "ne" %5, %0 : i32
                                                      11vm.cond br %6, ^bb3, ^bb4
                                                   ^bb3:
                                                      11vm.return %0 : i32
                                                   ^bb4:
                                                      llvm.return %1 : i32
```

```
module {
define i32 @areBothEven(i32 %0, i32 %1) {
                                                   11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
 %3 = srem i32 \%0, 2
                                                      %0 = llvm.mlir.constant(0 : i32) : i32
 %4 = icmp ne i32 %3, 0
                                                      %1 = llvm.mlir.constant(1 : i32) : i32
 br i1 %4, label %5, label %6
                                                      %2 = 11vm.mlir.constant(2 : i32) : i32
5:
                                                      %3 = 11vm.srem %arg0, %2 : i32
 ret i32 0
                                                      %4 = llvm.icmp "ne" %3, %0 : i32
6:
                                                      llvm.cond br %4, ^bb1, ^bb2
                                                   ^bb1:
                                                      llvm.return %0 : i32
                                                   ^bb2:
                                                      %5 = llvm.srem %arg1, %2 : i32
                                                      %6 = llvm.icmp "ne" %5, %0 : i32
                                                      11vm.cond br %6, ^bb3, ^bb4
                                                   ^bb3:
                                                      11vm.return %0 : i32
                                                   ^bb4:
                                                      llvm.return %1 : i32
```

9:

10:

ret i32 0

```
define i32 @areBothEven(i32 %0, i32 %1) {
    %3 = srem i32 %0, 2
    %4 = icmp ne i32 %3, 0
    br i1 %4, label %5, label %6
5:
    ret i32 0
6:
    %7 = srem i32 %1, 2
    %8 = icmp ne i32 %7, 0
    br i1 %8, label %9, label %10
```

```
module {
 11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
     %0 = llvm.mlir.constant(0 : i32) : i32
     %1 = 11vm.mlir.constant(1 : i32) : i32
     %2 = 11vm.mlir.constant(2 : i32) : i32
     %3 = 11vm.srem %arg0, %2 : i32
     %4 = llvm.icmp "ne" %3, %0 : i32
     llvm.cond br %4, ^bb1, ^bb2
 ^bb1:
     llvm.return %0 : i32
 ^bb2:
     %5 = llvm.srem %arg1, %2 : i32
     %6 = llvm.icmp "ne" %5, %0 : i32
     11vm.cond br %6, ^bb3, ^bb4
 ^bb3:
     11vm.return %0 : i32
 ^bb4:
     llvm.return %1 : i32
```

ret i32 0

ret i32 1

10:

```
define i32 @areBothEven(i32 %0, i32 %1) {
    %3 = srem i32 %0, 2
    %4 = icmp ne i32 %3, 0
    br i1 %4, label %5, label %6
5:
    ret i32 0
6:
    %7 = srem i32 %1, 2
    %8 = icmp ne i32 %7, 0
    br i1 %8, label %9, label %10
9:
```

```
module {
 11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
     %0 = llvm.mlir.constant(0 : i32) : i32
     %1 = 11vm.mlir.constant(1 : i32) : i32
     %2 = 11vm.mlir.constant(2 : i32) : i32
     %3 = 11vm.srem %arg0, %2 : i32
     %4 = llvm.icmp "ne" %3, %0 : i32
     llvm.cond br %4, ^bb1, ^bb2
 ^bb1:
     llvm.return %0 : i32
 ^bb2:
     %5 = llvm.srem %arg1, %2 : i32
     %6 = llvm.icmp "ne" %5, %0 : i32
     11vm.cond br %6, ^bb3, ^bb4
 ^bb3:
     11vm.return %0 : i32
 ^bb4:
     llvm.return %1 : i32
```

#### LLVM Dialect MLIR

```
module {
define i32 @areBothEven(i32 %0, i32 %1) {
 %3 = srem i32 \%0, 2
 %4 = icmp ne i32 %3, 0
  br i1 %4, label %5, label %6
5:
  ret i32 0
6:
 %7 = srem i32 %1, 2
                                                    ^bb1:
 %8 = icmp ne i32 \%7, 0
                                                        llvm.return %0 : i32
  br i1 %8, label %9, label %10
                                                    ^bb2:
9:
  ret i32 0
10:
  ret i32 1
                                                    ^bb3:
                                                        11vm.return %0 : i32
                                                    ^bb4:
```

Translated using the mlir-translate tool.

```
11vm.func @areBothEven(%arg0: i32, %arg1: i32) -> i32 {
   %0 = llvm.mlir.constant(0 : i32) : i32
   %1 = 11vm.mlir.constant(1 : i32) : i32
   %2 = 11vm.mlir.constant(2 : i32) : i32
   %3 = 11vm.srem %arg0, %2 : i32
   %4 = llvm.icmp "ne" %3, %0 : i32
   llvm.cond br %4, ^bb1, ^bb2
   %5 = llvm.srem %arg1, %2 : i32
   %6 = llvm.icmp "ne" %5, %0 : i32
   11vm.cond br %6, ^bb3, ^bb4
   llvm.return %1 : i32
```

# Tools

## **LLVM Tools**

```
clang - C front end
                                    opt - optimizer and analyzer
  .c -> .11 | .bc
                                      .11 | .bc -> .bc
llvm-dis - disassembler
                                    lli - interpreter
  .bc -> .11
                                      interpret .11 or .bc
11vm-as - assembler
                                    11c - compiler
                                      .11 | .bc -> .o
  .11 \rightarrow .bc
```

## **MLIR Tools**

```
mlir-opt - optimizer and lowerer
  optimize mlir
  lower mlir to lower level dialect
mlir-translate - translation tool
  mlir -> external representation
  external representation -> mlir
```

```
clang inFile.c -S -emit-llvm -o outFile.ll
```

See what LLVM IR clang generates.

```
clang inFile.c -S -emit-llvm -o outFile.ll
```

See what LLVM IR clang generates.

#### 1li -dlopen="pathToSharedLibrary" program.1l

Execute LLVM IR program with a dynamic library.

```
clang inFile.c -S -emit-llvm -o outFile.ll
```

See what LLVM IR clang generates.

#### 1li -dlopen="pathToSharedLibrary" program.1l

Execute LLVM IR program with a dynamic library.

#### mlir-translate inFile.llvm.mlir --mlir-to-llvmir -o outFile.ll

Translate LLVM dialect MLIR to LLVM IR.

## More Demo