RISC Processor Project Checklist
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Commitment:
Implement the 6.004 Beta processor in Verilog. This can be broken down into the following components: arithmetic logic unit, program counter, control logic, register file, and instruction and data memory. This processor should be capable of running basic programs such as merge sort.

Goal:
Implement additional RISC instructions such as the modulo % instruction.

Implement complex instructions. These instructions may involve more than one cycle on the processor to complete. An example is the *pusha* instruction which saves all registers to memory.

Add basic input output. This will allow a user to select which programs they wish to run, provide data inputs to the programs, and see the output. We plan to implement this using the seven-segment displays and the 16 switches.

Add simple optimizations to reduce clock cycle. Reducing the clock cycle from the default will improve the performance of our processor.

Stretch Goal:
Add pipelining for improved performance.

Add additional hardware components such as a memory management unit. This would allow our processor to support virtual memory.