QUINTAURIS

De la Nube a la FPGA: Introducción Práctica a RISC-V con Quintauris

Angel Berrio

Chief Product Officer

Introducción Curso

Title:
De la Nube a la FPGA: Introducción Práctica a RISC-V con Quintauris

Key Info:
- **Fechas:** 8–18 septiembre 2025
- **Lugar:** Facultad de Ciencias UGR, Granada
- **Duración:** 20 horas
- **Dirige:** Diego Pedro Morales | **Coordina:** Ángel Berrio (Quintauris)

Objetivo:
Obtener una introducción en RISC-V y su ecosistema, con un enfoque teórico-práctico.

Introducción Curso

- ~~**Lunes, 8 – 16:45 — 19:00** *Introducción a la arquitectura RISC-V: historia, filosofía y evolución.*~~
- **Martes, 9 – 16:45 — 19:00** *Ecosistema RISC-V: herramientas, comunidades, casos de uso.*
- **Miércoles, 10 – 16:45 — 19:00** *Presentación de Quintauris: visión, modelo de negocio y productos.*
- **Jueves, 11 – 16:45 — 19:00** *Exploración de la plataforma Quintauris: entorno, funcionalidades, primeros pasos.*
- **Lunes, 15 – 16:45 — 19:00** *IP hardware RISC-V Open source: introducción, licencias y repositorios.*
- **Martes, 16 – 15:00 — 17:00** Parte I: *De la nube a la FPGA: flujo de despliegue de una IP en la FPGA.*
  17:00 — 19:30 Parte II: *De la nube a la FPGA: flujo de despliegue de una IP en la FPGA.*
- **Jueves, 18 – 16:45 — 20:00** *Hackatón final: integración de conceptos y solución de un reto práctico.*

Priviledge Modes day II

From SW perspective:

By default, the processor starts in M-mode

The **booloader** or **OS** change the mode at start up:

1. Set the return program counter (*mepc*) with the address where user code will begin.
2. Change the MPP field (Machine Previous Privilege) in *mstatus* to 00 (U-mode).
3. Execute the *mret* instruction (machine return).
   - This loads *mepc* into the PC.
   - Execution mode changes to U.

```
# Setup in M-mode

la   t0, user_start          # 1. Address of user program
csrw mepc, t0

li   t1, 0
csrrs x0, mstatus, t1        # 2. clear MPP bits

mret                         # 3. Jump to user_start in U-mode
```

Priviledge Modes day II

From HW perspective:

Case: a program in **U–mode** tries to execute a privileged instruction (*csrw mtvec*, t0)

a) Status register (mstatus)

Contains the **current mode:** 2 bits indicate 00=U, 01=S, 11=M.

These bits travel through the pipeline as a **global privilege signal.**

b) Decode unit

The decoder identifies if the instruction is **privileged** (e.g., csrw mtvec).

It generates a signal: instr_privileged = 1.

c) Privilege check logic

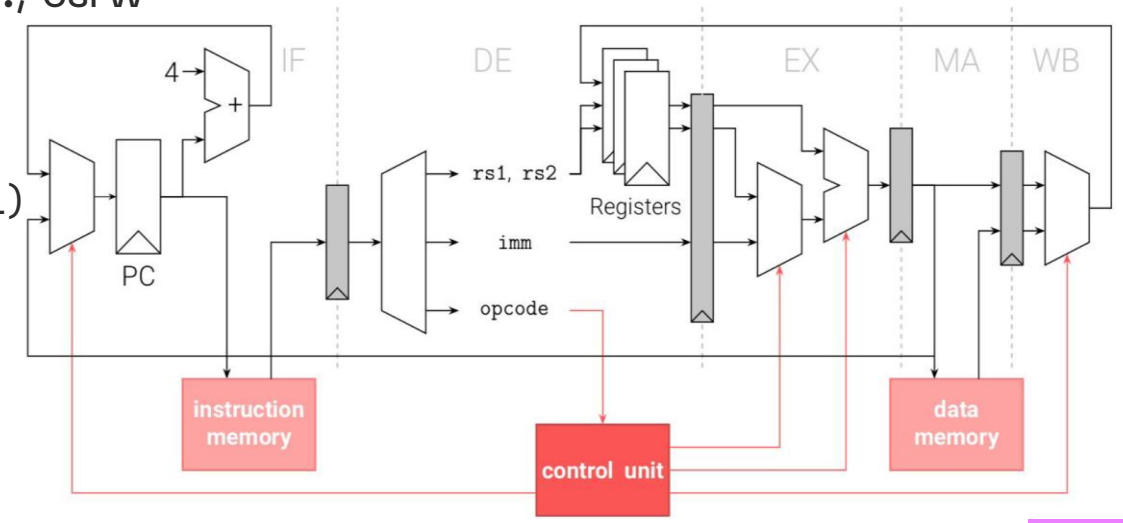
A logic gate compares allow=(priv_level >= required_level)

If allow=0, then trap_signal=1 is asserted.

d) Trap control unit

When trap_signal=1:

- The pipeline is flushed.
- The PC is loaded from *mtvec*.
- The old PC is saved into *mepc*.
- *mcause* is updated with the reason for the exception.



This is literally implemented with AND/OR gates and multiplexers.

Key takeways Day 1

- **RISC-V Basics**
  - Open, royalty-free ISA → fosters innovation & lowers costs
  - Simplicity (RISC) vs. complexity (CISC):
    efficiency through streamlined instructions

- **History & Philosophy**
  - From Berkeley projects (1980s) to today's global adoption
  - Open ISA comparable to Linux's impact on OS

- **Technical Strengths**
  - Modular instruction set
    (RV32I/RV64I base + extensions: M, F, D, C, V, Crypto, DSP)
  - Scalable: from IoT microcontrollers to HPC systems
  - Supports custom extensions for domain-specific acceleration

- **Privilege Architecture**
  - Three levels: User (U), Supervisor (S), Machine (M)
  - Optional H-extension enables virtualization

- **Non-ISA Specifications**
  - Debug, trace, RAS, QoS, profiles & platform standards
  - Ensure interoperability, reduce fragmentation, enable innovation

The RISC-V Ecosystem: Tools, Communities, and Use Cases.

Agenda

01 Introduction to RISC-V Ecosystem

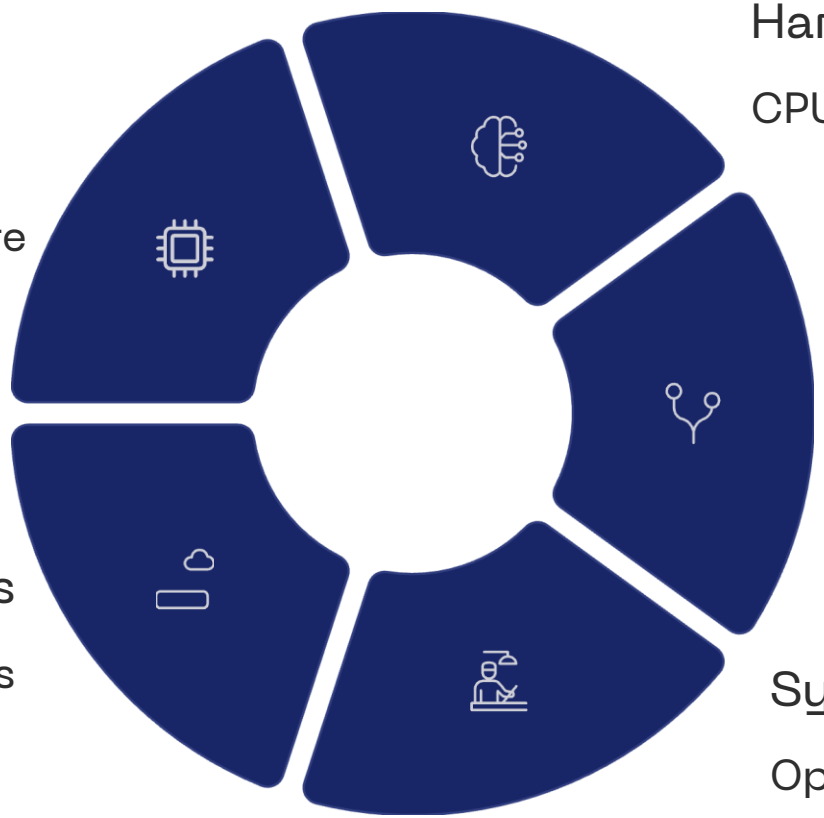
02 RISC-V International

03 RISE

04 RISC-V Market Status

The RISC-V Ecosystem

Beyond the ISA: RISC-V represents a complete ecosystem encompassing hardware, software, people, and standards that work together to enable innovation.



Hardware Cores

CPU implementations and designs

ISA Core

Instruction set architecture

Development Tools

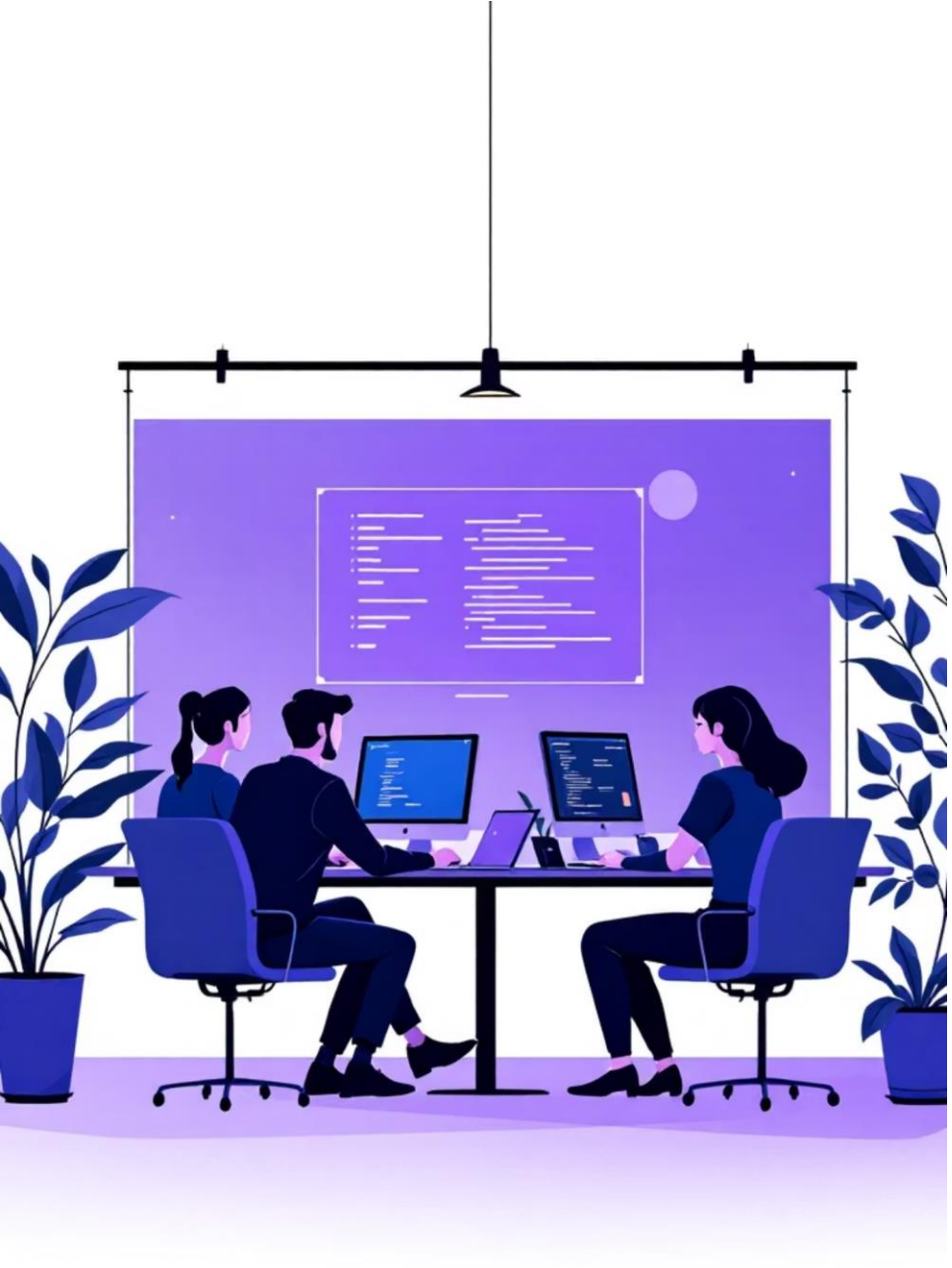
Compilers, debuggers, simulators

Applications

End-user software and use cases

System Software

Operating systems and runtime environments



Why Ecosystem Maturity Drives Success

Tools Enable Productivity

Mature toolchains, debuggers, and IDEs reduce development friction and accelerate time-to-market for embedded products.

Communities Drive Adoption

Active developer communities provide support, libraries, and knowledge sharing that make RISC-V viable for production use.

Use Cases Prove Value

Real-world implementations across IoT, automotive, and data center applications demonstrate RISC-V's commercial viability.

The ecosystem's health directly correlates with adoption rates and long-term sustainability of RISC-V investments.

RISC-V Development Stack

Complete software infrastructure for embedded development

Applications

User software and embedded applications

Operating Systems

Linux, FreeRTOS, bare metal environments

Hardware Frameworks

Chisel, SystemVerilog, FPGA tools

Debug & Simulation

GDB, Spike, QEMU, Renode

Toolchain

GCC, LLVM, compilers, linkers

Each layer builds upon the foundation below, creating a comprehensive development environment that rivals established architectures.

Compilers & Toolchains

GCC Toolchain

Complete support for RV32 and RV64 architectures with extensive optimization capabilities and mature ecosystem integration.

- Full C/C++ standard library support
- Robust optimization passes
- Newlib and glibc compatibility

LLVM/Clang

Modern compiler infrastructure with growing RISC-V support and excellent IDE integration for development workflows.

- Advanced static analysis
- IDE integration (VS Code, CLion)
- Modular architecture

Cross-compilation essentials enable development on x86 hosts while targeting RISC-V embedded systems efficiently.

Operating Systems Support

- **Linux**

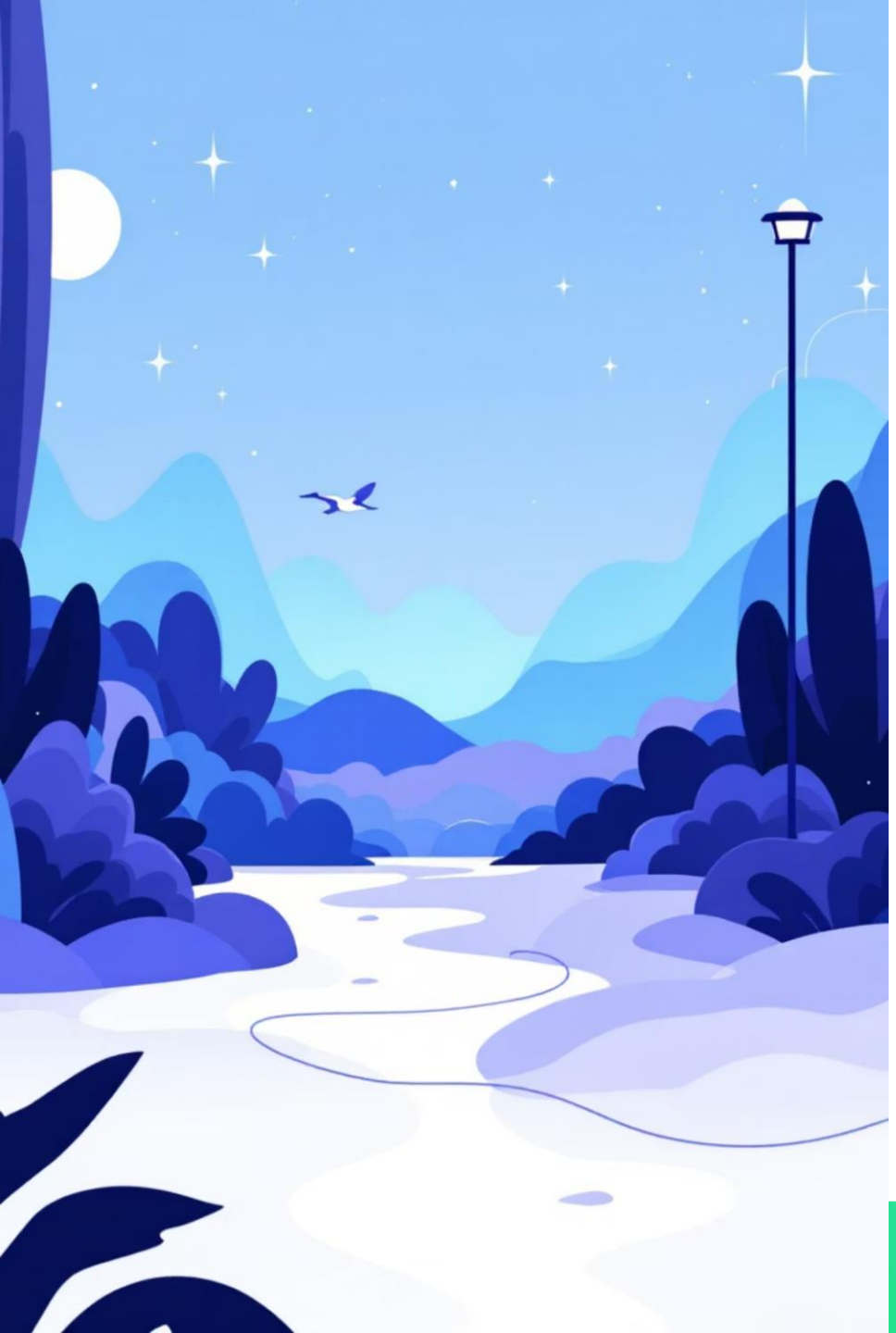
  Mainline kernel support since 4.15 with full SMP and virtualisation support. Distribution support from Debian, Fedora, openSUSE, and Yocto Project.

- **Real-Time Operating Systems**

  FreeRTOS, Zephyr, RT-Thread, and NuttX with optimised RISC-V ports. AUTOSAR-compliant RTOSes for automotive applications.

- **Bare-Metal Environments**

  SBI (Supervisor Binary Interface) implementations: OpenSBI, rustsbi. Boot loaders: U-Boot, coreboot.



Debug & Simulation Tools

Essential platforms for RISC-V development and testing

Spike ISS

The golden reference instruction set simulator provides cycle-accurate modeling for architectural validation and software verification. Essential for ensuring ISA compliance.

QEMU

High-performance emulation platform enabling rapid development cycles with full system emulation capabilities and excellent Linux support for application development.

Renode

Comprehensive system-level simulation framework supporting multi-core systems, peripherals, and complex SoC architectures for complete embedded system validation.

Comprehensive Debugging Stack

GDB Integration

Source-level debugging with breakpoints, variable inspection, and call stack analysis for both simulation and hardware targets.

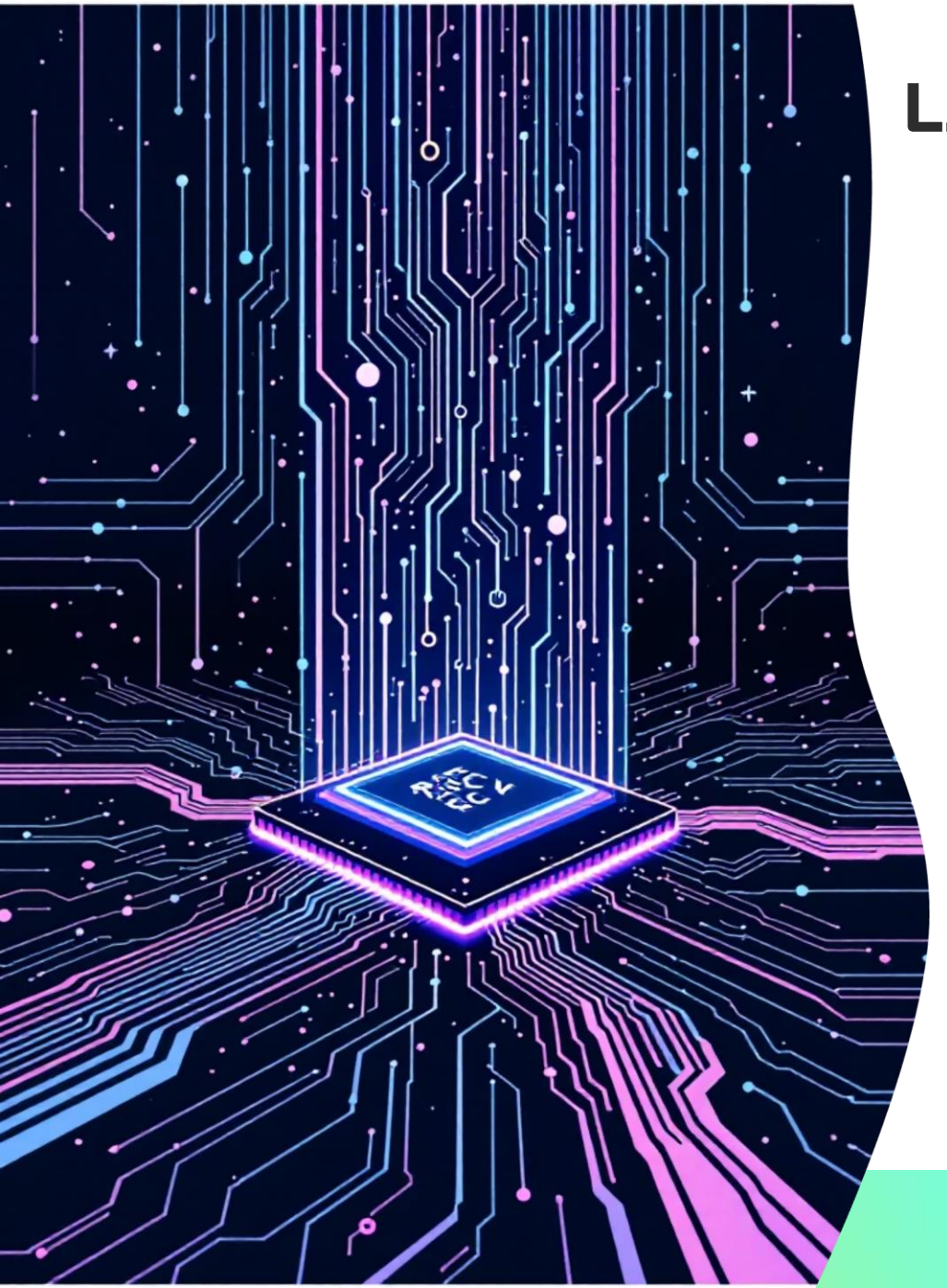
- Remote debugging support
- Multi-threaded debugging
- Python scripting capabilities

Hardware Debug

OpenOCD provides JTAG/SWD connectivity to physical hardware with real-time debugging and flash programming capabilities.

- JTAG probe support
- Flash programming
- Real-time trace

Professional debugging workflow with register windows, memory inspection, and program counter tracking enables efficient firmware development.



Libraries & Middleware Ecosystem

Core C Libraries

- glibc: Full support for RV32/RV64 with optimised assembly routines
- musl: Lightweight alternative with complete RISC-V support
- newlib: Embedded systems focused with RISC-V port

Performance Libraries

- BLAS, LAPACK with vector extension optimisations
- RISC-V optimised DSP libraries
- Cryptography acceleration using Zbkb/Zknd/Zkne extensions

AI/ML Frameworks

TensorFlow Lite

Optimised for RVV (RISC-V Vector) extension with quantised inference support

ONNX Runtime

Model compatibility layer with RISC-V accelerator integration paths

Apache TVM

Deep learning compiler framework with direct RISC-V code generation

Open-Source Hardware Cores

Community-driven implementations powering research and commercial products

Rocket Chip (CHIPS Alliance)

Berkeley's scalable generator framework supporting in-order execution with comprehensive system integration capabilities.

- Configurable pipeline stages
- Academic proven

Sargantana (BSC)

In-Order RISC-V Processor

- Vector Extension
- 1 GHz+

Hazard3

Minimal area-optimized 32-bit core perfect getting started with small footprint design.

- Ultra-compact design
- RasperryPi Pico 2
- Educational friendly

CVA6 (OpenHW)

64-bit application-class processor with MMU support, suitable for running Linux and complex operating systems.

- MMU support
- Linux capable

Commercial Hardware Cores

Production-ready implementations with enterprise support and optimization

SiFive Freedom

Industry-leading commercial RISC-V cores with comprehensive IP portfolio, design services, and proven silicon implementations across multiple process nodes.

Andes Technology

Extensive portfolio of 32/64-bit cores with custom extensions, advanced debug features, and comprehensive development tools for embedded applications.

Synopsys ARC-V

Configurable, power- and area-efficient RISC-V processor IP cores. It extends Synopsys's long-standing ARC line.

Commercial cores provide enterprise-grade support, extensive validation, and professional services for production deployments.

Hardware Design Tools

Modern approaches to RISC-V processor and system design

Chisel HDL

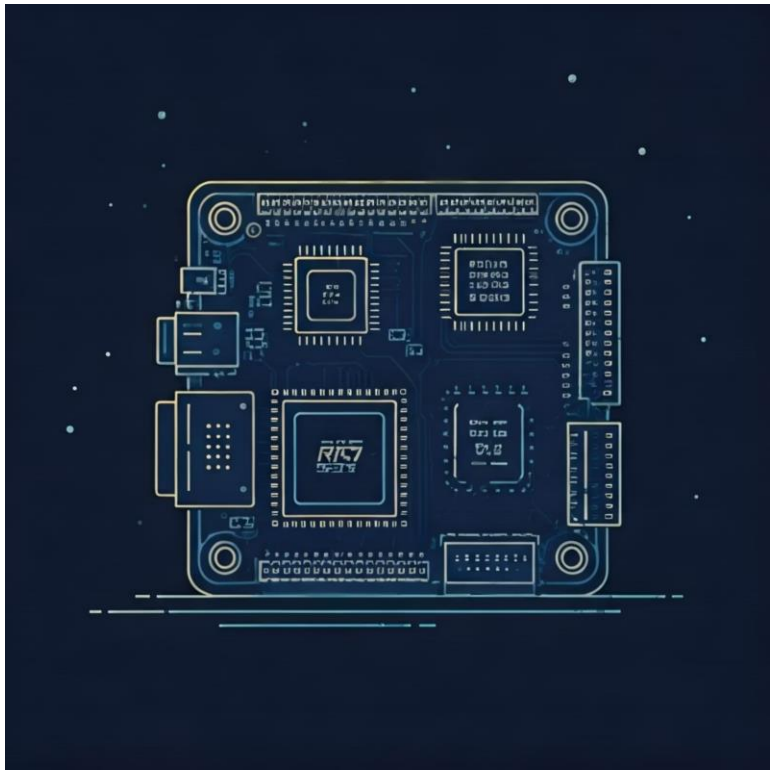
Scala-based hardware description language enabling high-level design with powerful generators and parameterization for complex processor architectures.

Traditional HDLs

Established Verilog and VHDL design flows with mature toolchain support, extensive IP libraries, and proven methodologies for ASIC development.

FPGA Prototyping

Rapid prototyping platforms enabling hardware validation, software development, and system integration testing before silicon implementation.



The combination of modern HDLs like Chisel with traditional flows and FPGA prototyping creates a comprehensive design environment that accelerates RISC-V development cycles.

Verification & Simulation

Industrial Simulators

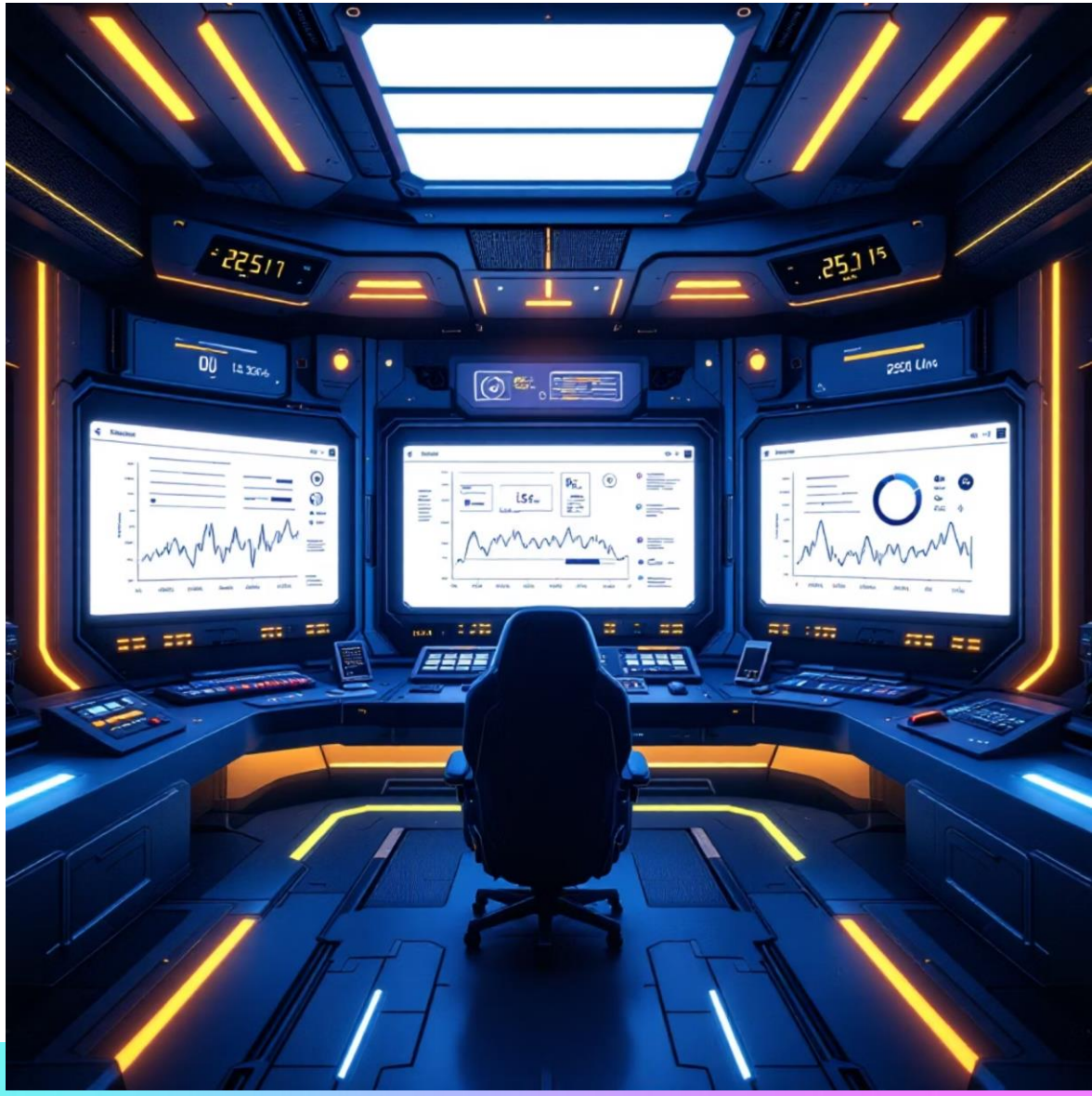
- Cadence Xcelium: Full support for RISC-V simulation
- Synopsys VCS: High-performance simulation with RISC-V models
- Siemens Questa: Comprehensive verification environment
- Imperas: High-speed instruction-accurate simulation

Compliance & Conformance

- RISC-V Architecture Test Framework: Checks ISA compliance of implementations
- Automated test suites for base ISA and extensions
- Privileged architecture compliance tests for supervisor mode operations

Formal Verification

- riscv-formal: Formal verification framework for RISC-V processors
- SymbiYosys: Open-source formal verification flow
- Commercial formal tools with RISC-V property sets



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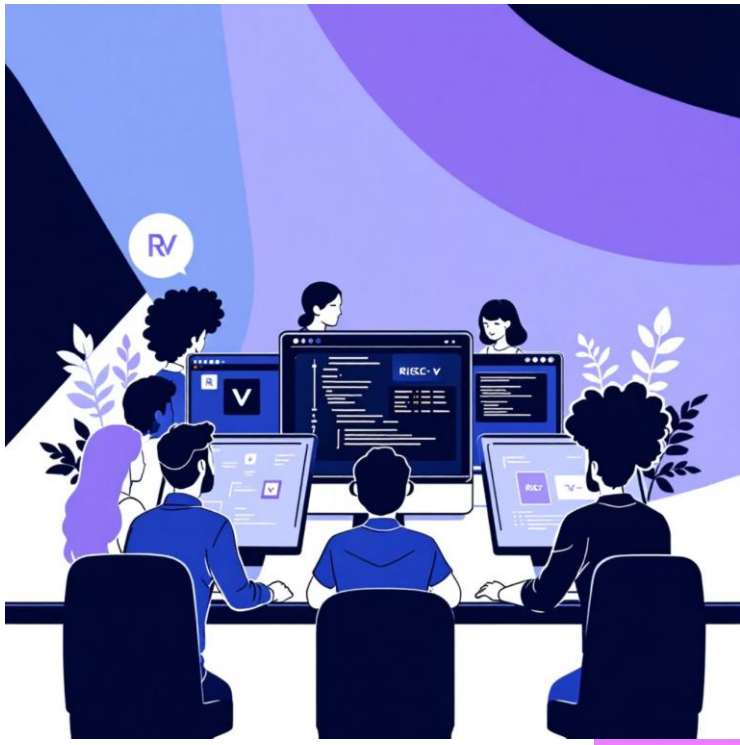
What is RISC-V International?

A **non-profit organisation** established to support and advance the open, royalty-free RISC-V instruction set architecture (ISA)

Our mission is to enable global collaboration, foster innovation, and drive ecosystem growth across the semiconductor and technology industries



Governance

Non-profit organisation with over 3,100 members globally

- Technical Steering Committee oversees ISA development
- Board of Directors includes industry leaders
- Transparent specification development process

Events & Engagement

Active community participation channels

- RISC-V Summit: Annual global conference
- Regional workshops and hackathons
- Working groups with open participation

Governance Structure: The Backbone of RISC-V

1

Board of Directors

Provides strategic oversight and guidance for the organisation

Elected by membership to represent diverse stakeholder interests

2

Technical Steering Committee (TSC)

Manages technical governance across all specification development

Includes Premier members and task group chairs, with monthly reports to the Board

3

Certification Steering Committee

Oversees all certification programmes

Open to participation from all membership levels

4

Technical Committees & Task Groups

Develop and maintain RISC-V specifications and architecture extensions

Drive technical innovation through collaborative work

Membership Tiers: Who Can Join and Why?

Community Members

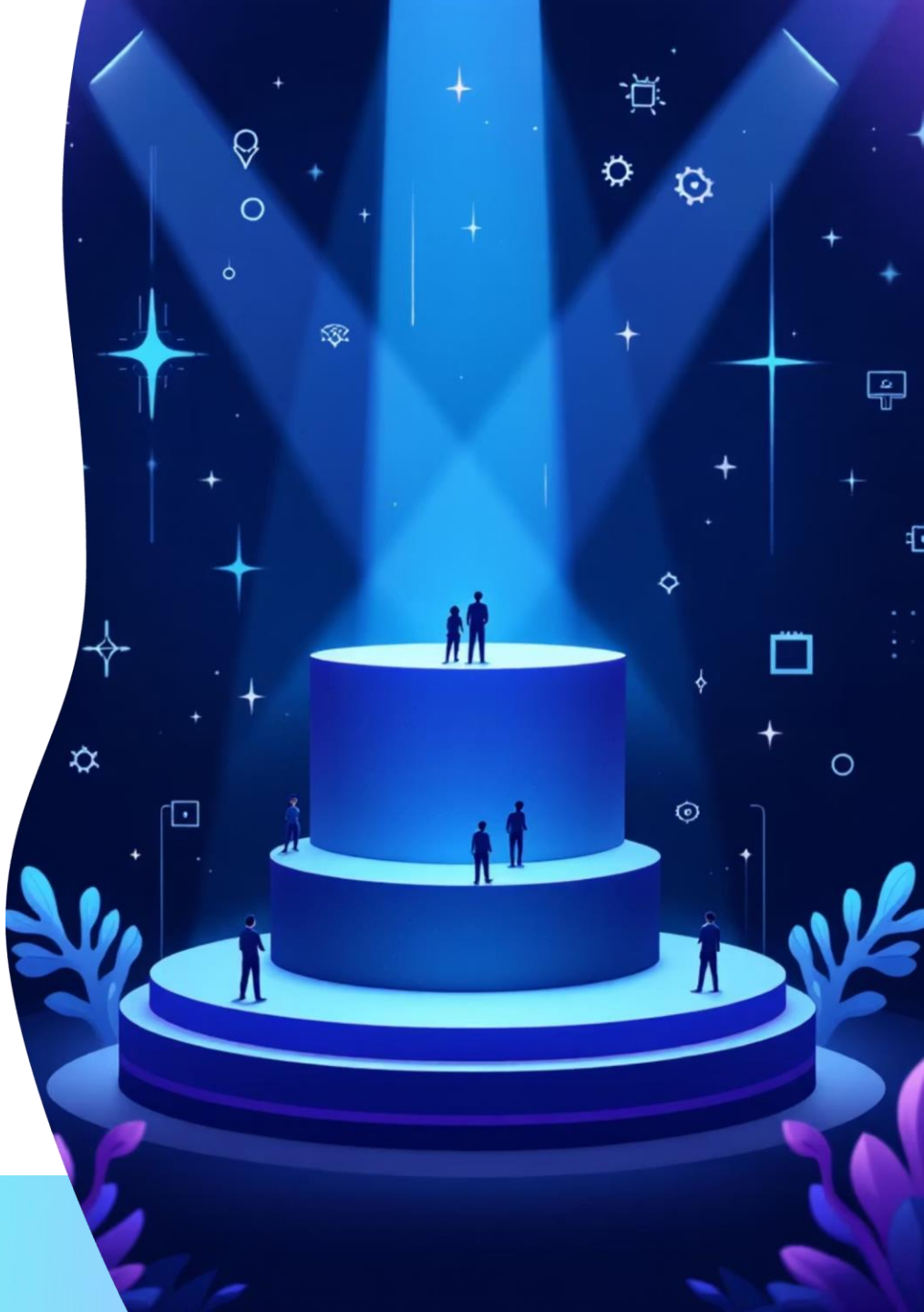
- Free for academics, nonprofits, individuals
- Elect 2 Directors and 1 TSC Delegate
- Access to open specifications

Strategic Members

- Commercial organisations driving adoption
- Elect 3 Directors and 2 TSC Delegates
- Training discounts and trademark use

Premier Members

- Highest tier with expanded roles
- Board Director positions
- Shape RISC-V's future direction



Key Benefits of Membership

Access to Open ISA

Reduced licensing costs and accelerated innovation through open-source hardware architecture

Strategic Influence

Shape RISC-V roadmap and standards to align with your company's strategic goals and requirements

Global Network

Connect with industry leaders, researchers, and potential partners from around the world

Marketing Visibility

Enhance your brand through RISC-V association and ecosystem presence

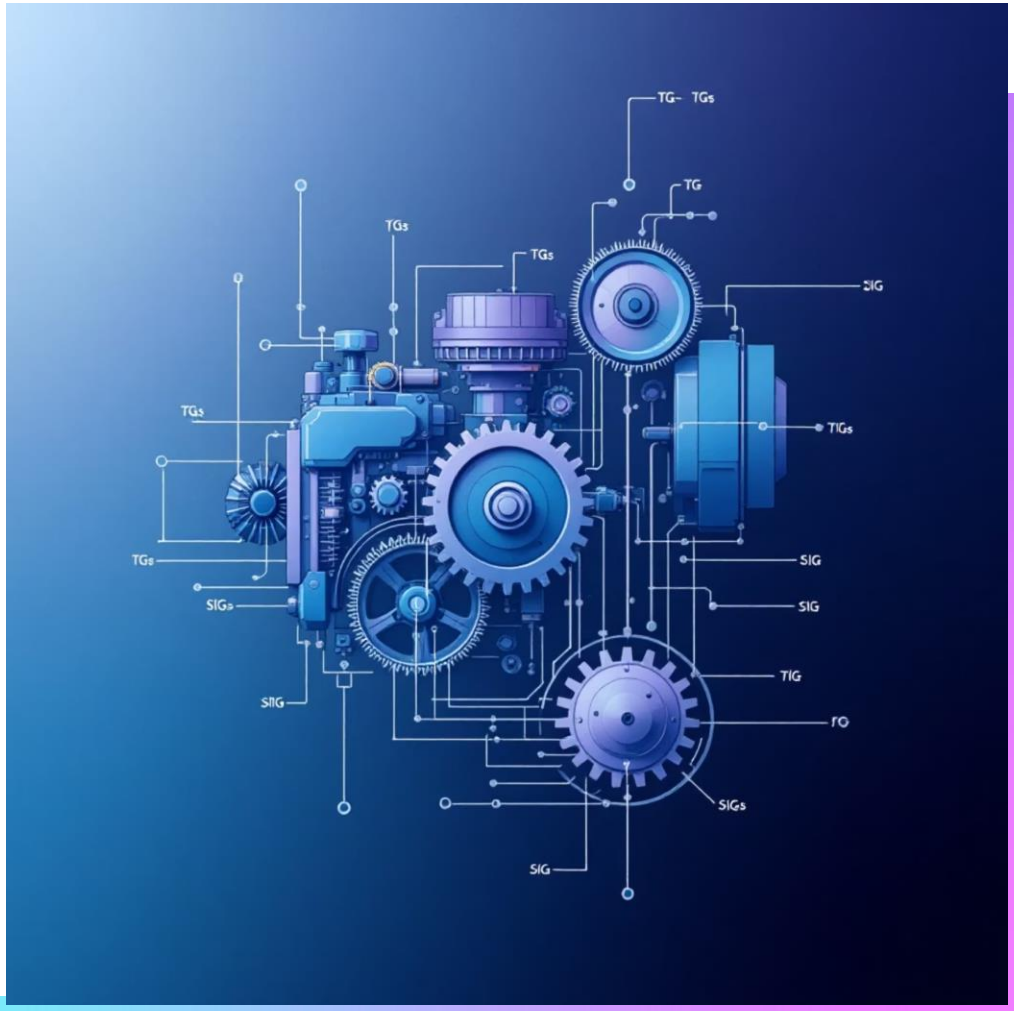
Working Groups: The Engine of Technical Progress

Task Groups (TGs)

- Focused on creating specifications, extensions, and best practices
- Require clear charters and defined deliverables
- Formal approval process through the Technical Steering Committee

Special Interest Groups (SIGs)

- Discussion forums without formal deliverables
- Foster community engagement and exploration
- Can evolve into Task Groups when mature



How Working Groups Operate

Regular Meetings

Scheduled on the members-only calendar with agendas shared in advance

Graduation

Completed work is archived but remains accessible for reference

Contributions

All work becomes RISC-V community property under Creative Commons licensing

Participation

Members can join multiple groups to influence various technical areas

Working groups provide a structured environment for collaborative development whilst ensuring transparency and continuity in the RISC-V ecosystem

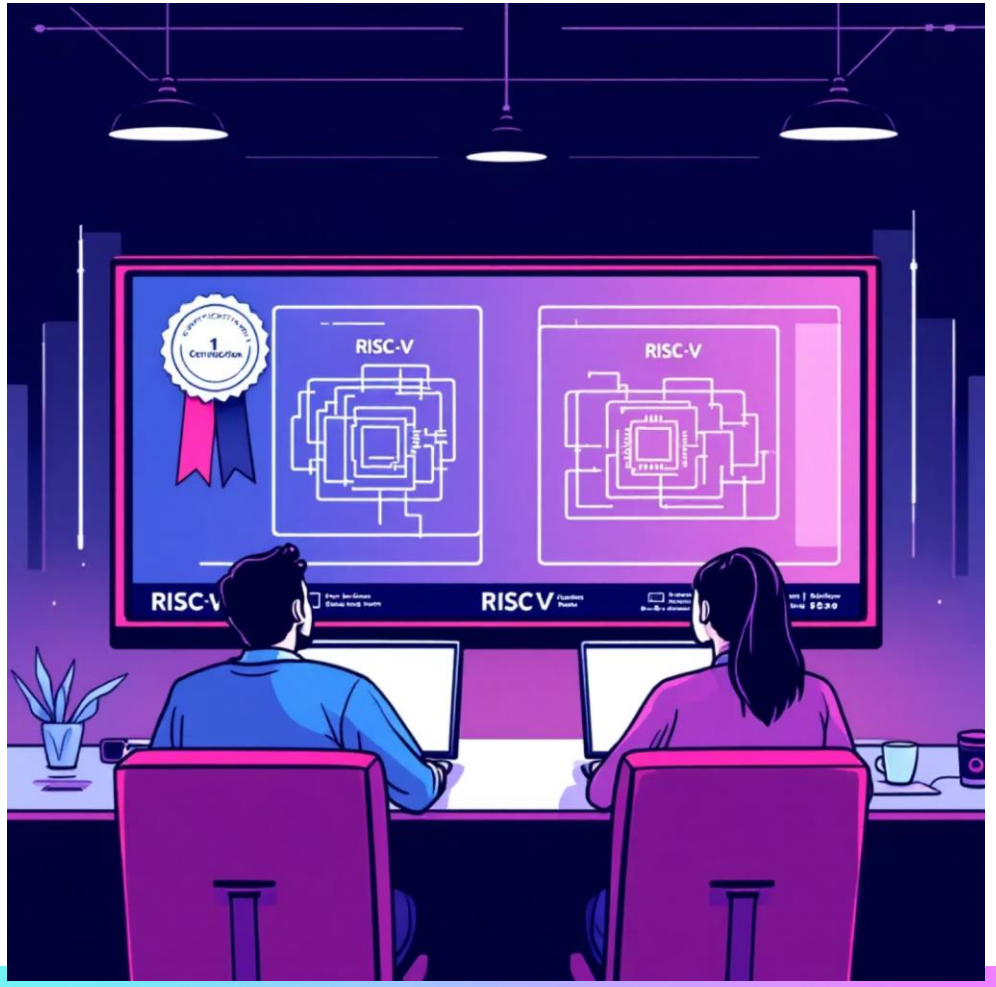
RVI Premier Members

Training & Certification Opportunities

RISC-V International offers vendor-neutral training through established partners:

- **Linux Foundation Education** — Comprehensive courses on RISC-V architecture and implementation
- **Maven Silicon** — Specialised training for hardware designers and developers
- **Member-exclusive benefits** — Training coupons and significant discounts for Strategic and Premier members

Validate your skills with certifications like the RISC-V Foundational Associate (RVFA), covering ISA fundamentals, assembly programming, and toolchain mastery

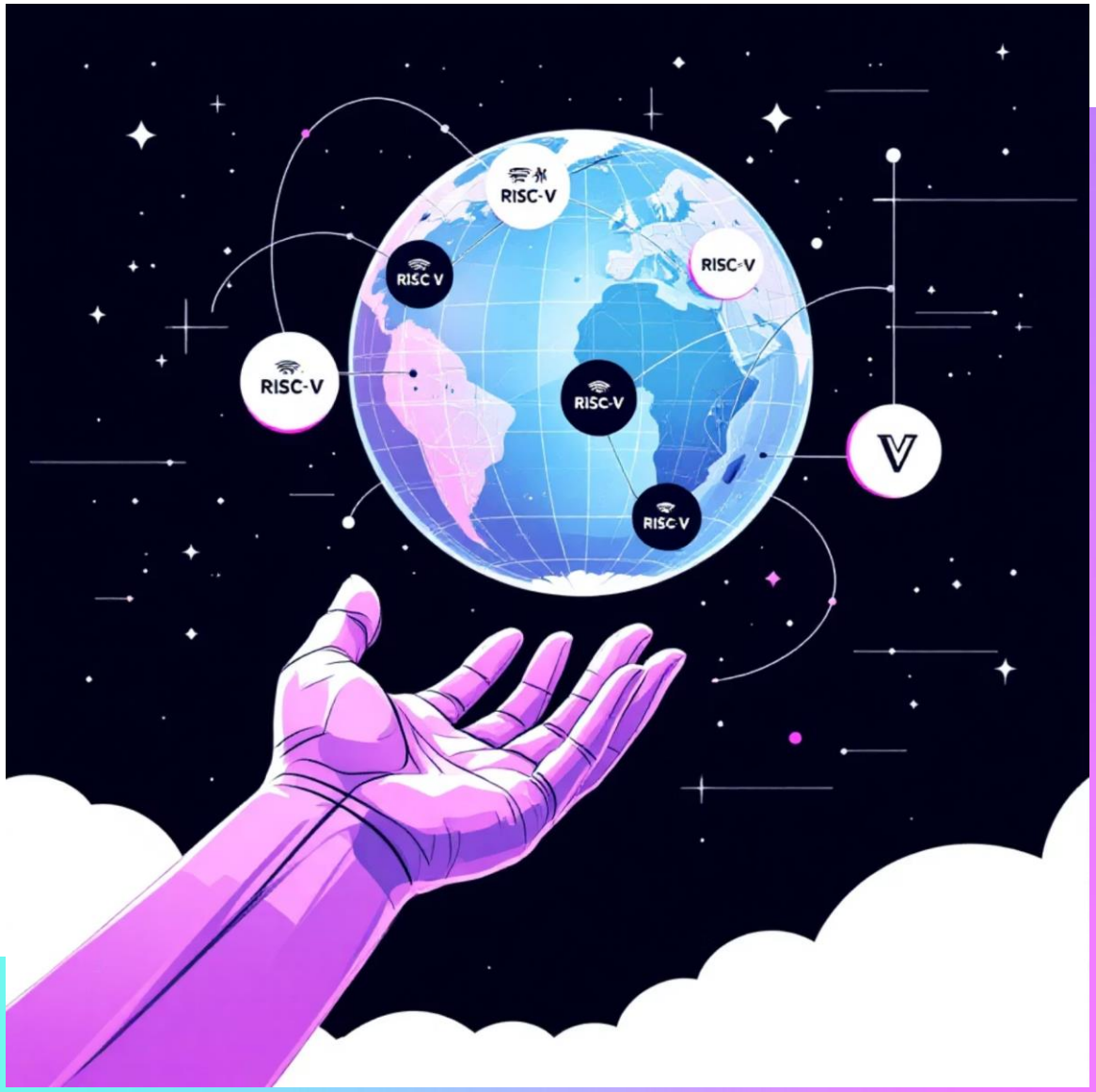


Join RISC-V International: Shape the Future of Open ISA

Become part of a vibrant global community driving semiconductor innovation through open collaboration and shared resources

Influence governance, standards, and training programmes to fit your organisation's strategic needs and technological direction

Visit riscv.org/members/join to explore membership options



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Mobilizing Software Ecosystem for Growth

RISE

Collaboration: RISE (RISC-V Software Ecosystem)

Raise

RISC-V platform quality

Ensure

RISC-V is tier 1 for tools and libraries

Align

Ecosystem partners efforts for adoption

How: Working Upstream, Transparently

Open and Transparent Organization

Coordinating contributions

Bringing open source communities together

RISE

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RISE Members

Premier Members

ANDES TECHNOLOGY
Google
達摩院 DAMO ACADEMY
Imagination
intel.
MEDIATEK
NVIDIA.
Qualcomm
Red Hat
RiVos
SAMSUNG
SiFive
VENTANA

General Members

AKEANA
AMD
BOSC 北京开源芯片研究院
ByteDance
Canonical
ESWIN 奕斯伟计算
ISCAS 中国科学院软件研究所
MICROCHIP
SPACEMIT 进迭时空
tenstorrent
ZTE

RISE

Additional Information: https://riseproject.dev/

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RISE Software Focus Areas

Coordination and collaboration among the RISE members is across an array of software areas to deliver high quality and high performance implementations for RISC-V software

Compilers & Toolchains	LLVM, GCC, GLIBC
System Libraries	FFmpeg, OpenBLAS, oneDAL, XNNPACK, oneDNN
Kernel & Virtualization	Linux, Android
Language Runtimes	Python, Java/OpenJDK, Go, JavaScript/V8, WebAssembly, Rust, .NET
Linux Distro Integration	Ubuntu, Debian, RedHat, Fedora, Alpine, RockyLinux, AlmaLinux, Gentoo
Debug & Profiling Tools	Performance Profiles, DynamoRIO, Valgrind
Simulators/Emulators	QEMU, SPIKE
System Firmware	UEFI, U-Boot, Coreboot, TF-M
Developer Infrastructure	Build Farm, Board Farm, Developer Tools
Security Software	Secure Root-of-Trust, Confidential Compute
AI/Machine Learning	PyTorch, TensorFlow, TFLite, Llama.cpp

RISE

Check out the RISE Wiki: https://wiki.riseproject.dev/

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NEW

AI/ML Working Group

Open source accelerates AI development and ensures a transparent RISC-V ecosystem

RISE AI/ML Working Group drives collaboration on PyTorch, TensorFlow, TFLite and Llama.cpp

Enhancing AI software performance strengthens RISC-V's position as a competitive AI Platform

Recent RFPs Focus on:

Optimization of PyTorch, OpenBLAS, and oneDNN for RISC-V

Develop and upstream a high-performance RVV 1.0 port of Llama.cpp

RISE

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RFP Highlighted Results

LLVM SPEC optimization

Reduces execution time by 15% on SPEC CPU® 2017-based benchmark on SpacemiT-X60
Improved Vectorization Efficiency, better Register Allocation, and more work to be done

Go

Compiler Optimization: expanding RVV and bitmanip support, implementing math and crypto intrinsics
Releases available since Go 1.21 at https://go.dev/dl

Python Packaging

Building packages for commonly used projects
https://gitlab.com/riseproject/python/

QEMU TCG

Enhanced performance for vector (V) and crypto (Zvk) extensions; faster emulation and CI/CD. Achieved 2x faster memory operations and halved AOSP boot time.

Rust

On track to meet full Tier-1 requirements

OpenOCD

RISC-V support upstreaming

LLVM CI

Leveraged QEMU-based testing to support profiles and optimized build configurations.

RISE

Developer Infrastructure

Build Farm

- Integration to Kernel and GCC CI: more testing to improve quality
- Increase quality while landing large autovectorization changes in GCC with pre-commit and post-commit automated testing
  - 137 bugs found and fixed with fuzzing
  - 792 post-commit builds, 400+ patches tested pre-commit
  - Fixing compiler bugs affecting SPEC

Board Farm

- Some usage of Scaleway EM-RV1
- Partnership with Eclipse Adoptium
  - Released Java 17, 21, 23 and later

Developer Resources

RISC-V Optimization Guide

- https://gitlab.com/riseproject/riscv-optimization-guide

RISE Case Study: Adding RVV 1.0 to dav1d AV1 decoder

- Part 1 - 2023-Oct-31, Part 2 - 2023-Nov-14, Part 3 - 2024-Mar-14
- RISCV-Summit EU 2024 Optimizing Software for RISC-V (slides)
- RISC-V 101 2024 (slides) RISC-V 101 2025 (slides)

Python Packaging

- https://gitlab.com/riseproject/python/
- 49 Python projects made available on RISC-V, and counting


How RISE is Contributing
Foster Public Open Source Standard Collaboration
Establish Developer Infrastructure
Activate Broader Developer Community
Becoming a member
Request For Proposals (RFPs)
Developer Appreciation Program
How you can get involved

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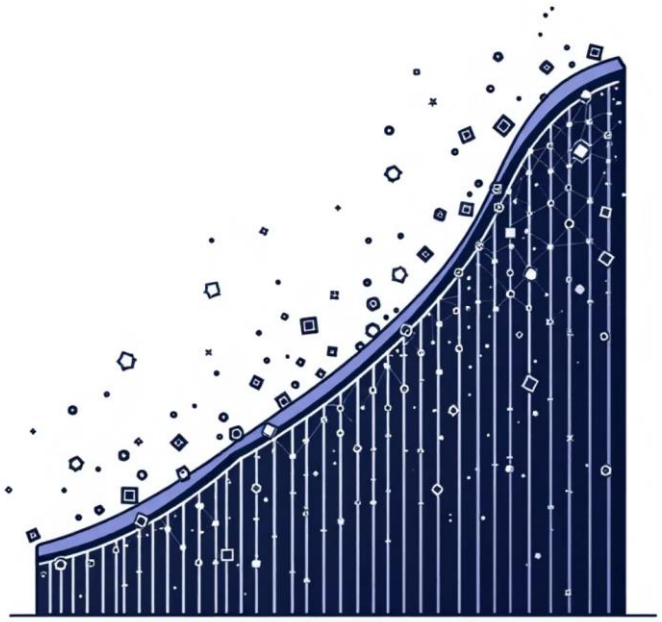
The RISC-V Market Explosion

The RISC-V ecosystem is experiencing unprecedented growth, driven by the industry's shift towards customizable open architectures and specialized computing needs:

- Market valued at **USD 1.76 billion** in 2024
- Projected to reach **USD 8.57 billion** by 2030
- Impressive **CAGR of 30.7%** over the forecast period
- More than **20 billion RISC-V cores** expected in use globally by end of 2025



Nvidia's Game-Changer: CUDA Comes to RISC-V

July 2025 Announcement

Nvidia officially begins porting its CUDA ecosystem to RISC-V CPUs, marking a significant shift in the high-performance computing landscape

Direct Competition

This move enables RISC-V to compete directly with established architectures like Arm and x86 in the lucrative high-performance computing market

Chinese Market Opportunity

Creates a rare opportunity for RISC-V CPU vendors, especially in China, to enter GPU-accelerated markets despite trade restrictions

Infineon's Strategic Moves in RISC-V

> "Our focus is on building a robust ecosystem that enables RISC-V to excel in safety-critical applications where real-time performance is non-negotiable."

— Thomas Schneid, Head of Software Partnership, Infineon (RISC-V Summit China 2025)

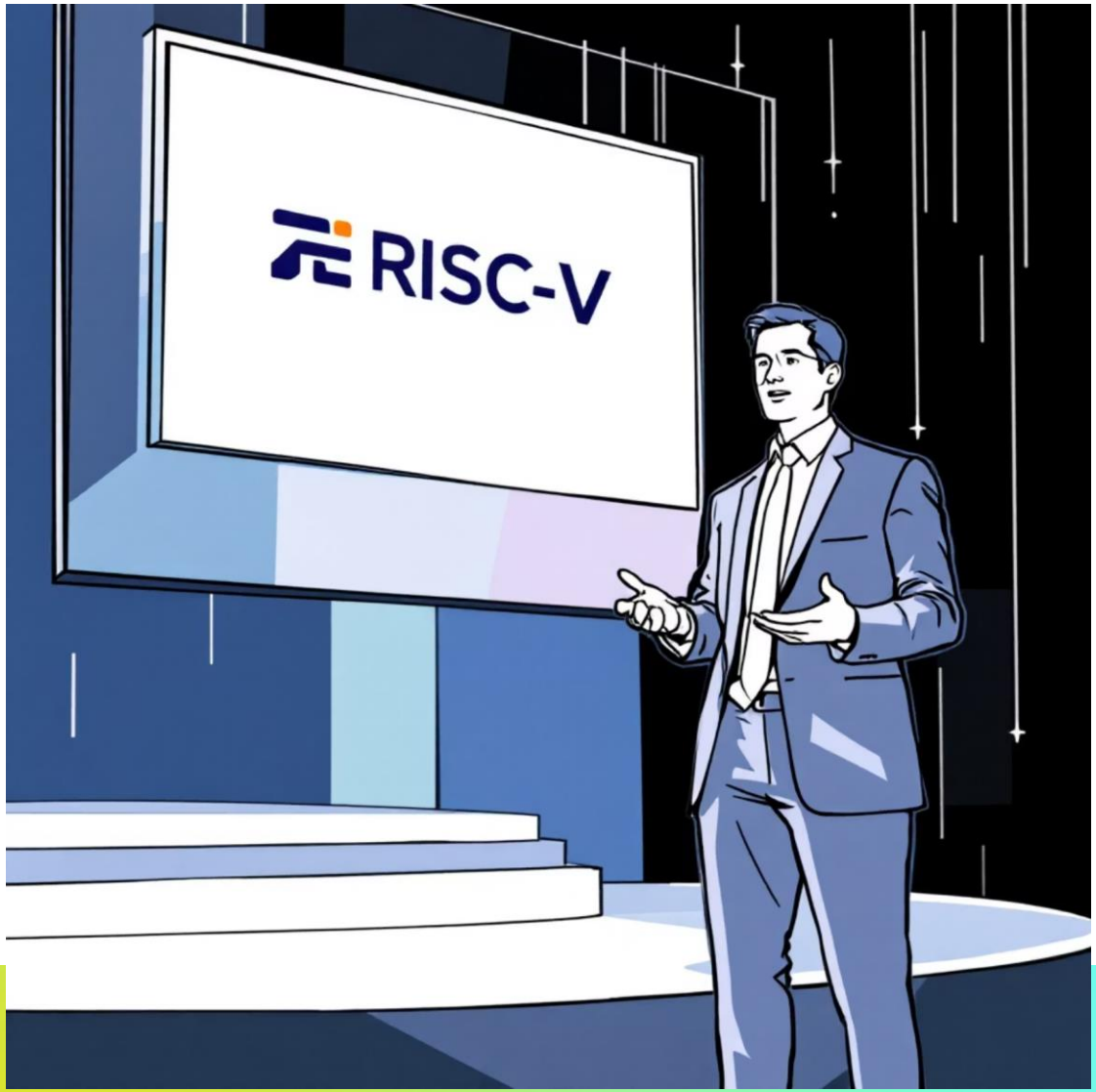
Key Focus Areas

- Automotive safety systems
- Real-time control applications
- Industrial automation

Strategic Initiatives

- Enhanced software tooling
- Cross-industry collaborations
- Ecosystem maturity investments

Qualcomm's Ecosystem Mindset



> "RISC-V is far more than just an ISA—it's an ecosystem that requires community-wide collaboration to scale beyond hardware IP."

— Leendert van Doorn, SVP, Qualcomm

- Qualcomm investing heavily in platform-level support
- Targeting mobile and edge AI applications
- Building developer tools and middleware solutions

Challenges on the Road Ahead

Software Ecosystem Maturity

Limited availability of optimised compilers, libraries, and development tools compared to x86 and Arm ecosystems

Fragmentation Risk

Vendor-specific ISA extensions threaten interoperability and could fragment the ecosystem if not properly standardised

Collaboration Needs

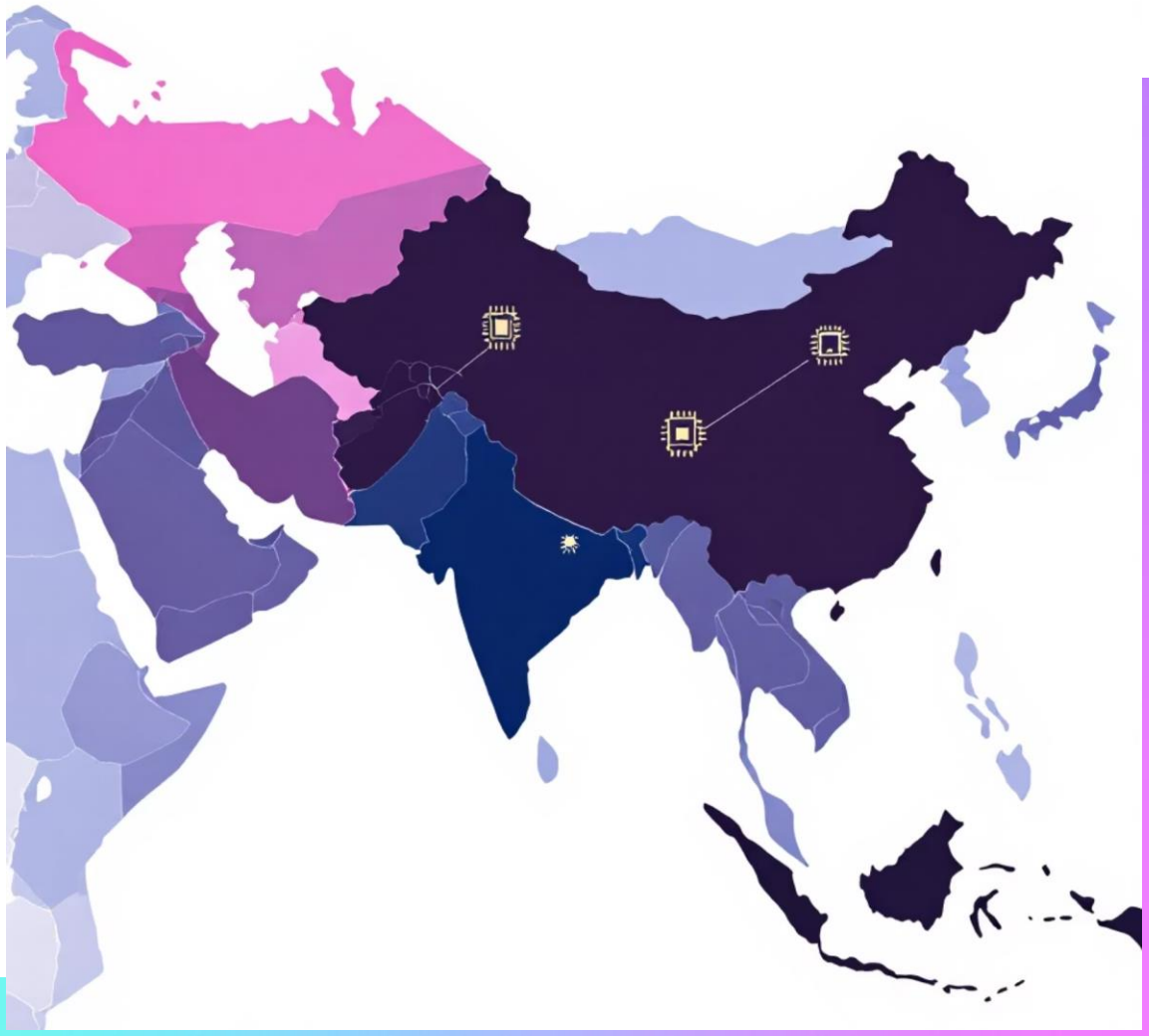
Greater coordination required between hardware vendors, software developers, and standardisation bodies

⚠ Without addressing these challenges, RISC-V risks hitting a growth ceiling that could limit its potential in high-value markets despite strong hardware innovation.

Geopolitical & Industry Dynamics

Regional Adoption Drivers

- **China:** Pursuing domestic RISC-V development to counter trade restrictions
- **India:** "Digital India RISC-V" programme creating semiconductor sovereignty
- **Europe:** European Processor Initiative investing €8 billion in RISC-V capabilities



These initiatives reflect growing concerns about **digital sovereignty** and the need for **supply chain resilience** in the semiconductor industry.

Key takeways

- **Ecosystem & Adoption**
  - Backed by major industry players (Google, NVIDIA, Qualcomm, Alibaba, etc.)
  - Strong academic, open-source, and community support (RISC-V International)
  - Expanding into data centers, automotive, AI, and embedded systems

- **Future Outlook**
  - Market projected to grow 30%+ CAGR through 2030
  - Strategic role in sovereignty & supply chain resilience (China, EU, India)
  - Supports custom extensions for domain-specific acceleration

- **Key challenges:** software maturity, ecosystem fragmentation, need for collaboration

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