



# **CSE 251**

# **Electronic Devices and Circuits**

## **Lecture 9**

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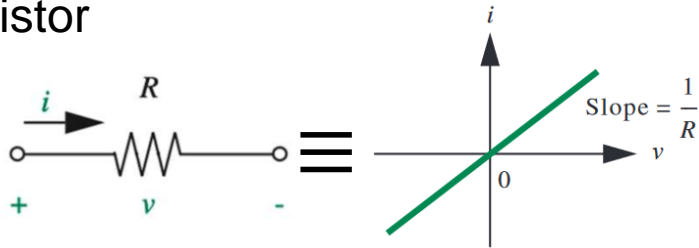
# Outline

- Introduction to Electronic Switches
- Basic Inverter
- Introduction to Controlled Sources
- Introduction to MOSFET
- MOSFET as digital switch
- Designing Logic gates with MOSFETs

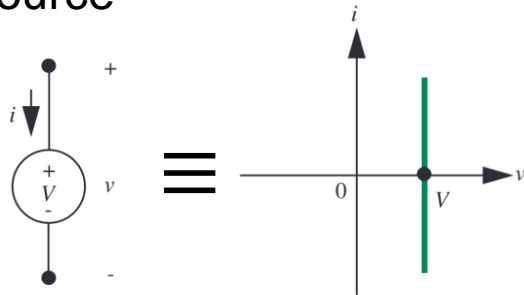
# Two terminal Devices

## Linear Devices

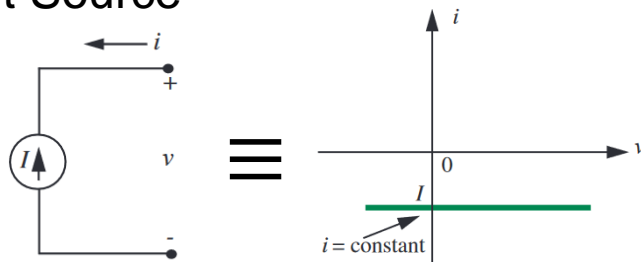
Resistor



Voltage Source



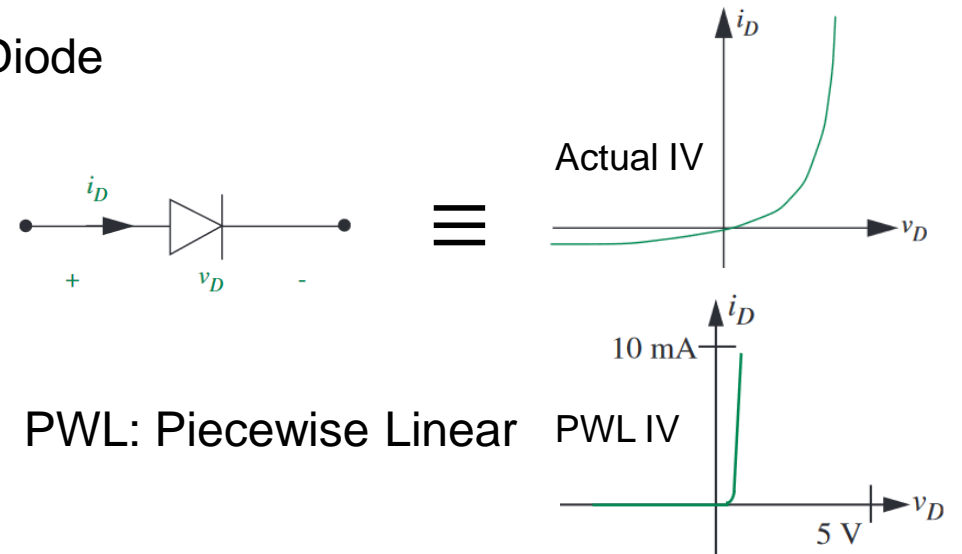
Current Source



IV characteristics of two terminal devices are fixed.

## Non-linear Devices

Diode



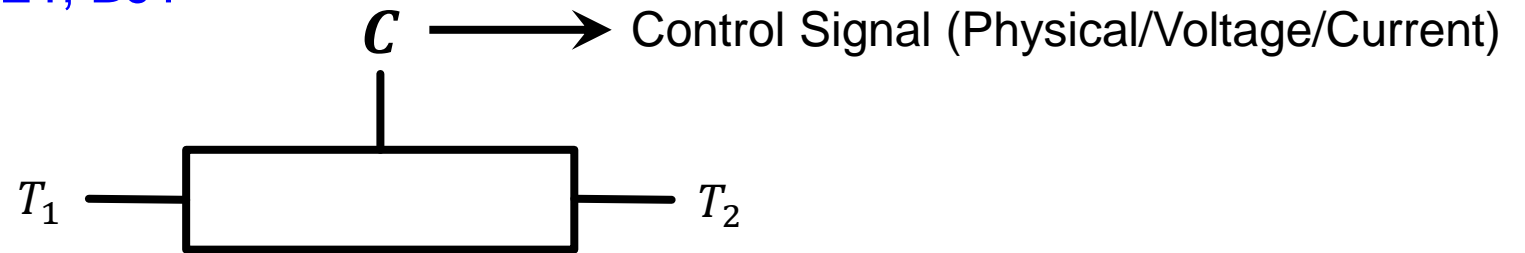
IV characteristics of **three terminal devices** can be changed

# Three terminal Devices

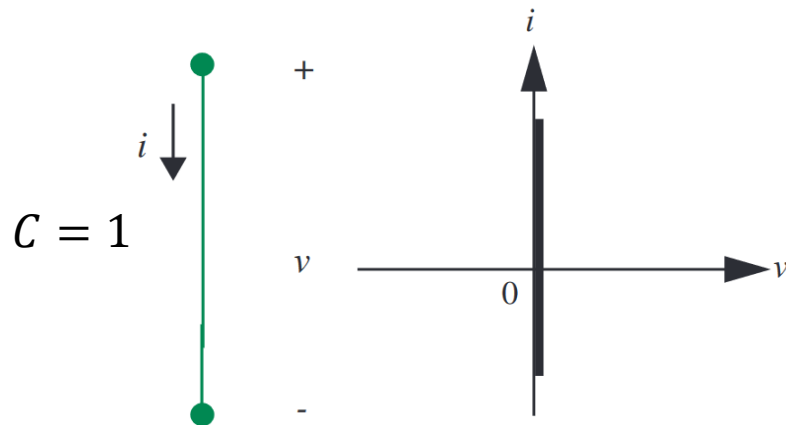
IV of two terminal can be controlled using a third terminal.

**Example:** Switch, MOSFET, BJT

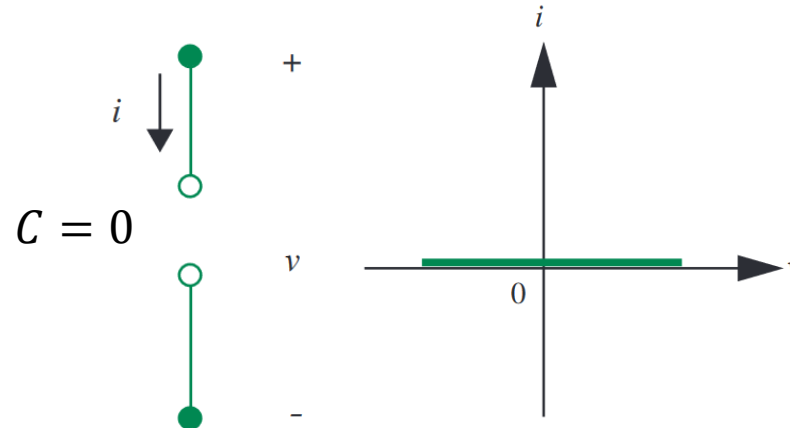
Switch



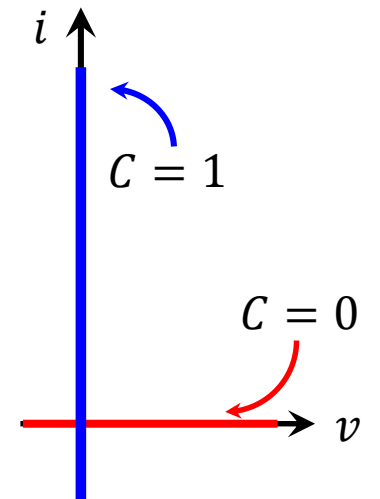
IV characteristics between  $T_1$  and  $T_2$  can be controlled by  $C$



Switch **ON**

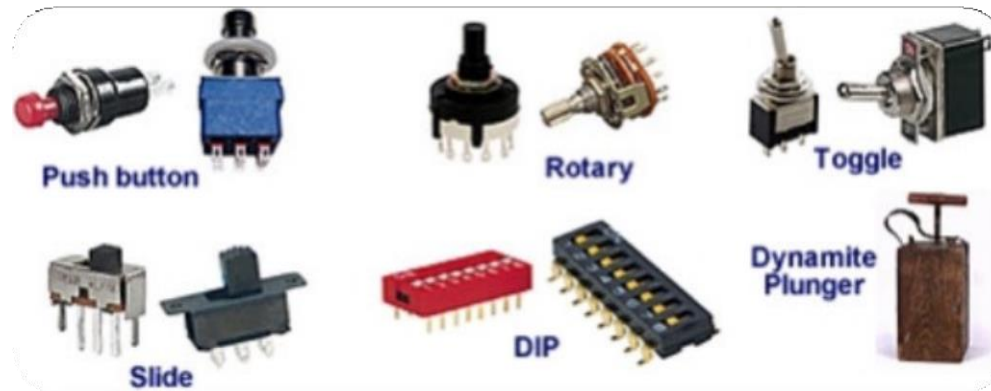


Switch **OFF**

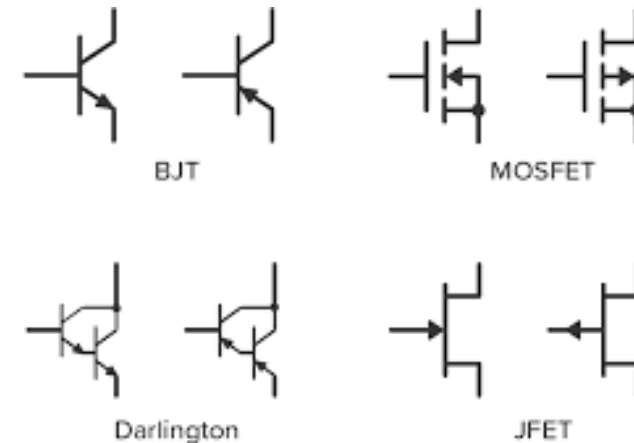


# Switch – Types

- Depending on the control, the switch can be
  - **Analog:** Controlled using physical toggle/button
  - **Digital:** Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



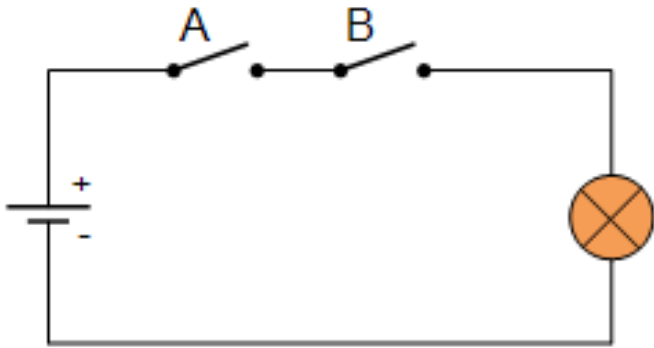
Analog switches



Digital switches (Transistors)

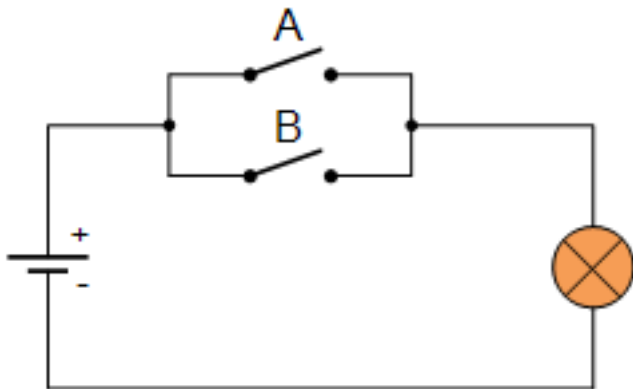
# Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

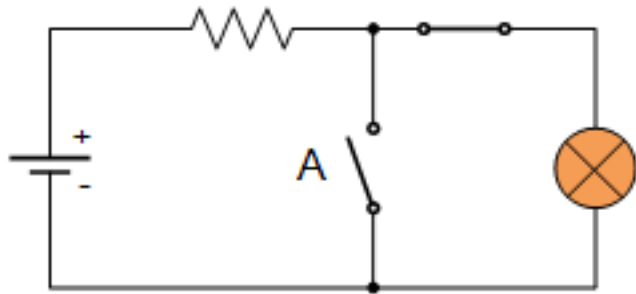
**AND operation**



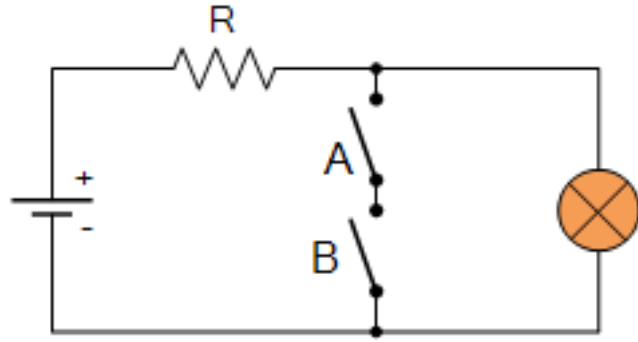
A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

**OR operation**

# Switch Application – Logic Gates

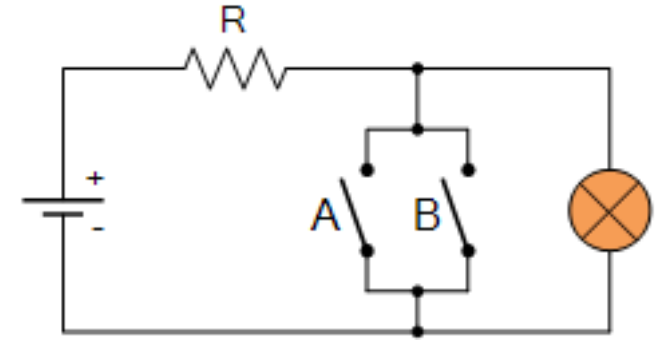


A	Bulb
0	ON
1	OFF



A	B	Bulb
0	0	ON
0	1	ON
1	0	ON
1	1	OFF

**NAND operation**



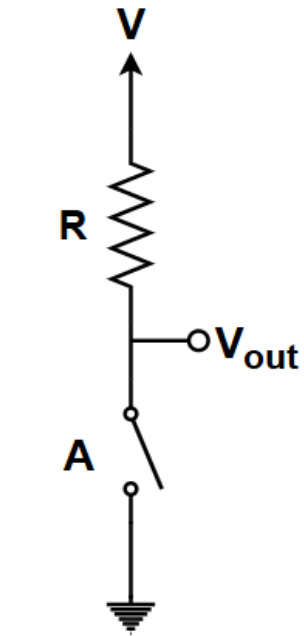
A	B	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

**NOR operation**

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits  
-> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

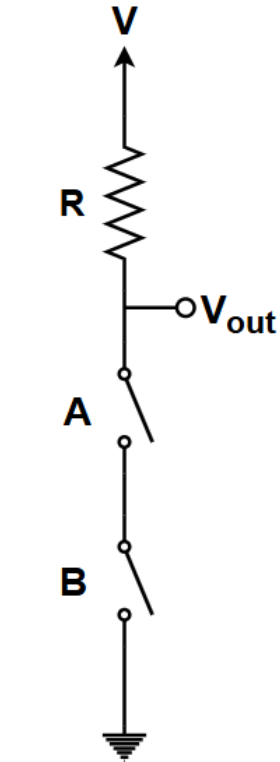
# Switch Application – Logic Gates

Alternative representations:



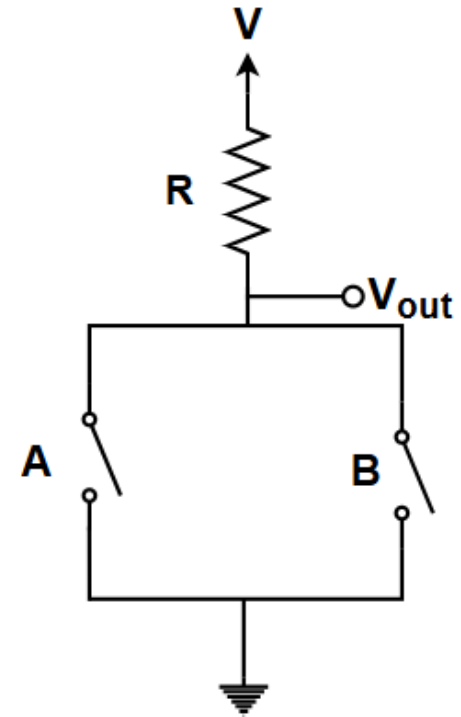
$$V_{out} = \bar{A}$$

NOT



$$V_{out} = \overline{AB}$$

NAND

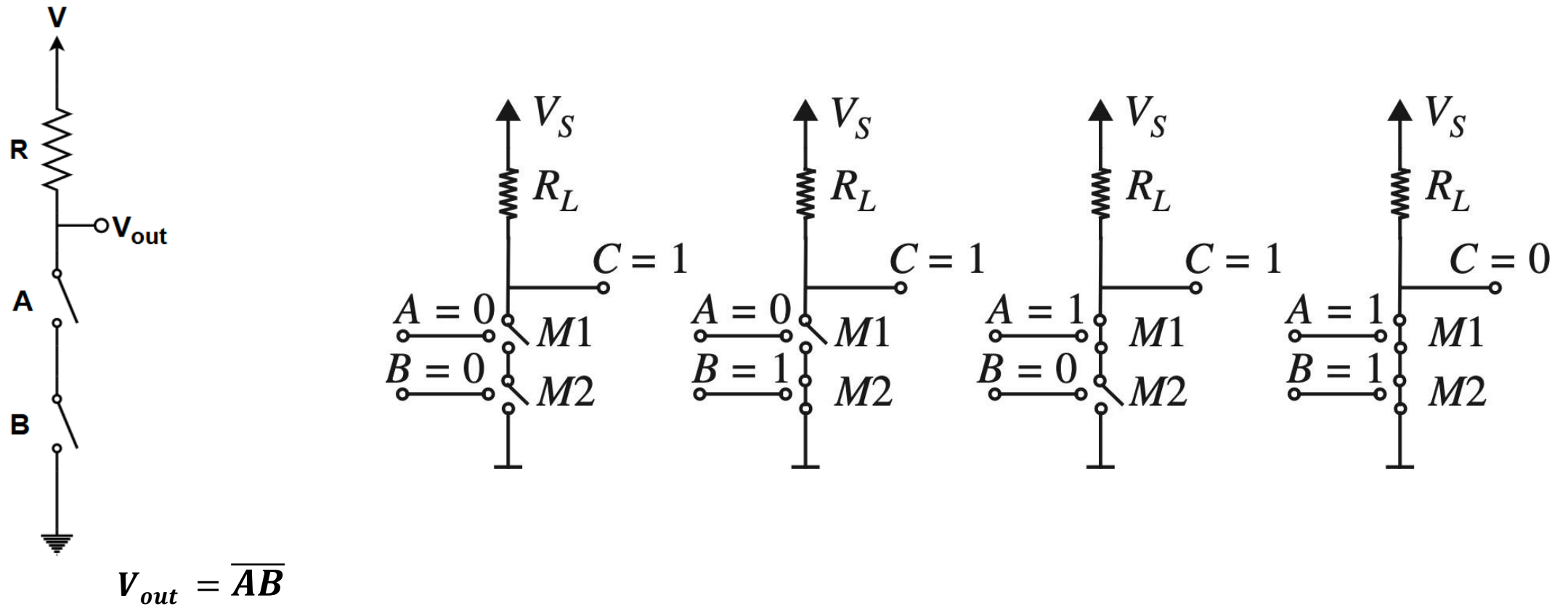


$$V_{out} = \overline{A + B}$$

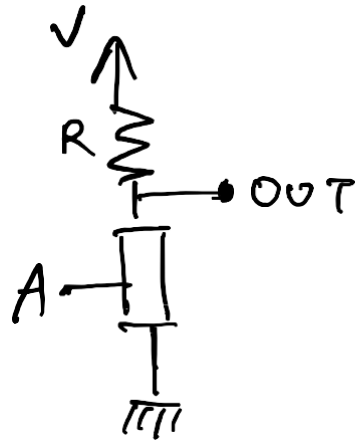
NOR

# Switch Application – Logic Gates

Alternative representations:

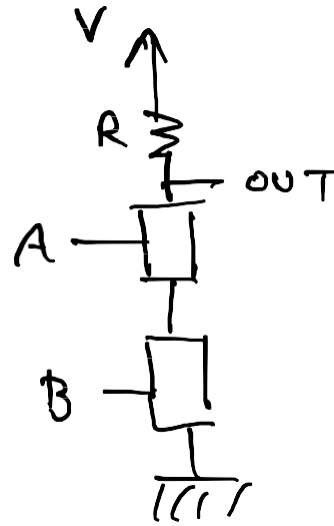


# Switch Application – Logic Gates



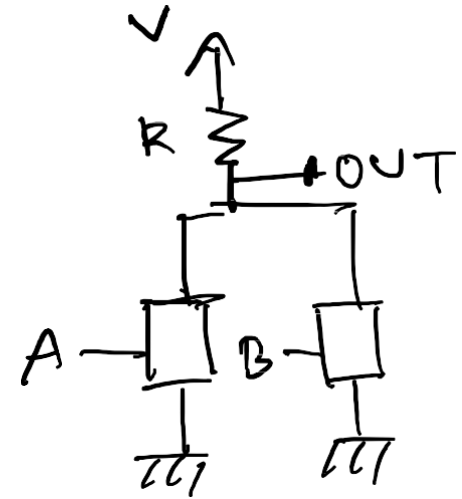
$$OUT = \overline{A}$$

A	V <sub>OUT</sub>
0	5V
1	0V



$$OUT = \overline{AB}$$

A	B	V <sub>OUT</sub>
0	0	5V
0	1	5V
1	0	5V
1	1	0V

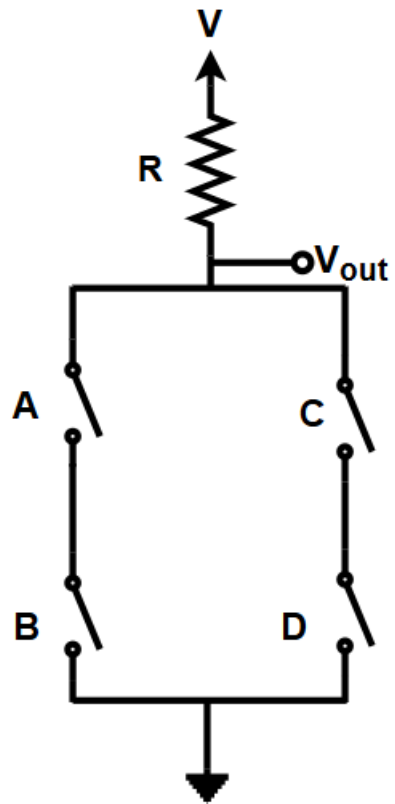


$$OUT = \overline{A+B}$$

A	B	V <sub>OUT</sub>
0	0	5V
0	1	0V
1	0	0V
1	1	0V

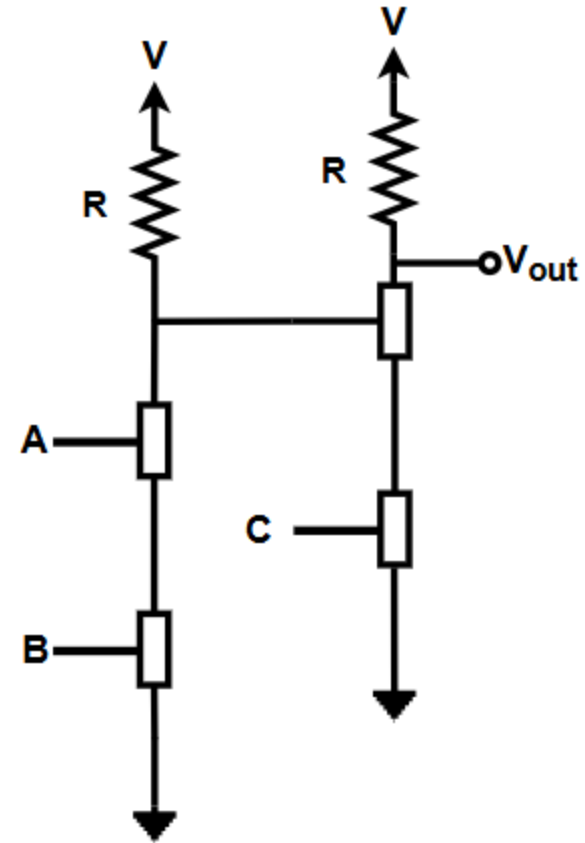
# Examples

1.



$$V_{out} = \overline{AB} + \overline{CD}$$

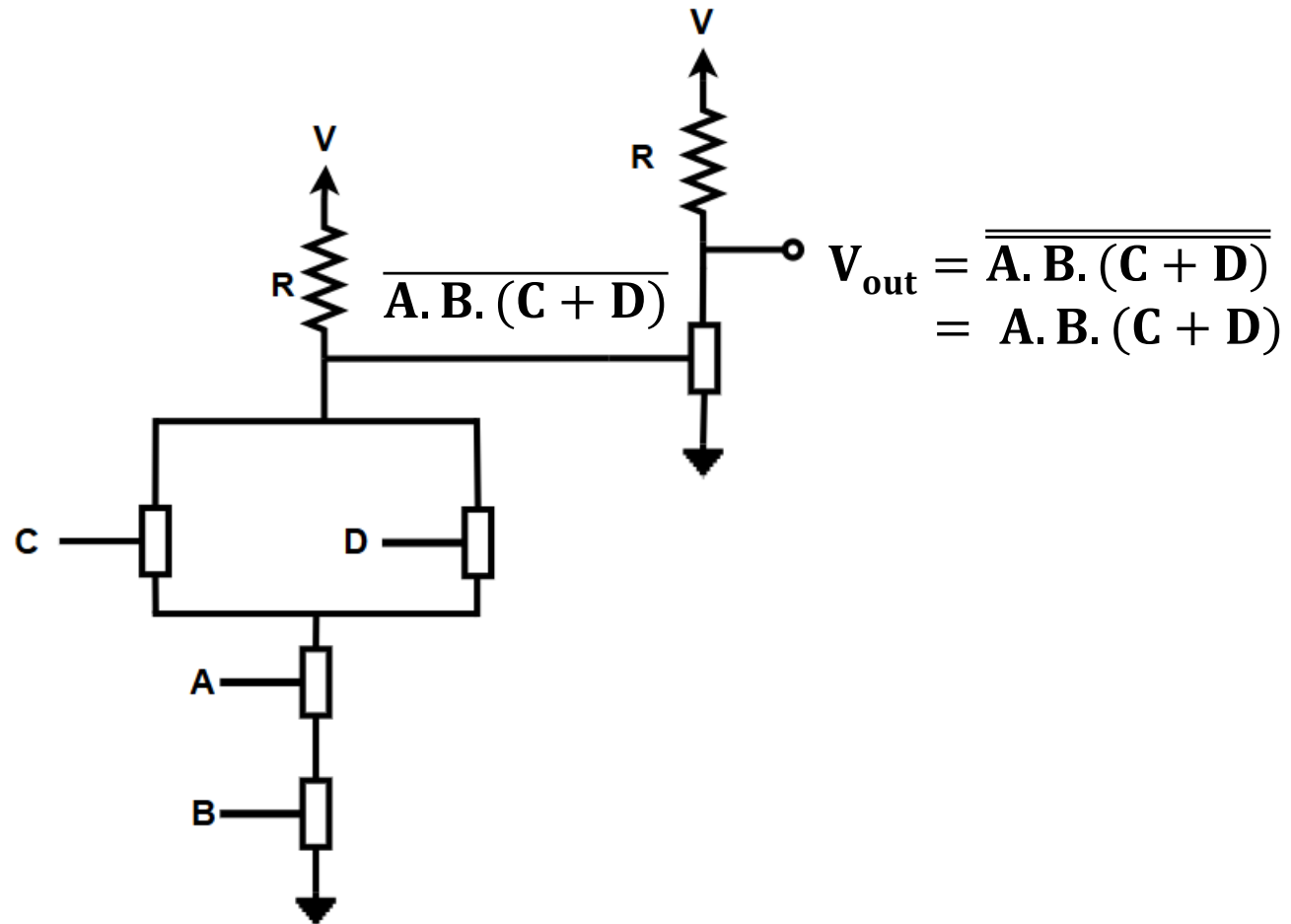
2.



$$V_{out} = \overline{\overline{AB} \cdot C}$$

## Example

Implement using switches:  $f = A.B.(C+D)$



# Digital Representation

- Binary  $\rightarrow$  Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

## Voltage

5V  $\rightarrow$  1

0V  $\rightarrow$  0

0V  $\rightarrow$  1

3.3V  $\rightarrow$  0

We use this  
convention usually

## Current

2mA  $\rightarrow$  1

3mA  $\rightarrow$  0

## State

Diode

ON  $\rightarrow$  1

OFF  $\rightarrow$  0

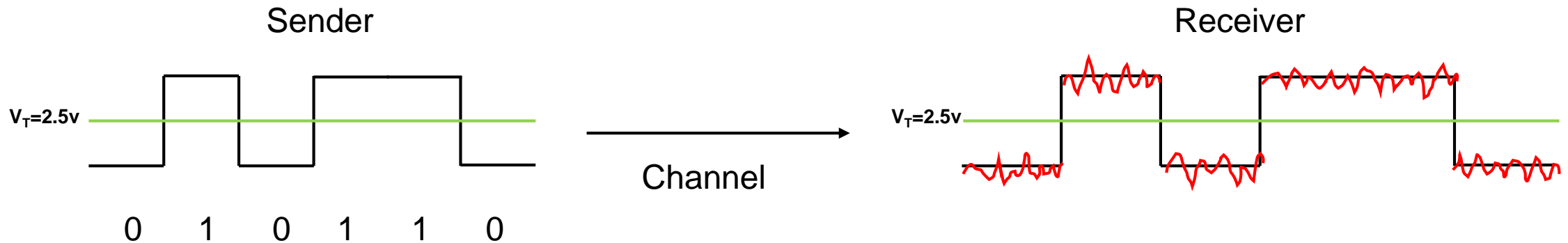
Memristor

Low resistance  $\rightarrow$  1

High resistance  $\rightarrow$  0

# Digital Representation

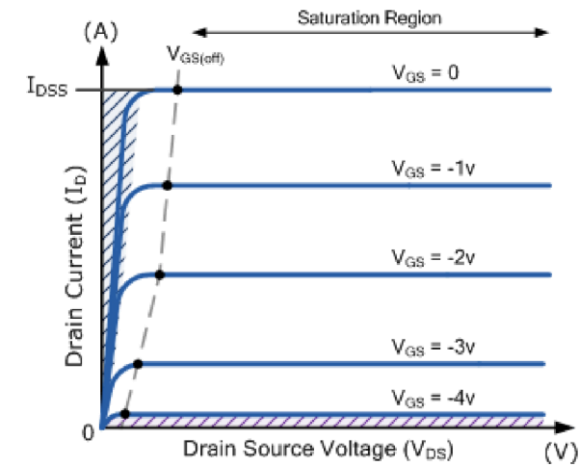
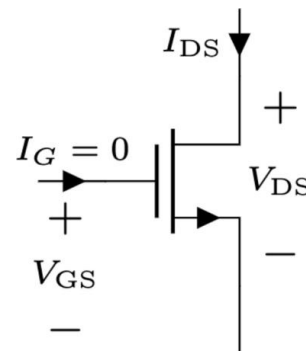
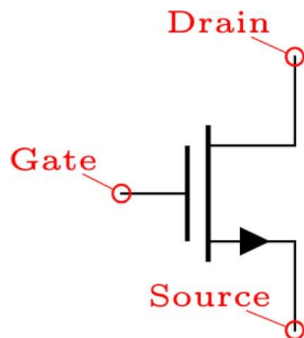
Suppose you want to send 010110



- Single value based representation fails in the presence of noise
- Better approach – threshold-based system
- Simplest: **Logical 0** =  $V < V_T$       **Logical 1** =  $V > V_T$

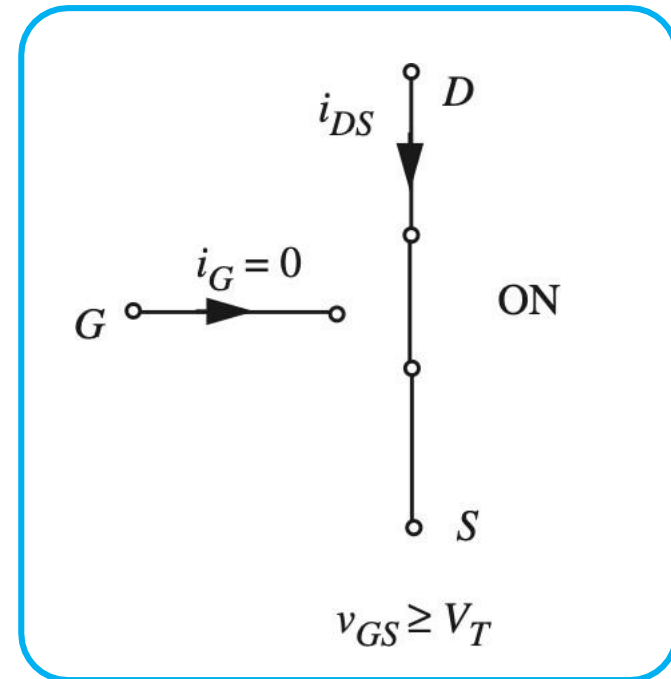
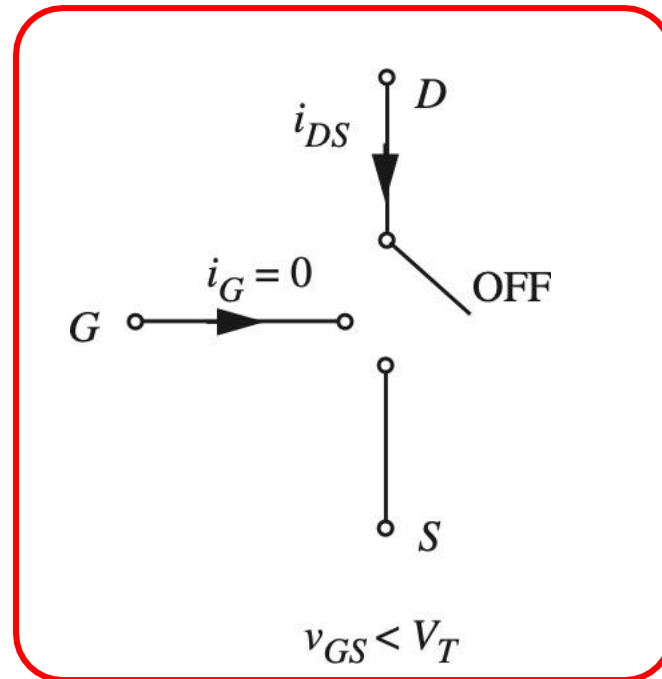
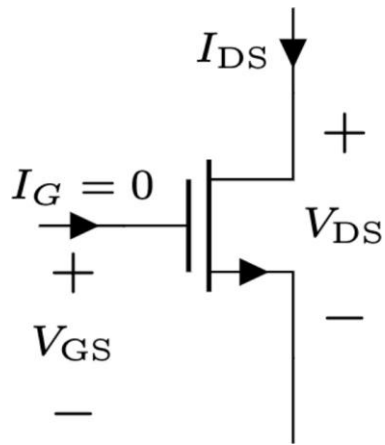
# Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – **Voltage Controlled**, **Current Controlled**
- **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (**MOSFET**) are **voltage controlled**
- Control,  $C = V_{GS}$ . The IV characteristics ( $I_{DS}$  vs  $V_{DS}$ ) depends on  $V_{GS}$
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)

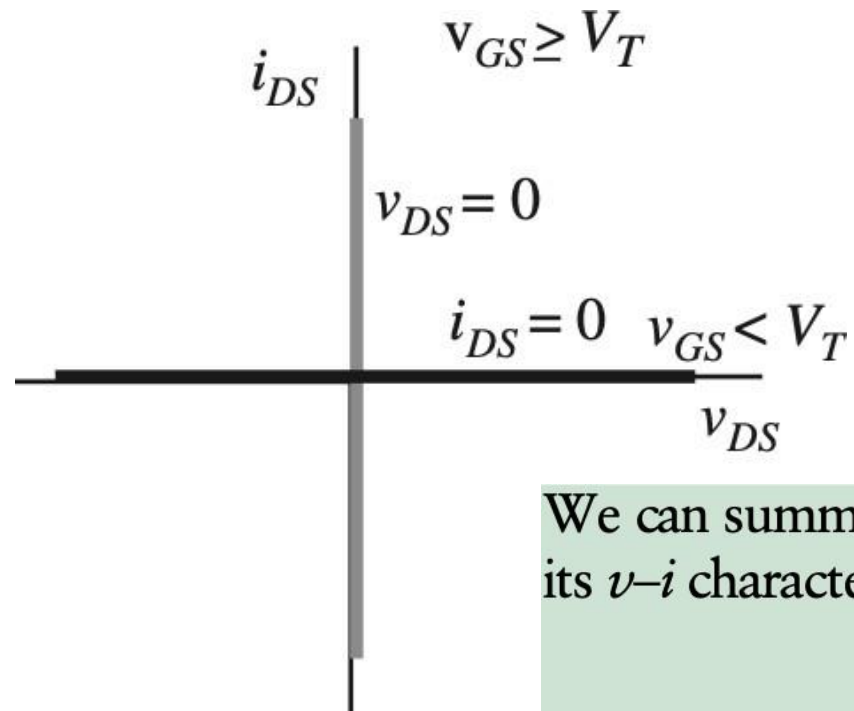


# MOSFET S-Model

- The MOSFET (approximately) behaves like a switch
- $C = V_{GS}$ . Here,  $C = \text{"0"} \Rightarrow V_{GS} < V_T$ , and  $C = \text{"1"} \Rightarrow V_{GS} > V_T$



# MOSFET S-Model



We can summarize the S model for the MOSFET in algebraic form by stating its  $v$ - $i$  characteristics as follows:

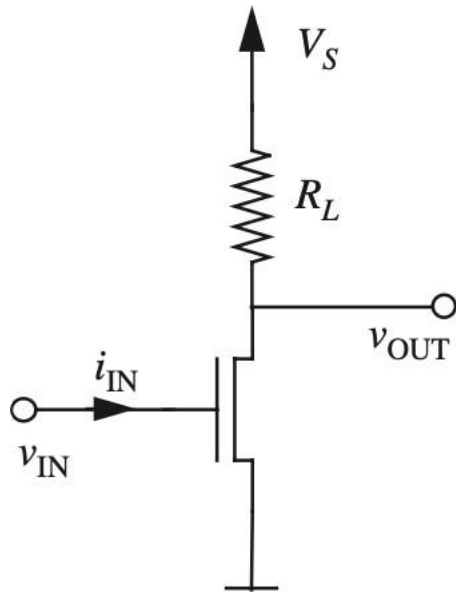
$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

and

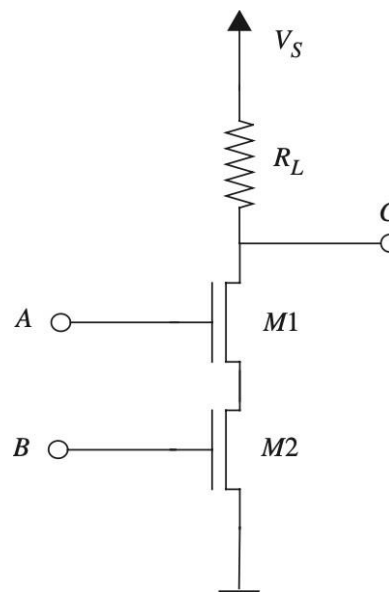
$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \quad (6.2)$$

# Logic Gates using MOSFET

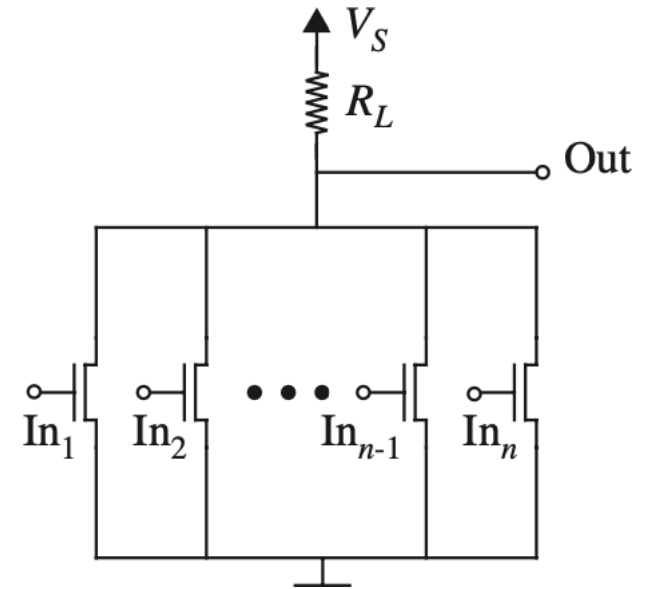
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

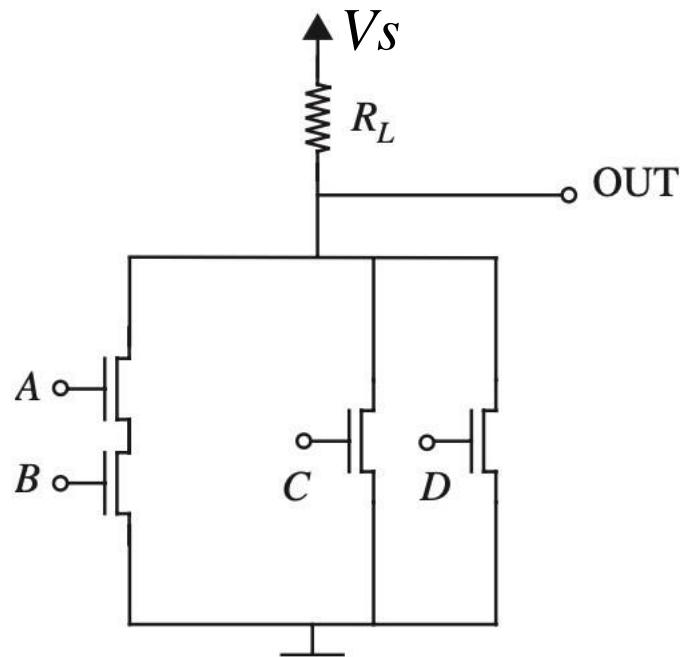


NAND Gate (Inverter)

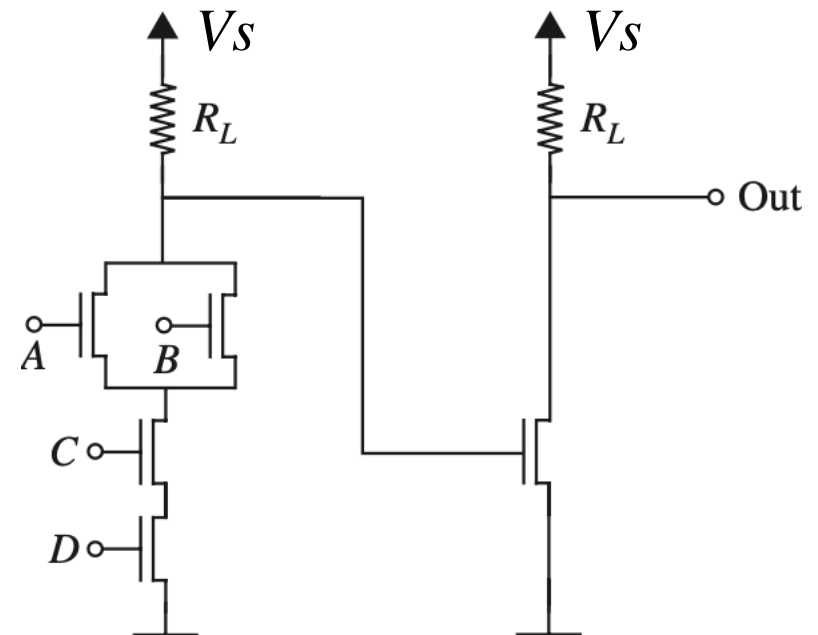


NOR Gate (Inverter)

# MOSFET Logic Gates – More Examples



$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

# Practice Problem 2

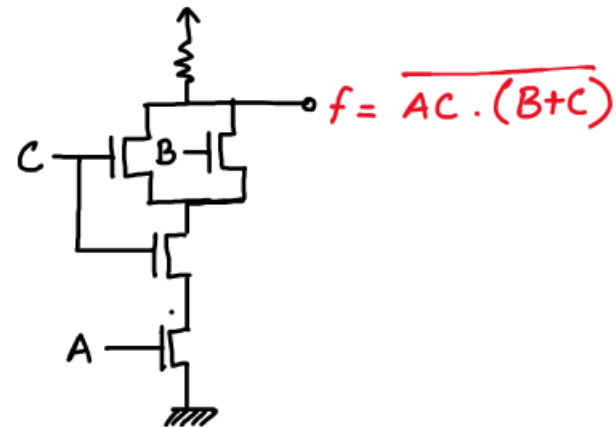
- **Design** a circuit using ideal MOSFETs (S-model) to implement the logic function

$$f = \overline{AC} + \overline{(B + C)}$$

$$= \overline{\overline{AC} + (B + C)}$$

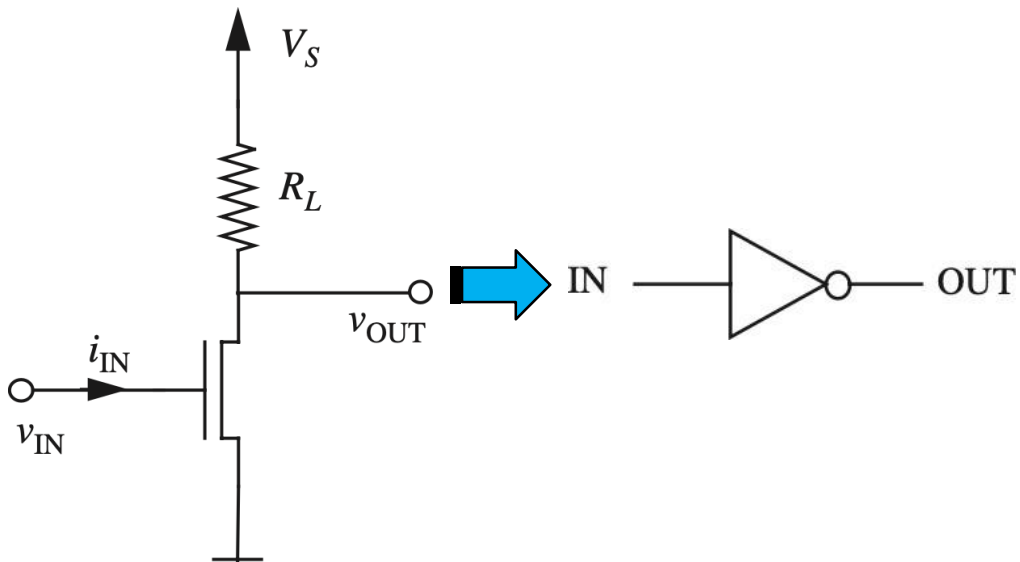
$$= \overline{\overline{AC}} \cdot \overline{(B + C)} \quad [\text{De Morgan's Theorem}]$$

$$= \overline{AC} \cdot (B + C)$$



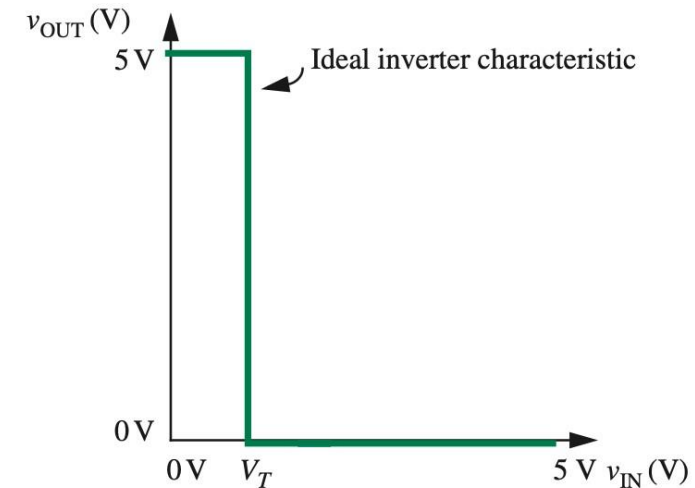
# Voltage Transfer Characteristics (VTC)

- **Reminder:** VTC is a graph where  $x$  –axis = input voltage,  $y$ -axis = output voltage
- **Why?** Design logic gates to follow a given static discipline



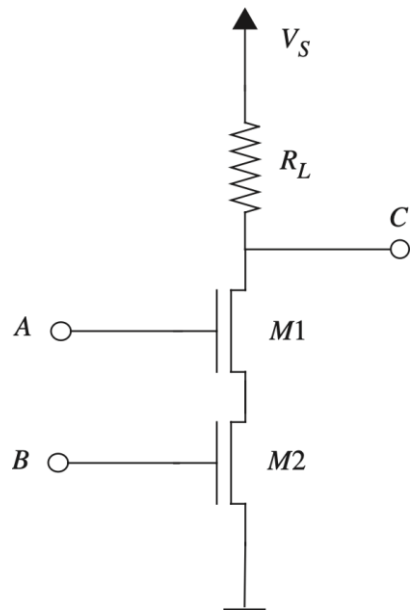
When  $v_{IN} < V_T$  (Logical 0)  $v_{OUT} = V_S = 5\text{ V}$  (Logical 1)

When  $v_{IN} \geq V_T$  (Logical 1)  $v_{OUT} = 0\text{ V}$  (Logical 0)

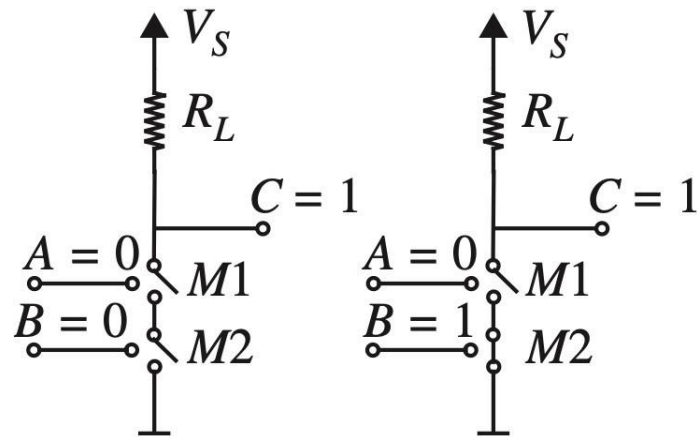


# VTC of NAND gate

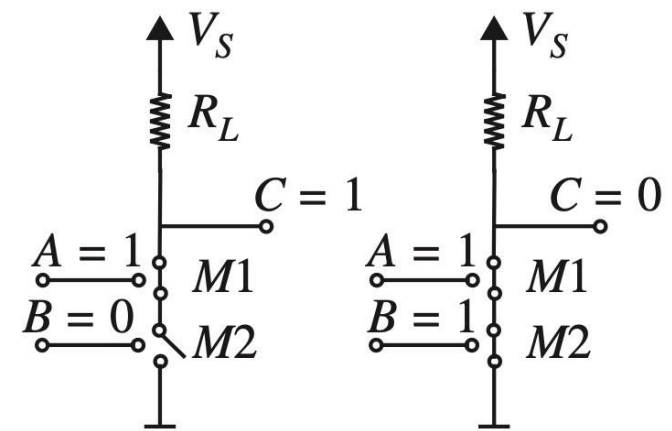
- We only have one  $x$  –axis, but two inputs
- **Solution:** Draw two VTC, one considering  $V_A = 0$  one considering  $V_A = 1$



When  $V_A = 0$

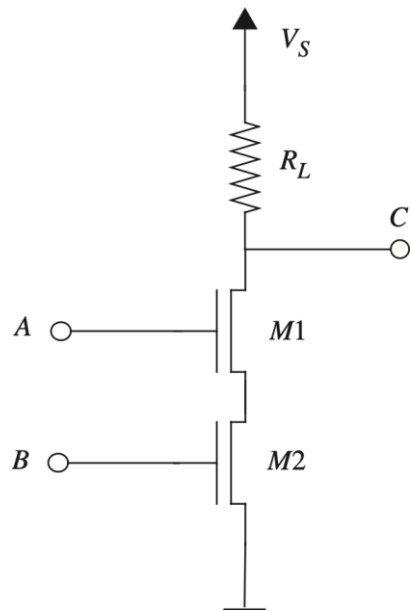


When  $V_A = 1$

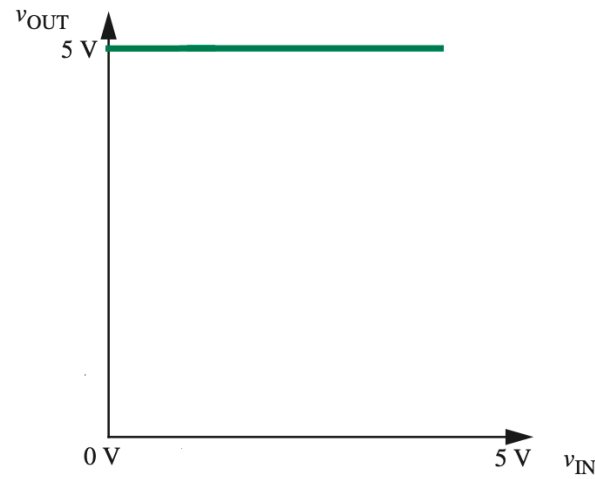


# VTC of NAND gate

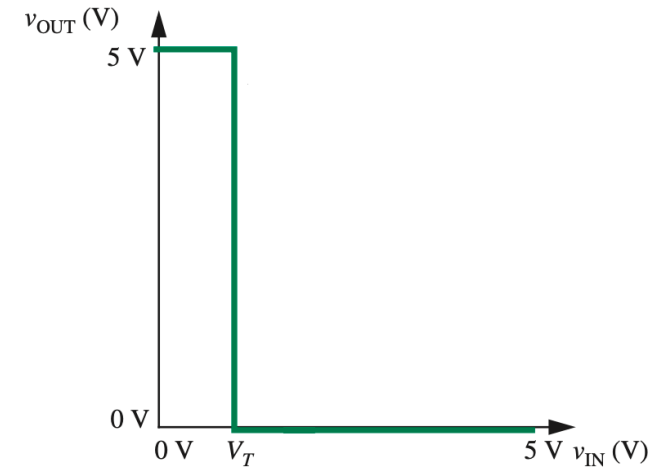
- We only have one  $x$  –axis, but two inputs
- **Solution:** Draw two VTC, one considering  $V_A = 0$  one considering  $V_A = 1$



When  $V_A = 0$



When  $V_A = 1$

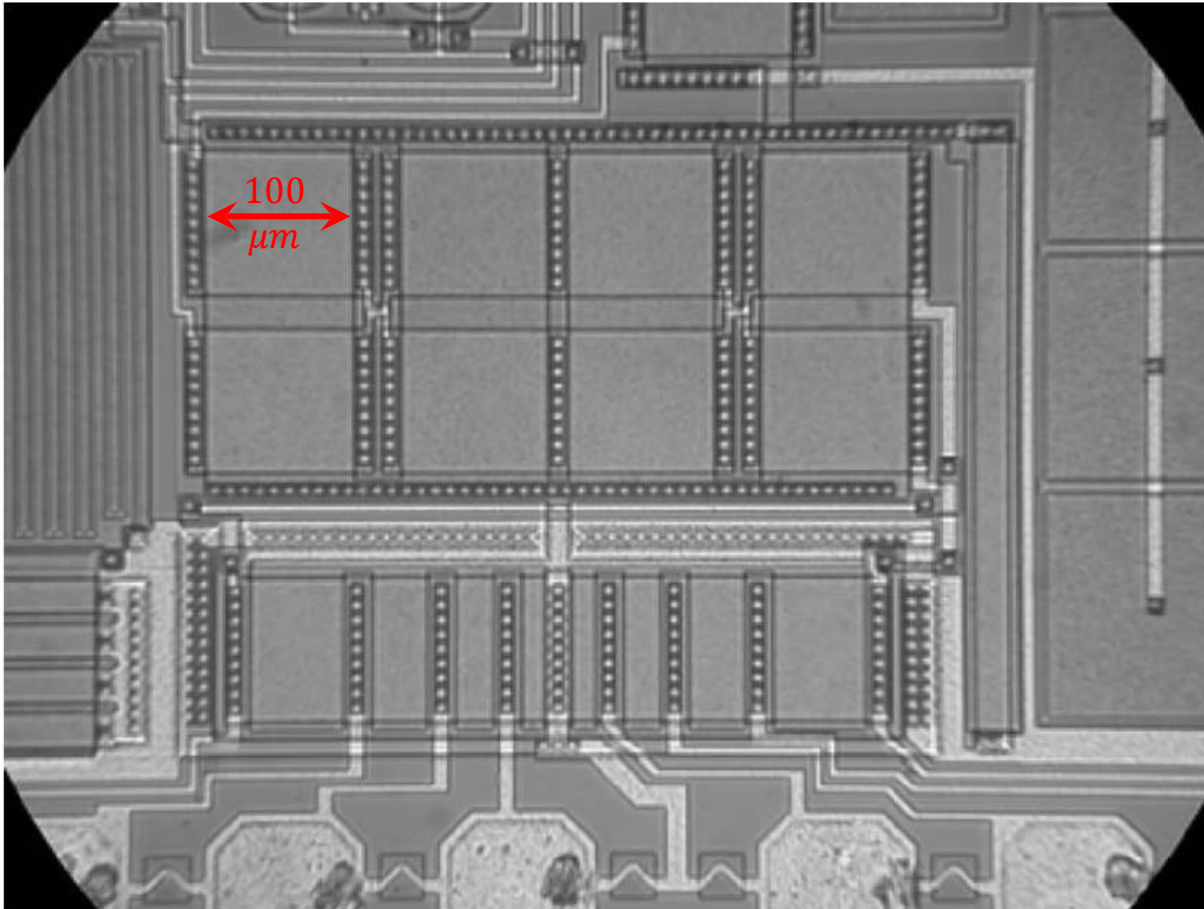


**Homework:** Find VTC for NOR gate

# Outline

- Constructing a \*real\* MOSFET – n/p-channel
- **Operation of an MOSFET-**
  1. Cut-Off
  2. Saturation
  3. Triode Mode
- Output Characteristics
- PWL Model and Non-ideal Analysis: **SR model**
- Real MOSFET equations
- Introduction to Static analysis

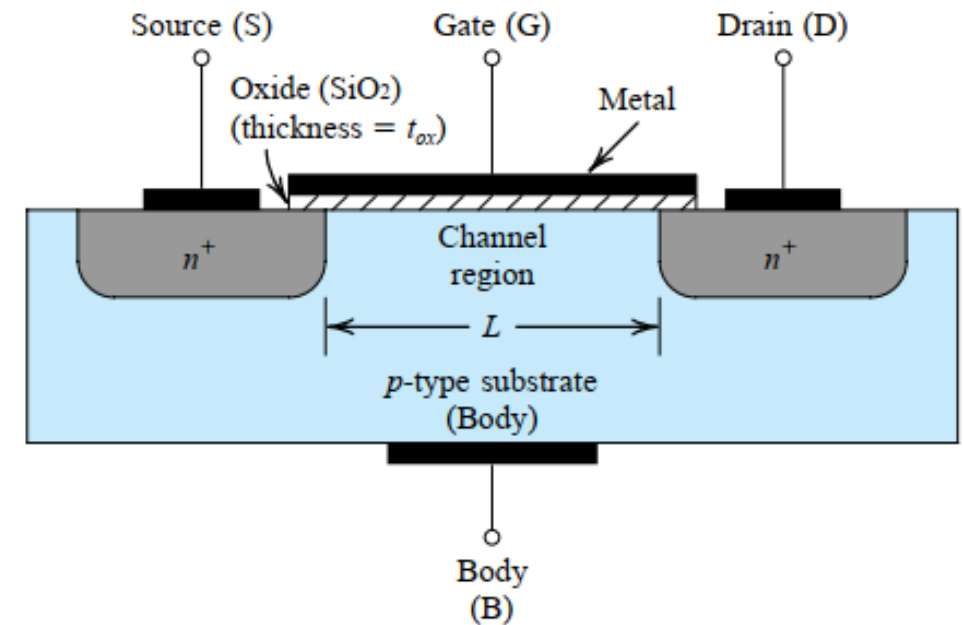
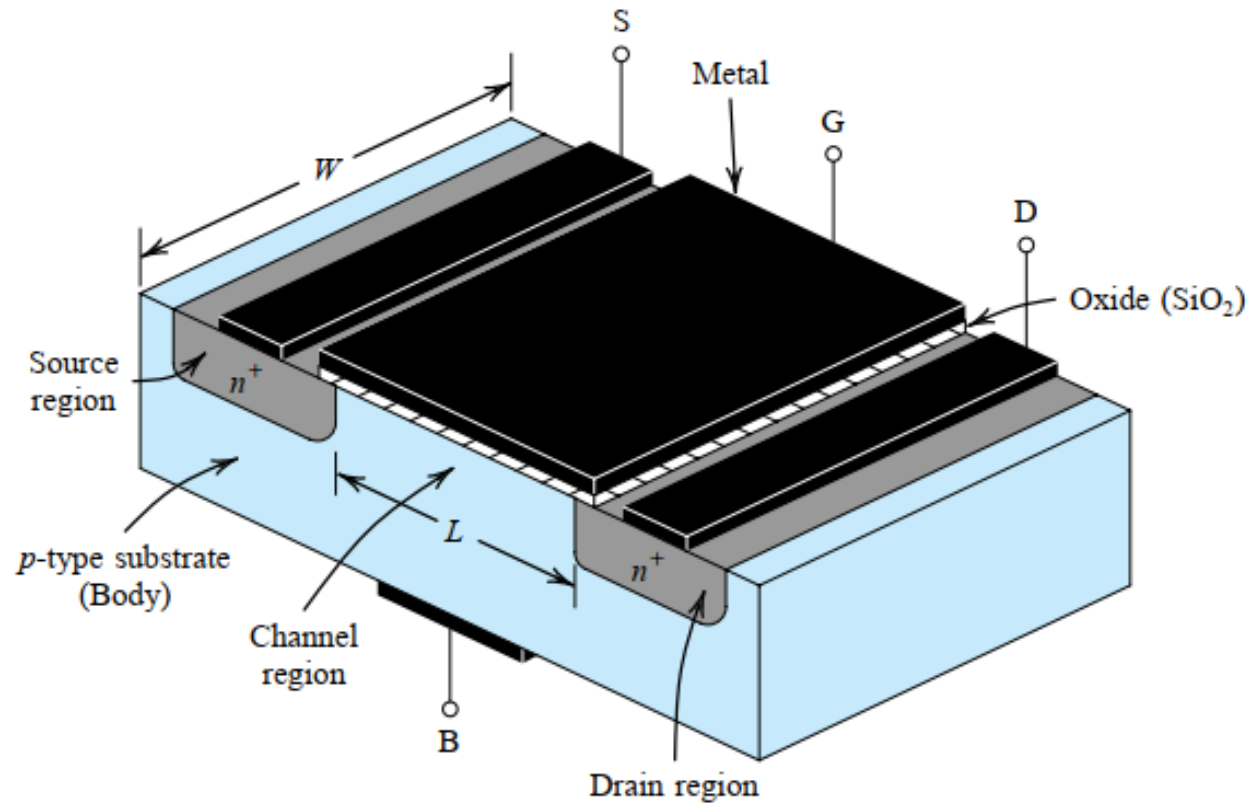
# Construction of Real MOSFET



Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100  $\mu\text{m}$ . (Photograph Courtesy of Maxim Integrated Products.)

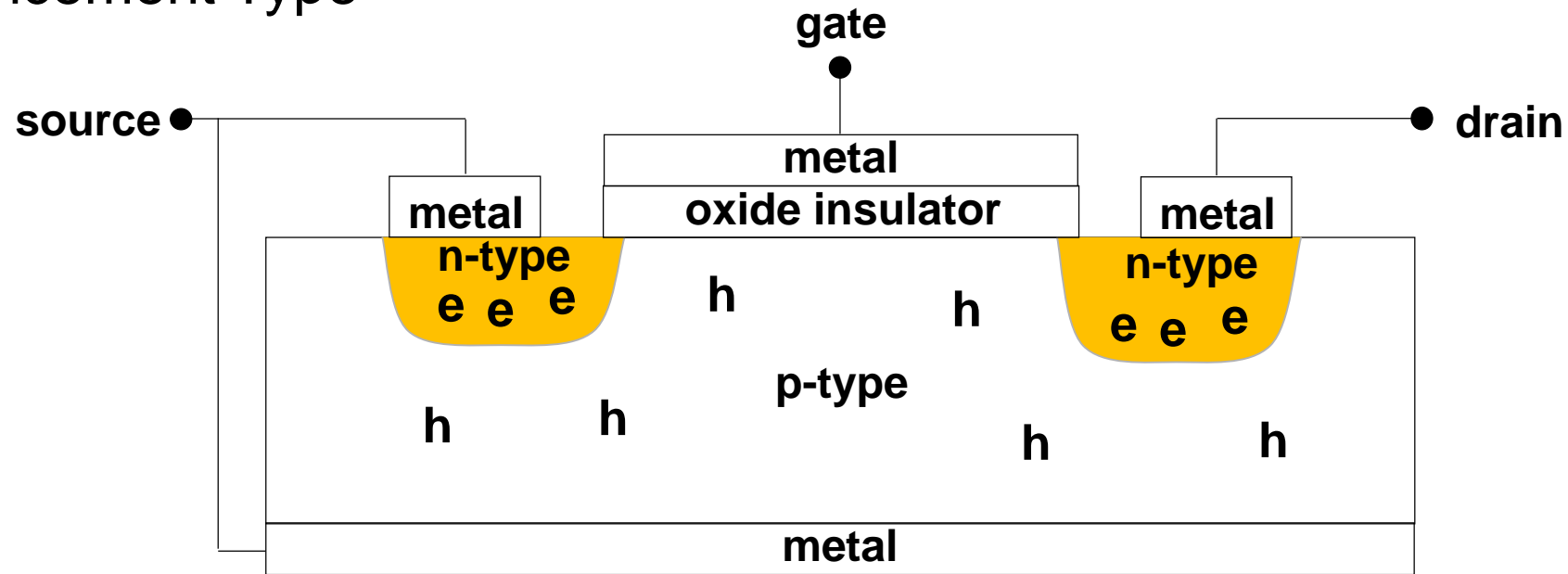
# Real MOSFET – Enhancement Type

## Device Structure (*n*-channel MOSFET)

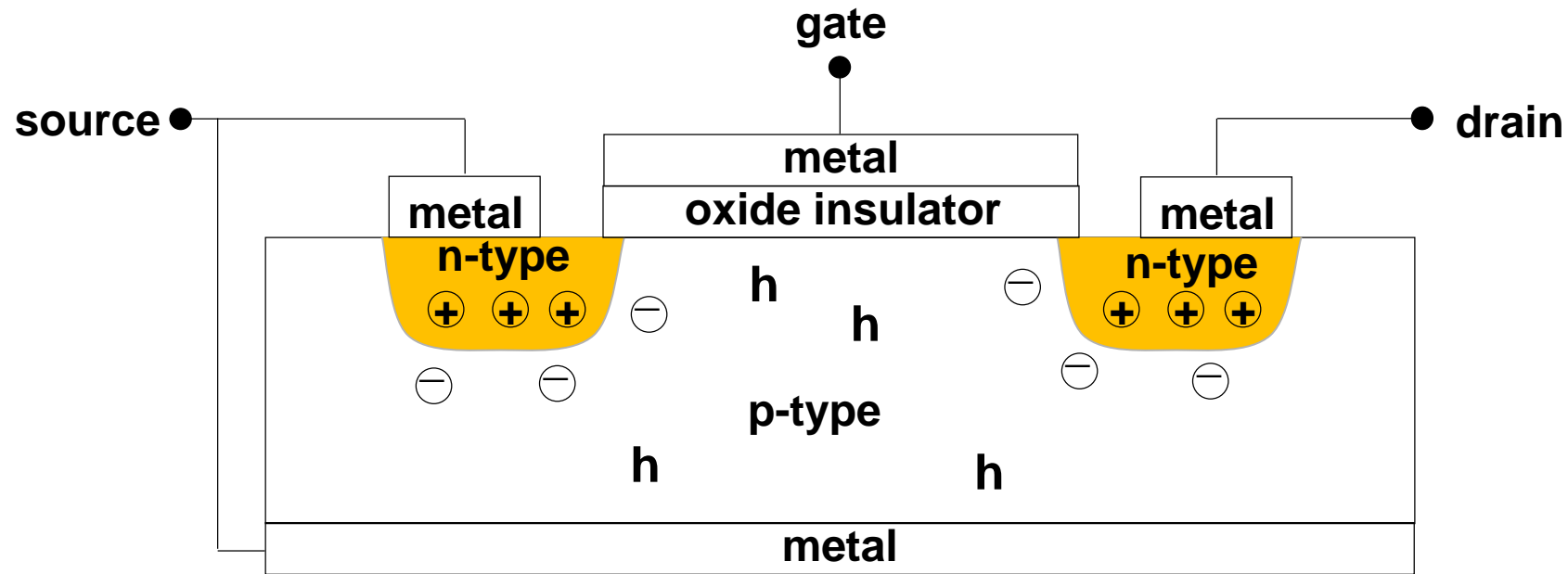


# *n*-channel MOSFET (NMOS) Physical Structure

Enhancement Type



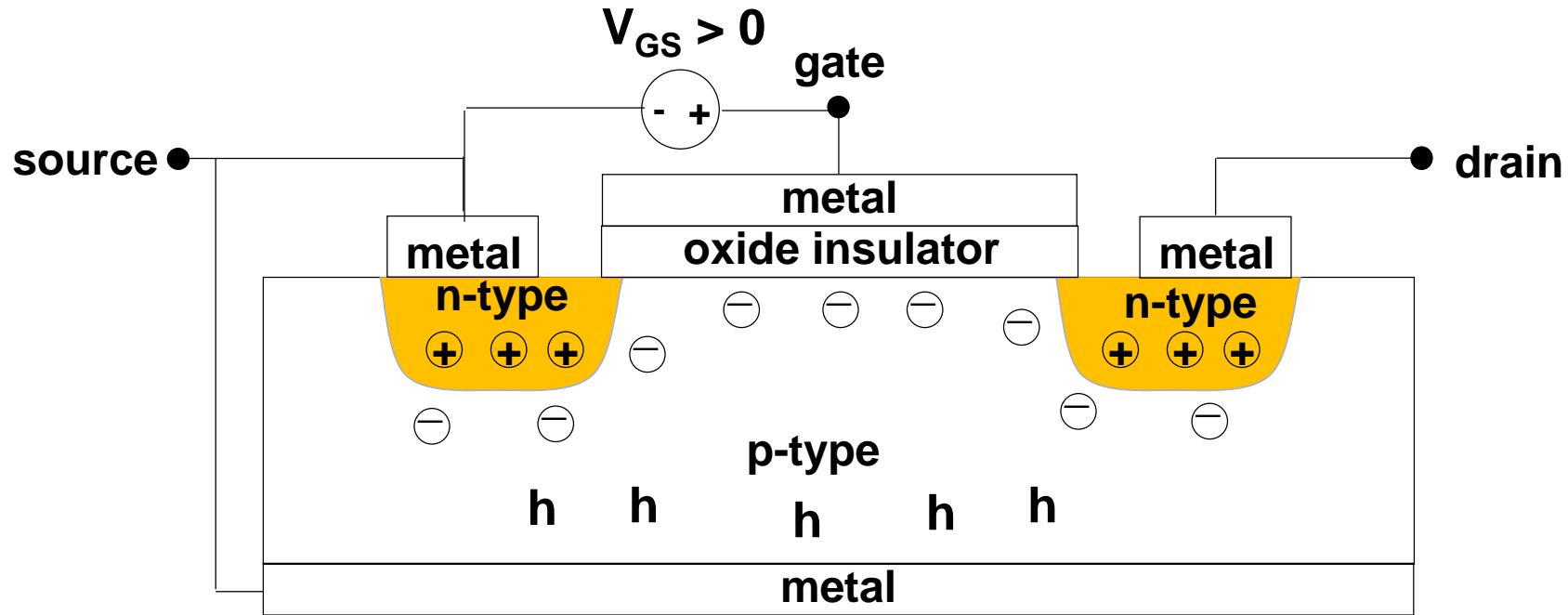
# NMOS in Equilibrium



When the transistor is left alone, some electrons from the n-type wells diffuse into the p-type material to fill holes.

This creates negative ions in the p-type material and positive ions are left behind in the n-type material.

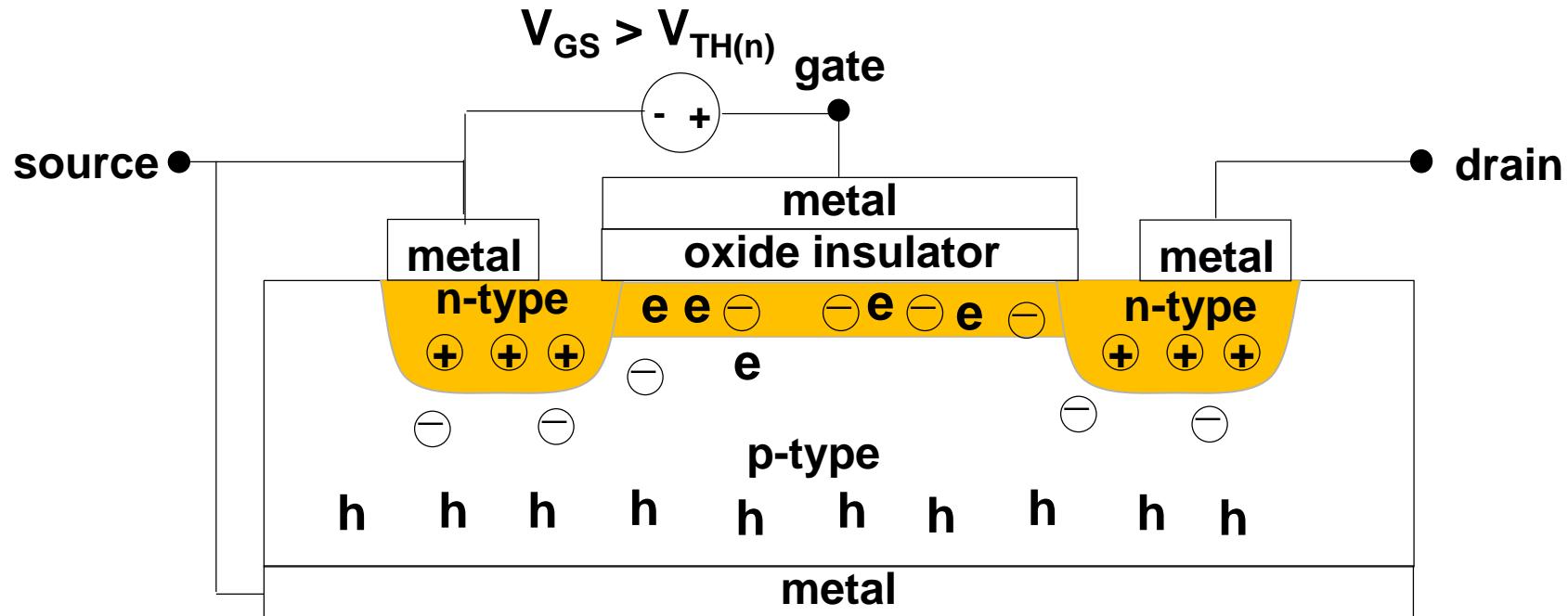
# NMOS in Cutoff



When a small, positive  $V_{GS}$  is applied, holes “move away” from the gate.

Electrons from complete atoms elsewhere in the p-type material move to fill holes near the gate instead.

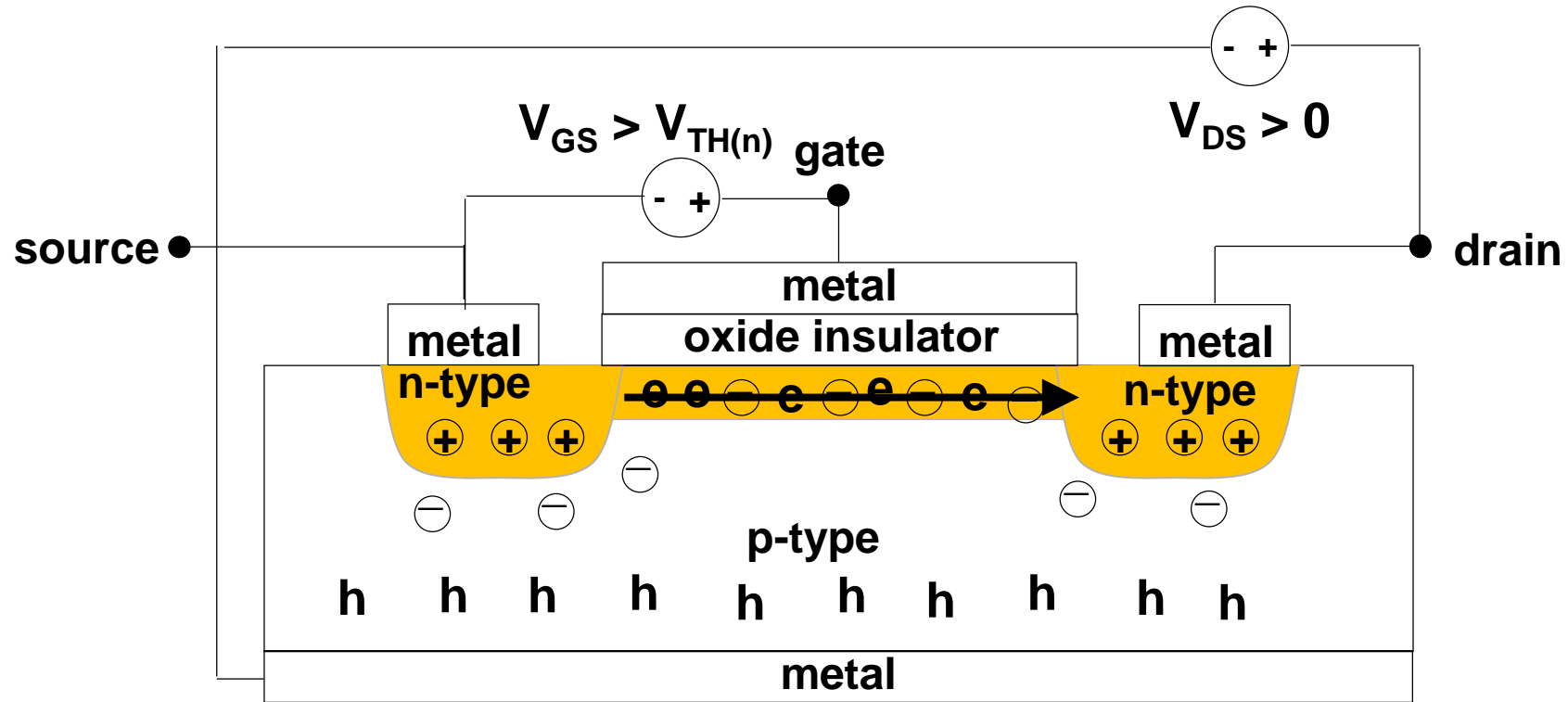
# NMOS Transistor channel



When  $V_{GS}$  is larger than a **threshold** voltage  $V_{TH(n)}$ , the attraction to the gate is so great that free electrons collect there.

The applied  $V_{GS}$  creates an **induced n-type channel** under the gate (an area with free electrons).

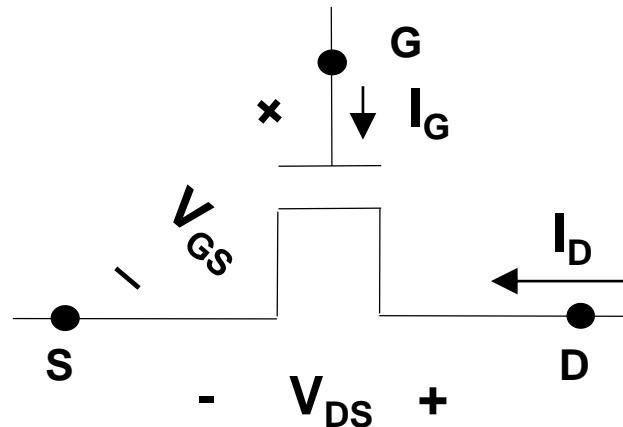
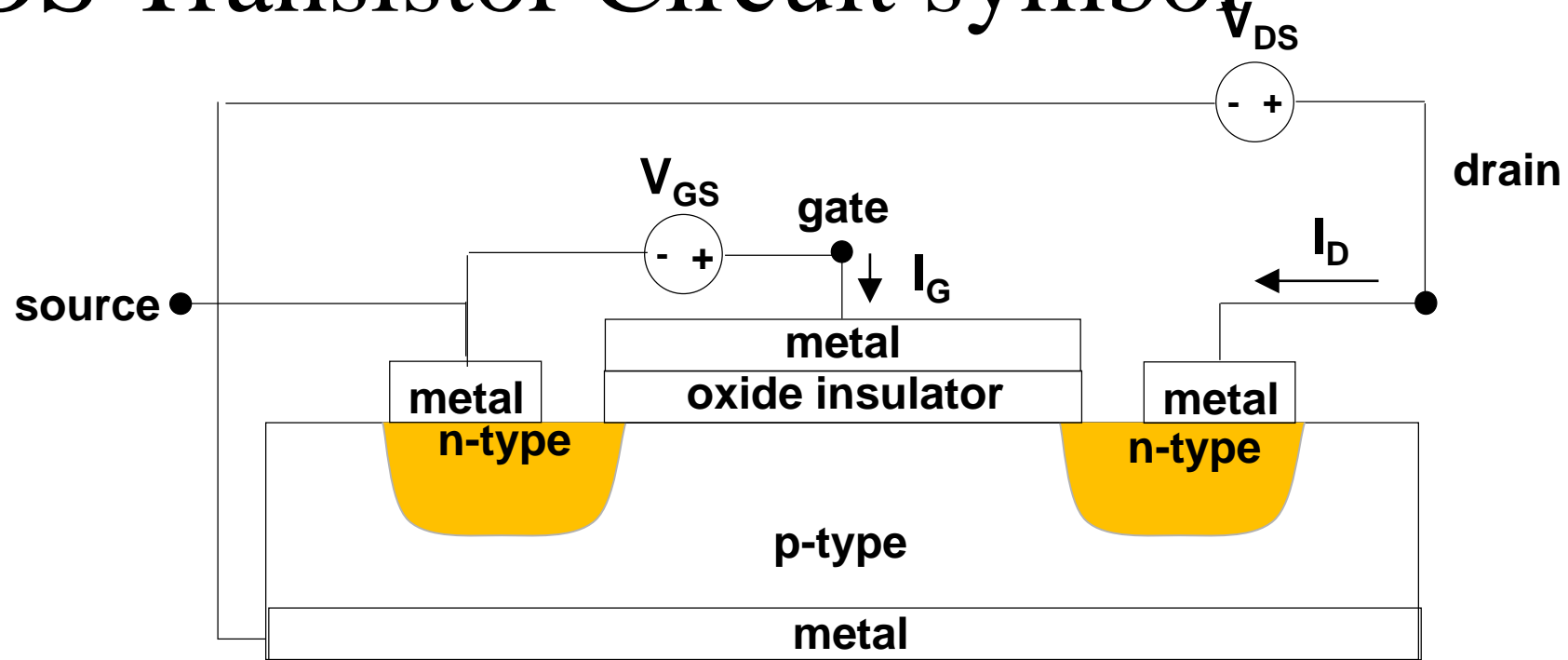
# NMOS Transistor Drain Current



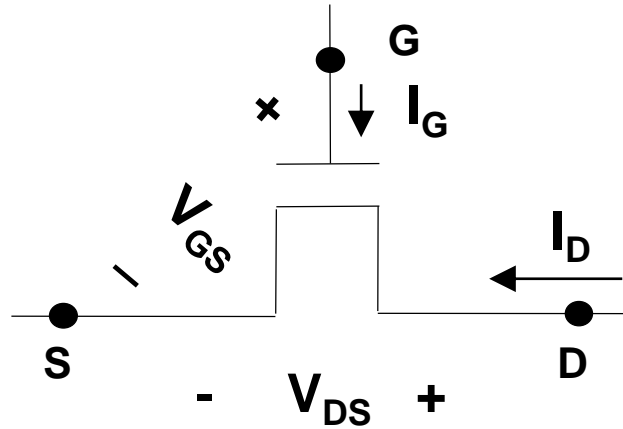
When a positive  $V_{DS}$  is applied, the free electrons flow from the source to the drain. (Positive current flows from drain to source).

The amount of current depends on  $V_{DS}$ , as well as the number of electrons in the channel, channel dimensions, and material.

# NMOS Transistor Circuit symbol



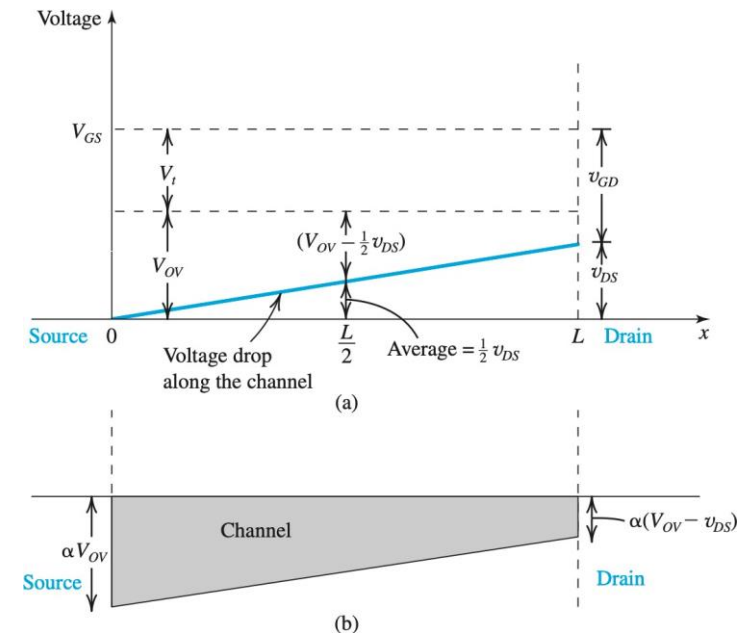
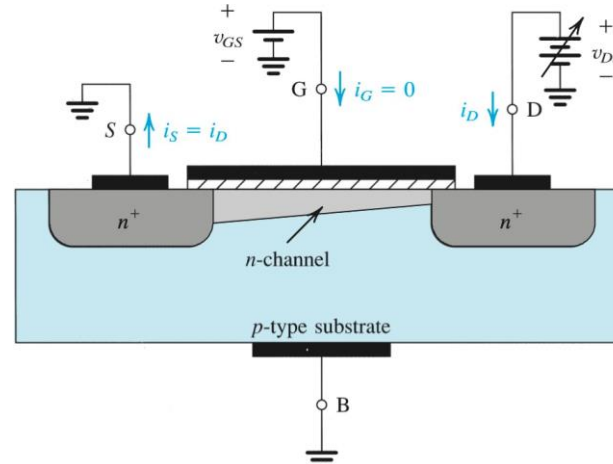
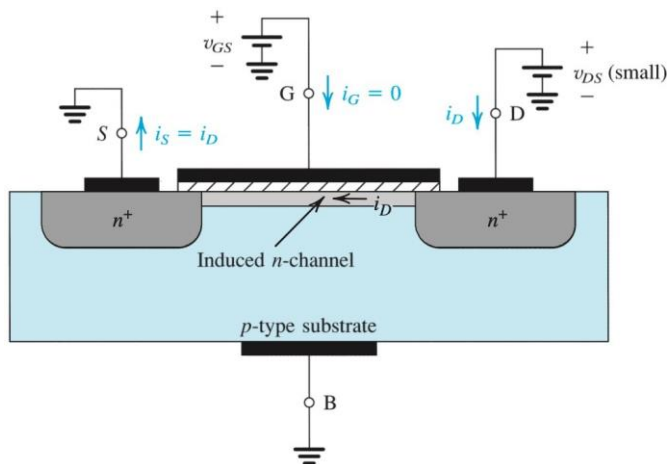
# NMOS I-V Characteristic



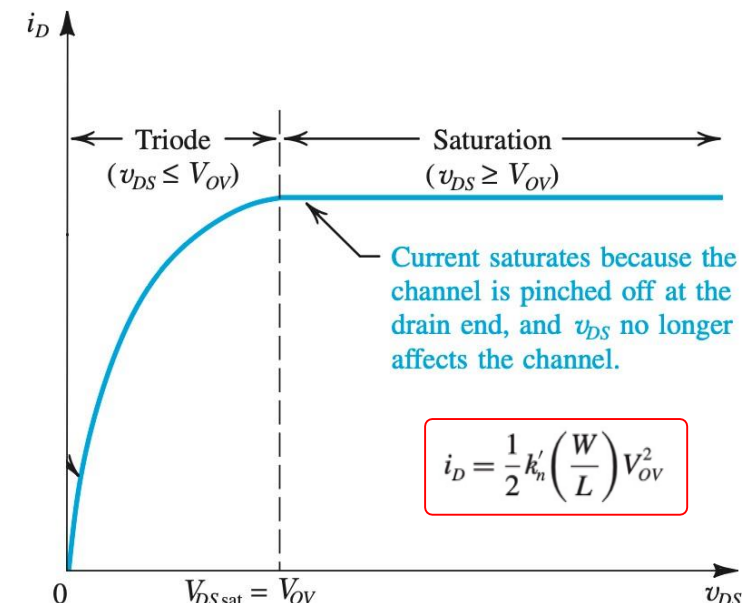
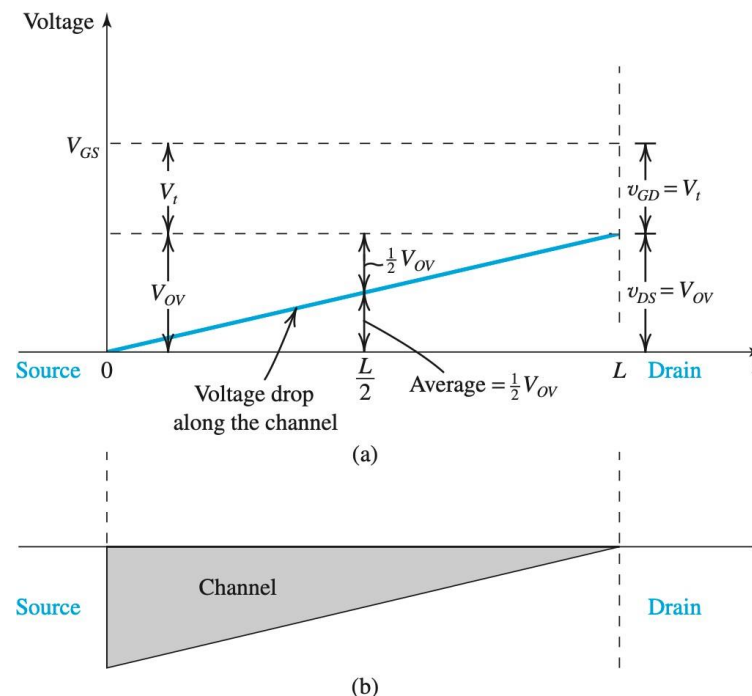
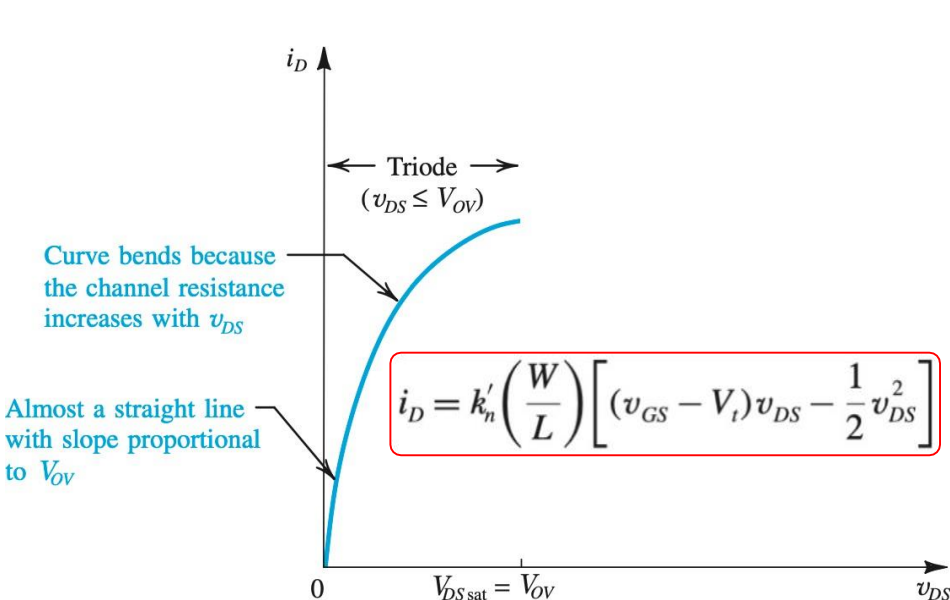
- Since the transistor is a 3-terminal device, there is no single I-V characteristic.
- Note that because of the insulator,  $I_G = 0$  A.
- We typically define the MOS I-V characteristic as  $I_D$  vs.  $V_{DS}$  for a fixed  $V_{GS}$ .
- The I-V characteristic changes as  $V_{GS}$  changes.

# Real MOSFET

- For small  $V_{DS}$ , uniform channel, hence fixed  $R_{ON}$  therefore SR model valid.
- As  $V_{DS}$  is increased, channel becomes tapered cause  $V_{GD} \downarrow$ . Resistance  $\uparrow$ , slope  $\downarrow$ .
- This mode is called the **triode mode**. Condition:  $V_{DS} < V_{OV}$



# Real MOSFET



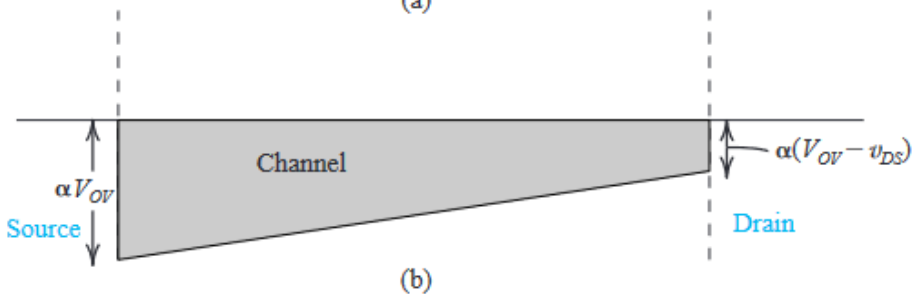
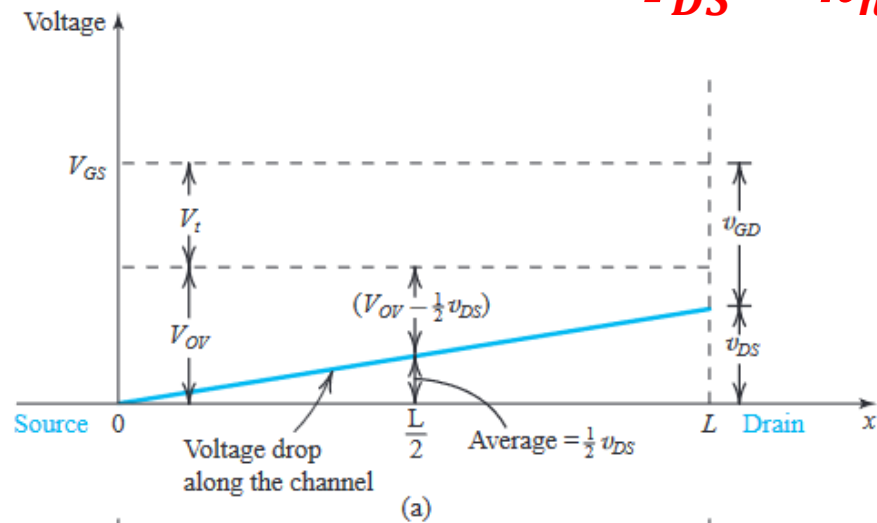
- When  $V_{DS} = V_{OV}$ , channel pinches off.
- Increasing  $V_{DS}$  further have no effect on channel shape. Hence, current saturates
- This mode is called the **saturation mode**. Condition:  $V_{DS} \geq V_{OV}$
- Behaves like a current source (constant current) that depends on  $V_{OV}$ ,

# NMOS Triode Mode

Occurs when  $v_{GS} \geq V_T$  and  $v_{DS} < v_{GS} - V_T$

$$I_{DS} = k_n \left( v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS}$$

$$\begin{aligned} I_{DS} &\propto k'_n \\ I_{DS} &\propto \frac{W}{L} \\ I_{DS} &\propto (V_{OV} - \frac{1}{2} v_{DS}) \end{aligned}$$



Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

In triode mode, average voltage across channel is actually:

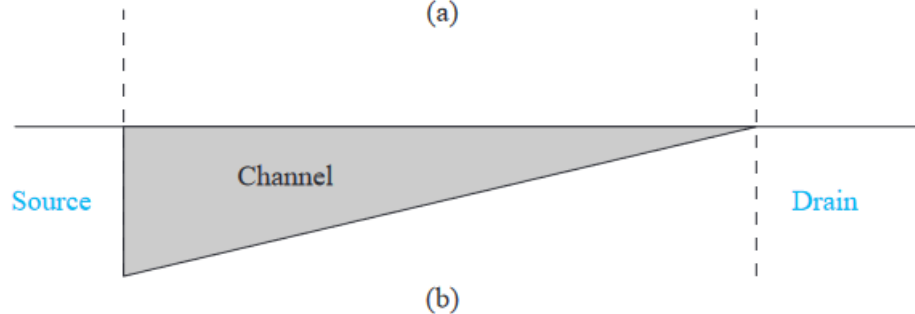
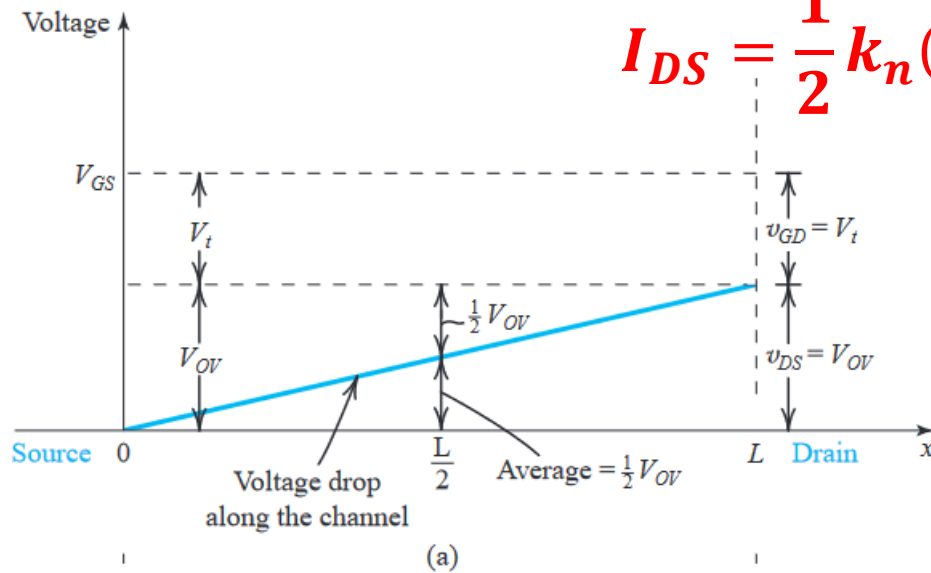
$$(V_{OV} - \frac{1}{2} v_{DS})$$

# NMOS Saturation mode

Occurs when  $v_{GS} > V_T$  and  $v_{DS} \geq v_{GS} - V_T$

$$I_{DS} = \frac{1}{2} k_n (v_{GS} - V_T)^2 = \frac{1}{2} k_n V_{OV}^2$$

$$\begin{aligned} I_{DS} &\propto k'_n \\ I_{DS} &\propto \frac{W}{L} \end{aligned}$$



Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

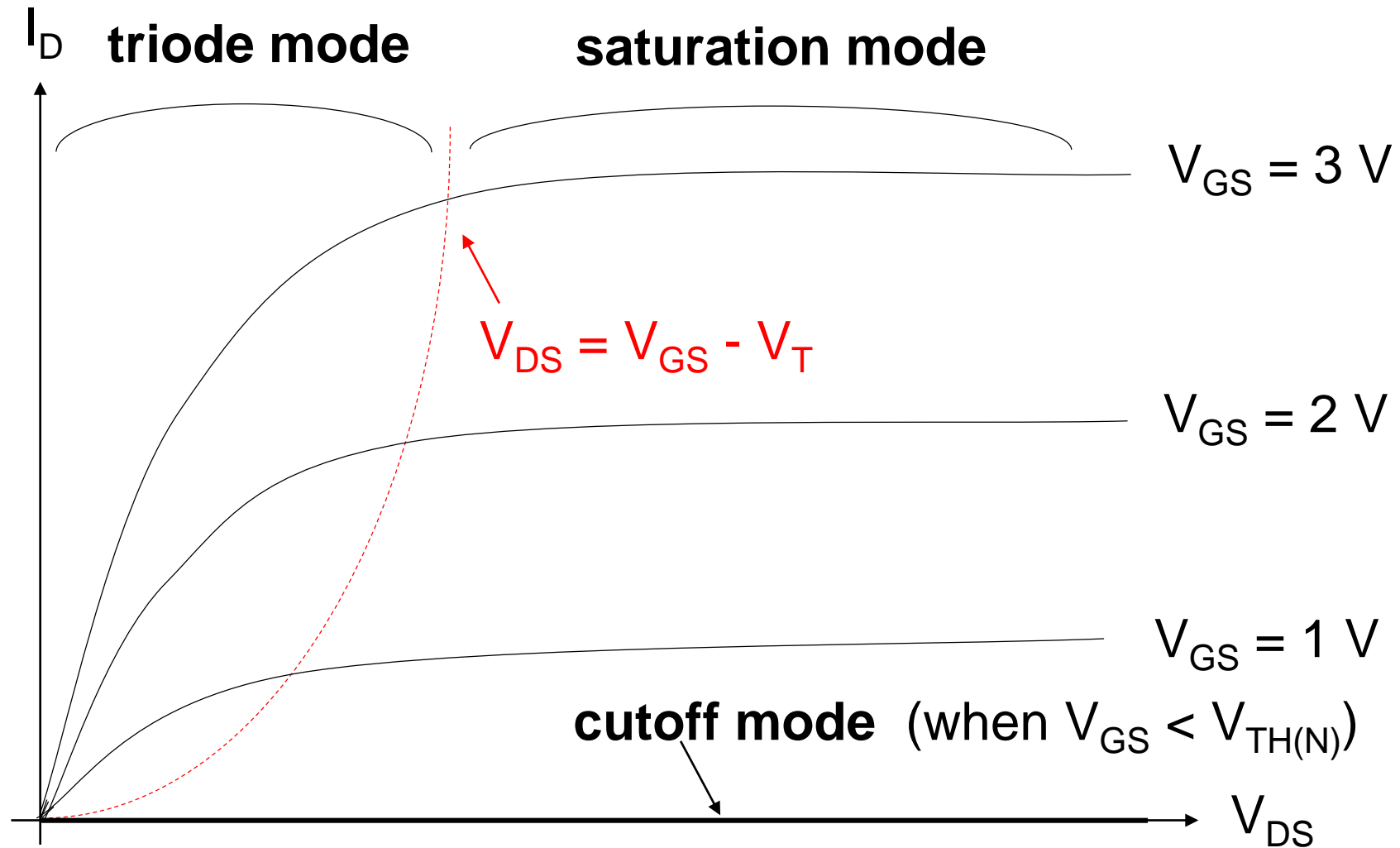
In **Saturation** mode, average voltage across channel fixed at:

$$\frac{1}{2} V_{OV}$$

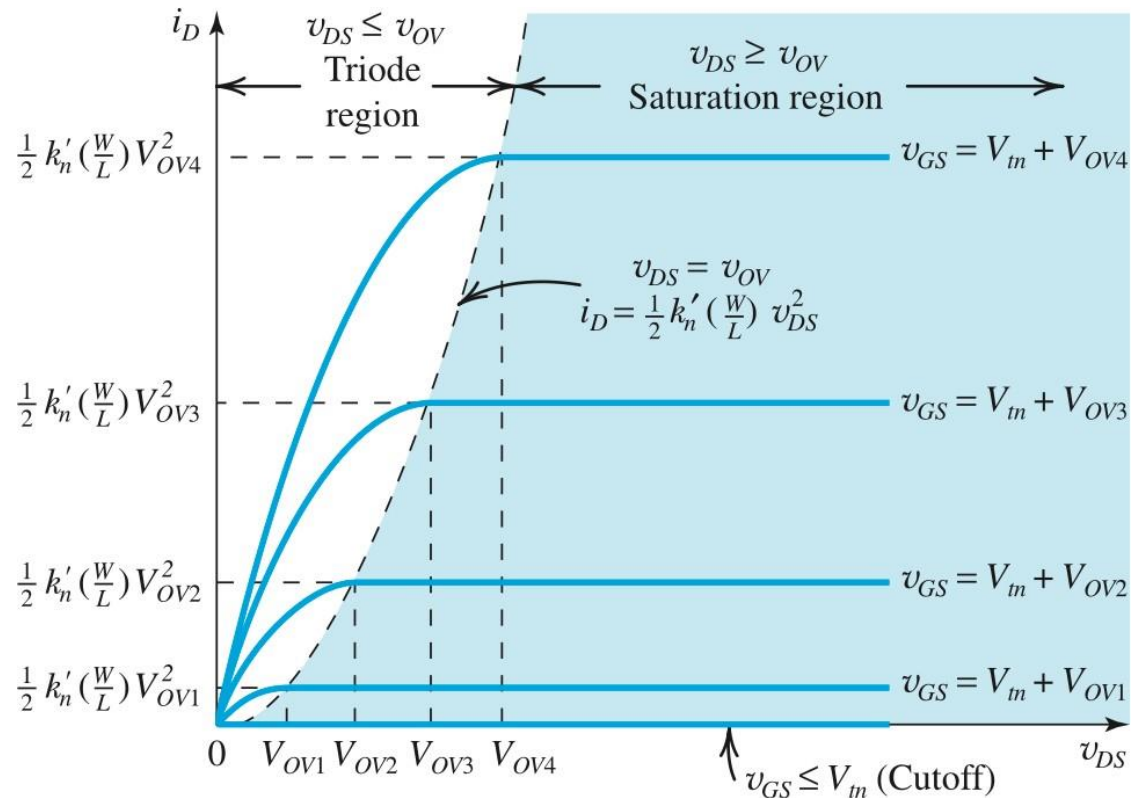
# Modes of Operation

- For small values of  $V_{GS}$ ,  $V_{GS} \leq V_{TH(n)}$ , the n-type channel is not formed. No current flows. This is **cutoff mode**.
- When  $V_{GS} > V_{TH(n)}$ , current  $I_D$  may flow from drain to source, and the following modes of current flow are possible.
  - The mode of current flow depends on the propelling voltage,  $V_{DS}$ , and the channel-inducing voltage,  $V_{GS} - V_{TH(n)}$ .
  - When  $V_{DS} < V_{GS} - V_{TH(n)}$ , current is starting to flow.  $I_D$  increases rapidly with increased  $V_{DS}$ . This is **triode mode**.
  - When  $V_{DS} \geq V_{GS} - V_{TH(n)}$ , current is reaching its maximum value.  $I_D$  does not increase much with increased  $V_{DS}$ . This is called **saturation mode**.

# NMOS I-V Characteristic



# IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \geq V_T$ $V_{DS} < V_{OV}$	$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$
Saturation	$V_{GS} \geq V_T$ $V_{DS} \geq V_{OV}$	$I_D = \frac{k}{2}V_{OV}^2$

$$V_{GS} - V_T = V_{OV}$$

$$k_n = \frac{k'_n W}{L}$$

# NMOS Equations

## Cutoff Mode

Occurs when  $v_{GS} < V_T$

$$I_D = 0$$

$v_{GS} - V_T = V_{OV}$ : Overdrive Voltage

## Triode Mode

Occurs when  $v_{GS} \geq V_T$  and  $v_{DS} < v_{GS} - V_T$

$$I_{DS} = k'_n \frac{W}{L} \left( v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS}$$

$V_{OV}$   
Indicates the available excess voltage at **gate** after forming the n-channel.

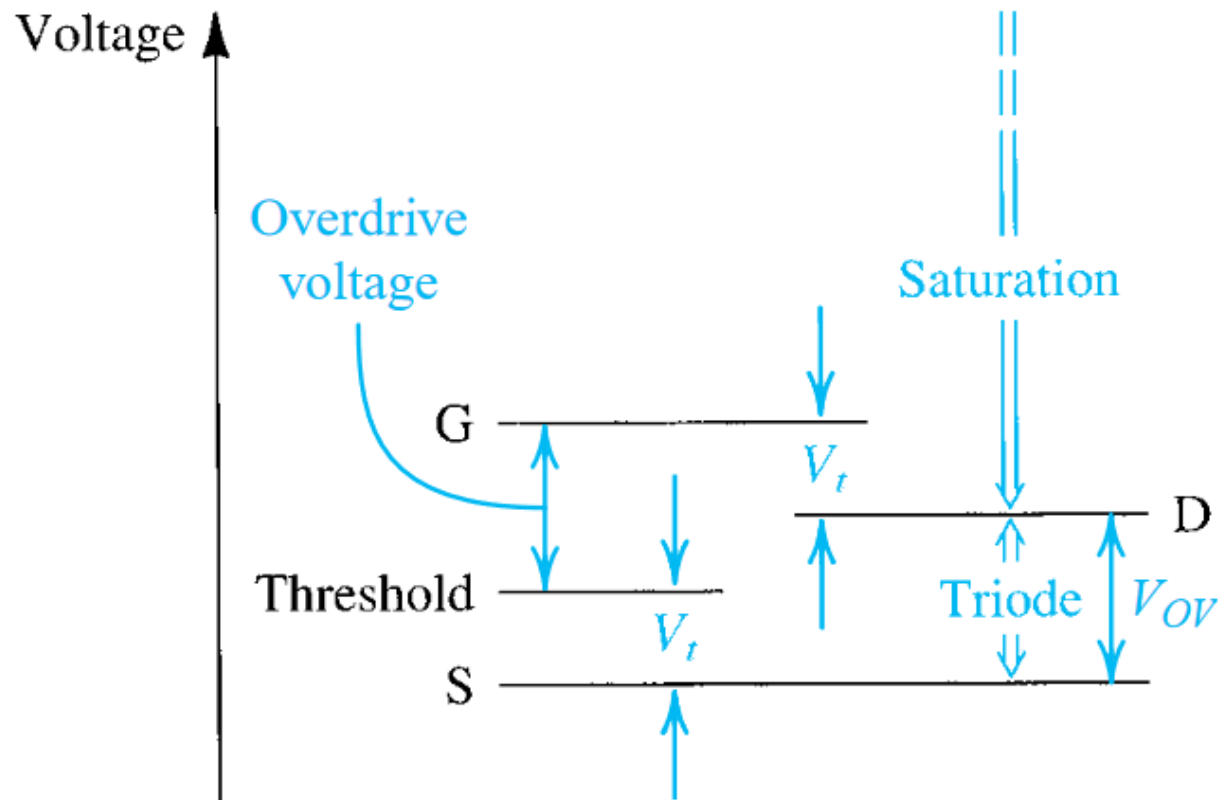
## Saturation Mode

Occurs when  $v_{GS} > V_T$  and  $v_{DS} \geq v_{GS} - V_T$

$$I_{DS} = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_T)^2$$

$V_T$   
The minimum voltage necessary at the **gate** terminal to form a channel.

# Real MOSFET



$$k_n = k'_n \frac{W}{L}$$

MOSFET  
transconductance

$v_{GS}$ :

Gate Voltage

$v_{DS}$ :

Drain to Source Voltage

$V_T$ :

Threshold Voltage

$V_{OV} = v_{GS} - V_T$ :

Overdrive voltage

# Solving Circuits with MOSFET

- Use **Method of Assumed State!**
- Three steps:
  - **Assume:** One of the modes (Cutoff, Triode, Saturation)
  - **Solve:** Use corresponding equation and KCL+KVL
  - **Verify:** Check if the conditions of  $V_{DS}$  and  $V_{GS}$  are satisfied. If not, repeat.
- Might need to solve quadratic equation ( $ax^2 + bx + c = 0$ ).
- If we get two roots, choose the one that's *favorable* to your assumption

# Example 1

Analyze the circuit to find  $i_D$  and  $v_{o2}$  using the Method of Assumed State. Here, the input of the MOSFET is  $v_{o1} = 1\text{ V}$ . You must validate your assumptions.

## Assume:

Let **MOSFET** be in **Saturation** mode:

$$v_{o1} > V_T$$

$$v_{DS} \geq v_{GS} - V_T \text{ or } v_{o2} \geq 0.8\text{ V}$$

## Solve:

$$v_{o1} - V_T = 1 - 0.2 = 0.8\text{ V}$$

Current Equation:  $I_D = \frac{k}{2}(v_{GS} - V_T)^2 = \frac{4}{2}(0.8)^2 = 1.28\text{ mA}$

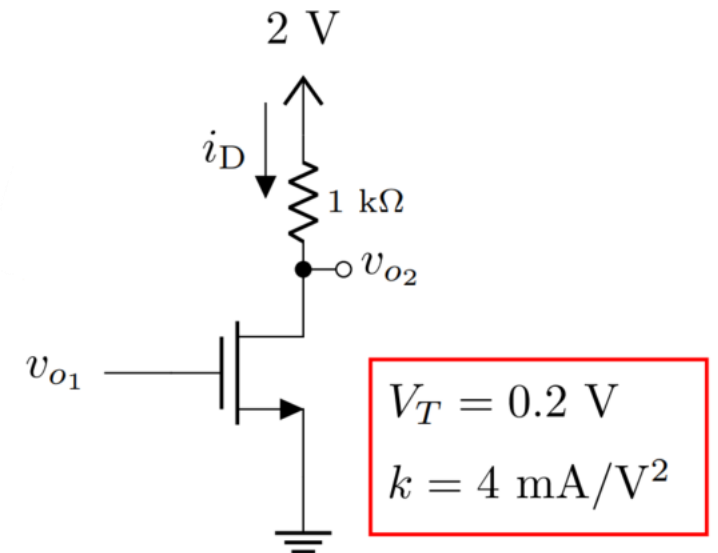
$$v_{o2} = 2 - I_D = 0.72\text{ V}$$

**Verify:** For **Saturation** mode  $\rightarrow v_{o2} \geq 0.8\text{ V}$

But here,  $v_{o2} = 0.72\text{ V} < 0.8\text{ V}$

Here, the conditions are **NOT** fulfilled.

**Assumption is INCORRECT!**



# Example 1

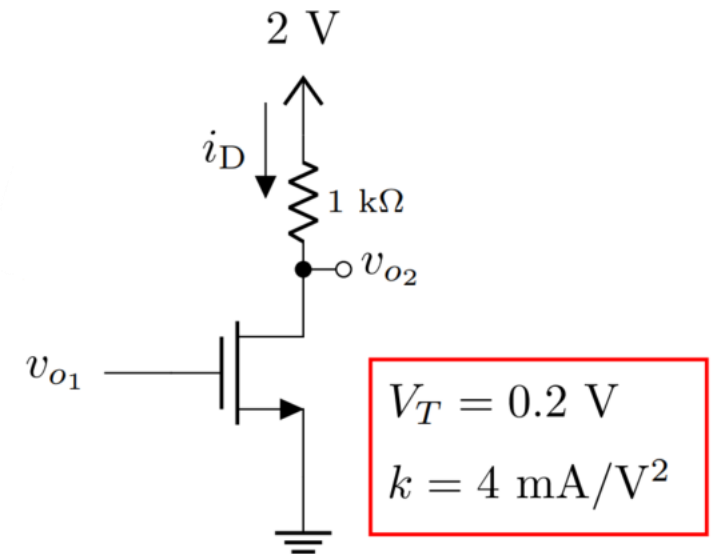
Analyze the circuit to find  $i_D$  and  $v_{o2}$  using the Method of Assumed State. Here, the input of the MOSFET is  $v_{o1} = 1\text{ V}$ . You must validate your assumptions.

$\therefore$  MOSFET is in Triode Mode.

$$I_D = k \left( v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS} = \frac{2 - v_{DS}}{1}$$

$$4 \left( 0.8 - \frac{1}{2} v_{o2} \right) v_{o2} = 2 - v_{o2}$$

$$v_{o2} = \cancel{1.37\text{ V}} \text{ or } 0.73\text{ V}$$



# Example 2

- Design the circuit, that is, determine the values of  $R_D$  and  $R$ , so that the transistor operates at  $I_D = 0.4 \text{ mA}$  and  $V_D = +0.5 \text{ V}$ . The NMOS transistor has  $V_T = 0.7 \text{ V}$ ,  $k = 3.2 \text{ mA/V}^2$ .

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

## Assume:

Let **MOSFET** be in **Saturation** mode:

$$v_{GS} > V_T$$

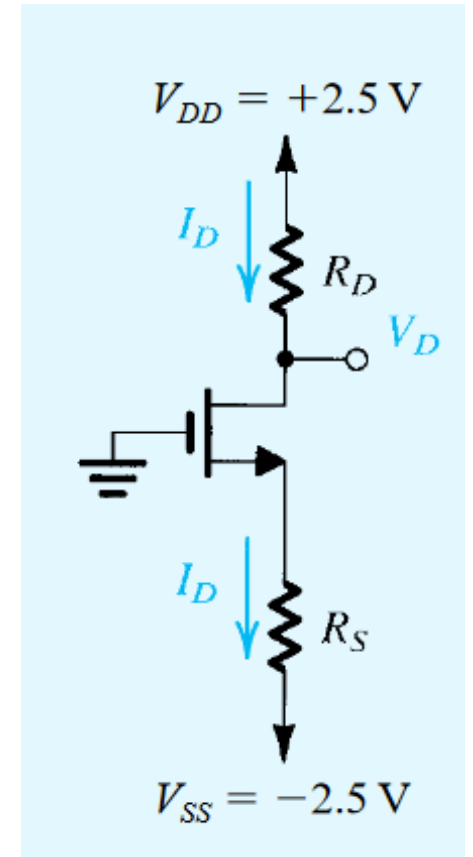
$$v_{DS} \geq v_{GS} - V_T$$

## Solve:

$$\begin{aligned} v_{GS} &= -V_S \\ V_{GS} - V_T &= -V_S - 0.7 \end{aligned}$$

$$\text{Current Equation: } I_D = \frac{k}{2} (v_{GS} - V_T)^2 = \frac{3.2}{2} (-V_S - 0.7)^2 = 0.4 \text{ mA}$$

$$V_S = \text{--0.2 V or --1.2 V}$$



# Example 2

- Design the circuit, that is, determine the values of  $R_D$  and  $R$ , so that the transistor operates at  $I_D = 0.4 \text{ mA}$  and  $V_D = +0.5 \text{ V}$ . The NMOS transistor has  $V_T = 0.7 \text{ V}$ ,  $k = 3.2 \text{ mA/V}^2$ .

**Verify:**

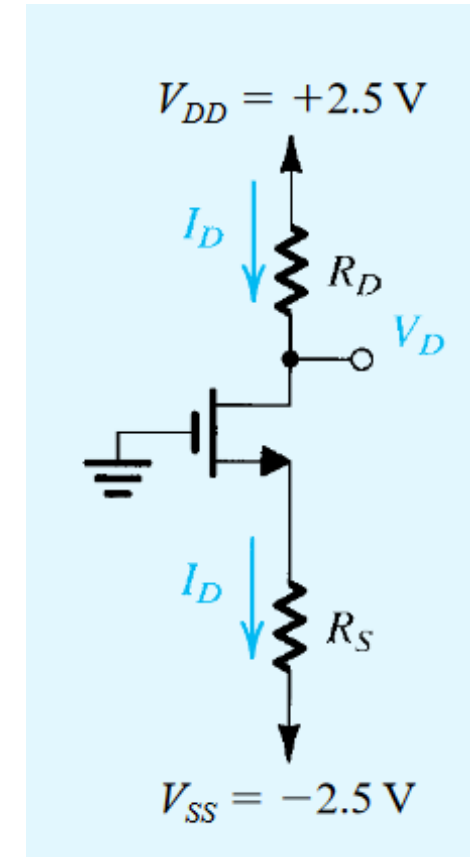
$$V_{DS} = 0.5 - V_S = 1.7 \text{ V}$$
$$V_{GS} - V_T = -V_S - 0.7 = 0.5 \text{ V}$$

**Clearly**

$$V_{DS} \geq V_{GS} - V_T$$

**Assumption is CORRECT!**

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 5.75 \text{ k}\Omega$$



# Example - 3

For the circuit, find the value of  $R$  that results in  $V_D = 0.8$  V. The MOSFET has

$$V_T = 0.5 \text{ V}, k'_n = \mu_n C_{OX} = 0.4 \text{ mA/V}^2, \frac{W}{L} = \frac{0.72 \mu\text{m}}{0.18 \mu\text{m}}$$

$$k_n = k'_n \frac{W}{L} = 1.6 \text{ mA/V}^2$$

**Assume:**

Let MOSFET be **IS** in **Saturation** mode:

**Proof:**

$$V_D = V_G$$

$$V_D - V_S = V_G - V_S$$

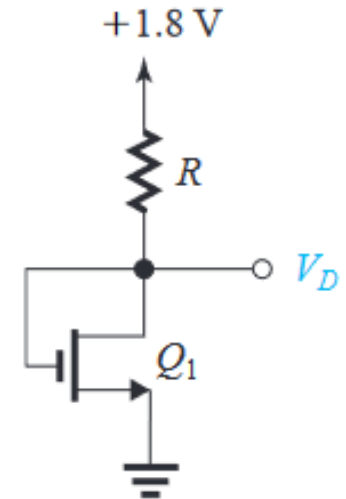
$$V_{DS} = V_{GS} \geq V_{GS} - V_T \rightarrow \text{Saturation Mode}$$

**Solve:**

$$V_{GS} - V_T = V_{DS} - V_T = 0.8 - 0.5 = 0.3 \text{ V}$$

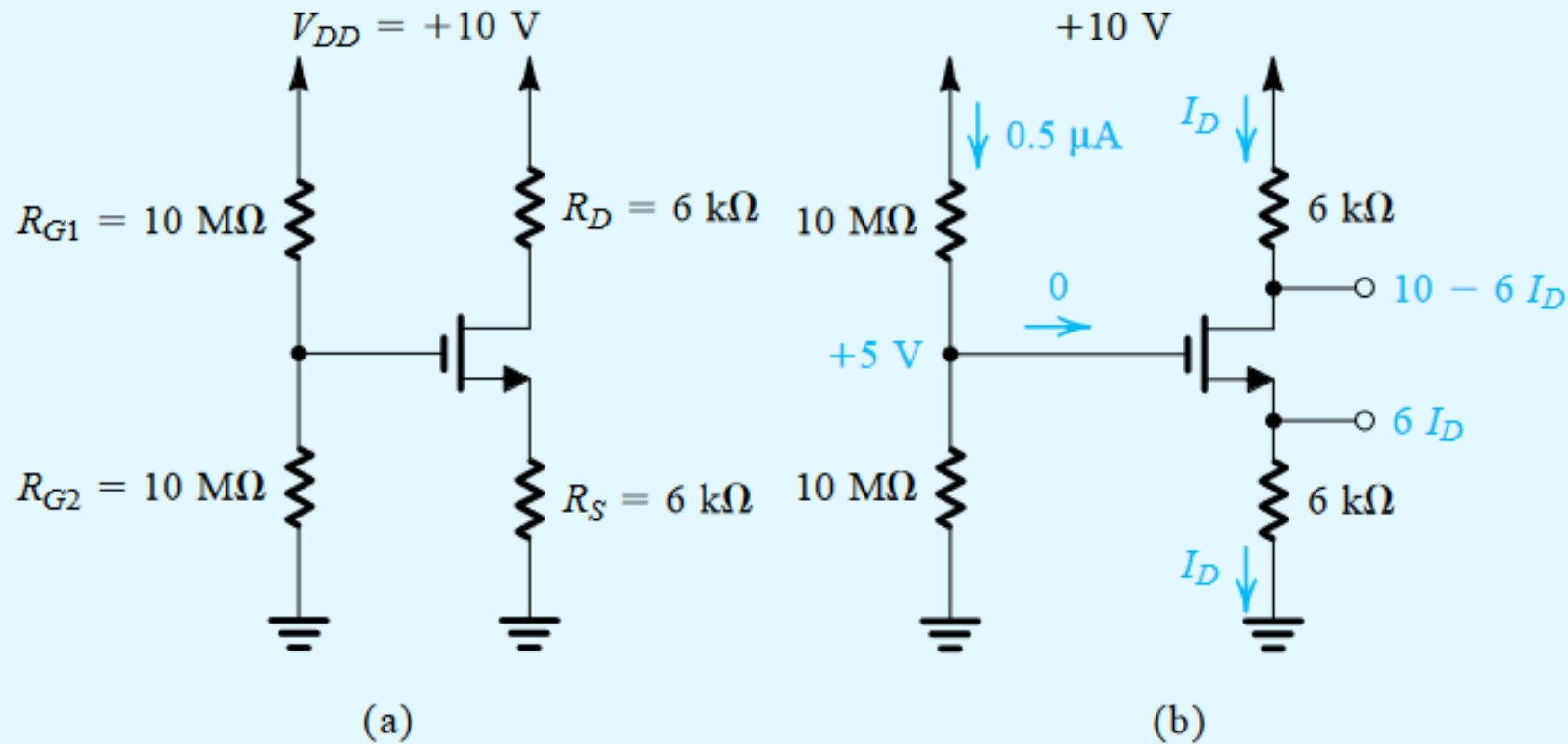
$$\text{Current Equation: } I_D = \frac{k_n}{2} (V_{GS} - V_T)^2 = \frac{1.6}{2} (0.3)^2 = 0.072 \text{ mA}$$

$$R_D = \frac{1.8 - V_D}{I_D} = \frac{1.8 - 0.8}{0.072} = 13.89 \text{ k}\Omega$$



# Example - 4

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let  $V_{tn} = 1$  V and  $k'_n(W/L) = 1$  mA/V<sup>2</sup>. Neglect the channel-length modulation effect (i.e., assume  $\lambda = 0$ ).



# Example - 4

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let  $V_{tn} = 1$  V and  $k'_n(W/L) = 1$  mA/V<sup>2</sup>. Neglect the channel-length modulation effect (i.e., assume  $\lambda = 0$ ).

## Assume:

Let **MOSFET** be in **Saturation** mode:

$$V_{GS} < V_T$$

$$V_{DS} \geq V_{GS} - V_T$$

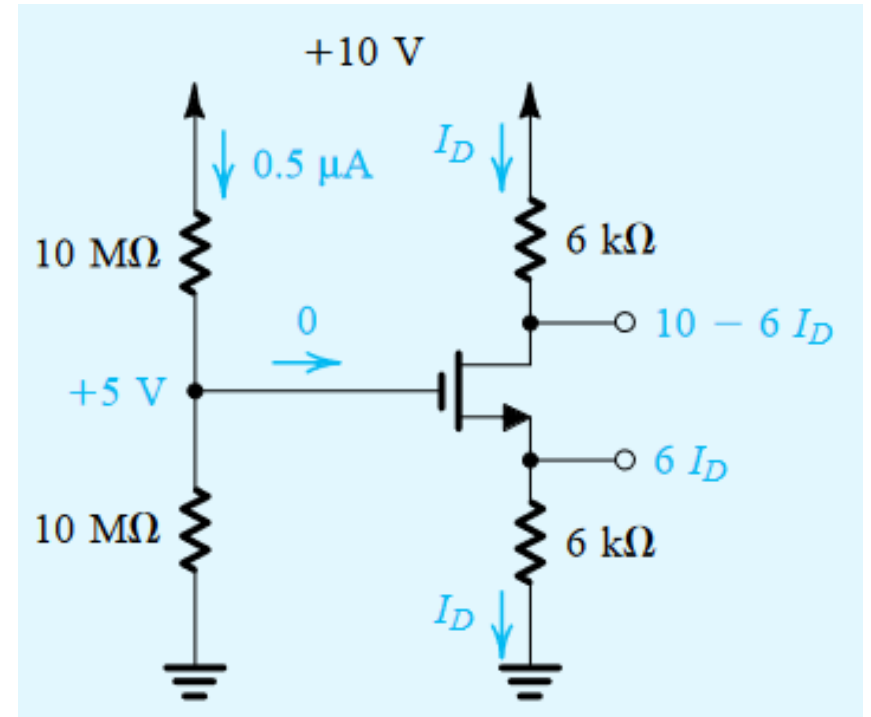
## Solve:

$$I_D = \frac{10 - V_D}{6} = \frac{V_S}{6}$$

Current Equation:  $I_D = \frac{k}{2}(V_{GS} - V_T)^2 = \frac{1}{2}(5 - V_S - 1)^2$

$$I_D = \frac{V_S}{6} = \frac{1}{2}(4 - V_S)^2$$

$$V_S = \cancel{5.33 \text{ V}} \text{ or } 3 \text{ V}$$



# Example - 4

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let  $V_{tn} = 1 \text{ V}$  and  $k'_n(W/L) = 1 \text{ mA/V}^2$ . Neglect the channel-length modulation effect (i.e., assume  $\lambda = 0$ ).

**Verify:**

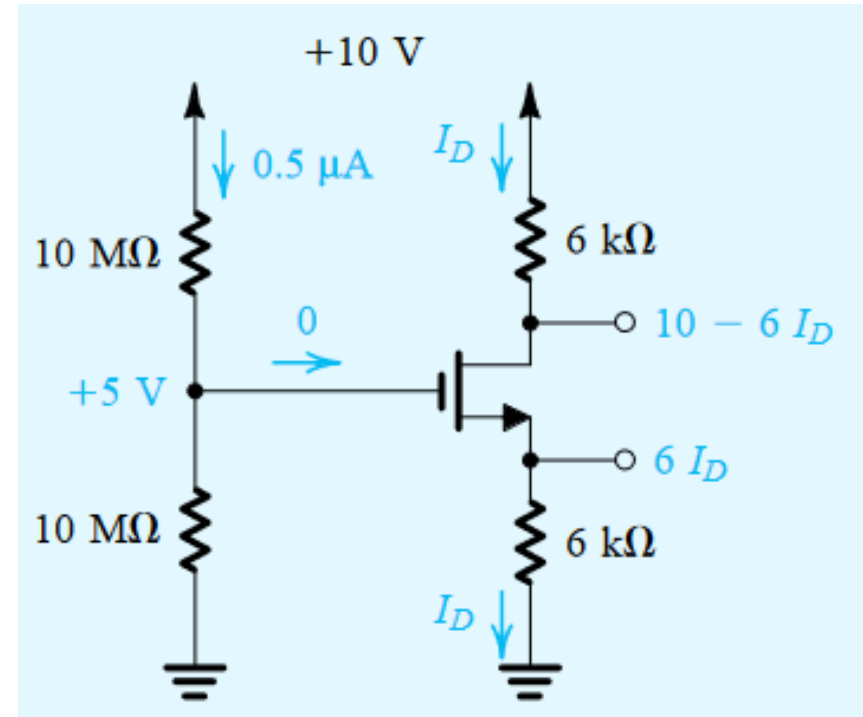
$$I_D = \frac{V_S}{6} = \frac{3}{6} = 0.5 \text{ mA}$$

$$V_D = 10 - 6I_D = 7 \text{ V}$$

$$V_{DS} = V_D - V_S = 7 - 3 = 4 \text{ V}$$

$$V_{GS} - V_T = 4 - V_S = 1 \text{ V}$$

For **Saturation** mode  $\rightarrow V_{DS} \geq V_{GS} - V_T$   
**Assumption is CORRECT!**



# Example - 5

**D 5.50** The NMOS transistors in the circuit of Fig. P5.50 have  $V_t = 0.5$  V,  $\mu_n C_{ox} = 250$   $\mu\text{A}/\text{V}^2$ ,  $\lambda = 0$ , and  $L_1 = L_2 = 0.25$   $\mu\text{m}$ . Find the required values of gate width for each of  $Q_1$  and  $Q_2$ , and the value of  $R$ , to obtain the voltage and current values indicated.

**Solve:**

**Both MOSFET are in SATURATION:**

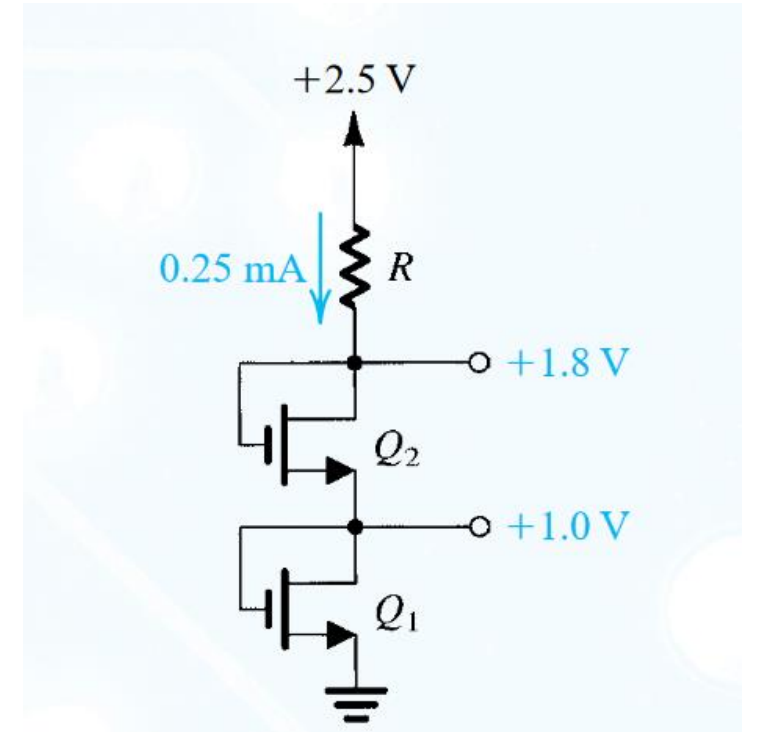
**Q1:**  $V_{GS1} - V_T = 1 - V_T = 1 - 0.5 = 0.5$  V

**Q2:**  $V_{GS2} - V_T = (1.8 - 1) - V_T = 0.8 - 0.5 = 0.3$  V

Current Equation:

$$I_D = \frac{\mu_n C_{ox}}{2} \left( \frac{W_1}{L_1} \right) (V_{GS1} - V_T)^2 = \frac{\mu_n C_{ox}}{2} \left( \frac{W_2}{L_2} \right) (V_{GS2} - V_T)^2 = 0.25 \text{ mA}$$

$$\frac{0.25}{2} \left( \frac{W_1}{0.25} \right) (0.5)^2 = \frac{0.25}{2} \left( \frac{W_2}{0.25} \right) (0.3)^2 = 0.25$$



# Example - 5

**D 5.50** The NMOS transistors in the circuit of Fig. P5.50 have  $V_t = 0.5$  V,  $\mu_n C_{ox} = 250$   $\mu\text{A}/\text{V}^2$ ,  $\lambda = 0$ , and  $L_1 = L_2 = 0.25$   $\mu\text{m}$ . Find the required values of gate width for each of  $Q_1$  and  $Q_2$ , and the value of  $R$ , to obtain the voltage and current values indicated.

$$R = \frac{2.5 - 1.8}{I_D} = 2.8 \text{ k}\Omega$$

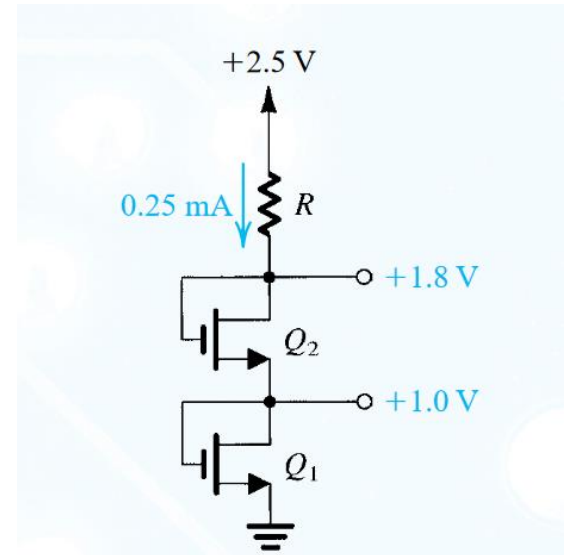
**Solve:**

$$I_D = \frac{\mu_n C_{ox}}{2} \left( \frac{W_1}{L_1} \right) (V_{GS1} - V_T)^2 = \frac{\mu_n C_{ox}}{2} \left( \frac{W_2}{L_2} \right) (V_{GS2} - V_T)^2 = 0.25 \text{ mA}$$
$$\frac{0.25}{2} \left( \frac{W_1}{0.25} \right) (0.5)^2 = \frac{0.25}{2} \left( \frac{W_2}{0.25} \right) (0.3)^2 = 0.25$$

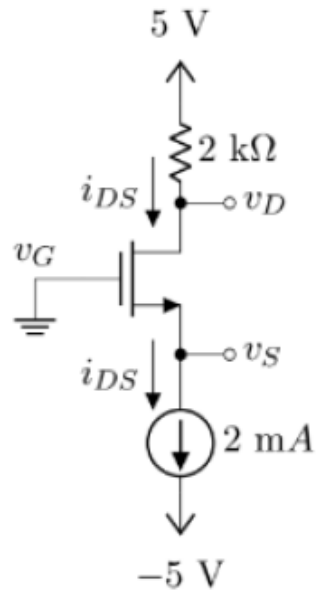
$$W_1 \times 0.25 = W_2 \times 0.09 = 2 \times 0.25$$

$$\frac{W_1}{4} = \frac{9W_2}{100} = \frac{1}{2}$$

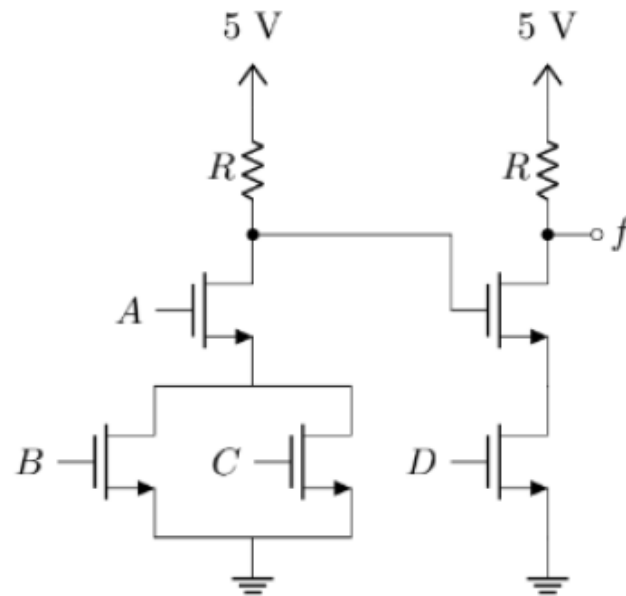
$$W_1 = 2 \text{ } \mu\text{m} \text{ or } W_2 = 5.556 \text{ } \mu\text{m}$$



# Problem 1



Circuit 1



Circuit 2

Refer to the circuit-1 above. For the MOSFET,  $V_T = 1\text{ V}$  and  $K = 4\text{ mA/V}^2$ .

a) **Identify** the value of the gate voltage  $V_G$  and the drain-source current  $i_{DS}$ .

b) **Calculate** the value of the drain voltage  $V_D$  using the  $2\text{ k}\Omega$  resistor.

c) **Analyze** the circuit to find  $V_S$ . Here, use the Method of Assumed State. You must validate your assumptions.

d) **Analyze** the Circuit 2 above to find  $f$  in terms of boolean inputs A, B, C, and D.

$$V_D = 1\text{ V}$$

$$V_{GS} = 2\text{ V}$$

$$V_S = -2\text{ V}$$

$$V_{ov} = 1\text{ V}$$

## Problem 2

In the circuit above, the MOSFETs have the following parameters,  $k_n' = 2 \text{ mA/V}^2$ ,  $W/L = 2.5$ ,  $V_T = 0.5 \text{ V}$ .

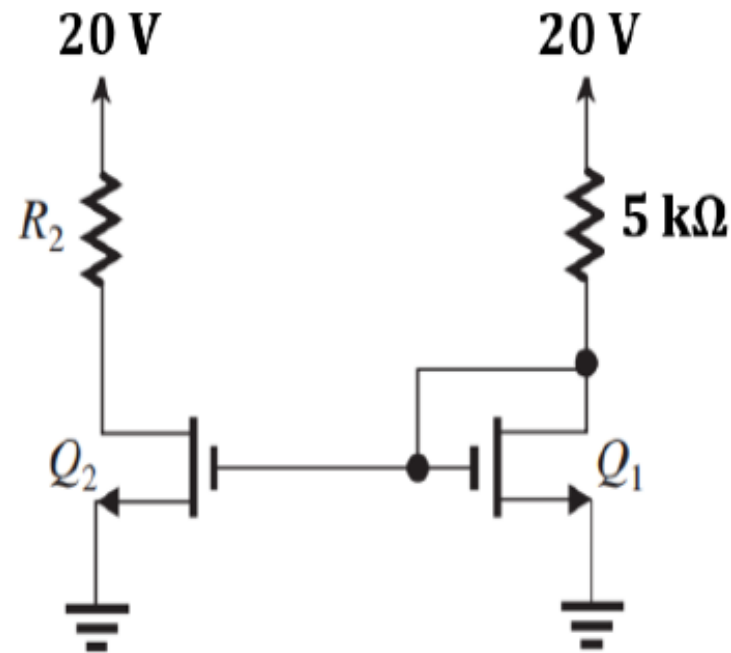
- a) **Find out** the operating mode of  $Q_1$
- b) **Determine** the value of  $R_2$  that results in  $Q_2$  operating at the edge of the saturation region.
- c) **Calculate** the on-state resistance,  $R_{on}$  for  $Q_2$

$$V_{G1} = 1.71 \text{ V or } -0.79 \text{ V}$$

$$V_{G1} = V_{G2} = 1.71 \text{ V}$$

$$V_{DS2} = 1.21 \text{ V}, V_D = 1.21 \text{ V} \quad I_{DS2} = 3.66 \text{ mA}$$

$$R_2 = 5.134 \text{ k}$$



## Problem 3

**Find**  $I_o$  and  $V_o$

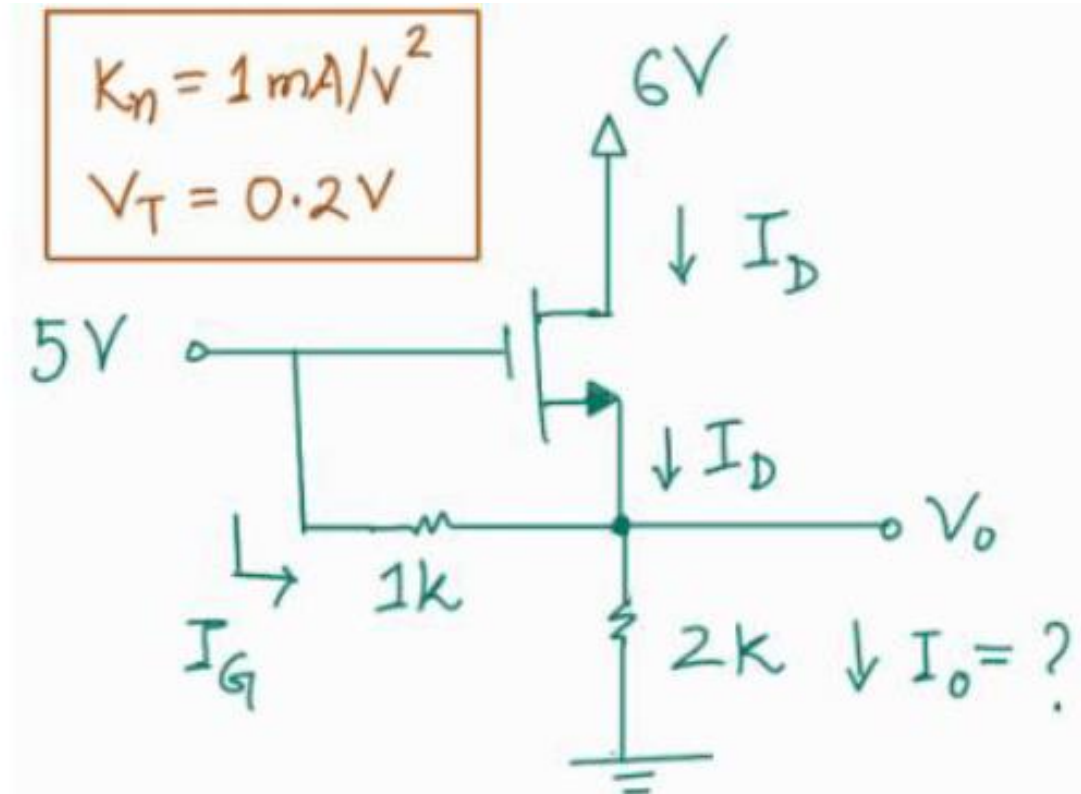
$$V_s = 3.72\text{V or } \cancel{8.87\text{V}}$$

$$V_{GS} = 1.26\text{V}$$

$$V_{ov} = 1.06\text{V}$$

$$V_{DS} = 2.28\text{V}$$

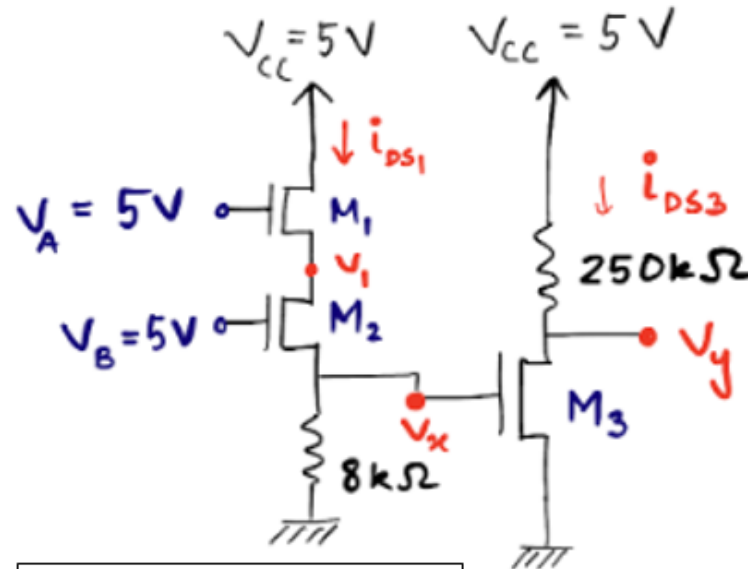
$$I_o = 1.86\text{mA}$$



## Problem 4

For the following circuit with MOSFETs, assume that  $V_T = 1V$ ,  $k_n' = 50 \mu A/V^2$  and the aspect ratio  $W/L$  is 1 for all the MOSFETS.

- a) If the gate voltage to  $M_3$  MOSFET,  $V_x = 0.938V$ , and MOSFET  $M_2$  is in triode mode, **find** the voltage  $V_1$ .
- b) **Find**  $V_y$ .
- c) If  $W/L=2$ , then  $V_1 = 2.1454 V$ . **Find**  $V_x$  for this case.



$$V_1 = 1.835V \text{ or } \cancel{6.16V}$$

$$V_{DS1} = 3.165V$$

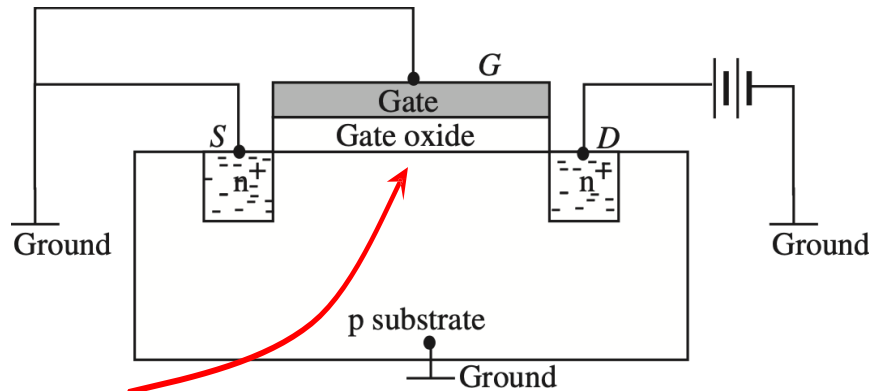
$$V_{GS1} = 3.165V$$

$$V_{ov} = 2.165V$$

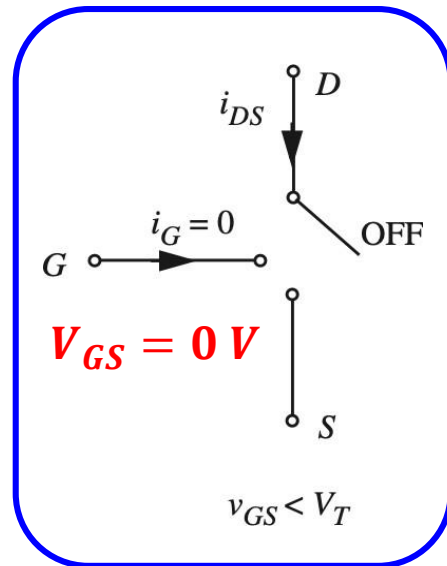
$$V_y = 5V$$

$$V_x = 1.377V$$

# n-channel MOSFET - Summary

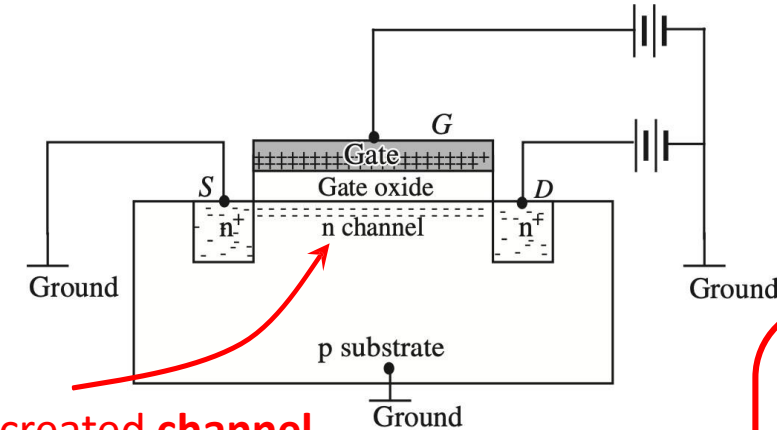


No channel, open ckt



Cut off mode

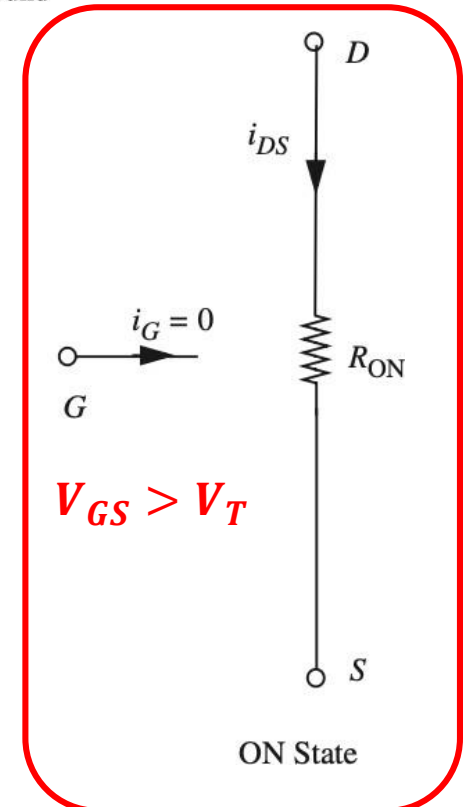
**G – Gate:**  
**S – Source:**  
**D – Drain:**



The created **channel**  
will have some  $R$   
-> SR model

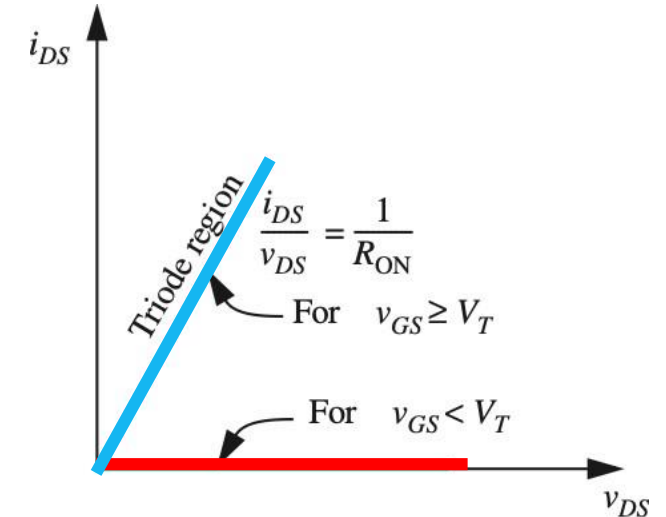
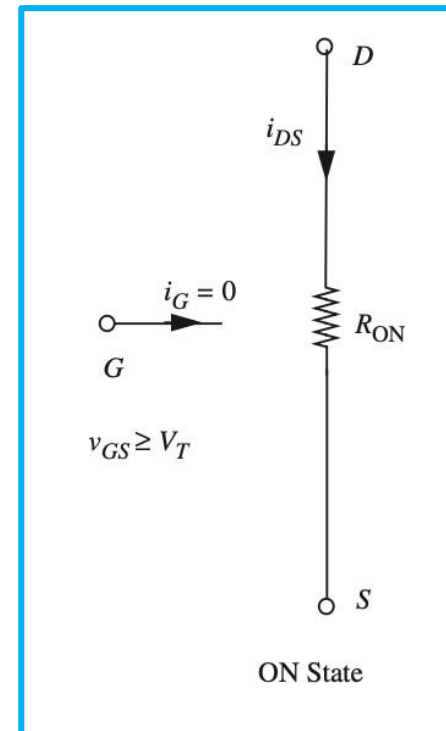
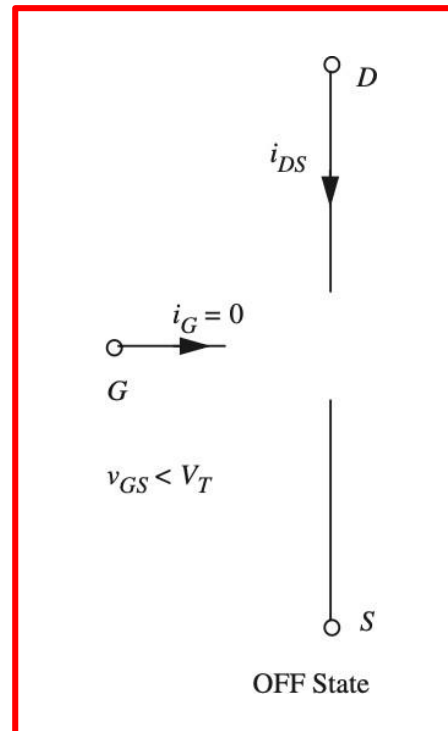
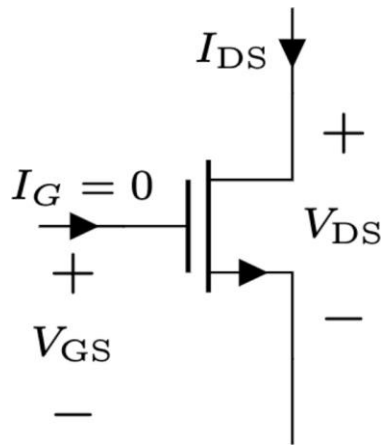
Trigger terminal  
Charge carrier reservoir  
Charge carrier sink

**Small  $v_{DS}$ :** Triode Mode  
**Large  $v_{DS}$ :** Saturation Mode



# n-channel MOSFET - Summary

## SR Model:

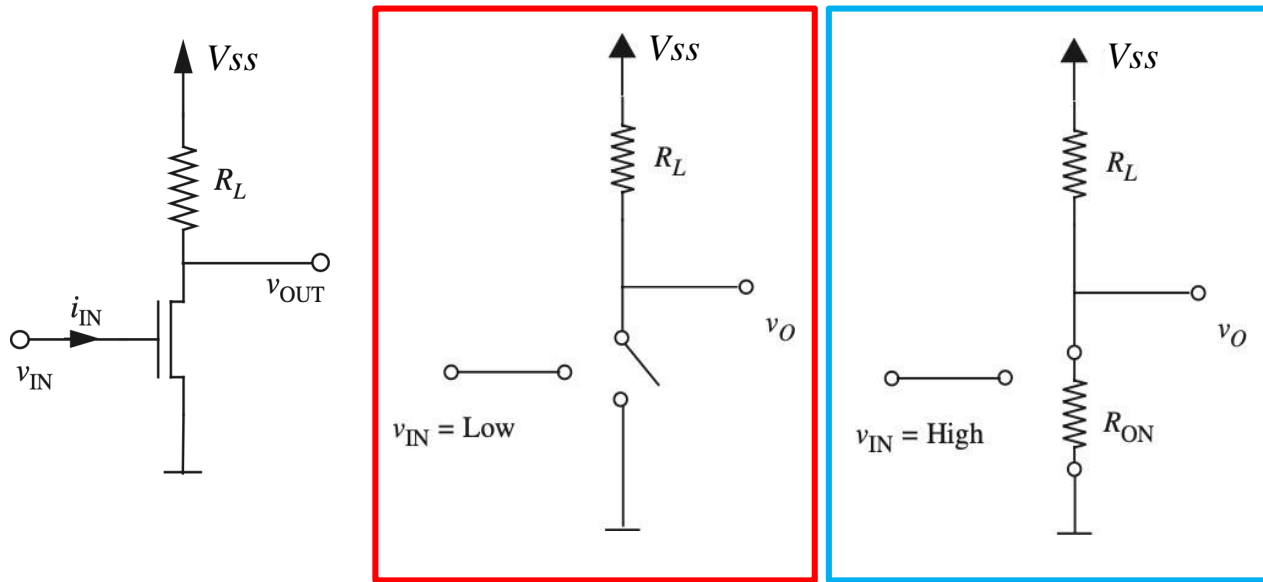


$$R_{ON} = \frac{1}{k_n(V_{OV})}$$

$V_{OV}$   
Indicates the available  
excess voltage at **gate** after  
forming the n-channel.

- SR model is a better approximation than S model.
- **Triode Mode exists until:**  $v_{DS} \leq (v_{GS} - V_T)$

# SR Model - Inverter



$$v_{o,HI} = V_{SS}$$

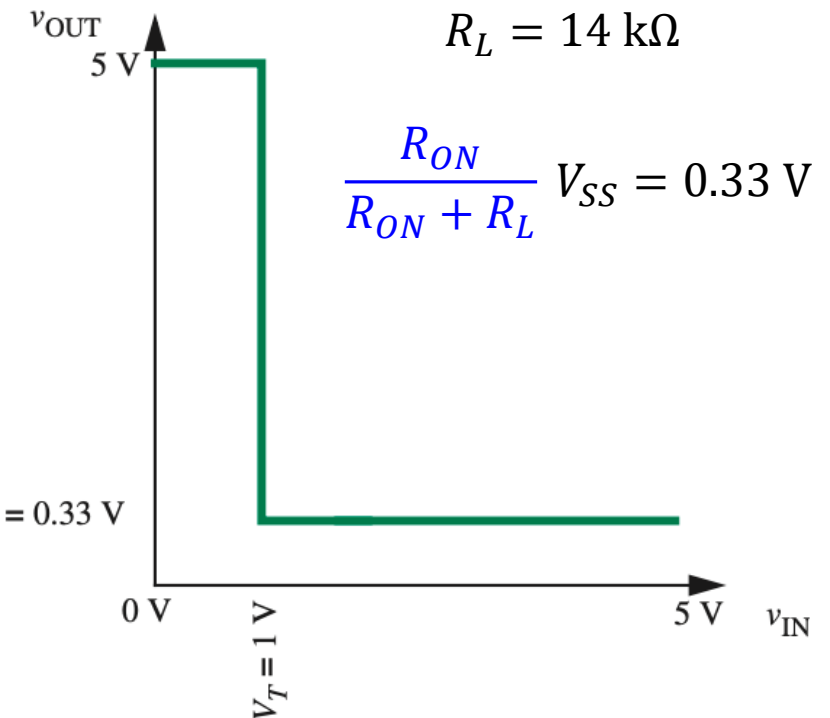
$$v_{o,LO} = \frac{R_{ON}}{R_{ON} + R_L} V_{SS}$$

For example, If

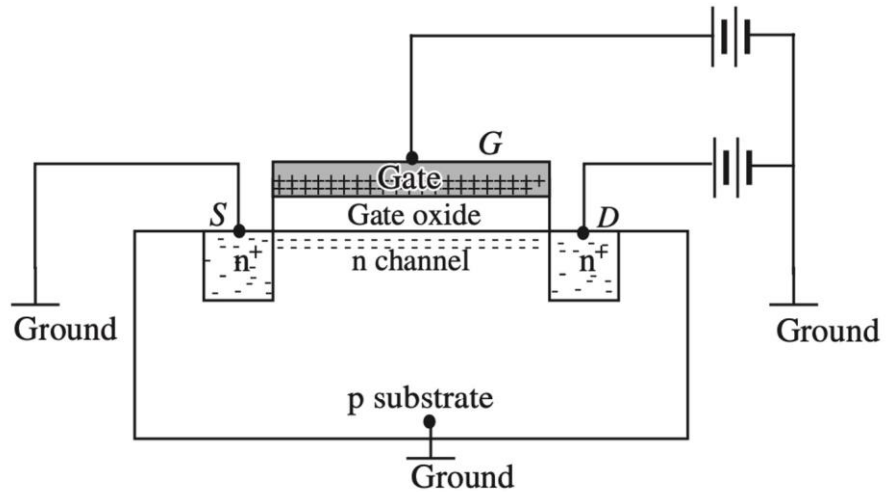
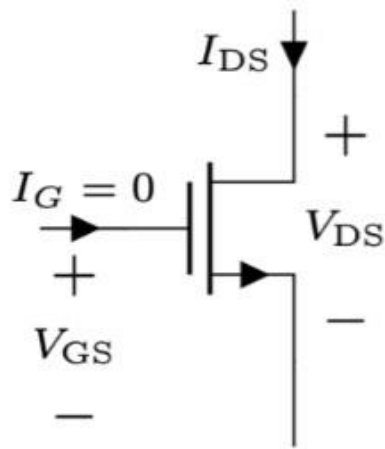
$$\begin{aligned} V_{SS} &= 5 \text{ V}, \\ R_{ON} &= 1 \text{ k}\Omega, \\ R_L &= 14 \text{ k}\Omega \end{aligned}$$

$$\frac{R_{ON}}{R_{ON} + R_L} V_{SS} = 0.33 \text{ V}$$

$$\frac{V_{SS} R_{ON}}{R_{ON} + R_L} = 0.33 \text{ V}$$



# Review – MOSFET



Control =  $V_{GS} = V_G - V_S$  controls the IV between drain-source ( $I_{DS}$  vs  $V_{DS}$ )

Threshold voltage =  $V_T$ , minimum voltage required to create the channel

## Models

1. **S Mode:** Assumes an ideal channel with zero resistance
2. **SR Model:** Assumes finite channel resistance,  $R_{ON}$ , depends on  $V_{GS} - V_T = V_{OV}$

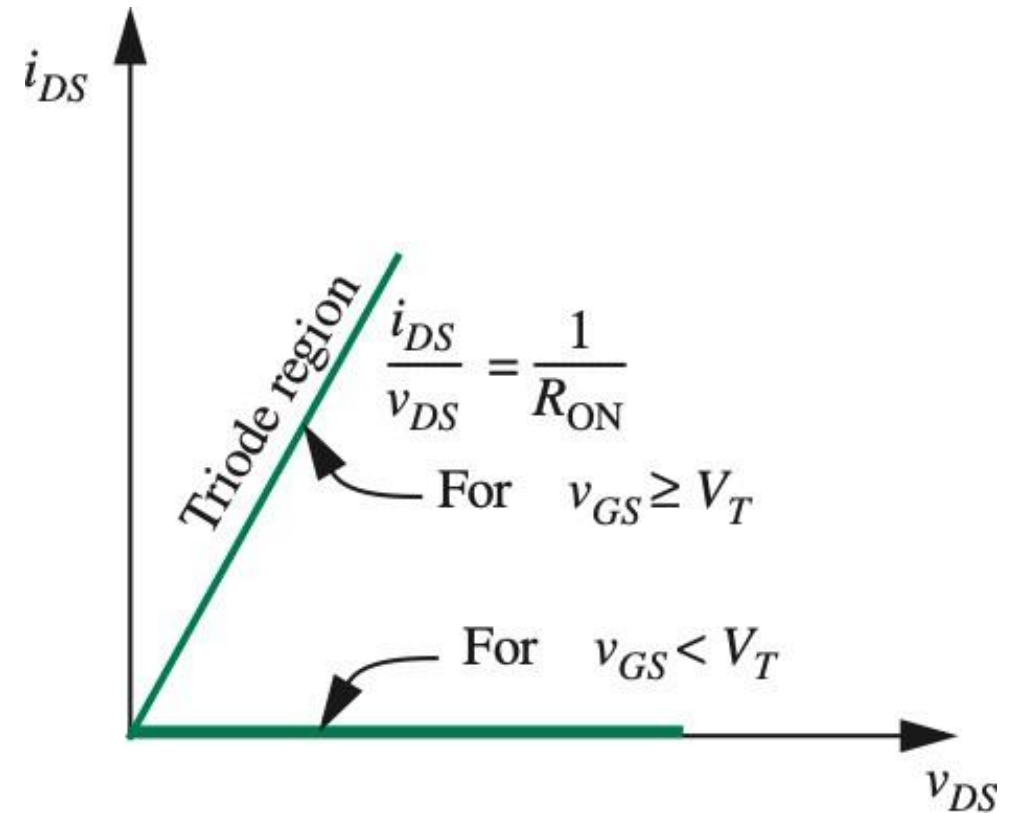
# NMOS Triode Mode

For small  $v_{DS}$

$$I_{DS} = k'_n \frac{W}{L} \left( v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS}$$

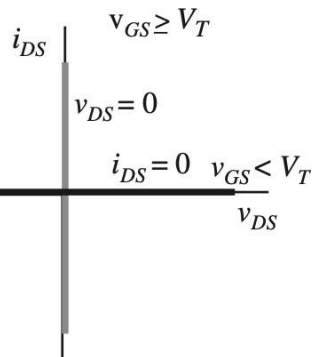
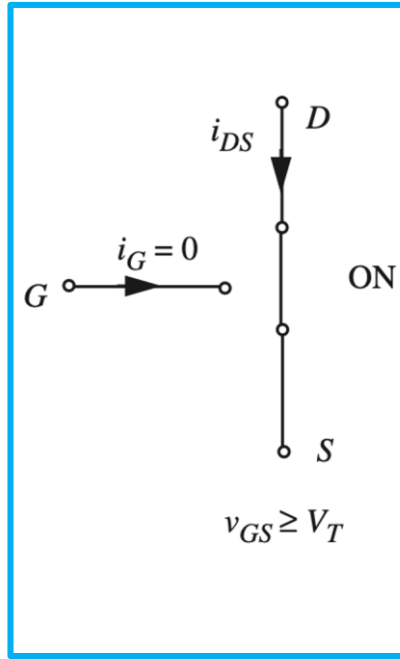
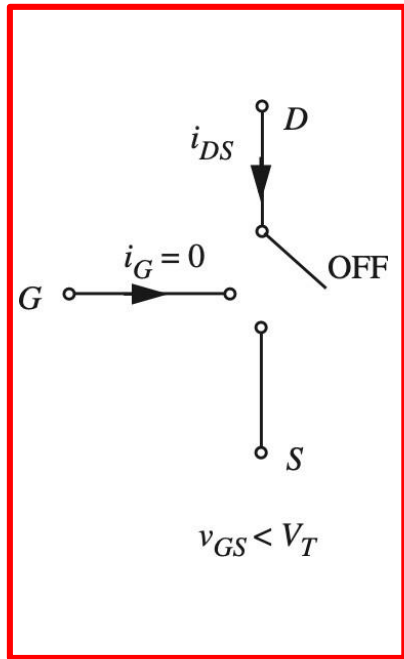
$$I_{DS} = \frac{1}{R_{ON}} v_{DS}$$

$$R_{ON} = \frac{1}{k'_n \frac{W}{L} (v_{GS} - V_T)}$$
$$= \frac{1}{k_n (V_{OV})}$$

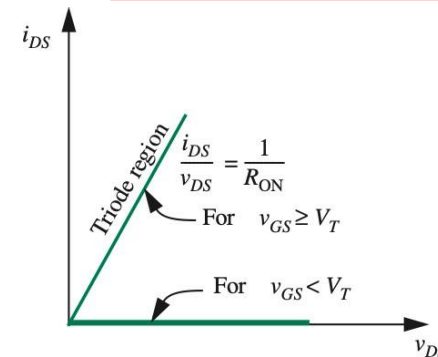
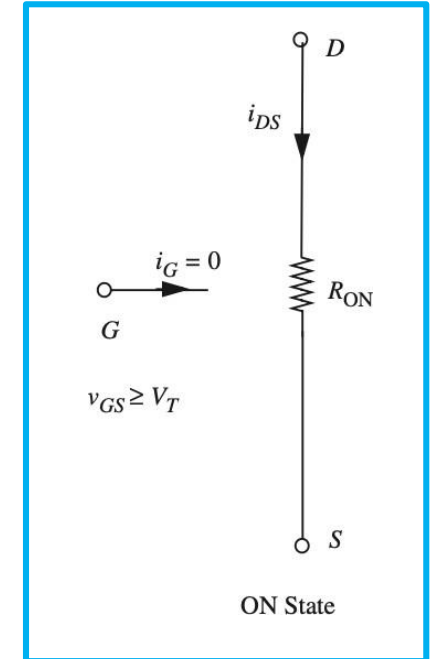
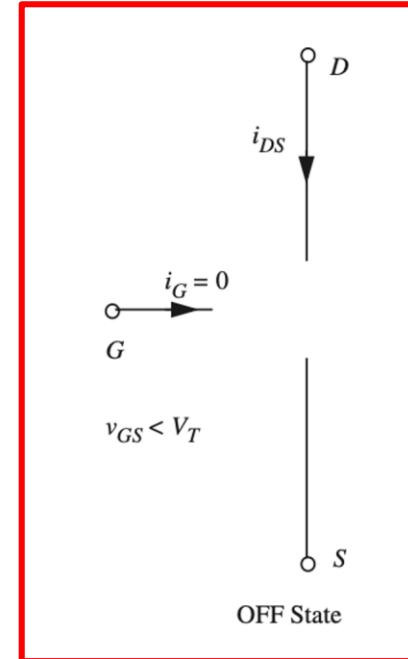


# MOSFET Linear Models

## S Model



## SR Model



$$R_{ON} = \frac{1}{k'_n \frac{W}{L} (v_{GS} - V_T)}$$