

## SPRING - 25

Analyze the circuit in Figure-1, and show that the MOSFET will operate in Saturation mode if it conducts current. [Hint: You don't need to solve the circuit]. Analyze the circuit and calculate  $V_O$ ,  $I_1$ ,  $I_2$  &  $I_D$  using the method of assumed states. You must validate your assumption.

$V_D > V_h$  so,  $V_D - V_S > V_{Gh} - V_S$  or, if MOSFET conducts current,

$$V_{GS} > V_T$$

$$\text{So, } V_{OV} = V_{GS} - V_T$$

So, we can write,

$$V_{GS} = V_{OV} + V_T$$

$$\text{or, } \underline{V_{GS} > V_{OV}} \quad (\because V_T \text{ is positive})$$

$$\text{or, } \underline{\underline{V_{DS} > V_{GS} > V_{OV}}} \quad \text{or, } V_{DS} > V_{OV} \text{ which is Saturation Mode.}$$

Applying KCL at  $V_S$  node.  $I_1 + I_D = I_2$

$$\text{Again, } \frac{V_h - V_S}{1} = I_1 \text{ or, } \boxed{5 - V_S = I_1} \quad \text{and} \quad I_2 = \frac{V_S - 0}{2} = \frac{V_S}{2}$$

$$I_D = \frac{k}{2} (V_{GS} - V_T)^2 \quad \text{or,} \quad I_1 - I_2 = \frac{1}{2} (I_1 - 1)^2$$

$$\text{or, } 5 - V_S - \frac{V_S}{2} = \frac{1}{2} (5 - V_S - 1)^2$$

$$\text{or, } V_S^2 - 11V_S + 26 = 0 \quad \text{or,} \quad V_S = 7.56, 3.43$$

If,  $V_S = 7.56$ , then  $V_{GS} = 5 - 7.56 = -2.56 < V_T(1V)$ , Cut-off.

If,  $V_S = 3.43$ , then  $V_{GS} = 5 - 3.43 = 1.57 > V_T(1V)$ , Saturation.

$$\text{So, } I_1 = 5 - V_S = \boxed{1.57 \text{ mA}}, \quad I_2 = \frac{V_S}{2} = \boxed{1.715 \text{ mA}}$$

$$I_D = I_2 - I_1 = \boxed{0.145 \text{ mA}}$$

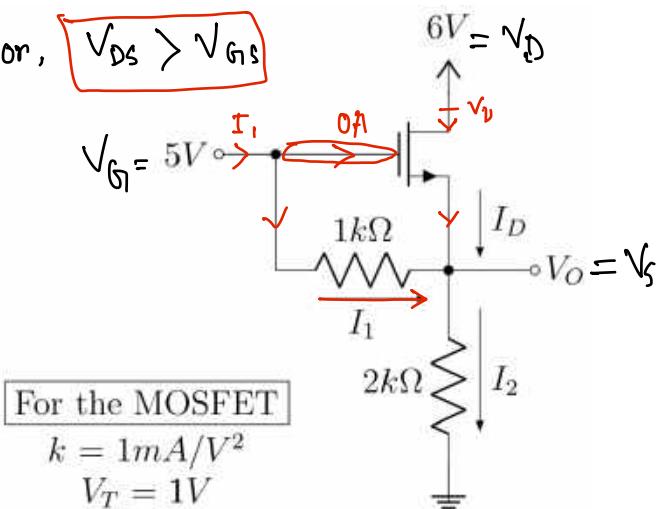
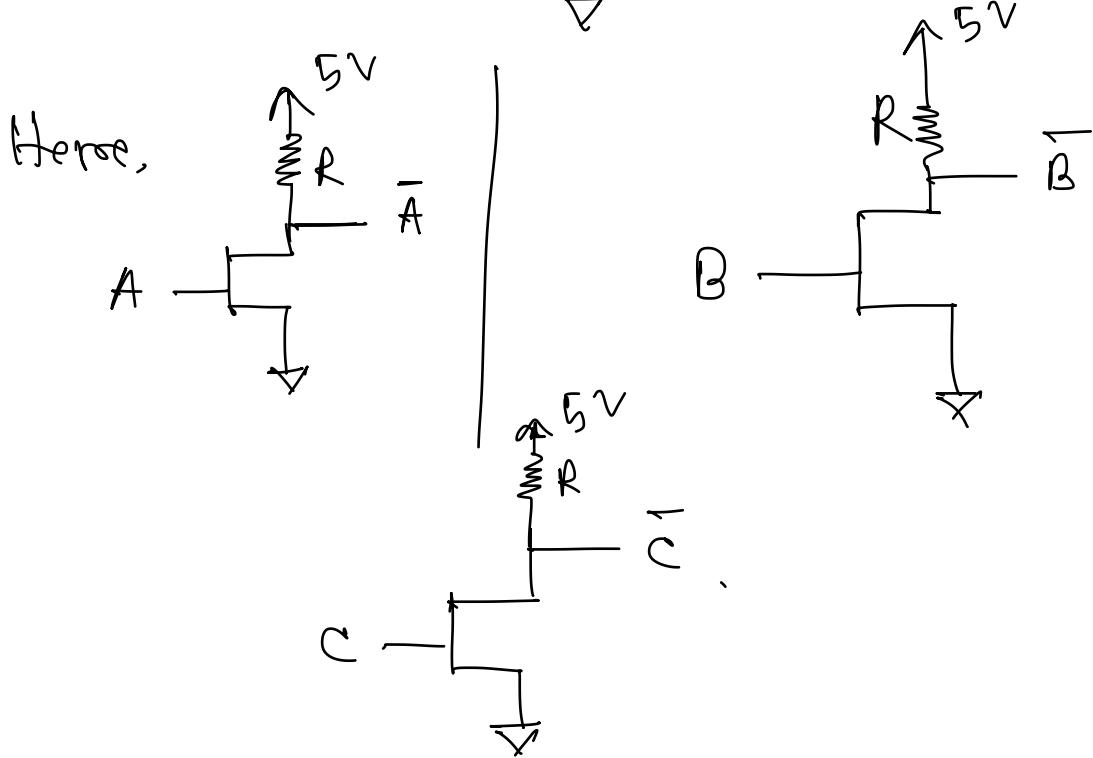
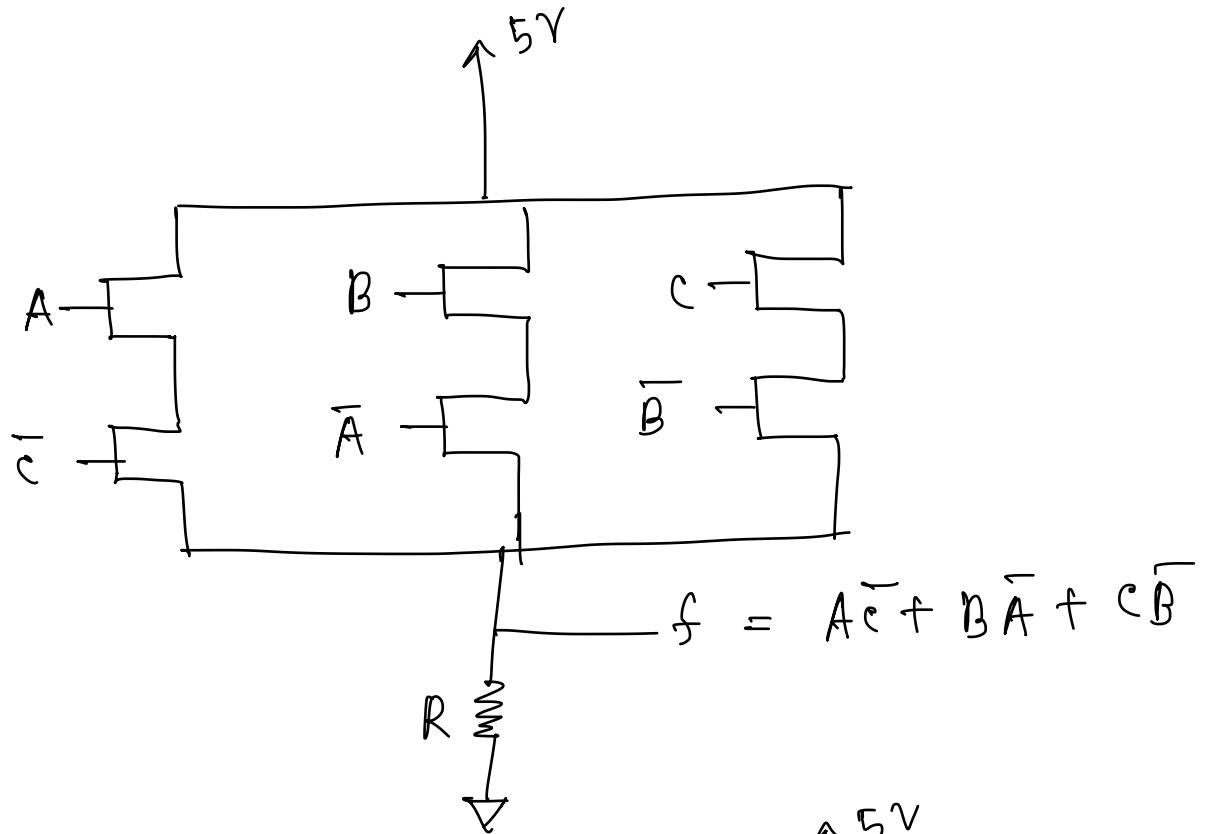


Figure-1

Design a circuit with boolean inputs A, B, and C using MOSFETs to implement the boolean logic function,

$$f = \overline{C} \cdot A + \overline{A} \cdot B + \overline{B} \cdot C$$



### FALL-24

Analyze the circuit and Show that, if the MOSFET, M2 conducts current, it will operate in the saturation mode. [Hint: You don't need to solve the circuit]. Calculate the values of  $V_{out}$ ,  $I_{RD1}$ , and  $I_{RD2}$  using the method of assuming states. You must validate your assumptions.

For  $M_2$ ,  $V_G = V_D$

if conducts current,

$$V_{GS} > V_T \text{ . So, } V_{GS} = V_{GS} - V_T$$

We can write,

$$V_{GS} = V_T + V_{OV}$$

or,  $V_{DS} = V_T + V_{OV}$

or,  $V_{DS} > V_{OV}$  [ $\because V_T$  positive]

proved Saturation Mode.

$$\text{Now, } I_D = \frac{k}{2} (V_{GS} - V_T)^2$$

$$\text{or, } I_D = \frac{2}{k} (V_G - V_S - 1)^2 \text{ or, } I_D = (12 - 6I_D - 4I_D - 1)^2 \quad [\because V_G = V_D]$$

$$\text{or, } 100I_D^2 - 221I_D + 121 = 0 \text{ or, } I_D = 1 \text{ mA, } 1.21 \text{ mA}$$

If  $I_D = 1 \text{ mA}$ ,  $V_{GS} = 12 - 6I_D - 4I_D = 2 \text{ v} > V_T (1 \text{ v})$  This is ok.

If  $I_D = 1.21 \text{ mA}$ ,  $V_{GS} = 12 - 10I_D = -0.1 < V_T (1 \text{ v})$ . Not ok.

So,  $I_{RD1} = 1 \text{ mA}$  and  $V_G$  for  $M_2 = 12 - 6I_D = 6 \text{ V}$

For  $M_1$ ,  $V_G = 6 \text{ V}$ ,  $V_S = 0$ ,  $V_{GS} = 6 \text{ V}$ ,  $V_{OV} = V_{GS} - V_T = 5 \text{ v}$  and  $V_{out} = V_D = 5 - I_D$

Assuming Saturation,  $I_D = \frac{k}{2} (V_{OV})^2 = \frac{0.5}{2} (5)^2 = 6.25 \text{ mA}$

So,  $V_D = 5 - I_D = -1.25 \text{ V}$

But,  $V_{DS} = -1.25 - 0 = -1.25 < V_{OV} (5 \text{ v})$  So, Not Saturation assumption wrong.

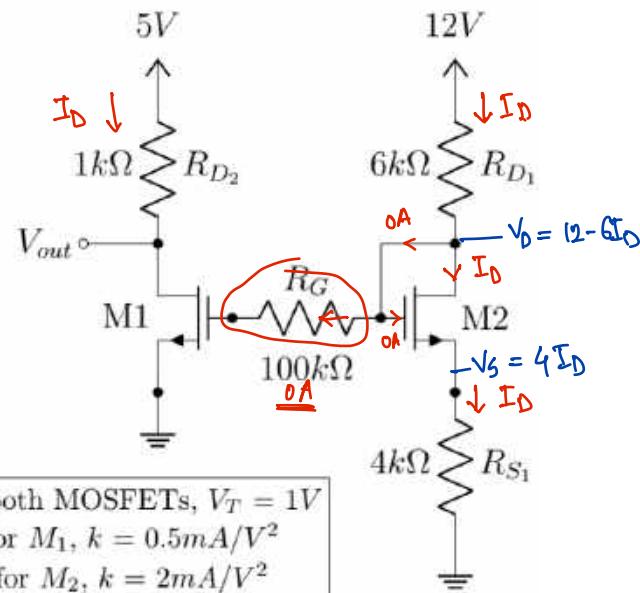
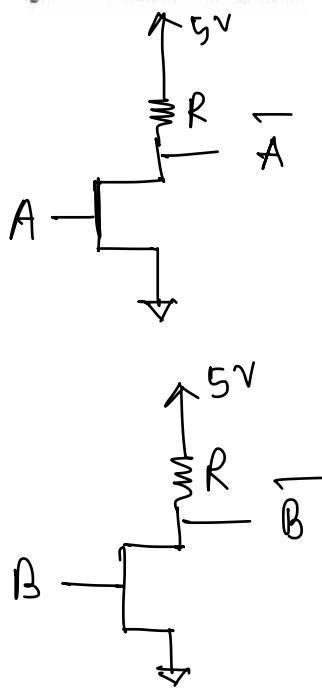


Figure-2

Design the circuits with the boolean inputs A, B, C to implement the following boolean logic Functions:

$$f = \overline{A} \cdot \overline{B} + A \cdot B$$



Assuming Saturation,

$$I_D = k \left( V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS} \quad | \quad V_{DS} = V_D = 5 - I_D$$

$$\text{or, } I_D = 0.5 \left( 6 - 1 - \frac{5 - I_D}{2} \right) (5 - I_D)$$

$$\text{or, } I_D^2 + 4I_D - 25 = 0 \quad \text{or, } I_D = -7.38 \text{ mA} \\ = 3.38 \text{ mA}$$

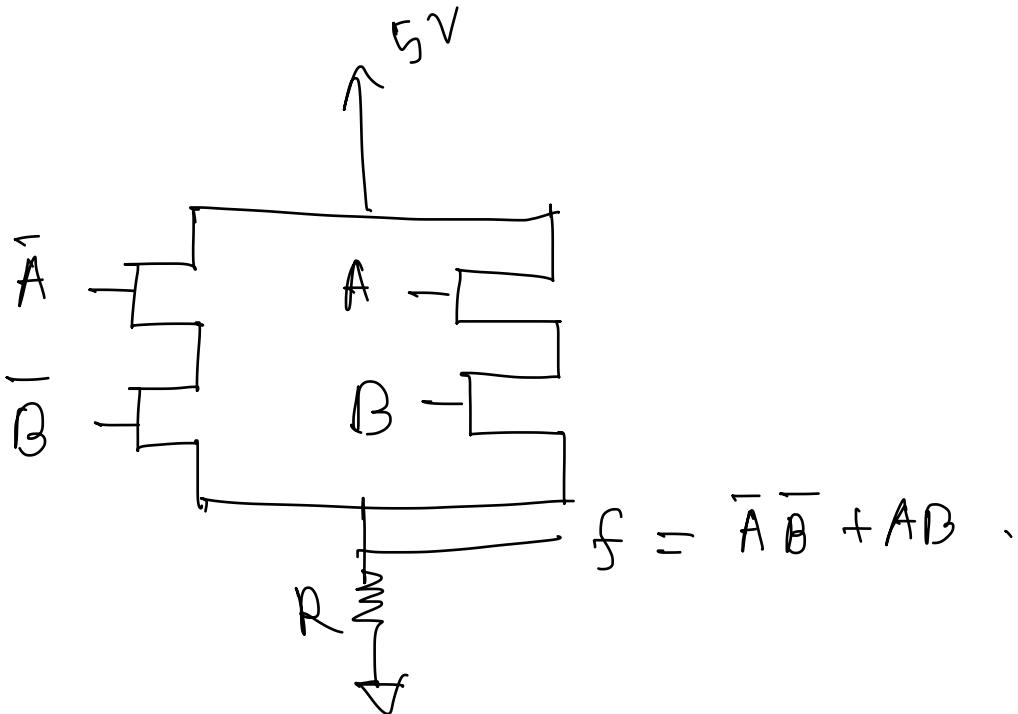
In Triode  $I_D$  cannot be negative.

$$\text{So, } I_D = \boxed{3.38 \text{ mA}} = I_{RD2}$$

$$\text{So, } V_{DS} = 5 - 3.38 = 1.62 \text{ V or } (5 \text{ V})$$

Proved Triod mode.

$$\text{So, } V_{out} = V_D = \boxed{1.62 \text{ V}}.$$

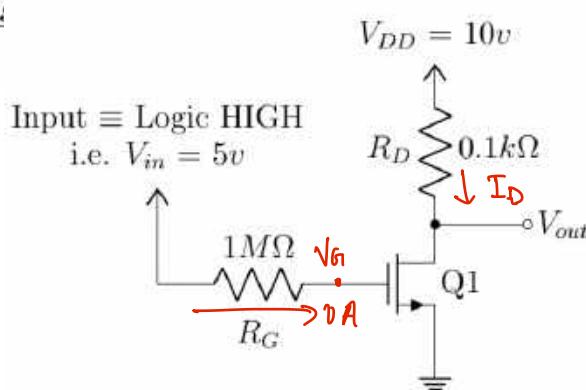


## SUMMER-24

Joy and Nirmol were designing an inverter circuit with MOSFET for their project. Joy designed the following circuit. However, Nirmol said that the designed inverter circuit would malfunction. When they tested the circuit, it malfunctioned. For logic HIGH input, the output was also logic HIGH instead of logic LOW. Nirmol modified the value of  $R_D$  to a larger value, and eventually it fixed the issue.

### MOSFET Parameter:

$$V_T = 1v, K = 4mA/v^2$$



| For Input      |               |
|----------------|---------------|
| Voltage Level  | Logic Level   |
| $V_{in} = 0v$  | LOW i.e. '0'  |
| $V_{in} = 5v$  | HIGH i.e. '1' |
| For Output     |               |
| Voltage Level  | Logic Level   |
| $V_{out} > 5v$ | HIGH i.e. '1' |
| $V_{out} < 5v$ | LOW i.e. '0'  |

State the conditions to verify the assumptions regarding the Saturation Mode of a MOSFET.

$$V_{GS} > V_T \text{ must, } V_{DS} = V_{GS} - V_T$$

then,  $V_{DS} \geq V_{DS}$  must satisfy.

Analyze the circuit shown above and calculate the value of  $V_{out}$  using the method of assumed states. You must validate your assumption. Determine whether Nirmol was correct or not.

Here,  $V_{in} = 5v = V_G$ ,  $V_S = 0v$ ,  $V_{GS} = 5v$ ,  $V_{DS} = V_{GS} - V_T = 4v$

Assuming Saturation,  $I_D = \frac{k}{2} (V_{DS})^2 = \frac{4}{2} (4)^2 = 32mA$

So,  $V_{out} = V_D = 10 - 0.1I_D = 10 - 3.2 = 6.8v$  | and  $V_{DS} = 6.8 > V_{DS}$  (4v)  
proved Saturation

For input  $V_{in} = 5v$  = logic high

for output,  $V_{out} = 6.8 > 5v$  = logic high.

For an inverter, For high input logic, output should be low output logic.

But we got high output logic.

So, inverter is malfunctioning, Nirmol was right.

Nirmol changed the value of  $R_D$  to  $1\text{k}\Omega$ . Now, Analyze the modified circuit and calculate  $V_{out}$ . Determine whether the inverter was working properly after the modification.

We have  $V_{GS} = 5\text{V}$ ,  $V_{DS} = 5\text{V}$ ,  $V_{ov} = 4\text{V}$

Now,  $R = 1\text{k}\Omega$  . So,  $V_D = 10 - I_D$

Assuming  $T_{model}$ ,  $I_D = k \left( V_{ov} - \frac{1}{2} V_{DS} \right) V_{DS}$

$$\text{or, } I_D = 4 \left[ 4 - \frac{1}{2} (10 - I_D) \right] (10 - I_D)$$

$$\text{or, } 4I_D^2 - 46I_D + 80 = 0$$

$$\text{or, } I_D = 2.136\text{mA}, 9.364\text{mA}$$

if  $I_D = 2.136\text{mA}$

$$V_{DS} = V_D = 10 - I_D = 7.864\text{V} > V_{ov} (4\text{V})$$

**Not  $T_{model}$  X**

If,  $I_D = 9.364\text{mA}$ ,  $V_{DS} = 0.636\text{V}$

Hence,  $V_{DS} < V_{ov} (4\text{V})$ ,  $T_{model}$  Proved.

Also,  $V_{out} = 0.636 < 5\text{V}$  which is low logic output.

Inverters is working properly.

Design the inverter circuit by choosing a suitable value of  $R_D$  such that the MOSFET operates at the edge of saturation. [Hint: At the edge of saturation,  $V_{DS} = V_{ov}$ ]

We got,  $V_{GS} = 5\text{V}$ ,  $V_{ov} = 4\text{V}$

We need  $V_{DS} = V_{ov} = 4\text{V}$

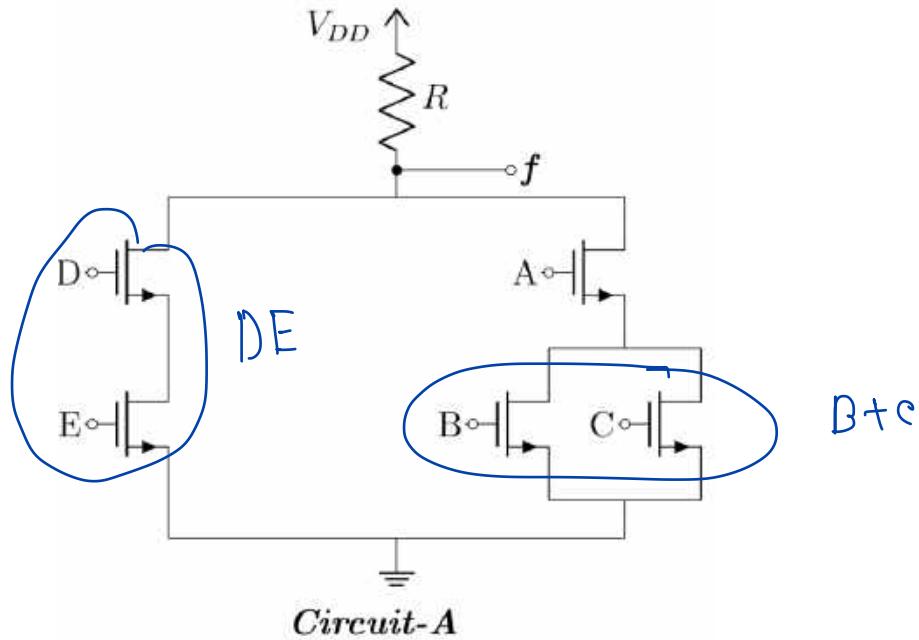
Since,  $V_S = 0$ , So,  $V_D = 4\text{V}$

The mode is Saturation,

$$\text{So, } I_D = \frac{k}{2} (V_{ov})^{\frac{1}{2}} = \frac{4}{2} (4)^{\frac{1}{2}} = 32\text{mA}$$

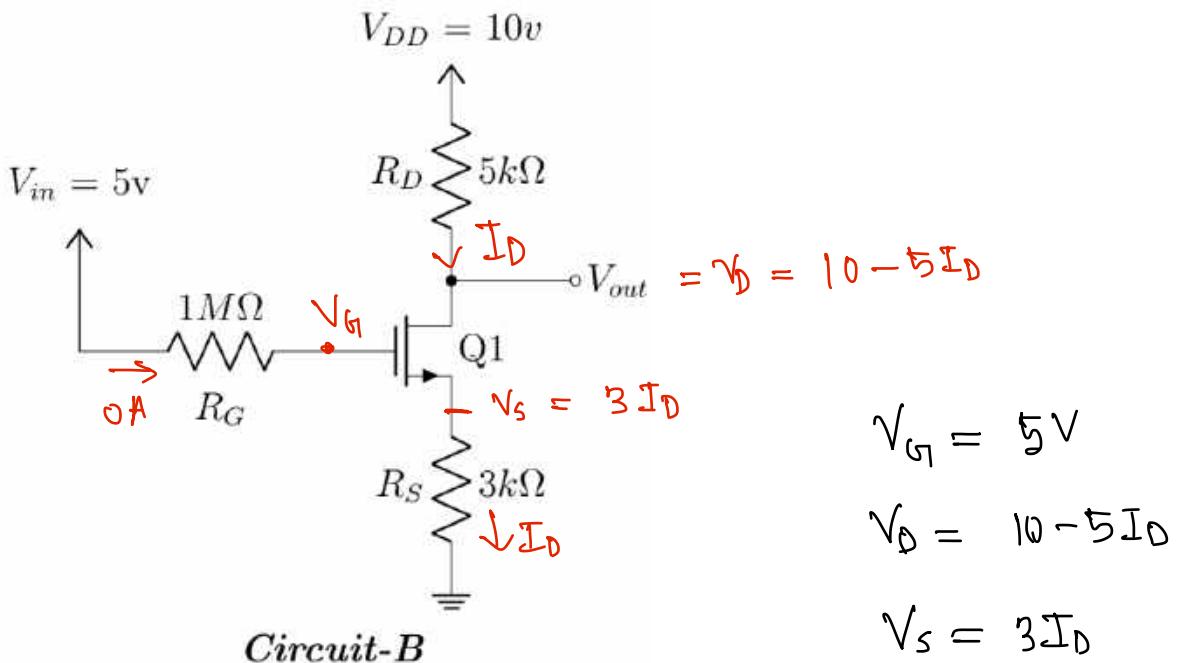
$$\text{So, } R_D = \frac{10 - V_D}{I_D} = \frac{10 - 4}{32} = \boxed{0.1875\text{k}\Omega}$$

Determine the logic function, f in 'Circuit-A' for the boolean inputs A, B, C , D and E.



$$\text{So, } f = \overline{DE} + A(B+C)$$

Analyze 'Circuit-B' and calculate  $I_{DS}$  and  $V_{out}$  using the method of assumed states. You must validate your assumptions. Here,  $V_T = 1V$  and  $k = 2mA/v2$ .



Assuming Saturation,

$$I_D = \frac{k}{2} (V_{GS} - V_T)^0.5 = \frac{2}{2} (5 - 3I_D - 1)^0.5$$

$$\text{or, } 9I_D^2 - 25I_D + 16 = 0 \quad \text{or, } I_D = 1mA, 1.77mA$$

For  $I_D = 1mA$

$$\begin{aligned} V_{GS} &= 5 - 3I_D = 2V \\ V_{ov} &= V_{GS} - V_T = 1V \\ V_{DS} &= 10 - 5I_D - 3I_D \\ &= 2V > V_{ov} (1V) \end{aligned}$$

proved Saturation.

For  $I_D = 1.77mA$

$$V_{GS} = 5 - 3I_D = -0.31V < V_T (1V)$$

This time cut-off.

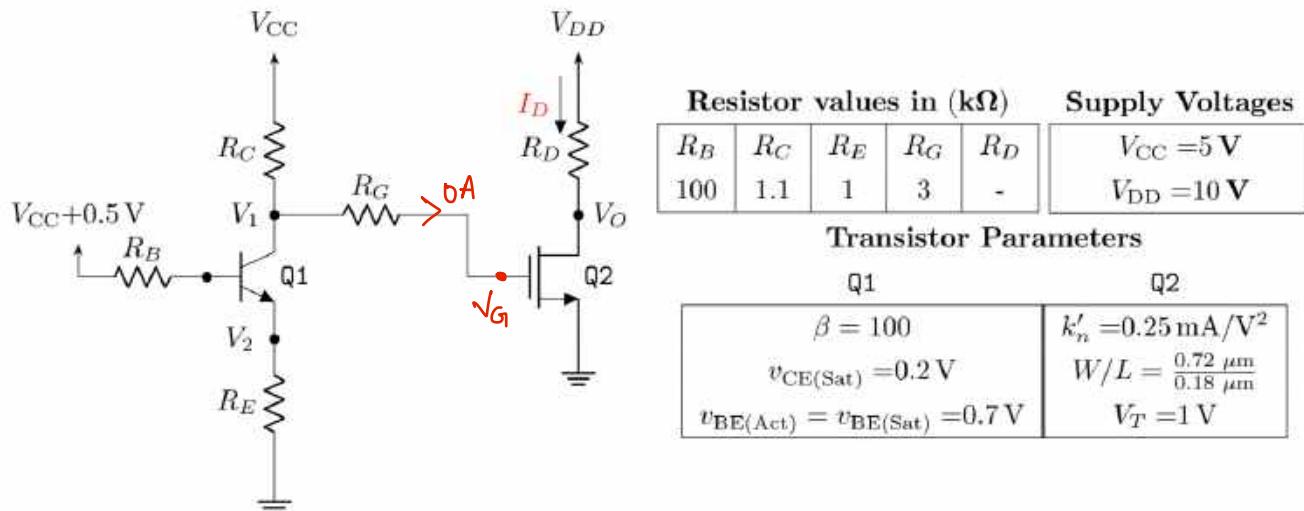
So, Not acceptable.

$$\text{So, } I_{DS} = \boxed{1mA}$$

$$V_{out} = V_D = 10 - 5I_D = \boxed{5V}$$

## SPRING-24

Design the circuit, i.e. find an appropriate value of  $R_D$ , such that  $Q_2$  remains at the edge of saturation, i.e., when  $V_{DS} = V_{GS} - V_T$ .



No current flow through  $R_G$ . So,  $V_1 (\text{BJT}) = V_G (\text{MOSFET})$

So,  $R_G$  can be omitted from whole solution. BJT will be solved separately, and find  $V_1 = V_C$  for BJT. Then use  $V_1 = V_G$  in MOSFET and solve it.

From the BJT solution sheet, see SPRING-24, same math  $V_1 = 2.5V$

So, for MOSFET,  $V_G = 2.5V$ ,  $V_S = 0V$ ,  $V_{GS} = 2.5V$

$$V_{OV} = V_{GS} - V_T = 1.5V$$

We are said at the edge of saturation

$$\text{So, } V_{DS} = V_{OV} = 1.5V$$

$$\text{or, } V_D = 1.5V$$

In Saturation,

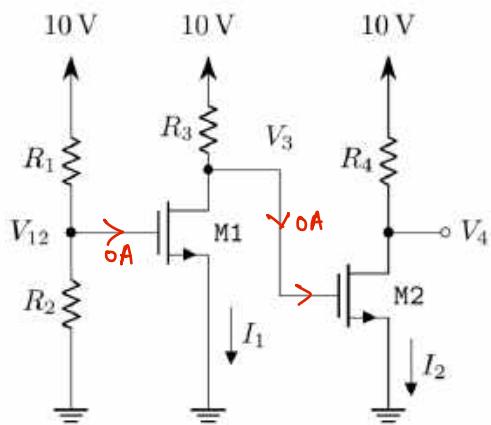
$$\begin{aligned} I_D &= \frac{k}{2} (V_{OV})^2 = \frac{1}{2} k_n' \left( \frac{W}{L} \right) (V_{OV})^2 \\ &= \frac{1}{2} \times 0.25 \times 4 \times (1.5)^2 = 1.125 \text{ mA} \end{aligned}$$

$$\text{So, } R_D = \frac{V_{DD} - V_D}{I_D} = \frac{10 - 1.5}{1.125} = \boxed{7.556 \text{ k}\Omega}$$

Relevant information for the circuit configuration on the right is given in the tables below:

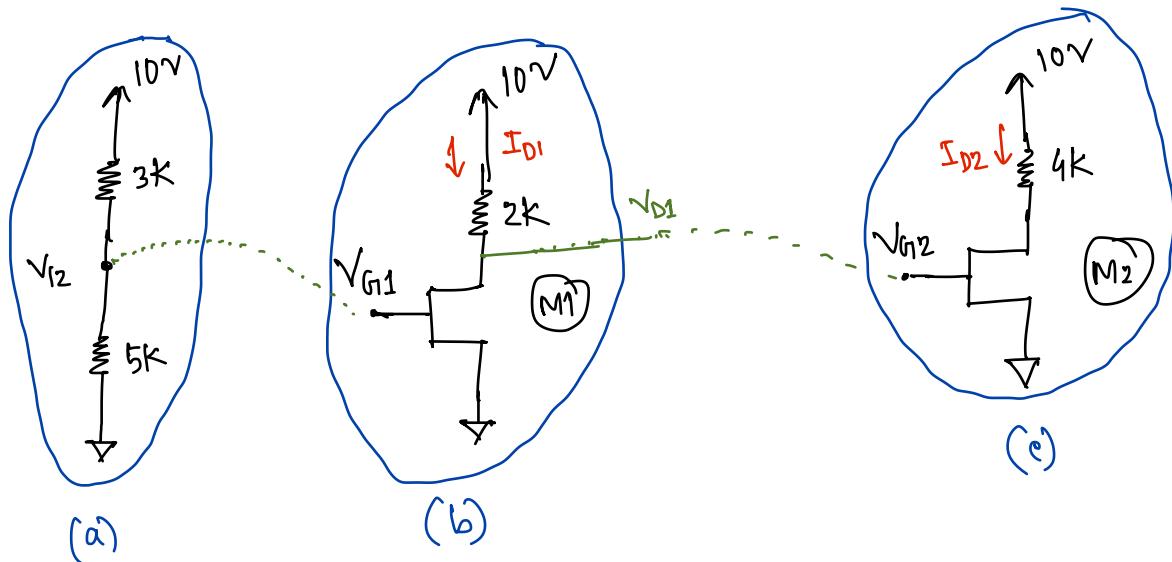
| Resistor values<br>in ( $k\Omega$ ) |       |       |       |
|-------------------------------------|-------|-------|-------|
| $R_1$                               | $R_2$ | $R_3$ | $R_4$ |
| 3                                   | 5     | 2     | 4     |

| Transistor<br>Parameters |  |
|--------------------------|--|
| $k_n = 2 \text{ mA/V}^2$ |  |
| $V_T = 1 \text{ V}$      |  |



Determine the value of  $V_{12}$ . Calculate the value of drain-to-source voltage of the transistor  $M_1$ . In the process, determine the operating mode of  $M_1$ . Determine which one of the four resistors will consume the least amount of power. [Hint, Power =  $I^2R$ ]. Determine how the operating mode of  $M_2$  would change if  $R_2$  were set to zero.

No current flow through the connection points, because they are with gate terminals. So, whole circuit = 3 separate parts.



So, basically we need to solve (a), (b), (c) separately

and use  $V_{12} = V_{G1}$  and  $V_{D1} = V_{A2}$ .

$$\text{From, circuit (a), } \frac{10 - V_{12}}{3} = \frac{V_{12} - 0}{5} \text{ or, } V_{12} = 6.25 \text{ V}$$

$$\text{So, } V_{G1} = 6.25 \text{ V}$$

$$\text{For } M_1, \quad V_{G1} = 6.25 \text{ V}, \quad V_{Dr} = V_{GS} - V_T = 5.25 \text{ V}$$

$$V_{DS} = V_{D1} - V_s = V_{D1} - 0 = V_{D1} = 10 - 2I_{D1}$$

Assuming Triode Mode,

$$I_{D1} = k \left( V_{DS} - \frac{1}{2} V_{DS} \right) V_{DS}$$

$$\text{or, } I_{D1} = 2 \left[ 5.25 - \frac{1}{2} (10 - 2I_{D1}) \right] (10 - 2I_{D1})$$

$$\text{or, } 8I_{D1}^2 - 36I_{D1} - 10 = 0$$

$$\text{or, } I_{D1} = \frac{-0.262 \text{ mA}}{\cancel{x}}, \frac{4.76 \text{ mA}}{\cancel{w}}$$

So,  $V_{DS}$  for M1,

$$V_D - V_S = V_{D1} = 10 - 2I_{D1} \\ = 0.48V < V_{DS} (5.25V)$$

So, Triode proved.

$$V_{DS} = 0.48V$$

Similarly for circuit (c)

$$V_{G2} = V_{D1} = 0.48V$$

$$\text{For M2, } V_{GS} = V_{G2} - V_S = V_{G2} - 0 = 0.48 < V_T (1V)$$

It is already in cut-off mode.

So, No current flow,  $I_{D2} = 0A$  and  $V_4 = 10V$

Now power calculation,

$$P(R1) = I^2 R1 = \left( \frac{10 - V_{G2}}{3k} \right)^2 \times 3k = 4.687 \text{ mW}$$

$$P(R2) = I^2 R2 = \left( \frac{V_{G2} - 0}{5k} \right)^2 \times 5k = 7.812 \text{ mW}$$

$$P(R3) = I_{D1}^2 R_3 = (4.76)^2 \times 2 = 45.315 \text{ mW}$$

$$P(R4) = I_{D2}^2 R_4 = (0)^2 \times 4 = 0 \text{ W.}$$

So,  $R_4$  consumes the least power.

Repeat the whole math from start with,  $R_2 = 0$ .  
and find operating mode of M2 by yourself.

### SUMMER-23

Answer the following questions for Figure-1 where  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 2\text{k}\Omega$ ,  $R_3 = 3\text{k}\Omega$ ,  $R_4 = 4\text{k}\Omega$ . Determine the values of  $I_C$ ,  $I_B$ ,  $I_E$ ,  $V_C$  of T1. Analyze the circuit in Figure-1 to determine the value of  $I_{DS2}$ ,  $V_O$  of T2.

Lower Part of BJT is connected to gate of  $T_3$ .

$$\text{So, } I_E = 0\text{A}$$

$$\therefore I_E = I_B + I_C = 0\text{A}$$

$$I_B = I_C = 0\text{A}$$

BJT in cut-off mode.

$$\text{KCL at } V_C, \quad I_{R1} = I_C = 0$$

$$\text{So, } V_C = 10 - R_1 \times 0 = 10\text{V}$$

For,  $T_2$ ,  $V_G = 10\text{V}$  [No current through

$$V_{GS} = 10\text{V}$$
 gate, just voltage transfer]

$$V_{OV} = V_{GS} - V_T \\ = 10 - 1 = 9\text{V}$$

$$V_O = V_D = 10 - R_3 I_{R3} = 10 - 3 I_{R3}$$

Here, basically  $I_{R3} = I_{DS2} = I_D$ .

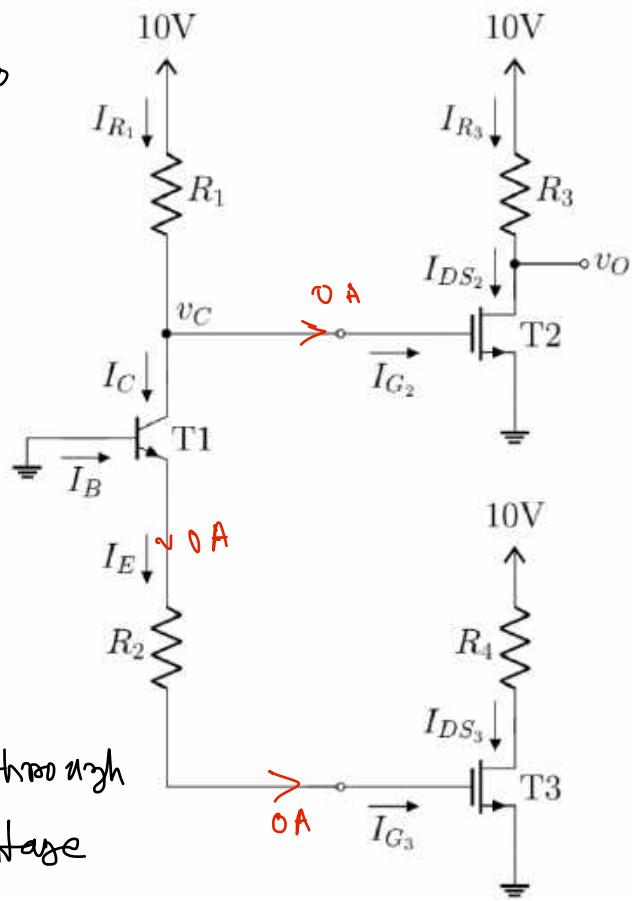
Assuming triode,

$$I_D = k \left( V_{OV} - \frac{1}{2} V_{DS} \right) V_{DS}$$

$$\text{or, } I_D = 1 \left[ 9 - \frac{1}{2} (10 - 3 I_D) \right] (10 - 3 I_D)$$

$$\text{or, } 9 I_D^2 - 4 I_D - 80 = 0$$

$$\text{or, } I_D = -2.767 \text{ mA} \\ = 3.211 \text{ mA}$$



We take  $I_D = 3.211 \text{ mA}$  [cannot be negative]

$$V_O = V_D = 10 - 3 I_D = 0.367 \text{V}$$

$$V_{DS} = 0.367 < V_T (\text{in})$$

proved Triode Mode.