Microprocessors

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Contents

- Data read / write operations from / to EEPROM data memory

EEPROM Data Memory Specs

- PIC16F628A has writeable and readable 128-byte EEPROM data memory.
- This memory area is used to store data that will not be deleted even if the power is cut off.
- There are special purpose registers to Access EEPROM data memory:
  - EECON1
  - EECON2
  - EEDATA
  - EEADR

Special Purpose Registers

- EEDATA: It is used to keep 8-bit data that used to in read or write operations.
- EEADR: It stores the EEPROM address to be accessed.
- EECON1 and EECON2: They are used select bits on read or write operations.

EEPROM Data Memory

- Only byte type of data can be written or read.
- It is required to clear data at the specified address firstly to write 1 byte of data.
- Writing and reading operations to the EEPROM data memory occur at high speeds.
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EEADR Register

- EEADR can address up to 256 byte EEPROM data memory.
- In PIC16F628A, only first 128 byte of address memory can be used. Therefore, 7.bit of this register always be 0.

EECON1 and EECON2 Registers

- It is a control register.
- First 3 bits are read as 0.
- RD and WR control bits starts the read write operation. They cant be cleared. They can setted only. When read write operations complete, they are cleared automatically by hardware.

Register 7-1: EECON1 Register

U-0	U-0	U-0	R/W-1	R/W-1	R/W-x	R/S-0	R/S-x
—	—	—	EEIF (1)	WRERR	WREN	WR	RD
bit 7							bit 0

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF**: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR**: EEPROM Error Flag bit
1 = A write operation is prematurely terminated
(any $\overline{\text{MCLR}}$ reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 **WREN**: EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR**: Write Control bit
1 = initiates a write cycle. The bit is cleared by hardware once write is complete.
The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 **RD**: Read Control bit
1 = Initiates an EEPROM read. Read takes one cycle. RD is cleared in hardware.
The RD bit can only be set (not cleared) in software.
0 = Does not initiate an EEPROM read

Legend		
R = Readable bit	W = Writable bit	S = Settable bit
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Note 1: Future devices will have this bit in the PIR register.

EECON1 and EECON2 Registers

- WREN bit allows write operation if it is 1. When PIC is powered on, the value of this bit is 0.
- When the writing operation is completed the EEIF bit (7.bit) of PIR1 register will be 1. It is needed to clear by program again.

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Read data from EEPROM

- Programmer is need to write the address value to EEADR register and set the RD bit of EECON1 register to read data from EEPROM Data Memory. Then data can be read by using EEDATA register.

```
BSF STATUS, RP0          ; Bank1
MOVLW ADDRESS            ; Load the address to be read.
MOVWF EEADR              ; EEADR<-W
BSF EECON1, RD           ; Read from EEPROM
MOVF EEDATA, W           ; W<-EEDATA
BCF STATUS, RP0          ; BANK0
```

Write data to EEPROM

- It is needed to write the address value to EEADR register and data to EEDATA register for writing data to EEPROM data memory. Then special codes are needed to write data.

BSF STATUS, RP0; Bank1

BCF INTCON, GIE; Ignore interrupts

BSF EECON1, WREN; Activate writing operation

MOVLW h’55’

MOVWF EECON2

MOVLW h’AA’

MOVWF EECON2

BSF EECON1, WR ; Start the writing operation

BSF INTCON, GIE

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte

Verification of Writing Operation

- Assume that we wrote some value to EEPROM.
- After the BSF EECON1, RD instruction, the EEDATA register gets updated with the data read from EEPROM memory.
- We can check the subtraction result to verify whether the writing operation is successfull or not.

```
MOVF some_value, W      ; W = value to write
MOVWF EEDATA            ; Put value in EEDATA
MOVWF temp              ; Save value to temp
; EEPROM write sequence here...
; Now verify the write:
BSF STATUS, RP0
BSF EECON1, RD          ; Start EEPROM read
BCF STATUS, RP0
SUBWF EEDATA, W         ; W = temp - EEDATA (if W was loaded with temp)
BTFSS STATUS, Z
GOTO WRITE_ERR
```

Example Prog

- When RA0 is pressed h’8F’ data will be written to h’05’ address of EEPROM.
- When RA1 is pressed h’3D’ data will be written to h’05’ address of EEPROM.
- When RA2 is pressed data will be read from h’05’ address of EEPROM and shown on PORTB