3.1 About this chapter

This chapter describes in detail the following subsystems of the MLCi/MLCi2:

- Control
- Optical
- Mechanical
- Electrical.

For systems diagrams relating to the MLCi/MLCi2 and the digital accelerator, refer to **[Ref: 14]**.

3.2 MLCi and MLCi2 control subsystem

3.2.1 Overview

The MLCi/MLCi2 are controlled by the following systems:

- The digital accelerator treatment control system (TCS)
  See **[Ref: 16]**.
- One of the following BLD electrical control systems:
- The remote terminal unit (RTU) assembly.
  See **Section 3.5.1**.

Note: *The Distribution, MTU/DAC and Analogue I/O PCBs are only applicable to MLCi serial number up to and including 141097, they are not applicable to MLCi2.*

- The BLD electronic assembly.
  See **Section 3.5.2**.

Note: *The BLD electronic assembly is only applicable to MLCi serial 141098 onwards, and also applicable to all MLCi2.*

3.2.2 Software

The BLD control software is structured in a similar way to the digital accelerator software in that it uses items and item part values. For a full list of MLCi/MLCi2 items and parts, see **[Ref: 1]**.

See **Chapter 4.2** for a list of error codes to facilitate system troubleshooting.

3.2.3 System communications

For details of the control system communications, see **[Ref: 1]**.

3.2.4 Block diagram

The control system is shown schematically in Figure 3.1 for an MLCi fitted with the RTU assembly and in Figure 3.2 for MLCi/MLCi2 fitted with the BLD electronic assembly.

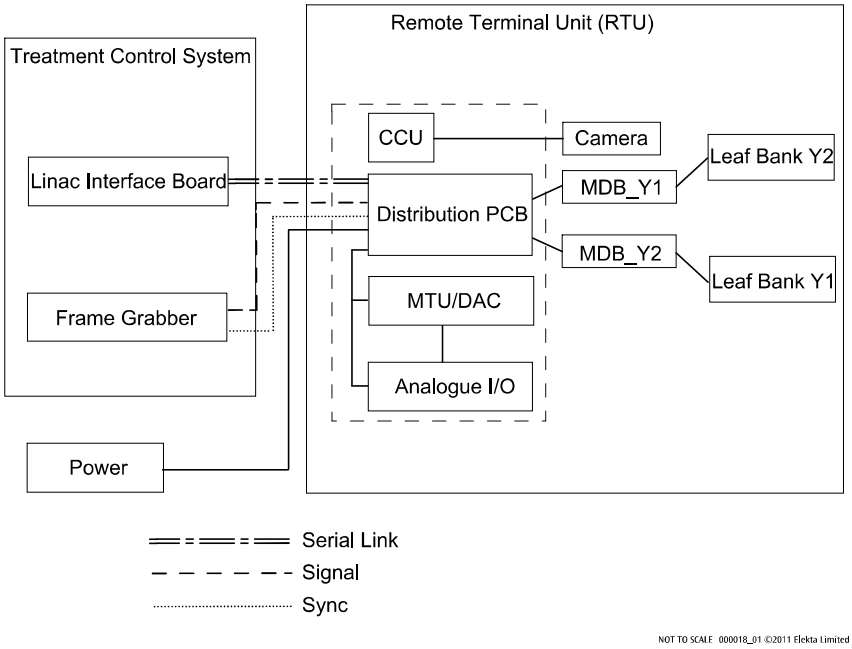

Figure 3.1 Schematic diagram of TCS and RTU (4513 332 6702)

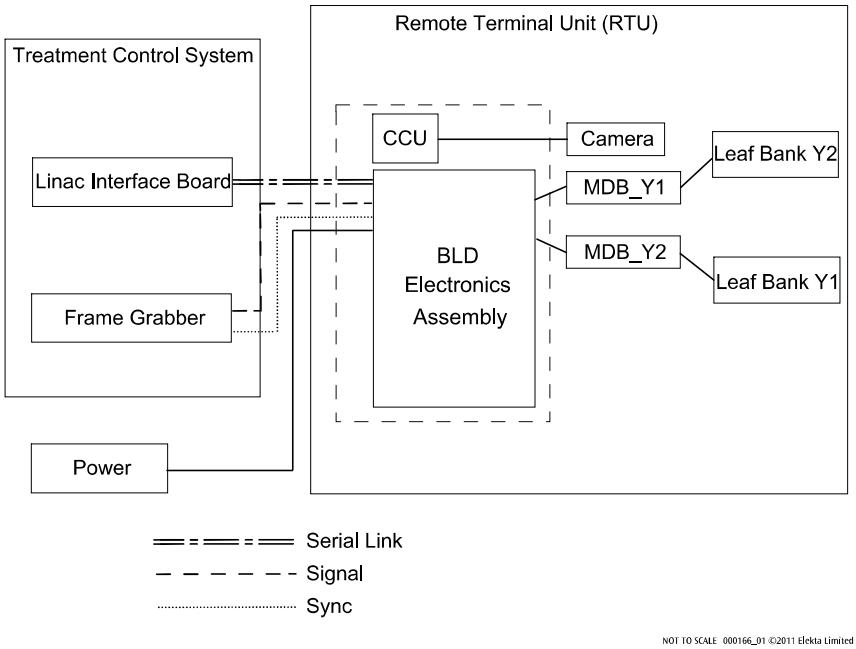

Figure 3.2 Schematic diagram of TCS and BLD electronic assembly (4513 332 8500)

3.2.5 VMAT control system (R7.0x and higher)

Desktop Pro™ R7.0x\Integrity™ R1.1 enables VMAT (Dynamic Therapy) through the purchase of additional software licences. VMAT lets the gantry, leaves, diaphragms and collimator of the MLCi/MLCi2 move during radiation delivery.

Note: *Beam Modulator™ has diaphragms which do not move.*

Before the implementation of the software Desktop Pro™ R7.0x\Integrity™ R1.1, the digital accelerator geometry parameters were set at 'segment' level directly into the TCS. See **Figure 3.3**.

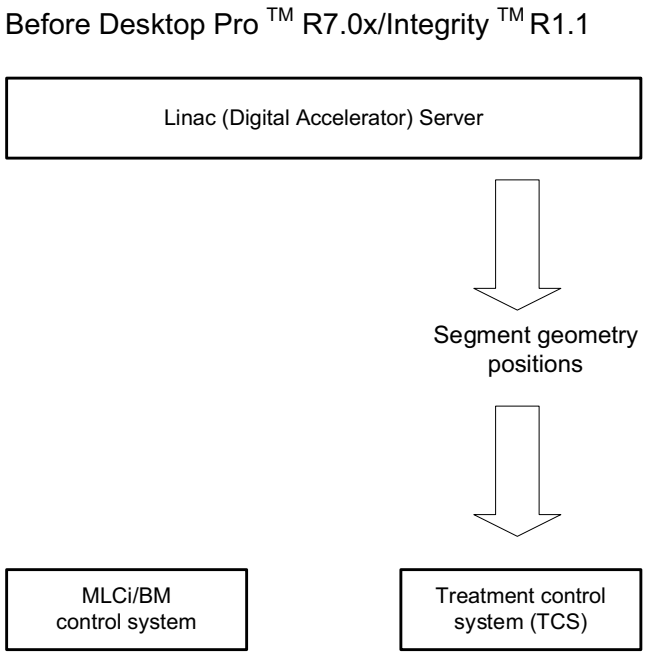

Figure 3.3 Digital accelerator geometry parameters set at segment level directly to TCS (pre R7.0x)

Note: *MLCi2 is supported only in Desktop Pro™ R7.0x and higher versions (see* **Figure 3.4***).*

In the software Desktop Pro™ R7.0x\Integrity™ R1.1, the digital accelerator geometry parameters are set into the TCS at 'step' level via the MLCi/MLCi2/Beam Modulator™. See **Figure 3.4**.

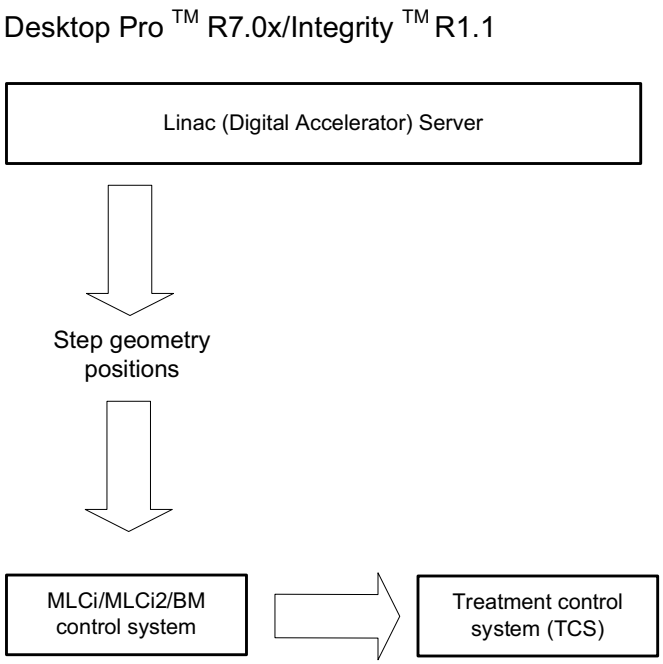

Figure 3.4 Digital accelerator geometry parameters set at step level via BLD to TCS

The geometry parameters that move are leaves , diaphragms (on MLCi/MLCi2), gantry and collimator rotation. Any combination of geometry parameter movement is supported, this includes a 'step' with no movement. Each geometry parameter is controlled independently.

Note: *A 'step' is the dose (in units of 0.1 MU) to be given between a pair of continuous control points and the geometry parameter movement to be done when the dose is given. A delivery segment can have one or more steps.*

3.2.5.1 Necessary position during VMAT dose delivery

That is the geometric parameter movement during each 'step' controlled in relation to the delivered dose. For example, if 1% of the dose is delivered, then 1% movement is completed, or if 2% of the dose is delivered then 2% of the movement is completed, if 99% of the dose is delivered then 99% of the movement is completed.

For each cycle a new position for each geometry is calculated, this uses the delivered dose. For movements of leaves and diaphragms the delivered dose is used in units of 1/64th MU. For movements of gantry and collimator rotation, the delivered dose is used in units of 1/32nd MU.

3.2.5.2 Positional errors and tolerances

During each cycle, the software compares the positional error (instantaneous or averaged) against a dynamic tolerance. If the positional error is more than the dynamic tolerance, then the software disables the PRF which stops the radiation temporarily.

Note: *Before the implementation of the Desktop Pro™ software R7.0x, if the gantry or collimator rotation was out of tolerance, then the TCS terminated the radiation immediately.*

The instantaneous positional errors for leaves and diaphragms are averaged along a number of cycles (this is currently equivalent to 1.4 seconds).
The leaf and diaphragm errors are averaged because there are no restrictions on changes in direction or speed. Therefore, with a direction change at maximum speed there can be a 'spike' in the measured error. The leaf and diaphragm errors are averaged to remove this 'spike'.

The leaf/diaphragm dynamic tolerance (**part 225**) is different from the leaf/diaphragm static tolerance (set in the database).

With a dose resolution of 1/64th MU the leaf control algorithm can accurately control the leaf position at dose rates to 50 MU/minute. Below this dose rate, accurate control cannot be achieved. So for very low dose rates, of 25 MU/minute or less a larger tolerance is applied.

The gantry and collimator rotation errors are not averaged because the direction and speed changes are set to limits by the digital accelerator server. The dynamic tolerance for the gantry and collimator rotation are held in its 'stop' item, and the static tolerance is half this value.

All tolerances are specified in absolute distances, that is, that they are not specified as percentages of distance to move.

3.2.5.3 Controlling dose delivery

When the radiation stops temporarily, the geometry items that are out of tolerance go back in tolerance, at which point radiation starts again.

The PRF disables for a maximum number of cycles (currently equal to 25 seconds) before the HT disables, this shows an inhibit of **i419—MLC Not Ready**.
Termination of radiation is controlled by the action mask of **i419**.

3.2.5.4 Movement and speed demand

It is possible for the control system to move the geometry parameters faster than the published maximum speeds. This lets a parameter 'catch up' if it falls behind when the necessary stable movement speed is equal to, or is very close, to the published maximum speed.

For static steps the speed demand signal necessary to move the parameter into position is calculated from the positional error and the proportional gain.

For dynamic steps, a feed-forward part has to be considered, even if the positional error for a cycle is zero, a speed demand signal must be applied to monitor the necessary dynamic movement above the subsequent cycle.

Note: *The feed-forward part is always implemented in gantry/collimator rotation arc treatments. The feed-forward movement is only put into effect during irradiation, if the radiation stops temporarily, only the speed demand signal that results from the positional error is put into effect.*

The feed-forward speed demand signal can cause a 'go past' of the necessary position. For example, if radiation stops temporarily because a leaf is left behind, the gantry can 'go past' the necessary position. The gantry control system thinks radiation is to be continuous and therefore applies a feed-forward speed demand signal.
If the radiation stops temporarily for a short time, for example, one cycle, the 'go past' is corrected as movement continues. If the radiation stops temporarily for a long time, the 'go past' is corrected by the positional error and can cause the gantry movement in the opposite direction.

Gantry and collimator rotation movement is controlled by the algorithm used before Release 7.0x. The movement on Release 7.0x is used on the 'step-arc' and not the 'segment-arc'. This lets 'segment-arcs' be delivered during change of speed.

3.2.5.5 Variable dose rate

The geometry parameters that move are leaves, diaphragms (on MLCi/MLCi2), gantry and collimator rotation.

During VMAT radiation delivery, these four geometry parameters have to work together in order to deliver the total radiation dose (in MU) per step.

For all fields where a geometric parameter is prescribed to move during radiation a dose rate will be calculated by the control system. This calculation aims to minimize the number of beam hold-offs caused a parameter failing to "keep up" with the delivered dose.

The maximum velocity of each geometry parameter can be seen in Desktop Pro™ R7.0x\Integrity™ R1.1, in the **Calibrate Movement Speeds** window:

1 In Service mode, click the **Calibration** primary function button.

2 Click the **Calibrate Movement Speeds** secondary function button.

In the **Calibrate Movement Speeds** window, the following information is displayed:

- Maximum gantry velocity (deg/s)
- Gantry inertia compensation distance (deg)
- Maximum collimator velocity (deg/s)
- Collimator inertia compensation distance (deg)
- Maximum leaf velocity (cm/s)
- Leaf inertia compensation distance (cm)
- Maximum diaphragm velocity (cm/s)
- Diaphragm inertia compensation distance (cm).

The default value for maximum velocity is the maximum speed of the movement. The Inertia Compensation Distance (ICD) is the distance necessary for each movement to reach the maximum velocity. The default value of the ICD is the recommended value for that the movement.

Each of these geometry parameters have a maximum velocity at which they can move. Therefore, the maximum velocity and the ICD (see *Inertia Compensation Distance (ICD)*) for each movement is used to calculate the necessary dose rate for each step of the VMAT radiation delivery.

Calculation of required dose rates and PRF for VMAT delivery

The dose rate and PRF code for each step is calculated as follows:

Ideal dose rate = Step dose / Minimum step time

Where:

Minimum step time is the maximum of:

Minimum dose time
Minimum gantry time
Minimum diaphragm travel time
Minimum collimator rotation time
Minimum leaf time.

Also:

Minimum dose time = Step dose / Maximum dose rate
Minimum gantry time = Gantry movement / Maximum gantry velocity
Minimum diaphragm travel time = Diaphragm travel / Maximum diaphragm velocity
Minimum collimator rotation time = Collimator rotation / Maximum diaphragm angular velocity.

For each leaf

Minimum Leaf Time = Leaf travel / Maximum leaf velocity.

The selected dose rate is the highest available dose rate which is not more than the ideal dose rate. The available dose rates are calculated, by successive halving of the Maximum Dose Rate (MDR) which is read from the **Linac Configuration** part. The maximum dose rate is obtained through **i44 part 134**. See Table 3.1.

Table 3.1 Maximum dose rate and PRF calculation

Dose rate	PRF code	
	Low energy	High Energy
MDR	7	6
MDR / 2	6	5
MDR / 4	5	4
MDR / 8	4	3
MDR / 16	3	2
MDR / 32	2	1
MDR / 64	1	1

If a dose rate is specified, (that is, prescribed or overridden), the nearest available dose rate to the specified dose rate, which is less than the ideal dose rate, is selected.
If the specified dose rate is equidistant from two available dose rates the higher dose rate is selected, (that is, the specified dose rate is rounded up).

Inertia Compensation Distance (ICD)

The geometry parameters do not always move at the maximum velocity.

The geometry parameters have inertia, that is, time is necessary for them to increase and decrease in speed.

The control system makes the adjustments for the inertia of geometry parameters. It causes them to move temporarily faster than their maximum velocity until they are in the correct position.

The Desktop Pro™ software takes account of the inertia compensation distance, when it calculates the movement time for each geometry parameter.

For distances above the ICD the movement time is correctly specified as Distance / Maximum velocity.
For distances less than ICD the movement time is approximate as the delivery time is not easily predicted.

In the worst condition the movement time must be less than the time to go to the ICD (that is, Inertia Compensation Distance / Maximum velocity). In the best condition the geometry item has an initial velocity equal to the maximum velocity, in this case the movement time is Distance / Maximum velocity.
The digital accelerator server does approximate between these two values based on the initial velocity to estimate the movement time.

When a change of direction is necessary the angular velocity at start for the step is assumed to be zero, the gantry is decreased in speed by the control system.

3.2.6 Description of the Leaf Nudge Algorithm

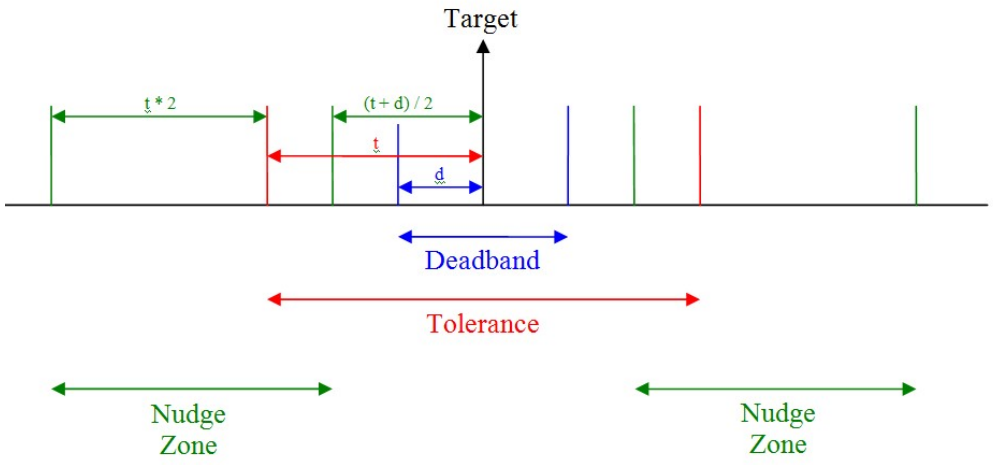

Figure 3.5 Leaf nudge algorithm

- For static leaves the positioning servo uses a proportional gain, for example the speed demand to the leaf motors is proportional to the position error.
- Each BM/MLC control system cycle the leaf positioning servo will check if the leaf is within the nudge zone and has stalled (has not moved out of the nudge zone within one second).
- If the leaf has stalled the nudge servo will increase the speed demand (voltage demand to leaf motor) by a value of one.
- The number of leaf speed demand increments is recorded in the associated leaf nudge count part.
- The nudge count value is an indication of the setup of the leaf's mechanical backlash - a high count indicates that the mechanical backlash should be reduced.
- Once a leaf was"nudged" into position any additional accumulated nudge speed demands are removed.

Figure 3.5 shows that a leaf can be in tolerance but still be nudged. This is to move the leaf away from the tolerance limit so that any subsequent small movements will not pause the dose delivery.

3.3 MLCi and MLCi2 optical system

3.3.1 Overview

The optical system has two main functions:

1 To project a light field onto the surface of the patient to represent a light equivalent of the radiation field. The center of the BLD diaphragm rotation is identified by a cross-wire, projected from the Mylar screen.

2 To project light onto reflectors, mounted on the upper surface of each leaf in the BLD leafbank, and onto four reference reflectors fixed to the leafbank frame. This light is reflected back into a video camera system, used to establish the exact location of each leaf.

The optical system is represented schematically in Figure 3.6.

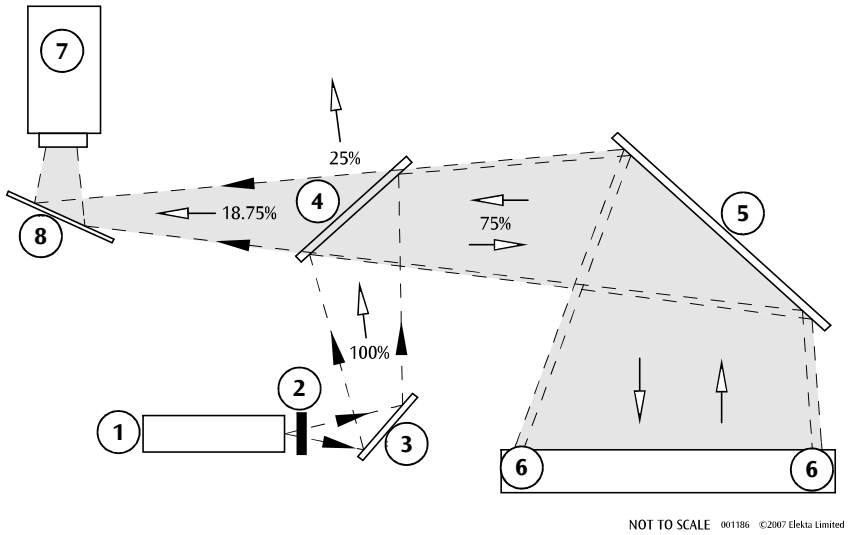

Figure 3.6 Schematic of the optical system

(1) Projector bulb assembly
(2) Projector baffle
(3) Projector mirror
(4) Beam splitter 75/25
(5) Mylar mirror
(6) Leafbank with reflectors
(7) Camera
(8) Camera mirror

The beam splitter mirror reflects 75% of the incident light and transmits 25%. The projected light passes through this mirror twice before it enters the camera, therefore, the maximum fraction of the light projected originally that enters the camera is 18.75% (100% × 75% × 25% = 18.75%).

3.3.2 Retractable optics assembly

3.3.2.1 Overview

From MLCi serial number 104173, and all MLCi2, the optical system is mounted on a single retractable module, known as the *retractable optics assembly*. This allows easy removal of the assembly for maintenance.

The modular mounting of the optical components also assists in minimizing differential movements between mirrors. When the module is refitted, all the original settings are maintained without the need for further adjustment.

The constituent parts of the optics assembly are illustrated in Figure 3.7.

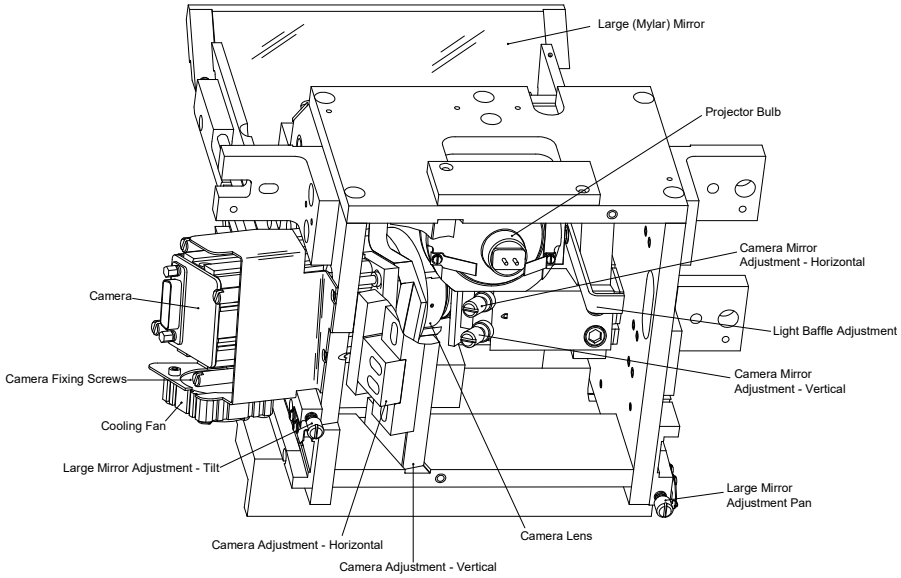

Figure 3.7 Retractable optics assembly

3.3.2.2 Projector bulb assembly

Note: *An alternative name for the projector bulb assembly is the field defining lamp.*

The projector has a longlife 13.8 V, 50 W tungsten halogen bulb with integral reflectors and slide-in bulb holder. The projector is secured on a V-block support by a clamping mechanism. This provides longitudinal adjustment and allows the projector to be adjusted to give best fit of X-ray to light fields.

Note: *The field lamp dimmer switch assembly, 4513 332 8285, controls the voltage across the bulb and should be adjusted to give a voltage reading of 12.7 V (±0.3 V). See* Section 6.2.6 *and* Section 6.2.9.

3.3.2.3 Projector baffle

The optics assembly is fitted with an adjustable baffle. The purpose of the baffle is to prevent the light from the projector passing over the projection tilting mirror and creating a secondary image in the light field area.

3.3.2.4 Projector mirror

The projector mirror reflects the projected light onto the beam splitter mirror and comprises a square, silvered glass mirror bonded to a metal support.

3.3.2.5 Beam splitter mirror

The beam splitting mirror reflects 75% of the incident light and transmits 25%. It reflects 75% of the light from the projector mirror onto the Mylar mirror and transmits 25% of the light reflected back off the Mylar mirror onto the camera mirror. Therefore, light reflected back from the leaves and reference reflectors passes through into the video camera.

The mirror is manufactured from a radiation resistant glass to prevent radiation darkening.

3.3.2.6 Mylar mirror

Note: *This mirror is not applicable to MLCi prior to 104173 and without retractable optics. It is applicable to MLCi 104174 onwards and all MLCi2.*

The Mylar mirror is manufactured from aluminized polyester film and allows X-rays or electrons to be transmitted, whilst reflecting light. It is mounted in the retractable optics assembly to reflect the image of the leaf reflectors and references reflectors into the camera.

3.3.2.7 Camera mirror

The camera mirror assembly comprises a silver glossed mirror mounted on a tilting stage. This mirror reflects the transmitted image of the reflectors into the camera.

3.4 MLCi and MLCi2 camera subsystem

3.4.1 Overview

The camera system comprises the following parts:

- Remote camera.
- Interface cable.
- Camera control unit (CCU) PCB.

The camera is mounted on the retractable optics assembly, outside the radiation beam axis. The CCU PCB is mounted in or on the BLD electrical control system (RTU or BLD electronic assembly). The camera images the leaf and reference reflectors and the CCU sends the video signal to the treatment control cabinet (TCC).

There are two camera systems, summarized in:

- Section 3.4.2 (for MLCi only)
- Section 3.4.3 (for later MLCi and all MLCi2).

Note: *The different cameras, CCU PCBs and BLD electrical control systems are all compatible, but the full functionality of camera 4513 332 8445 will only be realized with the system configuration described in* Section 3.4.3.

3.4.2 MLCi camera system — part number 4513 332 6640

3.4.2.1 Overview

The configuration of MLCi camera system part number 4513 332 6640 is shown in Table 3.2.

Table 3.2 MLCi system configuration for MLCi camera system part number 4513 332 6640

System	Description	Part number
MLCi camera	Remote camera	4513 332 6645
	CCU PCB	4513 332 6647
	Cable assembly	4513 332 6646
BLD electrical control	RTU assembly	4513 332 6702

See system diagram 4513 332 7065 for connections for the configuration in Table 3.2.

3.4.2.2 Camera

The remote BLD camera, part number 4513 332 6645, is the original radiation-hard camera fitted to the older MLCi only.

This camera incorporates a 17 mm CID (charge injection device) chip and a 12.5 mm f1.8 lens fixed to focus at 300 mm. Clamping brackets are used for positional adjustment. The camera mirror positioned in front of the camera lens allows optical alignment of the image to camera.

Note: *This camera is now obsolete.*

3.4.2.3 Camera control unit (CCU)

The CCU PCB, part number 4513 332 6647, processes the leaf and reference reflector video image from the camera and outputs the data to the treatment control cabinet (TCC) via the RTU assembly. The CCU receives a video synchronizing signal from the TCC via the RTU assembly.

Signal connections to the CCU PCB are shown in Figure 3.8.

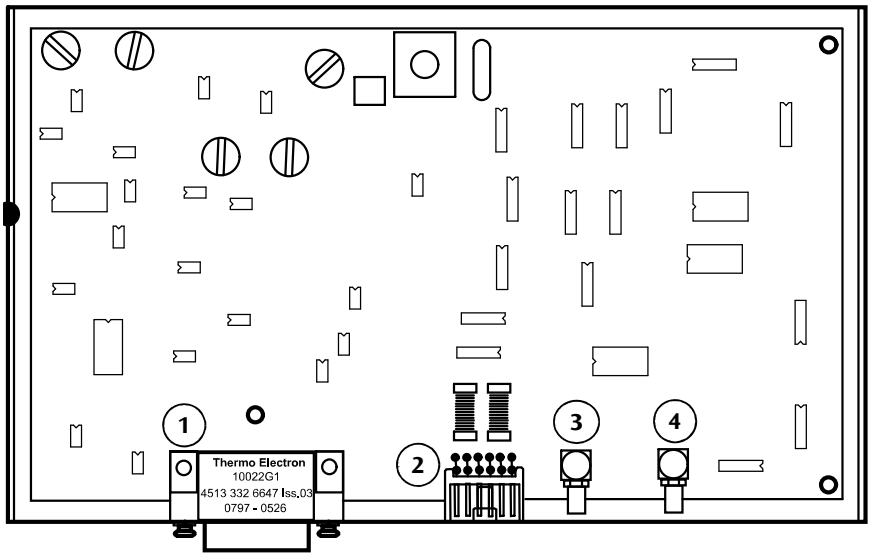

Figure 3.8 Signal connections to the CCU PCB (4513 332 6647)

(1) SKCA — camera in
(2) PLCB — to Distribution board
(3) SKCD — video out
(4) SKCC — sync. in

3.4.2.4 Interface cable

The interface cable is a multicore cable terminated with a 26-way plug and socket and connects the camera to the CCU.

3.4.3 MLCi/MLCi2 camera system — part number 4513 332 8440 and 1006512

The configuration of later MLCi camera system part number 4513 332 8440 is shown in Table 3.3. This is factory-fitted to MLCi serial number up to and including 141471 (except MLCi serial numbers 141464 and 141465 which are fitted with the upgraded camera system part number 1006512). This camera system is also used in conjunction with Desktop Pro™ Release 6.0x and onwards, it provides the functionality to adjust the image gain of the camera automatically and to read the temperature of the camera by item part values, as follows:

- Camera gain — **i2221 MLC Camera Iris**, **part 199** (enable) and **100** (set).
- Camera temperature — **i2222 MLC Temperature**, **part 101** (raw value) and **111** (actual value)

.

Table 3.3 MLCi system configuration for MLCi camera system part number 4513 332 8440

System	Description	Part number
MLCi camera	Remote camera	4513 332 8445
	CCU PCB	4513 332 8447
	Cable assembly	4513 332 8446
BLD electrical control	BLD electronic assembly	4513 332 8500

See system diagram 4513 332 7953 for connections for the configuration in Table 3.3.

Upgraded camera system — part number 1006512

The upgraded camera system is factory-fitted to MLCi serial number 141472 onwards and also to MLCi serial numbers 141464 and 141465.

The upgraded camera system is also factory-fitted to all MLCi2.

The upgraded camera system contains an upgraded CCU PCB—part number 1006511. The configuration of applicable MLCi and all MLCi2 camera system is shown in Table 3.4.

Table 3.4 MLCi/MLCi2 system configuration for camera system part number 1006512

System	Description	Part number
MLCi camera	Remote camera	4513 332 8445
	CCU PCB	1006511
	Cable assembly	4513 332 8446
BLD electrical control	BLD electronic assembly	4513 332 8500

Note: *FCO 554061 describes the upgrade kit, it gives instructions on how to upgrade a previous version of a MLCi camera system to the newer upgraded camera system.*

3.4.3.1 Camera

The remote camera, part number 4513 332 8445, is a modified radiation-hard camera with the following added features:

- Electronic iris control
- Thermoelectric (Peltier) cooling of the CID chip.

These features will only be realized using the MLCi/MLCi2 system configuration shown in Table 3.3.

3.4.3.2 Camera control unit

The CCU PCB, part number 4513 332 8447 (and 1006511), processes the leaf and reference reflector video image from the camera and outputs the data to the treatment control cabinet (TCC) via the BLD electronic assembly. The CCU receives a video synchronizing signal from the TCC via the BLD electronic assembly.

Signal connections to the CCU PCB are shown in Figure 3.9.

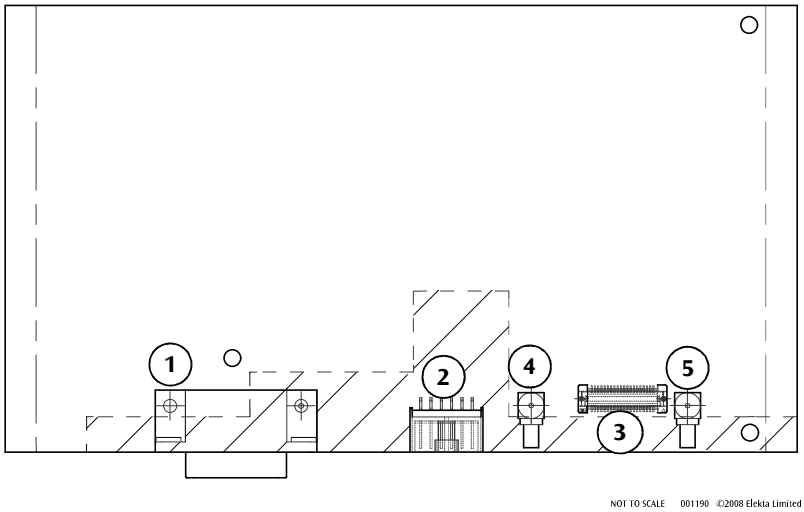

Figure 3.9 Signal connections to the CCU PCB (4513 332 8447 and 106511)

(1) SKCA — camera in

(2) PLCB — To Distribution board (RTU assembly only)

(3) SKCE — BLD electronic assembly daughterboard

(4) SKCD — video out (RTU assembly only)

(5) SKCC — sync. in (RTU assembly only)

Note: *Connectors PLCB, SKCD and SKCC are redundant for the camera system shown in Table 3.3 and Table 3.4. They are only used if the (older) camera part number 4513 332 6645 is connected to this CCU PCB or if this PCB is connected to an RTU assembly in MLCi numbers prior to and including 141096.*

3.4.3.3 Interface cable

The interface cable is a multicore cable terminated with a 26-way plug and socket and connects the camera to the CCU.

3.4.4 Mylar screen

The mylar screen is fitted across the face plate of the BLD. The mylar screen incorporates a crease to minimize unwanted reflections.

Cross-wires are marked on the screen and the projected image indicates the center of diaphragm rotation. The projected image of a triangle next to the cross-wires confirms the orientation of the wedge.

3.4.5 Positional read-out of the BLD leaves

During operation, the entire multileaf unit is controlled by the digital accelerator control system. The software identifies the current position of each leaf and changes it to meet new requirements as each prescription is downloaded. Visual confirmation of each new leaf position is provided by a color monitor that displays a live image of the white reflective spot on the upper surface of the leaf.

Light from the projector bulb assembly (field defining lamp) illuminates these spots and is reflected back through the optical system to form a real image at the CCD camera. The resulting black and white video signal is channelled through a vision processor, where image data is read to ascertain leaf reflector positions and perform associated computations. Computer generated colored overlays, which serve as indicators, may also be displayed on the color monitor.

In the event of a discrepancy between the required and actual leaf locations, after a prescription has been loaded, the computer software displays a small red rectangle (indicator) on the color monitor. Lying on the same video line as the leaf in question, this indicator appears on the left side of the screen if the leaf is in the left hand bank and vice versa. Separate indicators are displayed for each leaf discrepancy. Red indicators also appear when a leaf search is taking place before a prescription is loaded.

The video display indicates the prescription outline showing all leaves within the diaphragm position filled in with a solid color.

3.4.6 Digital image processing of the video signal

Analogue signals from the camera are routed by a coaxial cable to the signal isolation assembly in the treatment control cabinet (TCC). The signal is processed to reduce the effect of camera radiation and split into three signals, two of which are routed to the display processor for presentation on the user interface and the other routed to the video digitizer PCB. The analogue video signal is converted to a digital image of 512 × 512 pixels in systems with Deskop Pro™ R5.0 and lower. For systems with Desktop Pro™ R5.1 onwards, the analogue video signal is converted to a digital image of 768 × 512 pixels. The positional information for the leaves and reference reflectors is determined by the RMX processor and passed on to the display processor.

The analogue video signal from the camera contains both video and timing information. The synchronizing pulses at the start of each line act as timing references for the analogue data present between the pulses. A standard video signal has synchronizing pulses of depth 0.3 V and peak white amplitude of 0.7 V giving a nominal 1.0 V signal. The output is twice this level when correctly terminated with 75Ω at the camera/serial link interface board.

The horizontal scan lines that make up a frame are divided into two fields: an *even* field consisting of all the even numbered scan lines, beginning with line zero (the top-most line) and an *odd* field containing all odd numbered lines from line one. The two fields are interlaced to form the complete frame.

Lines from a pair of successive odd and even fields are merged in frame memory by the image processor and processed to create a non-interlaced image for display on the monitor.

3.4.7 Reference reflectors

The optical system described in this chapter also monitors the positions of four fixed reference reflectors located on the upper surface of the leafbank frame, near the corners of the maximum available multileaf aperture. These reflectors are checked at each computer video access to make sure that they maintain a fixed relationship with the optical system. This in turn makes sure that the leaf calibration data is still valid. Calibration data may be invalidated if some section of the optical system, such as the video camera, is accidentally moved. Once the positions of the fixed reflectors have been determined during calibration, a blue indicator is displayed inside each reference reflector image to confirm location.

If a reference reflector cannot be found, a red indicator is displayed at the position where the system is looking for a reflector (this is instead of the blue indicator which is displayed when the reflector is found). This assists in repositioning the camera to align the indicators with the white reflector images.

3.5 MLCi and MLCi2 electrical control subsystem

The primary function of the BLD electrical control system is to receive data from, and send data to the treatment control system (TCS) via the serial link.

There are two versions of the electrical control system:

- The remote terminal unit (RTU) assembly — fitted on MLCi serial numbers up to and including 141097 (see Section 3.5.1).
- The BLD electronic assembly — fitted on MLCi serial number 141098 onwards and all MLCi2 (see Section 3.5.2).

3.5.1 Remote Terminal Unit (RTU)—Part number 4513 332 6702

The RTU assembly comprises three boards:

- Distribution board
- Multiplex terminal unit (MTU)
- Analogue I/O PCB.

The assembly also houses the following PCB:

- Camera control unit (CCU).

3.5.1.1 Distribution board

The Distribution board is the central interconnection between the treatment control system (TCS), the retractile cable and other parts of the BLD electrical control system.

Power supplies

The power supplies that are monitored and distributed by the Distribution board are listed in Table 3.5.

Table 3.5 The power supplies of the Distribution board

Power supply	Location	Purpose
+5 V (VCC)	RHMD	Drives most MLCi circuitry.
±15 V (SIG)	RHMD	Drives the camera, fan and DACs on the MTU board.
±15 V (PWR)	Adjacent to the RHMD	Drives the leaves and motor drive board circuitry.
+10 V (REF1 & 2)	RHCA	REF1 supplies both fine and coarse read-out pots and REF2 supplies the check pots.

Note: *Although ±26 V is used by the BUD drive boards in the RHMD, these supplies do not pass through the Distribution board.*

A power-fail detection circuit monitors the foregoing supplies and provides a *SUPPLIES ON* signal as an input term on the Distribution board FPLA (field programmable logic array). The same signal inverted (called *SUPPLIES OK*) is a digital input on the MTU board and can be read straight onto the RT data bus. The Distribution board LEDs are listed in Table 3.6.

Table 3.6 Distribution board LEDs

LED	Color	Signal
D1	Yellow	Serial link active
D2	Red	Leaf limit activated
D4	Yellow	Camera video
D5	Green	+5 V VCC
D6	Green	+15 V SIG
D9	Green	+15 V PWR
D11	Green	–15 V SIG
D3	Green	–15 V PWR

The ±15 V (PWR) supplies to the motor drive boards are routed via the control logic on the Distribution board. This means that a range of error conditions can interrupt the ±15 V supply and inhibit leaf movement.

Serial link

This is isolated and buffered on the Distribution board to make sure that transmitted and received signals are passed to the MTU board.

Leaf control logic

Two pairs of relay contacts on this board form part of the *PRF* and *HT ENABLE* interlocks, although these contacts are housed on two independent relays.

Logic control is effected mainly by an FPLA, which receives various signals from the MTU board plus confirmatory connection signals from each of the motor drive boards. The FPLA then decides which relays should be energized (that is, PRF enable and HT enable).

BUD signals

The BUD analogue demand signals, plus the appropriate logic ENABLE signals, pass straight from the GP bus to PL5 and then the RHMD rack. These constitute the input signals to the diaphragm motor drive boards and are not processed by the Distribution board.

3.5.1.2 Multiplex terminal unit (MTU) PCB

The MTU is a multiplex terminal and digital-to-analogue converter unit. The PCB decodes remote terminal bus information from serial link data and encodes return information for transmission via the serial link. The PCB contains two DACs and handles some dedicated I/O. The DACs provide the analogue multiplex demand signals for the leaf and backup diaphragm drives.

The MTU PCB supports a parallel bus similar to the RTUs, which allows for future expansion.

MTU decoding

Data arriving from the serial link (and designated *Tx_in*) is shifted into an eight bit register, converted to parallel data and fed into a Field Programmable Logic Sequencer (FPLS) which generates a signal to trigger the watchdog timer. If the incoming serial data subsequently stops for more than 300 ms, the timer will cause the remote terminal to reset, thereby stopping leaf and diaphragm movement. The FPLS also decodes the incoming serial signal to provide data and address information.

MTU encoding

Data and status are loaded into two 16-bit shift registers such that information in the correct format can be serially shifted into the FPLS. It is buffered and sent to the serial link driver for transmission to the control system.

3.5.1.3 Analogue I/O PCB

The Analogue I/O PCB is the interface between the signals from the MLCi and the RTU. It handles analogue and digital inputs and analogue and digital outputs. It is connected to the MTU board by the RT bus and to the Distribution board by the GP bus.

The digital signals consist of the applicator type code bits (digital inputs 0 to 6), accessory type code bits (digital inputs 7 and 8) and applicator present and wedge out sense (digital inputs 14 and 15 respectively).

These signals are buffered by single transistor, inverting amplifiers, and fed in parallel into a 16-bit latch. When the correct address, accompanied by a control signal called *off_board_read*, is received by the field programmable logic array (FPLA), the contents of this latch are read onto the RT data bus.

The analogue inputs are fed into what is effectively a 16 channel multiplexer, via simple R-C filters. The multiplexer can then be addressed by the RT address bus. The multiplexer output goes to an ADC which is controlled by the FPLA. Finally the ADC output is read straight onto the RT data bus, again under the control of the FPLA.

When the FPLA on the board receives the correct address, and an *off_board_write* signal is present, an 8-bit latch is loaded from data bits 0 to 7 on the RT bus. These bits represent the signals shown in Table 3.7.

Table 3.7 RT data bus

RT data bus	Digital signal
D0	Bud_X1_Enable
D1	Bud_X2_Enable
D2	Bud_Y1_Enable
D3	Bud_Y2_Enable
D7	Hc_mode_LED

From the information on the RT bus, the FPLA decodes a signal called *Bdack_out* which is used to check regularly the presence of connectors PL3 and PL4. This signal is also used to re-trigger a watchdog timer which must be written to at least once every 300 ms, otherwise it will cause a reset. This resets the whole RTU and causes the 8-bit digital output latch to be cleared. This puts all the backup diaphragm enable signals to their inactive state and thereby stops diaphragm movement.

All the watchdog timers in the RTU are connected to the reset line which is part of the RT bus, so that if any one of them times out, the result will be the same.

There are four analogue outputs from this board for the four backup diaphragm motor demand signals. These analogue outputs are derived from analogue signals coming from the DACs on the MTU board, called *V_out_1* and *V_out_2*. The X1 and Y1 backup diaphragm drive signals are derived from *V_out_1* and the *X1* and *Y2* drive signals, from *V_OUT_2*. When the address is correct, together with an *off_board_write* signal, the FPLA will enable the relevant pair of sample and hold circuits. This captures the voltage level currently on *V_out_1* and *V_out_2*, which is then fed to the appropriate diaphragm motor drive board. The voltage level at the output of the sample and hold circuit will remain constant until the circuit is once more enabled to sample by the FPLA.

3.5.2 BLD electronic assembly—Part number 4513 332 8500

The BLD electronic assembly consists of two PCB assemblies, the mother and daughterboards, with associated firmware.

The BLD electronic assembly is used in MLCi serial number 141098 onwards and all MLCi2 (the assembly replaces the Distribution board, Analogue I/O PCB and multiplex terminal unit of the RTU. See Section 3.5.1).

Figure 3.10 illustrates the subsystems of the BLD electronic assembly interfacing with the MLCi or MLCi2 and the digital accelerator.

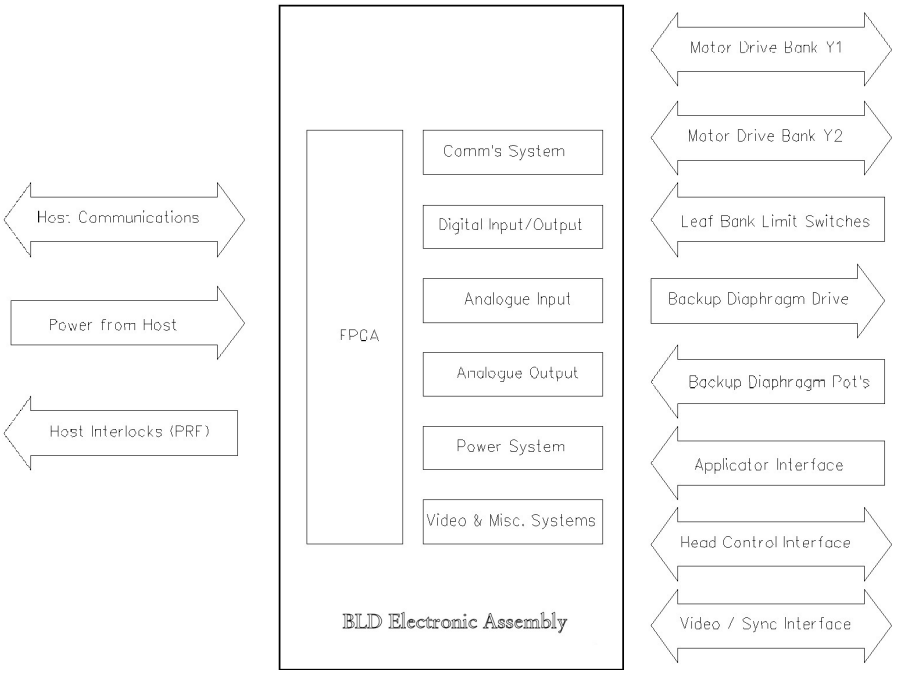

Figure 3.10 Interfacing of the BLD electronic assembly with the MLCi or MLCi2 and digital accelerator

3.5.2.1 Analogue output system

The purpose of the analogue output system is to provide eight channels of 8-bit analogue output. The daughterboard features two quad 8-bit DACs (MAX508) with a simple parallel data bus, two address lines and an enable. Data written to the DACs is latched. The daughterboard features a 16-bit bidirectional bus, which is split between the two DACs.

A 5 V reference is divided to 2.5 V by *IC105* to provide a reference for each of the DACs. The DACs employ a single +5 V supply and output a 0 to +2.5 V output voltage.

The raw signals are buffered by *IC103* and *IC104*. Eight identical circuit modules take the 0 to 2.5 V and with the use of a 1.667 V offset voltage produce outputs in the range ±5 V. The *TL084*s used are fairly low precision devices with adequate current and slew rate output capability.

The output from each amplifier is filtered to reduce output switching noise and to protect the amplifiers.

Therefore, the circuits produce eight analogue output signals which are used as shown in Table 3.8.

Table 3.8 Analogue output signals from the analogue output subsystem

Signal	Function	Data Source	Filter Time Constant (s)
VOut_0	Backup diaphragm X2 speed demand	lsb	10
VOut_1	Backup diaphragm Y2 speed demand	lsb	10
VOut_2	Speed demand Y1 leaves	lsb	1
VOut_3	Camera iris motor drive	lsb	1
VOut_4	Backup diaphragm X1 speed demand	msb	10
VOut_5	Backup diaphragm Y1 speed demand	msb	10
VOut_6	Speed demand Y2 leaves	msb	1
VOut_7	Spare — fed to analogue input channel 25	msb	10

The mapping of MTU subaddresses to DAC addresses is handled by the FPGA firmware.

The final section of circuitry in this subsystem is a high power amplifier for the camera iris motor drive. An *OPA549* power op-amp is used for this function because it features an output disable function. The ±5 V signal from *VOut_3* is amplified to produce an output in the range ±7.3 V at 100 mA. The *OPA549* is mounted on a heat sink. The bandwidth is limited with a 3 dB roll-off at 100 Hz. In the current application, the signal is routed to the CCU which performs this function electronically.

TR101, *TR102* and *TR103* form a level shifter to create active low output disable circuit. *D103* and *D104* OR an */Iris_Disable* signal and an inverted */W_D_OK* signal to disable the output under controlled conditions or if the hardware watchdog fails. Refer to the FPGA system for details of the watchdog circuit. The */Iris_Disable* signal is derived from digital output bit 4.

3.5.2.2 Digital I/O system

This system is responsible for providing 48 lines of digital input (in three channels of 16) and eight digital outputs.

The first 16 channels, *D_IN[15..0] (DIO[15..0])* feature active high inputs using a single NPN transistor. The inputs require +15 V (supplied via R13 on the motherboard) to turn on the transistor and provide an active low input signal. A simple RC filter is used to suppress noise. These 16 lines are mapped to subaddress 2 in the MTU. The signals are used by the applicator. Refer to the pinout for *PL26AH* for the bit assignments.

The next 32 channels all feature a passive active low input with an RC filter. *D_IN[31..16]* is mapped to subaddress 1. Refer to *PL26AF* pinout for bit assignments.

D_IN[47..32] is mapped to subaddress 3. Refer to *PL26AI* pinout for bit assignments.

The digital outputs feature a simple open collector drive arrangement. Current limiting resistors are included. The assignment of bits is described in Table 3.9.

Table 3.9 The digital output signal description from the digital I/0 subsystem

Signal	Function	Connector
DOut_0	Backup diaphragm X1 active LOW enable	PL26AA
DOut_1	Backup diaphragm X2 active LOW enable	PL26AA
DOut_2	Backup diaphragm Y1 active LOW enable	PL26AA
DOut_3	Backup diaphragm Y2 active LOW enable	PL26AA
DOut_4	Camera iris enable	N/A
DOut_5	Unassigned	N/A
DOut_6	Spare output (PL26AH Pin 9)	PL26AH
DOut_7	(BLD) Head control LED drive	PL26AH

All inputs and outputs connect to the FPGA without multiplexing.

3.5.2.3 Power systems

The power system provides some fundamental features, for example, supply rail decoupling. Five LEDs (301–305) indicate the status of the 5 V and the two ±15 V rails.

Two similar circuit modules are created by *IC302*. These amplifiers measure the voltage of *VPOS2* and *VNEG2* producing an output for feeding analogue input channels 29 and 30 respectively. The magnitude of the signal is such as to create a decimal count from the ADC equivalent to the voltage, that is 14.95 V gives a count of 1495. The values can be read from MTU subaddress *0x037* and *0x038*.

IC301 provides a precision 5 V reference for use in the analogue input and output systems.

IC303 is used to monitor the state of the two ±15 V power supply rails. The device features four open drain comparators. This circuit has several peculiar features deserving explanation. *IC303* features an onboard 1.18 V voltage reference for use by the comparators but this was not used as it may be susceptible to radiation damage. A 1.18 V reference was therefore created from the 5 V supply.

A negative supply is required by the IC in order for it to sense negative inputs. A -4.7 V supply is derived from the two –15 V supplies. Clearly, if both supplies disappear, sensing the negative supplies is not an issue.

The switching thresholds for the 15 V rails are set at approximately 6 V. This low value was chosen to duplicate the function of the Distribution board and make the system tolerant to transients on the power supplies.

The four outputs from the comparators are pulled up to 5 V with 100 kΩ resistors and then fed to the FPGA. The FPGA routes the signals as follows:

Table 3.10 The power supply signals

Signal	Channel mapping
VPOS1	Subaddress 1, bit 1
VNEG1	Subaddress 1, bit 0

Table 3.10 The power supply signals

Signal	Channel mapping
VPOS2	Subaddress 1, bit 3
VNEG2	Subaddress 1, bit 2

It also creates a single */Supplies_OK* signal that is mapped to subaddress 1, bit 8. It is therefore possible for the host to check the status of the 15 V supplies, because normal operation is not suspended. The firmware will, however, disable the PRF relays and cut the power to the motor drive boards.

The motherboard also contains some decoupling capacitors. Transient suppressors are provided on the signal ±15 V supplies and +5 V rail.

Finally, the motherboard features three identical dual power switches. These are used to switch the signal ±15 V supplies to both motor drive boards and the ±15 V motor supplies to each motor drive board. Power MOSFETs (N and P-channel) devices are used for switching with all six devices mounted on a heat sink via insulating kits. A push-pull driver is used for controlling the gates of the transistors. A transient suppressor is fitted between drain and source of each transistor to prevent damage from voltage transients.

3.5.2.4 Communication system

Most of the circuitry for the communication system is located on the motherboard, with the exception of the *SJA1000T* CAN controller.

The primary communication system used is the 1553 serial link as used elsewhere on the digital accelerator. This uses a transformer to couple transmit and receive data onto a pair of conductors. The circuitry is copied from the standard MTU cards (4513 390 7774) used in the control areas. See group 161 document of assembly 4513 330 5658 for further information.

The CAN bus interface is also duplicated from the standard MTU card. Opto-isolators and an isolated CAN driver are used to keep this interface separate from the remaining circuitry. Note that this isolation is functional only and it does not comply with any of the creepage and clearance requirements of IEC60601-1.

3.5.2.5 Video and miscellaneous systems

All of the circuitry for this subsystem is located on the daughterboard. Four elements comprise the video processing section. *IC501* forms a high-speed video amplifier with a gain of 4.92 that is used to increase the amplitude of the composite video (luminance, blanking and synchronizing, but no chrominance or burst) signal from the CCU from 1 V to approximately 5 V. This large signal is fed from the BLD, across the cable reeling and to the treatment control cabinet (TCC) in the control room. Here it is processed and returned to a 1 V level.

IC402 (host part in the communication schematic) is a differential receiver taking the synchronizing signal and converting it to a TTL compatible signal for the CCU.

LED501 is the *genlock* LED that indicates the synchronizing status of the CCU.

IC603 is a 12 V voltage regulator that is only required for older Mk1 BLDs. The device is mounted flat on the PCB, which constitutes a sufficient heat sink for load currents up to 0.5 A.

The BLD sense section takes the signal from the BLD control LEDs and level shifts it to a TTL compatible format for connection to the FPGA. The action of the FPGA is to disable the *PRF2* relay whenever the LEDs are illuminated.

The BDAck Processing section features some circuitry that operates as follows. When the *MUX_Enable* line is asserted for the motor drive boards, they will drive their respective BDAck signals LOW. Thus the signal *BDAck_Out* will be driven HIGH only if the BDAck signal from *Y1 MDB* and *Y2 MDB* are both LOW. The *BDAck_Out* signal is fed out to the BLD cable loom assembly via *PL26AG*. If the wiring is in tact, this signal will be fed via *PL26AH* where it becomes *BDAck_In*. Thus *R527* provides the collector load for *TR502* and *TR508*. *TR503* provides the signal *BDAck_3* which will be low if the two MDBs are connected and *SK26AG* and *SK26AH* are plugged in.

The *BDAck_3* signal is used as the BDAck signal by the MTU firmware whenever an access to the MDBs is made by the host. Failure of this signal will result in incomplete communication.

Finally the PRF relays section of circuitry features a drive circuit for the two PRF relays. The relay *PRF1* requires an active HIGH drive from the FPGA to energize the coil whereas relay *PRF2* requires an active LOW drive from the FPGA to energize its coil. This means that if the FPGA fails with all outputs HIGH or all outputs LOW, only one relay will be energized, thus preventing radiation.

Each drive circuit has an input of the appropriate sense from the watchdog circuit to inhibit energization if the watchdog has failed.

3.5.2.6 FPGA system

This is a complex subsystem, because the FPGA forms the active center of the BLD electronic assembly.

The FPGA is the 208 pin *FLEX 6024 QFP* device used in many other designs. The EPC1 configuration device is used to store the firmware.

Two clock oscillator modules are used, 10 MHz for the majority of the system including the 1553 communications firmware and 24 MHz for the CAN communications firmware.

The FPGA requires 5 V for the I/O circuits and 3.3 V for the logic core. *IC606* provides the lower voltage. Plenty of local decoupling is provided.

IC603 and *IC604* are octal buffers used to provide drive signals for the two motor drive boards (MUX address and enable), 1553 serial data to the host (*RX_1553* and *nRX_1553*) and drives for six LEDs (comms, comms latch, leaf limit and three spare).

A socket is provided for *IC605* so that new configurations can be deployed. The circuit arrangement for the configuration device is as per the Altera databook.

A JTAG port is provided for test purposes. The arrangement is as per the Altera databook.

An uncommitted test connector, *PL602* is provided for development and possible test purposes.

Five simple passive filters are provided to isolate the FPGA from the external connections status 0 – status 4 on *PL26AF*.

Two DIP switches are provided with functions as described in Table 3.11.

Table 3.11 The DIP switches in the FPGA system

Ref	Net	Function	Mode	
LK601	DIP_1	Camera iris mode	ON — disabled	OFF — enabled
LK602	DIP_2	Motor current mode	ON — disabled	OFF — enabled

Finally, there is a complex watchdog circuit. Two quad comparators are used to monitor power supply rails, configuration status, power-up status and various reference voltages. A single active LOW reset signal is produced that inhibits all FPGA logic activity. This means that no communications by the host will be successful. If all of the hardware conditions are fulfilled, the FPGA can start and it should generate pulses for a watchdog formed by *IC610*. If these pulses arrive approximately every 1 ms, then the *W_D_OK* line will be asserted HIGH. Similarly the active LOW */W_D_OK* will be asserted. This will enable energization of the PRF relays is commanded by the FPGA *PRF1/2* relay drive signals. The hardware ready LED will also illuminate when the watchdog is healthy.

Further explanation of the thresholds for the comparators is described in Table 3.12.

Table 3.12 Explanation of the thresholds for the comparators

Signal	Condition for OK
Vcc	>4.7 V (resets >4.8 V)
3.3 V	>2.6 V
FPGA configuration	Completed OK
C639 voltage	Power applied for > 0.5 s
5 V reference	>4.4 V AND < 5.4 V
1.667 V reference[1]	>-0.75 V AND <2.2 V
4.096 V reference[1]	>1.6 V AND <4.7 V
2.5 V reference A[1]	>0 V AND <3.0 V
2.5 V reference B[1]	>0 V AND <3.0 V

1 A summing network is used for these signals. The condition for OK assumes that only one of the signals is varying and that the other three are at their nominal value. The range is quite wide but the purpose of detection is to determine whether one of the op-amps that generate these references has failed.

A 1.18 V reference is generated from the 5 V rail, rather than using the internal voltage reference. Clearly, for the non-Vcc reference detection to operate correctly, it is assumed that the Vcc rail is at 5 V. If the Vcc rail is low, the *5 V reference <5.4 V* comparator will detect this and inhibit operation.

3.5.2.7 Analogue input system

The purpose of this subsystem is to provide 32 channels of 12-bit analogue input. All input channels are filtered with a 720 Hz, 1st-order passive network before feeding to two dual 8-channel multiplexers. Thus four signals are produced that are fed to the ADC. The *DG407* multiplexers require a ±15 V supply and have TTL compatible address (three lines) and enable inputs. The firmware controls the address select lines according to the subaddress requested by the host.

The multiplexer outputs are unity-gain buffered and fed to four inputs on a 6-channel, 12-bit ADC, the *MAX196*. This device features an onboard reference but this is not used in case it suffers radiation damage. *IC705* is used to create a 4.096 V reference and an unused -15 mV reference. The ADC features a microprocessor type interface with a 12-bit bidirectional data bus and read/write lines. Acquisition is achieved by writing a channel select and range select. Conversion is initiated by a second write to the device. A conversion complete signal is provided to indicate that data is ready. The firmware controls all of the sequencing to provide conversions. The device requires a 2 MHz clock that the firmware derives from the 10 MHz system clock. All of the 32-channels are read as unipolar 0-10 V inputs.

The other two inputs on the ADC (Ch4 and Ch5) are used for reading leaf motor current signals. These are time-division-multiplexed bipolar (±5 V) signals generated by the two motor drive boards. The signals are filtered with a 160 kHz, 1st-order passive network before feeding to Ch4 and Ch5 on the ADC.

3.5.3 Motor drive board

There are three versions of the motor drive board (Point of introduction in brackets):

- 4513 390 4654 (for MLCi serial numbers 104278 to 141096)
- 4513 390 9024 (for MLCi serial numbers from 141097 to 141311)
- 4513 390 9025 (for MLCi serial numbers 141312 onwards and all MLCi2).

3.5.3.1 Motor drive board — part number 4513 390 4654

The motor drive board receives analogue drive signals for each leaf in the bank that it controls. Its main function is to demultiplex these drive signals, sample and hold each one, and then regulate the speed of each leaf accordingly.

The analogue drive signals are present on the *V_out_1* and *V_out_2* lines. The former line carries all the Y1 leaf drive signals and the latter carries the Y2 signals. The address lines tell the demultiplexer which of the leaf drive signals is present on the *V_out_1* or *V_out_2* line at a particular time, thereby selecting a specific leaf drive channel.

The actual voltage on each of the leaf sample and hold outputs is then demultiplexed back for comparison with the demand value. If the sample and hold does not track the demand signal, the closed loop amplifier drives the sample and hold to correct the sampled value. These sampled values are then fed in as the demand to a fixed velocity speed circuit, which drives the leaf motors. The demand values range from +5 V to –5 V depending on direction.

The maximum value that the control system should write as a leaf speed should be 25% less than the absolute maximum demand, so that there is some margin for the regulator to increase the drive to the motor, as the torque requirements vary.

Three control signals exist:

- *MUX_EN*
  Enables the demultiplexers and multiplexers to become active.
- *BD_ACK_1* and *BD_ACK_2*
  These two signals check that each motor drive board is connected. They are ANDed with other board acknowledge signals to form a single signal which is part of the status byte read by the *Sys 320*.

3.5.3.2 Motor drive board — part number 4513 390 9024 and 4513 390 9025

Motor drive board part number 4513 390 9025 is a replacement for all BLD motor drives, therefore Motor drive board part number 4513 390 9024 is now obsolete.

In operation, the board receives demands from the BLD electronic assembly for any combination of the 40 BLD leaves and drives the corresponding outputs accordingly.

The BLD electronic assembly is capable of reading the current value of each of the drive outputs from the motor drive board, allowing the motor current to be read by Desktop Pro™ (release 6.0x onwards)/Integrity™ R1.1.

The board receives time-division-multiplexed analogue rate demands from the BLD electronic assembly and, once amplified, routes the demand to the corresponding one of the 40 motor drive sections on the board. The motor drive sections buffer the output to the motor and include IR compensation (motor current is sensed, and fed back positively into the motor drive.)

The clinical user should not notice any difference between the performance of this assembly and its predecessor, part number 4513390 4654. The service user will have access to the motor current data through software item part values, (see **[Ref: 1]**).

When a leaf is selected via the address lines, the multiplexers do not allow transmission of the analogue demand until the *MUX_EN* line is selected.

In this design, the *MUX_EN* signal is delayed by 20 µs and extended to 100 µs, which improves accuracy by allowing the analogue input to settle before the end of the *MUX_EN* pulse when old design BLD electronics are used.

3.5.4 BLD motor drive rack

The gantry-mounted BLD motor drive rack contains four backup diaphragm motor drive boards and a pair of boards for a BLD rotation. From digital accelerator serial number 5241 onwards, these PCBs are combined and one single UMD is used to drive the DROT as well as each diaphragm.

3.6 MLCi and MLCi2 mechanical subsystem

The mechanical aspects of the MLCi and MLCi2 are as follows:

- Leafbank assembly for collimation
- Backup diaphragms for collimation
- Full-width autowedge for wedged fields
- Accessory attachment.

The location of these subassemblies are shown in Section 2.4.

3.6.1 Leafbank assembly

This section describes the leafbank assembly for:

- MLCi (see Section 3.6.1.1)
- MLCi2 (see Section 3.6.1.2).

3.6.1.1 MLCi leafbank assembly

Summary

The MLCi leafbank assembly comprises two banks of 40 tungsten leaves which are mounted perpendicular to the direction of radiation and travel linearly across the beam path.

Each leaf is:

- Individually driven by a small motor.
- Separated from its neighbor by a small nominal gap to minimize friction.
- Slightly stepped on the vertical surfaces adjacent to the neighboring leaves to minimize the radiation leakage through the gap.
- Inclined on its vertical face to follow the divergence of the radiation beam. The leaves furthest from the central axis are more inclined.
- Curved on the end face to optimize the penumbra across the whole range of field sizes and offsets which can be achieved.

Correct positioning of the leaves is achieved through the video subsystem feeding positional data into the treatment control system (TCS). Any uncertainty regarding leaf position during treatment immediately puts the digital accelerator into the interrupt state.

Description

The MLCi leafbank assembly comprises two facing banks of tungsten alloy leaves (40 per bank) mounted perpendicularly to the radiation source, which can be adjusted to form a regular or irregular shape via the combined outline of their inner end surfaces. Each bank contains 38 leaves of identical section, plus two of slightly wider section to overlap the end shielding. Each leaf is controlled independently by a small, DC longlife motor and gearbox that drives the leaf in or out along a fine screw thread (lead screw). The leaf cannot back drive under gravity. Lead screw to gearbox connections are made with slotted couplings while the motors and gearboxes in each leafbank are mounted on a common bar for ease of replacement, either individually or as a set. Leaves of the same type can be interchanged, although this must be followed by a leakage check.