支持CXL的实现

当前论文

- 内存分解原型系统
  - Practical Memory Disaggregation using Compute Express Link
  - Direct Access, High-Performance Memory Disaggregation with DIRECTCXL
- CXL多级内存下页面迁移
  - TPP: Transparent Page Placement for CXL-Enabled Tiered Memory
- 内存分解全栈支持，完善软件栈
  - Pond: CXL-Based Memory Pooling Systems for Cloud Platforms
- SSD等块存储用于构建内存池
  - Performance Evaluation on CXL-enabled Hybrid Memory Pool
  - Hello bytes, bye blocks: PCIe storage meets compute express link for memory expansion (CXL-SSD)
- 除了内存分解/内存池外，利用CXL优化现有应用，包括：
  - CXL-PM和CXL-GPU训练DNN时检查点优化
    - Training Resilience with Persistent Memory Pooling using CXL Technology
  - 缓存一致性用于降低PM崩溃一致性开销
    - Cache-coherent accelerators for persistent memory crash consistency
  - 面向CXL-加速器的应用程序
    - Design and analysis of CXL performance models for tightly-coupled heterogeneous computing

学术界CXL实现与测试

- FPGA原型板

实现CXL控制器，内存控制器，switch，以及支持CXL的处理器架构

- NUMA节点模拟
- CXL性能模拟

基于CXL的行为，预计延迟

- 开源模拟器
  - CXLMemSim: A pure software simulated CXL.mem for performance characterization
  - https://github.com/zxhero/gem5-CXL
  - https://github.com/fadedzipper/gem5-cxl
  - https://github.com/luzhixing12345/gem5
  - https://github.com/ferry-hhh/gem5(有详细文档

主流产业界

- PMDK(Intel)

ndctl、daxctl用来管理Pmem和Namespace，cxl-cli用来管理CXL设备。

- Linux kernel
- Intel

The first CXL-capable processors are right around the corner, though: Intel's Sapphire Rapids and AMD's EPYC Genoa will come with early revisions of the specification built around the PCIe 5.0 interface.