Craig Scratchley's ARM0 instruction formats

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Load/Store Instructions (use memory)

LDRB – LoaD Register Byte

Syntax:
LDRB <Rd>, [<Rn> + #<offset2>]

RTL: Rd ← Memory[Rn + offset2]

7	6	5	4	3	2	1	0
MEM/nDP	L						
1	1	Rn		Rd		offset2	

STRB – STore Register Byte

Syntax:
STRB <Rd>, [<Rn> + #<offset2>]

RTL: Memory[Rn + offset2] ← Rd

7	6	5	4	3	2	1	0
MEM/nDP	L						
1	0	Rn		Rd		offset2	

Data Processing instructions (do not involve memory)

ADD – ADD

Syntax:
ADD <Rd>, <Rn>, <Rm>

RTL: Rd ← Rn + Rm

7	6	5	4	3	2	1	0
MEM/nDP	opcode1						
0	0	Rn		Rd		Rm	

MOV – MOVe

Syntax:
MOV <Rd>, <operand>

RTL: Rd ← operand

7	6	5	4	3	2	1	0
MEM/nDP	opcode1	NOT					
0	1	0	I	Rd		operand*	

MVN – MoVe Not

Syntax:
MVN <Rd>, <operand>

RTL: Rd ← NOT operand

7	6	5	4	3	2	1	0
MEM/nDP	opcode1	NOT					
0	1	1	I	Rd		operand*	

*operand can either be a 2-bit immediate referred to as immed_2 (I == 1) or source register Rm (I == 0). Note, immediate data is padded to the left with the bits "000000"

Examples:

MVN R0, #2 ;@ I == 1 **0**b011**1**0010
MVN R0, R2 ;@ I == 0 **0**b011**0**0010