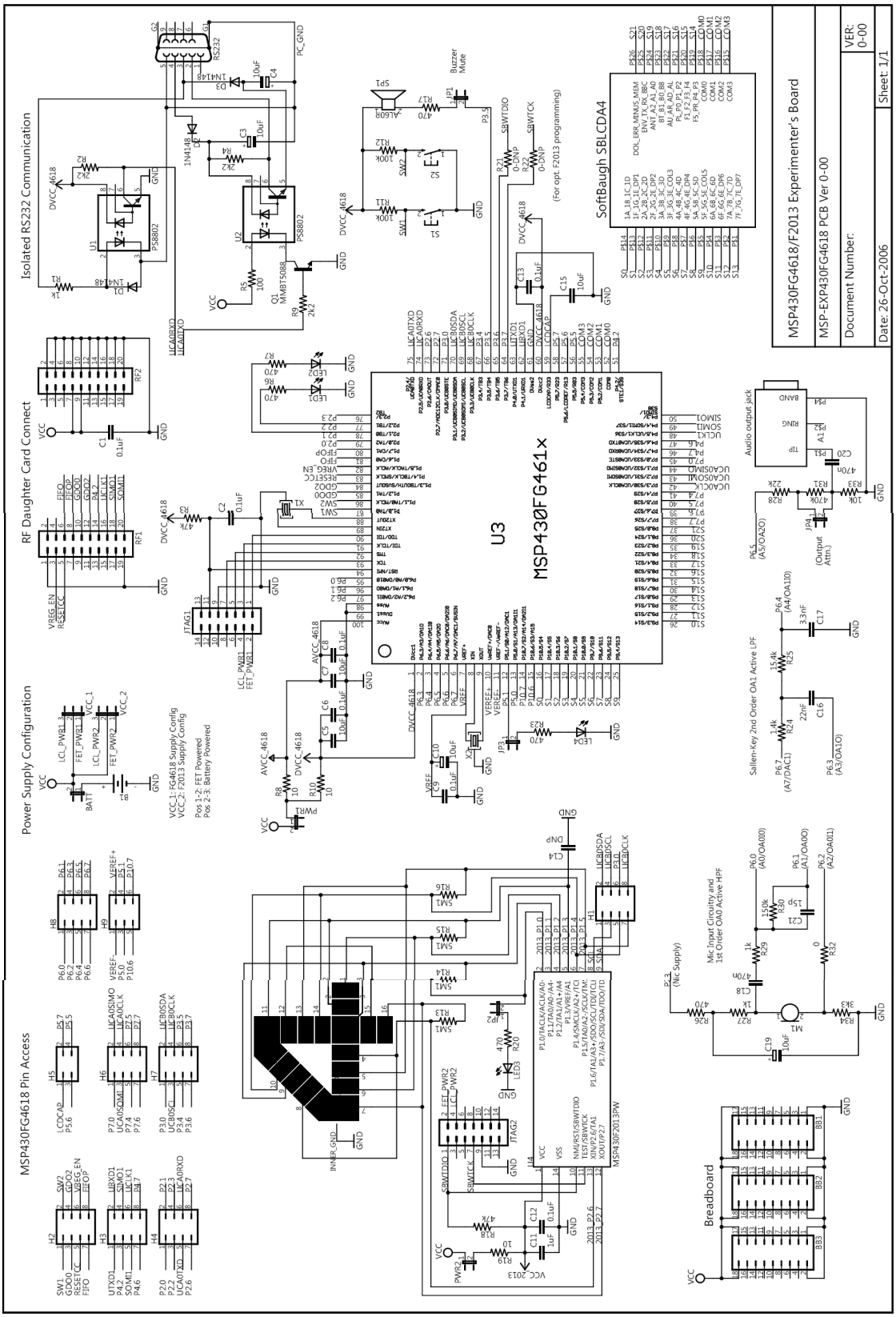
MSP430FG4618 Programming Reference

Revision 3

George Mason University

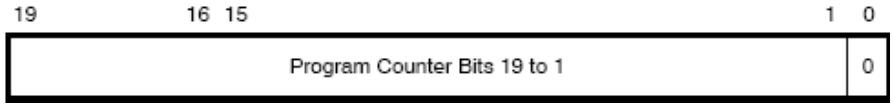
MSP430FG4618/F2013 Experimenter Board



1. CPU Registers

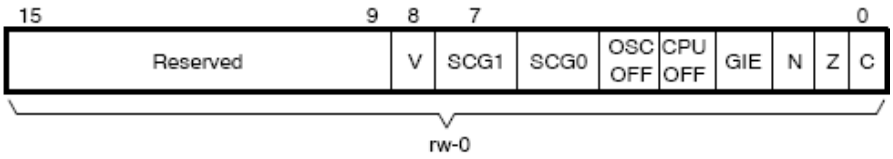
The CPU incorporates sixteen 20-bit registers. R0, R1, R2 and R3 have dedicated functions. R4 to R15 are working registers for general use.

PC, R0



SP, R1

SR, CG1, R2



CG2, R3

Six commonly-used constants are generated with the constant generator registers R2 and R3, without requiring an additional 16-bit word of program code. The constants are selected with the source-register addressing modes.

R4 - R15

R4 to R15, are general-purpose registers. All of these registers can be used as data registers, address pointers, or index values, and they can be accessed with byte or word instructions.

2. Interrupt Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY	VECTOR NAME
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1 and 5)	Reset	0FFFEh	31, highest	RESET_VECTOR
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1, 2, and 5)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	30	NMI_VECTOR
Timer_B7	TBCCR0 CCIFG0 (see Note 2)	Maskable	0FFFAh	29	TIMERB0_VECTOR
Timer_B7	TBCCR1 CCIFG1 ... TBCCR6 CCIFG6, TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	28	TIMERB1_VECTOR
Comparator_A	CAIFG	Maskable	0FFF6h	27	COMPARATORA_VECTOR
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26	WDT_VECTOR
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (see Note 1)	Maskable	0FFF2h	25	USCIAB0RX_VECTOR
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Note 1)	Maskable	0FFF0h	24	USCIAB0TX_VECTOR
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	23	ADC12_VECTOR
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECh	22	TIMERA0_VECTOR
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	21	TIMERA1_VECTOR
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	20	PORT1_VECTOR
USART1 Receive	URXIFG1	Maskable	0FFE6h	19	USART1RX_VECTOR
USART1 Transmit	UTXIFG1	Maskable	0FFE4h	18	USART1TX_VECTOR
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	17	PORT2_VECTOR
Basic Timer1/RTC	BTIFG	Maskable	0FFE0h	16	BASICTIMER_VECTOR
DMA	DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 and 2)	Maskable	0FFDEh	15	DMA_VECTOR
DAC12	DAC12.0IFG, DAC12.1IFG (see Notes 1 and 2)	Maskable	0FFDCh	14	DAC12_VECTOR
Reserved	Reserved (see Note 4)		0FFDAh	13	
			...	...	
			0FFC0h	0, lowest	

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module.
3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.
5. Access and key violations, KEYV and ACCVIFG, only applicable to F devices.

3. Instruction Set

Mnemonic		Description		V	N	Z	C
ADC(.B)†	dst	Add C to destination	dst + C → dst	*	*	*	*
ADD(.B)	src,dst	Add source to destination	src + dst → dst	*	*	*	*
ADDC(.B)	src,dst	Add source and C to destination	src + dst + C → dst	*	*	*	*
AND(.B)	src,dst	AND source and destination	src .and. dst → dst	0	*	*	*
BIC(.B)	src,dst	Clear bits in destination	.not.src .and. dst → dst	-	-	-	-
BIS(.B)	src,dst	Set bits in destination	src .or. dst → dst	-	-	-	-
BIT(.B)	src,dst	Test bits in destination	src .and. dst	0	*	*	*
BR†	dst	Branch to destination	dst → PC	-	-	-	-
CALL	dst	Call destination	PC+2 → stack, dst → PC	-	-	-	-
CLR(.B)†	dst	Clear destination	0 → dst	-	-	-	-
CLRC†		Clear C	0 → C	-	-	-	0
CLRN†		Clear N	0 → N	-	0	-	-
CLRZ†		Clear Z	0 → Z	-	-	0	-
CMP(.B)	src,dst	Compare source and destination	dst - src	*	*	*	*
DADC(.B)†	dst	Add C decimally to destination	dst + C → dst (decimally)	*	*	*	*
DADD(.B)	src,dst	Add source and C decimally to dst.	src + dst + C → dst (decimally)	*	*	*	*
DEC(.B)†	dst	Decrement destination	dst - 1 → dst	*	*	*	*
DECD(.B)†	dst	Double-decrement destination	dst - 2 → dst	*	*	*	*
DINT†		Disable interrupts	0 → GIE	-	-	-	-
EINT†		Enable interrupts	1 → GIE	-	-	-	-
INC(.B)†	dst	Increment destination	dst +1 → dst	*	*	*	*
INCD(.B)†	dst	Double-increment destination	dst+2 → dst	*	*	*	*
INV(.B)†	dst	Invert destination	.not.dst → dst	*	*	*	*
JC/JHS	label	Jump if C set/Jump if higher or same		-	-	-	-
JEQ/JZ	label	Jump if equal/Jump if Z set		-	-	-	-
JGE	label	Jump if greater or equal		-	-	-	-
JL	label	Jump if less		-	-	-	-
JMP	label	Jump	PC + 2 x offset → PC	-	-	-	-
JN	label	Jump if N set		-	-	-	-
JNC/JLO	label	Jump if C not set/Jump if lower		-	-	-	-
JNE/JNZ	label	Jump if not equal/Jump if Z not set		-	-	-	-
MOV(.B)	src,dst	Move source to destination	src → dst	-	-	-	-
NOP†		No operation		-	-	-	-
POP(.B)†	dst	Pop item from stack to destination	@SP → dst, SP+2 → SP	-	-	-	-
PUSH(.B)	src	Push source onto stack	SP - 2 → SP, src → @SP	-	-	-	-
RET†		Return from subroutine	@SP → PC, SP + 2 → SP	-	-	-	-
RETI		Return from interrupt		*	*	*	*
RLA(.B)†	dst	Rotate left arithmetically		*	*	*	*
RLC(.B)†	dst	Rotate left through C		*	*	*	*
RRA(.B)	dst	Rotate right arithmetically		0	*	*	*
RRC(.B)	dst	Rotate right through C		*	*	*	*
SBC(.B)†	dst	Subtract not(C) from destination	dst + 0FFFFh + C → dst	*	*	*	*
SETC†		Set C	1 → C	-	-	-	1
SETN†		Set N	1 → N	-	1	-	-
SETZ†		Set Z	1 → C	-	-	1	-
SUB(.B)	src,dst	Subtract source from destination	dst + .not.src + 1 → dst	*	*	*	*
SUBC(.B)	src,dst	Subtract source and not(C) from dst.	dst + .not.src + C → dst	*	*	*	*
SWPB	dst	Swap bytes		-	-	-	-
SXT	dst	Extend sign		0	*	*	*
TST(.B)†	dst	Test destination	dst + 0FFFFh + 1	0	*	*	1
XOR(.B)	src,dst	Exclusive OR source and destination	src .xor. dst → dst	*	*	*	*

4. Memory Mapped Registers Overview

Registers are grouped by module and may be repeated. Detailed breakouts for individual registers may be found in section 5.

4.1. FLL+ Clock Module Registers

Register	Short Form	Register Type	Address	Initial State
System clock control	SCFQCTL	Read/write	052h	01Fh with PUC
System clock frequency integrator 0	SCFI0	Read/write	050h	040h with PUC
System clock frequency integrator 1	SCFI1	Read/write	051h	Reset with PUC
FLL+ control register 0	FLL_CTL0	Read/write	053h	003h with PUC
FLL+ control register 1	FLL_CTL1	Read/write	054h	Reset with PUC
FLL+ control register 2†	FLL_CTL2	Read/write	055h	Reset with PUC
SFR interrupt enable register 1	IE1	Read/write	000h	Reset with PUC
SFR interrupt flag register 1	IFG1	Read/write	002h	Reset with PUC

† MSP430F41x2, MSP430F47x3/4, and MSP430F471xx devices only.

4.2. Flash Memory Controller

Register	Short Form	Register Type	Address	Initial State
Flash memory control register 1	FCTL1	Read/write	0128h	09600h with PUC
Flash memory control register 2	FCTL2	Read/write	012Ah	09642h with PUC
Flash memory control register 3	FCTL3	Read/write	012Ch	09618h† with PUC
Flash memory control register 4‡	FCTL4	Read/write	01BEh	0000h with PUC
Interrupt enable 1	IE1	Read/write	000h	Reset with PUC

† 09658h in MSP430FG47x, MSP430F47x, MSP430F47x3/4, and MSP430F471xx devices
‡ MSP430FG47x, MSP430F47x, MSP430F47x3/4, and MSP430F471xx devices only

4.3. Supply Voltage Supervisor

Register	Short Form	Register Type	Address	Initial State
SVS Control Register	SVSCTL	Read/write	056h	Reset with BOR

4.4. 16-Bit Hardware Multiplier

Register	Short Form	Register Type	Address	Initial State
Operand one - multiply	MPY	Read/write	0130h	Unchanged
Operand one - signed multiply	MPYS	Read/write	0132h	Unchanged
Operand one - multiply accumulate	MAC	Read/write	0134h	Unchanged
Operand one - signed multiply accumulate	MACS	Read/write	0136h	Unchanged
Operand two	OP2	Read/write	0138h	Unchanged
Result low word	RESLO	Read/write	013Ah	Undefined
Result high word	RESHI	Read/write	013Ch	Undefined
Sum Extension register	SUMEXT	Read	013Eh	Undefined

4.5. DMA Controller

Register	Short Form	Register Type	Address	Initial State
DMA control 0	DMACTL0	Read/write	0122h	Reset with POR
DMA control 1	DMACTL1	Read/write	0124h	Reset with POR
DMA interrupt vector	DMAIV	Read only	0126h	Reset with POR
DMA channel 0 control	DMA0CTL	Read/write	01D0h	Reset with POR
DMA channel 0 source address	DMA0SA	Read/write	01D2h	Unchanged
DMA channel 0 destination address	DMA0DA	Read/write	01D6h	Unchanged
DMA channel 0 transfer size	DMA0SZ	Read/write	01DAh	Unchanged
DMA channel 1 control	DMA1CTL	Read/write	01DCh	Reset with POR
DMA channel 1 source address	DMA1SA	Read/write	01DEh	Unchanged
DMA channel 1 destination address	DMA1DA	Read/write	01E2h	Unchanged
DMA channel 1 transfer size	DMA1SZ	Read/write	01E6h	Unchanged
DMA channel 2 control	DMA2CTL	Read/write	01E8h	Reset with POR
DMA channel 2 source address	DMA2SA	Read/write	01EAh	Unchanged
DMA channel 2 destination address	DMA2DA	Read/write	01EEh	Unchanged
DMA-channel 2 transfer size	DMA2SZ	Read/write	01F2h	Unchanged

4.6. Digital I/O

Port	Register	Short Form	Address	Register Type	Initial State
P1	Input	P1IN	020h	Read only	–
	Output	P1OUT	021h	Read/write	Unchanged
	Direction	P1DIR	022h	Read/write	Reset with PUC
	Interrupt Flag	P1IFG	023h	Read/write	Reset with PUC
	Interrupt Edge Select	P1IES	024h	Read/write	Unchanged
	Interrupt Enable	P1IE	025h	Read/write	Reset with PUC
	Port Select	P1SEL	026h	Read/write	Reset with PUC
	Resistor Enable	P1REN	027h	Read/write	Reset with PUC
P2	Input	P2IN	028h	Read only	–
	Output	P2OUT	029h	Read/write	Unchanged
	Direction	P2DIR	02Ah	Read/write	Reset with PUC
	Interrupt Flag	P2IFG	02Bh	Read/write	Reset with PUC
	Interrupt Edge Select	P2IES	02Ch	Read/write	Unchanged
	Interrupt Enable	P2IE	02Dh	Read/write	Reset with PUC
	Port Select	P2SEL	02Eh	Read/write	0C0h with PUC
	Resistor Enable	P2REN	02Fh	Read/write	Reset with PUC
P3	Input	P3IN	018h	Read only	–
	Output	P3OUT	019h	Read/write	Unchanged
	Direction	P3DIR	01Ah	Read/write	Reset with PUC
	Port Select	P3SEL	01Bh	Read/write	Reset with PUC
	Resistor Enable	P3REN	010h	Read/write	Reset with PUC
P4	Input	P4IN	01Ch	Read only	–
	Output	P4OUT	01Dh	Read/write	Unchanged
	Direction	P4DIR	01Eh	Read/write	Reset with PUC
	Port Select	P4SEL	01Fh	Read/write	Reset with PUC
	Resistor Enable	P4REN	011h	Read/write	Reset with PUC
P5	Input	P5IN	030h	Read only	–
	Output	P5OUT	031h	Read/write	Unchanged
	Direction	P5DIR	032h	Read/write	Reset with PUC
	Port Select	P5SEL	033h	Read/write	Reset with PUC
	Resistor Enable	P5REN	012h	Read/write	Reset with PUC
P6	Input	P6IN	034h	Read only	–
	Output	P6OUT	035h	Read/write	Unchanged
	Direction	P6DIR	036h	Read/write	Reset with PUC
	Port Select	P6SEL	037h	Read/write	Reset with PUC
	Resistor Enable	P6REN	013h	Read/write	Reset with PUC

Note: Resistor enable registers RxREN only available in MSP430x47x devices.

4.6. Digital I/O (continued)

Port	Register	Short Form	Address	Register Type	Initial State
P7 PA	Input	P7IN	038h	Read only	–
	Output	P7OUT	03Ah	Read/write	Unchanged
	Direction	P7DIR	03Ch	Read/write	Reset with PUC
	Port Select	P7SEL	03Eh	Read/write	Reset with PUC
	Resistor Enable	P7REN	014h	Read/write	Reset with PUC
P8	Input	P8IN	039h	Read only	–
	Output	P8OUT	03Bh	Read/write	Unchanged
	Direction	P8DIR	03Dh	Read/write	Reset with PUC
	Port Select	P8SEL	03Fh	Read/write	Reset with PUC
	Resistor Enable	P8REN	015h	Read/write	Reset with PUC
P9 PB	Input	P9IN	008h	Read only	–
	Output	P9OUT	00Ah	Read/write	Unchanged
	Direction	P9DIR	00Ch	Read/write	Reset with PUC
	Port Select	P9SEL	00Eh	Read/write	Reset with PUC
	Resistor Enable	P9REN	016h	Read/write	Reset with PUC
P10	Input	P10IN	009h	Read only	–
	Output	P10OUT	00Bh	Read/write	Unchanged
	Direction	P10DIR	00Dh	Read/write	Reset with PUC
	Port Select	P10SEL	00Fh	Read/write	Reset with PUC
	Resistor Enable	P10REN	017h	Read/write	Reset with PUC

Note: Resistor enable registers RxREN only available in MSP430x47x devices.

4.7. Watchdog Timer+

Register	Short Form	Register Type	Address	Initial State
Watchdog timer control register	WDTCTL	Read/write	0120h	06900h with PUC
SFR interrupt enable register 1	IE1	Read/write	0000h	Reset with PUC
SFR interrupt flag register 1	IFG1	Read/write	0002h	Reset with PUC†

† WDTIFG is reset with POR

4.8. Basic Timer1

Register	Short Form	Register Type	Address	Initial State
Basic Timer1 Control	BTCTL	Read/write	040h	Unchanged
Basic Timer1 Counter 1	BTCNT1	Read/write	046h	Unchanged
Basic Timer1 Counter 2	BTCNT2	Read/write	047h	Unchanged
SFR interrupt enable register 2	IE2	Read/write	001h	Reset with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	Reset with PUC

Note: The Basic Timer1 registers should be configured at power-up. There is no initial state for BTCTL, BTCNT1, or BTCNT2.

4.9. Real Time Clock

Register	Short Form	Register Type	Address	Initial State
Real-Time Clock control register	RTCCTL	Read/write	041h	040h with POR
Real-Timer Clock second Real-Timer Counter register 1	RTCSEC/ RTCNT1	Read/write	042h	Unchanged
Real-Time Clock minute Real-Time Counter register 2	RTCMIN/ RTCNT2	Read/write	043h	Unchanged
Real-Time Clock hour Real-Time Counter register 3	RTCHOUR/ RTCNT3	Read/write	044h	Unchanged
Real-Time Clock day-of-Week Real-Time Counter register 4	RTCDOW/ RTCNT4	Read/write	045h	Unchanged
Real-Time Clock day-of-month	RTCDAY	Read/write	04Ch	Unchanged
Real-Time Clock month	RTCMON	Read/write	04Dh	Unchanged
Real-Time Clock year (low byte)	RTCYEARL	Read/write	04Eh	Unchanged
Real-Time Clock year (high byte)	RTCYEARH	Read/write	04Fh	Unchanged
SFR interrupt enable register 2	IE2	Read/write	001h	Reset with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	Reset with PUC

4.10. Timer_A

Register	Short Form	Register Type	Address	Initial State
Timer_A control Timer0_A3 Control	TACTL/ TA0CTL	Read/write	0160h	Reset with POR
Timer_A counter Timer0_A3 counter	TAR/ TA0R	Read/write	0170h	Reset with POR
Timer_A capture/compare control 0 Timer0_A3 capture/compare control 0	TACCTL0/ TA0CCTL	Read/write	0162h	Reset with POR
Timer_A capture/compare 0 Timer0_A3 capture/compare 0	TACCR0/ TA0CCR0	Read/write	0172h	Reset with POR
Timer_A capture/compare control 1 Timer0_A3 capture/compare control 1	TACCTL1/ TA0CCTL1	Read/write	0164h	Reset with POR
Timer_A capture/compare 1 Timer0_A3 capture/compare 1	TACCR1/ TA0CCR1	Read/write	0174h	Reset with POR
Timer_A capture/compare control 2 Timer0_A3 capture/compare control 2	TACCTL2/ TA0CCTL2	Read/write	0166h	Reset with POR
Timer_A capture/compare 2 Timer0_A3 capture/compare 2	TACCR2/ TA0CCR2	Read/write	0176h	Reset with POR
Timer_A interrupt vector Timer0_A3 interrupt vector	TAIV/ TA0IV	Read only	012Eh	Reset with POR

4.11. Timer_B

Register	Short Form	Register Type	Address	Initial State
Timer_B control	TBCTL	Read/write	0180h	Reset with POR
Timer_B counter	TBR	Read/write	0190h	Reset with POR
Timer_B capture/compare control 0	TBCCTL0	Read/write	0182h	Reset with POR
Timer_B capture/compare 0	TBCCR0	Read/write	0192h	Reset with POR
Timer_B capture/compare control 1	TBCCTL1	Read/write	0184h	Reset with POR
Timer_B capture/compare 1	TBCCR1	Read/write	0194h	Reset with POR
Timer_B capture/compare control 2	TBCCTL2	Read/write	0186h	Reset with POR
Timer_B capture/compare 2	TBCCR2	Read/write	0196h	Reset with POR
Timer_B capture/compare control 3	TBCCTL3	Read/write	0188h	Reset with POR
Timer_B capture/compare 3	TBCCR3	Read/write	0198h	Reset with POR
Timer_B capture/compare control 4	TBCCTL4	Read/write	018Ah	Reset with POR
Timer_B capture/compare 4	TBCCR4	Read/write	019Ah	Reset with POR
Timer_B capture/compare control 5	TBCCTL5	Read/write	018Ch	Reset with POR
Timer_B capture/compare 5	TBCCR5	Read/write	019Ch	Reset with POR
Timer_B capture/compare control 6	TBCCTL6	Read/write	018Eh	Reset with POR
Timer_B capture/compare 6	TBCCR6	Read/write	019Eh	Reset with POR
Timer_B Interrupt Vector	TBIV	Read only	011Eh	Reset with POR

4.12. USART Peripheral Interface: UART Mode

Register	Short Form	Register Type	Address	Initial State
USART control register	U1CTL	Read/write	078h	001h with PUC
Transmit control register	U1TCTL	Read/write	079h	001h with PUC
Receive control register	U1RCTL	Read/write	07Ah	000h with PUC
Modulation control register	U1MCTL	Read/write	07Bh	Unchanged
Baud rate control register 0	U1BR0	Read/write	07Ch	Unchanged
Baud rate control register 1	U1BR1	Read/write	07Dh	Unchanged
Receive buffer register	U1RXBUF	Read	07Eh	Unchanged
Transmit buffer register	U1TXBUF	Read/write	07Fh	Unchanged
SFR module enable register 2	ME2	Read/write	005h	000h with PUC
SFR interrupt enable register 2	IE2	Read/write	001h	000h with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	020h with PUC

4.13. USART Peripheral Interface: SPI Mode

Register	Short Form	Register Type	Address	Initial State
USART control register	U1CTL	Read/write	078h	001h with PUC
Transmit control register	U1TCTL	Read/write	079h	001h with PUC
Receive control register	U1RCTL	Read/write	07Ah	000h with PUC
Modulation control register	U1MCTL	Read/write	07Bh	Unchanged
Baud rate control register 0	U1BR0	Read/write	07Ch	Unchanged
Baud rate control register 1	U1BR1	Read/write	07Dh	Unchanged
Receive buffer register	U1RXBUF	Read	07Eh	Unchanged
Transmit buffer register	U1TXBUF	Read/write	07Fh	Unchanged
SFR module enable register 2	ME2	Read/write	005h	000h with PUC
SFR interrupt enable register 2	IE2	Read/write	001h	000h with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	020h with PUC

4.14. Universal Serial Communication Interface: UART Mode

Register	Short Form	Register Type	Address	Initial State
USCI_A0 control register 0	UCA0CTL0	Read/write	060h	Reset with PUC
USCI_A0 control register 1	UCA0CTL1	Read/write	061h	001h with PUC
USCI_A0 Baud rate control register 0	UCA0BR0	Read/write	062h	Reset with PUC
USCI_A0 Baud rate control register 1	UCA0BR1	Read/write	063h	Reset with PUC
USCI_A0 modulation control register	UCA0MCTL	Read/write	064h	Reset with PUC
USCI_A0 status register	UCA0STAT	Read/write	065h	Reset with PUC
USCI_A0 Receive buffer register	UCA0RXBUF	Read	066h	Reset with PUC
USCI_A0 Transmit buffer register	UCA0TXBUF	Read/write	067h	Reset with PUC
USCI_A0 Auto Baud control register	UCA0ABCTL	Read/write	05Dh	Reset with PUC
USCI_A0 IrDA Transmit control register	UCA0IRTCTL	Read/write	05Eh	Reset with PUC
USCI_A0 IrDA Receive control register	UCA0IRRCTL	Read/write	05Fh	Reset with PUC
SFR interrupt enable register 2	IE2	Read/write	001h	Reset with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	00Ah with PUC

4.15. Universal Serial Communication Interface: SPI Mode

Register	Short Form	Register Type	Address	Initial State
USCI_A0 control register 0	UCA0CTL0	Read/write	060h	Reset with PUC
USCI_A0 control register 1	UCA0CTL1	Read/write	061h	001h with PUC
USCI_A0 Baud rate control register 0	UCA0BR0	Read/write	062h	Reset with PUC
USCI_A0 Baud rate control register 1	UCA0BR1	Read/write	063h	Reset with PUC
USCI_A0 modulation control register	UCA0MCTL	Read/write	064h	Reset with PUC
USCI_A0 status register	UCA0STAT	Read/write	065h	Reset with PUC
USCI_A0 Receive buffer register	UCA0RXBUF	Read	066h	Reset with PUC
USCI_A0 Transmit buffer register	UCA0TXBUF	Read/write	067h	Reset with PUC
USCI_B0 control register 0	UCB0CTL0	Read/write	068h	001h with PUC
USCI_B0 control register 1	UCB0CTL1	Read/write	069h	001h with PUC
USCI_B0 Bit rate control register 0	UCB0BR0	Read/write	06Ah	Reset with PUC
USCI_B0 Bit rate control register 1	UCB0BR1	Read/write	06Bh	Reset with PUC
USCI_B0 status register	UCB0STAT	Read/write	06Dh	Reset with PUC
USCI_B0 Receive buffer register	UCB0RXBUF	Read	06Eh	Reset with PUC
USCI_B0 Transmit buffer register	UCB0TXBUF	Read/write	06Fh	Reset with PUC
SFR interrupt enable register 2	IE2	Read/write	001h	Reset with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	00Ah with PUC

4.16. Universal Serial Communication Interface: I2C Mode

Register	Short Form	Register Type	Address	Initial State
USCI_B0 control register 0	UCB0CTL0	Read/write	068h	001h with PUC
USCI_B0 control register 1	UCB0CTL1	Read/write	069h	001h with PUC
USCI_B0 bit rate control register 0	UCB0BR0	Read/write	06Ah	Reset with PUC
USCI_B0 bit rate control register 1	UCB0BR1	Read/write	06Bh	Reset with PUC
USCI_B0 I^2C interrupt enable register	UCB0I2CIE	Read/write	06Ch	Reset with PUC
USCI_B0 status register	UCB0STAT	Read/write	06Dh	Reset with PUC
USCI_B0 receive buffer register	UCB0RXBUF	Read	06Eh	Reset with PUC
USCI_B0 transmit buffer register	UCB0TXBUF	Read/write	06Fh	Reset with PUC
USCI_B0 I2C own address register	UCB0I2COA	Read/write	0118h	Reset with PUC
USCI_B0 I2C slave address register	UCB0I2CSA	Read/write	011Ah	Reset with PUC
SFR interrupt enable register 2	IE2	Read/write	001h	Reset with PUC
SFR interrupt flag register 2	IFG2	Read/write	003h	00Ah with PUC

4.17. Operational Amplifier

Register	Short Form	Register Type	Address	Initial State
OA0 control register 0	OA0CTL0	Read/write	0C0h	Reset with PUC
OA0 control register 1	OA0CTL1	Read/write	0C1h	Reset with PUC
OA1 control register 0	OA1CTL0	Read/write	0C2h	Reset with PUC
OA1 control register 1	OA1CTL1	Read/write	0C3h	Reset with PUC
OA2 control register 0	OA2CTL0	Read/write	0C4h	Reset with PUC
OA2 control register 1	OA2CTL1	Read/write	0C5h	Reset with PUC

4.18. Comparator_A

Register	Short Form	Register Type	Address	Initial State
Comparator_A control register 1	CACTL1	Read/write	059h	Reset with POR
Comparator_A control register 2	CACTL2	Read/write	05Ah	Reset with POR
Comparator_A port disable	CAPD	Read/write	05Bh	Reset with POR

4.19. LCD_A Controller

Register	Short Form	Register Type	Address	Initial State
LCD_A control register	LCDACTL	Read/write	090h	Reset with PUC
LCD memory 1	LCDM1	Read/write	091h	Unchanged
LCD memory 2	LCDM2	Read/write	092h	Unchanged
LCD memory 3	LCDM3	Read/write	093h	Unchanged
LCD memory 4	LCDM4	Read/write	094h	Unchanged
LCD memory 5	LCDM5	Read/write	095h	Unchanged
LCD memory 6	LCDM6	Read/write	096h	Unchanged
LCD memory 7	LCDM7	Read/write	097h	Unchanged
LCD memory 8	LCDM8	Read/write	098h	Unchanged
LCD memory 9	LCDM9	Read/write	099h	Unchanged
LCD memory 10	LCDM10	Read/write	09Ah	Unchanged
LCD memory 11	LCDM11	Read/write	09Bh	Unchanged
LCD memory 12	LCDM12	Read/write	09Ch	Unchanged
LCD memory 13	LCDM13	Read/write	09Dh	Unchanged
LCD memory 14	LCDM14	Read/write	09Eh	Unchanged
LCD memory 15	LCDM15	Read/write	09Fh	Unchanged
LCD memory 16	LCDM16	Read/write	0A0h	Unchanged
LCD memory 17	LCDM17	Read/write	0A1h	Unchanged
LCD memory 18	LCDM18	Read/write	0A2h	Unchanged
LCD memory 19	LCDM19	Read/write	0A3h	Unchanged
LCD memory 20	LCDM20	Read/write	0A4h	Unchanged
LCD_A port control 0	LCDAPCTL0	Read/write	0ACh	Reset with PUC
LCD_A port control 1	LCDAPCTL1	Read/write	0ADh	Reset with PUC
LCD_A voltage control 0	LCDAVCTL0	Read/write	0AEh	Reset with PUC
LCD_A voltage control 1	LCDAVCTL1	Read/write	0AFh	Reset with PUC

4.20. ADC12

Register	Short Form	Register Type	Address	Initial State
ADC12 control register 0	ADC12CTL0	Read/write	01A0h	Reset with POR
ADC12 control register 1	ADC12CTL1	Read/write	01A2h	Reset with POR
ADC12 interrupt flag register	ADC12IFG	Read/write	01A4h	Reset with POR
ADC12 interrupt enable register	ADC12IE	Read/write	01A6h	Reset with POR
ADC12 interrupt vector word	ADC12IV	Read	01A8h	Reset with POR
ADC12 memory 0	ADC12MEM0	Read/write	0140h	Unchanged
ADC12 memory 1	ADC12MEM1	Read/write	0142h	Unchanged
ADC12 memory 2	ADC12MEM2	Read/write	0144h	Unchanged
ADC12 memory 3	ADC12MEM3	Read/write	0146h	Unchanged
ADC12 memory 4	ADC12MEM4	Read/write	0148h	Unchanged
ADC12 memory 5	ADC12MEM5	Read/write	014Ah	Unchanged
ADC12 memory 6	ADC12MEM6	Read/write	014Ch	Unchanged
ADC12 memory 7	ADC12MEM7	Read/write	014Eh	Unchanged
ADC12 memory 8	ADC12MEM8	Read/write	0150h	Unchanged
ADC12 memory 9	ADC12MEM9	Read/write	0152h	Unchanged
ADC12 memory 10	ADC12MEM10	Read/write	0154h	Unchanged
ADC12 memory 11	ADC12MEM11	Read/write	0156h	Unchanged
ADC12 memory 12	ADC12MEM12	Read/write	0158h	Unchanged
ADC12 memory 13	ADC12MEM13	Read/write	015Ah	Unchanged
ADC12 memory 14	ADC12MEM14	Read/write	015Ch	Unchanged
ADC12 memory 15	ADC12MEM15	Read/write	015Eh	Unchanged
ADC12 memory control 0	ADC12MCTL0	Read/write	080h	Reset with POR
ADC12 memory control 1	ADC12MCTL1	Read/write	081h	Reset with POR
ADC12 memory control 2	ADC12MCTL2	Read/write	082h	Reset with POR
ADC12 memory control 3	ADC12MCTL3	Read/write	083h	Reset with POR
ADC12 memory control 4	ADC12MCTL4	Read/write	084h	Reset with POR
ADC12 memory control 5	ADC12MCTL5	Read/write	085h	Reset with POR
ADC12 memory control 6	ADC12MCTL6	Read/write	086h	Reset with POR
ADC12 memory control 7	ADC12MCTL7	Read/write	087h	Reset with POR
ADC12 memory control 8	ADC12MCTL8	Read/write	088h	Reset with POR
ADC12 memory control 9	ADC12MCTL9	Read/write	089h	Reset with POR
ADC12 memory control 10	ADC12MCTL10	Read/write	08Ah	Reset with POR
ADC12 memory control 11	ADC12MCTL11	Read/write	08Bh	Reset with POR
ADC12 memory control 12	ADC12MCTL12	Read/write	08Ch	Reset with POR
ADC12 memory control 13	ADC12MCTL13	Read/write	08Dh	Reset with POR
ADC12 memory control 14	ADC12MCTL14	Read/write	08Eh	Reset with POR
ADC12 memory control 15	ADC12MCTL15	Read/write	08Fh	Reset with POR

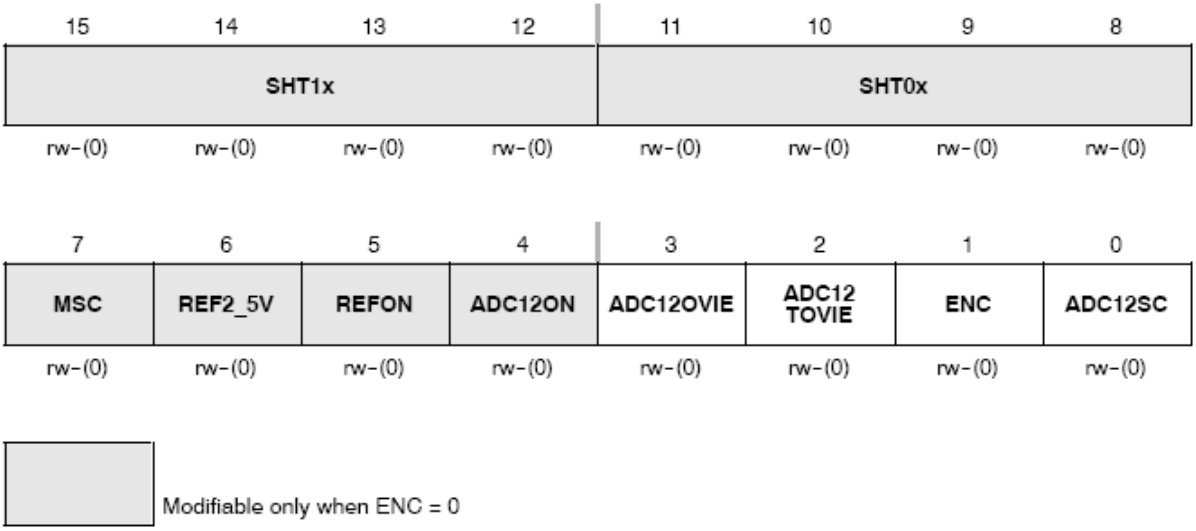
4.21. DAC12

Register	Short Form	Register Type	Address	Initial State
DAC12_0 control	DAC12_0CTL	Read/write	01C0h	Reset with POR
DAC12_0 data	DAC12_0DAT	Read/write	01C8h	Reset with POR
DAC12_1 control	DAC12_1CTL	Read/write	01C2h	Reset with POR
DAC12_1 data	DAC12_1DAT	Read/write	01CAh	Reset with POR

5. Memory Mapped Registers Detail

Registers are ordered alphabetically.

ADC12CTL0, ADC12 Control Register 0



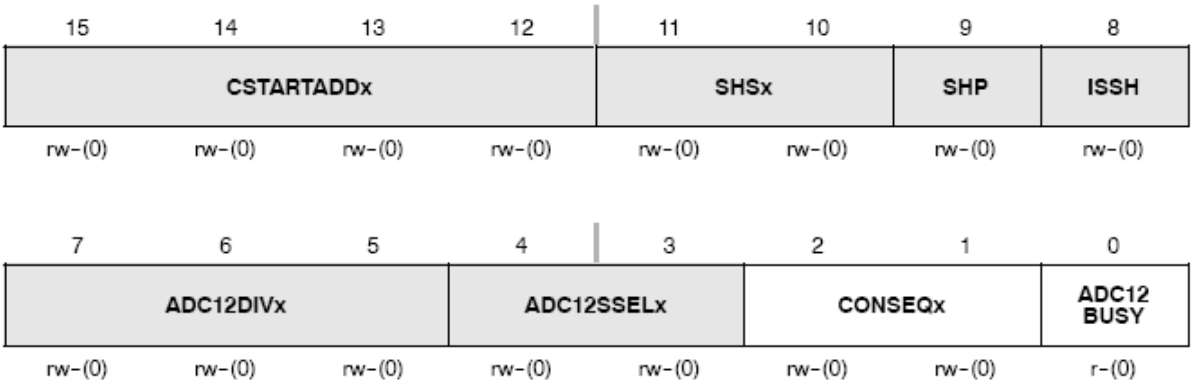
SHT1x Bits 15-12 Sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM8 to ADC12MEM15.

SHT0x Bits 11-8 Sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM0 to ADC12MEM7.

SHTx Bits	ADC12CLK cycles
0000	4
0001	8
0010	16
0011	32
0100	64
0101	96
0110	128
0111	192
1000	256
1001	384
1010	512
1011	768
1100	1024
1101	1024
1110	1024
1111	1024

MSC	Bit 7	Multiple sample and conversion. Valid only for sequence or repeated modes. 0 The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-conversion. 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.
REF2_5V	Bit 6	Reference generator voltage. REFON must also be set. 0 1.5 V 1 2.5 V
REFON	Bit 5	Reference generator on 0 Reference off 1 Reference on
ADC12ON	Bit 4	ADC12 on 0 ADC12 off 1 ADC12 on
ADC12OVIE	Bit 3	ADC12MEMx overflow-interrupt enable. The GIE bit must also be set to enable the interrupt. 0 Overflow interrupt disabled 1 Overflow interrupt enabled
ADC12 TOVIE	Bit 2	ADC12 conversion-time-overflow interrupt enable. The GIE bit must also be set to enable the interrupt. 0 Conversion time overflow interrupt disabled 1 Conversion time overflow interrupt enabled
ENC	Bit 1	Enable conversion 0 ADC12 disabled 1 ADC12 enabled
ADC12SC	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC12SC and ENC may be set together with one instruction. ADC12SC is reset automatically. 0 No sample-and-conversion-start 1 Start sample-and-conversion

ADC12CTL1, ADC12 Control Register 1



Modifiable only when ENC = 0

CSTART ADDx	Bits 15-12	Conversion start address. These bits select which ADC12 conversion-memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15.
SHSx	Bits 11-10	Sample-and-hold source select 00 ADC12SC bit 01 Timer_A.OUT1 10 Timer_B.OUT0 11 Timer_B.OUT1
SHP	Bit 9	Sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly. 0 SAMPCON signal is sourced from the sample-input signal. 1 SAMPCON signal is sourced from the sampling timer.
ISSH	Bit 8	Invert signal sample-and-hold 0 The sample-input signal is not inverted. 1 The sample-input signal is inverted.
ADC12DIVx	Bits 7-5	ADC12 clock divider 000 /1 001 /2 010 /3 011 /4 100 /5 101 /6 110 /7 111 /8

ADC12 SSELx	Bits 4-3	ADC12 clock source select 00 ADC12OSC 01 ACLK 10 MCLK 11 SMCLK
CONSEQx	Bits 2-1	Conversion sequence mode select 00 Single-channel, single-conversion 01 Sequence-of-channels 10 Repeat-single-channel 11 Repeat-sequence-of-channels
ADC12 BUSY	Bit 0	ADC12 busy. This bit indicates an active sample or conversion operation. 0 No operation is active. 1 A sequence, sample, or conversion is active.

ADC12IE, ADC12 Interrupt Enable Register

15	14	13	12	11	10	9	8
ADC12IE15	**ADC12IE14**	**ADC12IE13**	**ADC12IE12**	**ADC12IE11**	**ADC12IE10**	**ADC12IE9**	**ADC12IE8**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
ADC12IE7	**ADC12IE6**	**ADC12IE5**	**ADC12IE4**	**ADC12IE3**	**ADC12IE2**	**ADC12IE1**	**ADC12IE0**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

ADC12IEx	Bits 15-0	Interrupt enable. These bits enable or disable the interrupt request for the ADC12IFGx bits. 0 Interrupt disabled 1 Interrupt enabled

ADC12IFG, ADC12 Interrupt Flag Register

15	14	13	12	11	10	9	8
ADC12 IFG15	ADC12 IFG14	ADC12 IFG13	ADC12 IFG12	ADC12 IFG11	ADC12 IFG10	ADC12 IFG9	ADC12 IFG8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
ADC12 IFG7	ADC12 IFG6	ADC12 IFG5	ADC12 IFG4	ADC12 IFG3	ADC12 IFG2	ADC12 IFG1	ADC12 IFG0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

ADC12IFGx Bits 15-0 ADC12MEMx Interrupt flag. These bits are set when corresponding ADC12MEMx is loaded with a conversion result. The ADC12IFGx bits are reset if the corresponding ADC12MEMx is accessed, or may be reset with software.

0 No interrupt pending
1 Interrupt pending

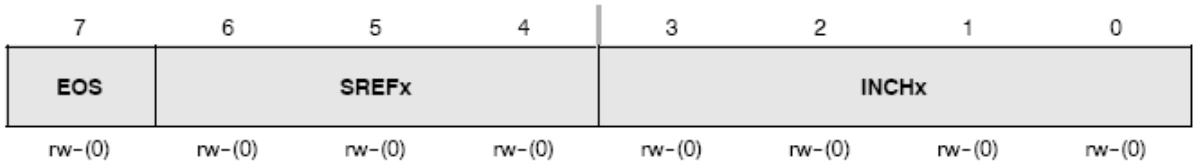
ADC12IV, ADC12 Interrupt Vector Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	0	ADC12IVx					0
r0	r0	r-(0)	r-(0)	r-(0)	r-(0)	r-(0)	r0

ADC12IVx Bits 15-0 ADC12 interrupt vector value

ADC12MCTLx, ADC12 Conversion Memory Control Registers



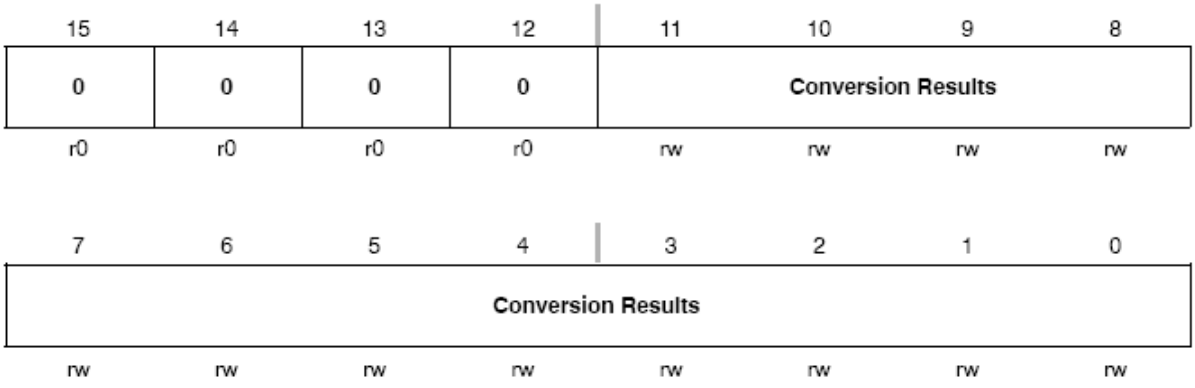
Modifiable only when ENC = 0

EOS Bit 7 End of sequence. Indicates the last conversion in a sequence.
- 0 Not end of sequence
- 1 End of sequence

SREFx Bits 6-4 Select reference
- 000 $V_{R+} = AV_{CC}$ and $V_{R-} = AV_{SS}$
- 001 $V_{R+} = V_{REF+}$ and $V_{R-} = AV_{SS}$
- 010 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$
- 011 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$
- 100 $V_{R+} = AV_{CC}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 101 $V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 110 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 111 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$

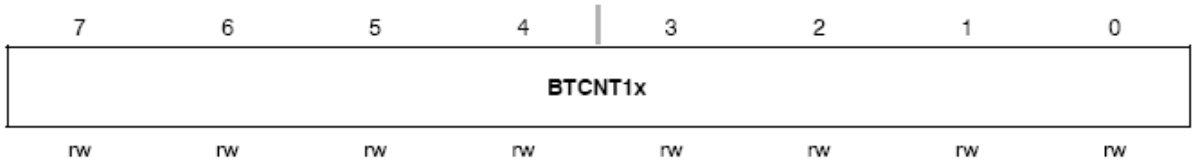
INCHx Bits 3-0 Input channel select
- 0000 A0
- 0001 A1
- 0010 A2
- 0011 A3
- 0100 A4
- 0101 A5
- 0110 A6
- 0111 A7
- 1000 Ve_{REF+}
- 1001 V_{REF-}/Ve_{REF-}
- 1010 Temperature sensor
- 1011 $(AV_{CC} – AV_{SS}) / 2$
- 1100 $(AV_{CC} – AV_{SS}) / 2$, A12 on 'FG43x and 'FG461x devices
- 1101 $(AV_{CC} – AV_{SS}) / 2$, A13 on 'FG43x and 'FG461x devices
- 1110 $(AV_{CC} – AV_{SS}) / 2$, A14 on 'FG43x and 'FG461x devices
- 1111 $(AV_{CC} – AV_{SS}) / 2$, A15 on 'FG43x and 'FG461x devices

ADC12MEMx, ADC12 Conversion Memory Registers



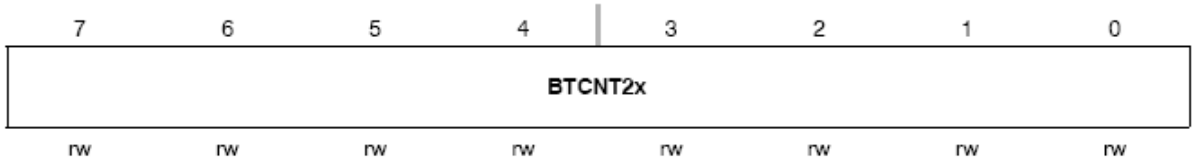
Conversion Results	Bits 15-0	The 12-bit conversion results are right-justified. Bit 11 is the MSB. Bits 15-12 are always 0. Writing to the conversion memory registers will corrupt the results.

BTCNT1, Basic Timer1 Counter 1



BTCNT1x	Bits 7-0	BTCNT1 register. The BTCNT1 register is the count of BTCNT1.

BTCNT2, Basic Timer1 Counter 2



BTCNT2x	Bits 7-0	BTCNT2 register. The BTCNT2 register is the count of BTCNT2.

BTCTL, Basic Timer1 Control Register

7	6	5	4	3	2	1	0
BTSSEL	BTHOLD	BTDIV	BTFRFQx		BTIPx		
rw	rw	rw	rw	rw	rw	rw	rw

BTSSEL Bit 7 BTCNT2 clock select. This bit, together with the BTDIV bit, selects the clock source for BTCNT2. See the description for BTDIV.

BTHOLD Bit 6 Basic Timer1 hold
0 BTCNT1 and BTCNT2 are operational
1 BTCNT1 is held if BTDIV=1
BTCNT2 is held

BTDIV Bit 5 Basic Timer1 clock divide. This bit together with the BTSSEL bit, selects the clock source for BTCNT2.

BTSSEL	BTDIV	BTCNT2 Clock Source
0	0	ACLK
0	1	ACLK/256
1	0	SMCLK
1	1	ACLK/256

BTFRFQx Bits 4–3 f_{LCD} frequency. These bits control the LCD update frequency.
00 $f_{ACLK}/32$
01 $f_{ACLK}/64$
10 $f_{ACLK}/128$
11 $f_{ACLK}/256$

BTIPx Bits 2–0 Basic Timer1 interrupt interval
000 $f_{CLK2}/2$
001 $f_{CLK2}/4$
010 $f_{CLK2}/8$
011 $f_{CLK2}/16$
100 $f_{CLK2}/32$
101 $f_{CLK2}/64$
110 $f_{CLK2}/128$
111 $f_{CLK2}/256$

CACTL1, Comparator_A Control Register 1

7	6	5	4	3	2	1	0
CAEX	CARSEL	CAREFx		CAON	CAIES	CAIE	CAIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

CAEX Bit 7 Comparator_A exchange. This bit exchanges the comparator inputs and inverts the comparator output.

CARSEL Bit 6 Comparator_A reference select. This bit selects which terminal the V_{CAREF} is applied to.
When CAEX = 0:
0 V_{CAREF} is applied to the + terminal
1 V_{CAREF} is applied to the – terminal
When CAEX = 1:
0 V_{CAREF} is applied to the – terminal
1 V_{CAREF} is applied to the + terminal

CAREF Bits 5-4 Comparator_A reference. These bits select the reference voltage V_{CAREF}.
00 Internal reference off. An external reference can be applied.
01 $0.25*V_{CC}$
10 $0.50*V_{CC}$
11 Diode reference is selected

CAON Bit 3 Comparator_A on. This bit turns on the comparator. When the comparator is off it consumes no current. The reference circuitry is enabled or disabled independently.
0 Off
1 On

CAIES Bit 2 Comparator_A interrupt edge select
0 Rising edge
1 Falling edge

CAIE Bit 1 Comparator_A interrupt enable
0 Disabled
1 Enabled

CAIFG Bit 0 The Comparator_A interrupt flag
0 No interrupt pending
1 Interrupt pending

CACTL2, Comparator_A Control Register 2

7	6	5	4	3	2	1	0
Unused				P2CA1	P2CA0	CAF	CAOUT
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

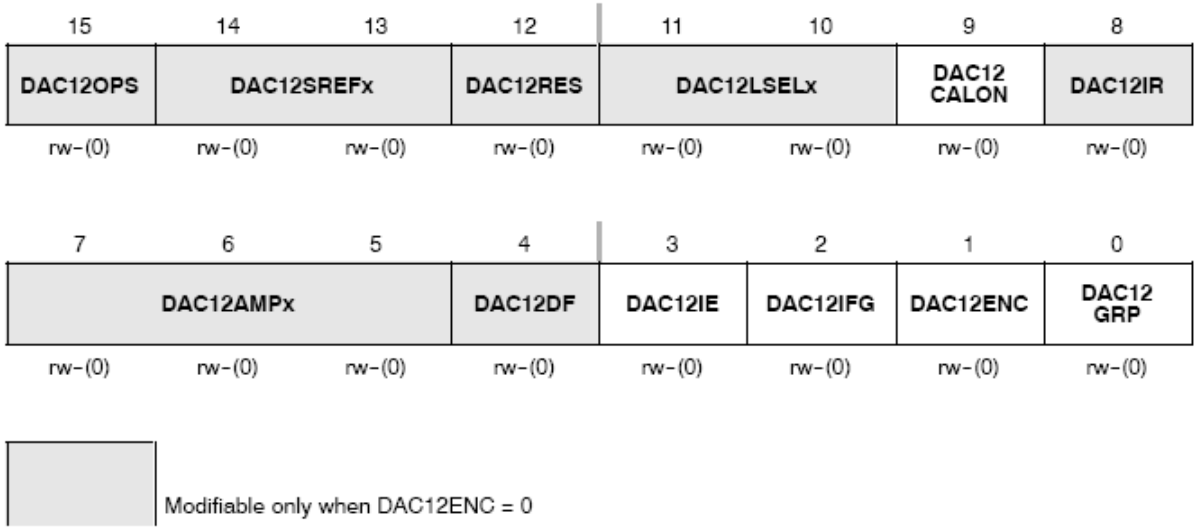
Unused	Bits 7-4	Unused.
P2CA1	Bit 3	Pin to CA1. This bit selects the CA1 pin function. 0 The pin is not connected to CA1 1 The pin is connected to CA1
P2CA0	Bit 2	Pin to CA0. This bit selects the CA0 pin function. 0 The pin is not connected to CA0 1 The pin is connected to CA0
CAF	Bit 1	Comparator_A output filter 0 Comparator_A output is not filtered 1 Comparator_A output is filtered
CAOUT	Bit 0	Comparator_A output. This bit reflects the value of the comparator output. Writing this bit has no effect.

CAPD, Comparator_A Port Disable Register

7	6	5	4	3	2	1	0
CAPD7	CAPD6	CAPD5	CAPD4	CAPD3	CAPD2	CAPD1	CAPD0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

CAPDx	Bits 7-0	Comparator_A port disable. These bits individually disable the input buffer for the pins of the port associated with Comparator_A. For example, the CAPDx bits can be used to individually enable or disable each P1.x pin buffer. CAPD0 disables P1.0, CAPD1 disables P1.1, etc. 0 The input buffer is enabled. 1 The input buffer is disabled.

DAC12_xCTL, DAC12 Control Register



15	14	13	12	11	10	9	8
DAC12OPS	DAC12SREFx		DAC12RES	DAC12LSELx		DAC12 CALON	DAC12IR
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
DAC12AMPx			DAC12DF	DAC12IE	DAC12IFG	DAC12ENC	DAC12 GRP
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Modifiable only when DAC12ENC = 0

DAC12OPS Bit 15 DAC12 output select
MSP430FG43x and MSP430FG461x Devices:
0 DAC12_0 output on P6.6, DAC12_1 output on P6.7
1 DAC12_0 output on VeREF+, DAC12_1 output on P5.1
MSP430Fx42x0 Devices:
0 DAC12_0 output not available external to the device
1 DAC12_0 output available internally and externally.
MSP430FG47x Devices:
0 DAC12_x output not available external to the device
1 DAC12_x output available internally and externally.

DAC12 SREFx Bits 14-13 DAC12 select reference voltage
MSP430FG43x and MSP430FG461x Devices:
00 V_{REF+}
01 V_{REF+}
10 Ve_{REF+}
11 Ve_{REF+}
MSP430Fx42x0 and MSP430FG47x Devices:
00 AV_{CC}
01 AV_{CC}
10 V_{REF} (internal from SD16_A or external)
11 V_{REF} (internal from SD16_A or external)

DAC12RES Bit 12 DAC12 resolution select
0 12-bit resolution
1 8-bit resolution

DAC12 LSELx Bits 11-10

DAC12 load select. Selects the load trigger for the DAC12 latch. DAC12ENC must be set for the DAC to update, except when DAC12LSELx = 0.

00 DAC12 latch loads when DAC12_xDAT written (DAC12ENC is ignored)
01 DAC12 latch loads when DAC12_xDAT written, or, when grouped, when all DAC12_xDAT registers in the group have been written.
10 Rising edge of Timer_A.OUT1 (TA1)
11 Rising edge of Timer_B.OUT2 (TB2)

DAC12 CALON Bit 9

DAC12 calibration on. This bit initiates the DAC12 offset calibration sequence and is automatically reset when the calibration completes.

0 Calibration is not active
1 Initiate calibration/calibration in progress

DAC12IR Bit 8

DAC12 input range. This bit sets the reference input and voltage output range.

0 DAC12 full-scale output = 3x reference voltage
1 DAC12 full-scale output = 1x reference voltage

DAC12 AMPx Bits 7-5

DAC12 amplifier setting. These bits select settling time vs. current consumption for the DAC12 input and output amplifiers.

DAC12AMPx	Input Buffer	Output Buffer
000	Off	DAC12 off, output high Z
001	Off	DAC12 off, output 0 V
010	Low speed/current	Low speed/current
011	Low speed/current	Medium speed/current
100	Low speed/current	High speed/current
101	Medium speed/current	Medium speed/current
110	Medium speed/current	High speed/current
111	High speed/current	High speed/current

DAC12DF Bit 4

DAC12 data format

0 Straight binary
1 2s complement

DAC12IE Bit 3

DAC12 interrupt enable

0 Disabled
1 Enabled

DAC12IFG Bit 2

DAC12 Interrupt flag

0 No interrupt pending
1 Interrupt pending

DAC12ENC Bit 1

DAC12 enable conversion. This bit enables the DAC12 module when DAC12LSELx > 0. When DAC12LSELx = 0, DAC12ENC is ignored.

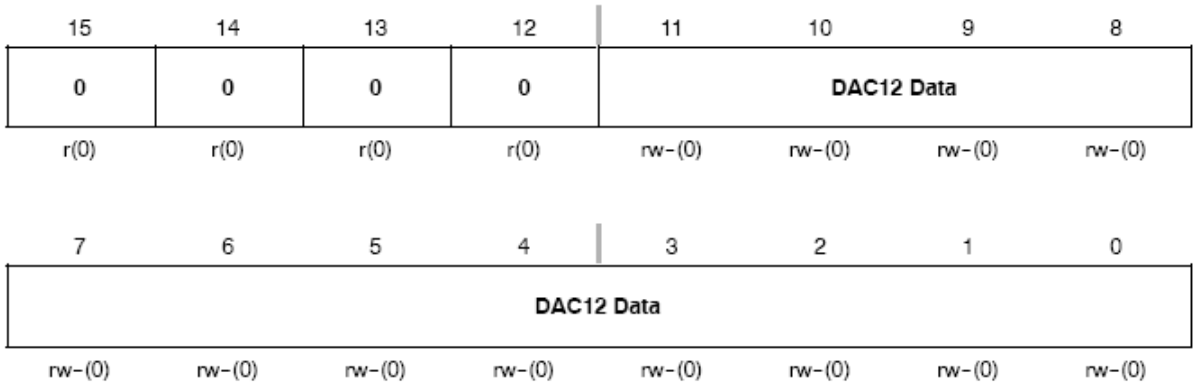
0 DAC12 disabled
1 DAC12 enabled

DAC12GRP Bit 0

DAC12 group. Groups DAC12_x with the next higher DAC12_x. Not used for DAC12_1 on MSP430FG43x, MSP430FG47x, MSP430x42x0, or MSP430FG461x devices.

0 Not grouped
1 Grouped

DAC12_xDAT, DAC12 Data Register



15	14	13	12	11	10	9	8
0	0	0	0	DAC12 Data			
r(0)	r(0)	r(0)	r(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

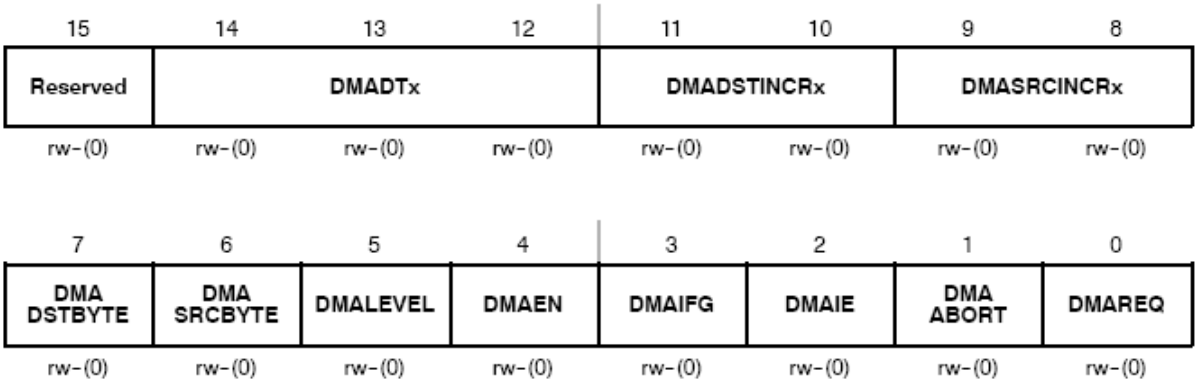
7	6	5	4	3	2	1	0
DAC12 Data							
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Unused Bits 15-12 Unused. These bits are always 0 and do not affect the DAC12 core.

DAC12 Data Bits 11-0 DAC12 data

DAC12 Data Format	DAC12 Data
12-bit binary	The DAC12 data are right-justified. Bit 11 is the MSB.
12-bit 2s complement	The DAC12 data are right-justified. Bit 11 is the MSB (sign).
8-bit binary	The DAC12 data are right-justified. Bit 7 is the MSB. Bits 11 to 8 are don't care and do not affect the DAC12 core.
8-bit 2s complement	The DAC12 data are right-justified. Bit 7 is the MSB (sign). Bits 11 to 8 are don't care and do not affect the DAC12 core.

DMAxCTL, DMA Channel x Control Register



15	14	13	12	11	10	9	8
Reserved	DMADTx			DMADSTINCRx		DMASRCINCRx	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

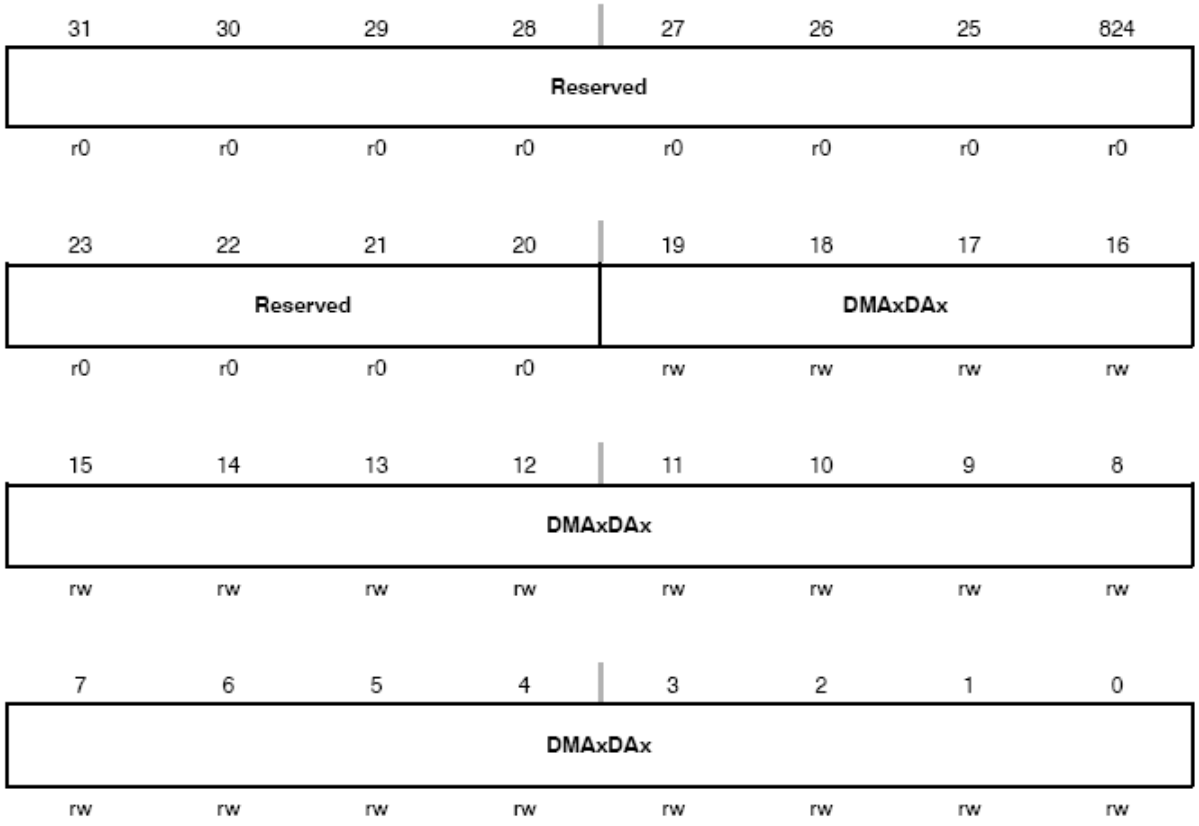
7	6	5	4	3	2	1	0
DMA DSTBYTE	DMA SRCBYTE	DMALEVEL	DMAEN	DMAIFG	DMAIE	DMA ABORT	DMAREQ
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Reserved Bit 15 Reserved

DMADTx	Bits 14–12	DMA Transfer mode. 000 Single transfer 001 Block transfer 010 Burst-block transfer 011 Burst-block transfer 100 Repeated single transfer 101 Repeated block transfer 110 Repeated burst-block transfer 111 Repeated burst-block transfer
DMA DSTINCRx	Bits 11–10	DMA destination increment. This bit selects automatic incrementing or decrementing of the destination address after each byte or word transfer. When DMADSTBYTE=1, the destination address increments/decrements by one. When DMADSTBYTE=0, the destination address increments/decrements by two. The DMAxDA is copied into a temporary register and the temporary register is incremented or decremented. DMAxDA is not incremented or decremented. 00 Destination address is unchanged 01 Destination address is unchanged 10 Destination address is decremented 11 Destination address is incremented
DMA SRCINCRx	Bits 9–8	DMA source increment. This bit selects automatic incrementing or decrementing of the source address for each byte or word transfer. When DMASRCBYTE=1, the source address increments/decrements by one. When DMASRCBYTE=0, the source address increments/decrements by two. The DMAxSA is copied into a temporary register and the temporary register is incremented or decremented. DMAxSA is not incremented or decremented. 00 Source address is unchanged 01 Source address is unchanged 10 Source address is decremented 11 Source address is incremented
DMA DSTBYTE	Bit 7	DMA destination byte. This bit selects the destination as a byte or word. 0 Word 1 Byte
DMA SRCBYTE	Bit 6	DMA source byte. This bit selects the source as a byte or word. 0 Word 1 Byte
DMA LEVEL	Bit 5	DMA level. This bit selects between edge-sensitive and level-sensitive triggers. 0 Edge sensitive (rising edge) 1 Level sensitive (high level)
DMAEN	Bit 4	DMA enable 0 Disabled 1 Enabled
DMAIFG	Bit 3	DMA interrupt flag 0 No interrupt pending 1 Interrupt pending

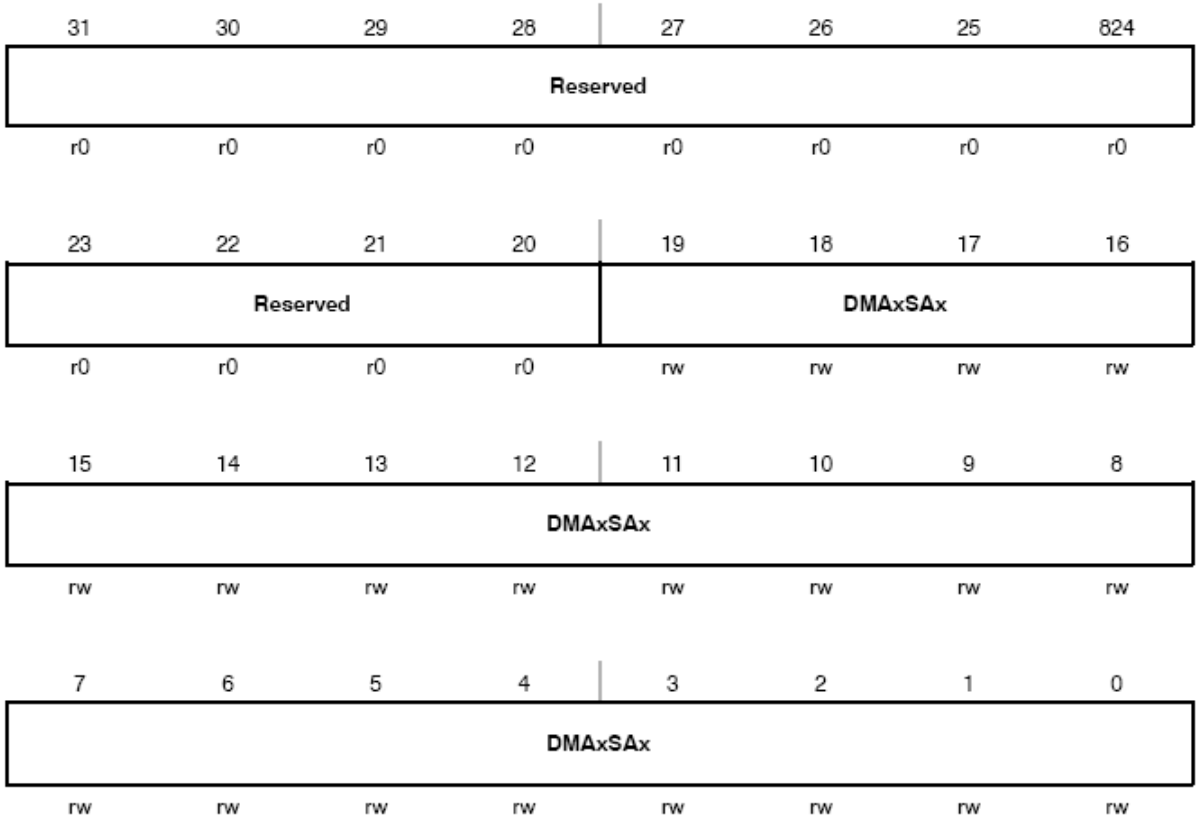
DMAIE	Bit 2	DMA interrupt enable 0 Disabled 1 Enabled
DMA ABORT	Bit 1	DMA Abort. This bit indicates if a DMA transfer was interrupt by an NMI. 0 DMA transfer not interrupted 1 DMA transfer was interrupted by NMI
DMAREQ	Bit 0	DMA request. Software-controlled DMA start. DMAREQ is reset automatically. 0 No DMA start 1 Start DMA

DMAxDA, DMA Destination Address Register



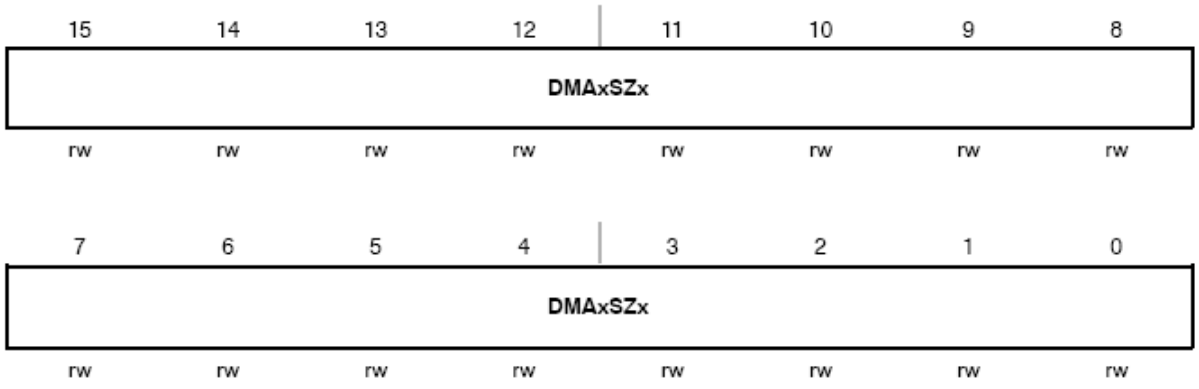
Reserved	Bits 31-20	Reserved
DMAxDAx	Bits 19-0	DMA destination address. The destination address register points to the destination address for single transfers or the first address for block transfers. The DMAxDA register remains unchanged during block and burst-block transfers. Devices that have addressable memory range 64-KB or below contain a single word for the DMAxDA. MSP430FG461x and MSP430F471xx devices implement two words for the DMAxDA register as shown. Bits 31-20 are reserved and always read as zero. Reading or writing bits 19-16 requires the use of extended instructions. When writing to DMAxDA with word instructions, bits 19-16 are cleared.

DMAxSA, DMA Source Address Register



Reserved	Bits 31–20	Reserved
DMAxSAx	Bits 19–0	DMA source address. The source address register points to the DMA source address for single transfers or the first source address for block transfers. The source address register remains unchanged during block and burst-block transfers. Devices that have addressable memory range 64-KB or below contain a single word for the DMAxSA. MSP430FG461x and MSP430F471xx devices implement two words for the DMAxSA register as shown. Bits 31–20 are reserved and always read as zero. Reading or writing bits 19-16 requires the use of extended instructions. When writing to DMAxSA with word instructions, bits 19-16 are cleared.

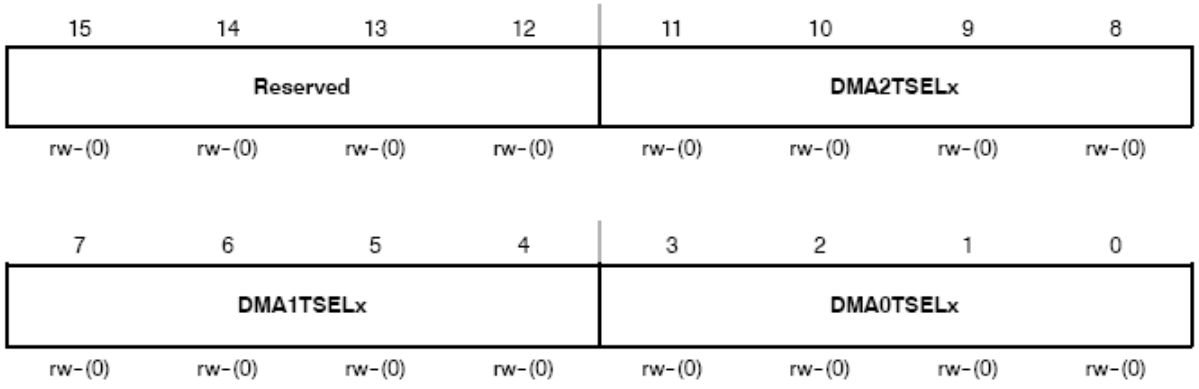
DMAxSZ, DMA Size Address Register



DMAxSZx Bits 15-0 DMA size. The DMA size register defines the number of byte/word data per block transfer. DMAxSZ register decrements with each word or byte transfer. When DMAxSZ decrements to 0, it is immediately and automatically reloaded with its previously initialized value.

00000h Transfer is disabled
00001h One byte or word to be transferred
00002h Two bytes or words have to be transferred
:
0FFFFh 65535 bytes or words have to be transferred

DMACTL0, DMA Control Register 0



Reserved Bits 15-12 Reserved

DMA2 TSELx	Bits 11-8	DMA trigger select. These bits select the DMA transfer trigger. The trigger selection is device-specific. For MSP430FG43x and MSP430FG461x devices it is given below; for other devices, see the device-specific data sheet. 0000 DMAREQ bit (software trigger) 0001 TACCR2 CCIFG bit 0010 TBCCR2 CCIFG bit 0011 URXIFG0 (MSP430FG43x), UCA0RXIFG (MPS430FG461x) 0100 UTXIFG0 (MSP430FG43x), UCA0TXIFG (MSP430FG461x) 0101 DAC12_0CTL DAC12IFG bit 0110 ADC12 ADC12IFGx bit 0111 TACCR0 CCIFG bit 1000 TBCCR0 CCIFG bit 1001 URXIFG1 bit 1010 UTXIFG1 bit 1011 Multiplier ready 1100 No action (MSP430FG43x), UCB0RXIFG (MSP430FG461x) 1101 No action (MSP430FG43x), UCB0TXIFG (MSP430FG461x) 1110 DMA0IFG bit triggers DMA channel 1 DMA1IFG bit triggers DMA channel 2 DMA2IFG bit triggers DMA channel 0 1111 External trigger DMAE0
DMA1 TSELx	Bits 7-4	Same as DMA2TSELx
DMA0 TSELx	Bits 3–0	Same as DMA2TSELx

DMACTL1, DMA Control Register 1

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	0	0	0	0	DMA ONFETCH	ROUND ROBIN	ENNMI
r0	r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)

Reserved	Bits 15-3	Reserved. Read only. Always read as 0.
DMA ONFETCH	Bit 2	DMA on fetch 0 The DMA transfer occurs immediately 1 The DMA transfer occurs on next instruction fetch after the trigger
ROUND ROBIN	Bit 1	Round robin. This bit enables the round-robin DMA channel priorities. 0 DMA channel priority is DMA0 - DMA1 - DMA2 1 DMA channel priority changes with each transfer

ENNMI Bit 0 Enable NMI. This bit enables the interruption of a DMA transfer by an NMI interrupt. When an NMI interrupts a DMA transfer, the current transfer is completed normally, further transfers are stopped, and DMAABORT is set.
0 NMI interrupt does not interrupt DMA transfer
1 NMI interrupt interrupts a DMA transfer

DMAIV, DMA Interrupt Vector Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	0	0	0	DMAIVx			0
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r0

DMAIVx Bits 15-0 DMA Interrupt Vector value

DMAIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
00h	No interrupt pending	-	
02h	DMA channel 0	DMA0IFG	Highest
04h	DMA channel 1	DMA1IFG	
06h	DMA channel 2	DMA2IFG	
08h	Reserved	-	
0Ah	Reserved	-	
0Ch	Reserved	-	
0Eh	Reserved	-	Lowest

FCTL1, Flash Memory Control Register

15	14	13	12	11	10	9	8
FRKEY, Read as 096h FWKEY, Must be written as 0A5h							

7	6	5	4	3	2	1	0
BLKWRT	WRT	Reserved	EEIEX‡	GMERAS† EEI‡	MERAS	ERASE	Reserved
rw-0	rw-0	r0	r0	rw-0	rw-0	rw-0	r0

† MSP430FG461x devices only. Reserved with r0 access on all other devices.
‡ MSP430F47x3/4 devices only. Reserved with r0 access on all other devices.

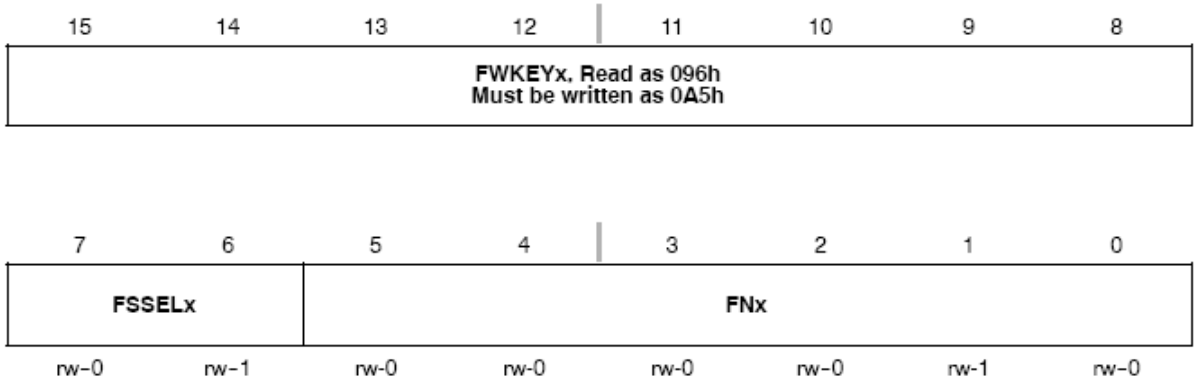
FRKEY/ FWKEY	Bits 15-8	FCTLx password. Always read as 096h. Must be written as 0A5h or a PUC is generated.
BLKWRT	Bit 7	Block write mode. WRT must also be set for block write mode. BLKWRT is automatically reset when EMEX is set. 0 Block-write mode is off 1 Block-write mode is on
WRT	Bit 6	Write. This bit is used to select any write mode. WRT is automatically reset when EMEX is set. 0 Write mode is off 1 Write mode is on
Reserved	Bit 5	Reserved. Always read as 0.
EEIEX	Bit 4	Enable emergency interrupt exit. Setting this bit enables an interrupt to cause an emergency exit from a flash operation when GIE = 1. EEIEX is automatically reset when EMEX is set. 0 Exit interrupt disabled 1 Exit on interrupt enabled
EEI	Bits 3	Enable erase Interrupts. Setting this bit allows a segment erase to be interrupted by an interrupt request. After the interrupt is serviced, the erase cycle is resumed. 0 Interrupts during segment erase disabled 1 Interrupts during segment erase enabled

GMERAS	Bit 3	Global mass erase, mass erase, and erase. These bits are used together to select the erase mode. GMERAS, MERAS, and ERASE are automatically reset when EMEX is set or the erase operation completes.
MERAS	Bit 2	
ERASE	Bit 1	

GMERAS	MERAS	ERASE	Erase Cycle
0	0	0	No erase
X	0	1	Erase individual segment only
0	1	0	Erase main memory segment of selected array
0	1	1	Erase main memory segments and information segments of selected array
1	1	0	Erase main memory segments of all memory arrays.
1	1	1	Erase all main memory and information segments of all memory arrays

Reserved	Bit 0	Reserved. Always read as 0.

FCTL2, Flash Memory Control Register



FWKEYx	Bits 15-8	FCTLx password. Always read as 096h. Must be written as 0A5h, or a PUC is generated.
FSSELx	Bits 7-6	Flash controller clock source select 00 ACLK 01 MCLK 10 SMCLK 11 SMCLK
FNx	Bits 5-0	Flash controller clock divider. These six bits select the divider for the flash controller clock. The divisor value is FNx + 1. For example, when FNx = 00h, 0the divisor is 1. When FNx = 03Fh the divisor is 64.

FCTL3, Flash Memory Control Register

15	14	13	12	11	10	9	8
FWKEYx. Read as 096h Must be written as 0A5h							

7	6	5	4	3	2	1	0
FAIL†	LOCKA†	EMEX	LOCK	WAIT	ACCVIFG	KEYV	BUSY
r(w)-0	r(w)-1	rw-0	rw-1	r-1	rw-0	rw-(0)	r(w)-0

† MSP430FG47x, MSP430F47x, MSP430F47x3/4, and MSP430F471xx devices only. Reserved with r0 access on all other devices.

FWKEYx Bits 15-8 FCTLx password. Always read as 096h. Must be written as 0A5h, or a PUC is generated.

FAIL Bit 7 Operation failure. This bit is set if the f_{FTG} clock source fails or if a flash operation is aborted from an interrupt when EEIEX = 1. FAIL must be reset with software.
0 No failure
1 Failure

LOCKA Bit 6 SegmentA and Info lock. Write a 1 to this bit to change its state. Writing 0 has no effect.
0 Segment A unlocked and all information memory is erased during a mass erase.
1 Segment A locked and all information memory is protected from erasure during a mass erase.

EMEX Bit 5 Emergency exit
0 No emergency exit
1 Emergency exit

LOCK Bit 4 Lock. This bit unlocks the flash memory for writing or erasing. The LOCK bit can be set anytime during a byte/word write or erase operation and the operation completes normally. In the block write mode, if the LOCK bit is set while BLKWRT=WAIT=1, then BLKWRT and WAIT are reset, and the mode ends normally.
0 Unlocked
1 Locked

WAIT Bit 3 Wait. Indicates the flash memory is being written.
0 The flash memory is not ready for the next byte/word write
1 The flash memory is ready for the next byte/word write

ACCVIFG Bit 2 Access violation interrupt flag
0 No interrupt pending
1 Interrupt pending

KEYV	Bit 1	Flash security key violation. This bit indicates an incorrect FCTLx password was written to any flash control register and generates a PUC when set. KEYV must be reset with software. 0 FCTLx password was written correctly 1 FCTLx password was written incorrectly
BUSY	Bit 0	Busy. This bit indicates the status of the flash timing generator. 0 Not busy 1 Busy

FLL_CTL0, FLL+ Control Register 0

7	6	5	4	3	2	1	0
DCOPLUS	**XTS_FLL**	**XCAPxPF**		**XT2OF†**	**XT1OF**	**LFOF**	**DCOF**
rw-0	rw-0	rw-0	rw-0	r-0	r-0	r-(1)	r-1

† Not present in MSP430x41x, MSP430x42x devices

DCOPLUS	Bit 7	DCO output pre-divider. This bit selects if the DCO output is pre-divided before sourcing MCLK or SMCLK. The division rate is selected with the FLL_D bits 0 DCO output is divided 1 DCO output is not divided
XTS_FLL	Bit 6	LFTX1 mode select 0 Low frequency mode 1 High frequency mode
XCAPxPF	Bits 5-4	Oscillator capacitor selection. These bits select the effective capacitance seen by the LFXT1 crystal or resonator. Should be set to 00 if the high-frequency mode is selected for LFXT1 with XTS_FLL = 1. 00 ~1 pF 01 ~6 pF 10 ~8 pF 11 ~10 pF
XT2OF	Bit 3	XT2 oscillator fault. Not present in MSP430x41x, and MSP430x42x devices. 0 No fault condition present 1 Fault condition present
XT1OF	Bit 2	LFXT1 high-frequency oscillator fault 0 No fault condition present 1 Fault condition present
LFOF	Bit 1	LFXT1 low-frequency oscillator fault 0 No fault condition present 1 Fault condition present
DCOF	Bit 0	DCO oscillator fault 0 No fault condition present 1 Fault condition present

FLL_CTL1, FLL+ Control Register 1

7	6	5	4	3	2	1	0
LFXT1DIG‡	SMCLK OFF†	XT2OFF†	SELMx†		SELS†	FLL_DIVx	
rw-0	rw-0	rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

† Not present in MSP430x41x, MSP430x42x devices except MSP430F41x2.
‡ Only supported by MSP430xG46x, MSP430FG47x, MSP430F47x, MSP430x47x3/4, and MSP430F471xx devices. Otherwise unused.

LFXT1DIG Bit 7 Select digital external clock source. This bit enables the input of an external digital clock signal on XIN in low-frequency mode (XTS_FLL = 0). Only supported in MSP430xG46x, MSP430FG47x, MSP430F47x, MSP430x47x3/4, and MSP430F471xx devices.
0 Crystal input selected
1 Digital clock input selected

SMCLKOFF Bit 6 SMCLK off. This bit turns off SMCLK. Not present in MSP430x41x and MSPx42x devices.
0 SMCLK is on
1 SMCLK is off

XT2OFF Bit 5 XT2 off. This bit turns off the XT2 oscillator. Not present in MSP430x41x and MSPx42x devices.
0 XT2 is on
1 XT2 is off if it is not used for MCLK or SMCLK

SELMx Bits 4-3 Select MCLK. These bits select the MCLK source. Not present in MSP430x41x and MSP430x42x devices except MSP430F41x2.
00 DCOCLK
01 DCOCLK
10 XT2CLK
11 LFXT1CLK
In the MSP430F41x2 devices:
00 DCOCLK
01 DCOCLK
10 LFXT1CLK or VLO
11 LFXT1CLK or VLO

SELS Bit 2 Select SMCLK. This bit selects the SMCLK source. Not present in MSP430x41x and MSP430x42x devices.
0 DCOCLK
1 XT2CLK

FLL_DIVx Bits 1-0 ACLK divider
00 /1
01 /2
10 /4
11 /8

IE1, Interrupt Enable Register 1

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

UTXIE0 Bit 7 USART0 transmit interrupt enable. This bit enables the UTXIFG0 interrupt.
0 Interrupt not enabled
1 Interrupt enabled

URXIE0 Bit 6 USART0 receive interrupt enable. This bit enables the URXIFG0 interrupt.
0 Interrupt not enabled
1 Interrupt enabled

ACCVIE Bit 5 Flash memory access violation interrupt enable. This bit enables the ACCVIFG interrupt. Because other bits in IE1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 Interrupt not enabled
1 Interrupt enabled

NMIIE Bit 4 NMI interrupt enable. This bit enables the NMI interrupt. Because other bits in IE1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 Interrupt not enabled
1 Interrupt enabled

OFIE Bit 1 Oscillator fault interrupt enable. This bit enables the OFIFG interrupt. Because other bits in IE1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 Interrupt not enabled
1 Interrupt enabled

WDTIE Bit 0 Watchdog timer interrupt enable. This bit enables the WDTIFG interrupt for interval timer mode. It is not necessary to set this bit for watchdog mode. Because other bits in IE1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 Interrupt not enabled
1 Interrupt enabled

IE2, Interrupt Enable Register 2

7	6	5	4	3	2	1	0
BTIE		UTXIE1	URXIE1	UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

BTIE Bit 7 Basic Timer1 interrupt enable. This bit enables the BTIFG interrupt. Because other bits in IE2 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 Interrupt not enabled
1 Interrupt enabled

UTXIE1 Bit 5 USART1 transmit interrupt enable. This bit enables the UTXIFG1 interrupt.
0 Interrupt not enabled
1 Interrupt enabled

URXIE1 Bit 4 USART1 receive interrupt enable. This bit enables the URXIFG1 interrupt.
0 Interrupt not enabled
1 Interrupt enabled

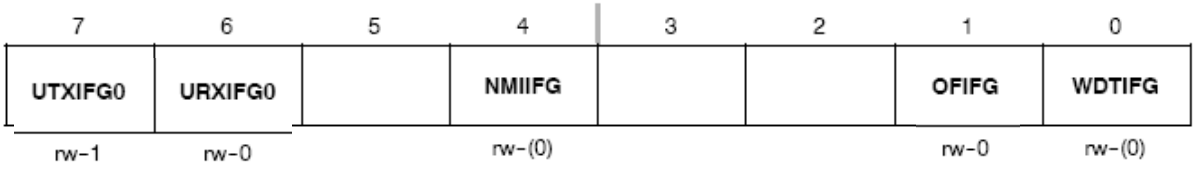
UCB0TXIE Bit 3 USCI_B0 transmit interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCB0RXIE Bit 2 USCI_B0 receive interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCA0TXIE Bit 1 USCI_A0 transmit interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCA0RXIE Bit 0 USCI_A0 receive interrupt enable
0 Interrupt disabled
1 Interrupt enabled

IFG1, Interrupt Flag Register 1



7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
rw-1	rw-0		rw-(0)			rw-0	rw-(0)

UTXIFG0 Bit 7 USART0 transmit interrupt flag. UTXIFG0 is set when U0TXBUF is empty.
0 No interrupt pending
1 Interrupt pending

URXIFG0 Bit 6 USART0 receive interrupt flag. URXIFG0 is set when U0RXBUF has received a complete character.
0 No interrupt pending
1 Interrupt pending

NMIIFG Bit 4 NMI interrupt flag. NMIIFG must be reset by software. Because other bits in IFG1 may be used for other modules, it is recommended to clear NMIIFG by using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 No interrupt pending
1 Interrupt pending

OFIFG Bit 1 Oscillator fault interrupt flag. Because other bits in IFG1 may be used for other modules, it is recommended to set or clear this bit using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 No interrupt pending
1 Interrupt pending

WDTIFG Bit 0 Watchdog timer interrupt flag. In watchdog mode, WDTIFG remains set until reset by software. In interval mode, WDTIFG is reset automatically by servicing the interrupt, or it can be reset by software. Because other bits in IFG1 may be used for other modules, it is recommended to clear WDTIFG by using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 No interrupt pending
1 Interrupt pending

IFG2, Interrupt Flag Register 2

7	6	5	4	3	2	1	0
BTIFG		UTXIFG1	URXIFG1	UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
rw-0		rw-1	rw-0	rw-1	rw-0	rw-1	rw-0

BTIFG Bit 7 Basic Timer1 interrupt flag. Because other bits in IFG2 may be used for other modules, it is recommended to clear BTIFG automatically by servicing the interrupt, or by using `BIS.B` or `BIC.B` instructions, rather than `MOV.B` or `CLR.B` instructions.
0 No interrupt pending
1 Interrupt pending

UTXIFG1	Bit 5	USART1 transmit interrupt flag. UTXIFG1 is set when U1TXBUF empty. 0 No interrupt pending 1 Interrupt pending
URXIFG1	Bit 4	USART1 receive interrupt flag. URXIFG1 is set when U1RXBUF has received a complete character. 0 No interrupt pending 1 Interrupt pending
UCB0 TXIFG	Bit 3	USCI_B0 transmit interrupt flag. UCB0TXIFG is set when UCB0TXBUF is empty. 0 No interrupt pending 1 Interrupt pending
UCB0 RXIFG	Bit 2	USCI_B0 receive interrupt flag. UCB0RXIFG is set when UCB0RXBUF has received a complete character. 0 No interrupt pending 1 Interrupt pending
UCA0 TXIFG	Bit 1	USCI_A0 transmit interrupt flag. UCA0TXIFG is set when UCA0TXBUF empty. 0 No interrupt pending 1 Interrupt pending
UCA0 RXIFG	Bit 0	USCI_A0 receive interrupt flag. UCA0RXIFG is set when UCA0RXBUF has received a complete character. 0 No interrupt pending 1 Interrupt pending

LCDACTL, LCD_A Control Register

7	6	5	4	3	2	1	0
LCDFREQx			**LCDMXx**		**LCDSON**	**Unused**	**LCDON**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LCDFREQx	Bits 7-5	LCD frequency select. These bits select the ACLK divider for the LCD frequency. 000 Divide by 32 001 Divide by 64 010 Divide by 96 011 Divide by 128 100 Divide by 192 101 Divide by 256 110 Divide by 384 111 Divide by 512
LCDMXx	Bits 4-3	LCD mux rate. These bits select the LCD mode. 00 Static 01 2-mux 10 3-mux 11 4-mux

LCDSON	Bit 2	LCD segments on. This bit supports flashing LCD applications by turning off all segment lines, while leaving the LCD timing generator and R33 enabled. 0 All LCD segments are off 1 All LCD segments are enabled and on or off according to their corresponding memory location.
Unused	Bit 1	Unused
LCDON	Bit 0	LCD On. This bit turns on the LCD_A module. 0 LCD_A module off. 1 LCD_A module on.

LCDAPCTL0, LCA_A Port Control Register 0

7	6	5	4	3	2	1	0
LCDS28	**LCDS24**	**LCDS20**	**LCDS16**	**LCDS12**	**LCDS8**	**LCDS4**	**LCDS0†**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

† Segments S0-S3 on the MSP430FG461x devices are disabled from LCD functionality when charge pump is enabled.

LCDS28	Bit 7	LCD segment 28 to 31 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS24	Bit 6	LCD segment 24 to 27 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS20	Bit 5	LCD segment 20 to 23 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS16	Bit 4	LCD segment 16 to 19 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS12	Bit 3	LCD segment 12 to 15 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS8	Bit 2	LCD segment 8 to 11 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions

LCDS4	Bit 1	LCD segment 4 to 7 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS0	Bit 0	LCD segment 0 to 3 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions

LCDAPCTL1, LCD_A Port Control Register 1

7	6	5	4	3	2	1	0
Unused						**LCDS36**	**LCDS32**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Unused	Bits 7-2	Unused
LCDS36	Bit 1	LCD segment 36 to 39 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS32	Bit 0	LCD segment 32 to 35 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions

LCDAVCTL0, LCD_A Voltage Control Register 0

7	6	5	4	3	2	1	0
Unused	**R03EXT**	**REXT**	**VLCDEXT**	**LCDCPEN**	**VLCDREFx**		**LCD2B**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Unused	Bit 7	Unused
R03EXT	Bit 6	V5 voltage select. This bit selects the external connection for the lowest LCD voltage. R03EXT is ignored if there is no R03 pin available. 0 V5 is AV_{SS} 1 V5 is sourced from the R03 pin

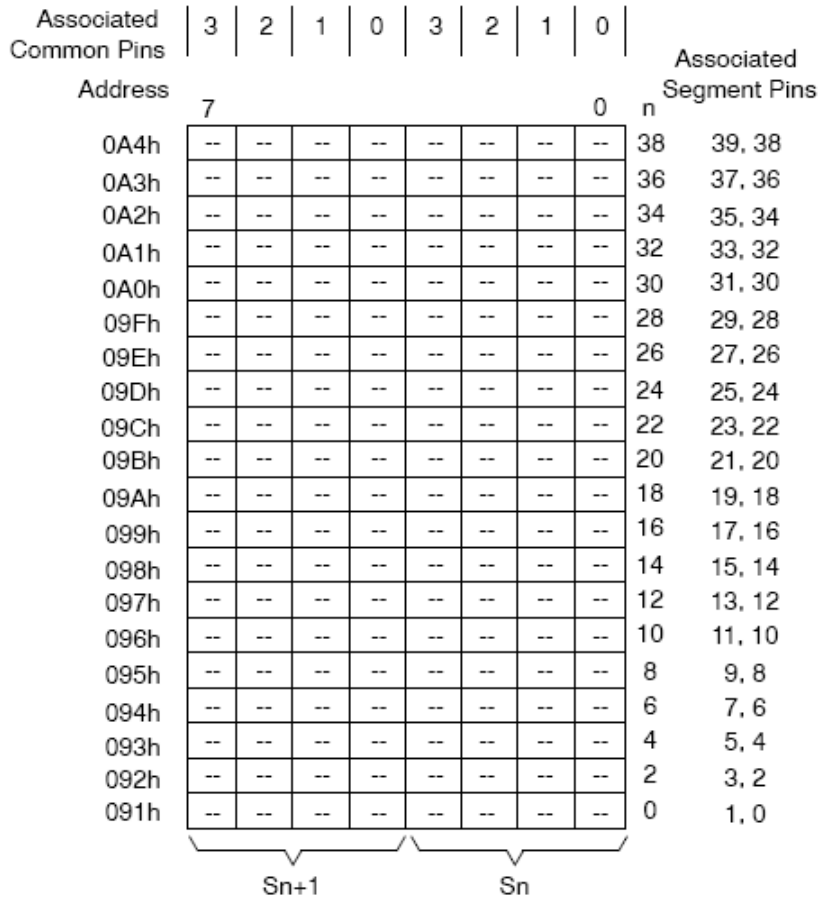
REXT	Bit 5	V2 – V4 voltage select. This bit selects the external connections for voltages V2 – V4. 0 V2 – V4 are generated internally 1 V2 – V4 are sourced externally and the internal bias generator is switched off
VLCDEXT	Bit 4	V_{LCD} source select 0 V_{LCD} is generated internally 1 V_{LCD} is sourced externally
LCDCPEN	Bit 3	Charge pump enable. 0 Charge pump disabled. 1 Charge pump enabled when V_{LCD} is generated internally (VLCDEXT = 0) and VLCDx > 0 or VLCDREFx > 0.
VLCDREFx	Bits 2–1	Charge pump reference select 00 Internal 01 External 10 Reserved 11 Reserved
LCD2B	Bit 0	Bias select. LCD2B is ignored when LCDMx = 00. 0 1/3 bias 1 1/2 bias

LCDAVCTL1, LCD_A Voltage Control Register 1

7	6	5	4	3	2	1	0
Unused			**VLCDx**				**Unused**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Unused	Bits 7–5	Unused
VLCDx	Bits 4–1	Charge pump voltage select. LCDCPEN must be 1 for the charge pump to be enabled. AV_{CC} is used for V_{LCD} when VLCDx = 0000 and VREFx = 00 and VLCDEXT = 0. 0000 Charge pump disabled 0001 V_{LCD} = 2.60 V 0010 V_{LCD} = 2.66 V 0011 V_{LCD} = 2.72 V 0100 V_{LCD} = 2.78 V 0101 V_{LCD} = 2.84 V 0110 V_{LCD} = 2.90 V 0111 V_{LCD} = 2.96 V 1000 V_{LCD} = 3.02 V 1001 V_{LCD} = 3.08 V 1010 V_{LCD} = 3.14 V 1011 V_{LCD} = 3.20 V 1100 V_{LCD} = 3.26 V 1101 V_{LCD} = 3.32 V 1110 V_{LCD} = 3.38 V 1111 V_{LCD} = 3.44 V
Unused	Bit 0	Unused

LCDMx, LCD Memory



Associated Common Pins	3	2	1	0	3	2	1	0		
Address	7							0	n	Associated Segment Pins
0A4h	--	--	--	--	--	--	--	--	38	39, 38
0A3h	--	--	--	--	--	--	--	--	36	37, 36
0A2h	--	--	--	--	--	--	--	--	34	35, 34
0A1h	--	--	--	--	--	--	--	--	32	33, 32
0A0h	--	--	--	--	--	--	--	--	30	31, 30
09Fh	--	--	--	--	--	--	--	--	28	29, 28
09Eh	--	--	--	--	--	--	--	--	26	27, 26
09Dh	--	--	--	--	--	--	--	--	24	25, 24
09Ch	--	--	--	--	--	--	--	--	22	23, 22
09Bh	--	--	--	--	--	--	--	--	20	21, 20
09Ah	--	--	--	--	--	--	--	--	18	19, 18
099h	--	--	--	--	--	--	--	--	16	17, 16
098h	--	--	--	--	--	--	--	--	14	15, 14
097h	--	--	--	--	--	--	--	--	12	13, 12
096h	--	--	--	--	--	--	--	--	10	11, 10
095h	--	--	--	--	--	--	--	--	8	9, 8
094h	--	--	--	--	--	--	--	--	6	7, 6
093h	--	--	--	--	--	--	--	--	4	5, 4
092h	--	--	--	--	--	--	--	--	2	3, 2
091h	--	--	--	--	--	--	--	--	0	1, 0
	Sn+1				Sn					

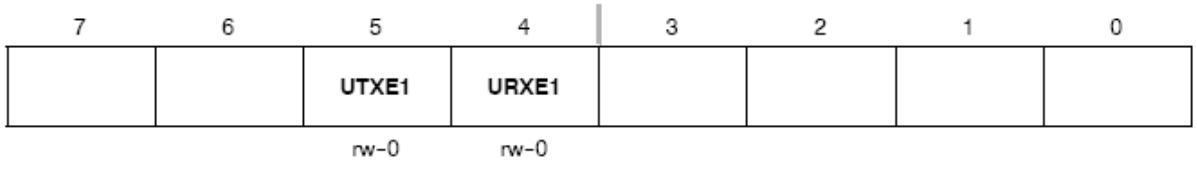
MAC, Operand 1: Unsigned Multiply Accumulate

One of the operand one registers for the 16 bit multiplier. Writing operand one to this register selects Unsigned Multiply Accumulate mode, but does not start the computation.

MACS, Operand 1: Signed Multiply Accumulate

One of the operand one registers for the 16 bit multiplier. Writing operand one to this register selects Signed Multiply Accumulate mode, but does not start the computation.

ME2, Module Enable Register



7	6	5	4	3	2	1	0
		UTXE1	URXE1				
		rw-0	rw-0				

	Bits 7-6	These bits may be used by other modules. See device-specific data sheet.
UTXE1	Bit 5	USART1 transmit enable. This bit enables the transmitter for USART1. 0 Module not enabled 1 Module enabled

URXE1	Bit 4	USART1 receive enable. This bit enables the receiver for USART1. 0 Module not enabled 1 Module enabled
	Bits 3-0	These bits may be used by other modules. See device-specific data sheet.

MPY, Operand 1: Unsigned Multiply

One of the operand one registers for the 16 bit multiplier. Writing operand one to this register selects Unsigned Multiply mode, but does not start the computation.

MPYS, Operand 1: Signed Multiply

One of the operand one registers for the 16 bit multiplier. Writing operand one to this register selects Signed Multiply mode, but does not start the computation.

OAxCTL0, Opamp Control Register 0

OANx	Bits 7-6	Inverting input select. These bits select the input signal for the OA inverting input. 00 OAxI0 01 OAxI1 10 DAC0 internal 11 DAC1 internal
OAPx	Bits 5-4	Non-inverting input select. These bits select the input signal for the OA non-inverting input. 00 OAxI0 01 OA0I1 10 DAC0 internal 11 DAC1 internal
OAPMx	Bits 3-2	Slew rate select These bits select the slew rate vs. current consumption for the OA. 00 Off, output high Z 01 Slow 10 Medium 11 Fast
OAADC1	Bit 1	OA output select. This bit connects the OAx output to ADC12 input Ax and output pin OAxO when OAFCx > 0. 0 OAx output not connected to internal/external A1 (OA0), A3 (OA1), or A5 (OA2) signals 1 OAx output connected to internal/external A1 (OA0), A3 (OA1), or A5 (OA2) signals

OAADC0	Bit 0	OA output select. This bit connects the OAx output to ADC12 input Ax when OAPMx > 0. 0 OAx output not connected to internal A12 (OA0), A13 (OA1), or A14 (OA2) signals 1 OAx output connected to internal A12 (OA0), A13 (OA1), or A14 (OA2) signals

OAxCTL1, Opamp Control Register 1

7	6	5	4	3	2	1	0
OAFBRx			**OAFCx**			**Reserved**	**OARRIP**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

OAFBRx	Bits 7-5	OAx feedback resistor select 000 Tap 0 001 Tap 1 010 Tap 2 011 Tap 3 100 Tap 4 101 Tap 5 110 Tap 6 111 Tap 7
OAFCx	Bits 4-2	OAx function control. This bit selects the function of OAx 000 General purpose 001 Unity gain buffer 010 Reserved 011 Comparing amplifier 100 Non-inverting PGA 101 Reserved 110 Inverting PGA 111 Differential amplifier
Reserved	Bit 1	Reserved
OARRIP	Bit 0	OA rail-to-rail input off. 0 OAx input signal range is rail-to-rail 1 OAx input signal range is limited. See the device-specific data sheet for parameters.

OP2, 16-Bit Multiplier Operand 2

The second operand to supply the hardware multiplier. Writing to this register causes the multiplier to begin calculating for the last mode selected (last operand 1 register written too).

PxDIR, Port x Direction Registers

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other module functions must be set as required by the other function.

Bit = 0: The port pin is switched to input direction

Bit = 1: The port pin is switched to output direction

PxIE, Port x Interrupt Enable Registers (Ports 1 and 2)

Each PxIE bit enables the associated PxIFG interrupt flag.

Bit = 0: The interrupt is disabled

Bit = 1: The interrupt is enabled

PxIES, Port x Interrupt Edge Selection Registers (Ports 1 and 2)

Each PxIES bit selects the interrupt edge for the corresponding I/O pin.

Bit = 0: The PxIFGx flag is set with a low-to-high transition

Bit = 1: The PxIFGx flag is set with a high-to-low transition

PxIFG, Port x Interrupt Flag Registers (Ports 1 and 2)

Each PxIFGx bit is the interrupt flag for its corresponding I/O pin and is set when the selected input signal edge occurs at the pin. All PxIFGx interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Each PxIFG flag must be reset with software. Software can also set each PxIFG flag, providing a way to generate a software-initiated interrupt.

Bit = 0: No interrupt is pending

Bit = 1: An interrupt is pending

PxIN, Port x Input Registers

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.

Bit = 0: The input is low

Bit = 1: The input is high

PxOUT, Port x Output Registers

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function and output direction.

Bit = 0: The output is low

Bit = 1: The output is high

PxREN, Port x Pull Resistor Enable Registers

In MSP430x47x devices all port pins have a programmable pullup/pulldown resistor. Each bit in each PxREN register enables or disables the pullup/pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin is pulled up or pulled down.

Bit = 0: Pullup/pulldown resistor disabled

Bit = 1: Pullup/pulldown resistor enabled

PxSEL, Port x Function Select Registers

Port pins are oftenmultiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each PxSEL bit is used to select the pin function — I/O port or peripheral module function.

Bit = 0: I/O function is selected for the pin

Bit = 1: Peripheral module function is selected for the pin

RESHI, Multiplier Result High Word

Holds the upper word of the multiplication result. If a signed mode was used, than the msb holds the sign bit of the result.

RESLO, Multiplier Result Low Word

Holds the lower word of the multiplication result.

RTCCTL, Real-Time Clock Control Register

7	6	5	4	3	2	1	0
RTCBCD	RTCHOLD	RTCMODEx		RTCTEVx		RTCIE	RTCFG
rw-(0)	rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-0	rw-0

RTCBCD Bit 7 BCD format select. This bit selects BCD format for the calendar registers when RTCMODEx = 11.
0 Hexadecimal format
1 BCD format

RTCHOLD Bit 6 Real-Time Clock hold
0 Real-Time Clock is operational
1 RTCMODEx < 11: The RTC module is stopped
RTCMODEx = 11: The RTC and the Basic Timer1 are stopped

RTCMODEx Bits 5-4 Real-Time Clock mode and clock source select

RTCMODEx	Counter Mode	Clock Source
00	32-bit counter	ACLK
01	32-bit counter	BTCNT2.Q6
10	32-bit counter	SMCLK
11	Calendar mode	BTCNT2.Q6

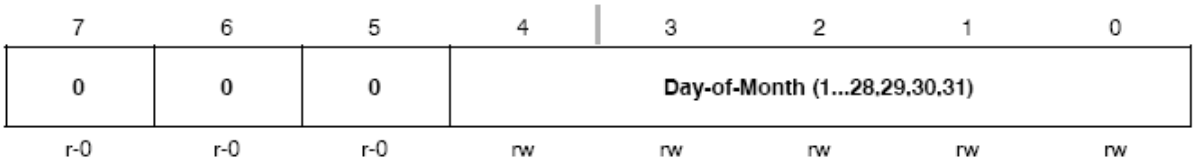
RTCTEVx Bits 3-2 Real-Time Clock interrupt event. These bits select the event for setting RTCFG.

RTC Mode	RTCTEVx	Interrupt Interval
Counter Mode	00	8-bit overflow
	01	16-bit overflow
	10	24-bit overflow
	11	32-bit overflow
Calendar Mode	00	Minute changed
	01	Hour changed
	10	Every day at midnight (00:00)
	11	Every day at noon (12:00)

RTCIE Bit 1 Real-Time Clock interrupt enable
0 Interrupt not enabled
1 Interrupt enabled

RTCFG Bit 0 Real-Time Clock interrupt flag
0 No time event occurred
1 Time event occurred

RTCDAY, RTC Day-of-Month Register, Calendar Mode with Hexadecimal Format

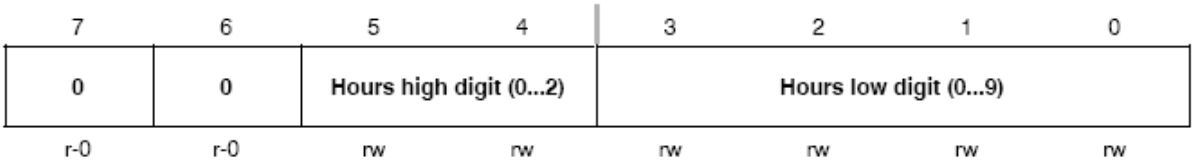


RTCDAY, RTC Day-of-Month Register, Calendar Mode with BCD Format

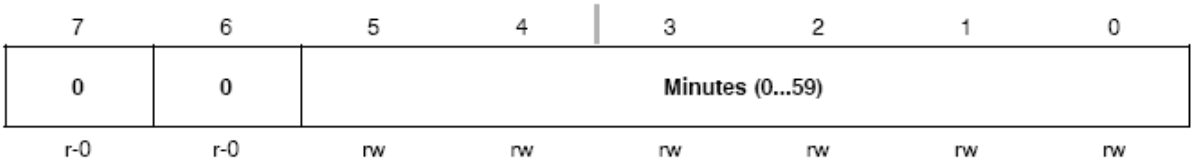
RTCDOW, RTC Day-of-Week Register, Calendar Mode

RTCHOUR, RTC Hours Register, Calendar Mode with Hexadecimal Format

RTCHOUR, RTC Hours Register, Calendar Mode with BCD Format

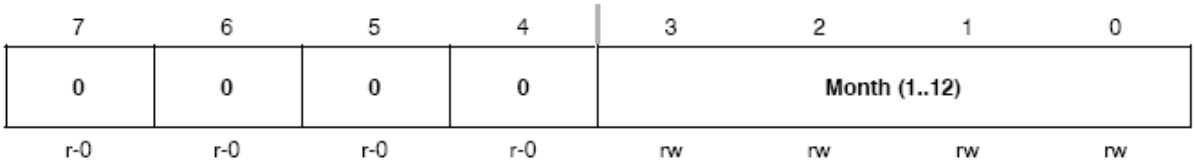


RTCMIN, RTC Minutes Register, Calendar Mode with Hexadecimal Format

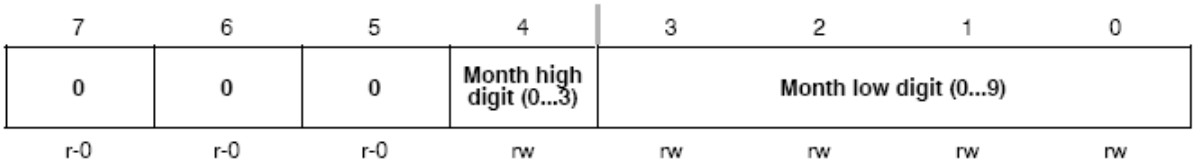


RTCMIN, RTC Minutes Register, Calendar Mode with BCD Format

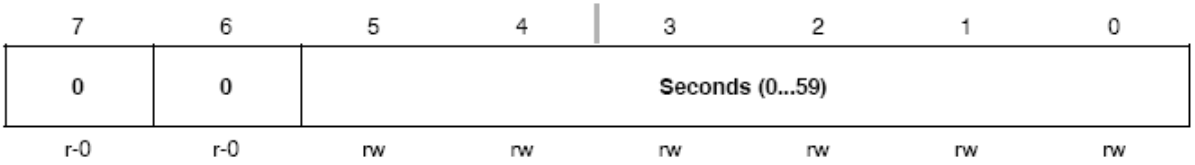
RTCMON, RTC Month Register, Calendar Mode with Hexadecimal Format



RTCMON, RTC Month Register, Calendar Mode with BCD Format

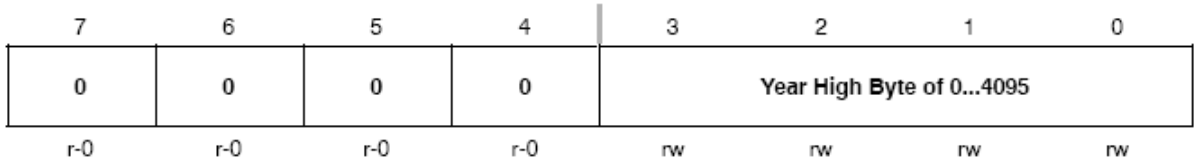


RTCSEC, RTC Seconds Register, Calendar Mode with Hexadecimal Format



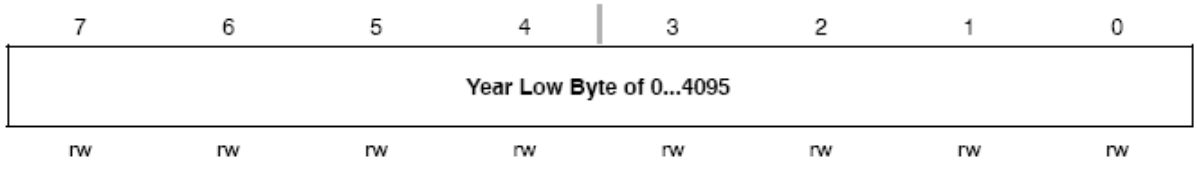
RTCSEC, RTC Seconds Register, Calendar Mode with BCD Format

RTCYEARH, RTC Year High-Byte Register, Calendar Mode with Hexadecimal Format

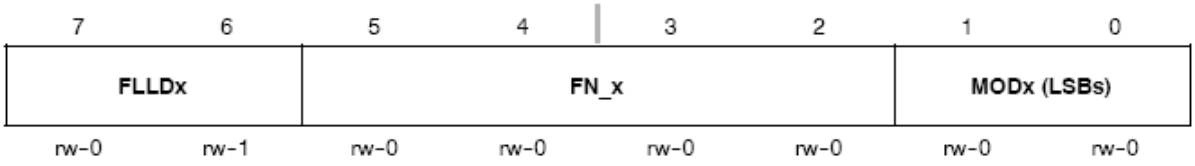


RTCYEARH, RTC Year High-Byte Register, Calendar Mode with BCD Format

RTCYEARL, RTC Year Low-Byte Register, Calendar Mode with Hexadecimal Format

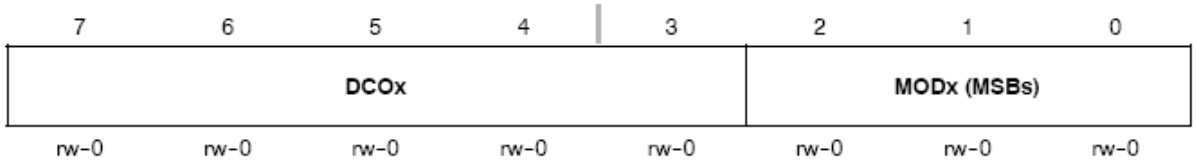


SCFI0, System Clock Frequency Integrator Register 0



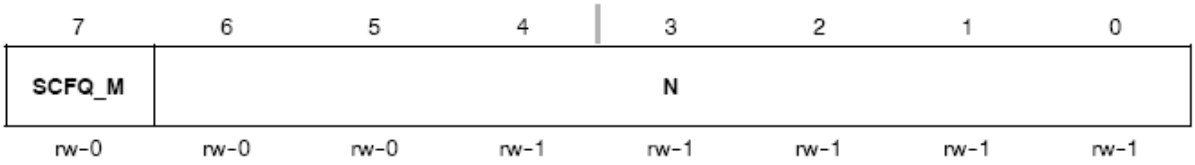
FLLDx	Bits 7-6	FLL+ loop divider. These bits divide f_{DCOCLK} in the FLL+ feedback loop. This results in an additional multiplier for the multiplier bits. See also multiplier bits. 00 /1 01 /2 10 /4 11 /8
FN_x	Bits 5-2	DCO range control. These bits select the f_{DCO} operating range. 0000 0.65 to 6.1 MHz 0001 1.3 to 12.1 MHz 001x 2 to 17.9 MHz 01xx 2.8 to 26.6 MHz 1xxx 4.2 to 46 MHz
MODx	Bits 1-0	Least significant modulator bits. Bit 0 is the modulator LSB. These bits affect the modulator pattern. All MODx bits are modified automatically by the FLL+.

SCFI1, System Clock Frequency Integrator Register 1



DCOx	Bits 7-3	These bits select the DCO tap and are modified automatically by the FLL+.
MODx	Bit 2	Most significant modulator bits. Bit 2 is the modulator MSB. These bits affect the modulator pattern. All MODx bits are modified automatically by the FLL+.

SCFQCTL, System Clock Control Register



SCFQ_M	Bit 7	Modulation. This enables or disables modulation. 0 Modulation enabled 1 Modulation disabled
N	Bits 6-0	Multiplier. These bits set the multiplier value for the DCO. N must be > 0 or unpredictable operation results. When DCOPLUS = 0: $f_{DCOCLK} = (N + 1) \cdot f_{crystal}$ When DCOPLUS = 1: $f_{DCOCLK} = D \times (N + 1) \cdot f_{crystal}$

SUMEXT, Multiplier Sum Extension Register

The sum extension registers contents depend on the multiply operation that was performed. For signed multiplication (MPYS, MACS), this register contains 0x0000 or 0xffff depending on whether the result was positive or negative. For MAC mode, this register contains either 0x0001 or 0x0000 depending on whether the result had a carry or no carry (respectively). For MPY mode, SUMEXT always contains 0x0000.

SVSCTL, SVS Control Register (Supply Voltage Supervisor)

7	6	5	4	3	2	1	0
VLDx				PORON	SVSON	SVSOP	SVSFG
rw-0†	rw-0†	rw-0†	rw-0†	rw-0†	r†	r†	rw-0†

† Reset by a brownout reset only, not by a POR or PUC.

VLDx Bits 7-4 Voltage level detect. These bits turn on the SVS and select the nominal SVS threshold voltage level. See the device-specific data sheet for parameters.
- 0000 SVS is off
- 0001 1.9 V
- 0010 2.1 V
- 0011 2.2 V
- 0100 2.3 V
- 0101 2.4 V
- 0110 2.5 V
- 0111 2.65 V
- 1000 2.8 V
- 1001 2.9 V
- 1010 3.05
- 1011 3.2 V
- 1100 3.35 V
- 1101 3.5 V
- 1110 3.7 V
- 1111 Compares external input voltage SVSIN to 1.2 V.

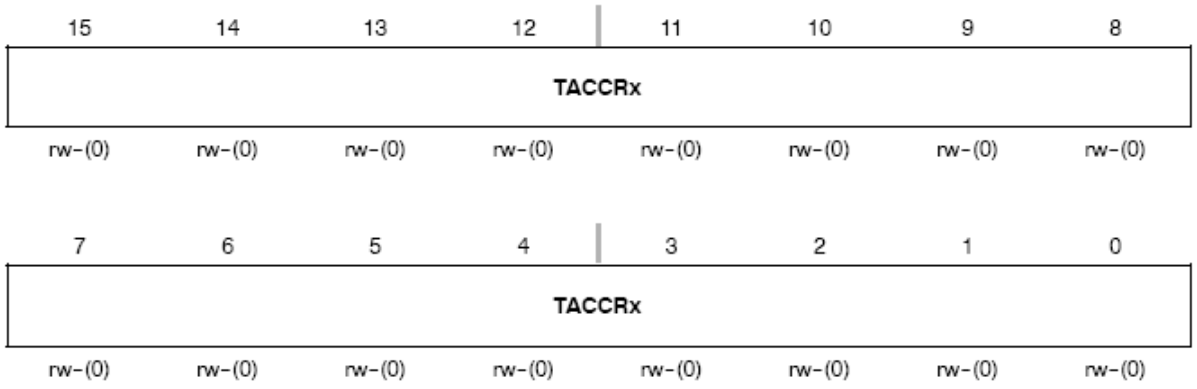
PORON Bit 3 POR on. This bit enables the SVSFG flag to cause a POR device reset.
- 0 SVSFG does not cause a POR
- 1 SVSFG causes a POR

SVSON Bit 2 SVS on. This bit reflects the status of SVS operation. This bit DOES NOT turn on the SVS. The SVS is turned on by setting VLDx > 0.
- 0 SVS is Off
- 1 SVS is On

SVSOP Bit 1 SVS output. This bit reflects the output value of the SVS comparator.
- 0 SVS comparator output is low
- 1 SVS comparator output is high

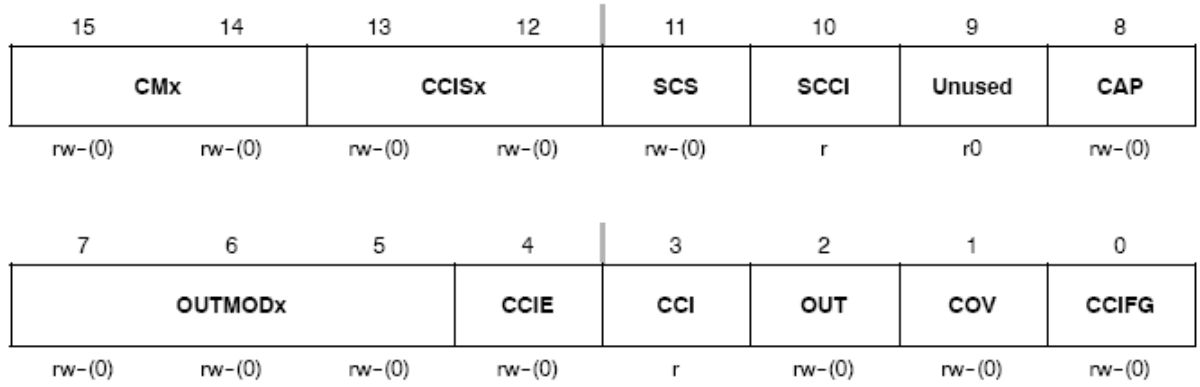
SVSFG Bit 0 SVS flag. This bit indicates a low voltage condition. SVSFG remains set after a low voltage condition until reset by software.
- 0 No low voltage condition occurred
- 1 A low condition is present or has occurred

TACCRx, Timer_A Capture/Compare Register x



TACCRx	Bits 15-0	Timer_A capture/compare register. Compare mode: TACCRx holds the data for the comparison to the timer value in the Timer_A Register, TAR. Capture mode: The Timer_A Register, TAR, is copied into the TACCRx register when a capture is performed.

TACCTLx, Capture/Compare Control Register



CMx	Bit 15-14	Capture mode 00 No capture 01 Capture on rising edge 10 Capture on falling edge 11 Capture on both rising and falling edges
CCISx	Bit 13-12	Capture/compare input select. These bits select the TACCRx input signal. See the device-specific data sheet for specific signal connections. 00 CCIxA 01 CCIxB 10 GND 11 V_{CC}
SCS	Bit 11	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0 Asynchronous capture 1 Synchronous capture

SCCI	Bit 10	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
Unused	Bit 9	Unused. Read only. Always read as 0.
CAP	Bit 8	Capture mode 0 Compare mode 1 Capture mode
OUTMODx	Bits 7-5	Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0 because EQUx = EQU0. 000 OUT bit value 001 Set 010 Toggle/reset 011 Set/reset 100 Toggle 101 Reset 110 Toggle/set 111 Reset/set
CCIE	Bit 4	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0 Interrupt disabled 1 Interrupt enabled
CCI	Bit 3	Capture/compare input. The selected input signal can be read by this bit.
OUT	Bit 2	Output. For output mode 0, this bit directly controls the state of the output. 0 Output low 1 Output high
COV	Bit 1	Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software. 0 No capture overflow occurred 1 Capture overflow occurred
CCIFG	Bit 0	Capture/compare interrupt flag 0 No interrupt pending 1 Interrupt pending

TACTL, Timer_A Control Register

15	14	13	12	11	10	9	8
Unused						TASSELx	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
IDx		MCx		Unused	TACLR	TAIE	TAIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	w-(0)	rw-(0)	rw-(0)

Unused	Bits 15-10	Unused

TASSELx	Bits 9-8	Timer_A clock source select 00 TACLK 01 ACLK 10 SMCLK 11 Inverted TACLK
IDx	Bits 7-6	Input divider. These bits select the divider for the input clock. 00 /1 01 /2 10 /4 11 /8
MCx	Bits 5-4	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00 Stop mode: the timer is halted 01 Up mode: the timer counts up to TACCR0 10 Continuous mode: the timer counts up to 0FFFFh 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h
Unused	Bit 3	Unused
TACLR	Bit 2	Timer_A clear. Setting this bit resets TAR, the clock divider, and the count direction. The TACLR bit is automatically reset and is always read as zero.
TAIE	Bit 1	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0 Interrupt disabled 1 Interrupt enabled
TAIFG	Bit 0	Timer_A interrupt flag 0 No interrupt pending 1 Interrupt pending

TAIV, Timer_A Interrupt Vector Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0

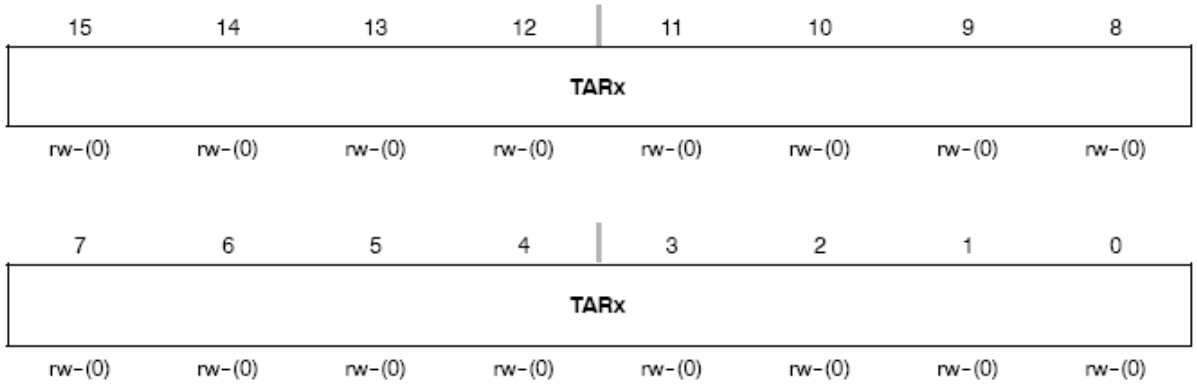
7	6	5	4	3	2	1	0
0	0	0	0	TAIVx			0
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r0

TAIVx	Bits 15-0	Timer_A interrupt vector value

TAIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
00h	No interrupt pending	-	
02h	Capture/compare 1	TACCR1 CCIFG	Highest
04h	Capture/compare 2	TACCR2 CCIFG	
06h	Capture/compare 3†	TACCR3 CCIFG	
08h	Capture/compare 4†	TACCR4 CCIFG	
0Ah	Timer overflow	TAIFG	
0Ch	Reserved	-	
0Eh	Reserved	-	Lowest

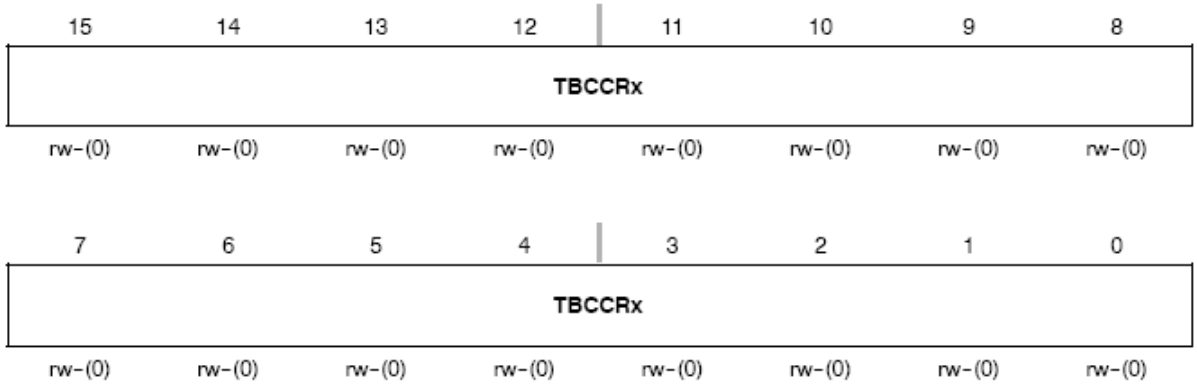
† Timer1_A5 only

TAR, Timer_A Register



TARx Bits 15-0 Timer_A register. The TAR register is the count of Timer_A.

TBCCRx, Timer_B Capture/Compare Register x



TBCCRx Bits 15-0 Timer_B capture/compare register
Compare mode: Compare data is written to each TBCCRx and automatically transferred to TBCLx. TBCLx holds the data for the comparison to the timer value in the Timer_B Register, TBR.
Capture mode: The Timer_B Register, TBR, is copied into the TBCCRx register when a capture is performed.

TBCCTLx, Timer_B Capture/Compare Control Register

15	14	13	12	11	10	9	8
CMx		CCISx		SCS	CLLDx		CAP
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	rw-(0)	rw-(0)	rw-(0)

CMx Bit 15-14 Capture mode
- 00 No capture
- 01 Capture on rising edge
- 10 Capture on falling edge
- 11 Capture on both rising and falling edges

CCISx Bit 13-12 Capture/compare input select. These bits select the TBCCRx input signal. See the device-specific data sheet for specific signal connections.
- 00 CCIxA
- 01 CCIxB
- 10 GND
- 11 V_{CC}

SCS Bit 11 Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.
- 0 Asynchronous capture
- 1 Synchronous capture

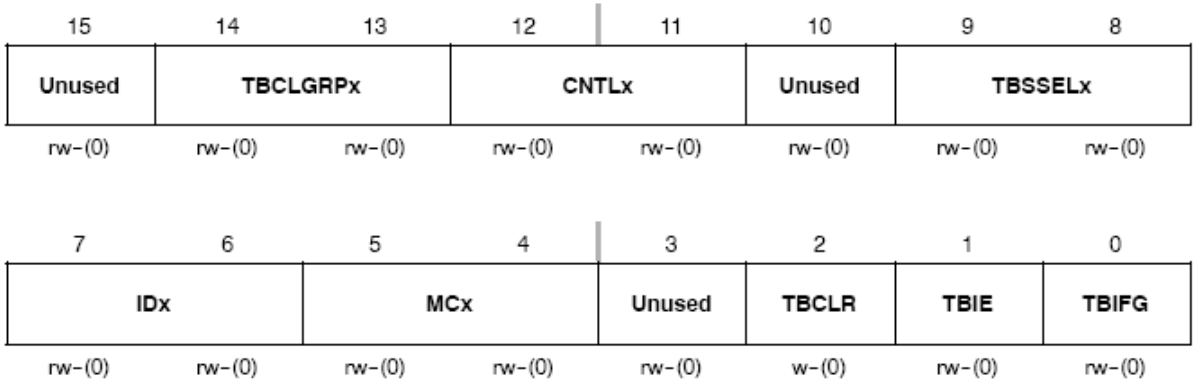
CLLDx Bit 10-9 Compare latch load. These bits select the compare latch load event.
- 00 TBCLx loads on write to TBCCRx
- 01 TBCLx loads when TBR *counts* to 0
- 10 TBCLx loads when TBR *counts* to 0 (up or continuous mode)
  TBCLx loads when TBR *counts* to TBCL0 or to 0 (up/down mode)
- 11 TBCLx loads when TBR *counts* to TBCLx

CAP Bit 8 Capture mode
- 0 Compare mode
- 1 Capture mode

OUTMODx Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TBCL0, because EQUx = EQU0.
- 000 OUT bit value
- 001 Set
- 010 Toggle/reset
- 011 Set/reset
- 100 Toggle
- 101 Reset
- 110 Toggle/set
- 111 Reset/set

CCIE	Bit 4	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0 Interrupt disabled 1 Interrupt enabled
CCI	Bit 3	Capture/compare input. The selected input signal can be read by this bit.
OUT	Bit 2	Output. For output mode 0, this bit directly controls the state of the output. 0 Output low 1 Output high
COV	Bit 1	Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software. 0 No capture overflow occurred 1 Capture overflow occurred
CCIFG	Bit 0	Capture/compare interrupt flag 0 No interrupt pending 1 Interrupt pending

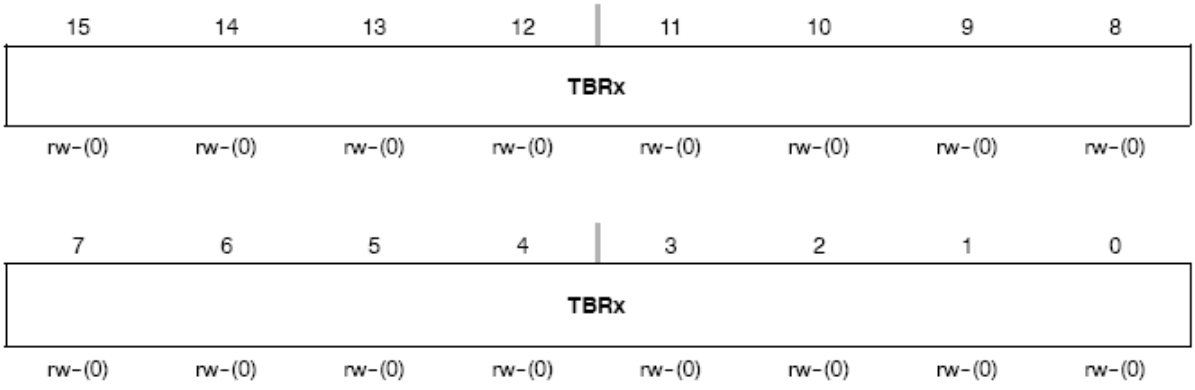
TBCTL, Timer_B Control Register



Unused	Bit 15	Unused
TBCLGRP	Bit 14-13	TBCLx group 00 Each TBCLx latch loads independently 01 TBCL1+TBCL2 (TBCCR1 CLLDx bits control the update) TBCL3+TBCL4 (TBCCR3 CLLDx bits control the update) TBCL5+TBCL6 (TBCCR5 CLLDx bits control the update) TBCL0 independent 10 TBCL1+TBCL2+TBCL3 (TBCCR1 CLLDx bits control the update) TBCL4+TBCL5+TBCL6 (TBCCR4 CLLDx bits control the update) TBCL0 independent 11 TBCL0+TBCL1+TBCL2+TBCL3+TBCL4+TBCL5+TBCL6 (TBCCR1 CLLDx bits control the update)
CNTLx	Bits 12-11	Counter length 00 16-bit, $TBR_{(max)}$ = 0FFFFh 01 12-bit, $TBR_{(max)}$ = 0FFFh 10 10-bit, $TBR_{(max)}$ = 03FFh 11 8-bit, $TBR_{(max)}$ = 0FFh

Unused	Bit 10	Unused
TBSSELx	Bits 9-8	Timer_B clock source select 00 TBCLK 01 ACLK 10 SMCLK 11 Inverted TBCLK
IDx	Bits 7-6	Input divider. These bits select the divider for the input clock. 00 /1 01 /2 10 /4 11 /8
MCx	Bits 5-4	Mode control. Setting MCx = 00h when Timer_B is not in use conserves power. 00 Stop mode: the timer is halted 01 Up mode: the timer counts up to TBCL0 10 Continuous mode: the timer counts up to the value set by TBCNTLx 11 Up/down mode: the timer counts up to TBCL0 and down to 0000h
Unused	Bit 3	Unused
TBCLR	Bit 2	Timer_B clear. Setting this bit resets TBR, the clock divider, and the count direction. The TBCLR bit is automatically reset and is always read as zero.
TBIE	Bit 1	Timer_B interrupt enable. This bit enables the TBIFG interrupt request. 0 Interrupt disabled 1 Interrupt enabled
TBIFG	Bit 0	Timer_B interrupt flag. 0 No interrupt pending 1 Interrupt pending

TBR, Timer_B Register



TBRx	Bits 15-0	Timer_B register. The TBR register is the count of Timer_B.

U1BR0, USART Baud Rate Control Register 0

7	6	5	4	3	2	1	0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
rw	rw	rw	rw	rw	rw	rw	rw

U1BR1, USART Baud Rate Control Register 1

7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
rw	rw	rw	rw	rw	rw	rw	rw

UxBRx The valid baud-rate control range is 3 ≤ UxBR < 0FFFFh, where UxBR = {UxBR1+UxBR0}. Unpredictable receive and transmit timing occurs if UxBR < 3.

U1CTL, USART Control Register

7	6	5	4	3	2	1	0
PENA	**PEV**	**SPB**	**CHAR**	**LISTEN**	**SYNC**	**MM**	**SWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

PENA Bit 7 Parity enable
- 0 Parity disabled
- 1 Parity enabled. Parity bit is generated (UTXDx) and expected (URXDx). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

PEV Bit 6 Parity select. PEV is not used when parity is disabled.
- 0 Odd parity
- 1 Even parity

SPB Bit 5 Stop bit select. Number of stop bits transmitted. The receiver always checks for one stop bit.
- 0 One stop bit
- 1 Two stop bits

CHAR Bit 4 Character length. Selects 7-bit or 8-bit character length.
- 0 7-bit data
- 1 8-bit data

LISTEN Bit 3 Listen enable. The LISTEN bit selects loopback mode.
- 0 Disabled
- 1 Enabled. UTXDx is internally fed back to the receiver.

SYNC Bit 2 Synchronous mode enable
- 0 UART mode
- 1 SPI Mode

MM Bit 1 Multiprocessor mode select
- 0 Idle-line multiprocessor protocol
- 1 Address-bit multiprocessor protocol

SWRST	Bit 0	Software reset enable 0 Disabled. USART reset released for operation 1 Enabled. USART logic held in reset state

U1MCTL, USART Modulation Control Register

7	6	5	4	3	2	1	0
m7	**m6**	**m5**	**m4**	**m3**	**m2**	**m1**	**m0**
rw	rw	rw	rw	rw	rw	rw	rw

UxMCTLx	Bits 7-0	Modulation bits. These bits select the modulation for BRCLK.

U1RCTL, USART Receive Control Register

7	6	5	4	3	2	1	0
FE	**PE**	**OE**	**BRK**	**URXEIE**	**URXWIE**	**RXWAKE**	**RXERR**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

FE	Bit 7	Framing error flag 0 No error 1 Character received with low stop bit
PE	Bit 6	Parity error flag. When PENA = 0, PE is read as 0. 0 No error 1 Character received with parity error
OE	Bit 5	Overrun error flag. This bit is set when a character is transferred into UxRXBUF before the previous character was read. 0 No error 1 Overrun error occurred
BRK	Bit 4	Break detect flag 0 No break condition 1 Break condition occurred
URXEIE	Bit 3	Receive erroneous-character interrupt-enable 0 Erroneous characters rejected and URXIFGx is not set 1 Erroneous characters received set URXIFGx
URXWIE	Bit 2	Receive wake-up interrupt-enable. This bit enables URXIFGx to be set when an address character is received. When URXEIE = 0, an address character does not set URXIFGx if it is received with errors. 0 All received characters set URXIFGx 1 Only received address characters set URXIFGx
RXWAKE	Bit 1	Receive wake-up flag 0 Received character is data 1 Received character is an address
RXERR	Bit 0	Receive error flag. This bit indicates a character was received with error(s). When RXERR = 1, on or more error flags (FE,PE,OE, BRK) is also set. RXERR is cleared when UxRXBUF is read. 0 No receive errors detected 1 Receive error detected

U1RXBUF, USART Receive Buffer Register

7	6	5	4	3	2	1	0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
r	r	r	r	r	r	r	r

UxRXBUFx Bits 7–0 The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UxRXBUF resets the receive-error bits, the RXWAKE bit, and URXIFGx. In 7-bit data mode, UxRXBUF is LSB justified and the MSB is always reset.

U1TCTL, USART Transmit Control Register

7	6	5	4	3	2	1	0
Unused	CKPL	SSELx		URXSE	TXWAKE	Unused	TXEPT
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

Unused Bit 7 Unused

CKPL Bit 6 Clock polarity select
- 0 UCLKI = UCLK
- 1 UCLKI = inverted UCLK

SSELx Bits 5-4 Source select. These bits select the BRCLK source clock.
- 00 UCLKI
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

URXSE Bit 3 UART receive start-edge. The bit enables the UART receive start-edge feature.
- 0 Disabled
- 1 Enabled

TXWAKE Bit 2 Transmitter wake
- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

Unused Bit 1 Unused

TXEPT Bit 0 Transmitter empty flag
- 0 UART is transmitting data and/or data is waiting in UxTXBUF
- 1 Transmitter shift register and UxTXBUF are empty or SWRST = 1

U1TXBUF, USART Transmit Buffer Register

7	6	5	4	3	2	1	0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
rw	rw	rw	rw	rw	rw	rw	rw

UxTXBUFx Bits 7–0 The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UTXDx. Writing to the transmit data buffer clears UTXIFGx. The MSB of UxTXBUF is not used for 7-bit data and is reset.

UCA0ABCT, USCI_A1 Auto Baud Rate Control Register

7	6	5	4	3	2	1	0
Reserved		UCDELIMx		UCSTOE	UCBTOE	Reserved	UCABDEN
r-0	r-0	rw-0	rw-0	rw-0	rw-0	r-0	rw-0

Reserved	Bits 7-6	Reserved
UCDELIMx	Bits 5-4	Break/synch delimiter length 00 1 bit time 01 2 bit times 10 3 bit times 11 4 bit times
UCSTOE	Bit 3	Synch field time out error 0 No error 1 Length of synch field exceeded measurable time.
UCBTOE	Bit 2	Break time out error 0 No error 1 Length of break field exceeded 22 bit times.
Reserved	Bit 1	Reserved
UCABDEN	Bit 0	Automatic baud rate detect enable 0 Baud rate detection disabled. Length of break and synch field is not measured. 1 Baud rate detection enabled. Length of break and synch field is measured and baud rate settings are changed accordingly.

UCA0BR0, USCI_A0 Bit Rate Control Register 0

7	6	5	4	3	2	1	0
UCBRx - low byte							
rw	rw	rw	rw	rw	rw	rw	rw

UCA0BR1, USCI_A0 Bit Rate Control Register 1

7	6	5	4	3	2	1	0
UCBRx - high byte							
rw	rw	rw	rw	rw	rw	rw	rw

UCBRx	Bit clock prescaler setting. The 16-bit value of (UCxxBR0+UCxxBR1×256) form the prescaler value UCBRx.

UCA0CTL0, USCI_A0 Control Register 0

7	6	5	4	3	2	1	0
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEx		UCSYNC=0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN	Bit 7	Parity enable 0 Parity disabled. 1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.
UCPAR	Bit 6	Parity select. UCPAR is not used when parity is disabled. 0 Odd parity 1 Even parity
UCMSB	Bit 5	MSB first select. Controls the direction of the receive and transmit shift register. 0 LSB first 1 MSB first
UC7BIT	Bit 4	Character length. Selects 7-bit or 8-bit character length. 0 8-bit data 1 7-bit data
UCSPB	Bit 3	Stop bit select. Number of stop bits. 0 One stop bit 1 Two stop bits
UCMODEx	Bits 2–1	USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0. 00 UART Mode. 01 Idle-Line Multiprocessor Mode. 10 Address-Bit Multiprocessor Mode. 11 UART Mode with automatic baud rate detection.
UCSYNC	Bit 0	Synchronous mode enable 0 Asynchronous mode 1 Synchronous Mode

UCA0CTL1, USCI_A0 Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx	Bits 7-6	USCI clock source select. These bits select the BRCLK source clock. 00 UCLK 01 ACLK 10 SMCLK 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
0 Erroneous characters rejected and UCAxRXIFG is not set
1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable
0 Received break characters do not set UCAxRXIFG.
1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.
0 Not dormant. All received characters will set UCAxRXIFG.
1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.
0 Next frame transmitted is data
1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.
0 Next frame transmitted is not a break
1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable
0 Disabled. USCI reset released for operation.
1 Enabled. USCI logic held in reset state.

UCA0IRRCTL, USCI_A0 IrDA Receive Control Register

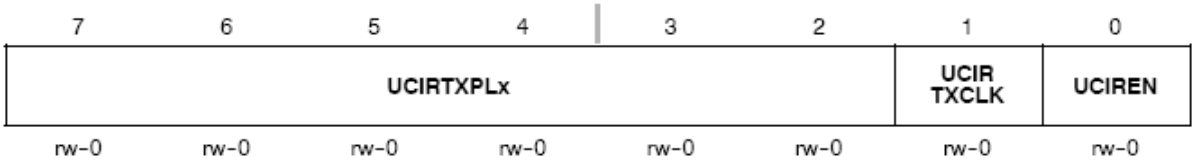
7	6	5	4	3	2	1	0
UCIRRXFLx						UCIRRXPL	UCIRRXFE
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCIRRXFLx Bits 7-2 Receive filter length. The minimum pulse length for receive is given by:
$t_{MIN} = (UCIRRXFLx + 4) / (2 \times f_{BRCLK})$

UCIRRXPL Bit 1 IrDA receive input UCAxRXD polarity
0 IrDA transceiver delivers a high pulse when a light pulse is seen
1 IrDA transceiver delivers a low pulse when a light pulse is seen

UCIRRXFE Bit 0 IrDA receive filter enabled
0 Receive filter disabled
1 Receive filter enabled

UCA0IRTCTL, USCI_A0 IrDA Transmit Control Register



7	6	5	4	3	2	1	0
UCIRTXPLx						UCIR TXCLK	UCIREN
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCIRTXPLx	Bits 7-2	Transmit pulse length Pulse Length t_{PULSE} = (UCIRTXPLx + 1) / (2 × $f_{IRTXCLK}$)
UCIRTXCLK	Bit 1	IrDA transmit pulse clock select 0 BRCLK 1 BITCLK16 when UCOS16 = 1. Otherwise, BRCLK
UCIREN	Bit 0	IrDA encoder/decoder enable. 0 IrDA encoder/decoder disabled 1 IrDA encoder/decoder enabled

UCA0MCTL, USCI_A0 Modulation Control Register

7	6	5	4	3	2	1	0
UCBRFx				UCBRSx			UCOS16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCBRFx	Bits 7-4	First modulation stage select. These bits determine the modulation pattern for BITCLK16 when UCOS16 = 1. Ignored with UCOS16 = 0. Table 19-3 shows the modulation pattern.
UCBRSx	Bits 3-1	Second modulation stage select. These bits determine the modulation pattern for BITCLK. Table 19-2 shows the modulation pattern.
UCOS16	Bit 0	Oversampling mode enabled 0 Disabled 1 Enabled

UCA0RXBUF, USCI_A0 Receive Buffer Register

7	6	5	4	3	2	1	0
UCRXBUFx							
r	r	r	r	r	r	r	r

UCRXBUFx	Bits 7-0	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCAxRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

UCA0STAT, USCI_A0 Status Register

7	6	5	4	3	2	1	0
UCLISTEN	UCFE	UCOE	UCPE	UCBRK	UCRXERR	UCADDR UCIDLE	UCBUSY
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0

UCLISTEN Bit 7 Listen enable. The UCLISTEN bit selects loopback mode.
0 Disabled
1 Enabled. UCAxTXD is internally fed back to the receiver.

UCFE Bit 6 Framing error flag
0 No error
1 Character received with low stop bit

UCOE Bit 5 Overrun error flag. This bit is set when a character is transferred into UCAxRXBUF before the previous character was read. UCOE is cleared automatically when UCxRXBUF is read, and must not be cleared by software. Otherwise, it will not function correctly.
0 No error
1 Overrun error occurred

UCPE Bit 4 Parity error flag. When UCPEN = 0, UCPE is read as 0.
0 No error
1 Character received with parity error

UCBRK Bit 3 Break detect flag
0 No break condition
1 Break condition occurred

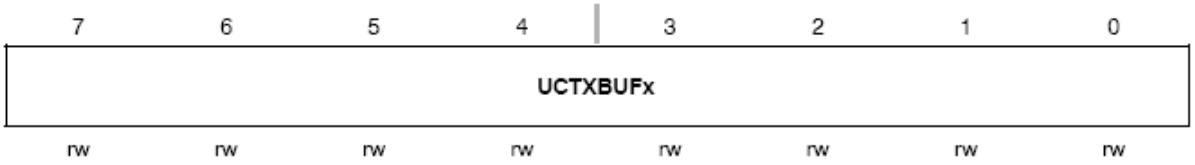
UCRXERR Bit 2 Receive error flag. This bit indicates a character was received with error(s). When UCRXERR = 1, on or more error flags (UCFE, UCPE, UCOE) is also set. UCRXERR is cleared when UCAxRXBUF is read.
0 No receive errors detected
1 Receive error detected

UCADDR Bit 1 Address received in address-bit multiprocessor mode.
0 Received character is data
1 Received character is an address

UCIDLE Idle line detected in idle-line multiprocessor mode.
0 No idle line detected
1 Idle line detected

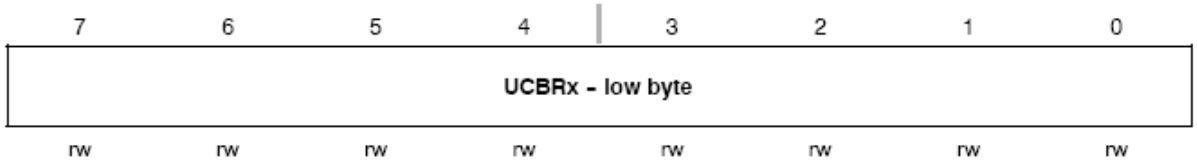
UCBUSY Bit 0 USCI busy. This bit indicates if a transmit or receive operation is in progress.
0 USCI inactive
1 USCI transmitting or receiving

UCA0TXBUF, USCI_A0 Transmit Buffer Register

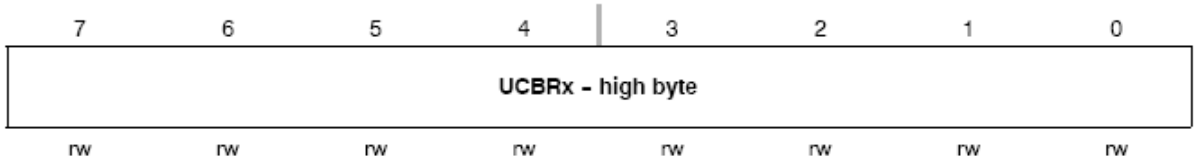


UCTXBUFx	Bits 7-0	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

UCB0BR0, USCI_B0 Baud Rate Control Register 0

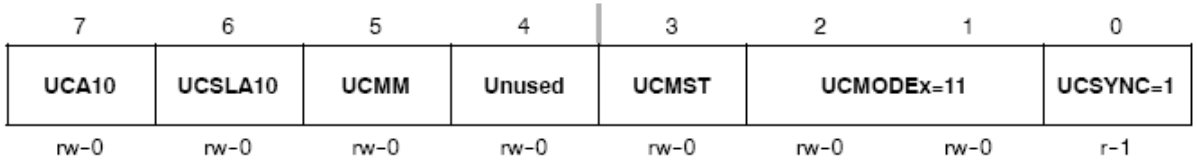


UCB0BR1, USCI_B0 Baud Rate Control Register 1



UCBRx	Bit clock prescaler setting. The 16-bit value of (UCxxBR0+UCxxBR1×256) form the prescaler value UCBRx.

UCB0CTL0, USCI_B0 Control Register 0



UCA10	Bit 7	Own addressing mode select 0 Own address is a 7-bit address 1 Own address is a 10-bit address
UCSLA10	Bit 6	Slave addressing mode select 0 Address slave with 7-bit address 1 Address slave with 10-bit address
UCMM	Bit 5	Multi-master environment select 0 Single master environment. There is no other master in the system. The address compare unit is disabled. 1 Multi master environment
Unused	Bit 4	Unused

UCMST	Bit 3	Master mode select. When a master looses arbitration in a multi-master environment (UCMM = 1) the UCMST bit is automatically cleared and the module acts as slave. 0 Slave mode 1 Master mode
UCMODEx	Bits 2-1	USCI Mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1. 00 3-pin SPI 01 4-Pin SPI (master/slave enabled if STE = 1) 10 4-Pin SPI (master/slave enabled if STE = 0) 11 I^2C mode
UCSYNC	Bit 0	Synchronous mode enable 0 Asynchronous mode 1 Synchronous mode

UCB0CTL1, USCI_B0 Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**Unused**	**UCTR**	**UCTXNACK**	**UCTXSTP**	**UCTXSTT**	**UCSWRST**
rw-0	rw-0	r0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx	Bits 7-6	USCI clock source select. These bits select the BRCLK source clock. 00 UCLKI 01 ACLK 10 SMCLK 11 SMCLK
Unused	Bit 5	Unused
UCTR	Bit 4	Transmitter/Receiver 0 Receiver 1 Transmitter
UCTXNACK	Bit 3	Transmit a NACK. UCTXNACK is automatically cleared after a NACK is transmitted. 0 Acknowledge normally 1 Generate NACK
UCTXSTP	Bit 2	Transmit STOP condition in master mode. Ignored in slave mode. In master receiver mode the STOP condition is preceded by a NACK. UCTXSTP is automatically cleared after STOP is generated. 0 No STOP generated 1 Generate STOP
UCTXSTT	Bit 1	Transmit START condition in master mode. Ignored in slave mode. In master receiver mode a repeated START condition is preceded by a NACK. UCTXSTT is automatically cleared after START condition and address information is transmitted. Ignored in slave mode. 0 Do not generate START condition 1 Generate START condition
UCSWRST	Bit 0	Software reset enable 0 Disabled. USCI reset released for operation. 1 Enabled. USCI logic held in reset state.

UCB0I2CIE, USCI_B0 I²C Interrupt Enable Register

7	6	5	4	3	2	1	0
Reserved				UCNACKIE	UCSTPIE	UCSTTIE	UCALIE
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Reserved	Bits 7-4	Reserved
UCNACKIE	Bit 3	Not-acknowledge interrupt enable 0 Interrupt disabled 1 Interrupt enabled
UCSTPIE	Bit 2	Stop condition interrupt enable 0 Interrupt disabled 1 Interrupt enabled
UCSTTIE	Bit 1	Start condition interrupt enable 0 Interrupt disabled 1 Interrupt enabled
UCALIE	Bit 0	Arbitration lost interrupt enable 0 Interrupt disabled 1 Interrupt enabled

UCB0I2COA, USCI_B0 I²C Own Address Register

15	14	13	12	11	10	9	8
UCGCEN	0	0	0	0	0	I2COAx	
rw-0	r0	r0	r0	r0	r0	rw-0	rw-0

7	6	5	4	3	2	1	0
I2COAx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCGCEN	Bit 15	General call response enable 0 Do not respond to a general call 1 Respond to a general call
I2COAx	Bits 9-0	I²C own address. The I2COAx bits contain the local address of the USCI_Bx I²C controller. The address is right-justified. In 7-bit addressing mode Bit 6 is the MSB, Bits 9-7 are ignored. In 10-bit addressing mode Bit 9 is the MSB.

UCB0I2CSA, USCI_B0 I²C Slave Address Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	I2CSAx	
r0	r0	r0	r0	r0	r0	rw-0	rw-0

7	6	5	4	3	2	1	0
I2CSAx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

I2CSAx Bits 9-0 I²C slave address. The I2CSAx bits contain the slave address of the external device to be addressed by the USCI_Bx module. It is only used in master mode. The address is right-justified. In 7-bit slave addressing mode Bit 6 is the MSB, Bits 9-7 are ignored. In 10-bit slave addressing mode Bit 9 is the MSB.

UCB0RXBUF, USCI_B0 Receive Buffer Register

7	6	5	4	3	2	1	0
UCRXBUFx							
r	r	r	r	r	r	r	r

UCRXBUFx Bits 7-0 The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCBxRXBUF resets UCBxRXIFG.

UCB0STAT, USCI_B0 Status Register

7	6	5	4	3	2	1	0
Unused	UC SCLLOW	UCGC	UCBBUSY	UCNACK IFG	UCSTPIFG	UCSTTIFG	UCALIFG
rw-0	r-0	rw-0	r-0	rw-0	rw-0	rw-0	rw-0

Unused Bit 7 Unused.

UC SCLLOW Bit 6 SCL low
- 0 SCL is not held low
- 1 SCL is held low

UCGC Bit 5 General call address received. UCGC is automatically cleared when a START condition is received.
- 0 No general call address received
- 1 General call address received

UCBBUSY Bit 4 Bus busy
- 0 Bus inactive
- 1 Bus busy

UCNACKIFG	Bit 3	Not-acknowledge received interrupt flag. UCNACKIFG is automatically cleared when a START condition is received. 0 No interrupt pending 1 Interrupt pending
UCSTPIFG	Bit 2	Stop condition interrupt flag. UCSTPIFG is automatically cleared when a START condition is received. 0 No interrupt pending 1 Interrupt pending
UCSTTIFG	Bit 1	Start condition interrupt flag. UCSTTIFG is automatically cleared if a STOP condition is received. 0 No interrupt pending 1 Interrupt pending
UCALIFG	Bit 0	Arbitration lost interrupt flag 0 No interrupt pending 1 Interrupt pending

UCB0TXBUF, USCI_B0 Transmit Buffer Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx	Bits 7-0	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCBxTXIFG.

WDTCTL, Watchdog Timer Control Register

15	14	13	12	11	10	9	8
WDTPW **Reads as 069h** **Must be written as 05Ah**							

7	6	5	4	3	2	1	0
WDTHOLD	**WDTNMIES**	**WDTNMI**	**WDTTMSEL**	**WDTCNTCL**	**WDTSSEL**	**WDTISx**	
rw-0	rw-0	rw-0	rw-0	r0(w)	rw-0	rw-0	rw-0

WDTPW	Bits 15-8	Watchdog timer password. Always read as 069h. Must be written as 05Ah, or a PUC is generated.
WDTHOLD	Bit 7	Watchdog timer hold. This bit stops the watchdog timer. Setting WDTHOLD = 1 when the WDT is not in use conserves power. 0 Watchdog timer is not stopped 1 Watchdog timer is stopped

WDTNMIES	Bit 6	Watchdog timer NMI edge select. This bit selects the interrupt edge for the NMI interrupt when WDTNMI = 1. Modifying this bit can trigger an NMI. Modify this bit when WDTNMI = 0 to avoid triggering an accidental NMI. 0 NMI on rising edge 1 NMI on falling edge
WDTNMI	Bit 5	Watchdog timer NMI select. This bit selects the function for the $\overline{\text{RST}}$/NMI pin. 0 Reset function 1 NMI function
WDTTMSEL	Bit 4	Watchdog timer mode select 0 Watchdog mode 1 Interval timer mode
WDTCNTCL	Bit 3	Watchdog timer counter clear. Setting WDTCNTCL = 1 clears the count value to 0000h. WDTCNTCL is automatically reset. 0 No action 1 WDTCNT = 0000h
WDTSSEL	Bit 2	Watchdog timer clock source select 0 SMCLK 1 ACLK
WDTISx	Bits 1-0	Watchdog timer interval select. These bits select the watchdog timer interval to set the WDTIFG flag and/or generate a PUC. 00 Watchdog clock source / 32768 01 Watchdog clock source / 8192 10 Watchdog clock source / 512 11 Watchdog clock source / 64

6. References

This programming reference is a compilation of information provided by Texas Instruments in various datasheets, user guides, and application notes.

[1] TI, “MSP430xG461x Mixed Signal Microcontroller,” Oct. 2007.

[2] TI, “MSP430x4xx Family User's Guide (SLAU056H),” Apr. 2009.

[3] TI, “MSP430FG4618/F2013 Experimenter's Board User's Guide (SLAU213A),” Oct. 2007.