

The diagram illustrates a serial transmitter circuit. It consists of several key components and their interconnections:

- Shift Register (8-bit):** Receives data from the SW input and shifts it out to the txdata output. It is loaded by tx\_en and clocked by clk0. Its reset is connected to the RST input of the byte counter.
- Byte Counter (8):** Counts the number of bytes transmitted. It is reset by the RST input and clocked by clk0. When it reaches 8, it outputs a signal labeled "Byte Done".
- Flag Counter (5):** Counts the number of flags transmitted. It is reset by the RST input and clocked by clk0. When it reaches 5, it outputs a signal labeled "Z5".
- Data Register (8-bit):** Receives data from the txdata output and shifts it out to the txd output. It is loaded by tx\_en and clocked by clk0. Its reset is connected to the RST input of the byte counter.
- Control Logic:** The txdata output is also connected to the txcl output. The txcl output is connected to the RST input of the byte counter. The txd output is connected to the txcl output.