Experiment 3

Part 1 (5 points)

Implement a generic k x k bit unsigned multiplier using the following three designs:

A. combinational multiplier, implemented in VHDL using a * operator

B. combinational array multiplier, shown in Figs. 1a and 1b (diagram for k=5)

C. pipelined array multiplier shown in Figs. 2a and 2b (diagram for k=5).

Optimize multipliers A and B for the minimum product of latency times area.

Optimize multiplier C for the maximum throughput to area ratio.

In both cases, assume that area is expressed in the number of CLB slices.

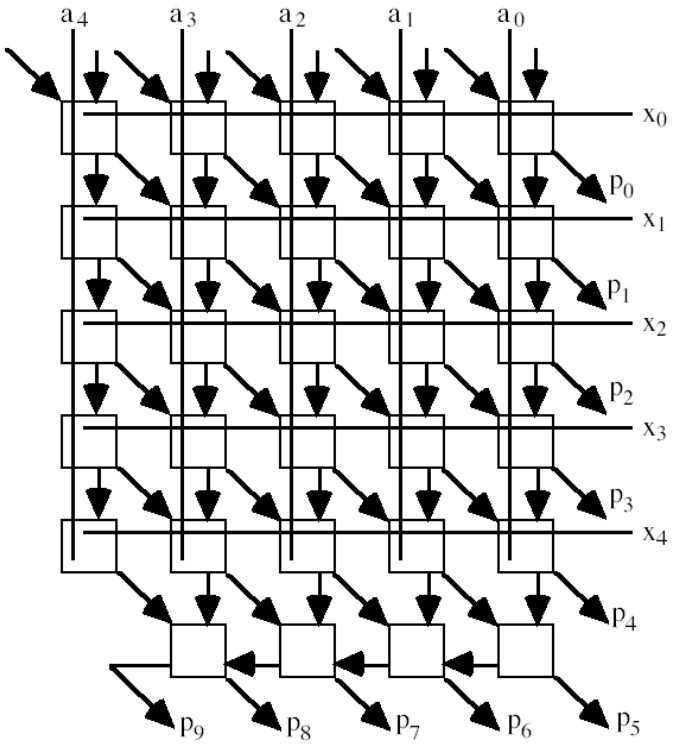

Fig. 1a. Combinational Array Multiplier (for k=5)

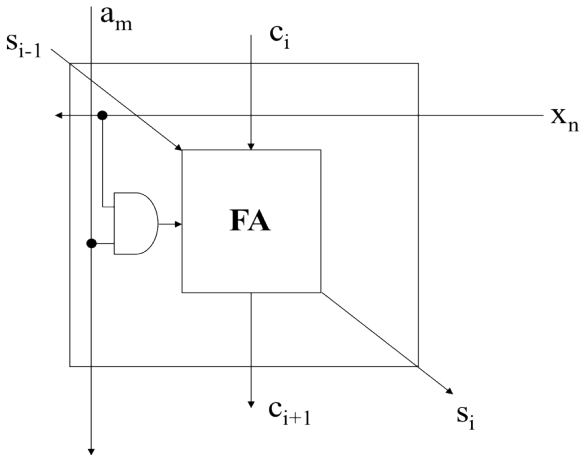

Fig. 1b Basic Cell of the Combinational Array Multiplier

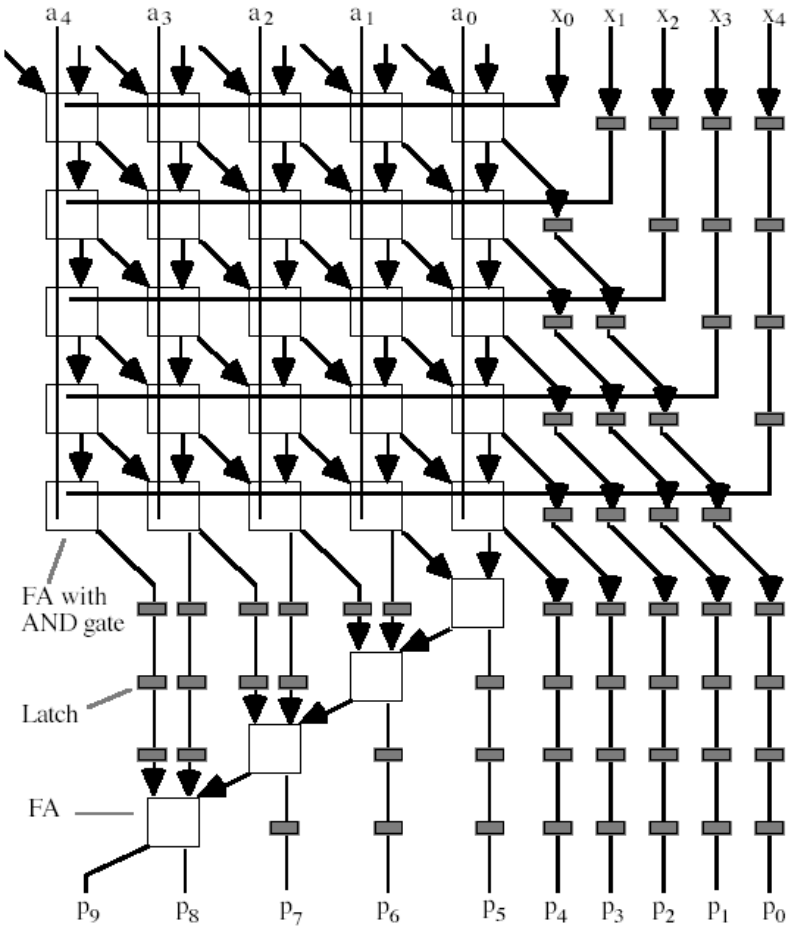

Fig. 2a. Pipelined Array Multiplier (for k=5)

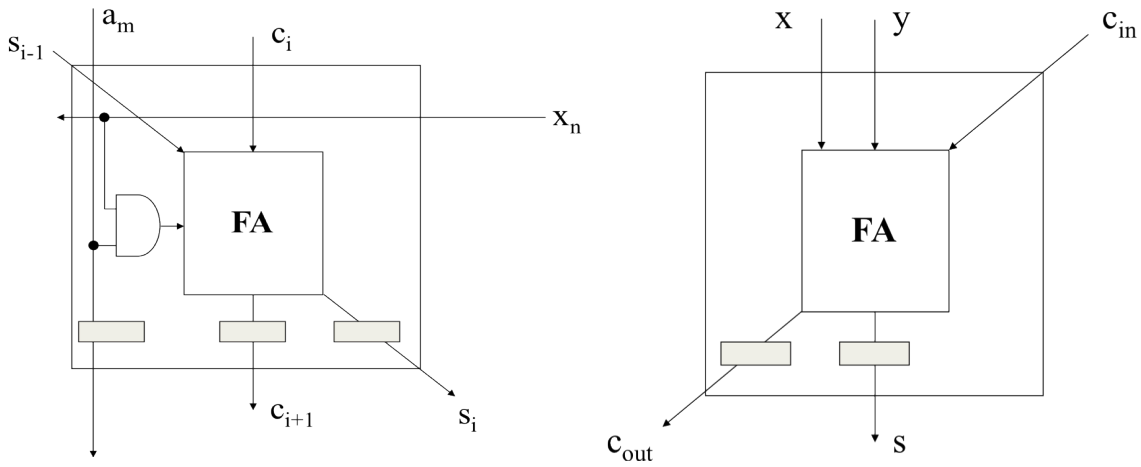

Fig. 2b Basic Cells of the Pipelined Array Multiplier

Verify your design using a comprehensive testbench, using design A as a reference implementation.

Synthesize and implement designs A, B, C, using FPGA Design Flow Based on Aldec Active-HDL, for the following values of the parameter k:

a. k=32
b. k=64
c. k=128

For each case, choose the smallest device of the Spartan 3E family capable of implementing a given multiplier with the resource utilization not exceeding 80%. In case, all Spartan 3E devices are too small to fit a given multiplier, choose an appropriate Virtex 4 FPGA instead.

For each multiplier, and each value of the parameter k, determine the following properties:

1. number of CLB slices
2. number of embedded multipliers (if any)
3. minimum clock period after synthesis [ns]
4. maximum clock frequency after synthesis [MHz]
5. minimum clock period after implementation [ns]
6. maximum clock frequency after implementation [MHz]
7. minimum latency after implementation [ns]
8. maximum throughput after implementation [multiplications/s]
9. latency * area (minimum latency after implementation * number of CLB slices)
10. throughput / area (maximum throughput after implementation / number of CLB slices).

Part 2 (2 bonus points)

Implement the following two multipliers

a. combinational k x k multiplier
b. pipelined k x k multiplier

using embedded multipliers of Xilinx FPGAs.

Synthesize and implement your designs using FPGA Design Flow Based on Aldec Active-HDL, for the following values of the parameter k:

a. k = 32
b. k = 64
c. k = 128.

For each case, choose the smallest device of the Spartan 3E family capable of implementing a given multiplier with the resource utilizations (for CLB slices and embedded multipliers) not exceeding 80%. In case, all Spartan 3E devices are too small to fit a given multiplier, choose an appropriate Virtex 4 FPGA instead.

Characterize all your designs using properties described in Part 1, and compare implementations based on CLB slices (developed in Part 1) vs. implementations based on embedded multipliers (developed in Part 2).

Important Dates

	Monday section	Tuesday section	Wednesday section	Thursday section
Hands-on Session and Introduction to the Experiment	02/15/2010	02/16/2010	02/17/2010	02/18/2010
Demonstration and Deliverables Due	**02/22/2010**	**02/23/2010**	**02/24/2010**	**02/25/2010**