ECEN 468 – Lab Report

Lab Number: 1

Lab Title: SystemC and Simulator

Section Number: 503

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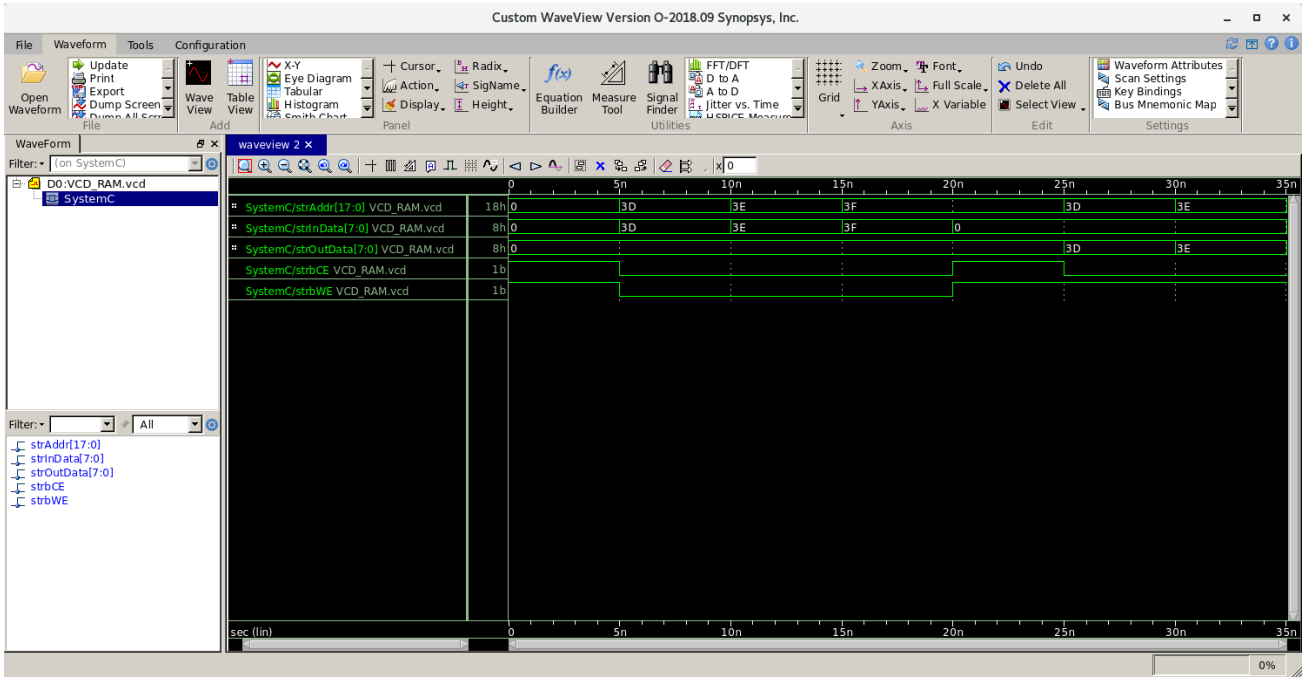
1. Screenshots of the waveform with analysis



From 0 ns to 5 ns, the testbench is in initialization state with bCE is 1 indicate that all address bins are disabled.

From 5 ns to 10ns, bCE and bWE are 0 which indicate the Write Operation, so 3D is written to address 3D

From 10 ns to 15ns, bCE and bWE are 0 which indicate the Write Operation, so 3F is written to address 3F

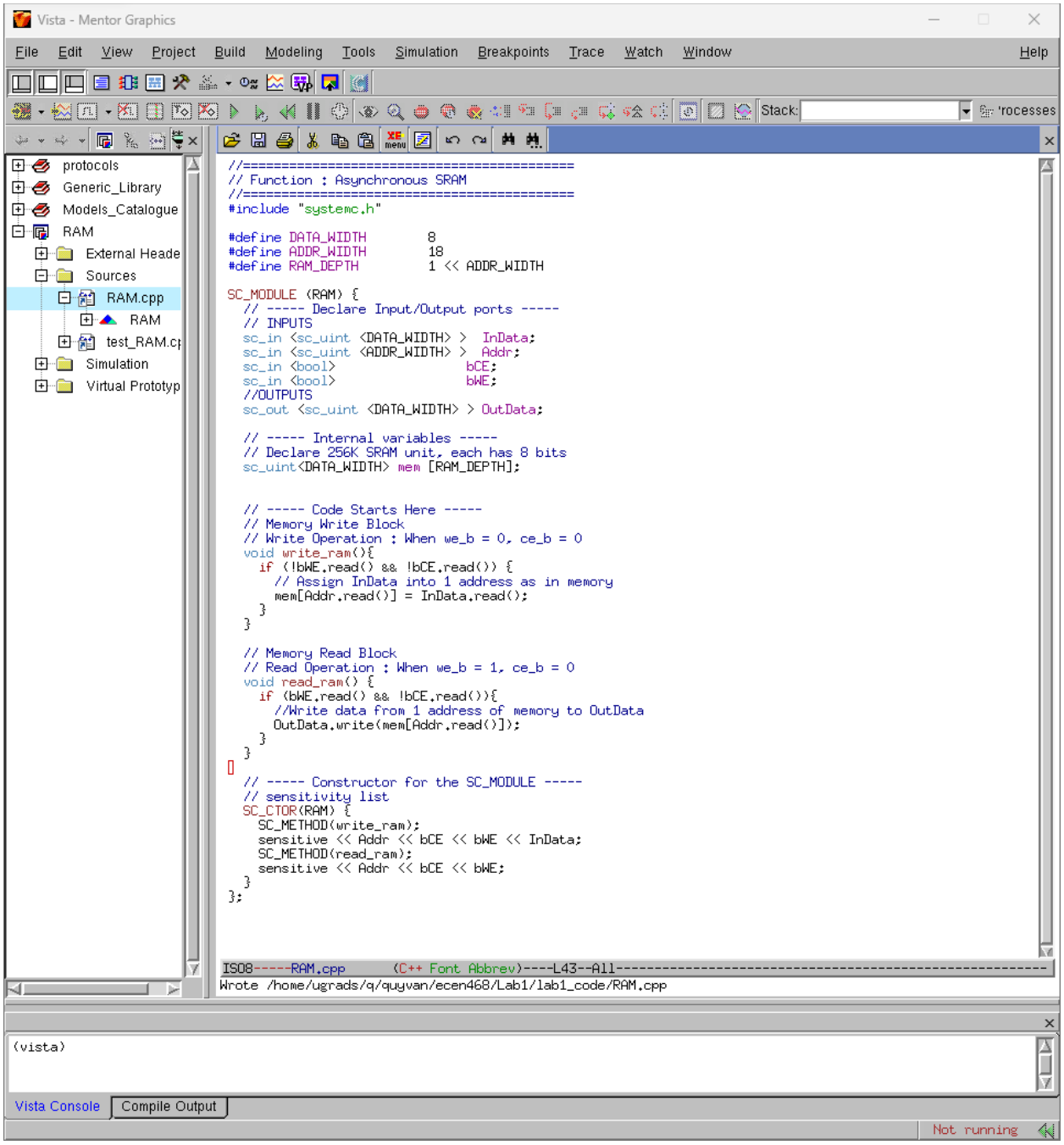
From 15 ns to 20ns, bCE and bWE are 0 which indicate the Write Operation, so 3E is written to address 3E

From 20 ns to 25 ns, bCE is 1, so all addresses bin are disabled, so InData = 0 does not take any action.

From 25 ns to 30 ns, bCE = 0 and bWE = 1 operate Read. OutData read data from address 3D then return 3D which was stored in that address from 5 ns → 10 ns

From 30 ns to 35 ns, bCE = 0 and bWE = 1 operate Read. OutData read data from address 3E then return 3E which was stored in that address from 10 ns → 15 ns

2. Screenshots of your code in this design with reasonable comments



3. What are the differences between asynchronous and synchronous SRAM?

- Synchronous SRAM has clock while asynchronous does not.
- Synchronous SRAM will only read or write as a designated clock (usually positive edge clock or negative edge clock).
- Asynchronous SRAM does not have clock, so it can read or write as soon as control signal for write or read is enabled.
- Synchronous SRAM also has additional registers to store the previous signal every clock edge.