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January 2015

FDBL86561_F085

N-Channel PowerTrench[®] MOSFET 60 V, 300 A, 1.1 m Ω

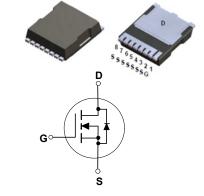
Features

- Typical $R_{DS(on)}$ = 0.85 m Ω at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{q(tot)}$ = 170 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems





For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/packing_dwg/PKG-PSOF08A.pdf

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain-to-Source Voltage		60	V	
V_{GS}	Gate-to-Source Voltage		±20	V	
	Drain Current - Continuous (V_{GS} =10) (Note 1) T_C = 25°C		300		
ID	Pulsed Drain Current T _C = 25°C		See Figure 4	Α	
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	1167	mJ	
D	Power Dissipation		429	W	
P_D	Derate Above 25°C		2.86	W/°C	
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.35	°C/W	
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		43	°C/W	

Notes

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25$ °C, L = 0.57mH, $I_{AS} = 64$ A, $V_{DD} = 40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package			
FDBL86561	FDBL86561_F085	MO-299A	-	-	-

Units

Max.

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Parameter

Off Ch	Off Characteristics						
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250μA, V _{GS} =	0V 60	-	-	V	
	Drain to Source Leakage Current	$V_{DS} = 60V T_{J} = 3$	25°C -	-	1	μА	
I _{DSS} Drain-to-Source Leakage Current		$V_{GS} = 0V$ $T_J = 0$	175°C (Note 4) -	-	3	mA	
I _{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA	

Test Conditions

Min.

Тур.

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	3.0	4.0	V
Drain to Source On Booist	Drain to Source On Resistance	I _D = 80A,	$T_J = 25^{\circ}C$	-	0.85	1.1	$m\Omega$
CDS(on)	R _{DS(on)} Drain to Source On Resistance	V _{GS} = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	1.5	2.2	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	.,	V _{DS} = 30V, V _{GS} = 0V, f = 1MHz		13650	-	pF
C _{oss}	Output Capacitance				3375	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			255	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.3	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	V _{DD} = 48V	-	170	220	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I _D = 80A	-	24	32	nC
Q_{gs}	Gate-to-Source Gate Charge		_	-	56	-	nC
Q _{qd}	Gate-to-Drain "Miller" Charge			-	24	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	137	ns
t _{d(on)}	Turn-On Delay		-	45	-	ns
t _r	Rise Time	V _{DD} = 30V, I _D = 80A,	-	61	-	ns
t _{d(off)}	Turn-Off Delay	$V_{DD} = 30V, I_{D} = 80A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	-	80	-	ns
t _f	Fall Time		-	41	-	ns
t _{off}	Turn-Off Time		-	-	156	ns

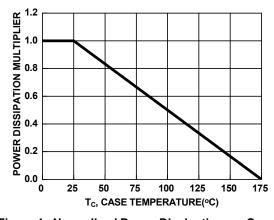
Drain-Source Diode Characteristics

V	Source-to-Drain Diode Voltage	I _{SD} =80A, V _{GS} = 0V	-	-	1.25	V
V _{SD} Source-to-Drain Diode Voltage		$I_{SD} = 40A, V_{GS} = 0V$	-	-	1.2	V
t _{rr}	Reverse-Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	107	139	ns
Q _{rr}	Reverse-Recovery Charge	V _{DD} =48V	-	183	265	nC

Note

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics



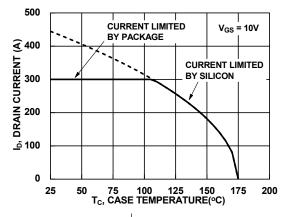
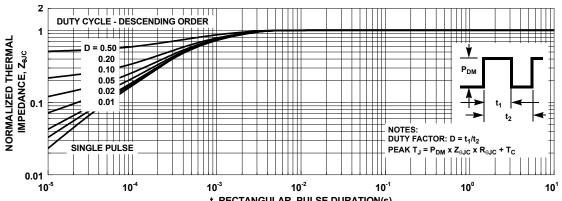


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs. Case Temperature



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Figure 3. Normalized Maximum Transient Thermal Impedance

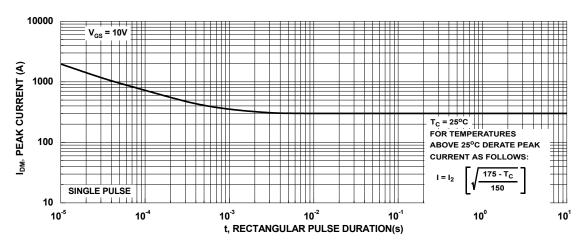


Figure 4. Peak Current Capability

Typical Characteristics

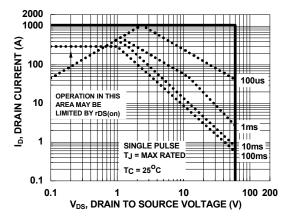
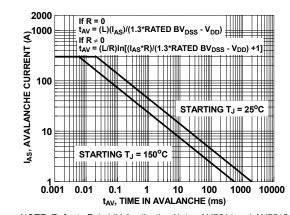


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

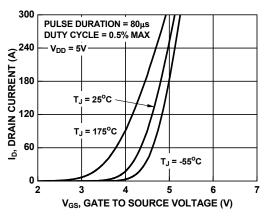


Figure 7. Transfer Characteristics

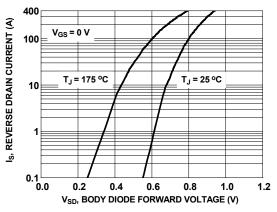


Figure 8. Forward Diode Characteristics

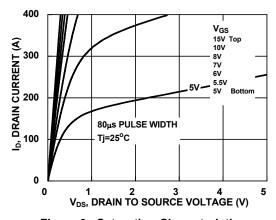


Figure 9. Saturation Characteristics

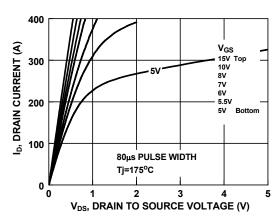


Figure 10. Saturation Characteristics

Typical Characteristics

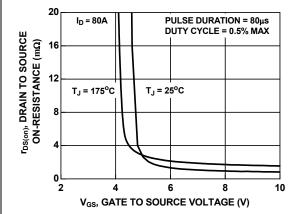


Figure 11. R_{DSON} vs. Gate Voltage

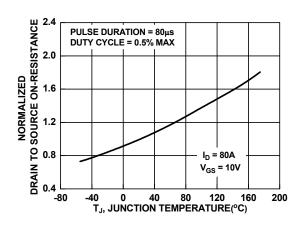


Figure 12. Normalized R_{DSON} vs. Junction Temperature

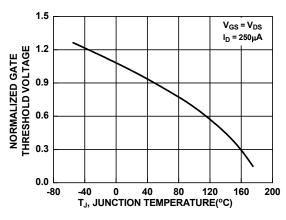


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

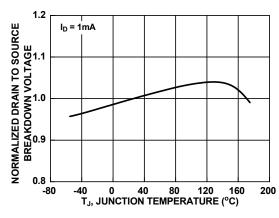


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

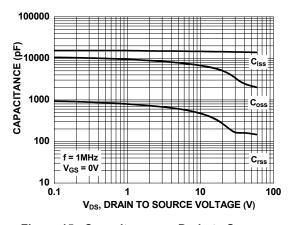


Figure 15. Capacitance vs. Drain to Source Voltage

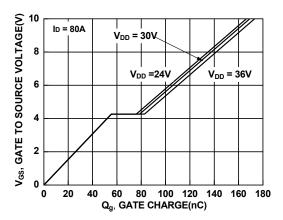


Figure 16. Gate Charge vs. Gate to Source Voltage





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