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The Significance of an In Situ ALD Al$_2$O$_3$ Stacked Structure for p-Type SnO TFT Performance and Monolithic All-ALD-Channel CMOS Inverter Applications

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Tin monoxide (SnO) has been studied widely over the past several decades due to its promising theoretical p-type performance. However, limited fabrication processes due to the low thermal and air stability of SnO have resulted in poor performance in thin-film transistors (TFTs). Here, it is suggested that in situ atomic layer deposition (ALD) of an Al$_2$O$_3$ capping layer can improve the electrical performance in SnO TFTs. By adopting an in situ stacking process, which protects vulnerable SnO thin films from exposure to air and contamination, SnO exhibits enhanced crystallinity, electrical performance, and improved scaling limitation of channel thickness. Especially, in situ stacked Al$_2$O$_3$ on a 7 nm SnO TFT has an exceptionally low subthreshold swing (0.15 V decade^{-1}), high on/off ratio (6.54 × 10^5), and reasonable mobility (1.14 cm^2 V^{-1} s^{-1}) while the bare SnO TFT is not activated. Computational thermodynamics such as chemical potential analysis, nucleation Gibbs free-energy calculations, and various analytical techniques are used to reveal the origin of highly crystallized SnO formations via in situ deposition of Al$_2$O$_3$. Finally, state-of-the-art all-ALD-channel complementary metal–oxide–semiconductor inverters using n-type indium gallium zinc oxide and p-type SnO TFTs are integrated, which exhibit a maximum voltage gain of 240 V V^{-1} and a noise margin of 89.3%.

1. Introduction

Since the first demonstration of amorphous indium gallium zinc oxide (a-IGZO) by Nomura et al. (2004), interest in oxide semiconductors has increased dramatically, particularly among researchers studying thin-film transistors (TFTs).[1] The high mobility (≈10 cm^2 V^{-1} s^{-1}), low off-current (<10^{-12} A), and high uniformity of a-IGZO TFT have led to commercially viable flat-panel displays as active-matrix backplanes. Nowadays, with continuous scaling down requirements, studies of complementary metal–oxide–semiconductor (CMOS) technology and 3D devices such as fin, gate-all-around (GAA), and channel-all-around (CAA) structured field-effect transistors (FET) have increased.[2–4] Oxide semiconductors draw attention to the possibilities of logic-inverter devices and integration of gate-driver circuits with high on-current capabilities and large-area applicability beyond those of traditional silicon semiconductors.[5] Despite a lack of studies for comparable performance in p-type oxide semiconductor devices, CMOS inverter fabrication with both n- and p-type oxide semiconductors is highly demanded than unipolar-based devices due to superior performance, including low power consumption, low noise immunity, and a small device unit area, compared with unipolar devices when device scaled down.[5–10]

The current generation of p-type oxide semiconductors is underperforming n-type oxide semiconductors by significant margins. Valence-band maximum (VBM) consists of the highly localized and anisotropic hole conduction paths in p-type oxide semiconductors, which leads to inferior hole mobility. Due to these characteristics, both delocalization of a VBM orbital and low formation energy of metal vacancies are needed for a p-type oxide semiconductor to alleviate the localized hole conduction path and achieve sufficient electrical performance.[11] Among the various reported candidates, tin monoxide (SnO) is a promising option which has the low formation energy of a tin vacancy (V_{Sn}), delocalization of hole conduction paths by orbital hybridization of oxygen 2p and tin 5s orbitals, and subsequent high hole mobility and hole concentrations.[12,13] However, obtaining high-quality SnO is not a simple issue due to its low thermal stability and facile oxidation to SnO$_2$, which exhibits n-type performance. Various deposition processes, such as

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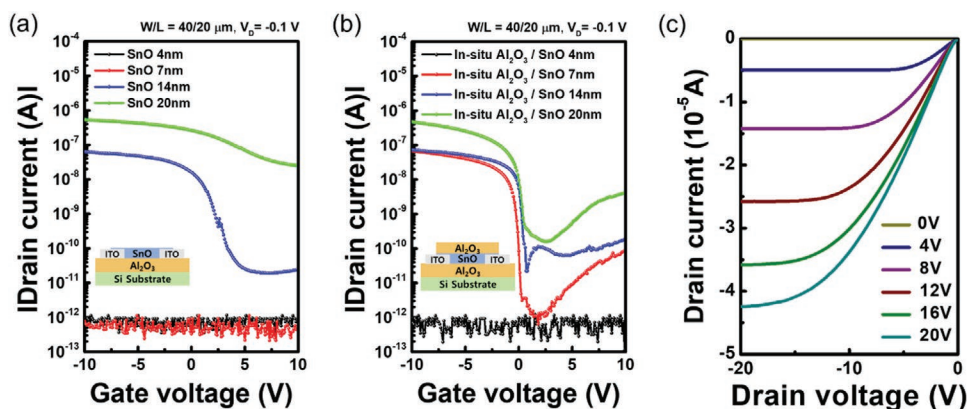206 Worldcup-ro, Yeongtong-gu, Suwon 16499, Republic of Korea

Figure 1. a) Transfer curves of bare SnO and b) in situ stacked Al_2O_3/SnO TFTs depending on SnO film thicknesses. c) An output curve of an in situ stacked Al_2O_3/7 nm SnO TFT.

physical vapor deposition (PVD),[13–18] liquid-metal printing,[19] and atomic layer deposition (ALD)[20–23] have been proposed. However, the high subthreshold swing (S-value), inadequate threshold voltage (V_{th}) or stability induced by large defect sites and phase mixing,[18,24] and limited surface coverage of conventional processes can hinder the production of high-quality SnO thin films and limit the process windows.

Among these obstacles, air and thermal stability are crucial factors for development of practical SnO devices. Our previous research revealed that ALD, highly desired fabrication process in scalability to practical applications, is quite effective tool to fabricate SnO but the surface region is oxidized to SnO_2 which can induce high off-current and/or ambipolar characteristics, resulting in degradation of p-type performance.[25] Especially, when channel thickness is scaled down, such effects can be critical to device performance. Thereby, precise control to protect SnO from external deterioration and achieve better TFT performance, reliability, and scaling down by versatile process is required. Recently, various passivation layers have been adopted to passivate surface defect states of SnO and enhance TFT performance and air stability.[21,26–28] However, those processes still include inevitable air exposure and contamination between deposition processes. Also, the mechanism of improvement in SnO TFT performances by passivation has yet to be determined.

In this study, we demonstrate that versatile process of stable, scaled-down, and defect-less SnO TFT via in situ ALD stacking process of SnO with a Al_2O_3 passivation layer. This suggested method can enhance the electrical performance of SnO and scaling down of channel thickness by fundamental exclusion of SnO surfaces from air deterioration or contamination. We fabricated high-performance TFTs using an in situ process for Al_2O_3 deposition on 7 nm of SnO, which exhibits an exceedingly low S-value (0.15 ± 0.02 V decade^{-1}), a high on/off ratio ($I_{on/off}$, 6.54×10^5), superior V_{th} (0.10 ± 0.03 V) and field-effect mobility (μ_{FE}, 1.14 ± 0.08 cm^2 V^{-1} s^{-1}). Also, we figured out highly crystallized p-type SnO with very low defect states is fabricated during in situ stacking process. Various analytical tools are exploited to reveal the correlation of film properties with TFT electrical performance depending on fabrication process, and the crystallization mechanism is interpreted according to first-principles thermodynamics. In addition, a CMOS inverter

using all ALD-deposited channel layer using this SnO TFT exhibited a state-of-the-art performance in terms of ALD fabrication process, voltage gain of 240 V V^{-1}, and noise margin of 89% of supply voltage.

2. Results and Discussion

2.1. Electrical Properties of Bare SnO and In Situ Stacked Al_2O_3/SnO TFTs

We investigated the scaling limitation of channel thickness on SnO TFTs and compared the structural effect of an in situ Al_2O_3 capping layer. Transfer characteristics of TFTs are presented in **Figure 1** and electrical parameters in **Table 1**. Figure 1a depicts the transfer curve of bare SnO TFTs without a capping layer, and Figure 1b shows the transfer curve of SnO TFTs with an in situ stacked Al_2O_3 capping layer and channel thicknesses from 4 to 20 nm. When Al_2O_3 was deposited by an in situ process (Figure 1 and Table 1), V_{th} shifted considerably in the negative direction, μ_{FE} was slightly decreased, and S-value was greatly enhanced. Generally, V_{th} and μ_{FE} are closely related to carrier density or charged defect sites,[29] and the S-value depends on internal and interfacial defect sites.[30,31] This implies that in situ Al_2O_3 passivation process is effective for passivating defect sites such as tin vacancies or oxygen-related defects in the back-channel region. On the other hand, interestingly, scaling limitations depend heavily on the existence of in situ Al_2O_3 stacked structures. In Figure 1a,b, transfer characteristics exist up to 14 nm in bare SnO TFTs and to 7 nm in in situ stacked Al_2O_3/SnO TFTs. Thicknesses less than 7 nm in bare SnO and 4 nm in in situ stacked Al_2O_3/SnO TFTs are not activated and exhibit insulating properties, which indicate a channel-thickness dependency and a scaling limitation of the two devices. In both conditions, the insulating behavior of 4-nm SnO TFT can be attributed to a decrease in carrier concentration under accumulation thickness and structural defects induced from bulk and interface defects, surface oxidation, and deterioration.[31] However, 7 nm SnO TFTs exhibit far different characteristics: bare SnO one is insulating, and in situ stacked SnO has optimal transfer curves in V_{th}, off-current, and S-value. In situ stacking process therefore not only passivates back-channel

Table 1. TFT parameters of bare SnO and in situ stacked Al$_2$O$_3$/SnO TFTs with different SnO thicknesses.

SnO thickness [nm]	V_{th} [V]		μ_{FE} [cm^2 V^{-1} s^{-1}]		S-value [V decade^{-1}]		I_{on}/I_{off}		D_{it} [cm^{-2}]	
	SnO	In situ Al$_2$O$_3$	SnO	In situ Al$_2$O$_3$	SnO	In situ Al$_2$O$_3$	SnO	In situ Al$_2$O$_3$	SnO	In situ Al$_2$O$_3$
4	N/D	N/D	N/D	N/D	N/D	N/D	N/D	N/D	N/D	N/D
7	N/D	0.06 ± 0.03	N/D	1.14 ± 0.08	N/D	0.15 ± 0.02	N/D	6.54 × 10^5	N/D	6.72 × 10^{11}
14	3.12 ± 0.70	1.10 ± 0.12	1.71 ± 0.20	1.23 ± 0.12	2.79 ± 0.05	0.25 ± 0.10	5.16 × 10^3	8.42 × 10^3	8.02 × 10^{12}	1.12 × 10^{12}
20	7.83 ± 0.85	1.18 ± 0.20	3.83 ± 0.20	3.49 ± 0.22	5.38 ± 0.31	0.28 ± 0.03	2.16 × 10	2.98 × 10^3	3.95 × 10^{13}	1.64 × 10^{12}

regions and protects SnO from the air but may also alleviate structural defects in the bulk/interface region and expand scaling limitations. Details of this phenomenon are discussed in the following paragraph and later part in this manuscript using various film analysis tools and calculations.

To identify the differences between the two devices, we investigated the thickness dependencies and electrical parameters of TFTs. When the channel thickness was decreased, (Figure 1 and Table 1), μ_{FE} also decreased (3.83 to 1.71 cm^2 V^{-1} s^{-1}), as did V_{th} and S-value (from 7.83 to 3.12 V and from 5.38 to 2.79 V decade^{-1}, respectively), while $I_{on/off}$ increased (2.16 × 10 to 5.16 × 10^3). This tendency was maintained for in situ stacked Al$_2$O$_3$/SnO TFT (μ_{FE} decreased from 3.49 to 1.14 cm^2 V^{-1} s^{-1}, V_{th} from 1.18 to 0.06 V, S-value from 0.28 to 0.15 V decade^{-1}, and $I_{on/off}$ increased from 2.98 × 10^3 to 6.54 × 10^5). The thickness dependencies of the S-value and V_{th} mean that trap-state density was reduced in thinner SnO channel layers.[21] However, the decline of μ_{FE} according to channel thickness has yet to be clearly identified and may result from the microstructure of SnO: grain size, orientation, and crystallinity.[32] As discussed previously, with an in situ Al$_2$O$_3$ passivation layer, the SnO channel length can be further scaled down to 7 nm while retaining robust TFT characteristics. Compared with bare SnO TFTs, in situ stacked Al$_2$O$_3$/SnO TFTs exhibited far more dramatic enhancements, particularly with respect to S-value and V_{th}, with adequate μ_{FE}. Moreover, in situ stacked Al$_2$O$_3$/7 nm SnO TFT, exhibits outstanding performance: 0.06 V of V_{th}, 1.14 cm^2 V^{-1} s^{-1} of μ_{FE}, 0.15 V decade^{-1} of S-value, and 6.54 × 10^5 of $I_{on/off}$, while bare SnO TFT was not activated. This exceedingly low S-value was far lower than that reported for ALD SnO TFTs[21,23,25,33] and even comparable to that of SnO TFTs with a gate insulator with a high dielectric constant, such as HfO$_2$.[34–36] This is noticeable because the S-value is related to the capacitance of the gate insulator layer and trap states in the depletion layer. Also, superb switching performance with very low V_{th}, we could deduce an in situ stacked Al$_2$O$_3$/SnO TFT has a low trap-state density in the channel layer.[37] Trap-state density (D_{it}) can be calculated as follows (Equation (1)):

$$D_{it} = \left(\frac{qS\log(e)}{k_BT} - 1 \right) \frac{C_i}{q} \tag{1}$$

where k_B is the Boltzmann constant, e is electron charge, S is the S-value, T is temperature, and C_i is the capacitance of the gate insulator. The calculated D_{it} of 7 nm SnO TFT with in situ stacked Al$_2$O$_3$ of 6.7 × 10^{11} cm^{-2} eV^{-1} was lower than that of reported p-type SnO TFTs.[19] Also, the D_{it} of bare 20-nm SnO

TFT (4.0 × 10^{13} cm^{-2} eV^{-1}) was 25 times that of passivated SnO TFT (1.6 × 10^{12} cm^{-2} eV^{-1}). This difference indicates that in situ stacking process of an Al$_2$O$_3$ capping layer leads to fabricate defect-free, high-quality SnO thin films, and this directly influences to electrical performance of the TFT. In addition, the output characteristics of TFT exhibited both linearly increasing and hard-saturated current regions (Figure 1c).

2.2. Physical and Chemical Properties of In Situ Stacked Al$_2$O$_3$/SnO Layers

To further understand the defect-releasing effect of in situ Al$_2$O$_3$ deposition process on SnO films, we examined the film properties of the deposited samples. The 20-nm SnO sample was selected to identify the mechanism of the performance improvement associated with the in situ process and an Al$_2$O$_3$ layer. XPS, GIXRD, and GIWAXS analyses were conducted to compare TFT performances to film morphologies. **Figure 2**a,b includes deconvoluted XPS peak information of Sn 3d$^{5/2}$ spectra (486.8 ± 0.1 eV for Sn^{4+} [SnO$_2$], 486.1 ± 0.1 eV for Sn^{2+} [SnO], 484.9 ± 0.1 eV for Sn^0 [Sn]), and individual area ratios are listed in Table S1, Supporting Information. Figure 2a makes clear that SnO films have a certain amount of oxidized surface. However, when an Al$_2$O$_3$ capping layer was deposited on SnO film by an in situ process (Figure 2b), no SnO$_2$ peaks formed and unoxidized SnO is confirmed. From XPS analysis, we can conclude that oxidization of an SnO surface to SnO$_2$ can be successfully prevented by in situ Al$_2$O$_3$ capping, and an oxygen-deficient atmosphere can be induced in SnO. We also examined the crystallinity and crystal orientation using GIXRD and GIWAXS (Figure 2c–e). Both bare SnO and SnO with a capping layer had a tetragonal SnO structure with (001), (101), (002), (202) planes (Figure 2c, JCPDS 85-0423). In GIWAXS on bare SnO, we identified a partially oriented and randomly arranged nanocrystallites which could be identified from broad, and vague signal (Figure 2d). On the other hand, c-axis preferred orientation enhancement was observed for the in situ capped SnO (Figure 2e), indicating that an Al$_2$O$_3$ capping layer not only prevents surface oxidation of SnO, but also enhances the crystallinity of SnO.

To identify the effects of channel thicknesses on crystallinity, we conducted TEM analysis on 7-nm SnO samples of cross-sectional specimens of bare SnO TFT, ex situ stacked Al$_2$O$_3$/SnO, and in situ stacked Al$_2$O$_3$/SnO. The ex situ Al$_2$O$_3$-deposited sample was also evaluated to determine the influence of air exposure and the effect of the Al$_2$O$_3$ layer on SnO; its TFT also did not exhibit TFT activation (not shown). All layers were
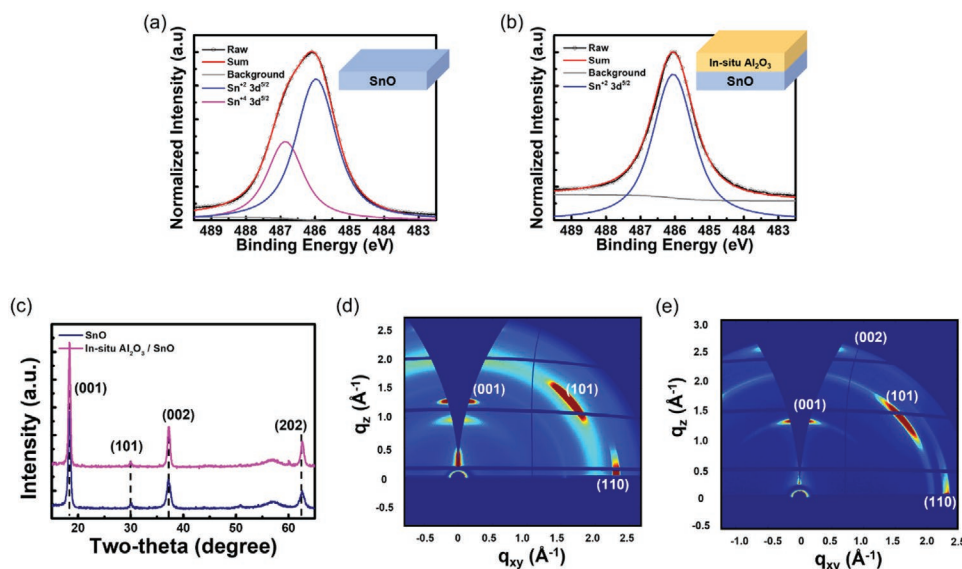
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Figure 2. a,b) Deconvoluted Sn 3d$^{5/2}$ spectra measured by XPS; a) bare SnO and b) in situ stacked Al$_2$O$_3$/SnO. Sample information is illustrated in each graph as an inset. c–e) Film crystallinities of SnO samples with various conditions: c) film crystallinity of bare SnO and in situ stacked Al$_2$O$_3$/SnO examined by GIXRD, d) film crystallinity and orientation of bare SnO, and e) in situ stacked Al$_2$O$_3$/SnO examined by GIWAXS. Indexed (hkl) indicate the respective planes of tetragonal SnO.

conformally deposited but exhibited different and distinguishable grain boundaries in the SnO layer (**Figure 3**a). In Figure 3b–d, higher-resolution TEM is shown, and corresponding fast Fourier transform images are inserted as insets. Based on these observations, three SnO phases were identified. In Figure 3b, bare SnO thin films showed evidence of an amorphous phase. In Figure 3c, crystallinity was enhanced in ex situ stacked Al$_2$O$_3$/SnO, but polycrystalline crystallites of (101) planes were embedded in an amorphous matrix with a high density of grain boundaries. Finally, in Figure 3d, a highly c-axis oriented, and aligned SnO crystal structure emerged in in situ stacked Al$_2$O$_3$/SnO. For this sample,

clearly defined layers were examined by EDAX scans without significant Al diffusion in SnO (Figure 3e–h). These results indicate that a stacking effect of Al$_2$O$_3$ on SnO rather than Al doping in SnO is quite effective to enhance crystallinity, particularly when an in situ deposition process is adopted. This also indicates the importance of crystallinity in SnO TFT performance. In conclusion, an impressive electrical performance of in situ stacked Al$_2$O$_3$/SnO TFT results from SnO crystallization. This result suggests that high crystallinity with low grain boundaries and defects are key factors in the assembly of high-performance SnO TFTs at low thicknesses less than 7 nm.
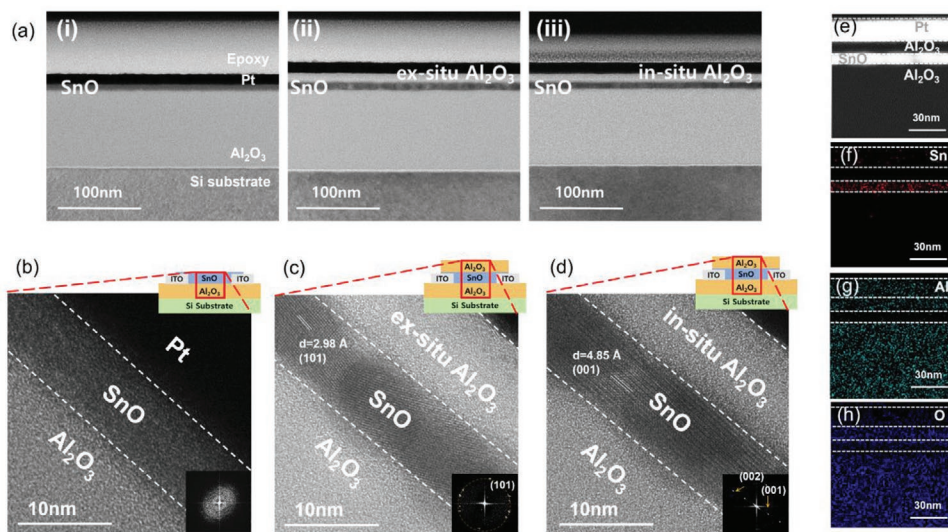

Figure 3. a–d) Cross-sectional TEM images of TFT samples (i–iii), e–h) EDAX scan and EDAX images of Sn, Al, and O signals of in situ stacked Al$_2$O$_3$/SnO. The Fast Fourier Transform patterns of each SnO area are shown in (b–d).

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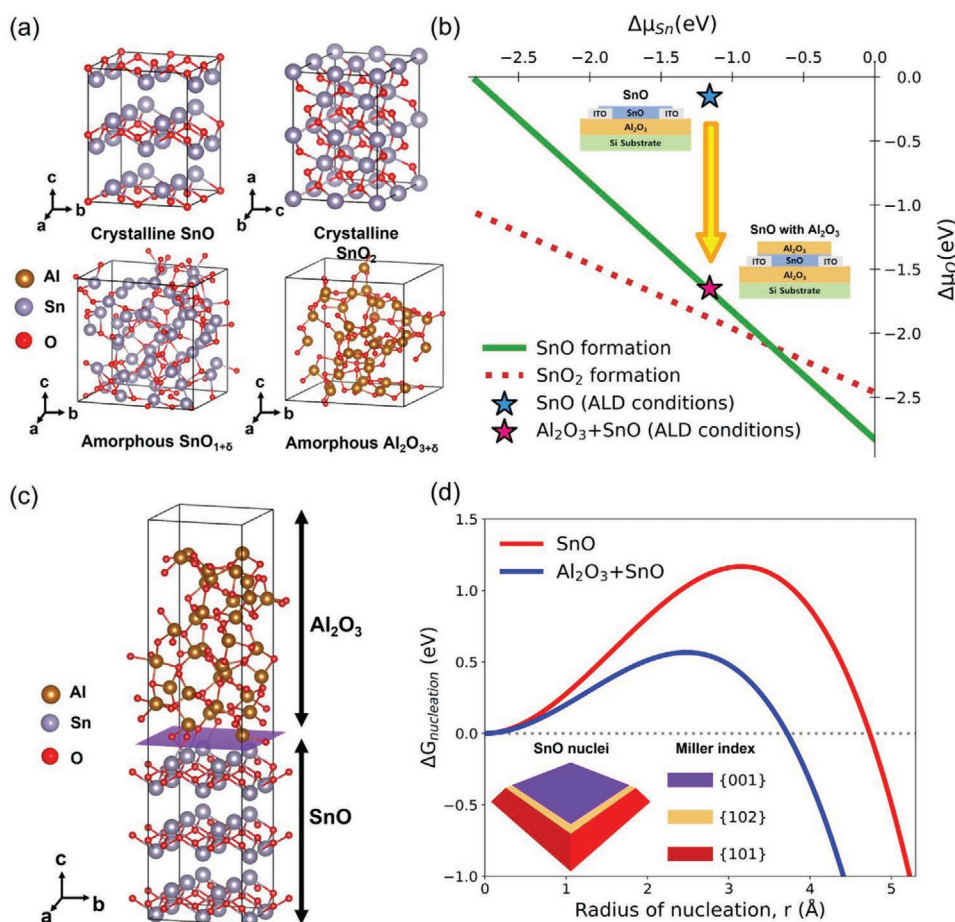**SCIENCE NEWS**
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Figure 4. a) Atomic structures of crystalline SnO and SnO_2 and amorphous $Al_2O_{3+\delta}$ and $SnO_{1+\delta}$. The brown, silver, and red spheres represent Al, Sn, and O atoms, respectively. b) The chemical potential of Sn and O for two different configurations. The blue star is SnO and the pink star is SnO with Al_2O_3. The solid green and dotted red lines are the growth conditions of crystalline SnO and SnO_2 phases, respectively. c) Atomic structure of crystalline SnO with amorphous Al_2O_3. The purple plane describes the interface between SnO and Al_2O_3. d) Calculated nucleation Gibbs free energy with respect to average surface energy obtained from the Wulff construction. Surface energy values were obtained from the literature.[39]

2.3. Computational Results for Formation of SnO Crystals

To understand the mechanism of SnO crystallinity enhancement by Al_2O_3, we investigated the chemical potential of an Sn–O system and the effect of an Al_2O_3 capping layer. We considered two crystalline phases (SnO and SnO_2) and two amorphous systems (Sn–O and Al–O). We first identified the chemical potential of Sn and O under ALD growth at 7.895×10^{-5} atm (the blue star in **Figure** 4b). This point is far from the growth condition of the two crystalline phases. To form crystalline SnO and SnO_2, the chemical potential under growth conditions of each element should satisfy the following thermodynamic conditions (Equation (2) and (3)).

$$\text{SnO: } \Delta\mu_{Sn} + \Delta\mu_O = \Delta H_{f,SnO} = -2.827 \text{ eV} \tag{2}$$

$$\text{SnO}_2\text{: } \Delta\mu_{Sn} + 2\Delta\mu_O = \Delta H_{f,SnO_2} = -4.923 \text{ eV} \tag{3}$$

where $\Delta H_{f,SnO_x}$ represents the formation enthalpies of the corresponding SnO_x calculated for bulk Sn and molecular O_2.[38] The chemical potential of as-deposited SnO is above this line,

which means they cannot form a crystalline phase, thereby as-deposited SnO exists in an amorphous condition (Figure 4a).

When a capping layer is deposited, the chemical potential of oxygen can drastically shift to the thermodynamic line. As determined by XPS characterization, the amorphous phases had excessive oxygen in their stoichiometry. The measured stoichiometries were $Al_2O_{3.08}$ and $SnO_{1.02}$ (Table S2, Supporting Information), and this oxygen stoichiometry difference can generate an additional $\Delta\mu_O$ term (Equation (4)).

$$\Delta\mu_O = \frac{(\Delta H_{Al_2O_{3.08}} + \Delta H_{SnO_{1.02}}) - (\Delta H_{Al_2O_3} + \Delta H_{SnO})}{N_O}$$
$$= \frac{(-46.943) - (-46.793)}{0.08 + 0.02} = -1.498 \text{ eV} \tag{4}$$

Because the energetics were obtained directly from the density functional theory (DFT) calculation for the given stoichiometries, an additional term, $\Delta\mu_O = \left(\dfrac{\partial G}{\partial N_i}\right)$, was calculated, for which ΔH_i is the total energy of each material for a given stoichiometry extracted from a DFT calculation, and N_O is the number of excessive oxygen atoms of stoichiometric crystals.
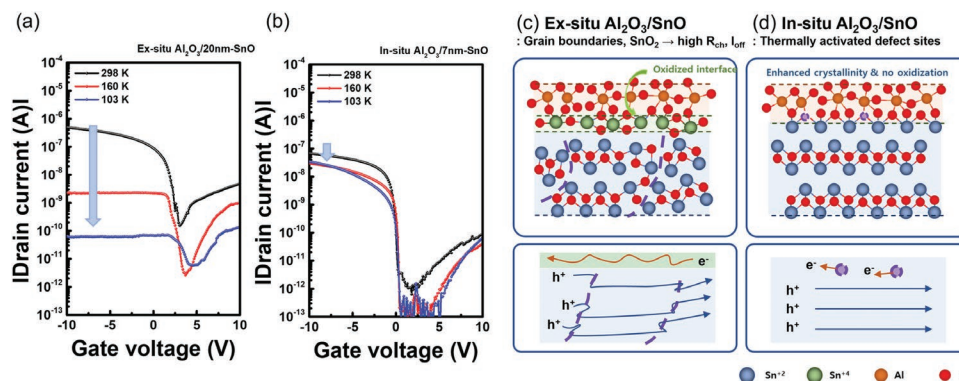
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Figure 5. a) Transfer curves of ex situ stacked Al_2O_3 and b) in situ stacked Al_2O_3/SnO depending on measurement temperature and c–d) following an estimated scheme of hole/electron transport mechanisms.

This $\Delta\mu_O$ is dramatically decreased oxygen chemical potential (−1.498 eV) and located in the thermodynamic equilibrium growth state of crystalline SnO (the pink star in Figure 4b). This means that deposition of Al_2O_3 layer provided new thermodynamic environments for crystallization. The calculated results may also provide a basis for why the ex situ stacked Al_2O_3/SnO samples exhibited degraded performance and crystallinity and why we were unable to achieve enhanced performance for SnO TFT when Al_2O_3 was deposited at 100 °C. This could be result from incorporated high ratio of excess oxygens into the Al_2O_3 film (Table S2, Supporting Information).

In addition, the interface formation with the capping layer contributes to nucleation of the crystallization. We generated a heterostructure of crystalline SnO with Al_2O_3 to investigate the nucleation Gibbs free energy compared with bare crystalline SnO (Figure 4c). In the nucleation process, the equilibrium shape of the particle is determined by the Gibbs–Wulff theorem, which states that the shape of crystalline material is determined by the polyhedron that minimizes overall surface energy.[40] We therefore created a Wulff construction from the average surface energy of the representative orientation of crystalline SnO with the energetics of low-index surfaces.[39,41] A particle of SnO consists of (001)-, (101)-, and (102)-oriented surfaces which is an 18-facet polyhedron. Because each facet is significantly large and the polyhedron is symmetric, the nucleation energetics of crystalline SnO can be calculated by considering those of a spherical surface, as described as follows (Equation (5)).

$$\Delta G_{nucle}(r) = \frac{4}{3}\pi r^3 \Delta G_v + 4\pi r^2 \sigma \tag{5}$$

where r is the radius of nucleation, ΔG_v is the Gibbs free energy per volume of SnO obtained from the DFT calculations, and σ is the average surface energy for each configuration: 1) bare SnO and 2) SnO with Al_2O_3 capping layer. As shown in Figure 4d, the energy barrier of SnO with Al_2O_3 is much lower than that of bare SnO. This confirms that SnO with Al_2O_3 easily forms its crystalline phase compared with its bare state. Consequently, the above two results regarding the chemical potential and nucleation Gibbs free energy show that Al_2O_3 can offer significant help in alleviating the amorphous SnO, and this is consistent with our experimental data.

2.4. Transport Mechanism and Stability of an In Situ Stacked Al_2O_3/SnO TFT

Based on the experimental and computational results, we found that the Al_2O_3 capping layer, crystallinity, and electrical performance were interrelated. In this section, we confirmed the importance of in situ deposition process for defect-less SnO fabrication and evaluated TFT stability. **Figure 5** exhibits and illustrates the differences in transfer characteristics at low-temperature analysis depending on ex situ and in situ processes exploited for the Al_2O_3 capping layer. In Figure 5a, from 298 K (25 °C, room temperature) to 103 K, on-current levels are dramatically decreased and exhibit abnormal on-current saturation in ex situ stacked Al_2O_3/SnO TFT. This could have resulted from channel resistance (R_{ch}) or contact resistance (R_c) in SnO with ex situ deposited capping layer.[42] Based on the results of this analysis, we assumed that the high density of grain boundaries and internal defects from the deposition process led to a high R_{ch} in ex situ stacked Al_2O_3/SnO TFT. SnO_2 formation near the interface served as a scattering point as well. Because electronic scattering by those defects has greater sensitive dependency according to temperature, the ex situ stacked Al_2O_3/SnO channel layer showed high temperature dependency. In addition, the in situ capped TFT did not show such temperature-dependent behavior (Figure 5b and Figure S1, Supporting Information). This could be a result of fewer grain boundaries and interface defects in the in situ stacked Al_2O_3/SnO TFT. The off-current level of the two TFTs also differed by temperature, and this could be interpreted as follows. In crystalline SnO, oxygen vacancies (V_O) and oxygen interstitials (O_i) are the main defects that contribute to electron transport, and those defects are generated less often at low temperatures.[43] This indicates that electron density can be slowed at a low temperature, and the resulting off-current reportedly decreases at a temperature below 300 K.[44] However, compared with in situ stacked Al_2O_3/SnO TFT (10^{-13} A), the minimum point of off-current in ex situ deposited TFT did not decrease (>10^{-12} A), which indicates defect formation and a transport mechanism of electrons which differs by TFT. Thus, surface oxidation by air exposure and structural defects could explain this high off-current. Also, we could deduce the origin of high off-current level of SnO TFT compared to n-type TFTs as thermally
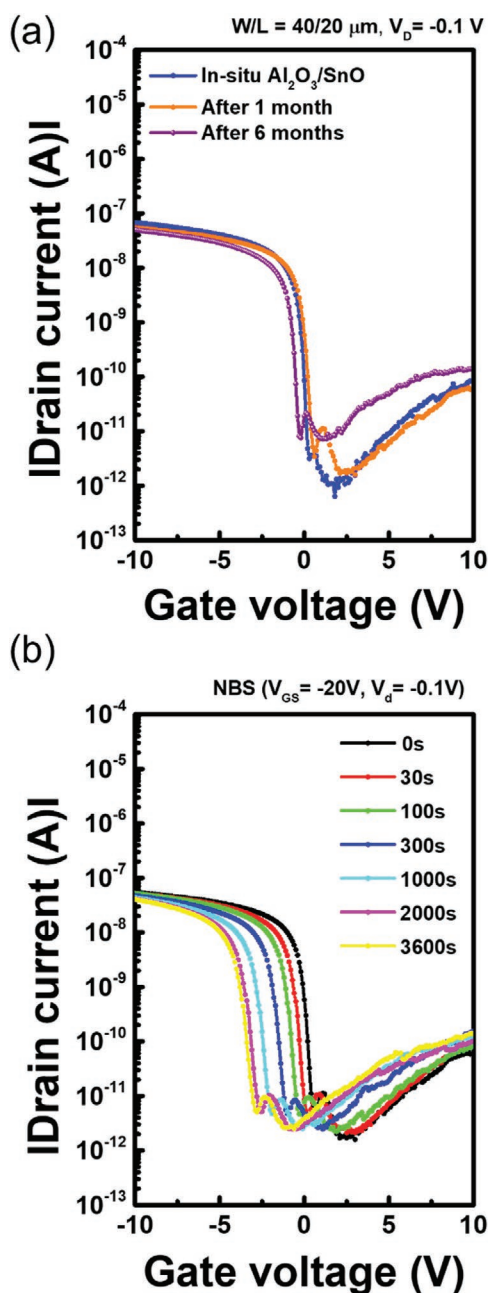
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Figure 6. a,b) Device stability evaluation: a) exposed to air ambient and b) measurement of negative bias stability of in situ stacked Al_2O_3 and 7 nm SnO.

on time. 3.52 V negative V_{th} shift occurred in the NBS test, although the S-value and μ_{FE} were maintained. This indicates that, during device operation, charge trapping in the interface region would be the main reason and only few charge-induced trap states are generated. Also, we could reduce that this shift is dominantly influenced by trap states in interface region rather than bulk channel from the discussions on Figure 5. This instability would require more refinement in further study using gate insulator engineering or passivate interface trap states. However, the performance of in situ stacked Al_2O_3/SnO TFT suggests superior stability against air ambient as well as the reasonable bias stability. It would be very promising to integrate conventional electronic based on the SnO TFT with an in situ Al_2O_3 capping layer due to low internal defect states.

2.5. Monolithic All-ALD-Channels-CMOS Inverter Performance

Finally, we fabricated and evaluated an all-ALD-channels (AAC)-CMOS inverter, which is not reported before, using ALD IGZO (n-type) and in situ stacked Al_2O_3/SnO TFTs; the oxide-semiconductor-based channel layer, gate insulator, and capping layer were fabricated by ALD processes. Detailed fabrication process of the device is described in supporting information. For the n-channel layer, we adopted ALD-fabricated IGZO with ozone as a co-reactant. Transfer characteristics of the IGZO TFT are described in Figure S2a, Supporting Information (V_{th} 0.3 V, μ_{FE} 42.6 cm^2 V^{-1} s^{-1}, and S-value 0.11 V decade^{-1}). **Figure 7a** provides an optical microscope image and diagram of the fabricated AAC-CMOS inverter. During the IGZO channel defining process, in situ deposited Al_2O_3 acts as etch stop layer to avoid SnO film degradation from back etching processes.[45]

Figure 7b–e displays the device performances of the fabricated AAC-CMOS inverter. From the voltage transfer characteristics (VTCs) of the CMOS inverter at different supply voltages (V_{DD}), CMOS exhibited prominent rail-to-rail inverter output characteristics (Figure 7b). The calculated voltage gain ($-dV_{out}/dV_{in}$) of the device is shown in Figure 7c and Figure S2b, Supporting Information, with the maximum voltage gain at 240 V/V. The inversion transition voltage extracted from output characteristics (V_T, input voltage at $V_{in} = V_{out}$) shifted slightly to a positive direction with an increasing V_{DD} (Figure S2c, Supporting Information).[43] The noise margin high (NM$_H$) and low (NM$_L$) were calculated by $V_{OH} - V_{IH}$ and $V_{IL} - V_{OL}$ (V_{OH} and V_{IL} were defined as 0; V_{DD} voltage and V_{IH} and V_{IL} were the high and low voltage points, where the gain is 1 V/V), respectively. The calculated noise margin (%) ((NM$_H$ + NM$_L$)/V_{DD}) was relatively high at 89.3% (Figure 7d). The input and output pulses at a 100 Hz operating frequency (Figure 7e) indicated successful inverter operation.[19] The propagation delay time (t_P, calculated by [t_{PLS} + t_{PHL}]/2), of the inverter was 377 μs (The propagation delay times from low to high (t_{PLH}) and high to low (t_{PHL}) were 657 and 97 μs, respectively). From these results, we successfully identified a fabricated CMOS inverter with high performance despite degraded p-type performances of SnO TFT (V_{th} 5.0 V, μ_{FE} 0.28 cm^2 V^{-1} s^{-1}, and S-value 1.07 V decade^{-1}), and large differences exist with IGZO TFT (Figure S2a, Supporting Information). This degraded electrical performances of p-type SnO may have resulted from post processes such as oxidation
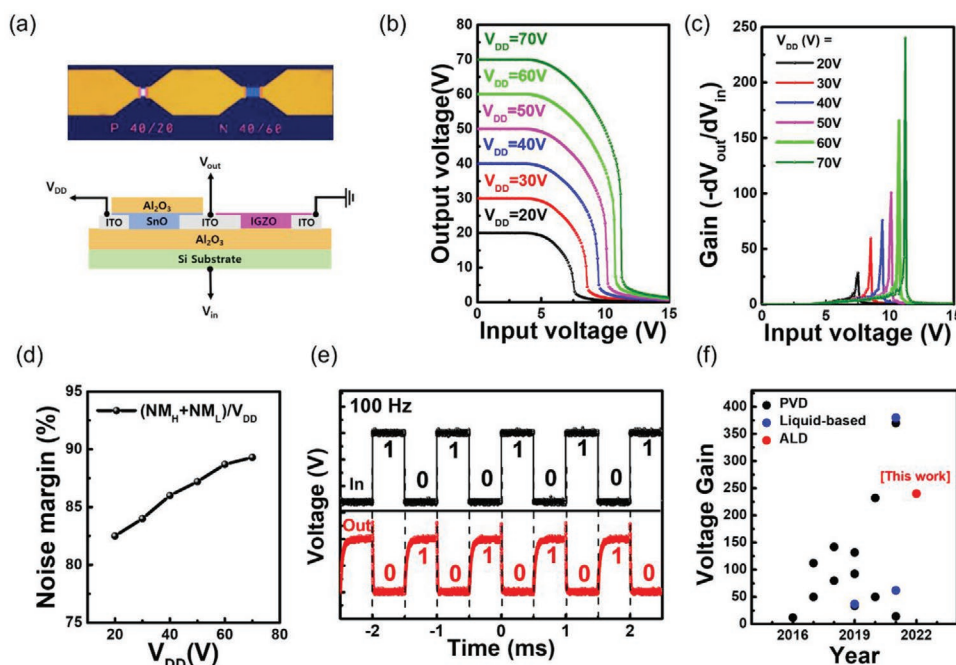
activated electrons from the decrease on off-current level in Figure 5b and Figure S1, Supporting Information. Figure 5c,d depicts a model of the expected carrier transport for ex situ and in situ stacked Al_2O_3/SnO TFT from the analysis data.

Device stability is another key factor for creation of practical TFT applications. Air stability, and negative bias stability (NBS) are evaluated in **Figure 6**. Against air exposure, transfer characteristics persisted for 6 months, particularly the S-value, and demonstrated about one order of off-current degradation (Figure 6a). For the case of NBS, in Figure 6b, we applied −20 V as gate voltage and measured transfer characteristics depending

Figure 7. a) Schematics and an optical image of a CMOS inverter, b) output voltage, and c) gain of the CMOS inverter as a function of input voltage (V_{in}) at different supply voltages (VDD), d) linear dependence of the total noise margin as a function of VDD, e) input and output voltage waveform (100 Hz), and f) gain comparison of CMOS using an oxide semiconductor as active layers in TFTs which references are listed in Table S3, Supporting Information.

by ozone reactants during the ALD IGZO process and/or UV–ozone post-annealing processes, which need to be optimized and improved in a future study.

A comparison of the device performances of the reported oxide-channel-based CMOS inverters (Figure 7f and Table S3, Supporting Information) colored by deposition method for channel layers indicates that this study achieves a state-of-the art gain and noise margin especially in terms of the fabrication process. Although other deposition methods such as PVD and liquid-based methods can produce superior performance, they have weakness from the perspective of mass production and reproducibility. Also, conventional processes exhibited poor step coverage with limited uniformity and conformality and suffered from inferior thickness controllability at the nanometer scale. In this study, both p-type and n-type channels and other oxide parts were fabricated using ALD. Furthermore, this work can be applied to the highly integrated circuits and the scaling down of 3D-structured devices such as vertical, fin-, GAA-, and CAA-structured FETs due to the precise controllability of film thickness and excellent uniformity possible in ALD. Although an optimization process would be needed for higher performance, this could be a milestone for production of ALD-based p-type TFTs and CMOS devices.

3. Conclusion

High-quality, *c*-axis aligned SnO film can be fabricated by deposition of an in situ Al2O3 capping layer on a film. For 7 nm SnO with an in situ Al_2O_3 capping layer, a low subthreshold swing (0.15 V decade^{-1}), high $I_{on/off}$ (6.54×10^5), low threshold voltage (0.06 V), and adequate field-effect mobility (1.14 cm^2 V^{-1} s^{-1})

is possible. Based on XPS, GIXRD, GIWAXS, and TEM analysis, we were able to determine that electrical performances are highly affected by SnO crystallinity, and in situ capped Al_2O_3 TFTs exhibit *c*-axis-aligned SnO films to lower the range of SnO thickness (7 nm). Computational results support crystallization mechanisms. The chemical potential and nucleation Gibbs free energy indicate that an Al_2O_3 layer provides a new thermodynamic equilibrium state for SnO and leads to formation of a crystalline structure. From low-temperature analysis and stability tests, we were able to determine that SnO films with Al_2O_3 as an in situ capping layer have exceptionally low internal defect sites. Finally, AAC-CMOS device fabricated by in situ Al_2O_3/SnO with IGZO exhibited a maximum voltage gain of 240 V V^{-1} with a noise margin of 89.3%. This device was fabricated by ALD, except for the electrodes, providing information to researchers exploring future possibilities for highly integrated and 3D-structured transistors.

4. Experimental Section

Film and TFT Fabrication Methods: SnO was deposited by ALD in a circular, lateral-gas-flow-type thermal reactor (Lucida D-100, NCD). Chamber pressure was held at 300 mTorr by 50 sccm of nitrogen purge gas (N$_2$, 99.999%). *N,N′*-tert-Butyl-1,1-dimethylethyldiamine stannylene (II) and deionized water (DI) were used as precursor and reactant, respectively. Sn precursor was heated to a temperature of 40 °C and DI was cooled to 20 °C by a cooling system. Detailed deposition information is described in the previous studies.[25,46]

SnO TFT has a coplanar structure fabricated on a p^{++}-doped silicon wafer, which acts as a gate electrode. The gate insulator layer was composed of 100 nm of Al$_2$O$_3$ deposited by ALD using trimethylaluminum (TMA) as a precursor at 200 °C. An indium tin oxide (ITO) source/drain electrode was deposited by sputtering and patterned

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by lithography and wet etching processes. After electrode patterning, the SnO was deposited as an active layer. For the capping layer, 10 nm of Al_2O_3 was deposited without breaking a vacuum state by ALD. The TFTs have active dimensions of 40 µm in width (W) and 20 µm in length (L). Post-annealing process was conducted under a N_2 atmosphere for 1 h at 300 °C. The electrical performance of each TFT was measured by a Keithley 4200 semiconductor parameter analyzer.

Analysis Methods: Film properties and morphologies were measured with various analytical tools. Film thickness was measured by spectroscopic ellipsometry (UV-FMS, Ellipso Technology). Chemical binding states of Sn metal were investigated by X-ray photoelectron spectroscopy (XPS; K-alpha$^+$, Thermo Fisher Scientific Co). Film crystallinity and orientations were analyzed by grazing-incidence X-ray diffraction (GIXRD; Rigaku Model Smartlab, Rigaku Corporation) using the 2θ-method and a 1° as incidence angle and grazing-incidence wide-angle X-ray scattering (GIWAXS, 3C beamline in Pohang Accelerator Laboratory). From GIWAXS spectra, interplanar distances (d) were interpreted using a scattering vector (q) (Equation (6)).[47]

$$d = \frac{2\pi}{q} \qquad (6)$$

To identify the cross-sectional film morphology, crystal structure, and elemental distribution, transmittance electron microscopy (TEM; JEM-2000EXII, JEOL) and energy dispersive spectrometry (EDS) were employed. Cross-sectional TEM specimens were prepared from fabricated TFTs using a focused ion beam (FIB; Nova 200, FEI) etching system.

Computational Methods: All DFT calculations were performed using the Vienna Ab initio Simulation Package (VASP).[48,49] For crystalline SnO, a DFT calculation with a van der Waals (vdW) correction was used in VASP because crystalline SnO is a well-known layered structure. A projector-augmented wave potential was applied with the generalized gradient approximation within the Perdew–Burke–Ernzerhof framework to describe the exchange-correlation energy of valence electrons.[49] The 3s and 3p states of Al; the 4d, 5s, and 5p states of Sn; and 2s and 2p states of O were considered as valence states. The electronic wave functions were expanded in plane waves with a cutoff energy of 520 eV to minimize Pulay stress during structural optimization, which was truncated when the Hellmann–Feynman forces reached the threshold value of 0.001 eV Å^{-1}. The Brillouin zone was sampled using a 100 k-points density per 1 Å^3 in the reciprocal cell.

The chemical potential was calculated based on the ideal gas assumption as follows:

$$\mu_i(T, p) = \mu_i^0 + \Delta\mu_i = \mu_i^0 + k_B T \ln\left(\frac{p_i}{p_i^0}\right) \qquad (7)$$

where μ_i^0 is the internal energy of i in standard conditions that can be extracted from the DFT calculations. The latter term represents the activity, in which k_B is the Boltzmann constant, T is temperature, p is pressure, and p^0 is the pressure in the standard state. The temperature and pressure were obtained from experimental parameters described in the previous experimental reports.[25,46]

Amorphous structures were generated with constrained random packing of N atoms of the given material in a cubic box using the Packmol package.[50] Nitrogen was chosen as the 100% that can represent the composition exactly. Starting with this configuration, ab initio molecular dynamics (AIMD) simulations from 1500 to 3000 K were performed, which was above the melting point of each material, to rapidly determine the equilibrium state. These generated structures were quenched to 0 K to obtain the total energies after AIMD simulation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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