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ABSTRACT

This study addresses the optimization of strain in continuous MOSFET downscaling, particularly at the nanoscale, where traditional Fourier models fail due to non-diffusive phonon transport effects. We introduce a multi-physics simulation approach that combines Finite Element Method (FEM) and Density Functional Theory (DFT) calculations to design strain-optimized 3D MOSFET structures. By implementing the kinetic collective model within FEM simulations, we accurately predict thermal-induced strains in the Si channel layer. Our DFT calculations further elucidate the impact of these strains on the electronic properties, particularly the electron effective mass, thereby offering insights into mobility enhancement strategies. The study not only advances the implications of nanoscale heat transfer for device performance but also provides a robust framework for optimizing next-generation semiconductor devices through strain engineering and sophisticated multi-physics simulations.

I. INTRODUCTION

Strain is a critical factor in the semiconductor. It is an inevitable consequence of nanoscale fabrication but has a significant impact on device performance. It can enhance carrier mobility by altering the band structures of channel materials such as Si and Ge, thereby reducing the effective mass of charge carriers.[1–7] Conversely, it can also introduce the formation of undesirable dislocations or defects that negatively affect the reliability and lifespan of the device.[8–10] Thus, controlling strain behavior is essential for achieving ideal device conditions.[11] Strain fundamentally arises from residual stresses induced by various factors during the manufacturing process. A critical source of this strain is the thermal expansion coefficient mismatch between the substrate and the thin film, particularly when an amorphous dielectric material is involved at the interface. This mismatch occurs during thermal processing steps like annealing or cooling; therefore, understanding heat distribution is essential for strain optimization. Despite its significance, the strain–heat relationship at the nanoscale remains challenging, as the mechanism of heat transfer differs from those at a larger scale.

There have been experimental efforts[12–18] to measure the strain–heat relationship; however, it becomes more challenging as semiconductor dimensions shrink below 10 nm. This nanoscale regime not only introduces the complexity in device geometry, such as the 3D integration structure,[19,20] but also hinders the accurate quantification of thermal effects on strain behavior. Traditionally, the Fourier model has been used to explain heat transfer in solids, stating that heat flux is proportional to thermal gradient as defined: $q = -k\frac{dT}{dx}$, where k is a constant thermal conductivity of materials and $\frac{dT}{dx}$ is the temperature gradient. However,

at the nanoscale, thermal conductivity becomes variable, significantly influenced by phonon dynamics, which act as the primary heat carriers in solids. As device dimensions become smaller than the phonon mean free path, reduced phonon collision and scattering rates lead to decreased thermal conductivity.[16,21–23] To address this nanoscale issue, alternative models such as a non-Fourier model are required. The Kinetic Collective Model (KCM) represents one such approach.[24–26] This model assumes the phonon behavior as a hydrodynamic-like heat transport and, thus, showed the improved capability for predicting a temperature-dependent thermal conductivity at the nanoscale. Consequently, KCM is appropriate to characterize the strain–heat relationships in nanoscaled semiconductor devices.[27,28]

In this study, we employed the KCM model to address semiconductor design by predicting the thermal-induced strain at the nanoscale. Specifically, we aim to design strain-optimized n-type 3D MOSFET structures using a combined method of Finite Element Method (FEM) and Density Functional Theory (DFT) calculations. A parametric study was conducted on representative n-type 3D MOSFET structures that are widely adopted in the semiconductor industry to analyze the effect of each geometry parameter on the strain on the Si channel layer. We attempted to simulate the cooling process of the device after depositing TiN, the gate metal, with Atomic Layer Deposition (ALD).[29,30] The thermal behavior of Si was calculated with FEM by applying KCM, which accounts for the influence of nanoscale boundaries on phonon thermal conduction. This approach enabled the prediction of thermal and strain distributions in the silicon channel layer at the nanoscale. DFT calculations were performed to predict changes in the electron effective mass of Si along the xx-strain and yy-strain obtained by FEM. From these data, we created metamodels with about 95% accuracy that can predict the structure, which can minimize the electron effective mass. This multi-physics modeling approach will be applicable to other nano-scaled electronics, not just 3D MOSFETs.

II. METHODS

Figure 1 illustrates our workflow for optimizing the heat-induced residual strain remaining in 3D MOSFET structures after the ALD cooling process, using a nanoscale heat transfer model. Initially, we perform a time-dependent FEM simulation to model the cooling process in nanoscale MOSFET structures, allowing us to obtain the saturated temperature distribution. This saturated temperature solution is subsequently used as a boundary condition in a stationary FEM calculation to determine the resulting residual strain. Here, the KCM[25] is utilized to simulate the heat transfer in the Si channel, enabling precise strain predictions. Following this, the strain values calculated via FEM allow for the determination of electron effective mass under strained conditions using DFT calculations, with the goal of evaluating changes in electrical mobility properties. Finally, leveraging the comprehensive data derived from both FEM and DFT calculations, we utilized the machine learning-based optimization for strain-effective mass relation.

The finite element method (FEM) was used to model MOSFET devices that had dimensions close to real devices. These models can simultaneously consider the two different types of physics: (1) heat transport in the solid during cooling and (2) the resulting strain distribution. All FEM calculations were carried out using COMSOL Multiphysics 6.2 software with the implementation of Heat transfer in solids, KCM, and Solid mechanics.

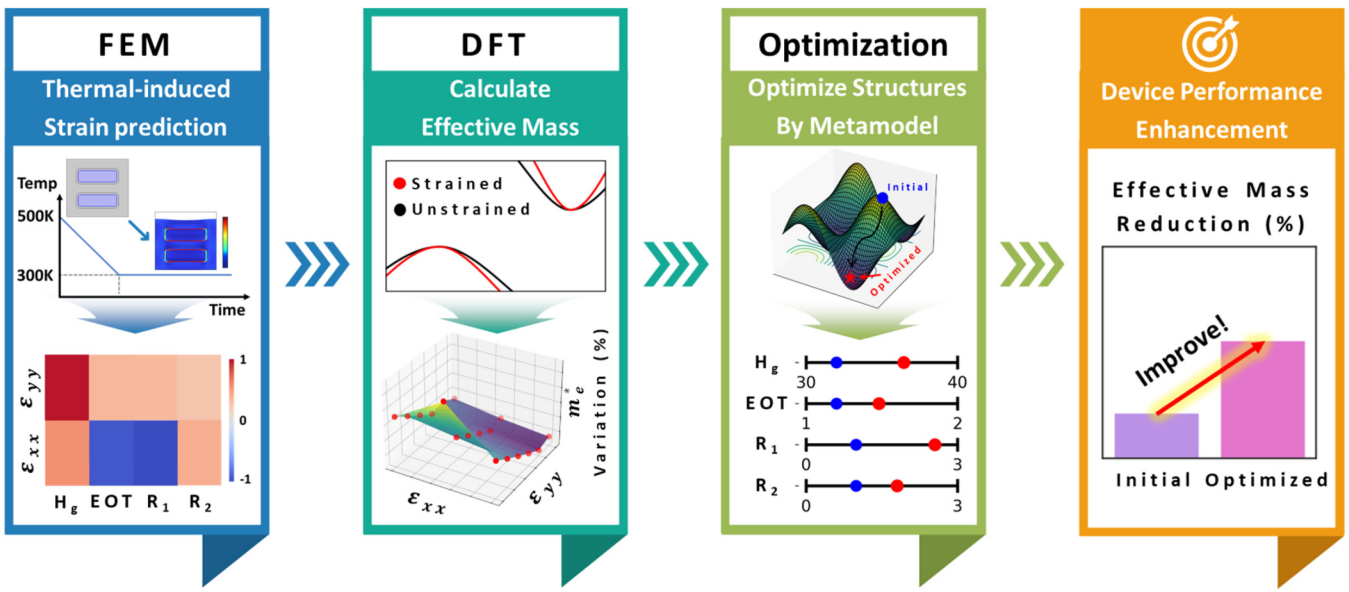

FIG. 1. Workflow for the strain optimization process in 3D MOSFET.

The heat transport is described based on two different heat transfer models depending on the device part. The heat transport from the substrate to the gate metal was calculated with a conventional heat transfer equation, Fourier model, which can be written as

$$\rho c_p \frac{\partial T}{\partial t} + \nabla \cdot q = Q, \tag{1}$$

where ρ is the density of the material, c_p is the constant pressure heat capacity, T is the temperature, t is the time, q is the heat flux, Q is heat source of the system, and k is the thermal conductivity. Equation (1) describes the change of temperature with time. Convection and radiation are not considered in this study, thereby those terms can be ignored. A conduction model was considered with KCM for Si, which can consider the size effect, and a Fourier model for the rest of the materials. KCM, which is based on the Guyer and Krumhansl equation[31,32] and the Fourier model, can be written as

$$\tau \frac{dq}{dt} + q = -k\nabla T + l^2\left(\nabla^2 q + \alpha \nabla(\nabla \cdot q)\right), \tag{2}$$

$$q = -k\nabla T, \tag{3}$$

where τ is the relaxation time of flux q, k is the bulk thermal conductivity of the substrate, and l is the nonlocal length, which can be microscopically interpreted as a weighted average phonon mean free path. These parameters are properties of the Si channel. We set the relaxation time as a temperature-dependent function, referring to Ref. 31. Furthermore, to address the overestimation of KCM when the sample size is smaller than the nonlocal length, we applied the effective nonlocal length and $\alpha = 1/3$, as suggested in Ref. 27.

To calculate the heat-induced residual strain in MOSFET, we solved the structural mechanics equations. The static equilibrium equation of solid mechanics follows from Newton's second law, which, if neglecting inertial terms, can be written as

$$0 = \nabla \cdot \sigma + F_V, \tag{4}$$

where σ is the stress tensor and F_V is the body force vector representing external forces. To define the relationship between stress tensor and strain tensor, including thermal-induced strain tensor ε_{th}, Hooke's law is applied,

$$\sigma = C(E,\nu)\colon \varepsilon_{el} = C(E,\nu)\colon(\varepsilon - \varepsilon_{th}), \tag{5}$$

where ε is the symmetric strain tensor, ε_{el} is the elastic strain tensor, and $C(E,\nu)$ is the fourth-order elasticity tensor, defined by Young's modulus E and Poisson's ratio ν, which characterize the material's elastic properties. The strain tensor can be defined in terms of displacements u for cases of small displacements and rotations,

$$\varepsilon = \frac{1}{2}\left[(\nabla u)^T + \nabla \mathrm{u}\right]. \tag{6}$$

Thermal-induced strain can be calculated by using the equation below:

$$\varepsilon_{th} = \alpha \Delta T I, \tag{7}$$

where ΔT is the temperature difference, α is the thermal expansion coefficient, and I is the second-order unit tensor. The specific parameters utilized in the modeling are detailed in Table I.

The effect of strain on the electronic structure was calculated with Density functional theory (DFT) calculations. All DFT calculations were performed with the Vienna *Ab initio* Simulation Package (VASP)[33] using the projector augmented-wave (PAW) method[34] with generalized gradient approximation (GGA)[35] within the Perdwe–Burke–Ernzerhof (PBE) framework. The plane-wave basis set was expanded to a cutoff energy of 520 eV to minimize Pulay stress during the structural optimization. The structure was truncated until the Hellmann–Feynman forces were under 0.01 eV/Å. The electronic energy convergence was set to 1×10^{-5} eV. The Brillouin zone was sampled using 100 k-points density per inverse Å^3 of the reciprocal cell. After optimization, 18 strained structures were

TABLE I. Parameters and their values used in the Kinetic Collective Model (KCM).

Symbol	Description	Material	Value (units)
T	Initial temperature		500 (K)
c_p	Heat capacity at constant pressure	Si	700 [J/(kg K)]
		SiO_2	730 [J/(kg K)]
		TiN	520 [J/(kg K)]
		HfO_2	120 [J/(kg K)]
ρ	Density	Si	2329 (kg/m^3)
		SiO_2	2200 (kg/m^3)
		TiN	5200 (kg/m^3)
		HfO_2	9700 (kg/m^3)
k	Thermal conductivity	Si	130 [W/(m K)]
		SiO_2	1.4 [W/(m K)]
		TiN	25 [W/(m K)]
		HfO_2	1.1 [W/(m K)]
α	Thermal expansion coefficient	Si	2.6×10^{-6} (1/K)
		SiO_2	0.5×10^{-6} (1/K)
		TiN	10×10^{-6} (1/K)
		HfO_2	6×10^{-6} (1/K)
E	Young's modulus	Si	170 (GPa)
		SiO_2	70 (GPa)
		TiN	350 (GPa)
		HfO_2	57 (GPa)
ν	Poisson's ratio	Si	0.28
		SiO_2	0.17
		TiN	0.24
		HfO_2	0.3
l	Non-local length for FinFET		3 (nm)
	Non-local length for GAAFET		3 (nm)
	Non-local length for MBCFET		10 (nm)

implemented by applying deformations in the xx-direction range (0%– 1%) and yy-direction range (−2.0% to 0.5%) divided by 0.5% intervals. Effective mass was extracted from the DFT-calculated band structure using the Effmass Package.[36]

The optimization is utilized through kernel regression over graphs,[37] phase regeneration,[38] relevant-based feature ranking[39] algorithm, which is implemented in PIAnO package. For efficient optimization, we have constructed metamodels, a sophisticated and light mathematical representation, rather than fully solving the governing equation again. It serves to encapsulate the complex simulation outcomes, offering efficient means to predict the performance of various design configurations under strain. Through these metamodels, we were able to forecast the strain-optimized 3D MOSFET structures, thus significantly enhancing device performance by maximizing electron mobility.

III. RESULT AND DISCUSSION

The Fourier equation has traditionally served as the foundation for describing heat transfer in solids; however, its limitation becomes evident at the nanoscale, where it fails to account for the reduction in silicon's thermal conductivity. To address this shortcoming, we utilize the KCM, devised to capture non-Fourier heat transport behaviors within nanoscale structures. In order to compare the heat distribution predicted by the KCM model and the Fourier model, we simulated the cooling process following gate deposition with ALD. We employed temperatures of 300 K at the top and 500 K at the bottom of the Si channel layer. As shown in Fig. 2, the heat transfer under the KCM is smaller compared to that of the Fourier model, a finding that is consistent with experimental observations noting a decrease in silicon's thermal conductivity due to size effects.[24,40,41] This discrepancy highlights KCM's enhanced capability to incorporate nonlocal terms in the transport equation, thereby providing a more accurate description of thermal effects at the nanoscale, including heat vorticity and viscosity due to the presence of complex boundaries. Consequently, we utilize KCM for a more precise prediction of complex thermal behaviors at the nanoscale.

With this KCM model, we investigated various transistor structures to understand their thermal behavior and residual stresses. The MOSFET structures, including the Pragmatic Fin FET (PFFET), Gate-All-Around FET (GAAFET), and Multi-Bridge Channel FET (MBCFET), were constructed, as shown in Fig. 3. These structures are based on the research by Huang *et al.*,[42] which provides a significant representation of nanoscale MOSFET technology in line with current industrial applications. The PFFET, GAAFET, and MBCFET structures feature a vertically oriented channel, which is central to the 3D MOSFET characteristic. The PFFET has a single vertical channel with a height of 24 nm and a width of 6 nm, whereas the GAAFET and MBCFET have two channels covered by equivalent oxide thickness (EOT) and gate: 6×6 and 24×6 nm, respectively. The material choices—TiN and HfO_2 for the gate and oxide layers, Si for the channel and substrate, and SiO_2 for the Shallow Trench Isolation (STI)—are consistent with industry-standard High-K Metal Gate (HKMG) technologies. The initial comprehensive geometry parameters of these designs are detailed in Table II.

The geometrical parameters detailed in Table I influence the heat-induced strain in the Si channel. However, the specific impact of these parameters on strain remains challenging to determine due

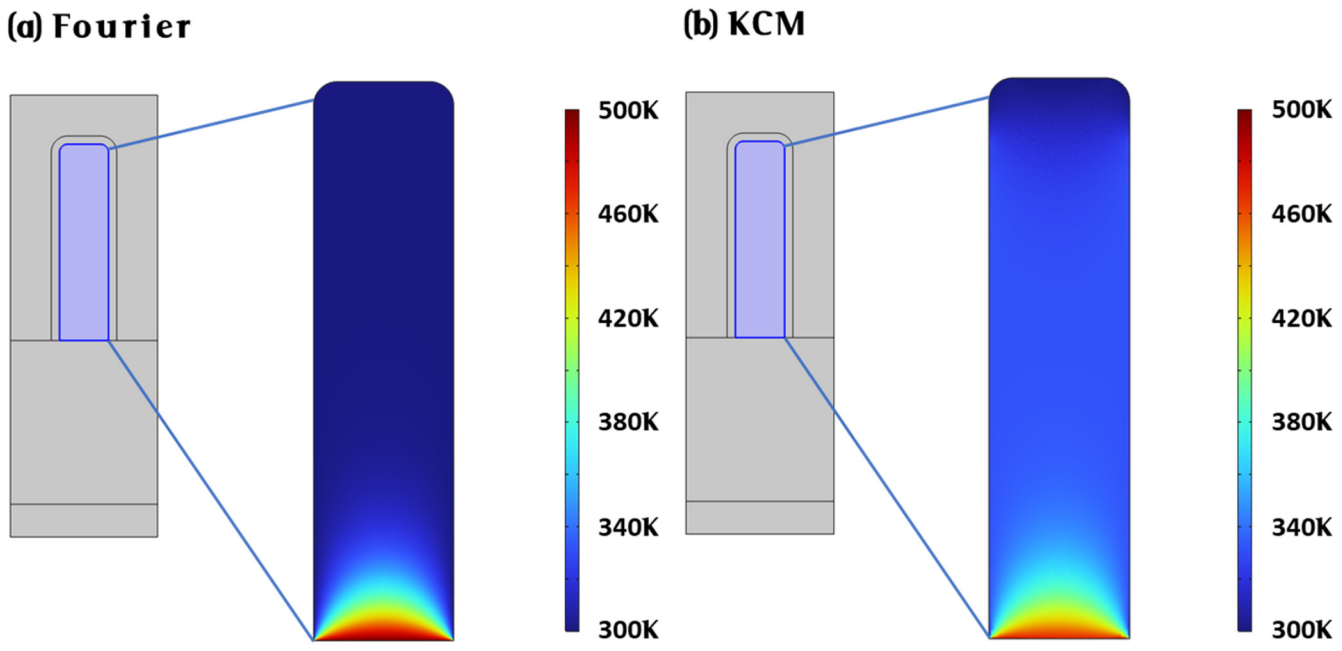

FIG. 2. Heat distribution in the Si channel layer calculated by FEM applying (a) Fourier model and (b) KCM model.

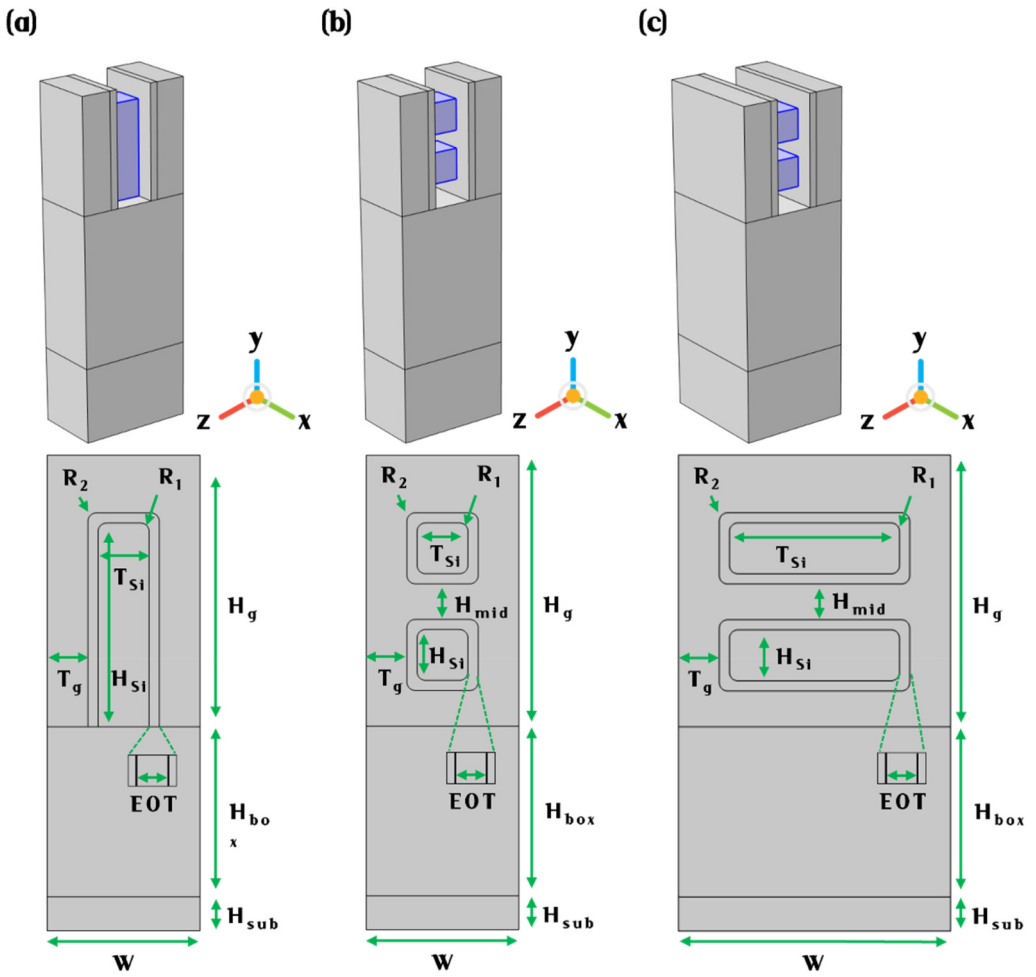

FIG. 3. 3D architecture and 2-D cross sections along the x-y plane of (a) PFFET, (b) GAAFET, and (c) MBCFET.

TABLE II. Initial geometry parameters in nm units for simulated PFFET, GAAFET, and MBCFET.

	PFFET	GAAFET	MBCFET
W	18	18	32
EOT	1.2	1.2	1.2
R_1	1	1	1
R_2	1	1	1
H_{Si}	24	6	6
H_g	32	32	32
H_{sub}	4	4	4
H_{box}	20	20	20
T_g	5	5	5
T_{Si}	6	6	20
H_{mid}	0	4.2	4.2

to difficulties in isolating the individual contributions from the overall effect. The parametric study can serve as a guideline for understanding the relationship between parameters and thermal-induced strain. Herein, based on the research studies,[43–45] we selected four key parameters that critically influence the strain in the channel layer without substantially altering the size of the Si channel, primarily affecting the electron effective mass. These parameters are R_1 and R_2, which represent the curvatures of the channel and EOT, respectively; H_g, which is the height of the gate; and EOT, the thickness of the oxide layer.

The influences of individual geometric parameters on device strain were systematically investigated in the PFFET, GAAFET, and MBCFET, respectively. Figures 4(a)–4(c) present the results for the strain distribution of xx- and yy- directions as each geometric parameter is adjusted to its maximum allowable value (R1 and R2 to 3 nm, H_g to 40 nm, and EOT to 2 nm). These adjustments

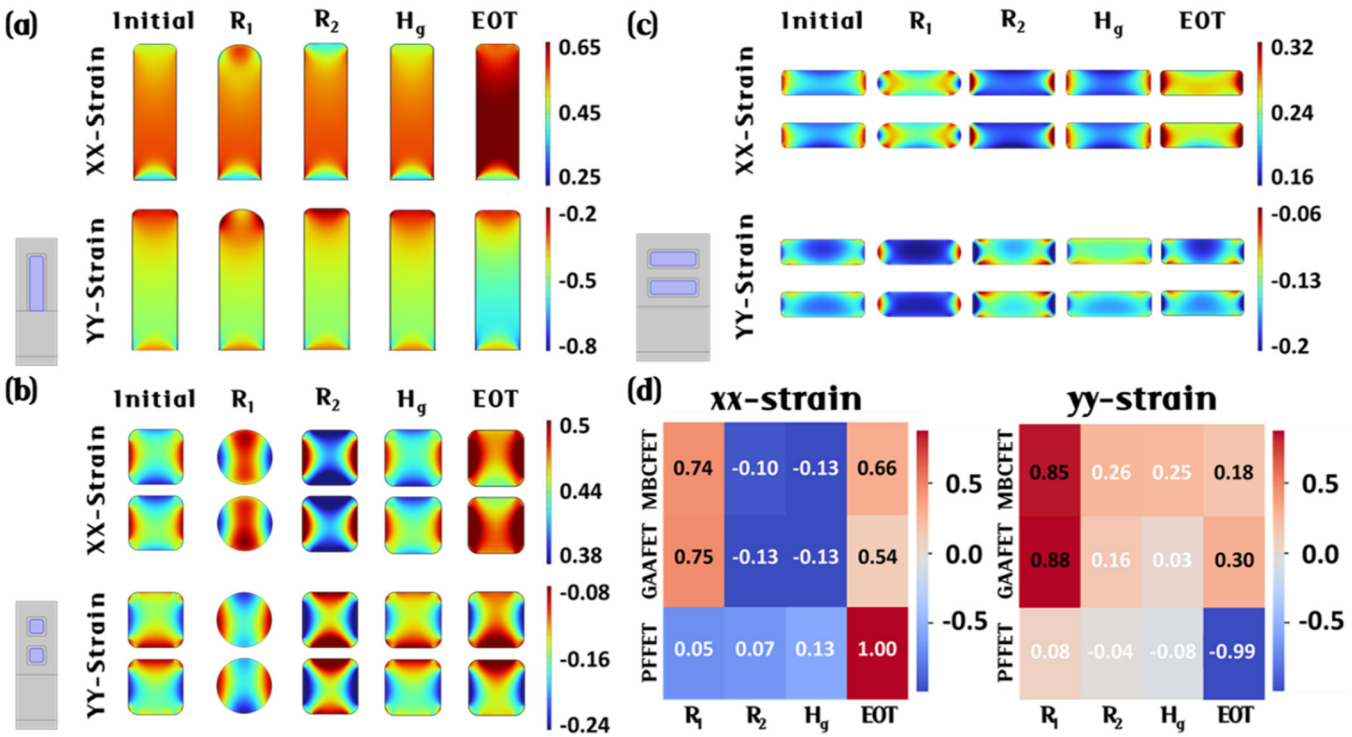

FIG. 4. The result of the parameter study of xx-strain and yy-strain in (a) PFFET, (b) GAAFET, (c) MBCFET, and (d) Pearson correlation between average xx-strain and geometry parameters and between average yy-strain and geometry parameters. In (a), (b), and (c), "initial" represents the baseline MOSFET structure before any parametric variations in geometry parameters (R1, R2, Hg, EOT) were applied.

generally led to tensile xx-strain and compressive yy-strain across all structures. This pattern is primarily attributed to the metal gate contracting significantly in the yy-direction during cooling. Notably, EOT plays a pivotal role in all structures; its modifications result in pronounced tensile xx-strain and compressive yy-strain compared to other parameters, highlighting its critical influence on strain fluctuations. This significant effect stems from EOT's direct interface formation with the Si channel, allowing its modifications to directly affect the channel's strain characteristics.

To thoroughly examine the interdependencies among the variables, we expanded our investigation to include a comprehensive parametric study that simultaneously altered all four selected variables. Given that subdividing each variable into n segments necessitates n^4 calculations per structure, the complexity and computational load increase exponentially with finer divisions. Since the number of experiments increases exponentially as the explore ranges are divided more closely, we employed Design of Experiments (DOE)[46] techniques to efficiently generate approximately 100 simulation points. This approach allowed us to maintain the accuracy of the parametric study while drastically enhancing computing efficiently. From these simulation points, we obtained the average values of xx-strain and yy-strain and expressed them as Pearson correlation for each geometric parameter [Fig. 4(d)]. As expected, EOT was the most crucial factor in PFFET, while R_1 took precedence in GAAFET and MBCFET due to structural variances. Interestingly, due to the structural similarities of GAAFET and MBCFET, values of Pearson correlation are similar.

Strain patterns play a crucial role in optimizing device characteristics. This is because changes in strain alter the effective electron mass of silicon, impacting electron mobility, which, in turn, directly influences the drive current.[1,3,47] The equation for mobility [Eq. (7)] shows

$$\mu = \frac{e\tau}{m^*}, \tag{8}$$

which is the relationship between effective mass and mobility. Thus, the electron effective mass plays an important role in quantifying the effect of strain on the electrical properties of the device. According to the study,[1] the electron effective mass decreases increased tensile xx-strain and decreased compressive yy-strain. Achieving this reduction requires geometric parameters with a Pearson correlation close to 1 with both xx-strain and yy-strain. However, identifying the most impactful variable of the PFFET was complex due to conflicting Pearson correlation values: EOT showed a correlation of 1 with xx-strain but −1 with yy-strain. To address this complexity, we applied DFT calculations to more accurately

quantify the relationship between these parameters and effective mass.

The DFT calculations were performed to analyze band structures and calculate the electron effective mass, determining the influence of strain parameters derived from the FEM calculations. The average values of xx-strain and yy-strain obtained from the FEM calculations were applied to the constructed atomic structure for DFT calculation. Given the high computational demands of DFT, we initially focused on a distinct set of 18 strained Si structures rather than calculating all approximately 300 simulation points generated by DOE. These 18 structures were selected based on the xx-strain range from 0 to 1% and yy-strain range from 0.5 to −2%, with an interval of 0.5%, to conduct the initial DFT analysis. Figure 5(a) shows the band structures of strained Si and unstrained Si obtained by DFT calculation. From the curvature of each band structure, we derived the electron effective mass. The calculated effective mass values were interpolated as a function of xx-strain and yy-strain and the resulting function is visualized as a plane in Fig. 5(b). This function reveals that the electron effective mass decreases with tensile xx-strain, while it increases with compressive yy-strain. This result is consistent with the trend presented in previous research studies.[1,48]

Subsequent application of the FEM-derived strain values into these DFT-based functions allowed us to quantify the variations in electron effective mass. As shown in Fig. 5(c), the Pearson correlation between geometry parameters and electron effective mass revealed that, contrary to initial strain-only findings, curvature R_1 had the most substantial impact on reducing electron effective mass across all models. Notably, the structural characteristics of GAAFET and MBCFET yielded similar correlation profiles across all parameters, highlighting the pronounced effect of EOT in structures with longer horizontal channels. Conversely, in PFFET, which features vertically elongated channels, the influence of EOT on electron effective mass was less significant.

Based on our previous understandings, we now optimized structures to minimize electron effective mass for mobility enhancement. We employed PIAnO, an optimization tool, to build a metamodel for each structure, achieving Normalized Root Mean Square Error (NRMSE) values of 4.9% for PFFET, 4% for GAAFET, and 5.1% for MBCFET. Subsequently, these metamodels were utilized to predict the strain-optimized 3D MOSFET structures where the electron effective mass is minimized.

Figure 6 shows the optimized structures, detailing the range of parameter changes, the optimized values, and the extent of

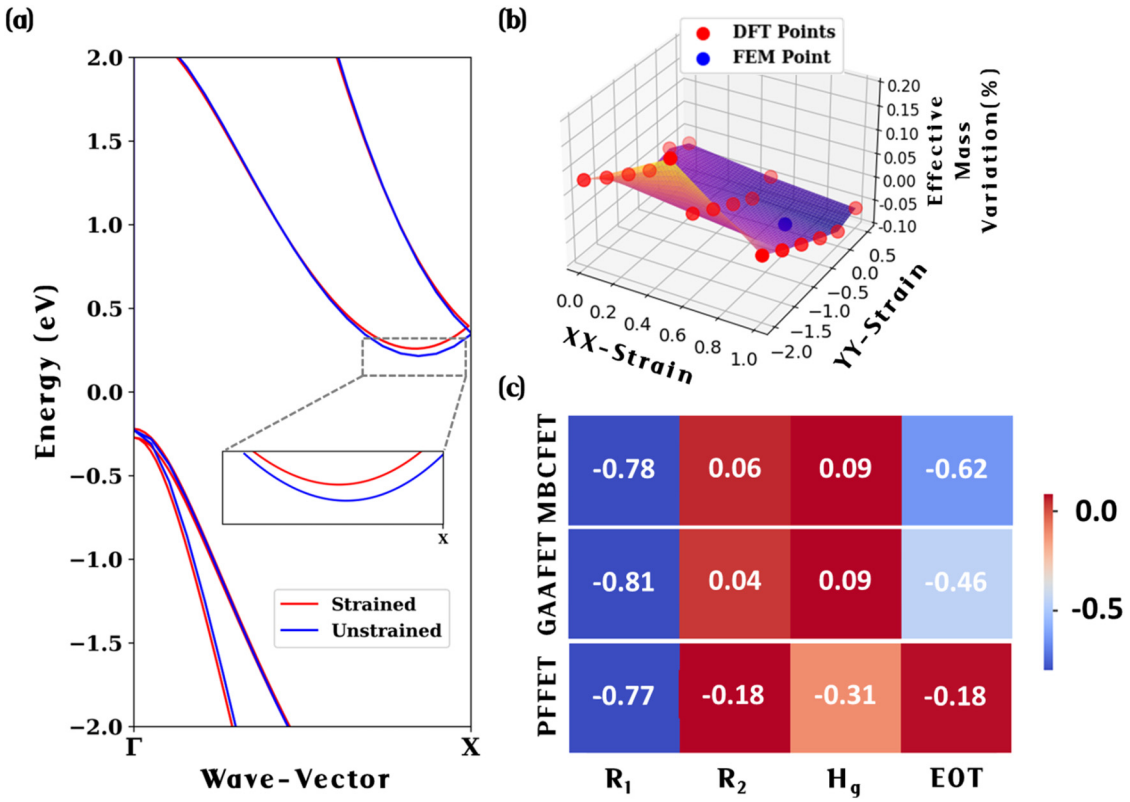

FIG. 5. (a) Band structure of Si with 1% strain in the xx direction and 0.5% strain in the yy direction, along with unstrained Si, and (b) interpolated plane of electron effective mass as a function of xx-strain and yy-strain, constructed from DFT simulation data (red dots). The blue dot represents a FEM-derived strain point applied to the interpolated DFT surface, and (c) Pearson correlation for geometry parameters of effective mass for each 3D MOSFET structure.

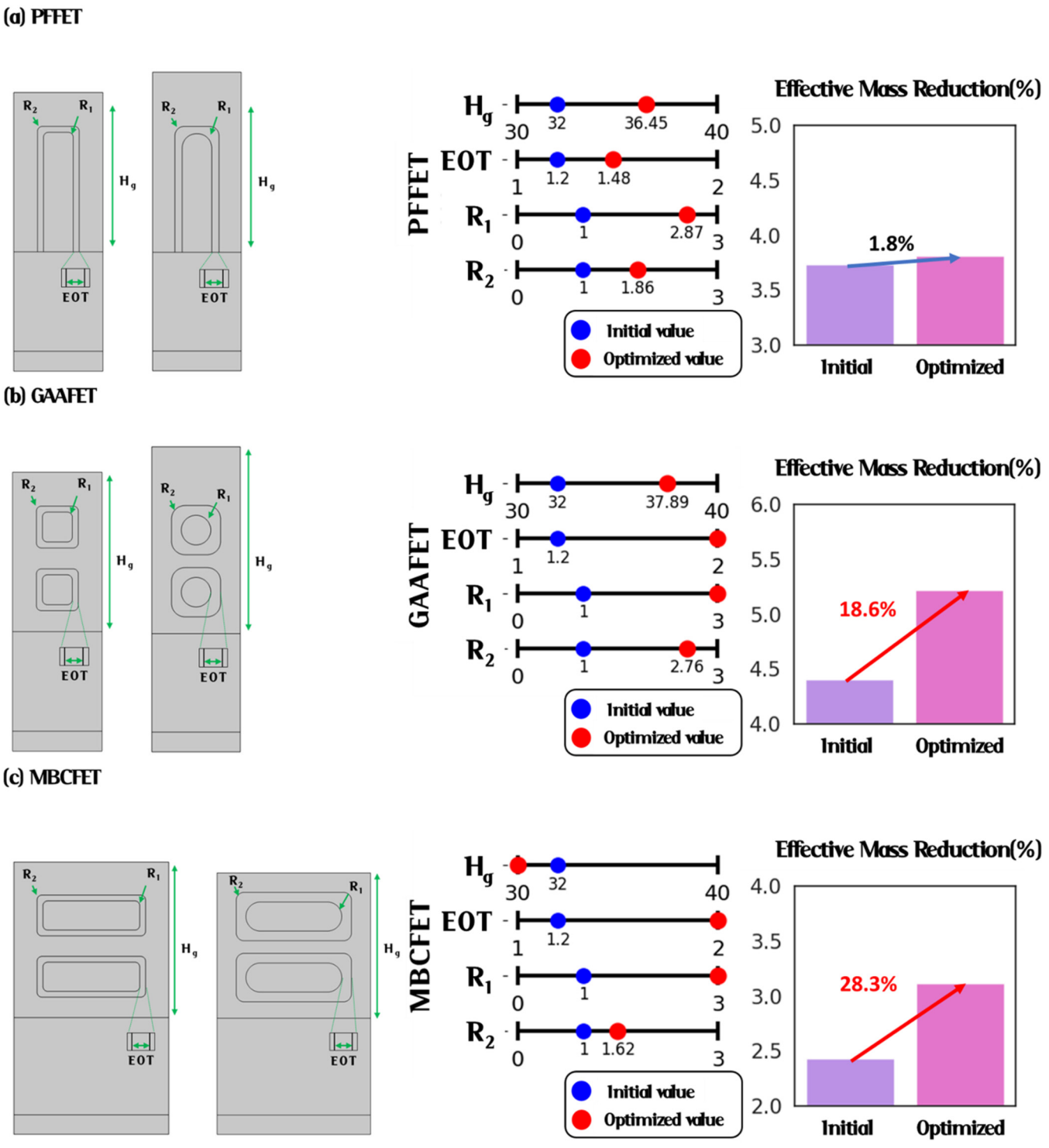

FIG. 6. Geometry of the strain-optimized structure, range of each geometry parameter, and improvement of effective mass reduction for (a) PFFET, (b) GAAFET, and (c) MBCFET.

performance improvement achieved. For all structures, the most significant change was observed in the parameters R_1, which was a critical factor for the electron effective mass decrease in the previous result. The electron effective mass of GAAFET and MBCFET decreased by 18.6% and 28.3%, respectively, while the electron effective mass of PFFET decreased by only 1.8%. This discrepancy is attributed to the structural differences between these devices. Specifically, the vertically elongated Si channel in PFFET results in strong compressive yy-strain, limiting the effectiveness of tensile xx-strain adjustments. In contrast, both GAAFETs and MBCFETs benefit from having two channels and smaller heights, which allow for more effective strain distribution. Furthermore, MBCFET's longer horizontal Si channels compared to GAAFET enabled even greater improvements through geometric optimization. These results demonstrate the significant impact of geometric optimizations on reducing the electron effective mass in GAAFET and MBCFET structures, which, in turn, leads to increased mobility. This increased mobility enhances semiconductor device performance by enabling faster and more efficient electron transport through the channel, highlighting their potential to enhance semiconductor device performance.

In summary, our workflow provides an optimization strategy for conventional 3D MOSFET systems by theoretically engineering thermal-induced strain. This approach has the potential to significantly enhance device performance. We believe that this theoretical framework can be applied to other devices where strain engineering is crucial, thereby enhancing its broad applicability. However, given that our model is confined to thermal strain, its effectiveness may be limited in systems where lattice misfits, impurity effects, and non-uniform deformations are significant.

IV. CONCLUSION

We simulated 3D MOSFET devices using FEM and DFT calculations to explore the impact of nanoscale thermal-induced strains and their relationship with electron effective mass. FEM analysis, incorporating non-diffusive nanoscale heat transport effects, revealed that EOT is the most critical parameter affecting strain in PFFET structures, while R_1 plays a dominant role in other configurations. To further investigate the impact of geometric changes on the electron effective mass, we employed DFT calculations. These calculations provided a new insight: across all structures, R_1 emerged as the paramount factor in reducing the electron effective mass, contrary to the initial findings from the strain analysis. Based on these findings, we optimized the structures for performance improvement by developing metamodels. Subsequent optimization using these metamodels demonstrated that adjustments to geometry parameters, particularly in GAAFET and MBCFET structures, led to reductions in electron effective mass by 18.6% and 28.3%, respectively. This reduction leads to a significant improvement in mobility, directly enhancing the speed and efficiency of the MOSFET structures. Such optimizations underscore the necessity for tailored optimization strategies across different MOSFET configurations to substantially enhance overall device performance. The insights from this research not only contribute to the theoretical understanding of strain effects at the nanoscale but also guide the design of next-generation semiconductor devices with optimized performance, aiding in the development of more efficient and robust semiconductor technologies.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Ji Hoon Hong: Project administration (equal); Writing – original draft (equal). **Min Sung Kang:** Project administration (equal); Writing – original draft (equal). **Inho Ha:** Supervision (equal). **Hong-Lae Park:** Supervision (equal). **Kyungwook Park:** Supervision (equal). **Joohyun Jeon:** Supervision (equal). **Wonseok Yoo:** Supervision (equal). **Jueun Kim:** Supervision (equal). **Chunhyung Chung:** Supervision (equal). **Sung Min Park:** Supervision (equal). **Sung Beom Cho:** Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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