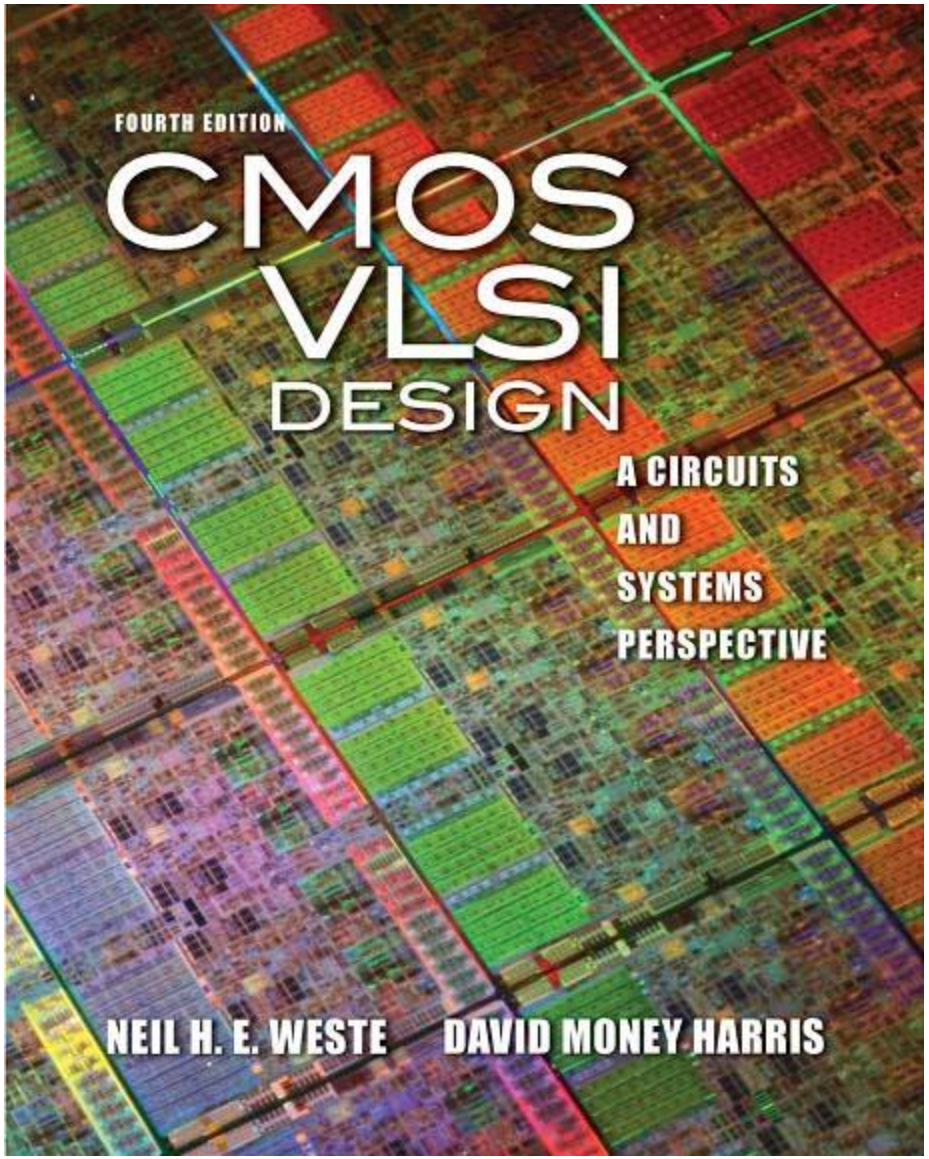


Review for Week 1

Layout of the CMOS

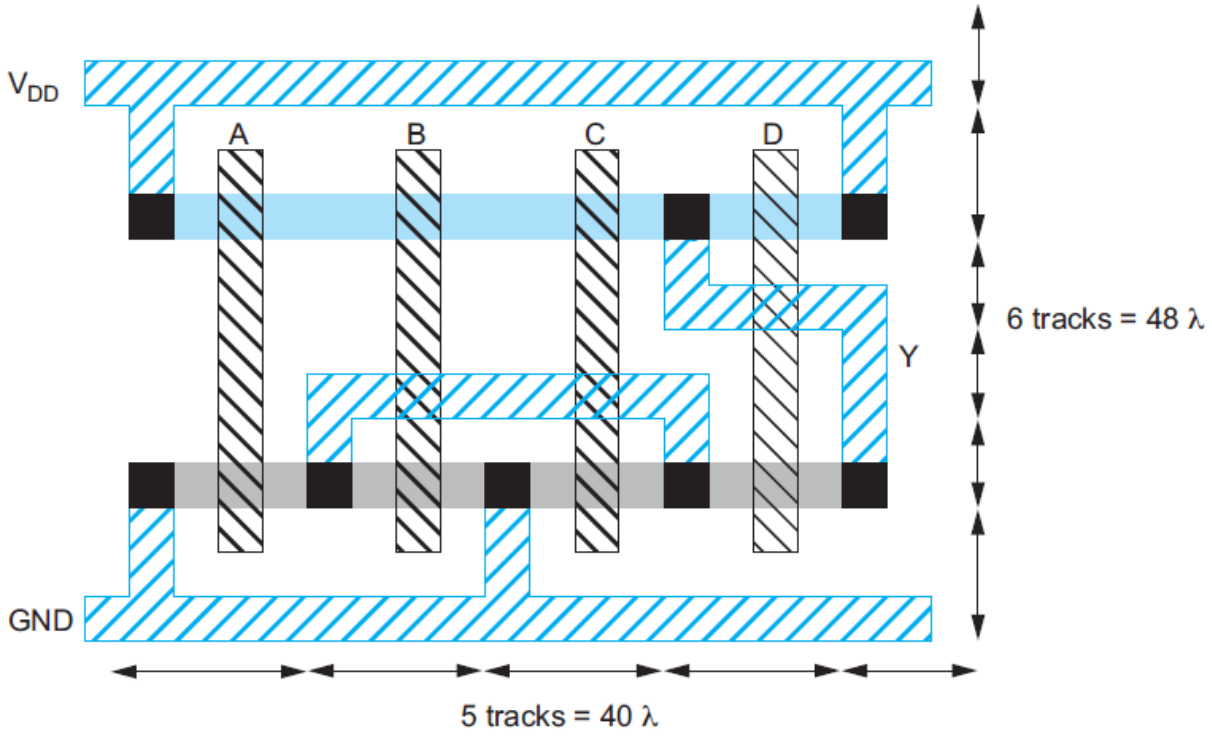
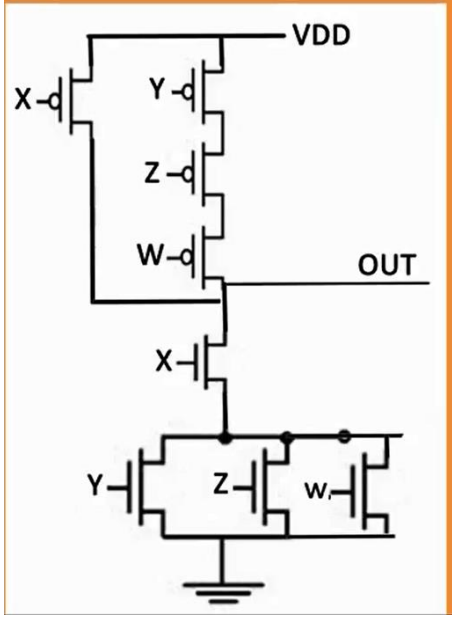


FIGURE 1.47 CMOS compound gate for function $Y = \overline{(A + B + C) \cdot D}$

Page 29 in Ref book CMOS_VLSI_design_4th_Edition

Stick Diagram Design of a Complemetary Static CMOS Device

$$F = \overline{X(Y+Z)+WX} = \overline{X(Y+Z+W)}$$

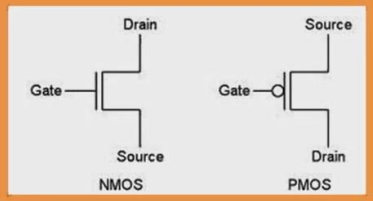


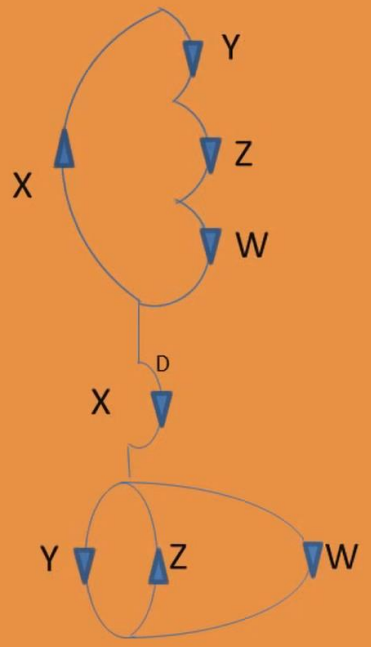
Summary of Steps to be followed:
1. Always start from the NMOS section.(i.e Bottom to top approach)
2. Draw the transistors as per the convention Which means "•" or "+" convention as per the transistor.
3. Label each transistor with the variables mentioned in the function.
4. Label the Power Supply V_{DD} and ground connection

Select the Euler's path

Selecting the Euler's path for the stick Diagram

Rules for Finding the Euler's Path
1. Represent each NMOS transistor in curvy lines.
2. Represent each PMOS transistor in curvy lines.
3. Select the path such that no line is traversed TWICE.
4. Consider the following drawing. Here we have selected the path X – Y – Z - W.
5. Write the source and drain terminals for each NMOS and PMOS transistor.





Select the Euler's path

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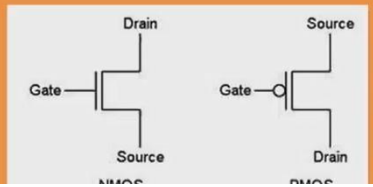
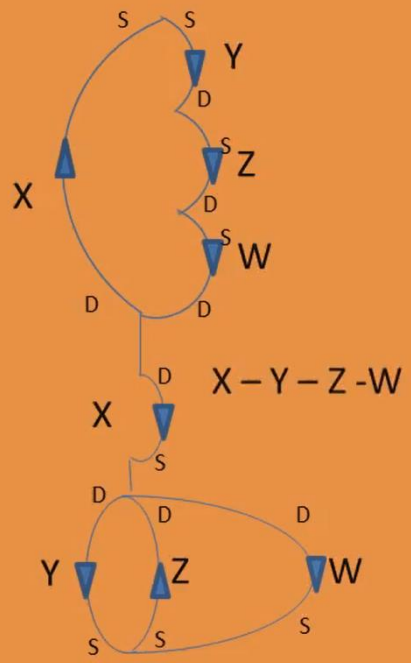
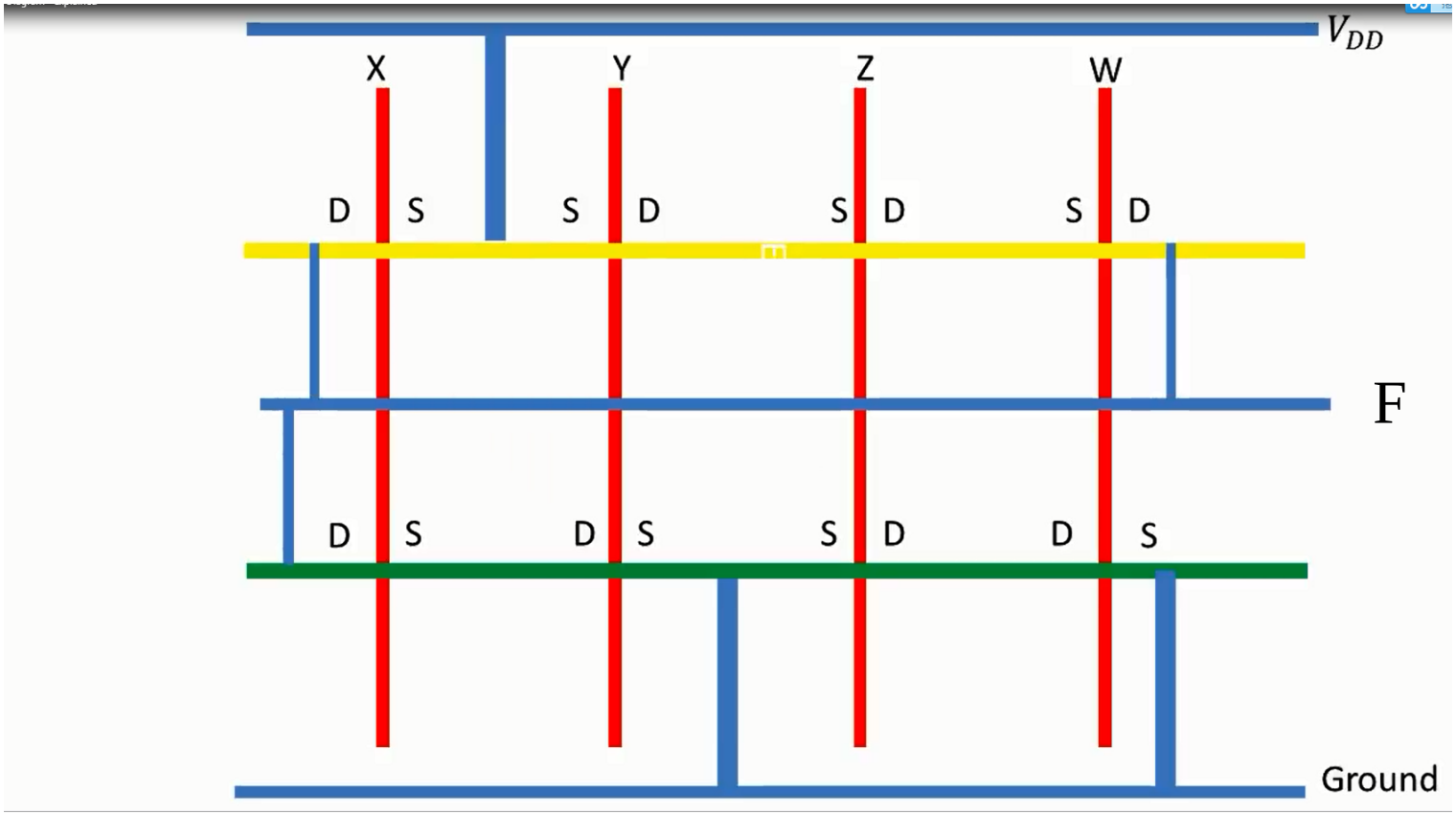
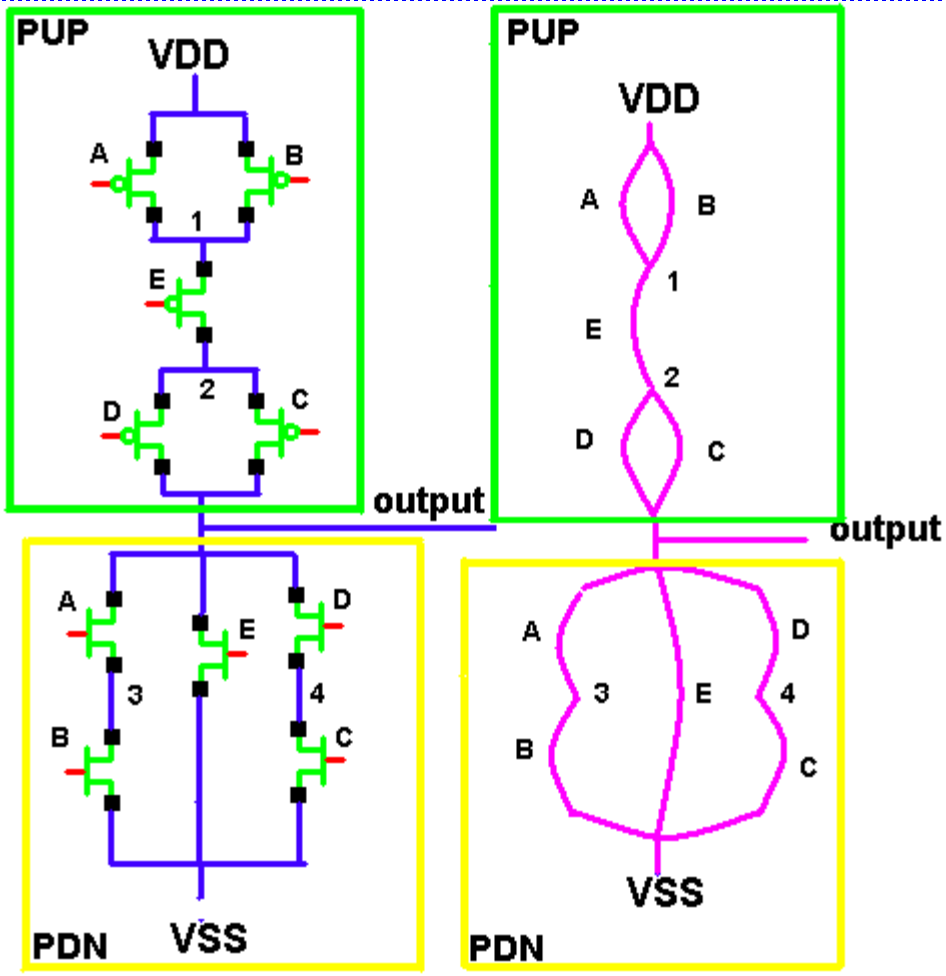




Stick diagame

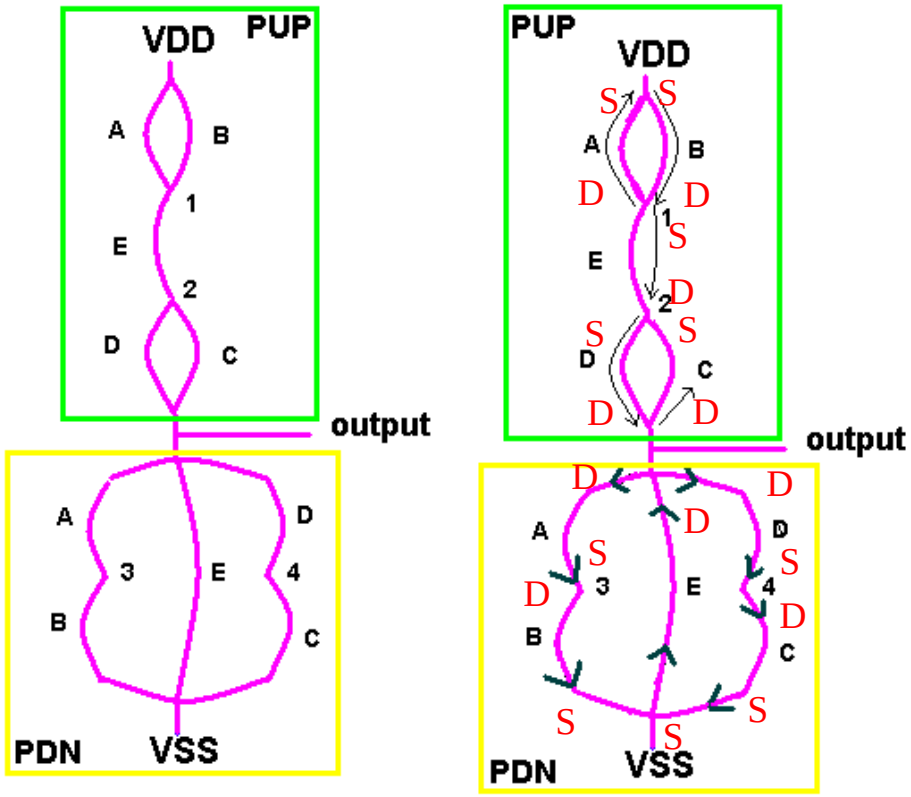


Schematic 2



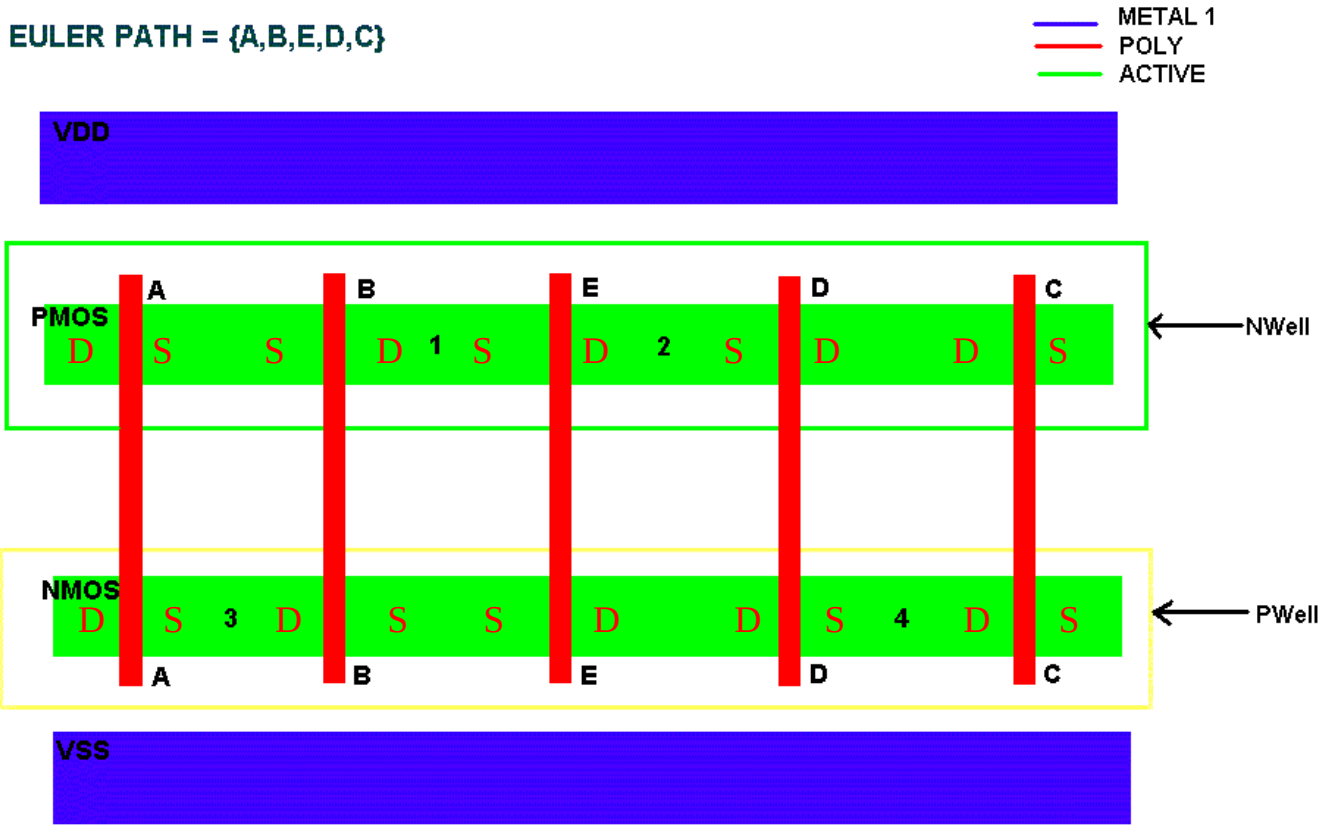
$$F = \overline{(AB) + E + (CD)}$$

Euler Path

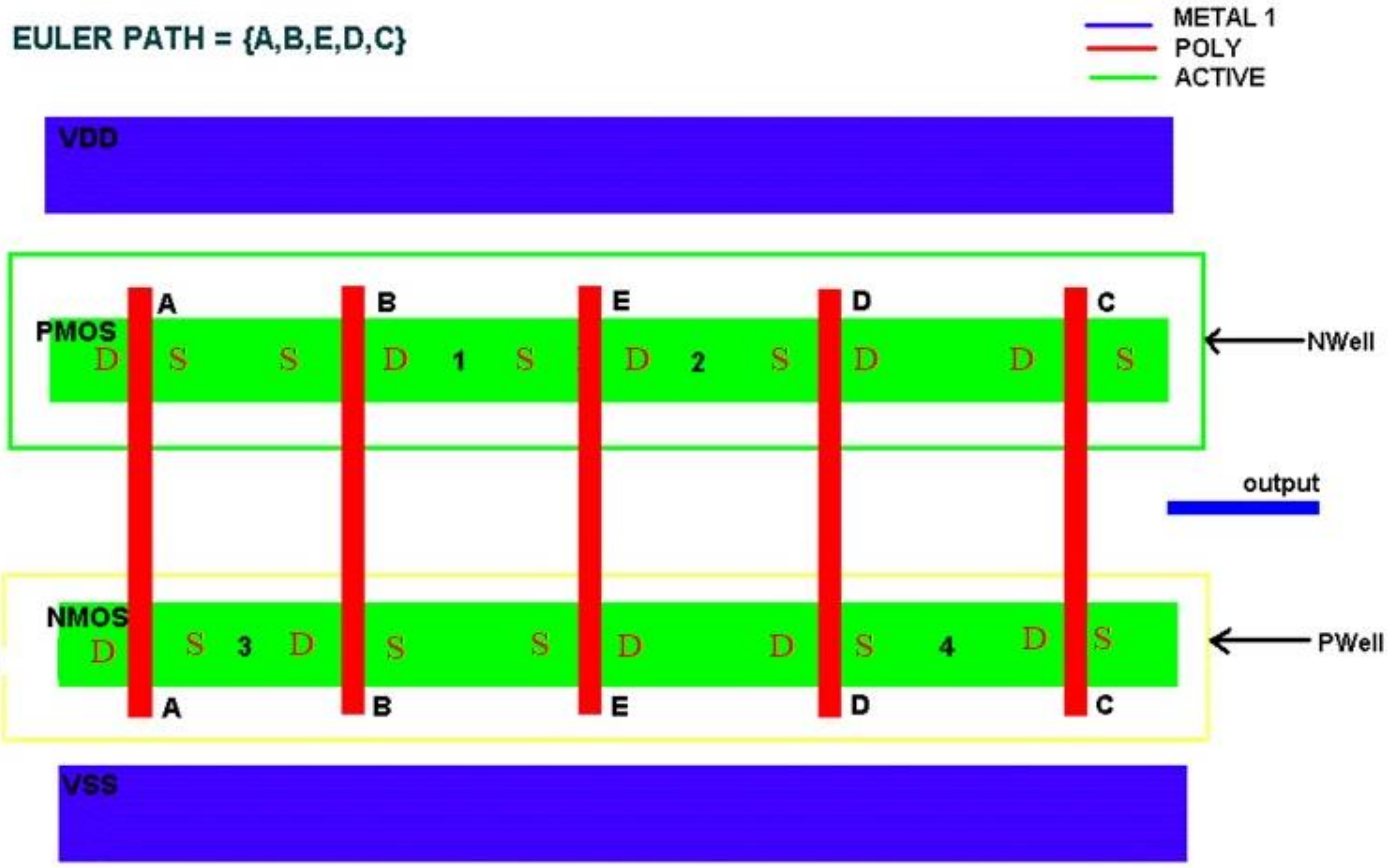


EULER PATH = {A,B,E,D,C}

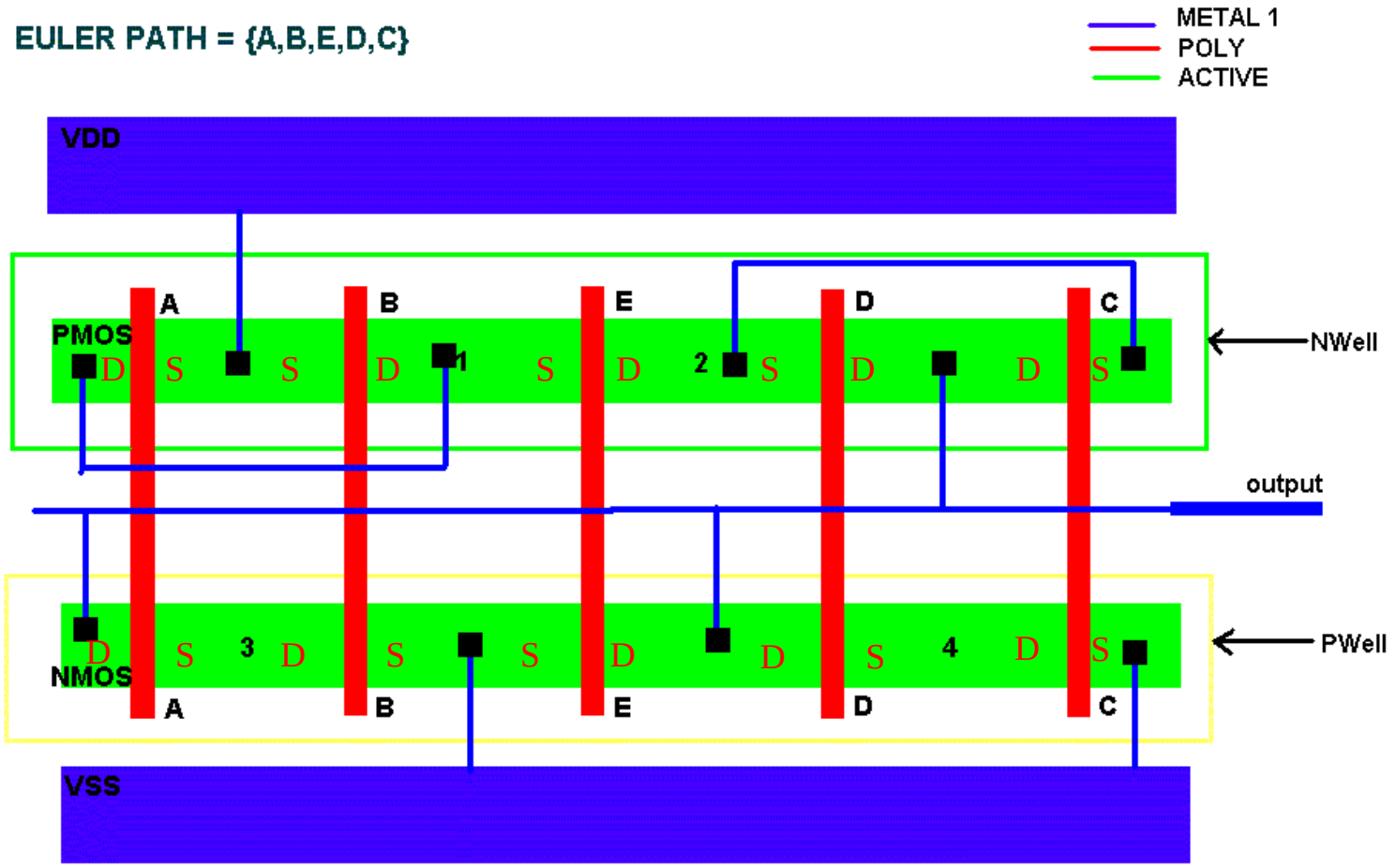
Connection label layout



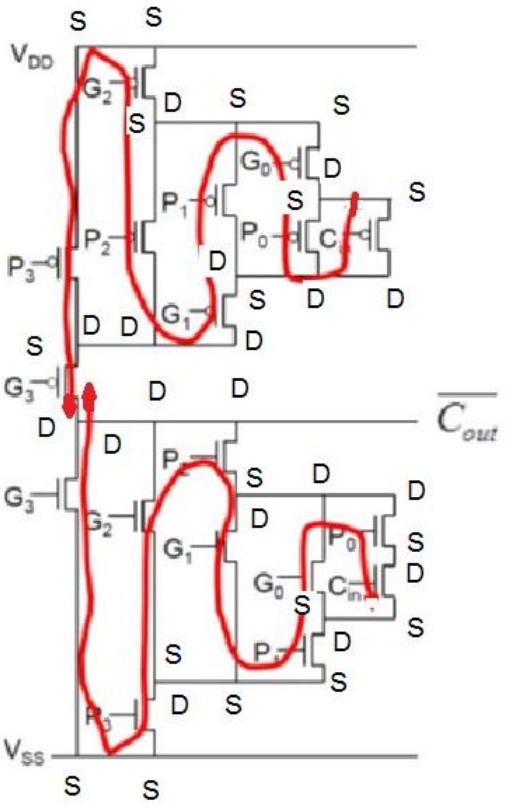
VDD, VSS and Output Labels



Stick Diagram, Interconnected



Schematic 3



$C_{out}=G_3+P_3(G_2+P_2(G_1+P_1(G_0+P_0C_{in})$

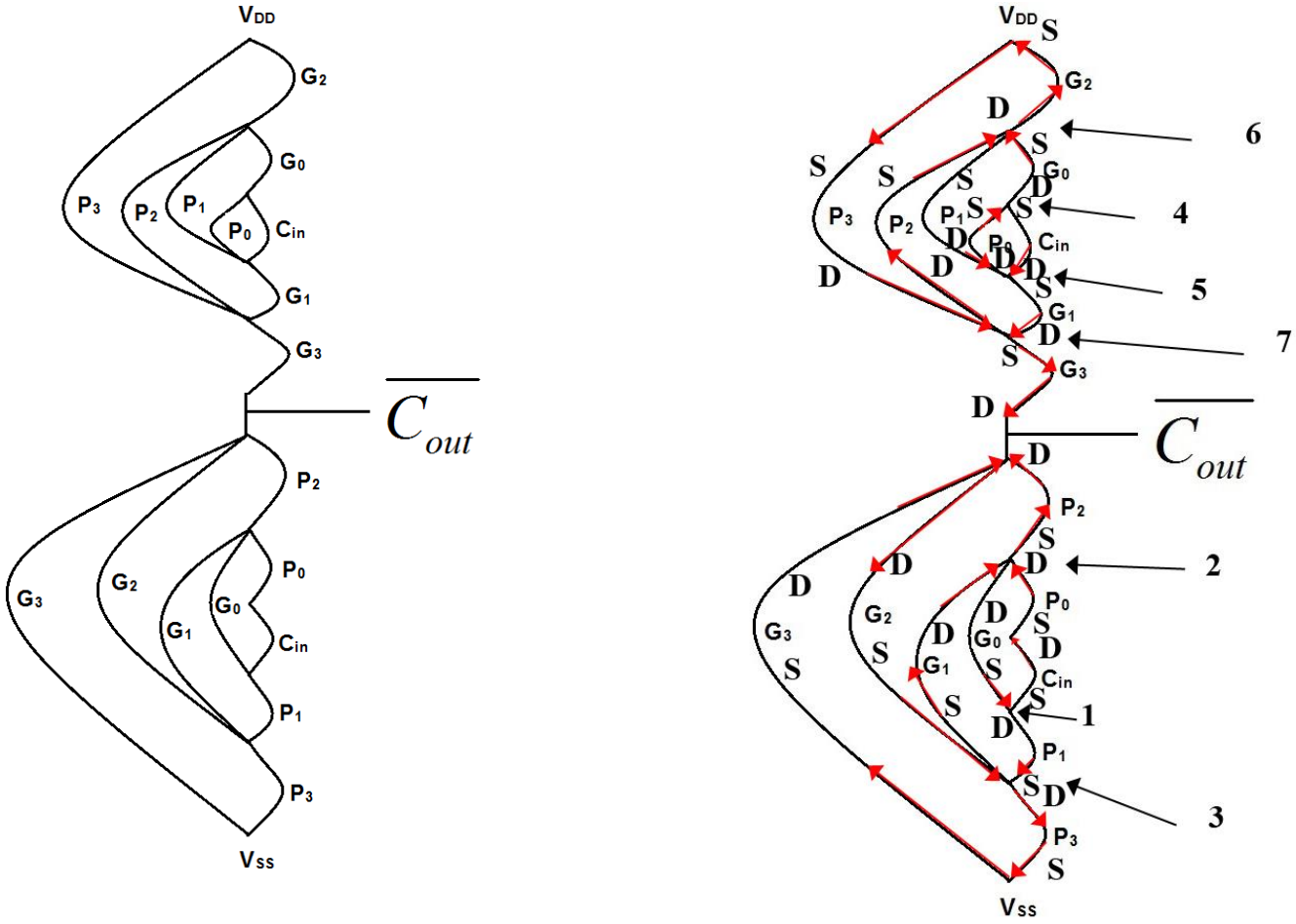
1.20 A carry lookahead adder computes $G = G_3 + P_3(G_2 + P_2(G_1 + P_1G_0))$. Consider designing a compound gate to compute $\overline{G}$.

a) sketch a transistor-level schematic

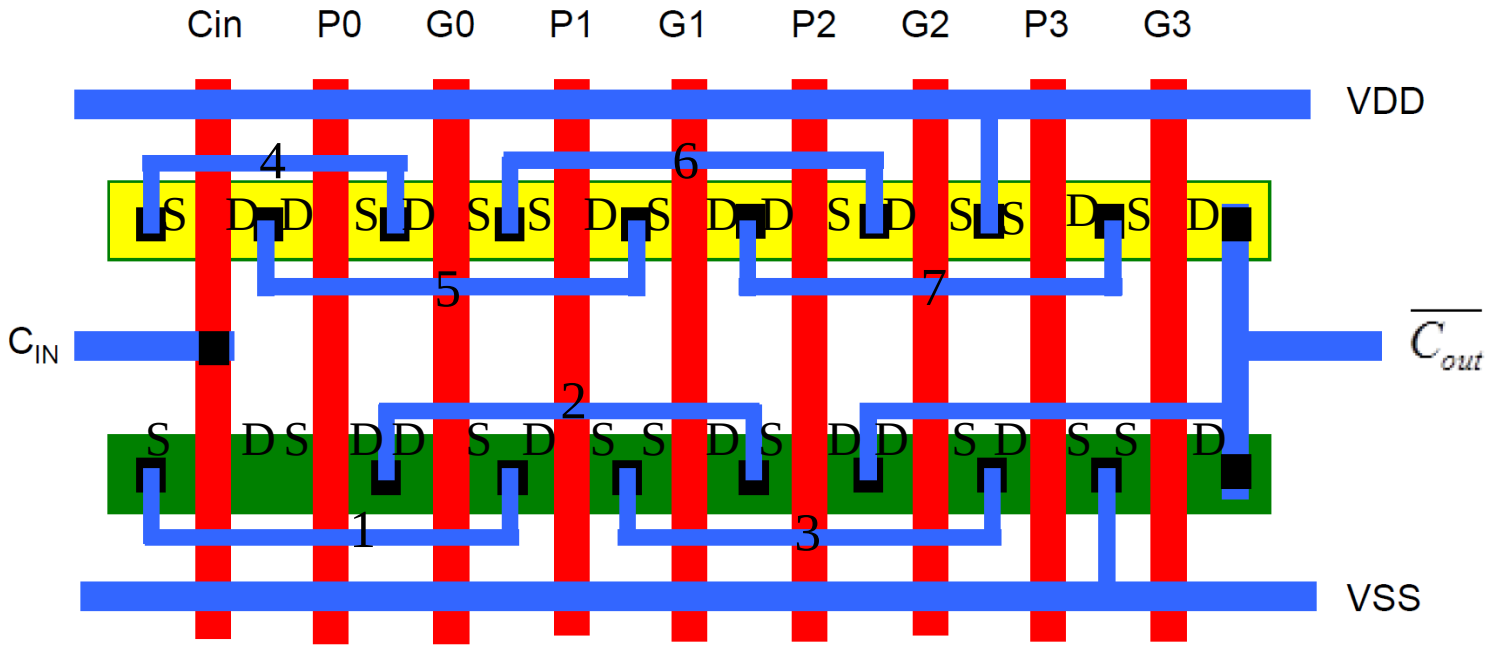
b) sketch a stick diagram

c) estimate the area from the stick diagram

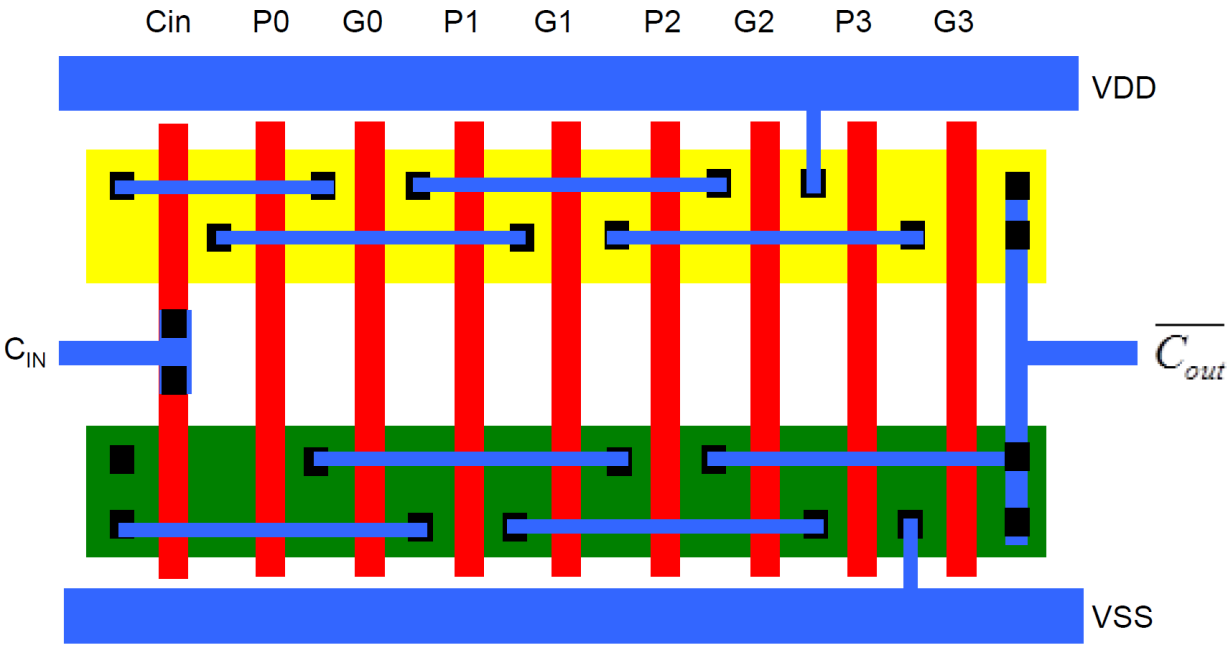
Euler Path


VDD
G2
G0
P3
P2
P1
P0
Cin
G1
G3
Cout
P2
P0
G3
G2
G0
G1
Cin
P1
P3
VSS
VDD
S
G2
D
6
S
G0
S
S
S
D
P3
P2
P1
S
4
D
P0
Cin
D
D
D
D
5
S
G1
D
7
S
G3
D
Cout
D
P2
S
D
D
2
D
P0
G3
G2
D
S
D
S
G0
D
G1
S
Cin
S
1
S
D
P1
S
D
3
P3
S
VSS

Stick diagram



The layout again, a bit more refined!



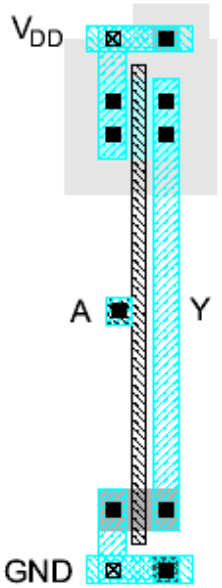
NOTE: The layout is very compact and elegant, however, only post-layout circuit simulations with node capacitances extracted from the layout will reveal the exact performance of the cell.

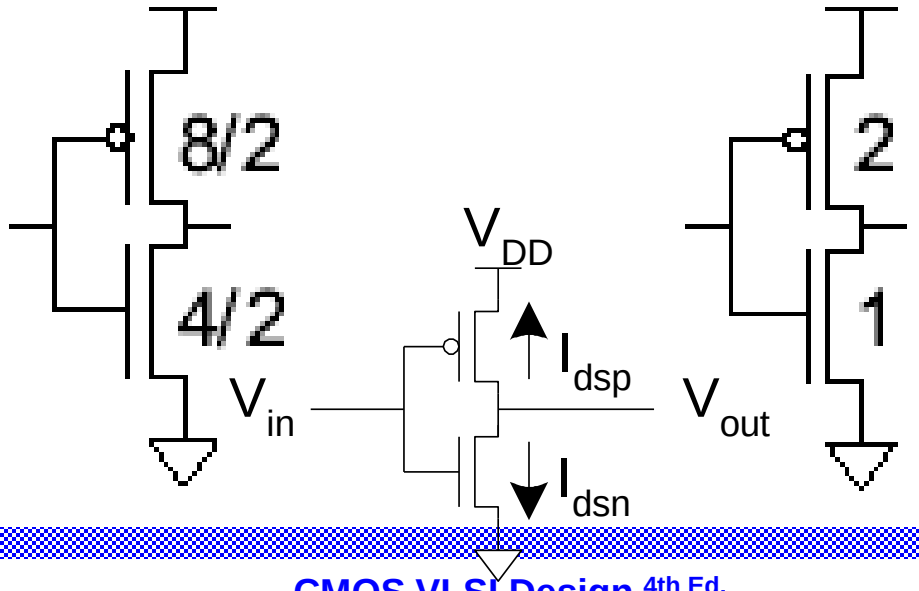
General Rules for CMOS Layout

- General Rules for CMOS Layout
- Run supply lines for VDD and VSS along the upper and lower cell boundaries
- Run a vertical poly wire for each input signal
- Order the poly wires to obtain maximal connectivity between transistors through abutment of source/drain areas. Connected transistors then form transistor segments
- Place n-transistor segments close to the bottom VSS supply rail and p-transistors close to the top VDD supply rail
- Wires necessary to complete the design are drawn in metal, poly, or, if necessary in diffusion (for instance when connecting segments to the supply rails
- Remember to keep internal node capacitances at a minimum

Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long

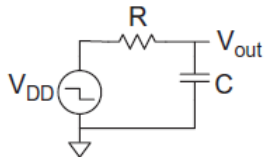


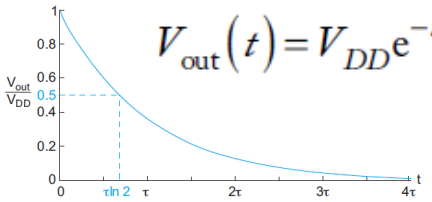


$$I_{ds} = \frac{Q_{channel}}{L/v}$$
$$= \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$
$$= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds}$$

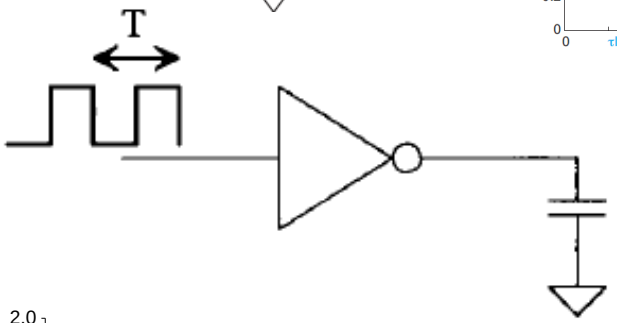
$$\beta = \mu C_{ox} \frac{W}{L};\ V_{GT} = V_{gs} - V_t$$

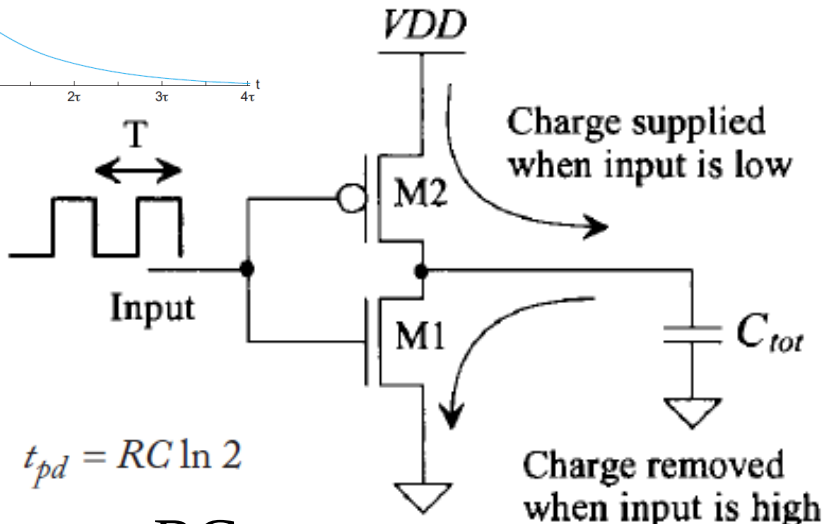
Inverter with a capacitor

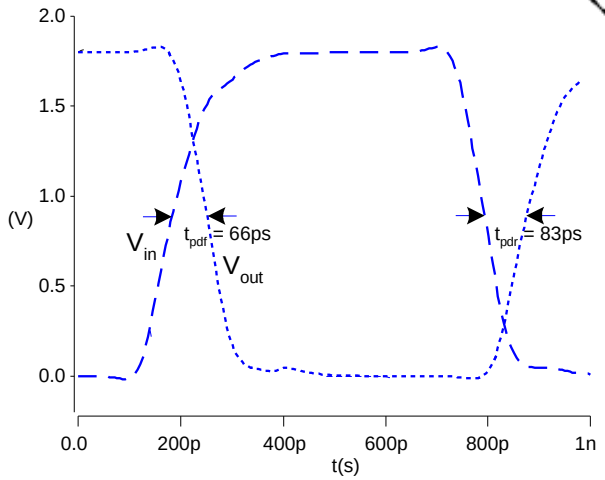




$$V_{out}(t) = V_{DD}e^{-t/\tau}$$







$$t_{pd} = RC\ln 2$$

$$t_{pd} = RC$$

$$I_{ds} = V_{ds}/R$$

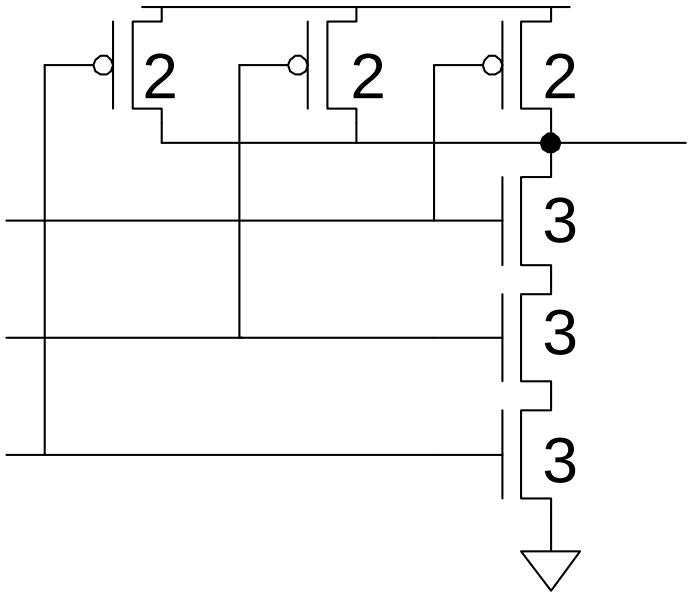
$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})}$$

$$\mu_n / \mu_p = 2$$

$$W_p = 2W_n$$

Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



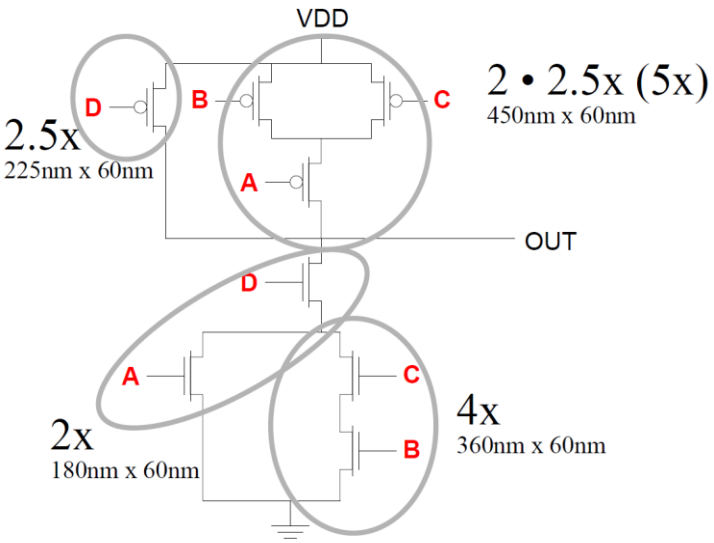
Size CMOS transistor in Circuit

Consider the function out = $\overline{((a + bc) \cdot d)}$. **Draw the circuit and size the transistors: size all NMOS and PMOS transistors so that the PUN and PDN each has equivalent resistance to a minimum-sized MOSFET, and then take into account the fact that $\mu_n = r \cdot \mu_p$ where $r = 2.5$ (i.e. the resistance of a unit PMOS device is 2.5 times that of a unit NMOS device).**

Important: Assume the circuit is implemented in a 60nm technology and that the dimensions of a **minimum-sized MOSFET** in this technology are **90nm width x 60nm length**. Express the dimensions of each MOSFET in the optimized circuit in nanometers (W nm x L nm).
I.e., what is it that you are scaling?

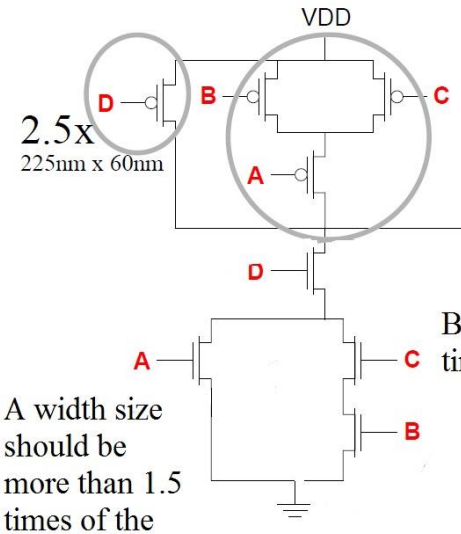
some equivalent solutions (there is more than one correct answer):

min. device: WxL = 90nm x 60nm



2 • 2.5x (5x)
450nm x 60nm

or



A, B, C width size should be 5 times of the unit size

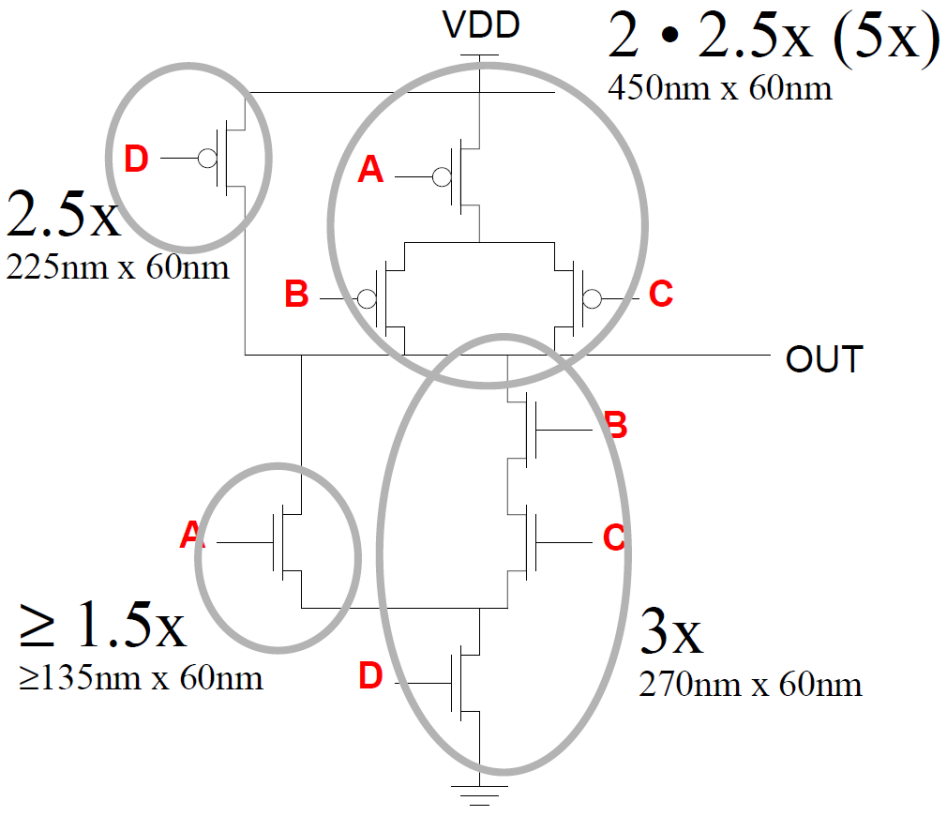
2 • 2.5x (5x)
450nm x 60nm

B, C, D width size should be 3 times of the unit size

3x
270nm×60 nm

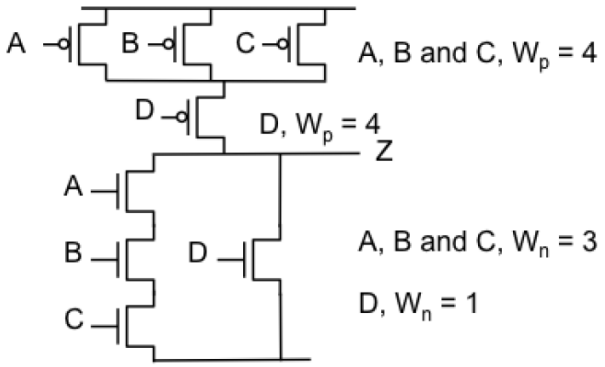
A width size should be more than 1.5 times of the unit size

≥ 1.5x
≥135nm x 60nm


VDD
2 • 2.5x (5x)
450nm x 60nm
D
A
2.5x
225nm x 60nm
B
C
OUT
B
A
C
≥ 1.5x
≥135nm x 60nm
D
3x
270nm x 60nm

(a) Sketch the transistor-level schematic circuit diagram for a CMOS cell with the following function, using the smallest number of transistors possible:

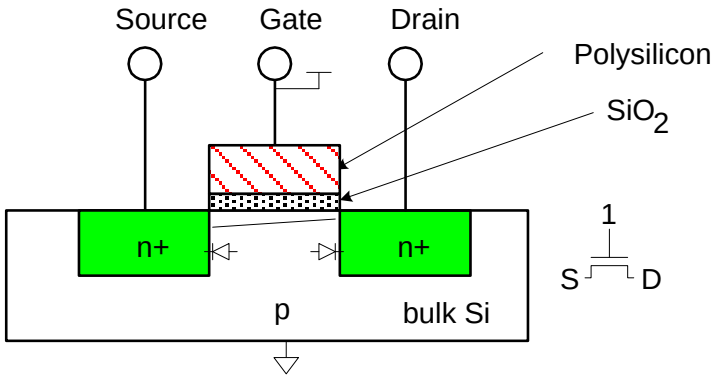
$$Z = \overline{ABC + D}$$ [8]



The design is based on a standard cell library with a "unit" inverter using $W_{ni} = 1$ and $W_{pi} = 2$. Correctly size the transistors in your circuit for part (a) of this question to match the inverter's output characteristics using a linear T-sizing method. [7]

nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



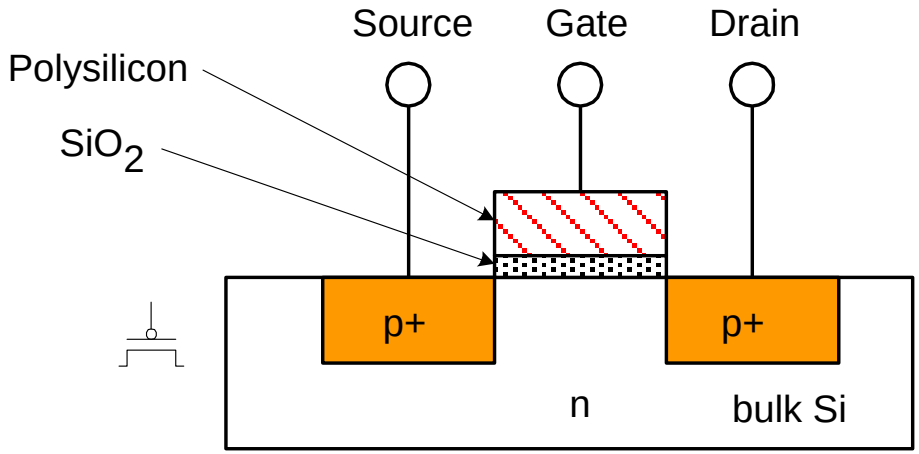
nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

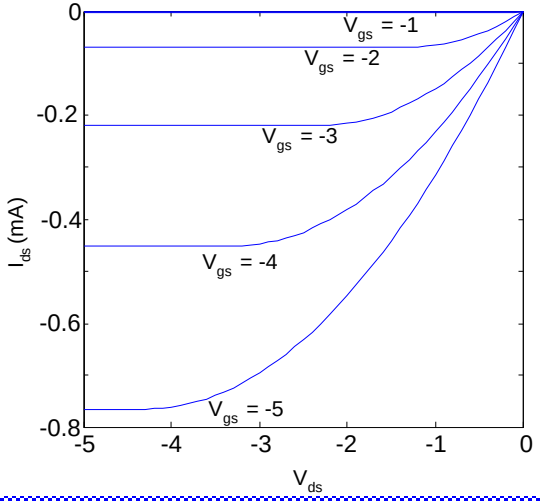
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V \cdot s$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

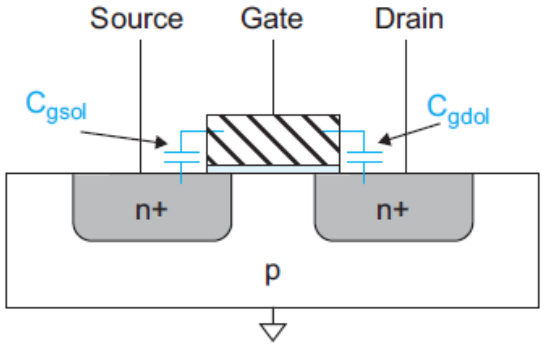


Gate Capacitance

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cut-off	$C_{ox}WL_{eff}$	C_{ov}	C_{ov}
Resistive	0	$C_{ox}WL_{eff}/2 + C_{ov}$	$C_{ox}WL_{eff}/2 + C_{ov}$
Active	0	(2/3) $C_{ox}WL_{eff} + C_{ov}$	C_{ov}

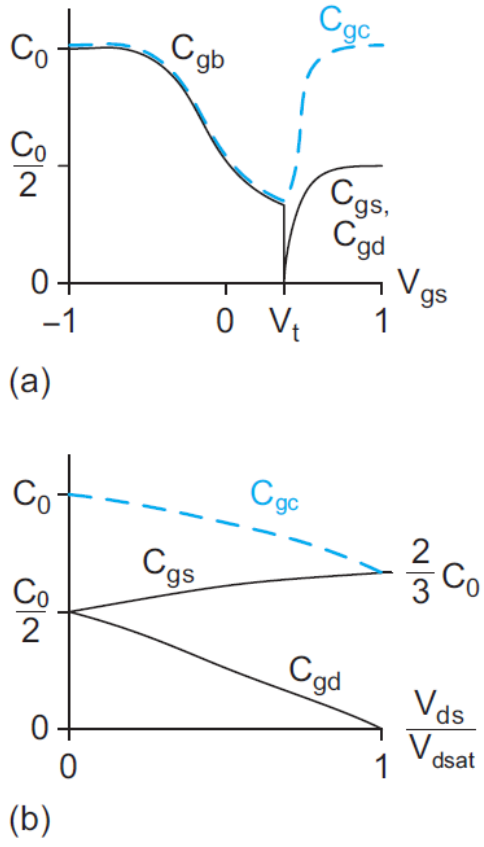
$$C_g = C_{gs} + C_{gd} + C_{gb} \approx C_0 + 2C_{gol}W$$

Parameter	Cutoff	Linear	Saturation
C_{gb}	$\leq C_0$	0	0
C_{gs}	0	$C_0/2$	2/3 C_0
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	2/3 C_0



$$C_{gsol(\text{overlap})} = C_{gsol}W$$
$$C_{gdol(\text{overlap})} = C_{gdol}W$$

Intrinsic gate capacitance vs V_{gs} and V_{ds}



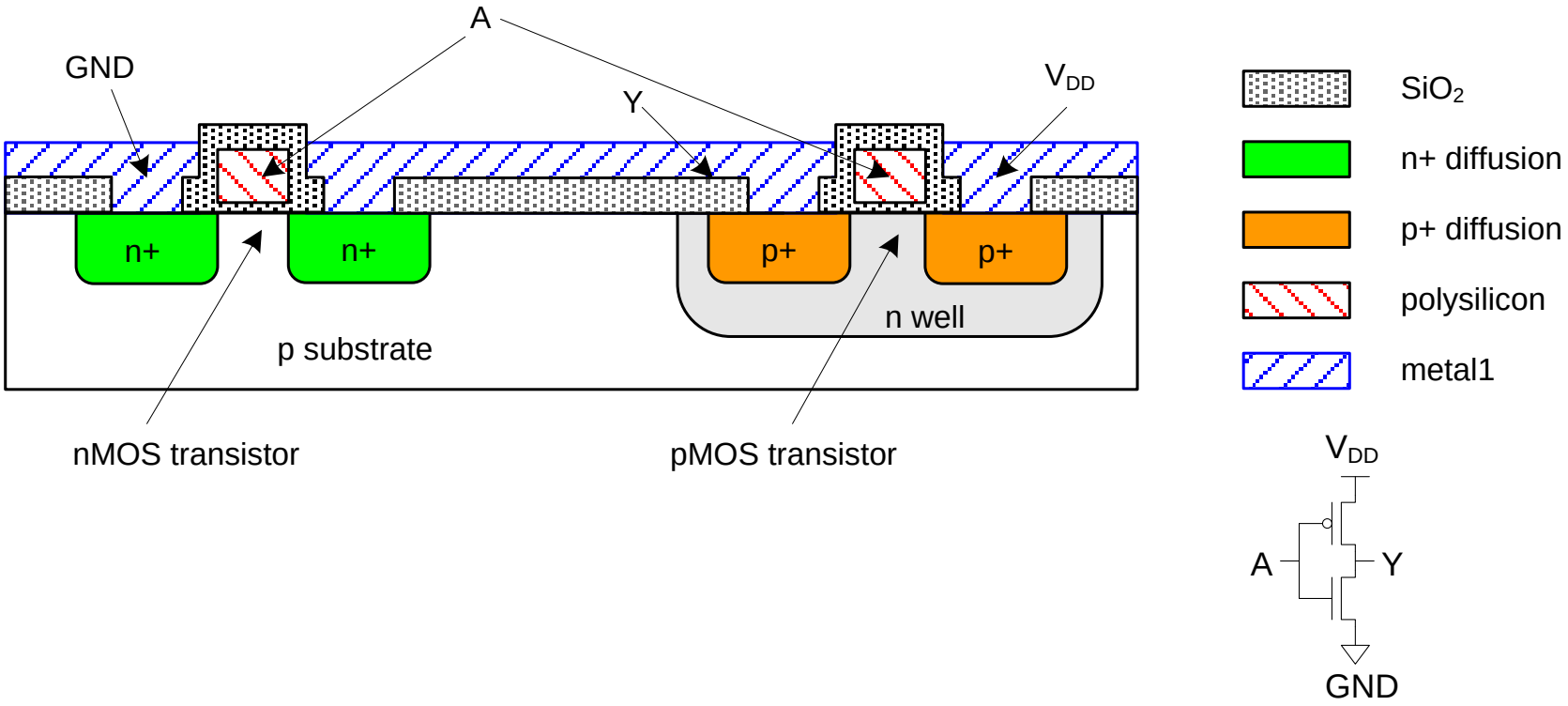
1. *Cutoff.* When the transistor is OFF ($V_{gs} < V_t$), the channel is not inverted and charge on the gate is matched with opposite charge from the body. This is called C_{gb}, the gate-to-body capacitance. For negative V_{gs}, the transistor is in accumulation and $C_{gb} = C_0$. As V_{gs} increases but remains below a threshold, a depletion region forms at the surface. This effectively moves the bottom plate downward from the oxide, reducing the capacitance, as shown in Figure 2.9(a).

2. *Linear.* When $V_{gs} > V_t$, the channel inverts and again serves as a good conductive bottom plate. However, the channel is connected to the source and drain, rather than the body, so C_{gb} drops to 0. At low values of V_{ds}, the channel charge is roughly shared between source and drain, so $C_{gs} = C_{gd} = C_0/2$. As V_{ds} increases, the region near the drain becomes less inverted, so a greater fraction of the capacitance is attributed to the source and a smaller fraction to the drain, as shown in Figure 2.9(b).

3. *Saturation.* At $V_{ds} > V_{dsat}$, the transistor saturates and the channel pinches off. At this point, all the intrinsic capacitance is to the source, as shown in Figure 2.9(b). Because of pinchoff, the capacitance in saturation reduces to $C_{gs} = 2/3\ C_0$ for an ideal transistor [Gray01].

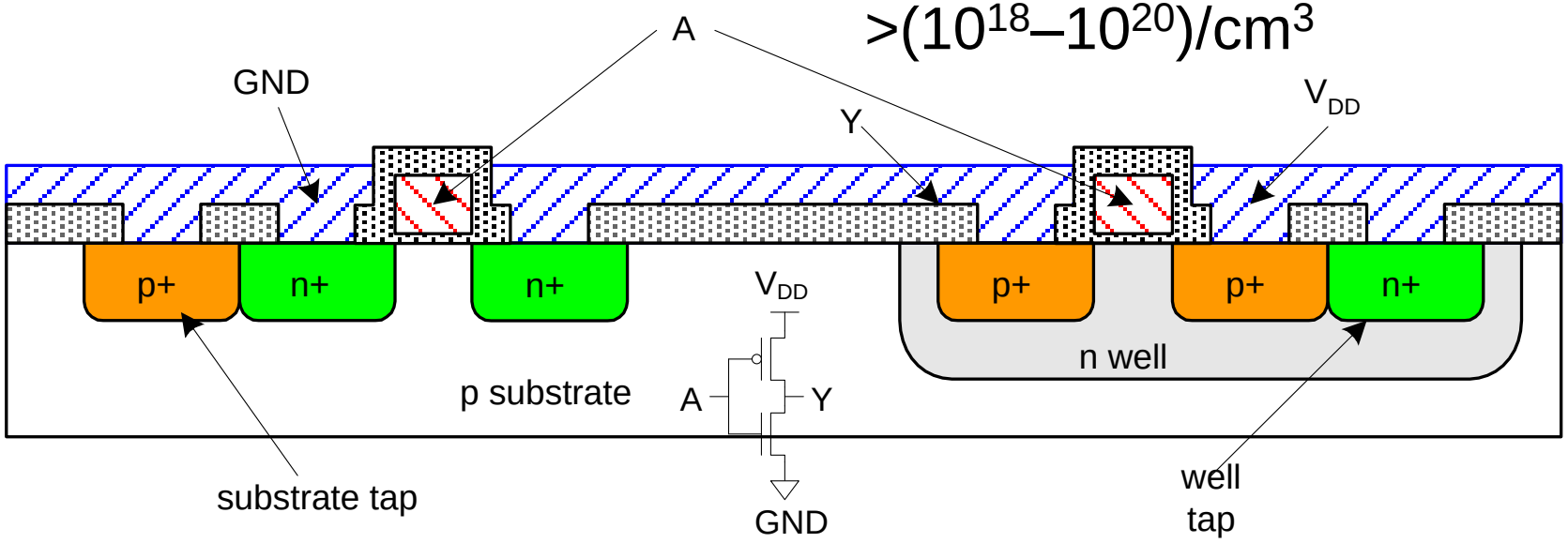
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



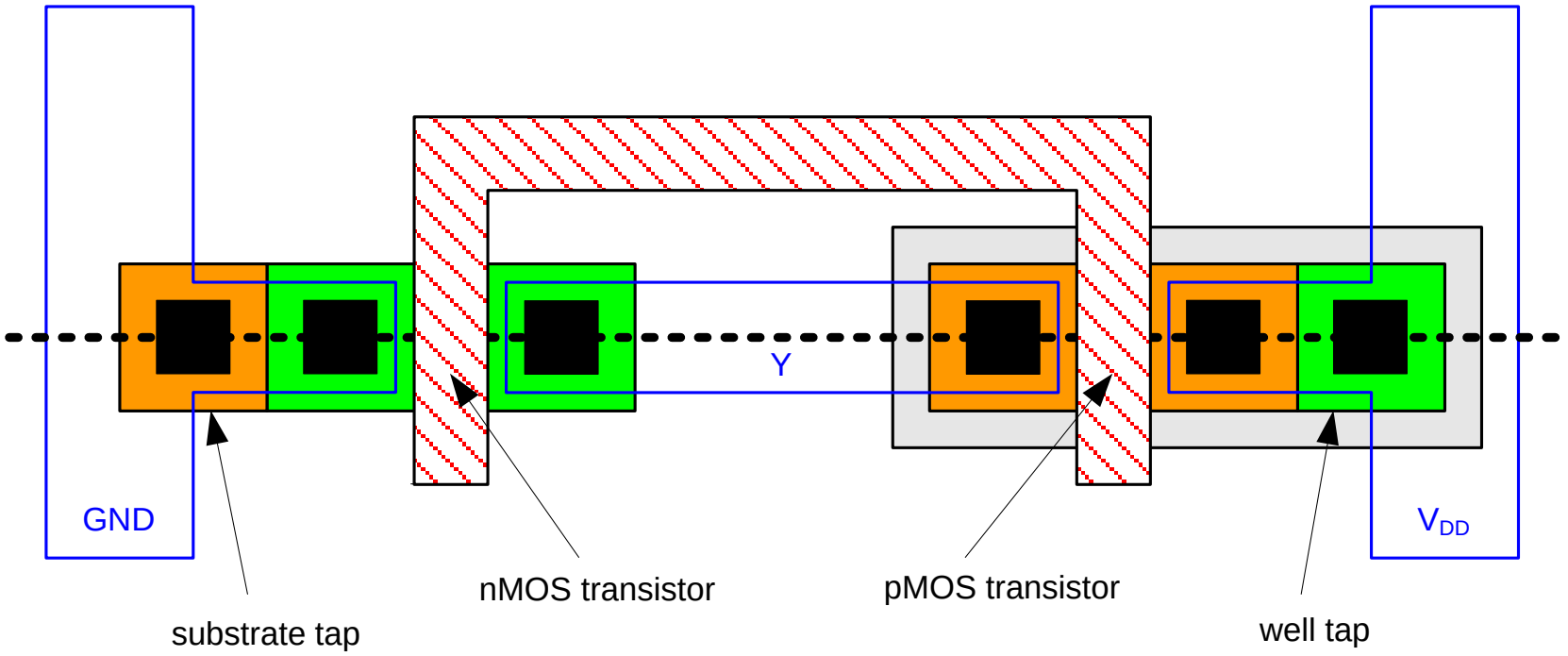
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



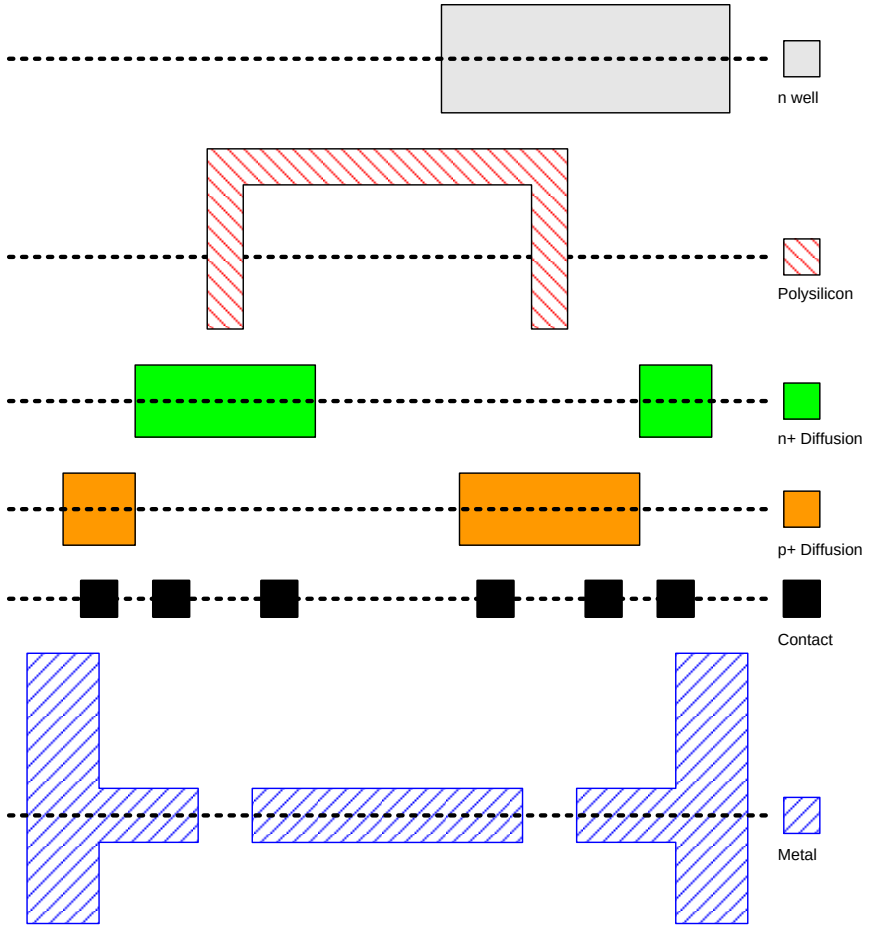
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Layout

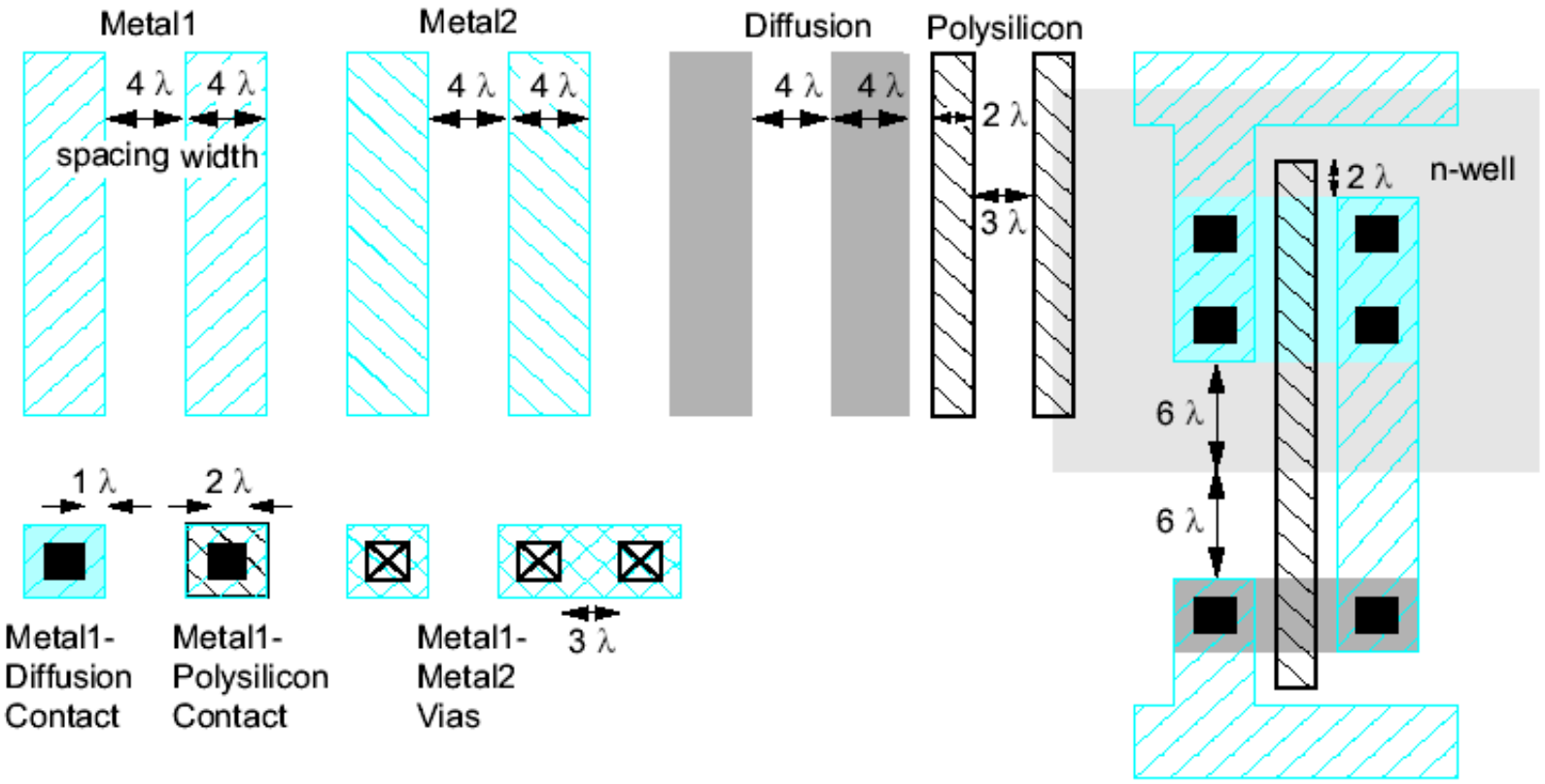
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Simplified Design Rules

- Metal and diffusion have minimum width and spacing of 4 λ.
- Contacts are 2 $\lambda \times 2\ \lambda$ and must be surrounded by 1 λ on the layers above and below.
- Polysilicon uses a width of 2 λ.
- Polysilicon overlaps diffusion by 2 λ where a transistor is desired and has a spacing of 1 λ away where no transistor is desired.
- Polysilicon and contacts have a spacing of 3 λ from other polysilicon or contacts.
- N-well surrounds pMOS transistors by 6 λ and avoids nMOS transistors by 6 λ.

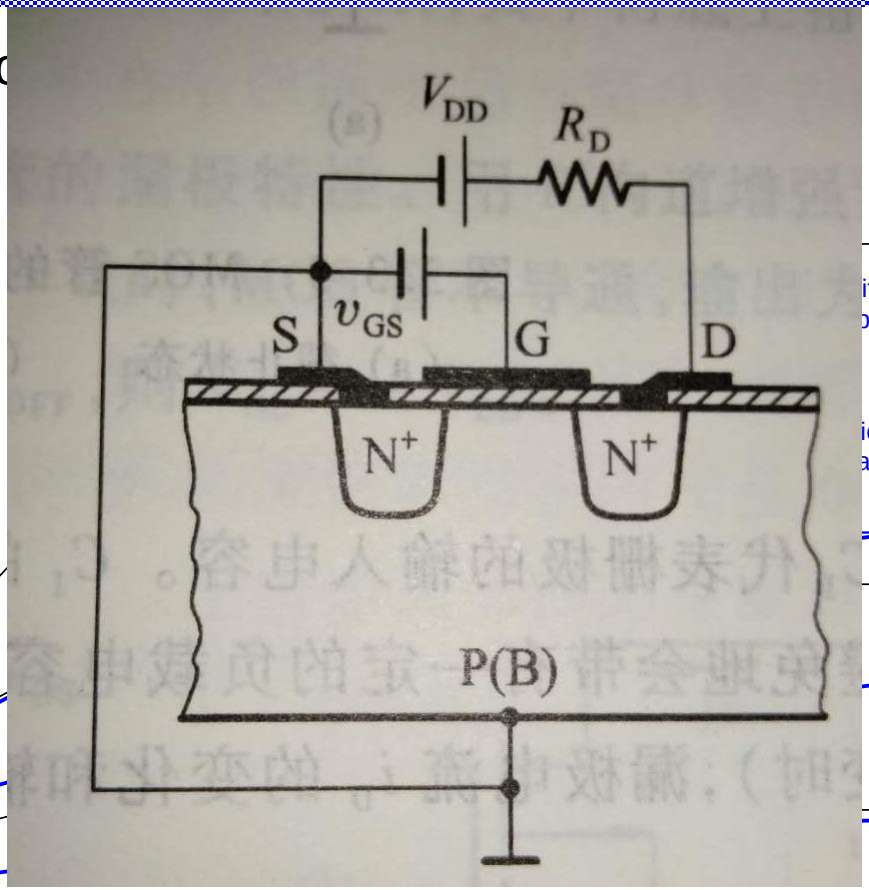
Simplified Design Rules

- Conservative rules to get you started



Ideal vs. Simulated nMOS I-V Plot

- 65 nm IBM pr

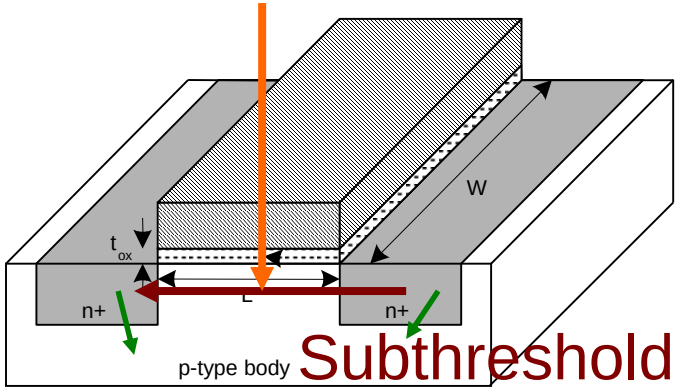


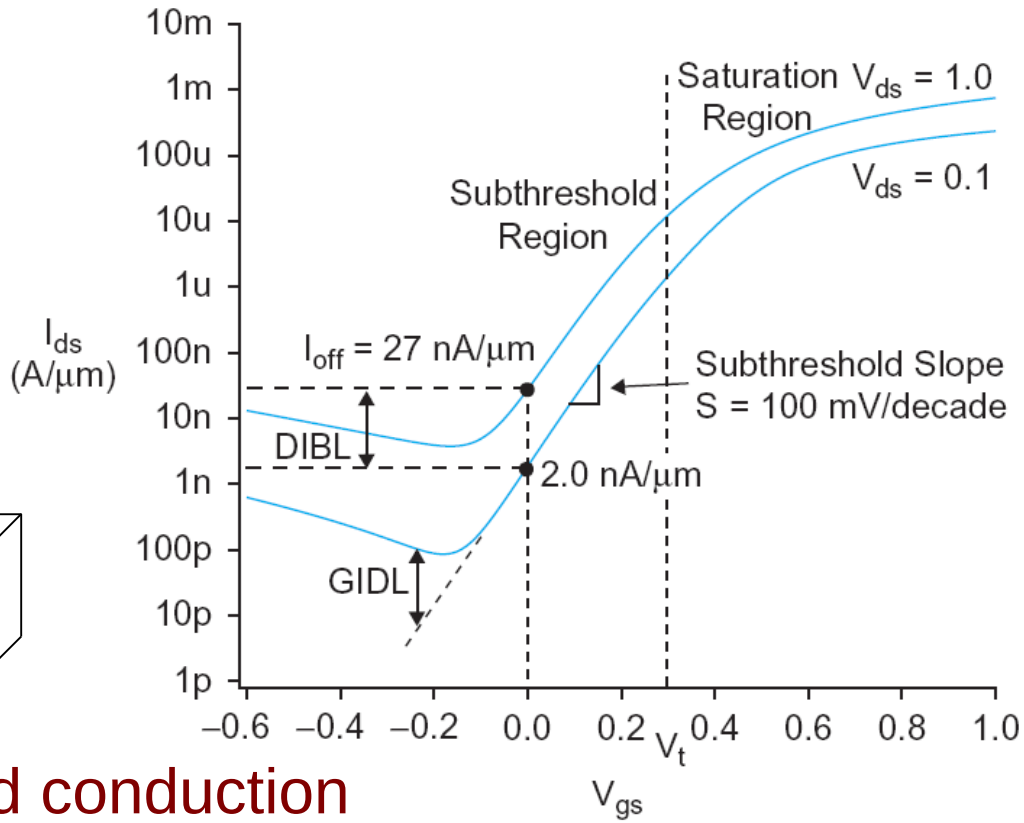
Threshold Voltage Effects

- V_t is V_{gs} for which the channel starts to invert
- Ideal models assumed V_t is constant
- Really depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

Leakage

- What about current in cutoff?
- Simulated results
- What differs?
  -





Subthreshold conduction

Junction leakage