Data Converter Architectures

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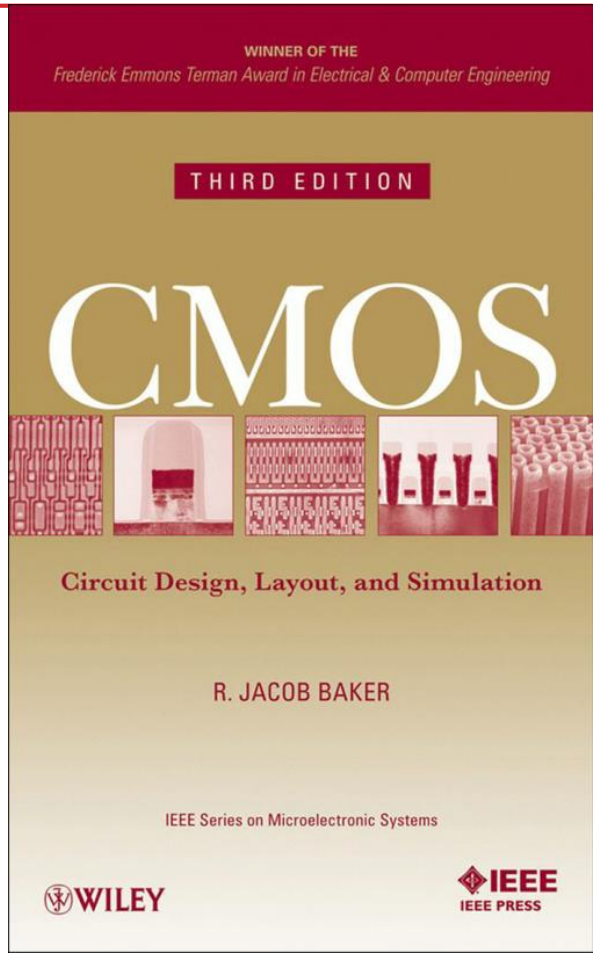
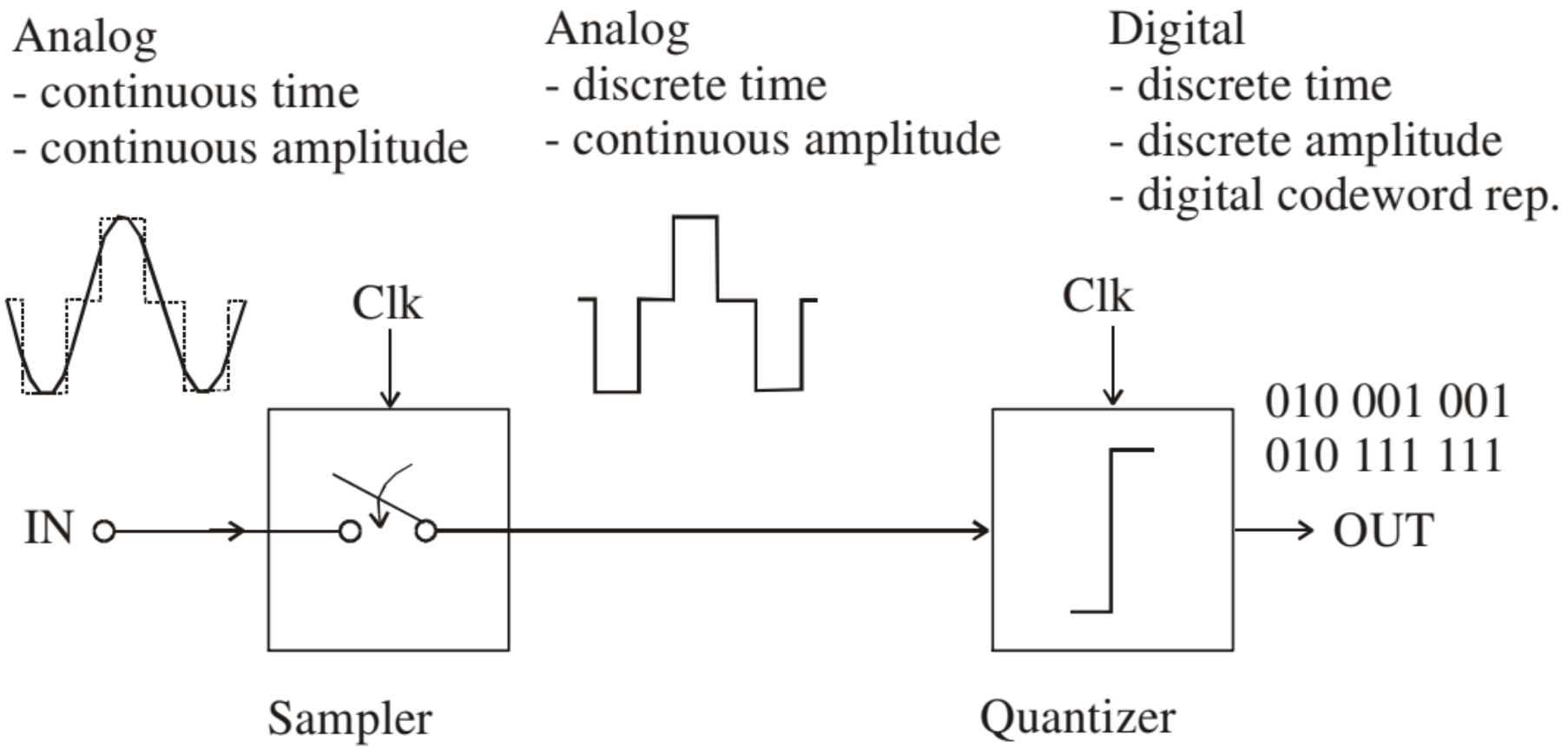


Ref book:

R. J. Baker, CMOS: circuit design, layout, and simulation(3rd Edition). Wiley-IEEE press, 2012

Principle of A/D conversion



Sampling in Time Domain

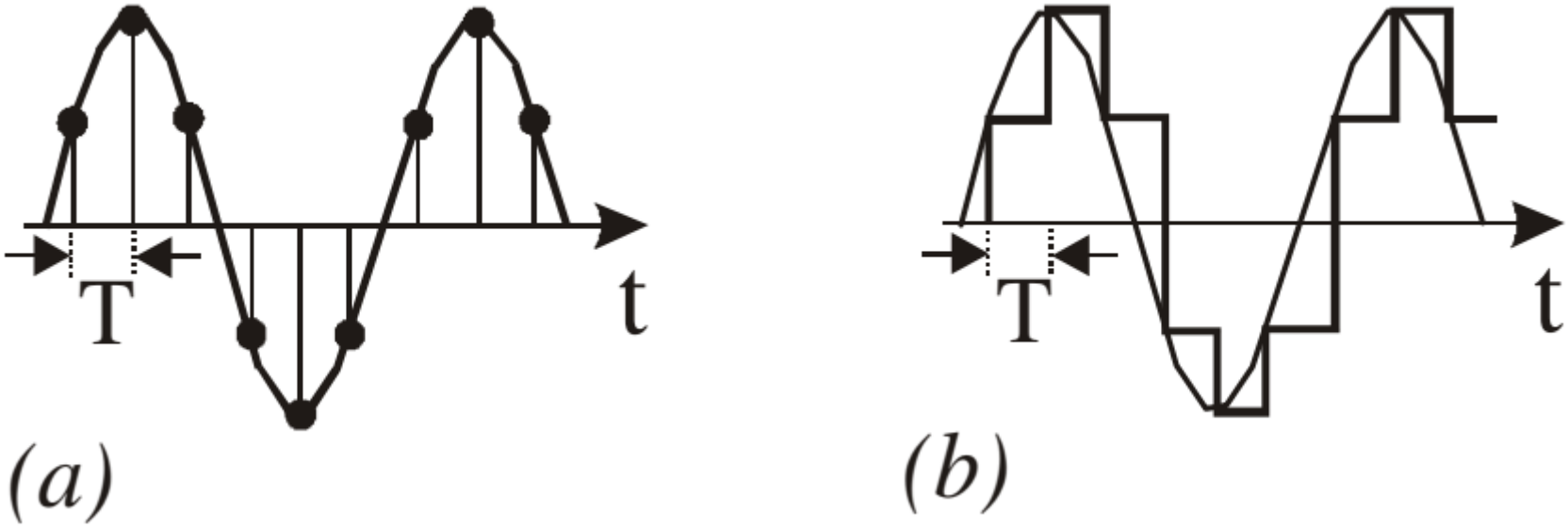
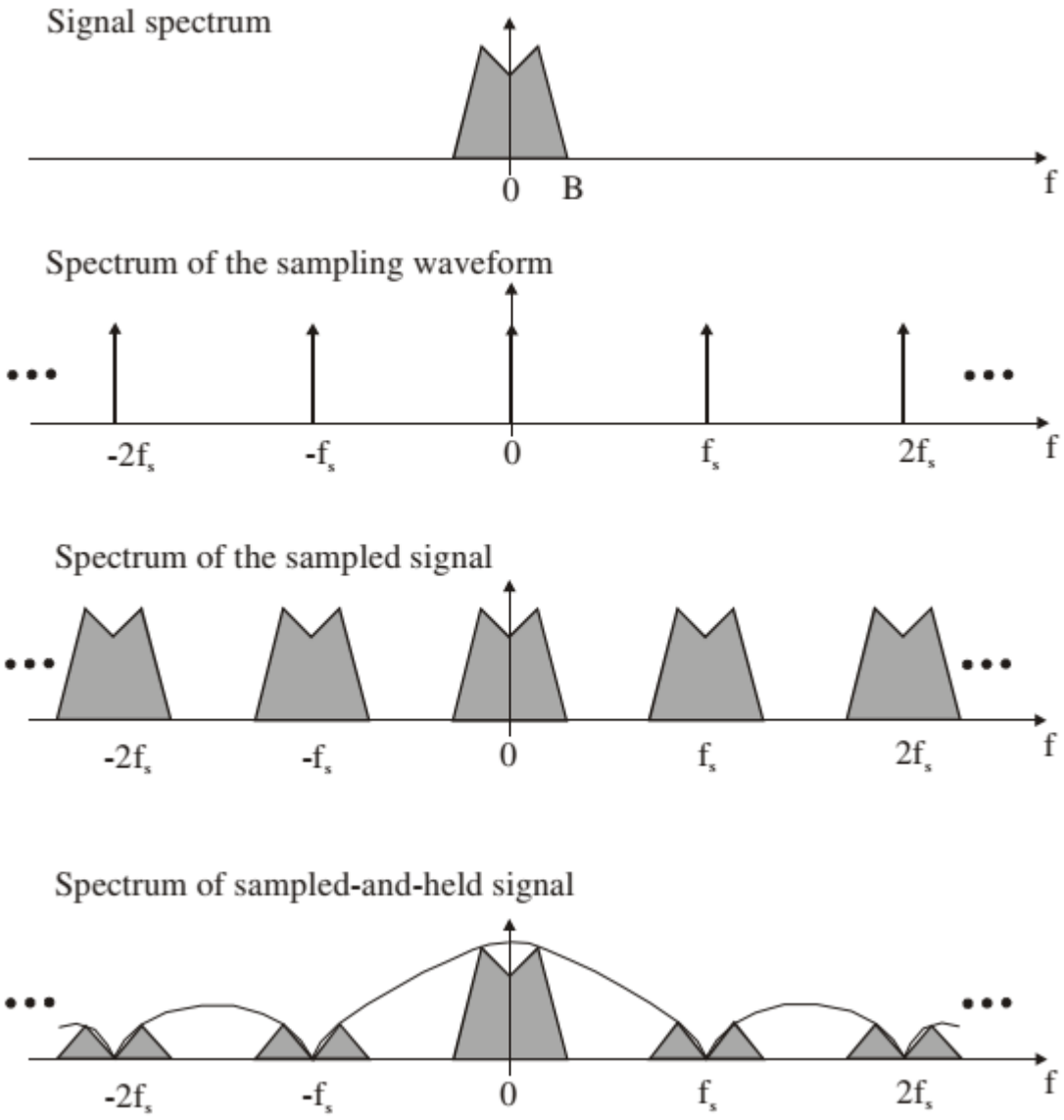


Figure (a) shows the sampling instants. Figure (b) is a sample-and-held signal

$$y(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT)$$

where $\delta(t)$ represents Dirac's delta function

Spectrum of a sampled signal



A periodic impulse train:

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) = \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{j2\pi nt/T}$$

$$S(f) = \sum_{n=-\infty}^{\infty} e^{-j2\pi nTf} = \frac{1}{T} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T}\right)$$

Quantization: an ideal A/D converter

$$V_{in} = 0 \quad then \quad B_{out} \equiv 00$$

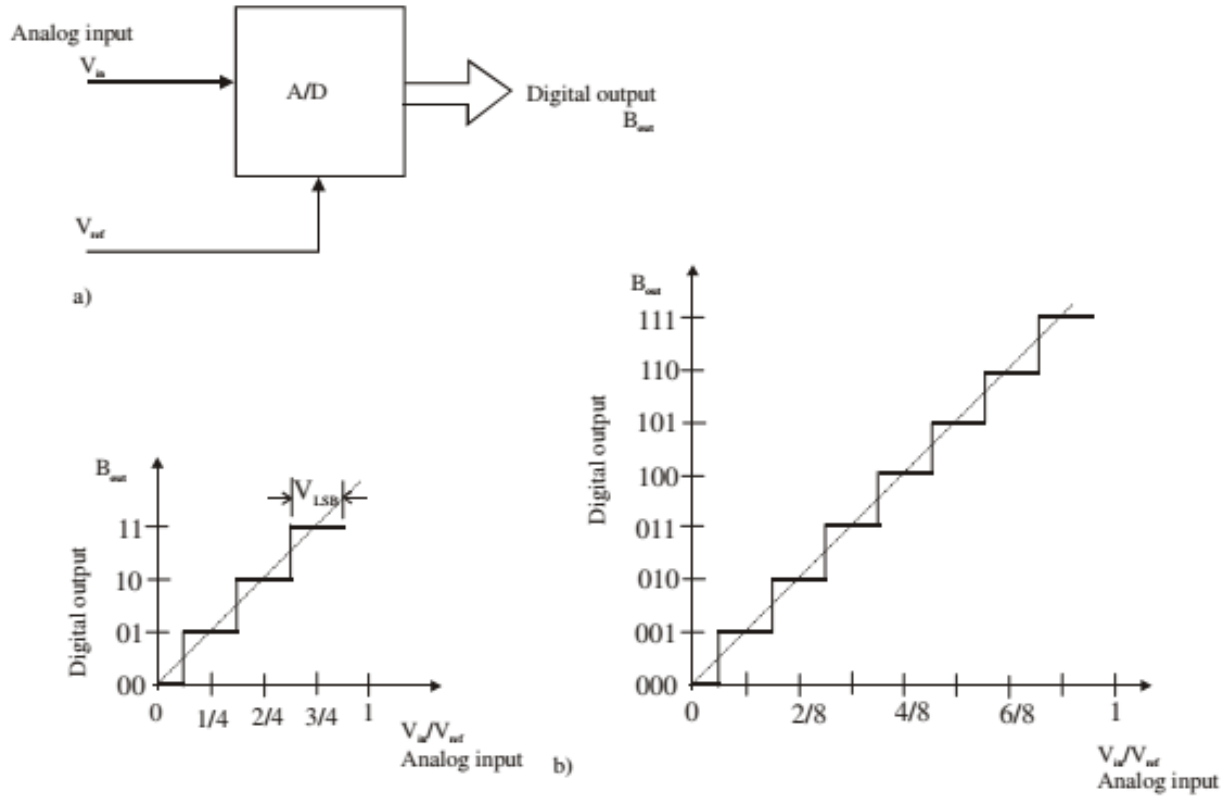
$$V_{in} = \frac{1}{4}V_{ref} \quad then \quad B_{out} \equiv 01$$

$$V_{in} = \frac{2}{4}V_{ref} \quad then \quad B_{out} \equiv 10$$

$$V_{in} = \frac{3}{4}V_{ref} \quad then \quad B_{out} \equiv 11$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

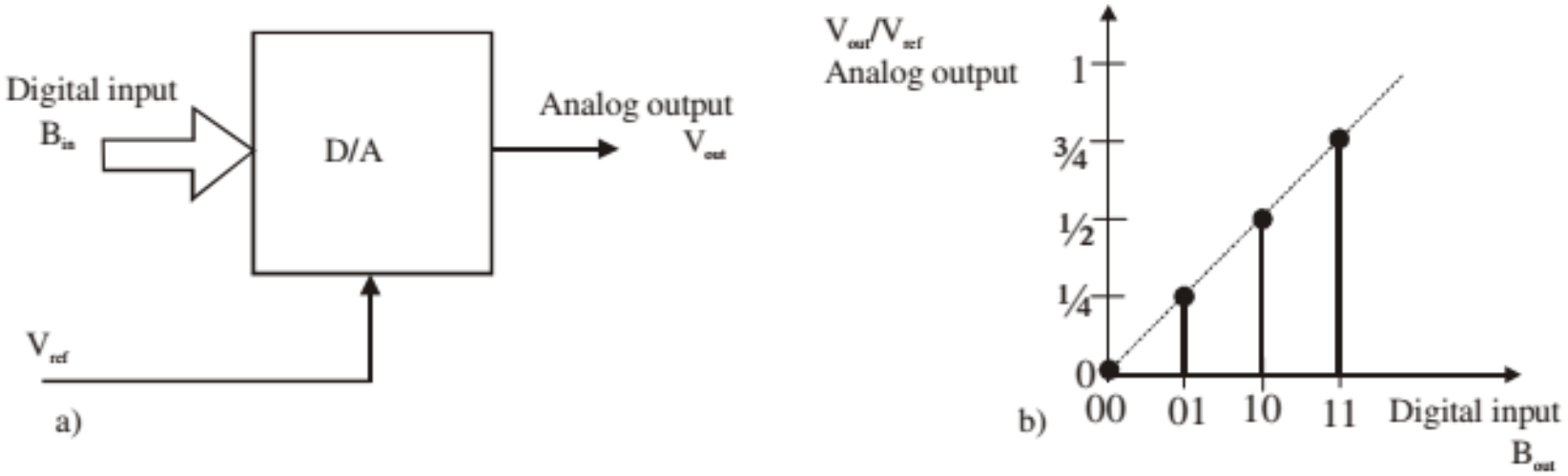
$$V_{in,\max} = \left(1 - \frac{1}{2^N}\right) V_{ref}$$



a) A block diagram representing an A/D converter, b) Input-output transfer curve for a 2-bit and 3-bit A/D converter

- V_{LSB} which is the change in input voltage required for the output to change the least significant bit (for an N-bit ADC). It becomes clear that there is a range of valid input values that produce the same digital output word

Ideal D/A converter



a) A block diagram representing a D/A converter, b) Input-output transfer curve for an ideal 2-bit DAC

$$V_{out} = B_{in} V_{ref}$$

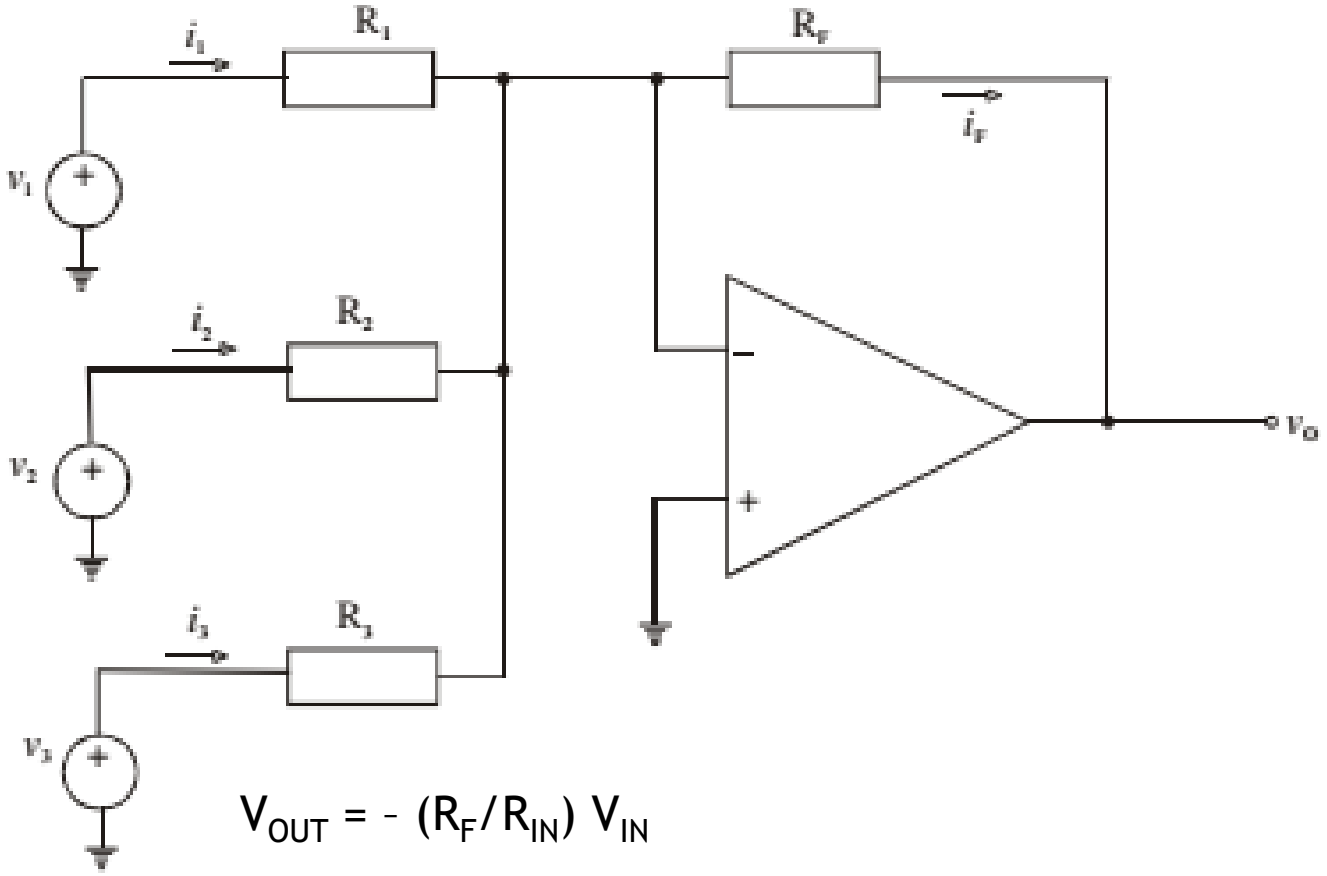
$$B_{in} = \frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_n}{2^n}$$

$$V_{out} = \left(\frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_n}{2^n} \right) V_{ref}$$

- The DAC output is the result of multiplying the analogue input signal V_{ref} by the digital variable B_{in}
- B_{in} can assume 2^n equally spaced values from 0 (when all bits are '0') to $1 - 1/2^n$ (when all bits are '1'), spacing between adjacent values is $1/2^n$

Basic Digital-to-Analog Converters

Summing amplifier



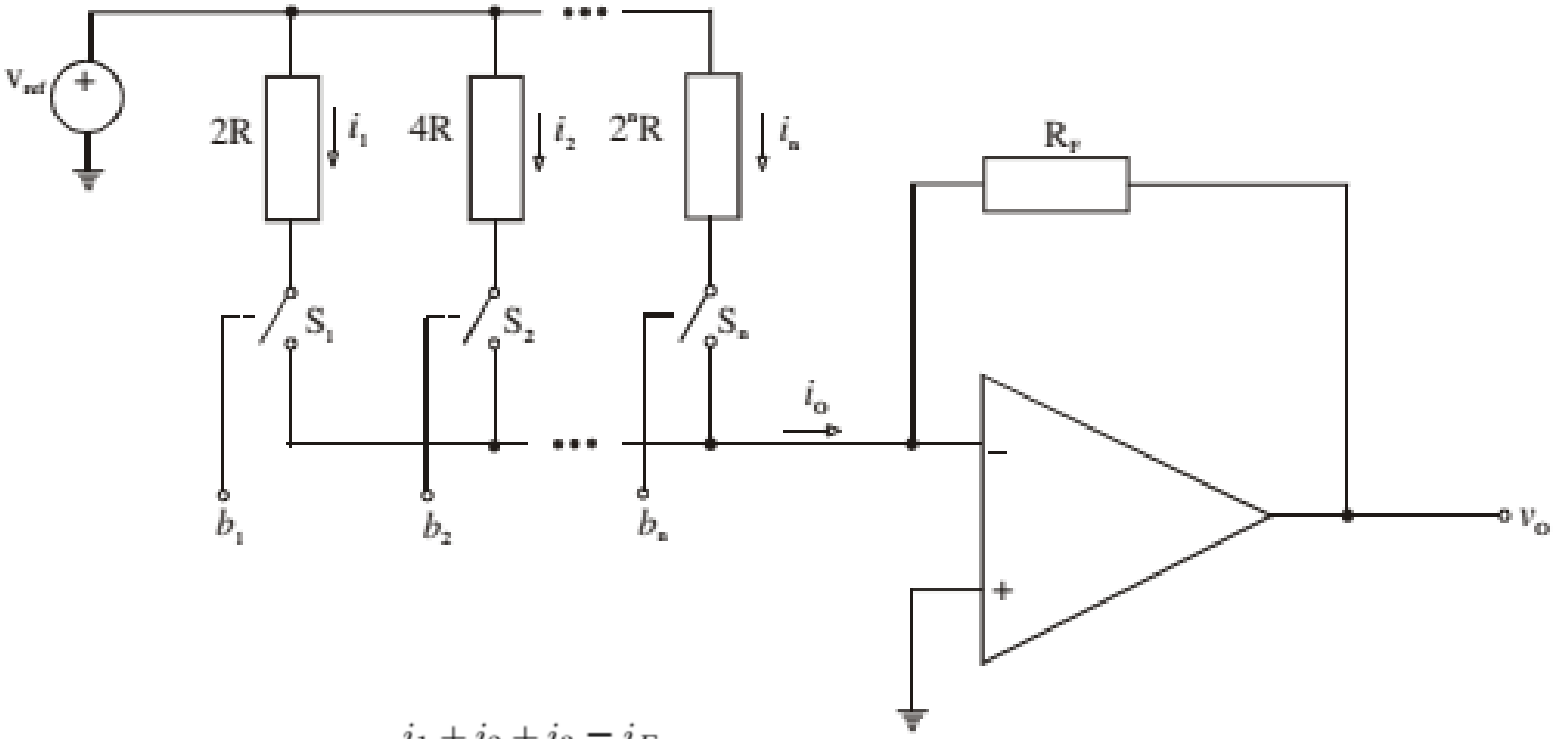
$$V_{OUT} = - (R_F/R_{IN})\ V_{IN}$$

$$V_{OUT} = - \{(R_F/R_1)\ V_1 + (R_F/R_2)\ V_2 + (R_F/R_3)\ V_3\}$$

$$V_{OUT} = - \{(R_F/R_{IN})\ \{V_1 + V_2 + V_3\}$$

$$V_{OUT} = - \{(R_f/R_{IN})\ \{V_1 + V_2 + V_3 + \ldots\ldots\ldots + V_N\}$$

Weighted-Resistor DACs



$$i_1 + i_2 + i_3 = i_F$$

Using Ohm's law, we obtain

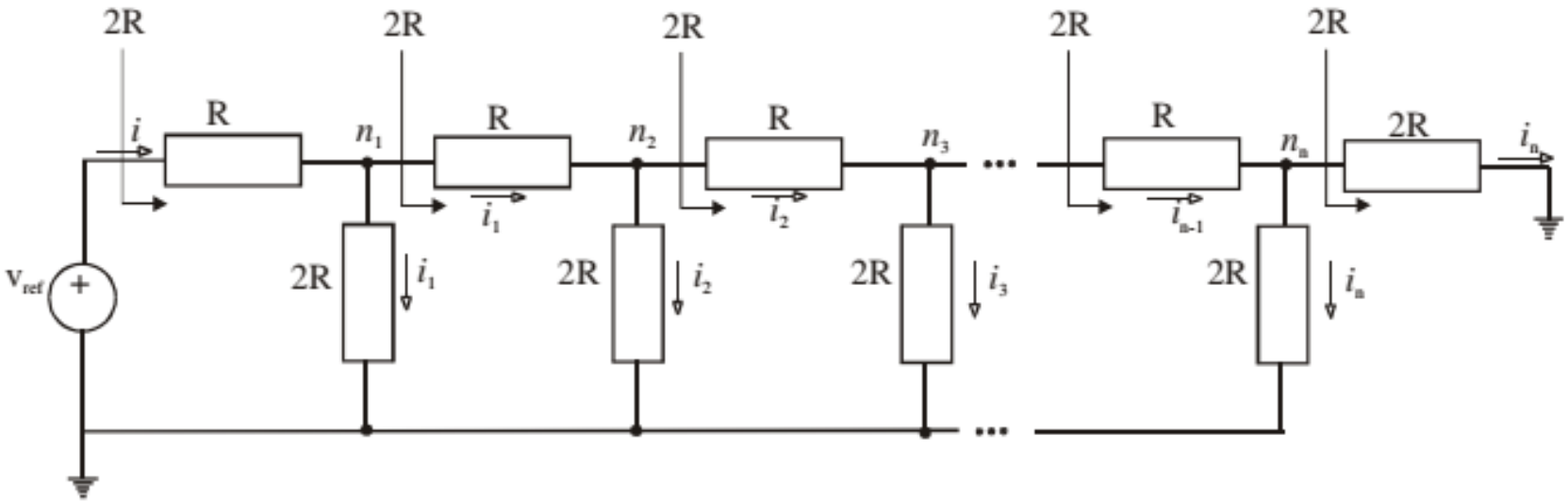
$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = -\frac{v_O}{R_F}$$

$$v_O = -\frac{V_{ref} R_F}{R}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_n}{2^n}\right)$$

and therefore

$$v_O = -R_F\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right)$$

Resistor-ladder (R-2R) network



$$i_1 = \frac{i}{2}; \quad i_2 = \frac{i_1}{2}; \quad i_3 = \frac{i_2}{2}; \quad \cdots \quad i_n = \frac{i_{n-1}}{2}$$

$$i_1 = \frac{V_{ref}}{2R} = \frac{V_{ref}/R}{2};$$

or

$$i_1 = \frac{i}{2}; \quad i_2 = \frac{i}{2^2}; \quad i_3 = \frac{i}{2^3}; \quad \cdots \quad i_n = \frac{i}{2^n}$$

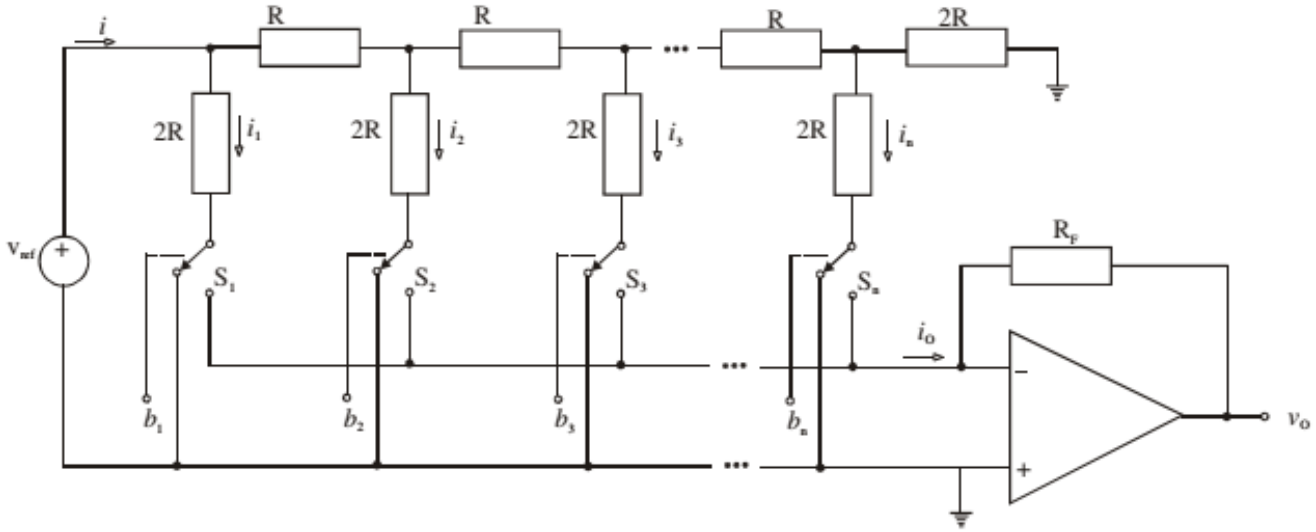
$$i_2 = \frac{i_1}{2} = \frac{V_{ref}/R}{2^2}; \cdots$$

$$i_n = \frac{i_{n-1}}{2} = \frac{V_{ref}/R}{2^n}$$

where

$$i = \frac{V_{ref}}{2R}$$

R-2R Ladder DACs



$$i_1 = \frac{V_{ref}}{2R} = \frac{V_{ref}/R}{2};$$

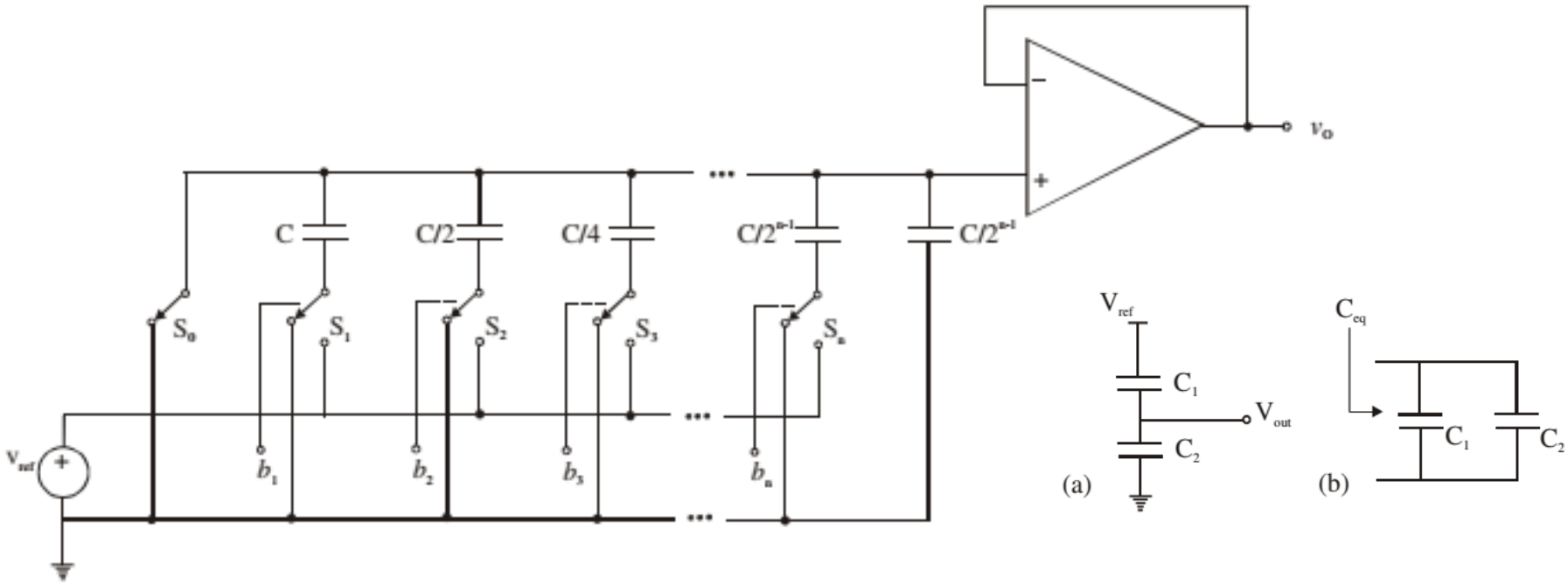
$$i_2 = \frac{i_1}{2} = \frac{V_{ref}/R}{2^2}; \cdots$$

$$i_n = \frac{i_{n-1}}{2} = \frac{V_{ref}/R}{2^n}$$

$$v_O = -R_F i_O$$

$$v_O = -V_{ref}\frac{R_F}{R}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_n}{2^n}\right)$$

Weighted-Capacitor DACs



$$V_{out} = V_{ref}\frac{C_1}{C_1 + C_2}$$

$$C_r = b_1 C + b_2\frac{C}{2} + \cdots + b_n\frac{C}{2^{n-1}}$$

and

$$C_{eq} = C_1 + C_2$$

$$C_t = C + \frac{C}{2} + \cdots + \frac{C}{2^{n-1}} + \frac{C}{2^{n-1}} = 2C$$

Thus the output voltage of the DAC in Fig 43 is given by

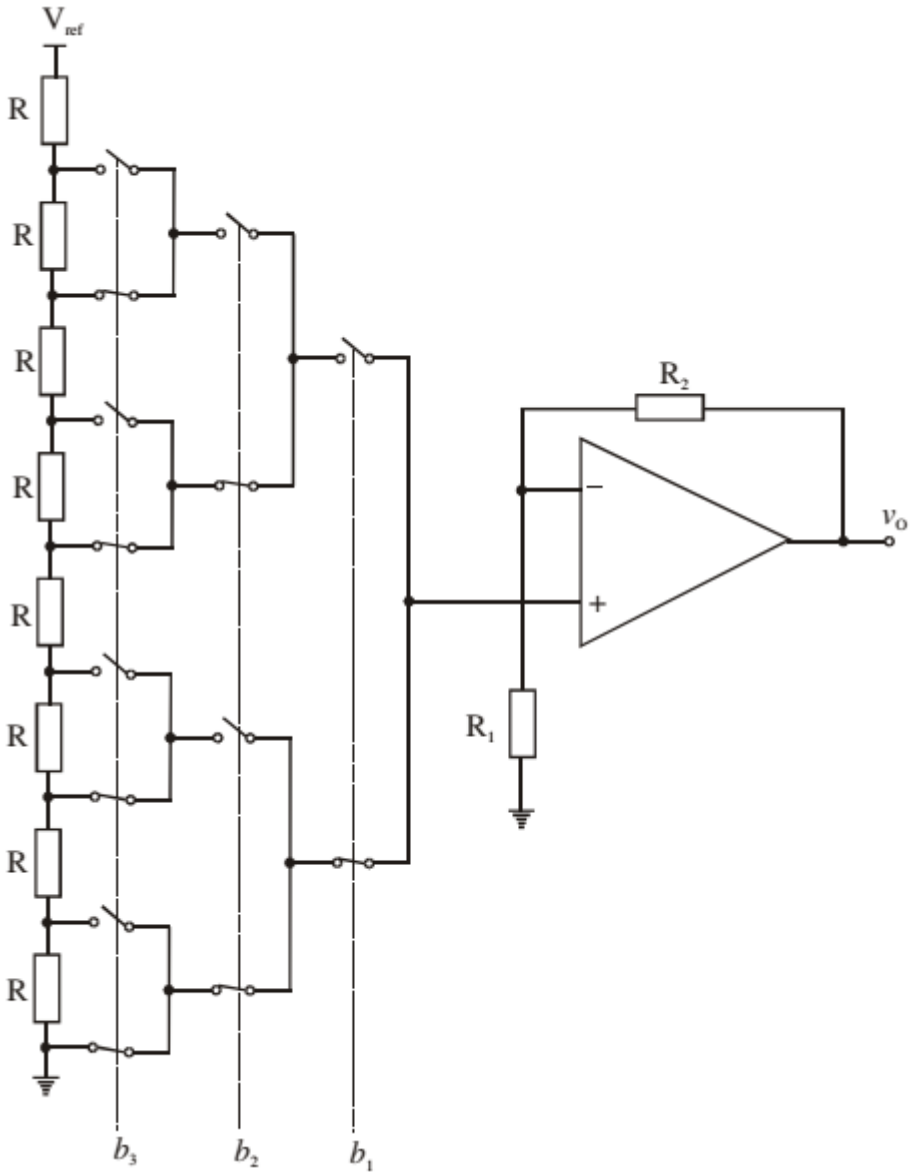
$$v_O = V_{ref}\frac{C_r}{C_t}$$

$$v_O = V_{ref}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_n}{2^n}\right)$$

Potentiometric DACs

- An n-bit DAC uses 2^n resistors
- No matter how mismatched the resistors, v0 will always increase as the amplifier is switched from one tap to the next, up the ladder, hence the inherent monotonicity.
- Another advantage of the potentiometric DAC is that if the top and bottom nodes of the resistive string are biased at some arbitrary voltages V_H and V_L, the DAC will interpolate between V_L and V_H with a resolution of 2^n steps.
- However, the large number of resistors (2^n) and switches ($2^{n+1} - 2$) required limits practical potentiometric DACs to n ≤ 8, even though the switches can be fabricated very efficiently in MOS technology

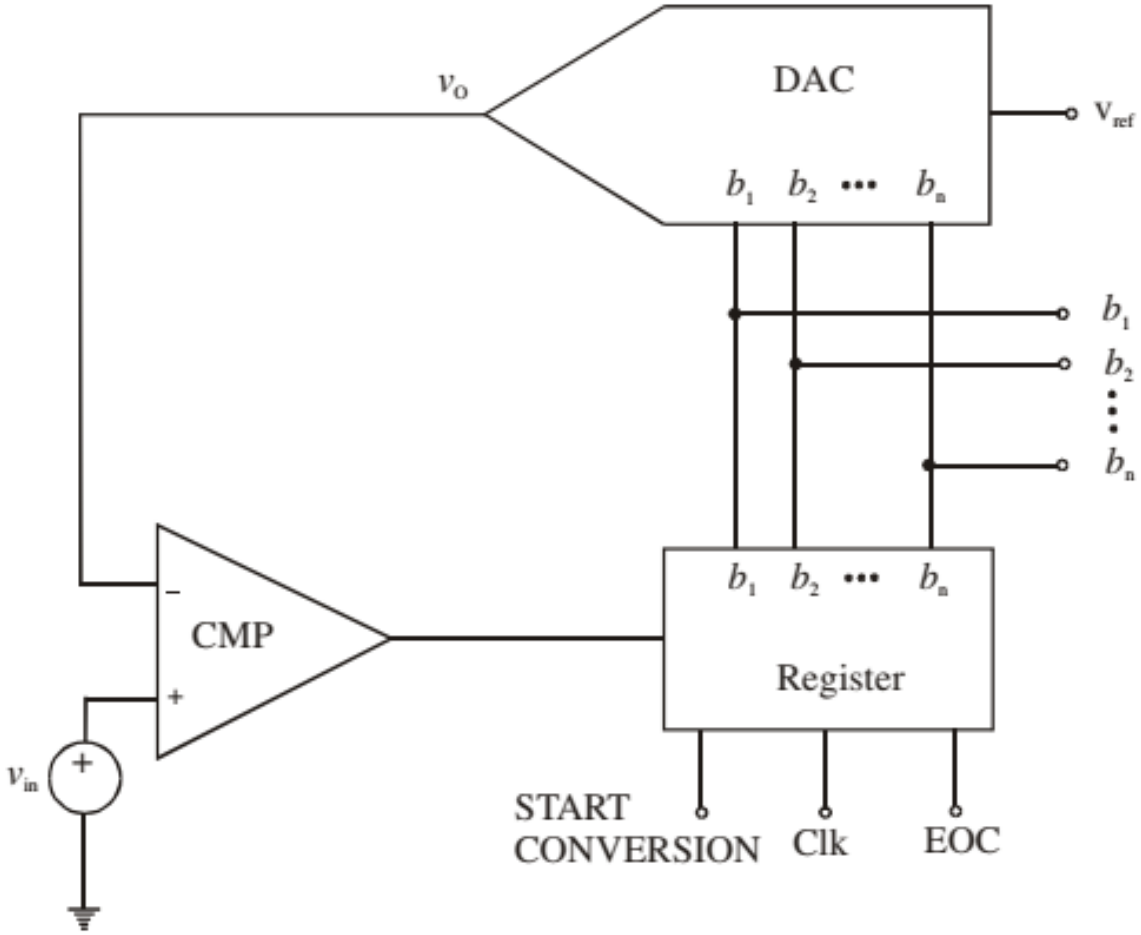
$$B_{in} = \frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3}$$



Segmentation

- High-resolution DACs achieve monotonicity by a technique know as segmentation. Here the reference range is partitioned into a sufficiently large number of contigous segments, and a DAC of lesser resolution is then used to interpolate between the extremes of the selected segment (the interested student can refer to the course texts for more information).

DAC-Based A-D Conversion



Successive-Approximation Converters

This technique uses the register as a *successive-approximation register* (SAR) to find each bit by trial and error. Starting from the MSB, the SAR inserts a trial 1 and the interrogates the comparator to find whether this causes v_O to rise above v_{in}. If it does, the trial bit is changed back to 0; otherwise it is left at 1. The procedure is repeated for all subsequent bits, one bit at a time.

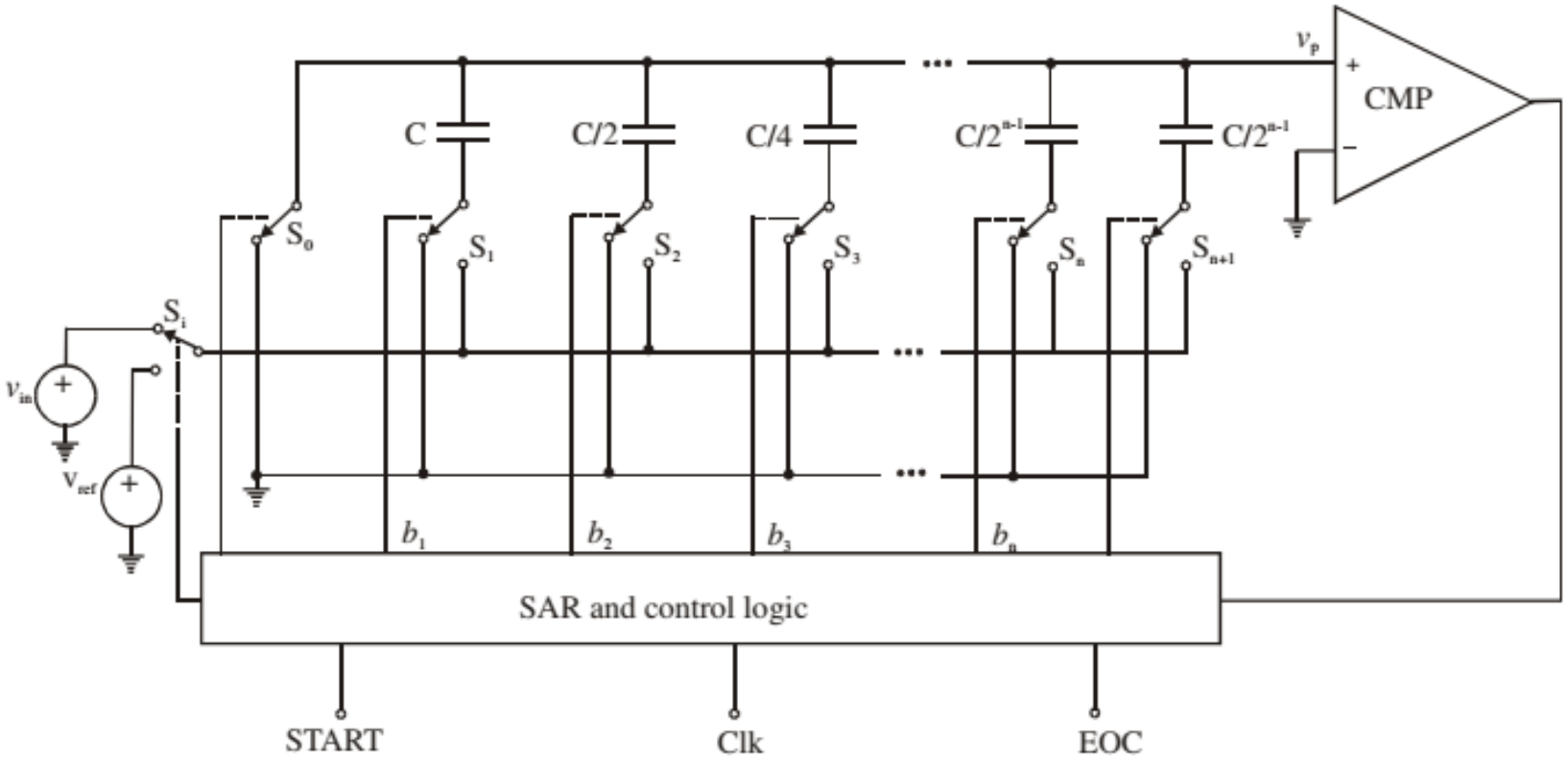
To illustrate this consider the conversion of a 10.8V input to a 4-bit code with a $V_{ref} = 16V$. To ensure correct results, the DAC output must be offset by $+\frac{1}{2}V_{LSB}$ or 0.5V. Following the arrival of the START command, the SAR sets b_1 to 1 with all remaining bits at 0 so that the trial code is 1000. This causes the DAC output $v_O = 16\left(\frac{1}{2}\right) + 0.5 = 8.5V$. At the end of clock period T_1, v_O is compared against v_{in} and since $8.5 < 10.8$, b_1 is left at 1.

At the beginning of T_2, b_2 is set to 1, so the trial code is now 1100 and $v_O = 16\left(\frac{1}{2} + \frac{1}{2^2}\right) + 0.5 = 12.5V$. Since $12.5 > 10.8$, b_2 is changed back to zero at the end of T2.

At the beginning of T_3, b_3 is set to 1, so the trial code is now 1010 and $v_O = 10.5V$. Since $10.5 < 10.8$, b_3 is left at 1.

At the beginning of T_4, b_4 is set to 1, so the trial code is now 1011 and $v_O = 11.5V$. Since $11.5 > 10.8$, b_4 is changed back to zero. Thus when leaving T4, the SAR has generated the code 1010, which corresponds to 10.5V. Since the entire conversion takes a total of n clock cycles, a SA ADC offers a major speed improvement over a sequential search ADC.

Charge-Redistribution ADCs



$$v_p = -v_{in} + V_{ref}\left(\frac{C}{C + \frac{C}{2} + \frac{C}{4} + \cdots + \frac{C}{2^{n-1}} + \frac{C}{2^{n-1}}}\right)$$

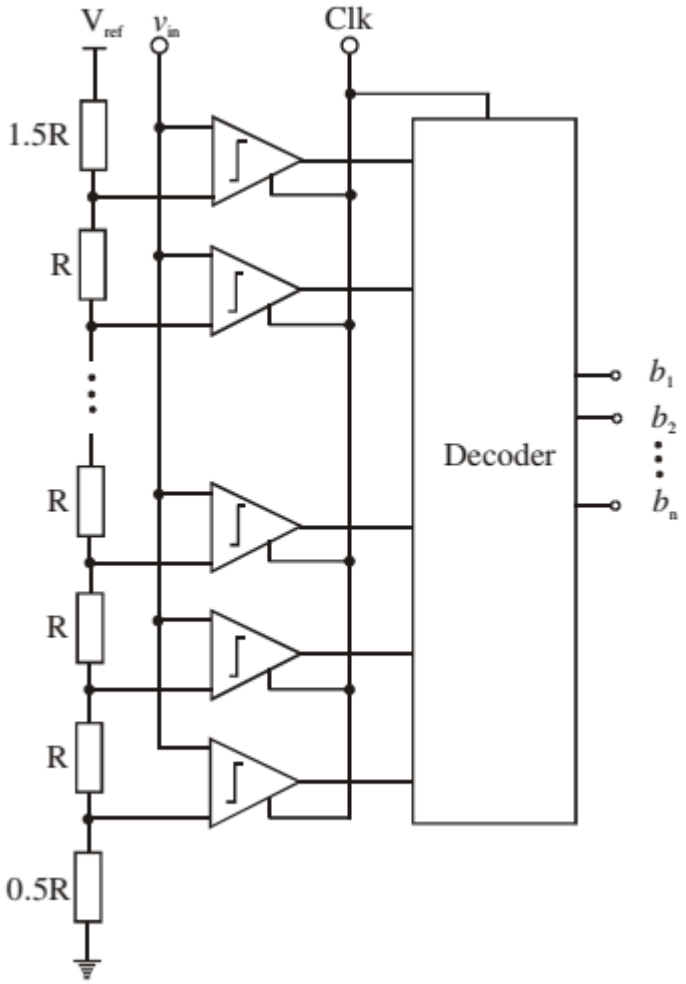
$$= -v_{in} + \frac{V_{ref}}{2}$$

$$v_p = -v_{in} + \frac{V_{ref}}{2^2}$$

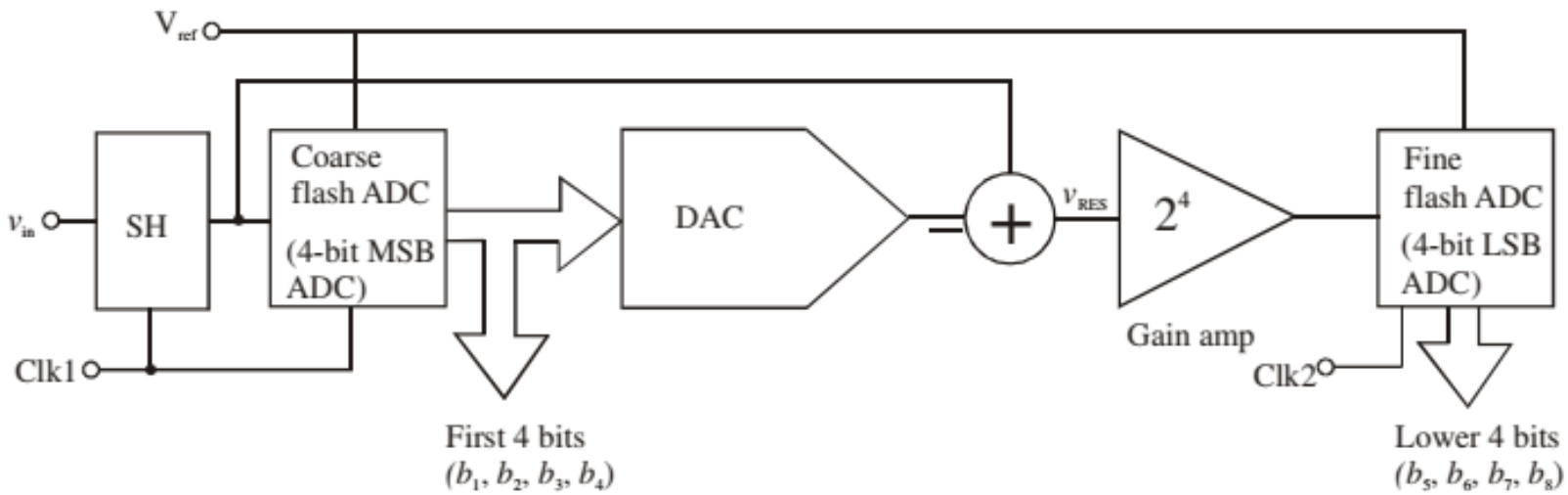
$$v_p = -v_{in} + \frac{V_{ref}}{2^k}$$

$$v_p = -v_{in} + V_{ref}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \cdots + \frac{b_n}{2^n}\right)$$

Flash Converters

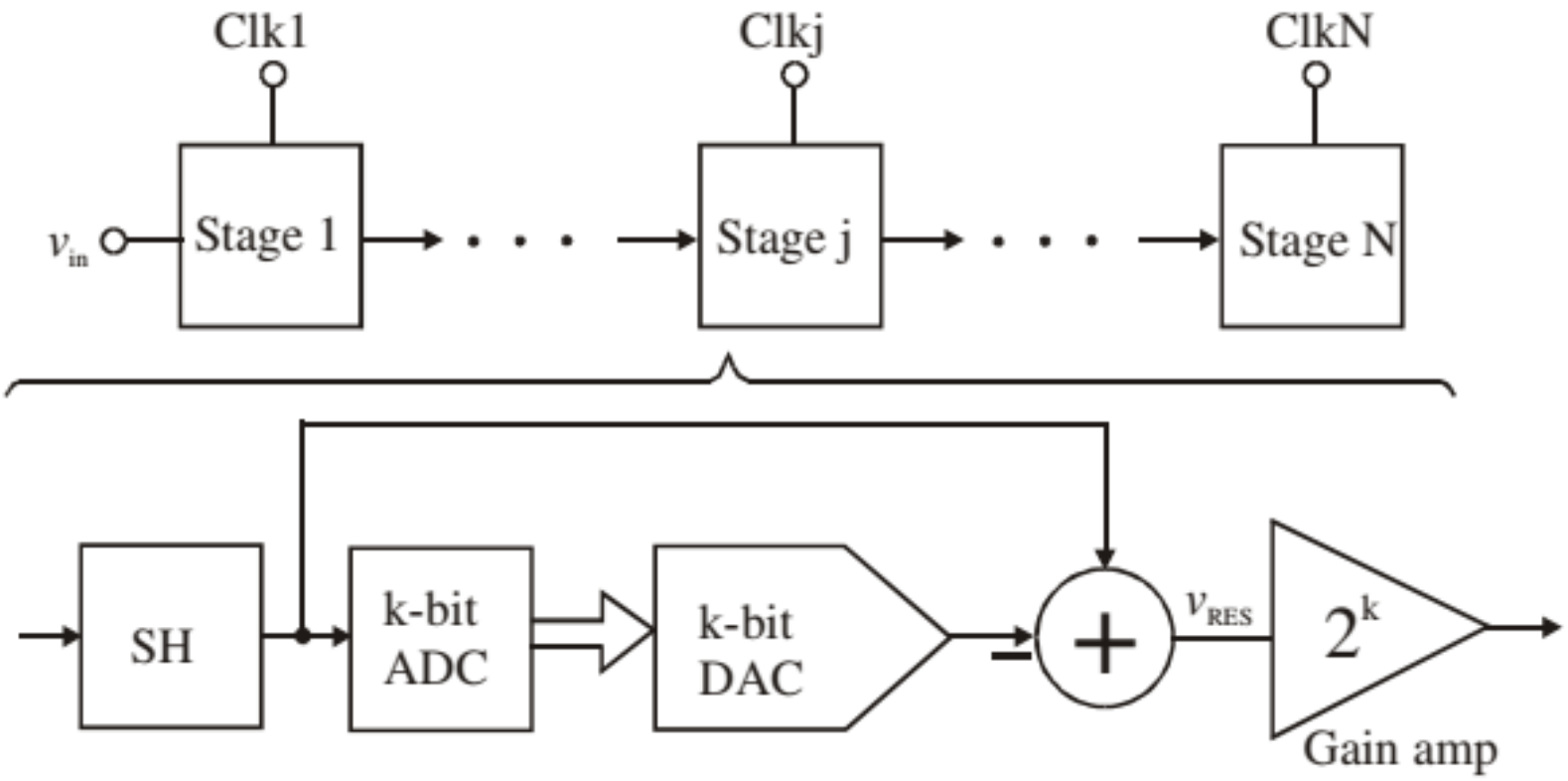


Two-step (Subranging) Converters



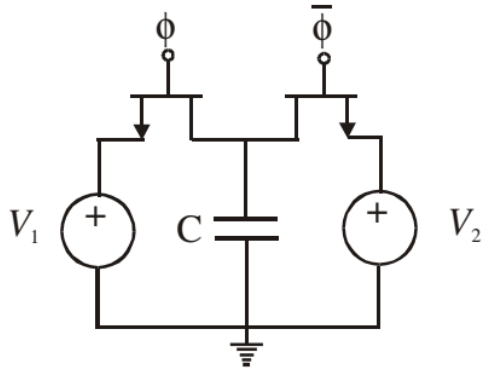
8-bit subranging ADC

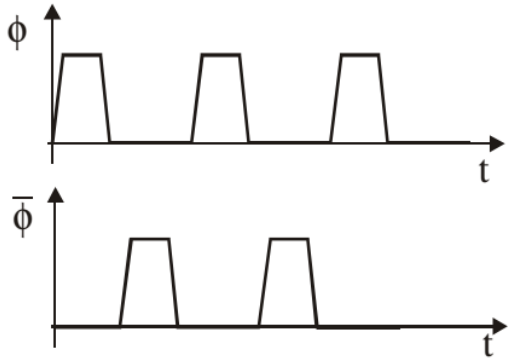
Pipelined Converters

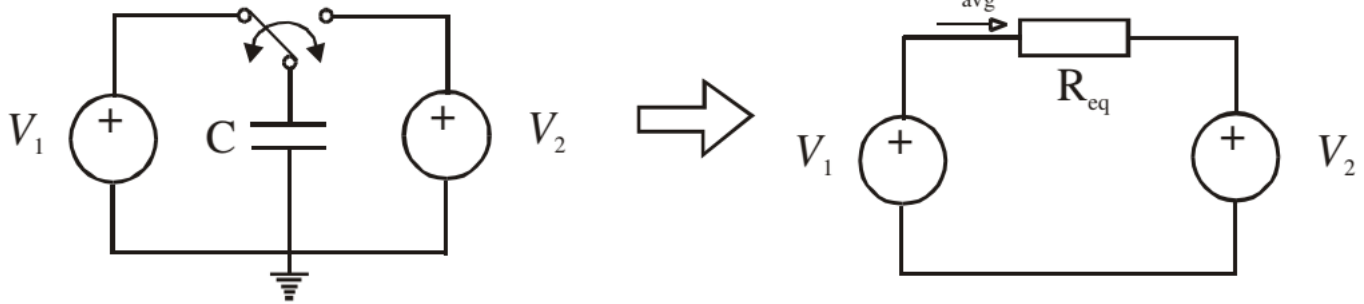


Pipeline ADC architecture

Switched-Capacitor Circuits





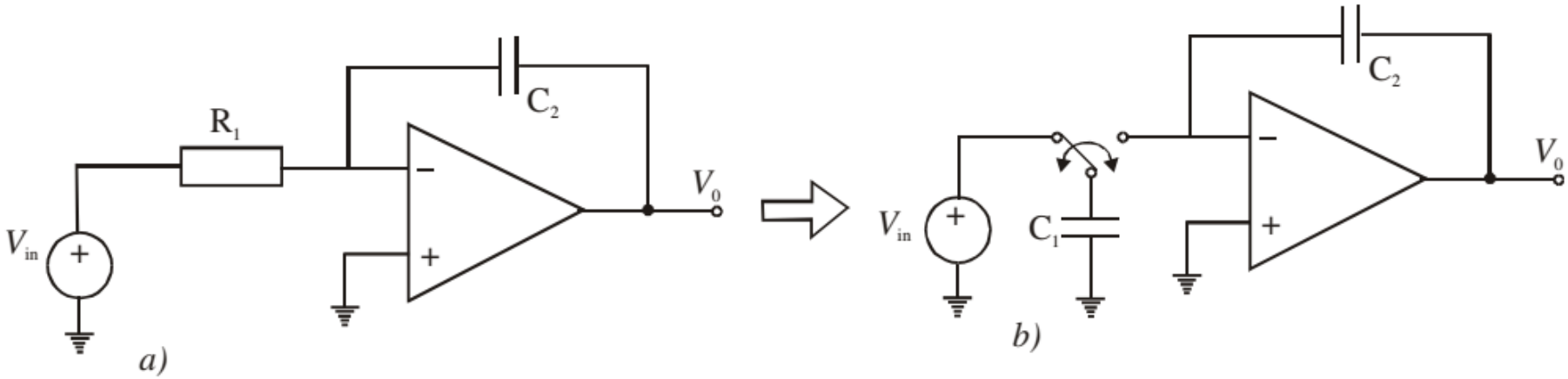


$$\Delta Q = C\,(V_1 - V_2)$$

$$\begin{aligned} I_{avg} &= f_{CK}\Delta Q \\ &= C f_{CK}\,(V_1 - V_2) \end{aligned}$$

$$R_{eq} = \frac{V_1 - V_2}{I_{avg}} = \frac{1}{C f_{CK}}$$

SC integrators



$$\frac{V_{in}}{R_1} = -\frac{V_0}{1/j\omega C_2}$$

$$H(j\omega) = \frac{V_0}{V_{in}} = -\frac{1}{j\omega/\omega_0}$$

$$\omega_0 = \frac{1}{R_1 C_2}$$

$$R_1 = \frac{1}{C_1 f_{CK}}$$

$$\omega_0 = \frac{C_1}{C_2} f_{CK}$$

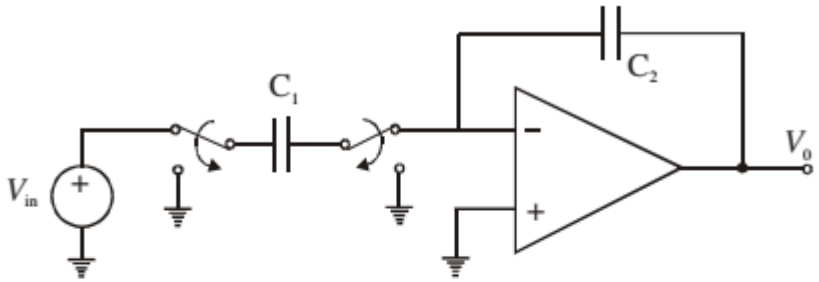
Advantages of SC filters

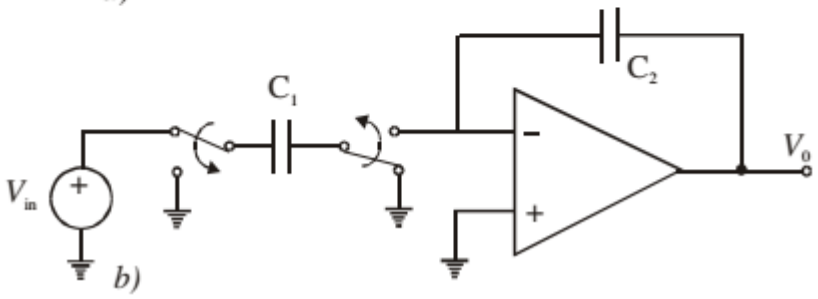
1. There are no resistors. This is highly desirable from the viewpoint of IC fabrication, since monolithic resistors are plagued by large tolerances and thermal drift, and also take up precious chip area. Swiches, on the other hand, are implemented with MOSFETs, which are the basic ingredients of VLSI technology and occupy very little chip area.

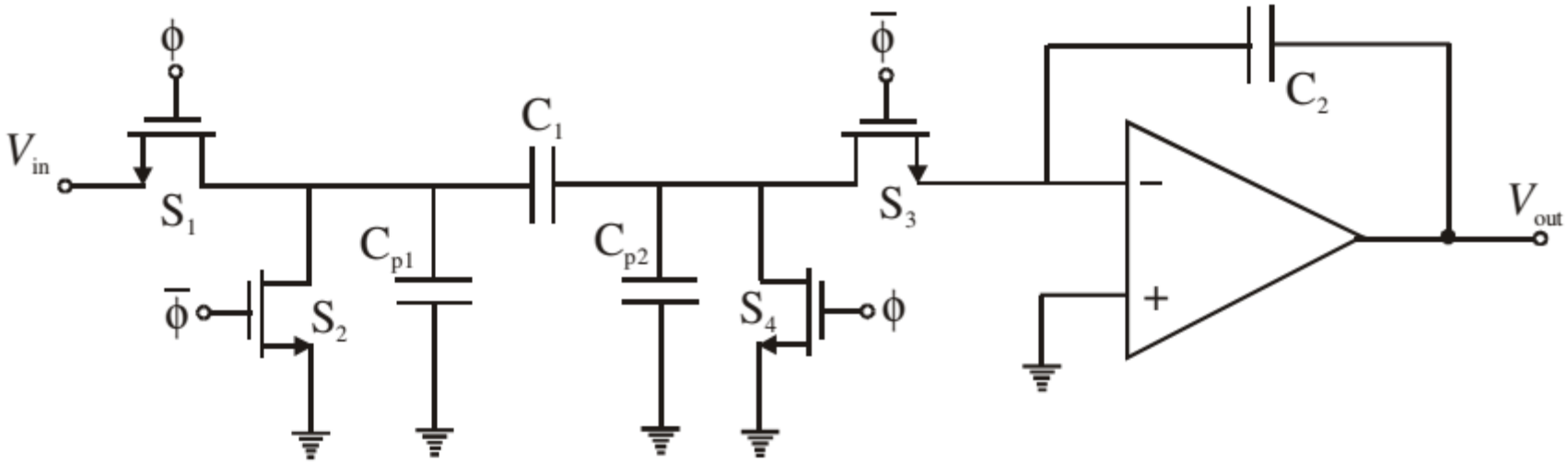
2. The characteristic frequency ω_0 depends on capacitance ratios, which are much easier to control and maintain with temperature and time than RC products.

3. ω_0 is proportional to f_{CK} indicating that SC filters are inherently of programmable type.

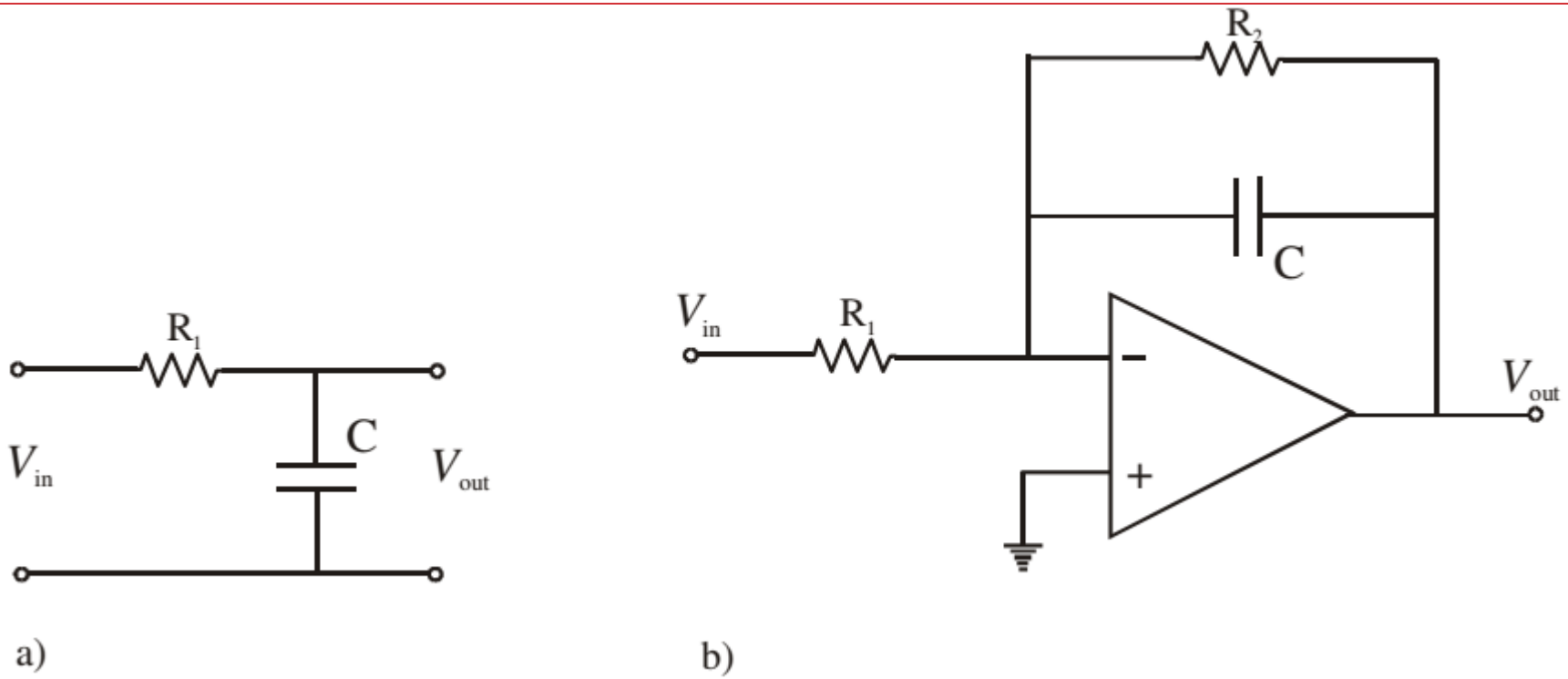
SC integrators







Low pass first-order filter



Low pass first-order filter a) passive realization, b) Op amp realization.

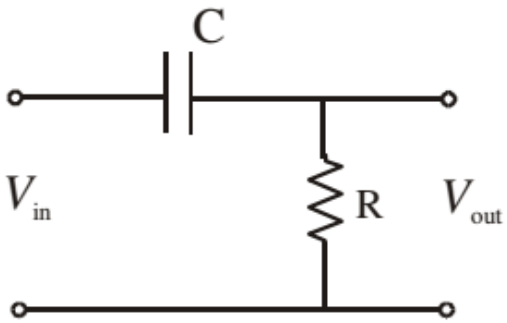
$$DC\ gain = 1$$

$$RC = \frac{1}{\omega_0}$$

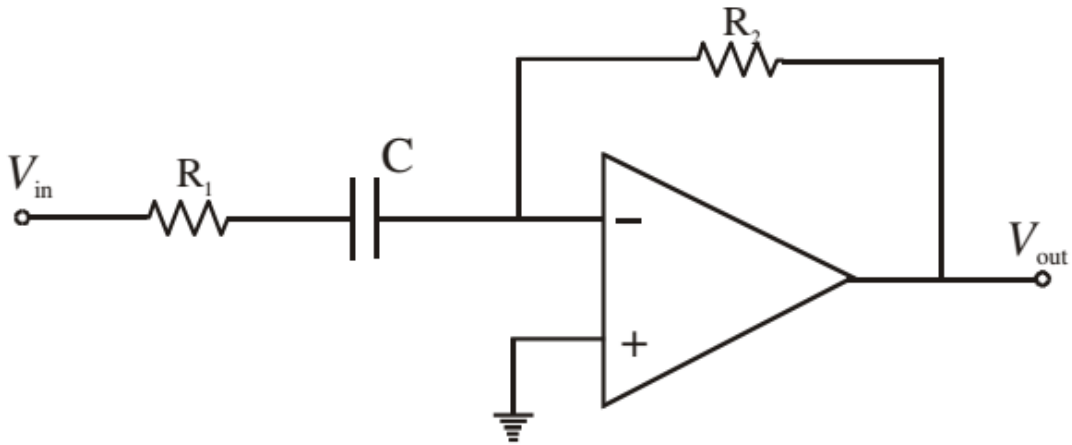
$$DC\ gain = -\frac{R_2}{R_1}$$

$$R_2C = \frac{1}{\omega_0}$$

High pass first-order filter



a)



b)

High pass first-order filter a) passive realization, b) Op amp realization.

$$High\,Frequency\,gain = 1$$

$$RC = \frac{1}{\omega_0}$$

$$High\,Frequency\,gain = -\frac{R_2}{R_1}$$

$$R_1 C = \frac{1}{\omega_0}$$