Layout of Analog CMOS Integrated Circuit

Outline

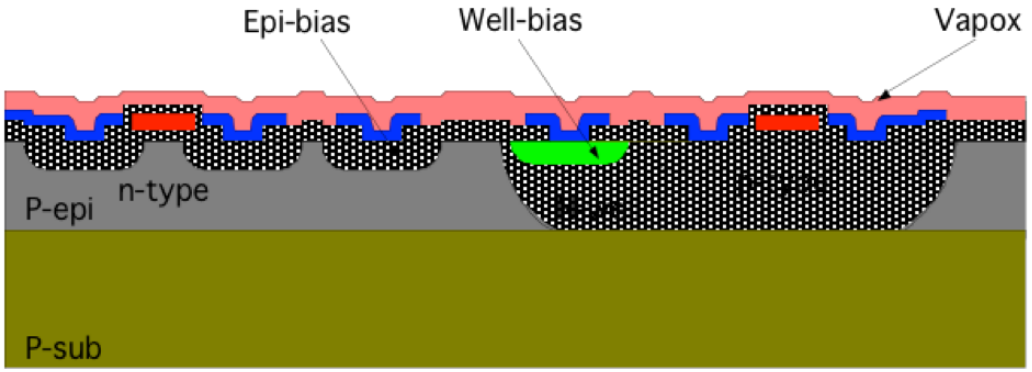
- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout

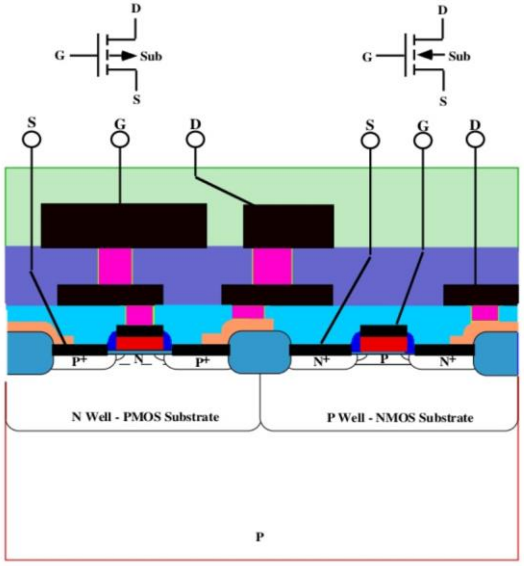
Part I: Process and Overview Topics

- CMOS process Overview
  - Generic CMOS cross-section
  - How layers form parasitic effects
  - Process gradients: die and wafer
- General Constrains
  - Design rules
  - Failure mechanisms
- High frequency/radio frequency considerations
  - EM fields near traces
  - Grounding, Shielding

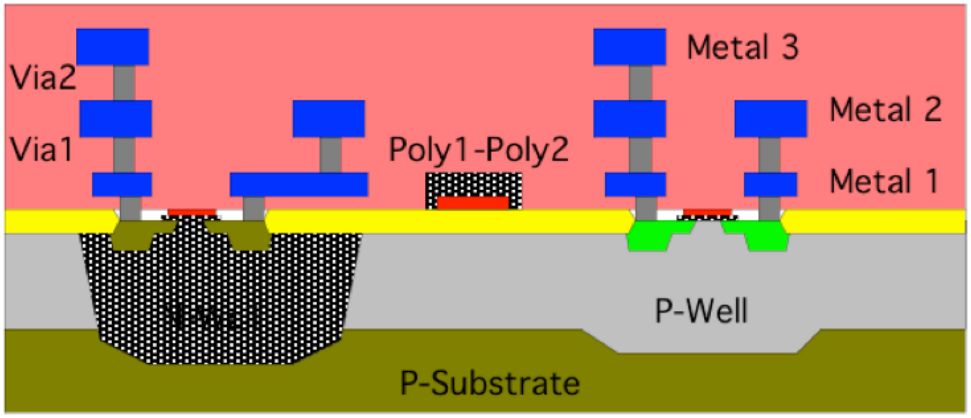
CMOS process Overview

Single metal, single poly cross-section

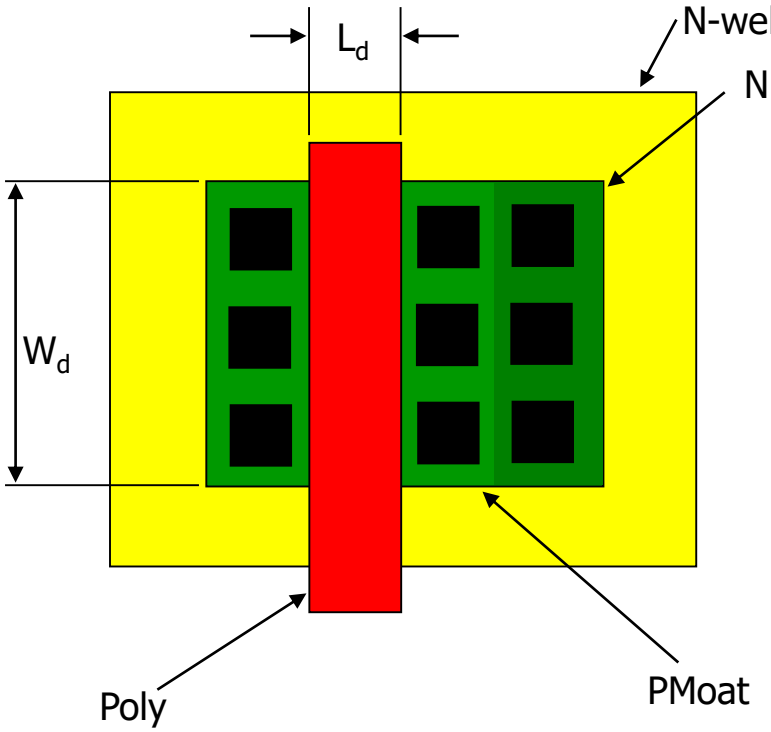


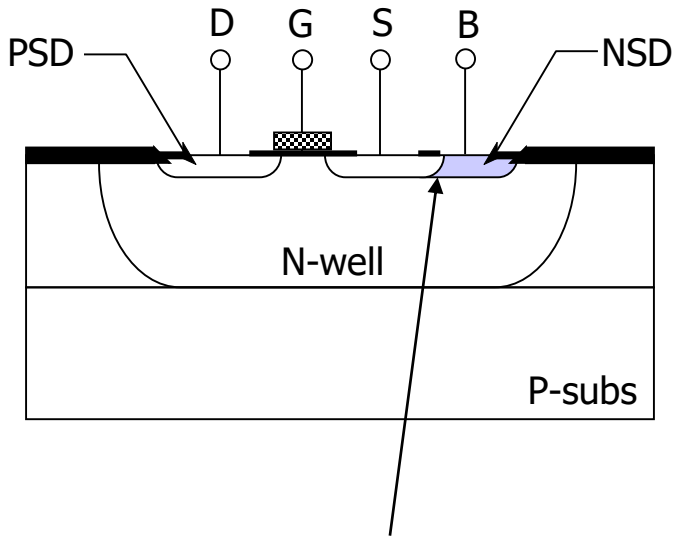


Triple metal, double poly cross-section



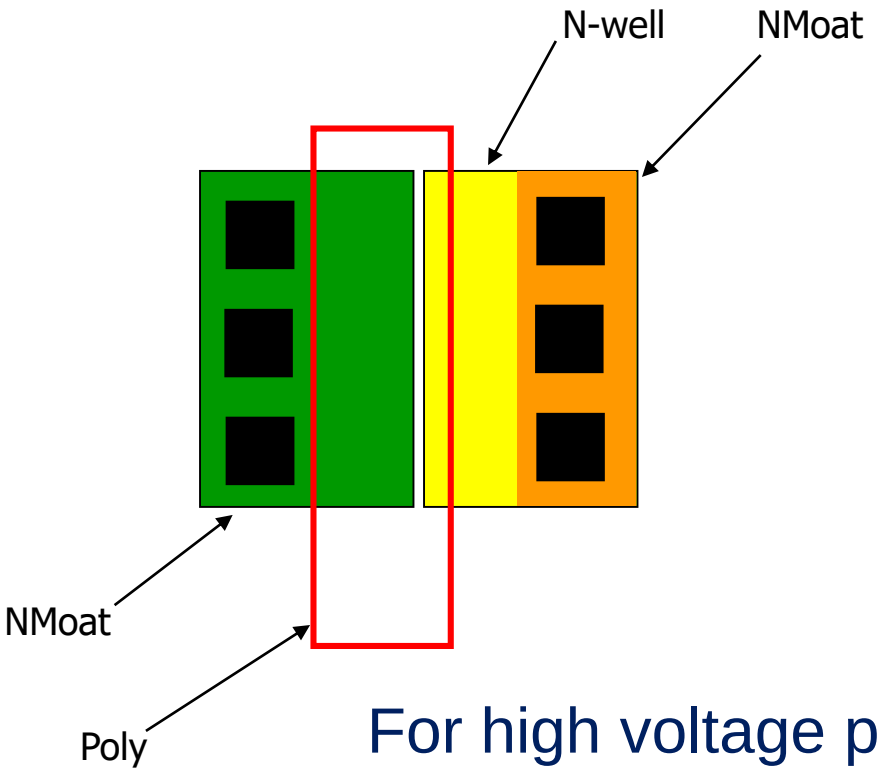
CMOS Transistor

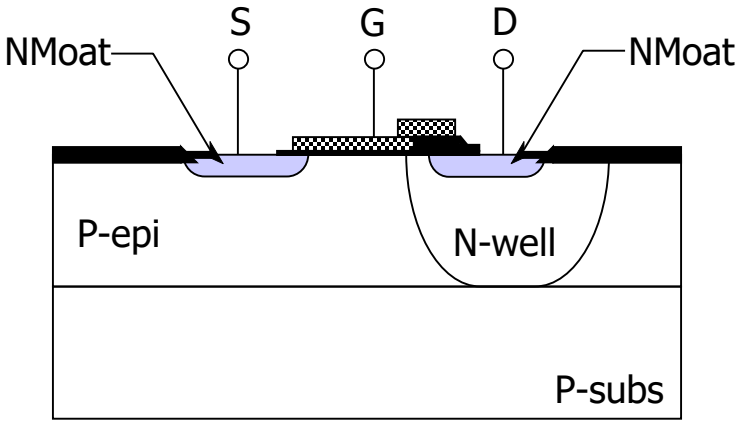




Improves the latch-up immunity

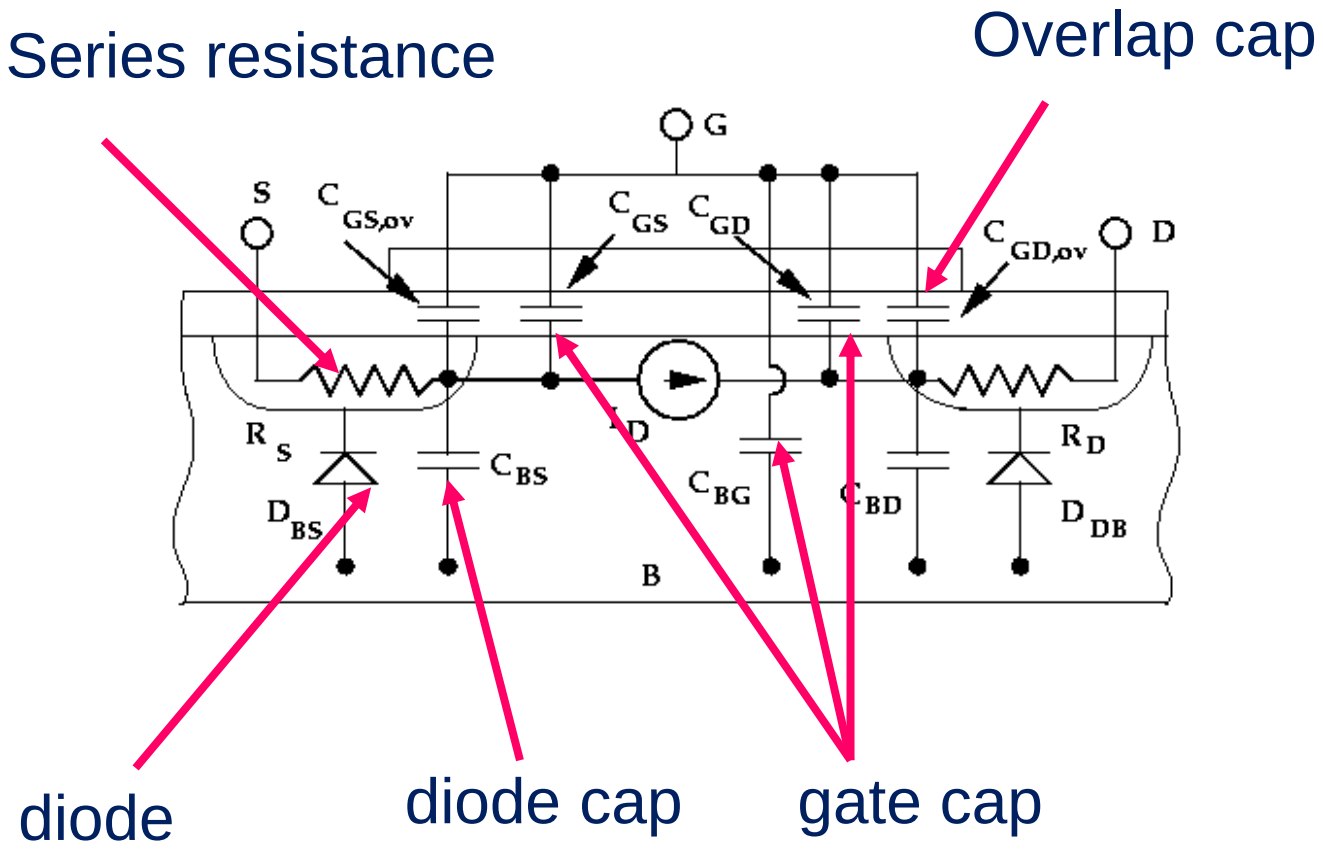
Extended-drain Transistor





For high voltage performances
(not symmetrical)

Parasitic Elements in MOS



Parasitic Resistance and Diode

Parasitic resistance: depends on the source or drain diffusion specific resistance

$$R_D \approx R_S \approx 10 - 50\ \Omega$$

Diodes reversely biased; the reverse current is dominated by generation recombination term

$$I_{GR} = A\frac{qn_i x_j}{2\tau_0}$$

A : area of the junction

x_j : depletion region width

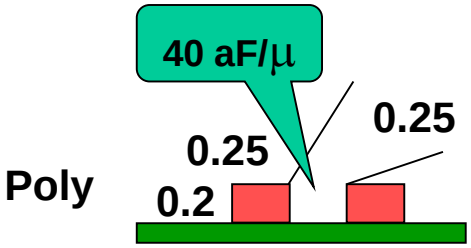
τ_o : mean lfetime for minority carriers

I_{GR} doubles for an increase of 10 K typically at room temperature

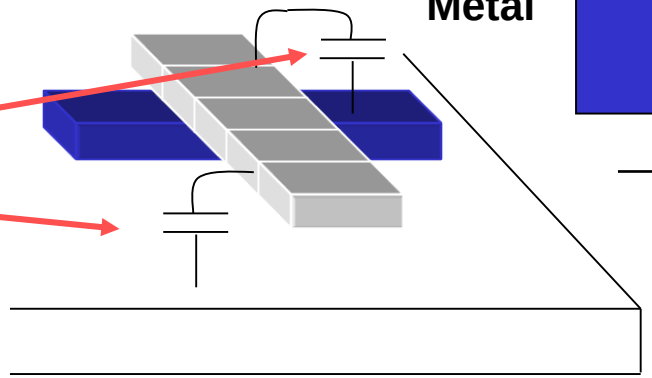
$I_{GR}/A = 10^{-15}$ A/μm^2.

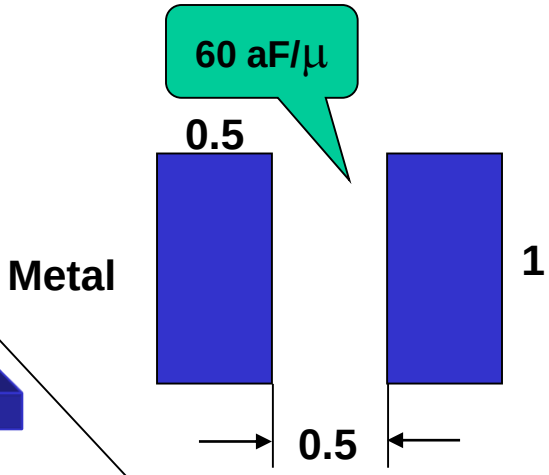
How Layers form Parasitic

- Coupling capacitance same layers
  - lateral capacitance
  - depends distance
  - depends on layer thickness

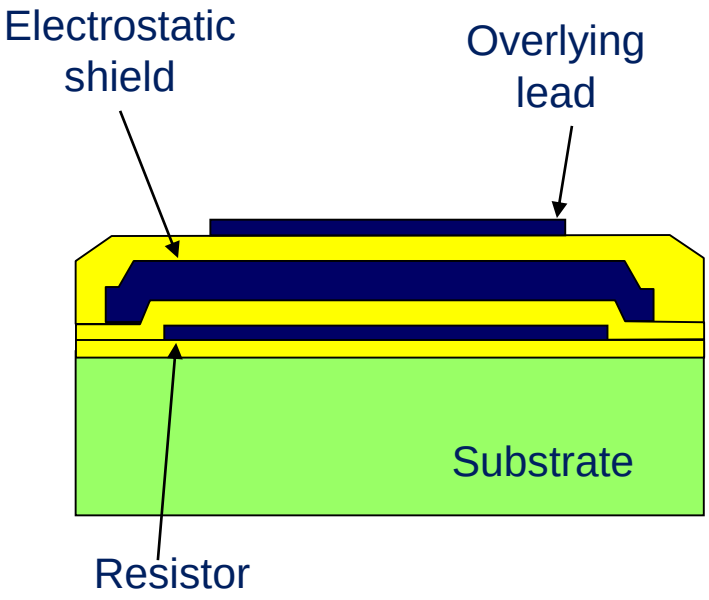


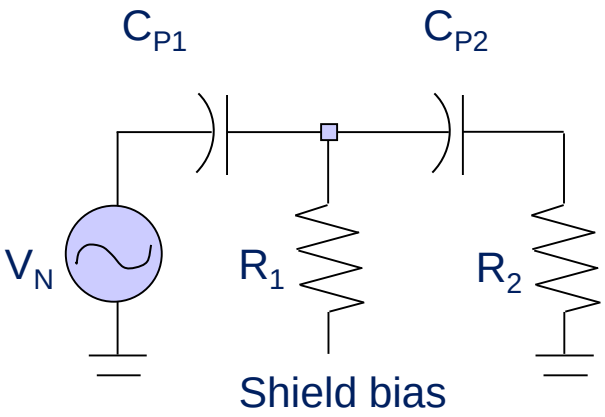
- Coupling between layers
  - metals, poly, substrate
  - layer-layer 5-10 aF/μ^2
  - fringing cap 10-15 aF/μ^2





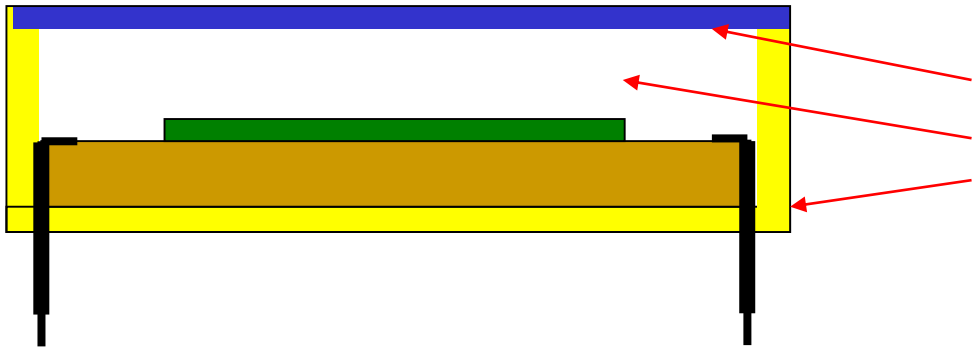
Electrostatic Shield



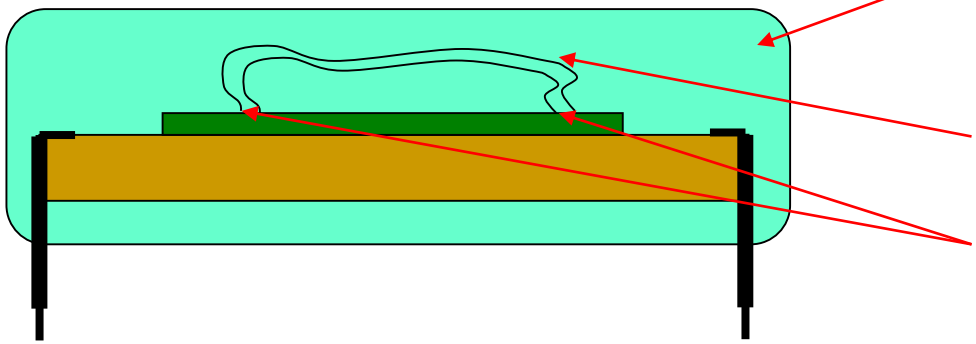


Be sure that the shield bias is not a noise source!

Cross-talk from Package



Metal led
Filling
Ceramic Package



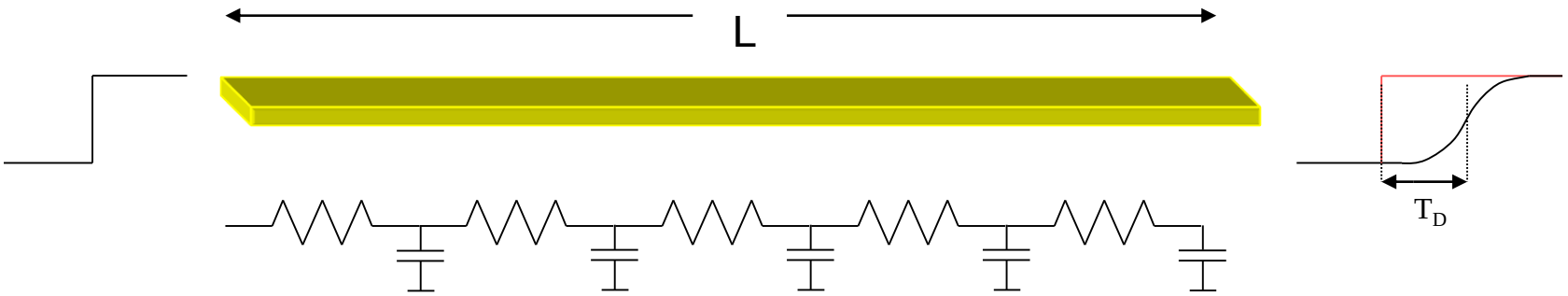
Plastic package
low impedance at high freq.

Interference paths

Use shield on the top

Long Interconnections

The distributed resistance and capacitance introduce a dispersion of the signal



$$T_D = \frac{1}{2} R_U C_U L^2$$

R_U, C_U resistance and capacitance per unit length

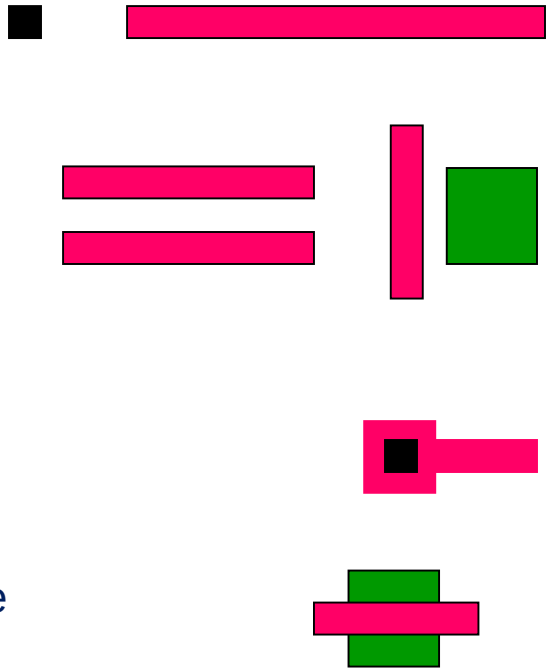
Part I: Process and Overview Topics

- Basic Materials
  - Silicon, Polysilicon,
  - Silicon dioxide, Silicon nitride
- CMOS process Overview
  - Generic CMOS cross-section
  - How layers form parasitic effects
  - Process gradients: die and wafer
- General Constrains
  - Design rules
  - Failure mechanisms
- High frequency/radio frequency considerations
  - EM fields near traces
  - Grounding, Shielding

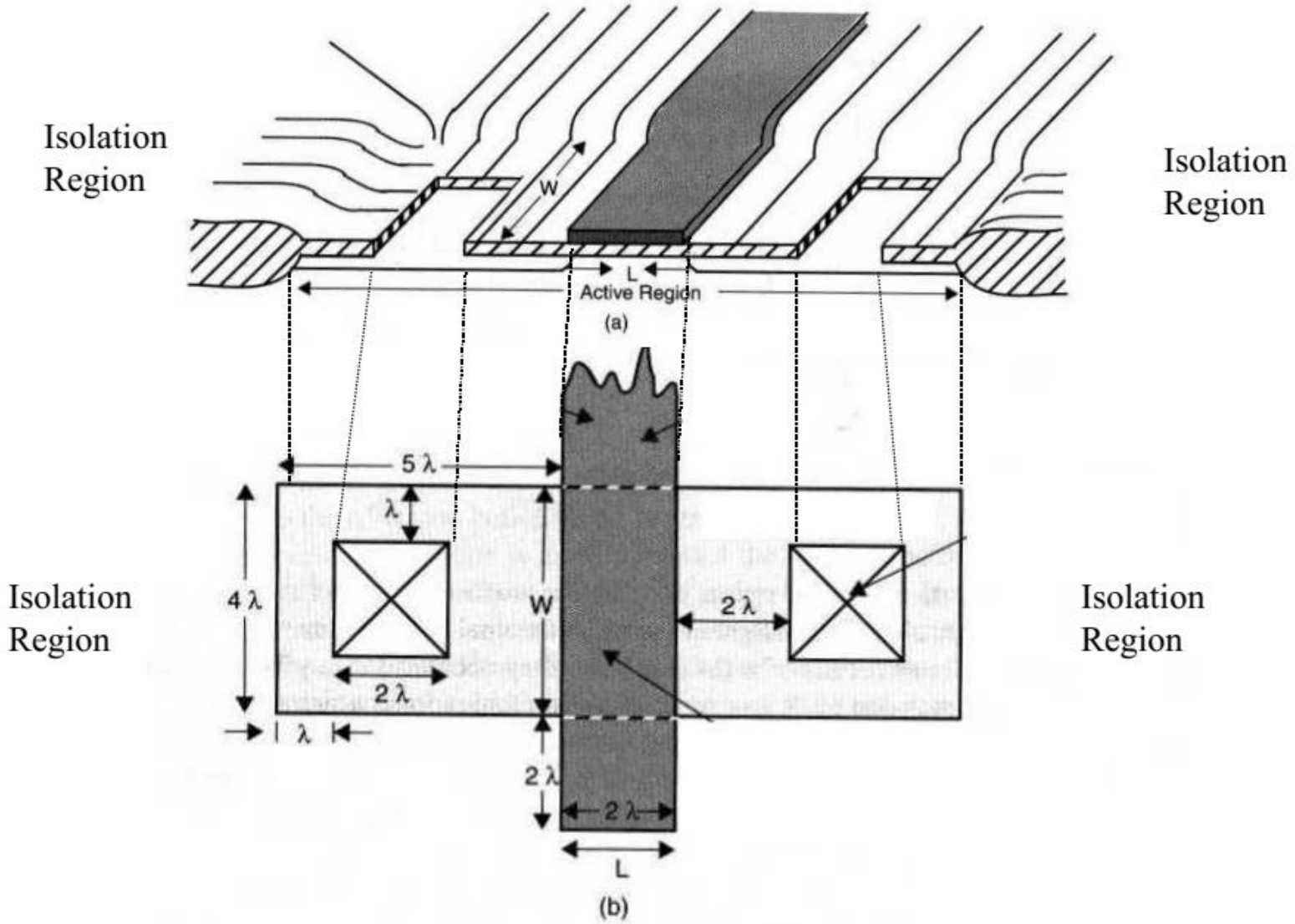
Design Rules

- Design rules guarantee a proper yield despite tolerances in each step of the technology flow

- Minimum width and length
  - imposed by lithography and etching
- Minimum spacing
  - geometry's on the same mask
  - geometry’s on different masks
- Minimum enclosure
  - a geometry must completely surround another
- Minimum extension
  - a geometry must completely cross another one



Design Rules

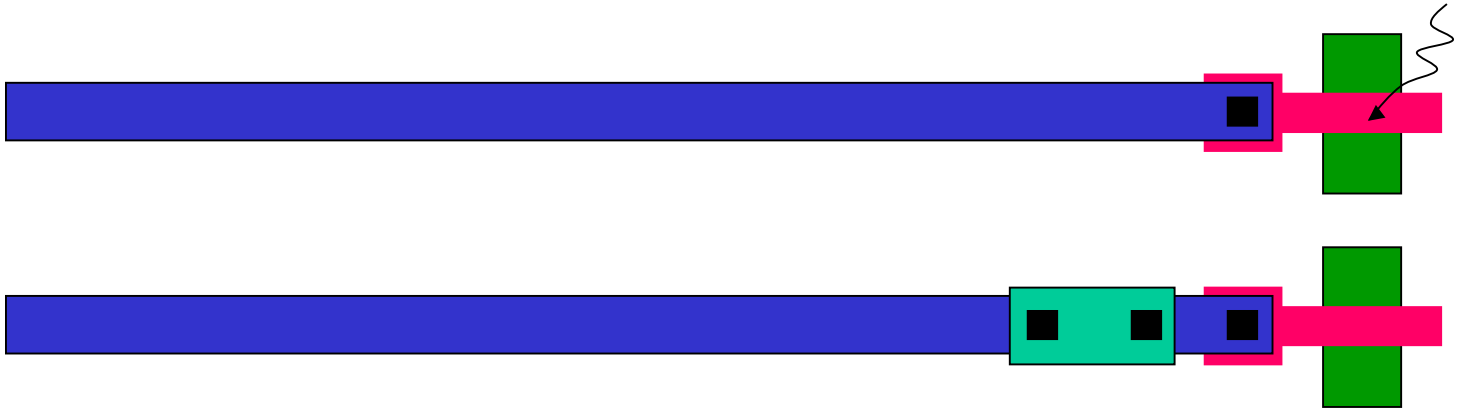


Failure Mechanisms

- Electrical Overstress
  - The antenna effect
- Corrosion
- Hot Carrier Effect
- Substrate Debiasing
- Electro-migration

Electrical Overstress: antenna effect

- Electrical stress can break the gate oxide. Assuming 4×10^6 V/cm dielectric strength, the maximum voltage across a 40 nm oxide is 16 V.
- During dry etching an ionized plasma charges conductors proportionally to their area. For large areas the resulting voltage can be disruptive (antenna effect)

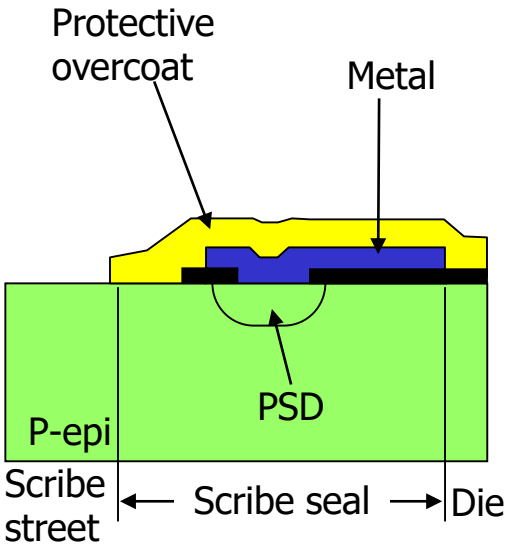


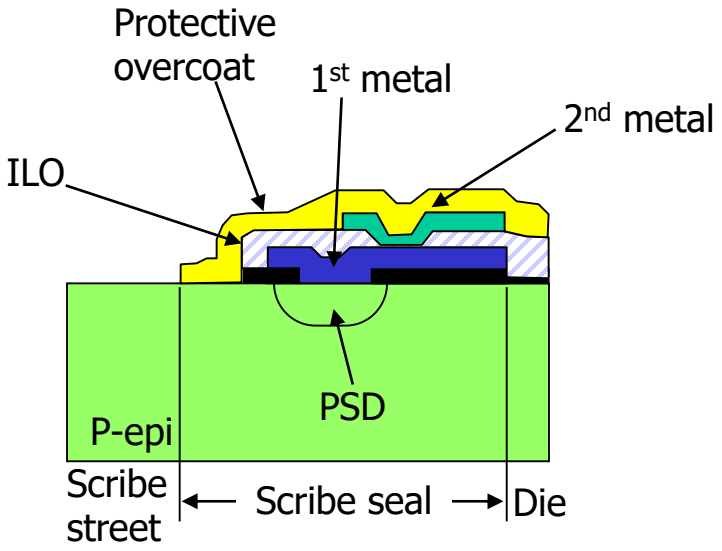
Use of metal 2 jumper

The large metal 1 area is etched when the gate is not connected

Corrosion

- Moisture favor the corrosion (oxidation) of aluminum
  - Minimize protective overcoat opening
  - Testpad for evaluation on a special mask
  - Scribe-line seal



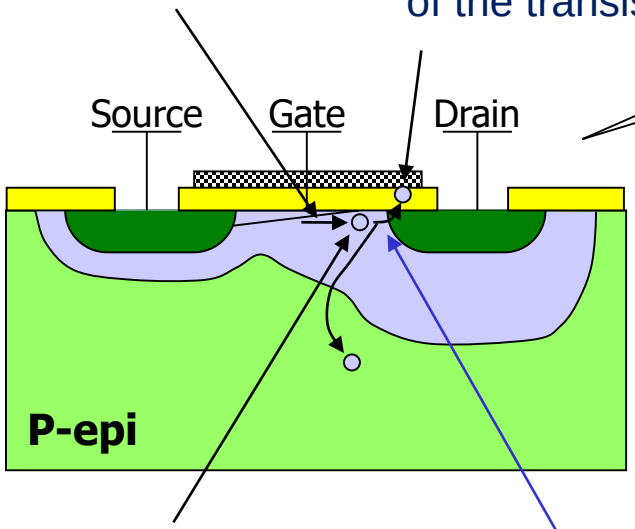


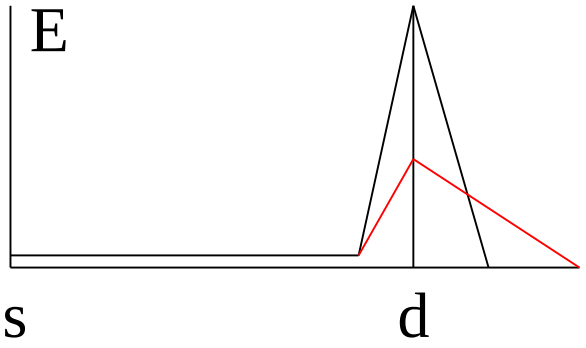
Hot Carrier Effect

High electric fields in the pinched-off region produce hot electrons

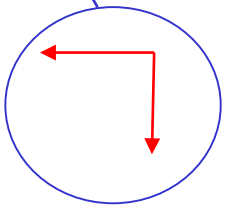
Hot electrons injected into the gate oxide shift the threshold voltage of the transistor

threshold shift: AGING





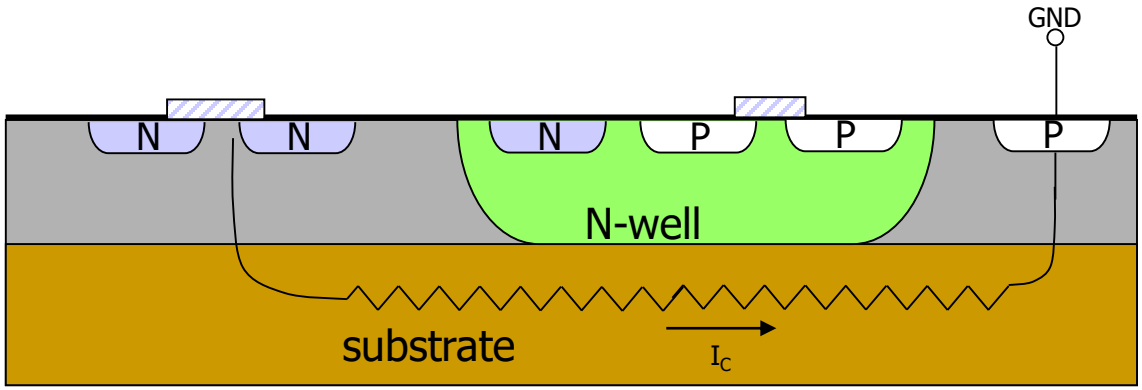
Hot carriers colliding with lattice atoms are deflected away from the drain



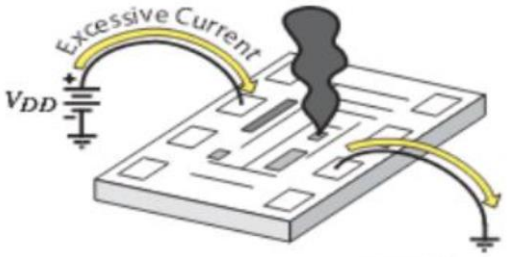
Low doped drain or drain extension

Substrate Debiasing

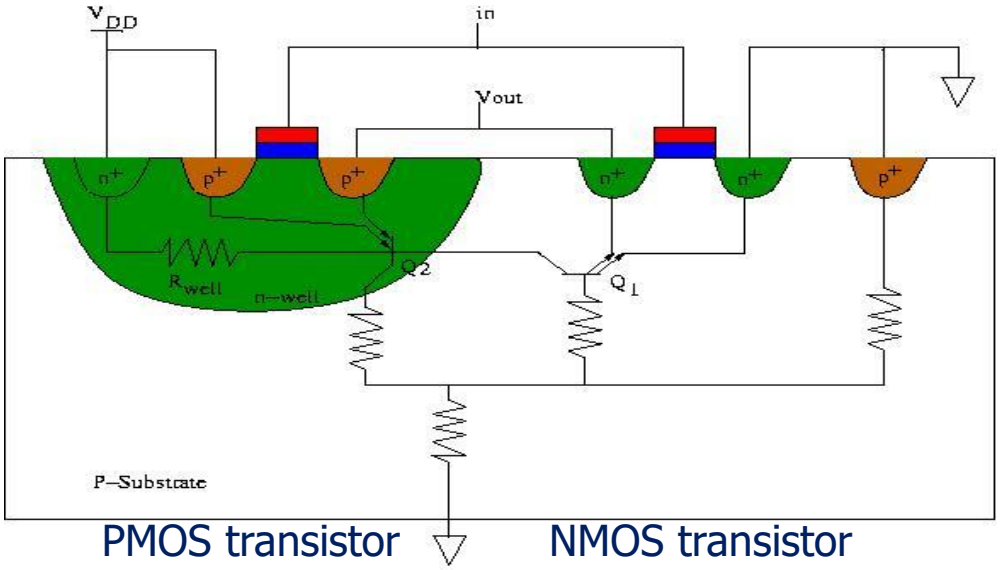
- Current in the high resistive substrate lead to significant drop voltages
  - bias solidly the substrate (or epi)
  - but a protection ring around devices that can suffer by current injection



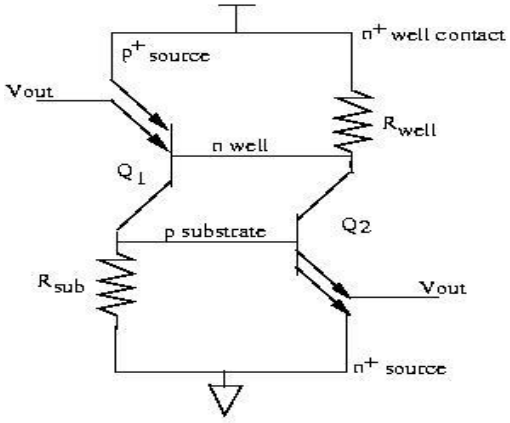
Latch-up

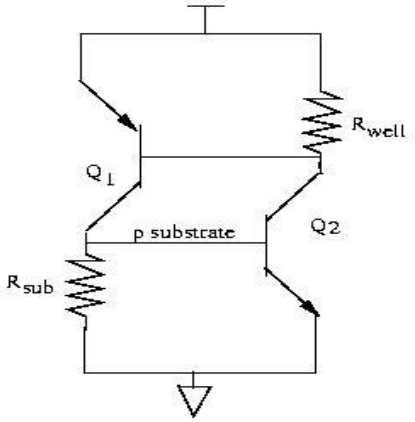


Latch is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic pnp and npn bipolar transistors.



PMOS transistor NMOS transistor





Electro-migration

- Electron flowing through the metal collide with atoms of the lattice. When the current density exceeds many 10 $\mu A/\mu^2$ metal atoms begin to move
- The displacement of atoms can produce a local thinning of the metal or gaps and, eventually, cause an open circuit
- A fraction of percent of copper added to the aluminum improves the electro-migration resistance
  - Large current requires thick or wide metal lines

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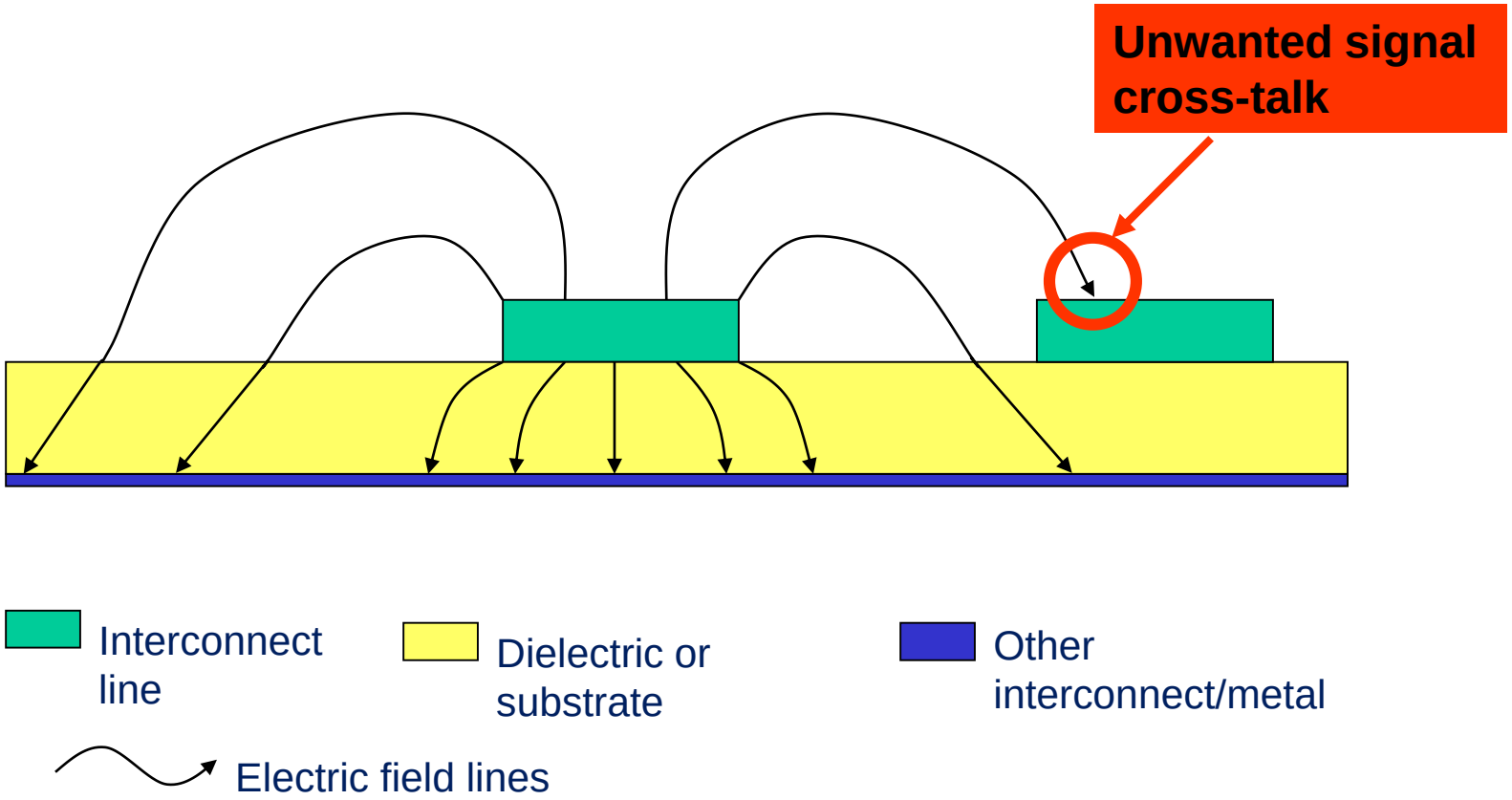
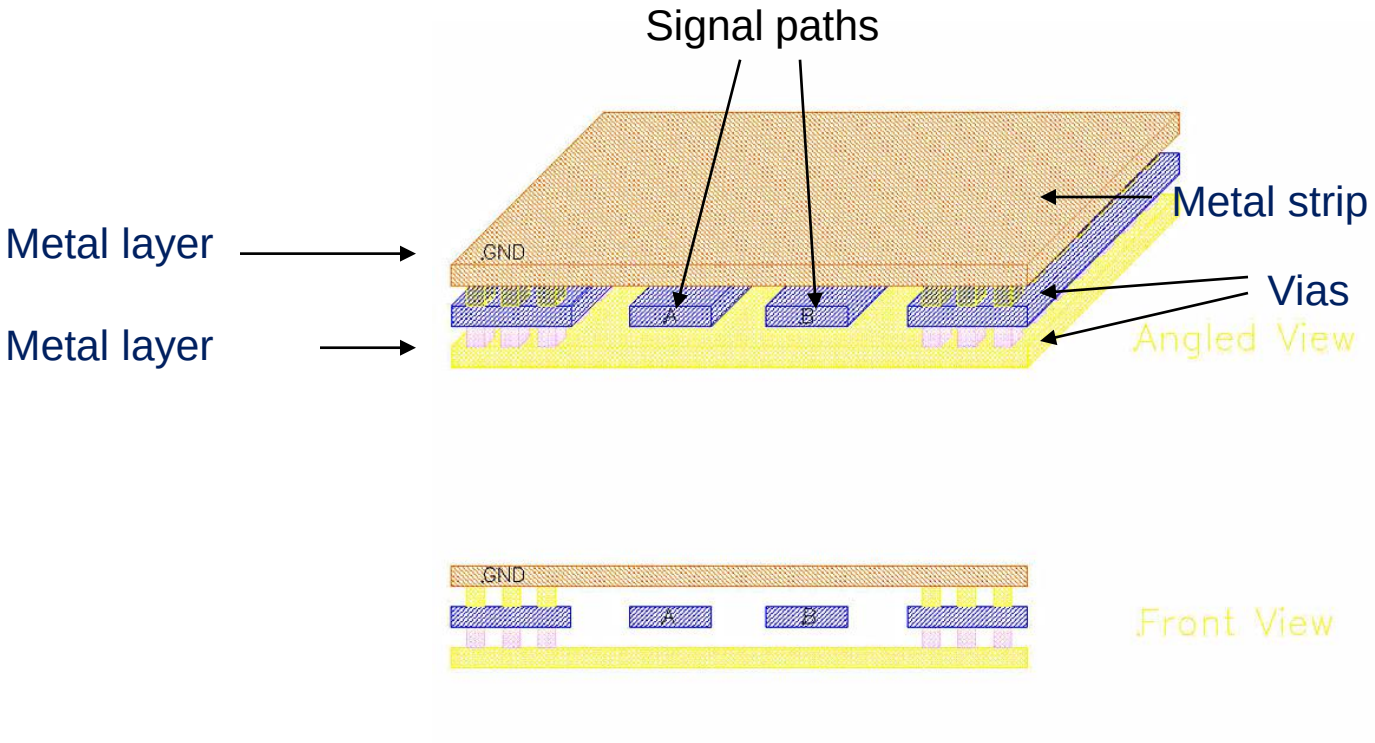
EM Field Near Traces



Grounding, Shielding



The technique shown here creates a shield surrounding the signal traces that are connected to ground. This prevents signals from radiating out to other parts on the chip.

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- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
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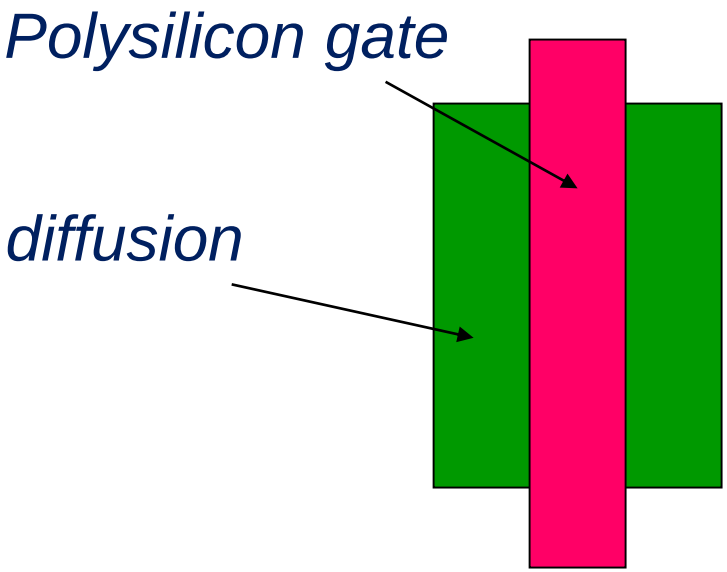
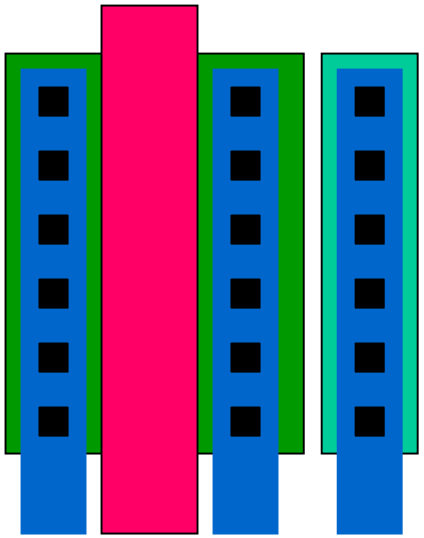
Part II: Transistor and Basic Cell Layout

- Transistors and Matched Transistors
  - Layout of a single transistor
  - Use of multiple fingers
  - Interdigitated devices
  - Common Centroid
  - Dummy devices on ends
  - Matched interconnect (metal, vias, contacts)
  - Surrounded by guard ring
- Design for Layout
  - Stacked layout of analog cells
  - Stick diagram of analog cells
  - Example 1: two stages op-amp
  - Example 2: folded cascode

Single Transistor Layout

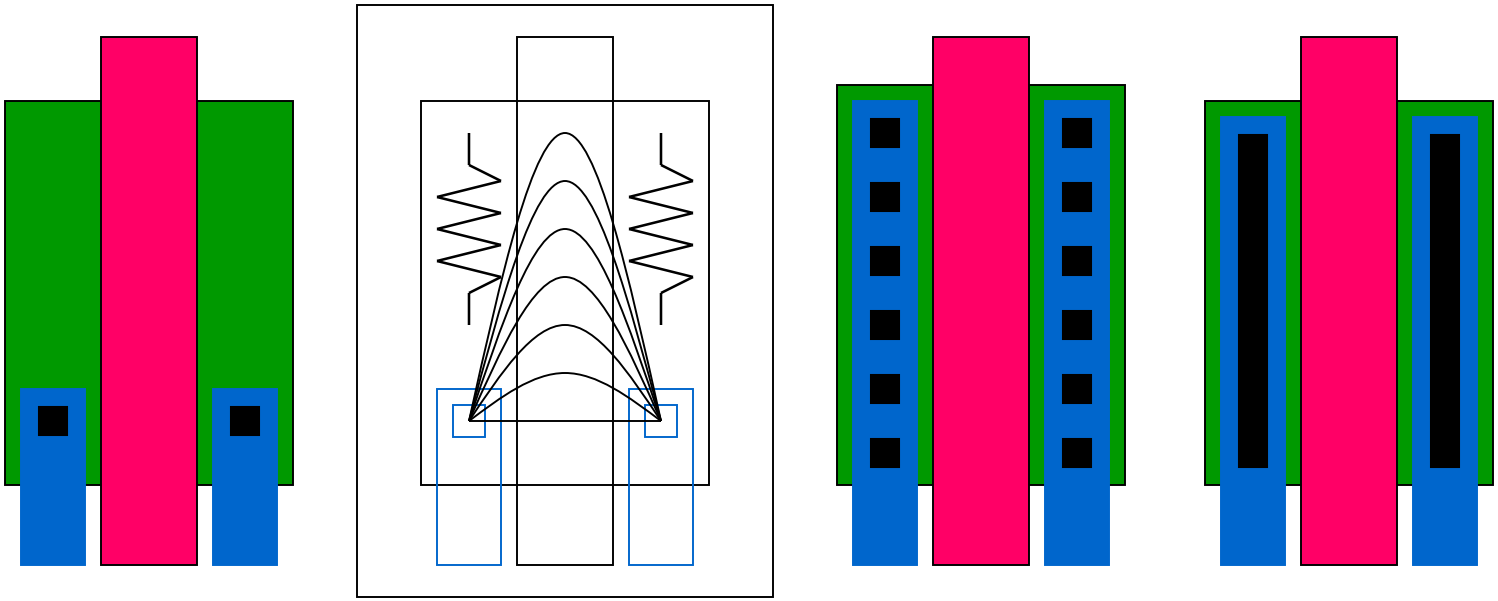
- A CMOS transistor is the crossing of two rectangles, polysilicon and active area
- but, … we need the drain and source connections and we need to bias the substrate or the well





Source and Drain Connections

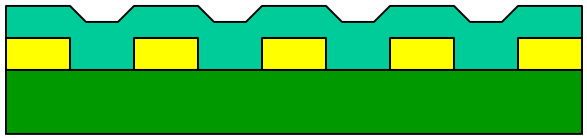
- Ensure good connections



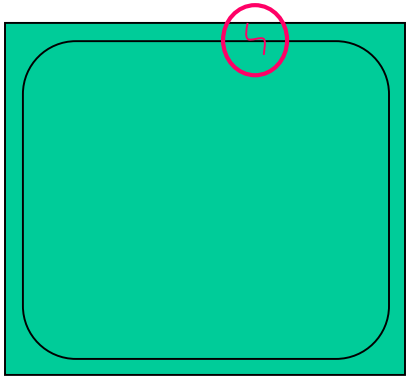
- Multiple contacts or one big contact?

Multiple or single contacts?

- Curvature in the metal layer can lead to micro-fractures



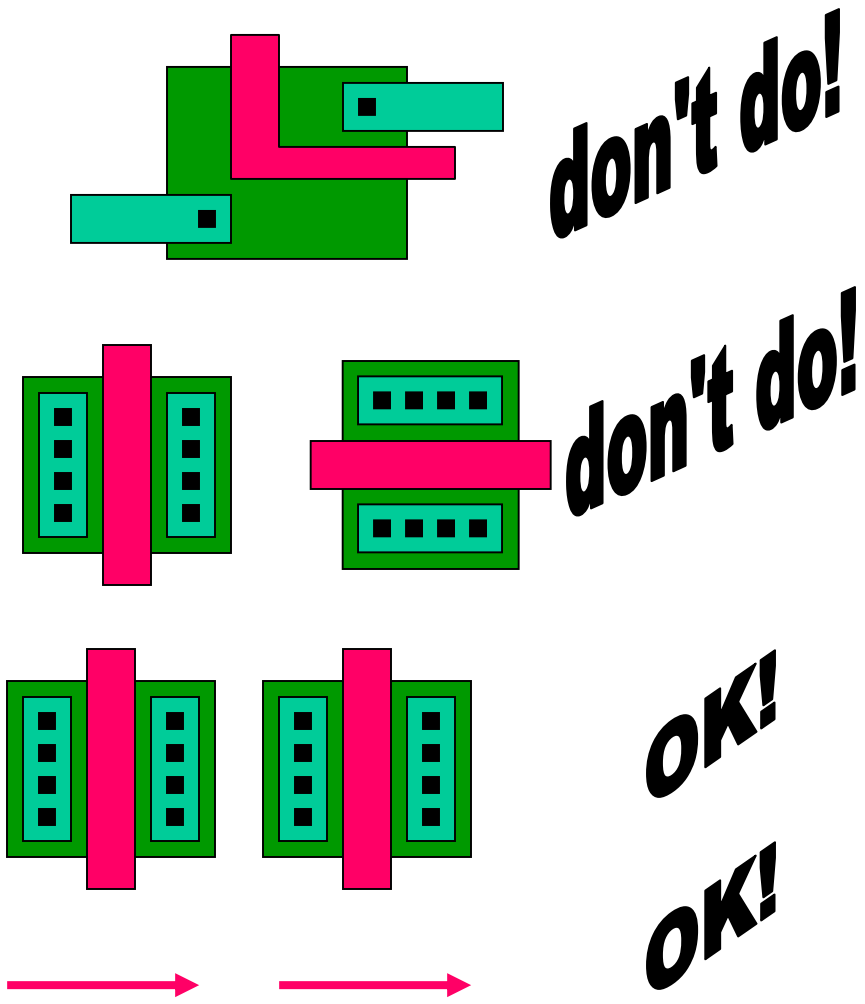
- Not important for large areas



Reliability problems, possible electro-migration

Matching single Transistors(Geometric Effects)

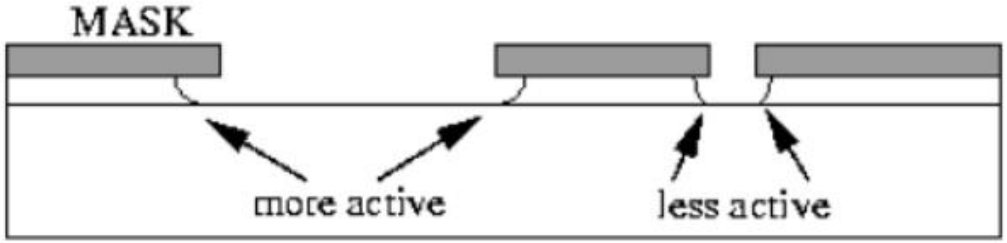
- Regular (rectangular shape)
  - the W and L matter!!
- Parallel elements
  - silicon is unisotropic
- Possibly, the current flowing in the same direction

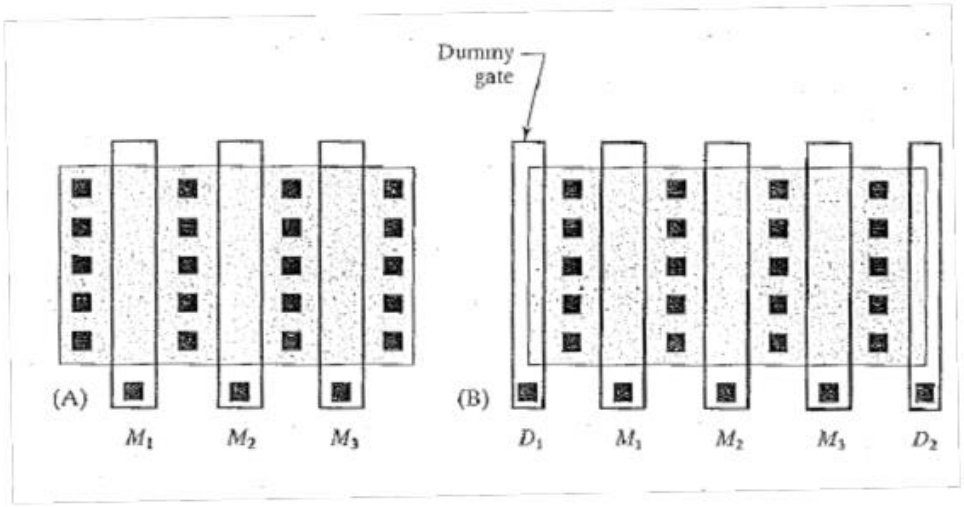


Geometric Effects

Etch Effects

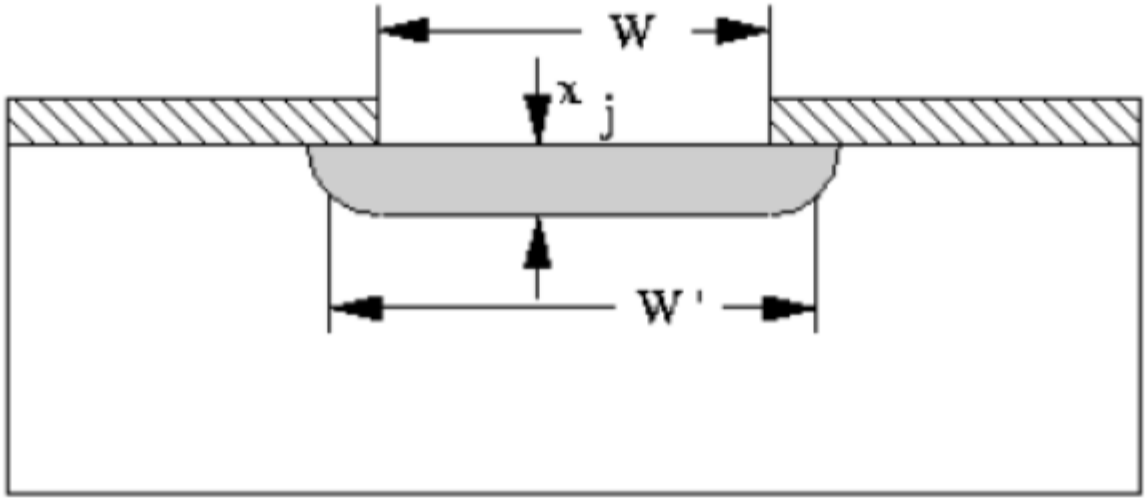
- Polysilicon does not always etch uniformly
  - Large openings etch faster than small openings in mask
  - Solution is to use dummy structures





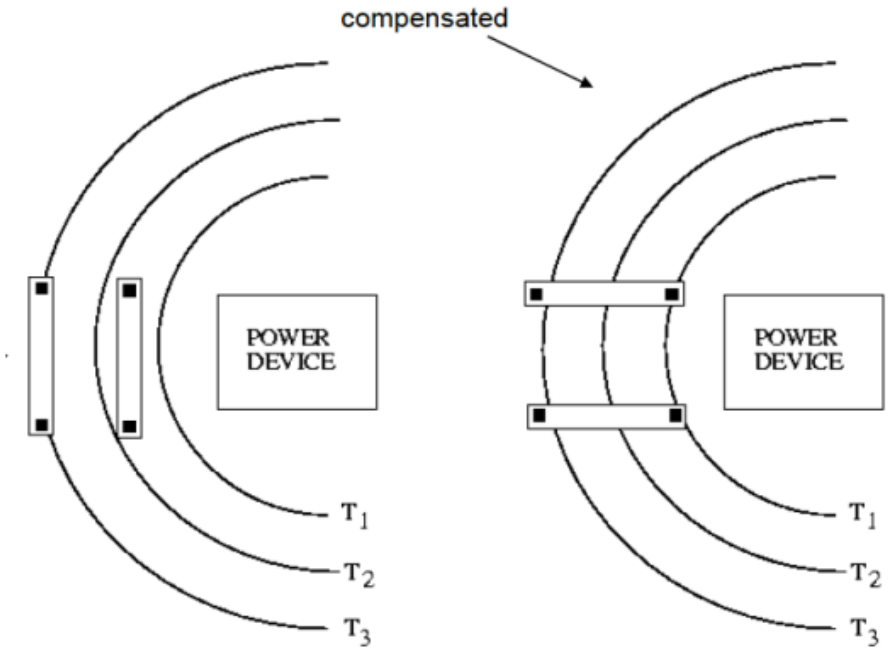
Diffusion Effects

- Diffusion widens implanted region
  - Can affect doping of neighboring devices
  - Solution is to increase distance and use dummy structures that affect all transistors the same



Thermal Effects

- Temperature affects
  - Mobility and threshold voltage
  - Resistance value



Stress Effects

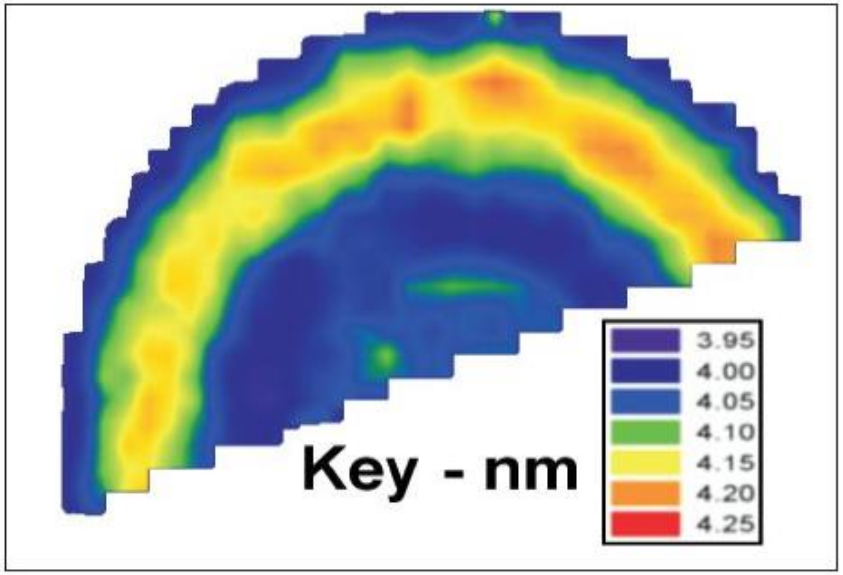
- The fabrication under high temperatures may leave residual stresses in chip
- Packaging can cause stress in chip

Solutions

- Keep critical matched devices in centre of chip or on centerlines
- Avoid using corners for matched devices

Oxide Thickness Gradients

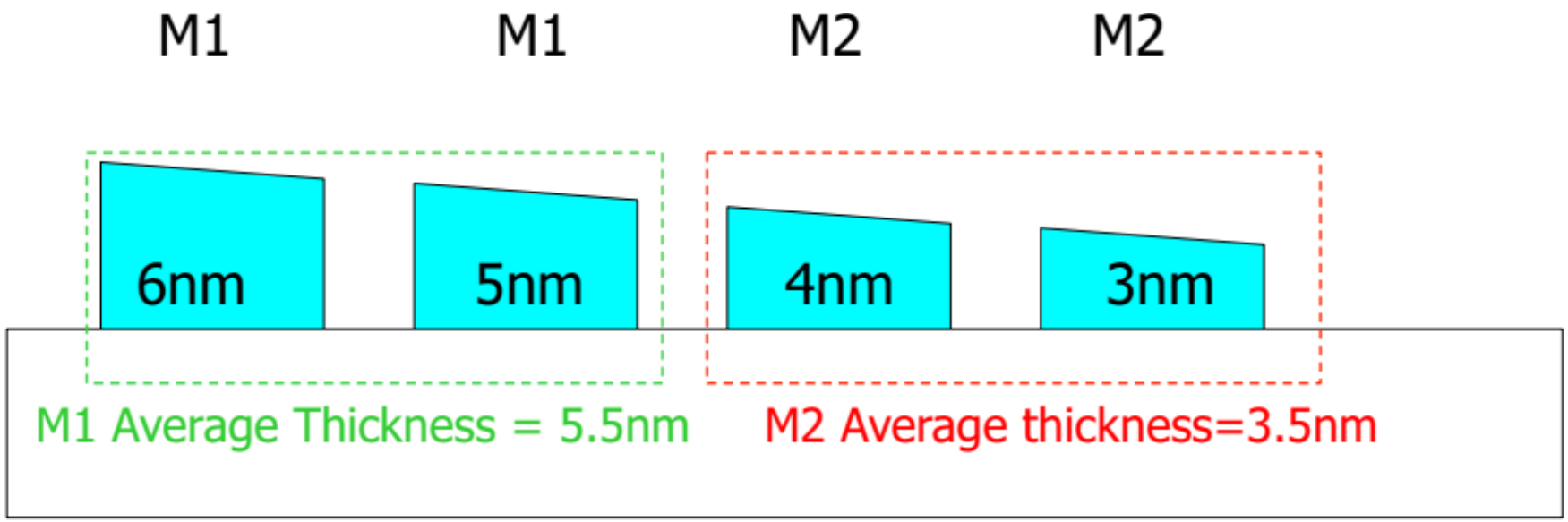
- Thermally grown oxides depend on temperature and oxidizing atmosphere
- Modern oxidation furnaces, although well controlled in temperature still have temperature gradients.



Oxide thickness on 200 mm wafer

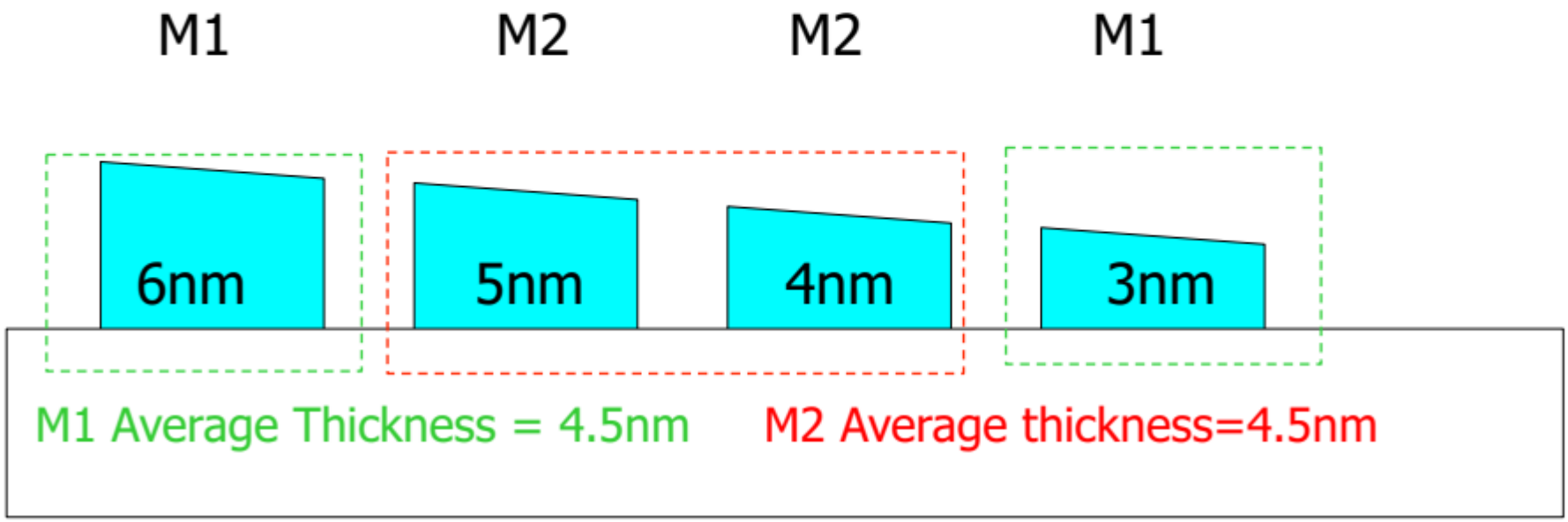
Common Centroid

- Matching Won't be good!!!



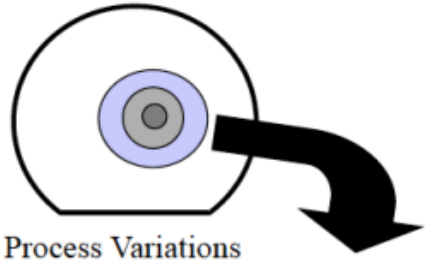
Common Centroid

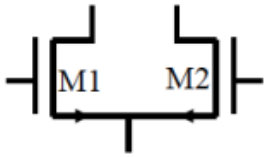
- Break and distribute parts of a transistor so as to canell out the effects of oxide / doping gradient profiles.



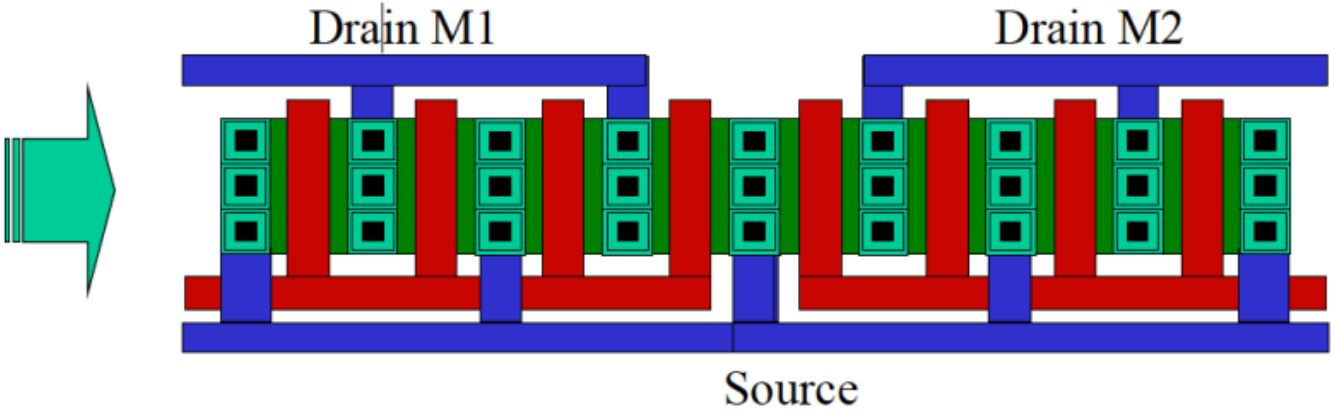
Transistor Matching

- Example of Differential Pair
  - ✗ Not matching with thermal gradients!!!



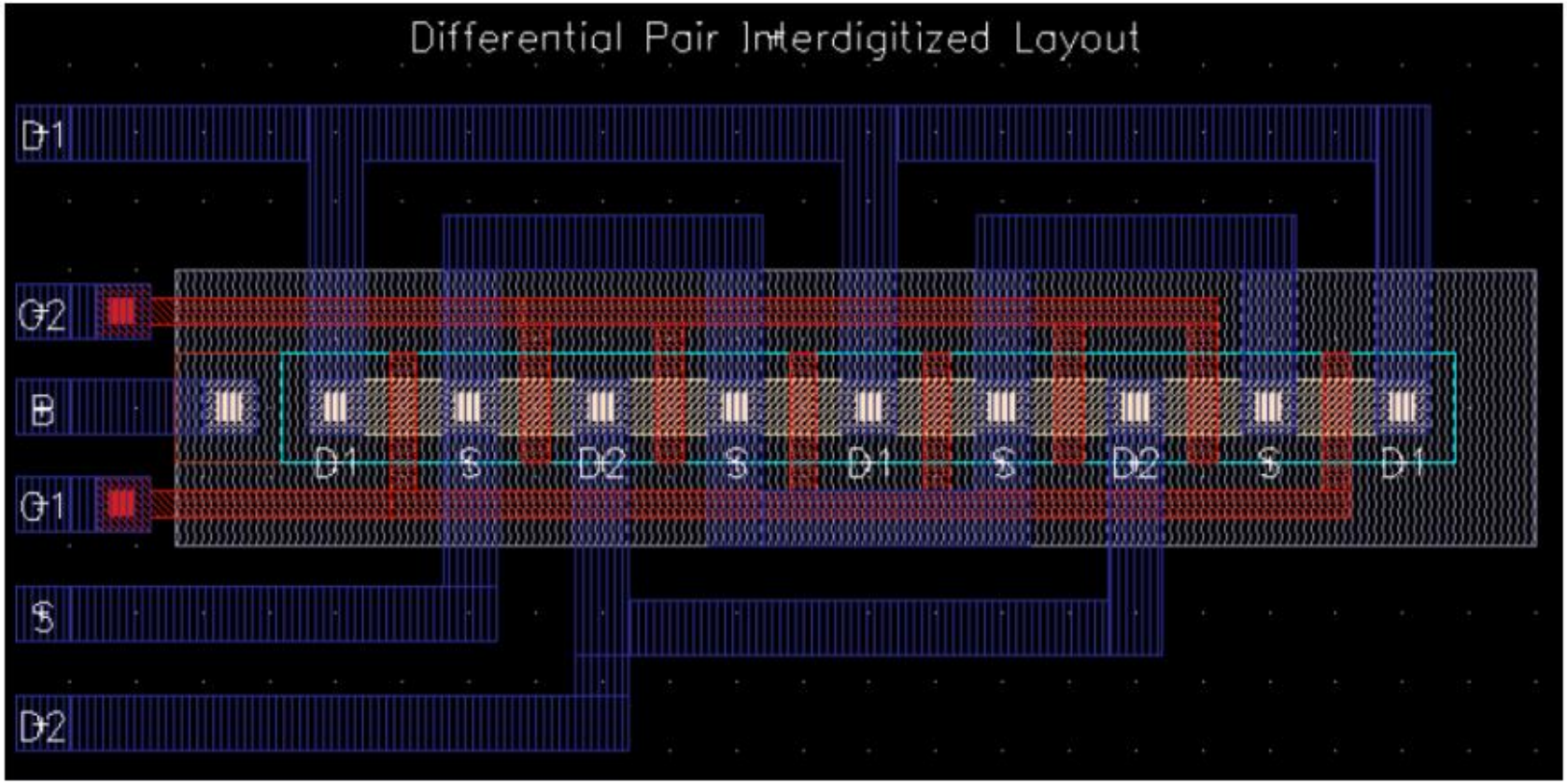


Differential pair requiring "matched transistors"



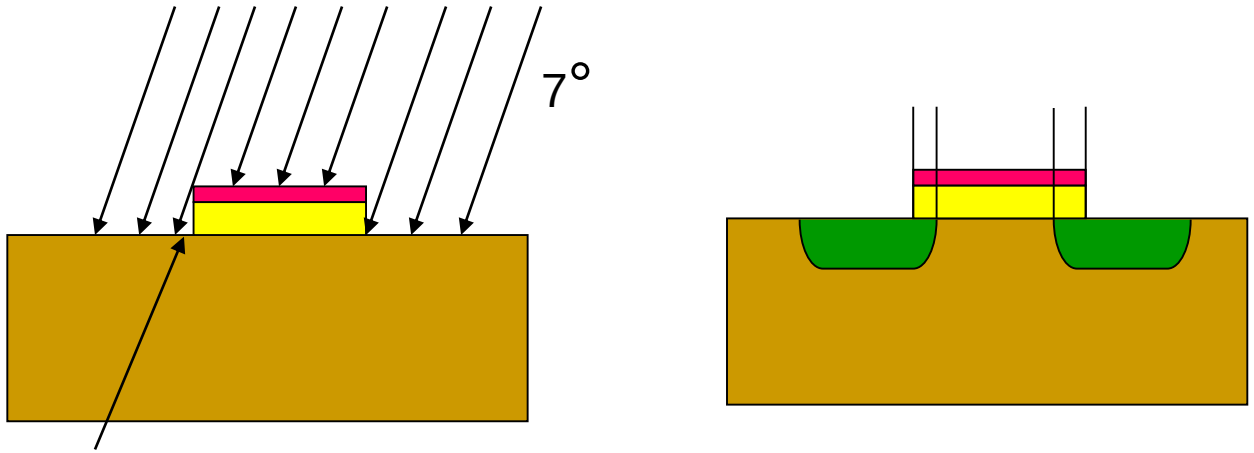
Common Centroid Layouts

- Averages Process Variations



Asymmetry due to Fabrication

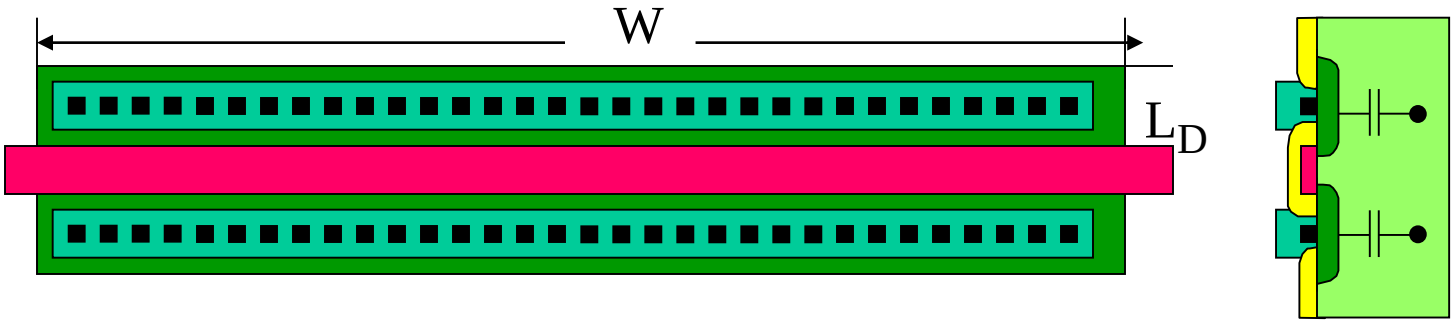
An MOS transistor is not a symmetrical device. To avoid channeling of implanted ions the wafer is tilted by about 7 °.



Source and drain are not equivalent

Parasitics in Transistors

- Analog transistors often have a large W/L ratio



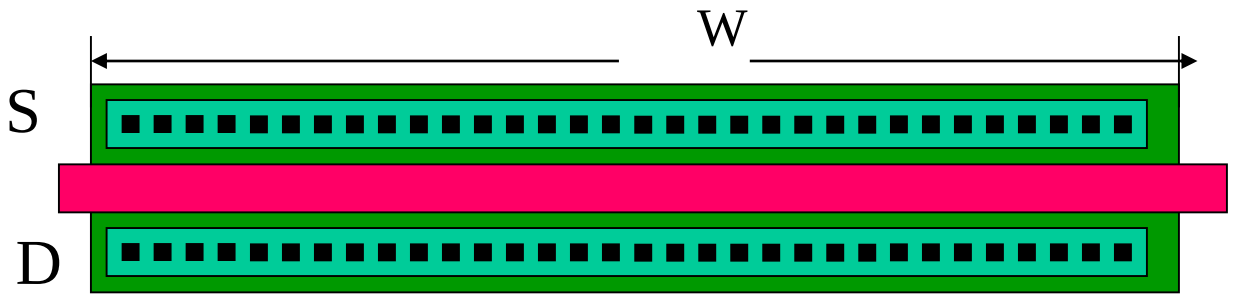
  - Capacitance diffusion substrate

$$C_{SB} = C_{DB} = (W + 2l_{diff})(L_D + 2l_{diff})$$

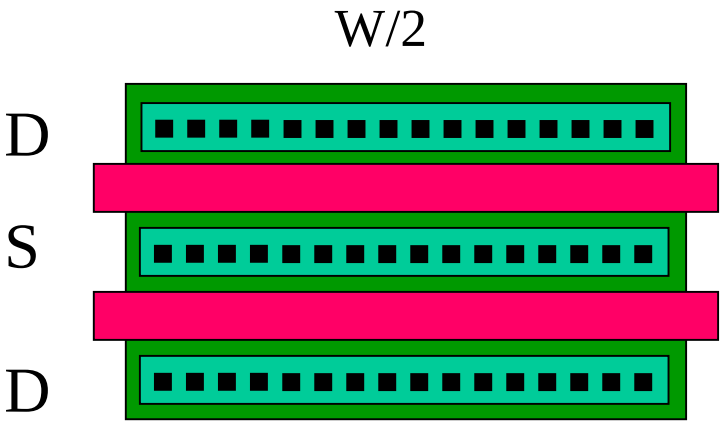
  - Resistance of the poly gate

$$R_{gate} = L_{gate} R_{sq,poly}$$

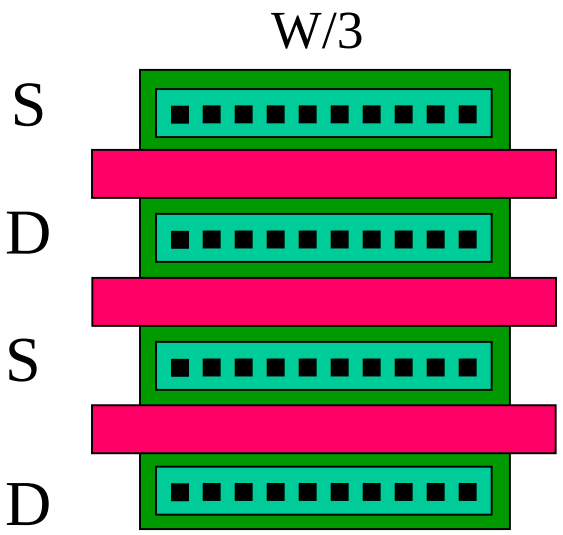
Use of multiple fingers



$C'_{SB}; C'_{DB}$



$$C_{SB} = \frac{1}{2} C_{DB}; C_{DB} = C'_{DB}$$



$$C_{SB} = \frac{2}{3} C'_{SB}$$

$$C_{DB} = \frac{2}{3} C'_{DB}$$

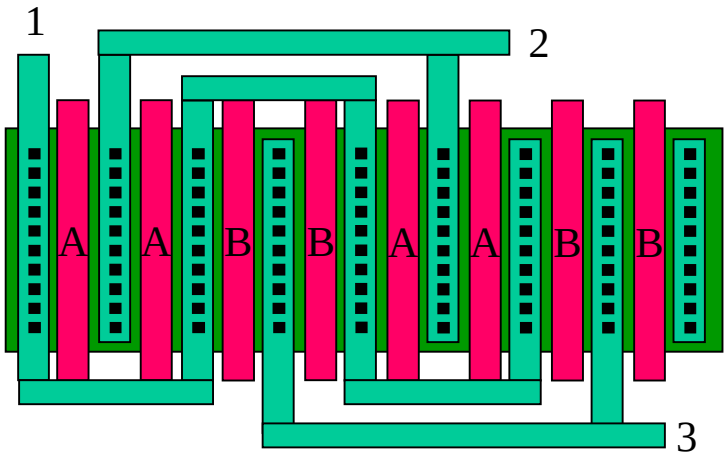
Parasitic in Transistors: Exercise

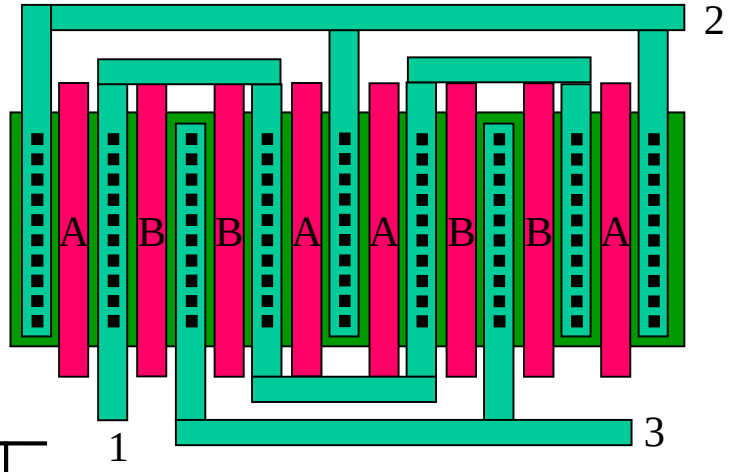
- Calculate the parasitic capacitance diffusion-substrate for a 40 micron width transistor
  - one finger
  - 5 finger
  - 8 finger

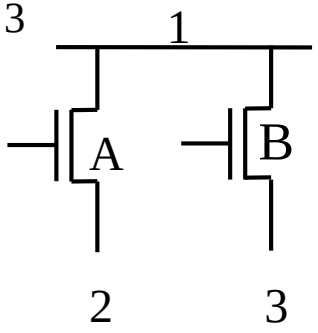
  - Use the design rules available and minimum diffusion length

Interdigitated Devices

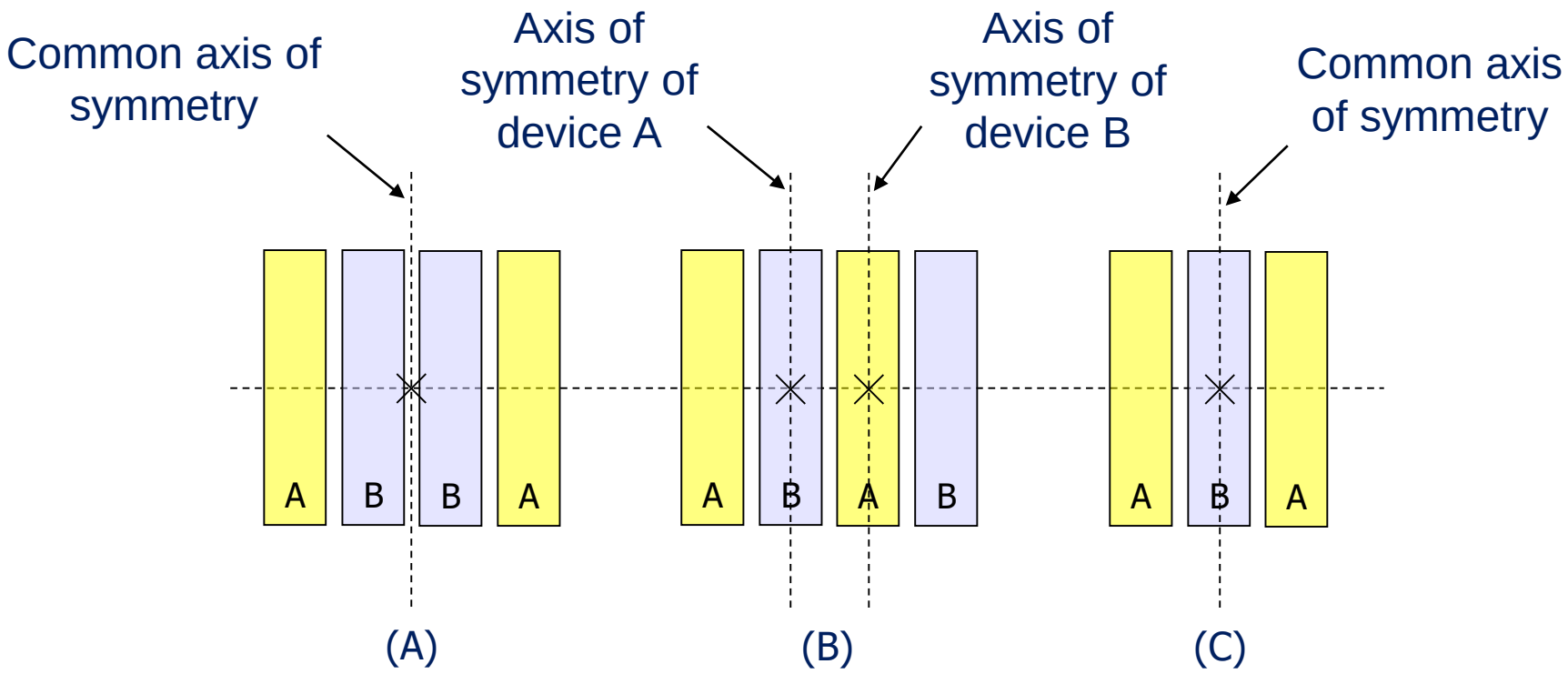
- Two matched transistors with one node in common
  - spilt them in an equal part of fingers (for example 4)
  - interdigitate the 8 elements: AABBAABB or ABBAABBA



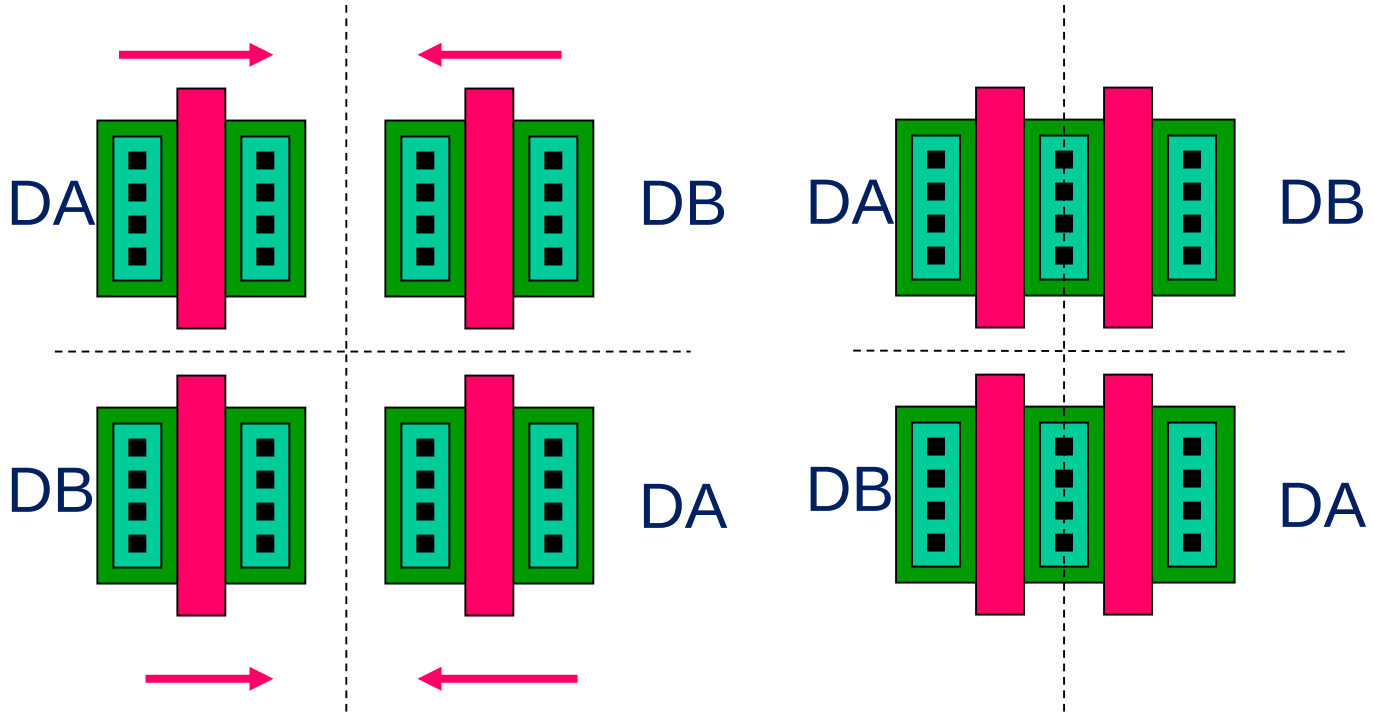




Axis of Symmetries

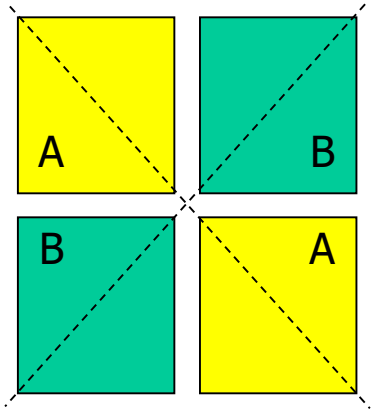


Common Centroid

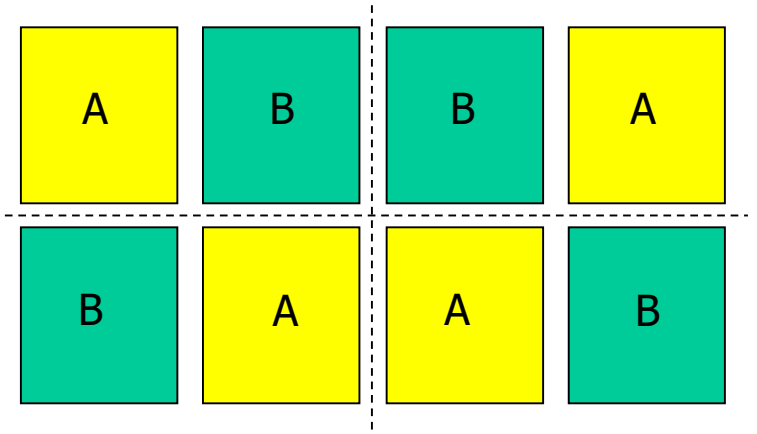


- Gradients in features are compensated for (at first approximation)
  - metal and poly interconnections are more complex

Common Centroid Arrays



Cross coupling



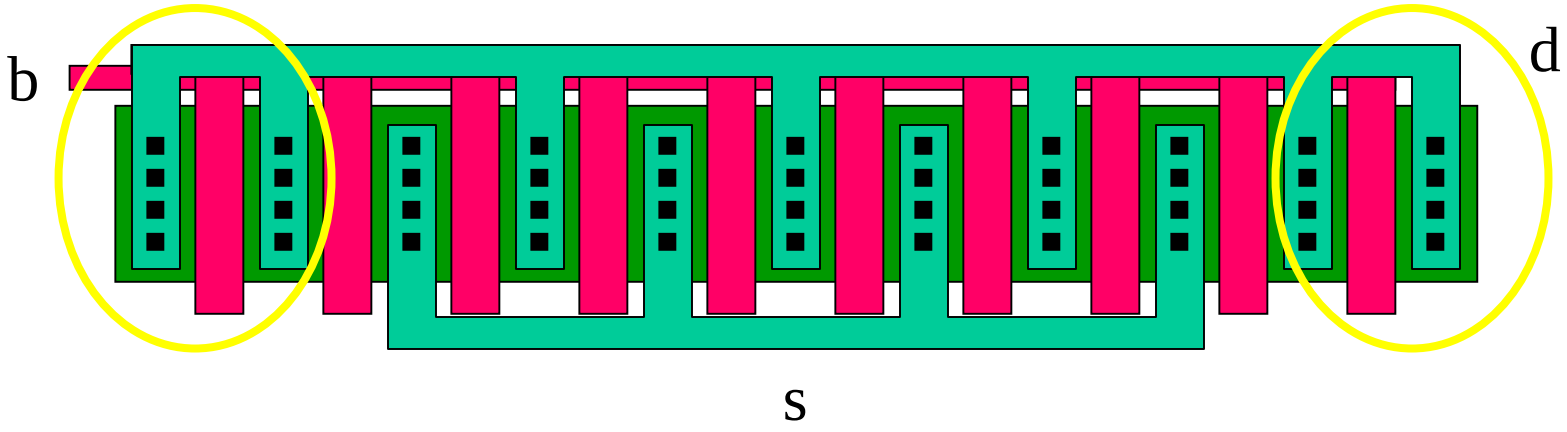
Tiling (more sensitive to high-order gradients)

Common Centroid Patterns

ABBA BAAB	ABBAABBA BAABBAAB	ABBAABBA BAABBAAB ABBAABBA	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
ABA BAB	ABAABA BABBAB	ABAABA BABBAB ABAABA	ABAABAABA BABBABBAB BABBABBAB ABAABAABA
ABCCBA CBAABC	ABCCBAABC CBAABCCBA	ABCCBAABC CBAABCCBA ABCCBAABC	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
AAB BAA	AABBAA BAAAAB	AABBAA BAAAAB AABBAA	AABBAA BAAAAB BAAAAB AABBAA

Dummy Devices on Ends

- Ending elements have different boundary conditions than the inner elements -> use dummy



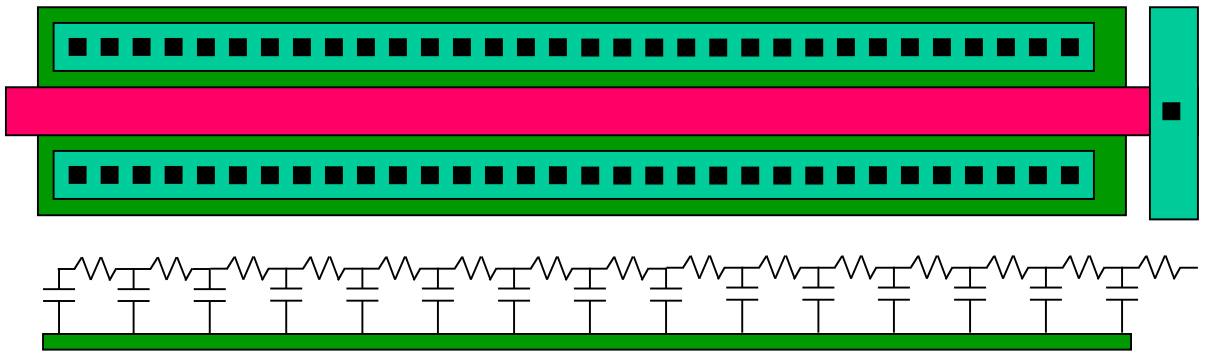
- Dummies are shorted transistors
  - Remember their parasitic contribution!

Matched interconnections

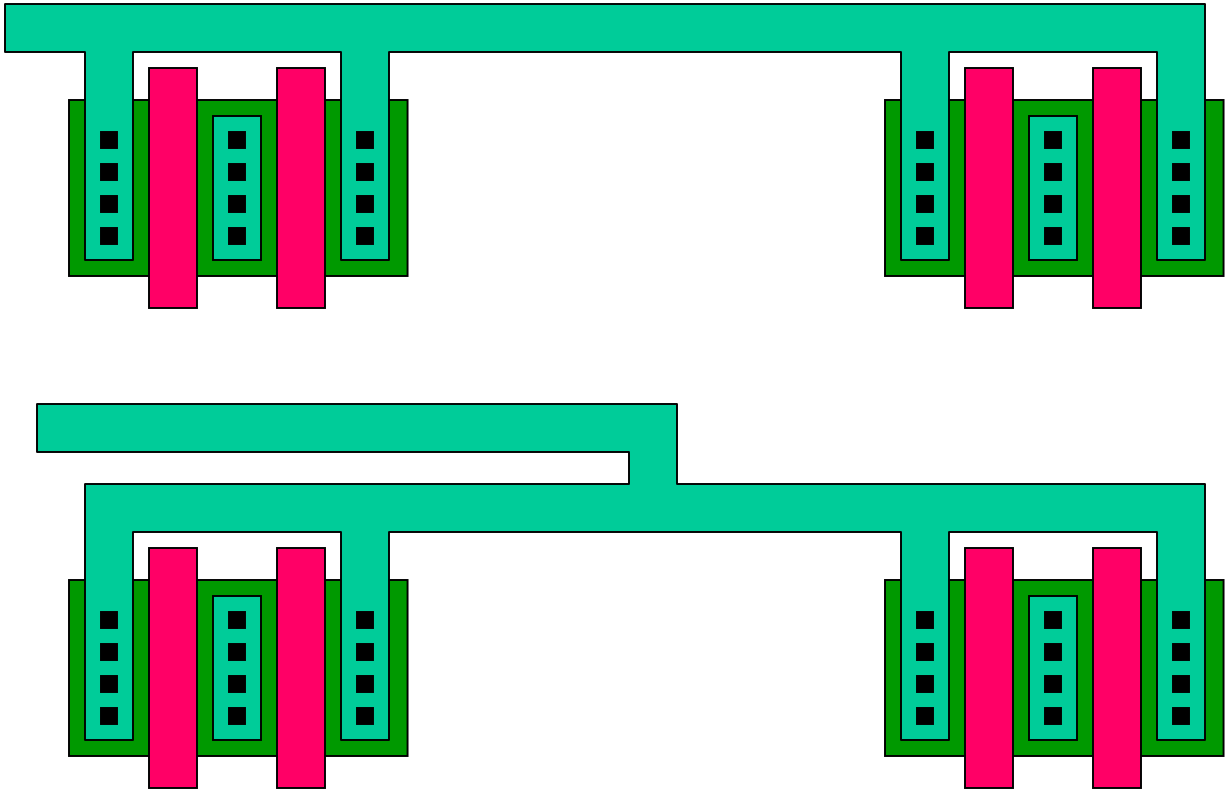
- Specific resistance of metal lines
- Specific resistance of poly
- Resistance of metal-contact
- Resistance of via

$$\Delta V = Z_{int} I$$

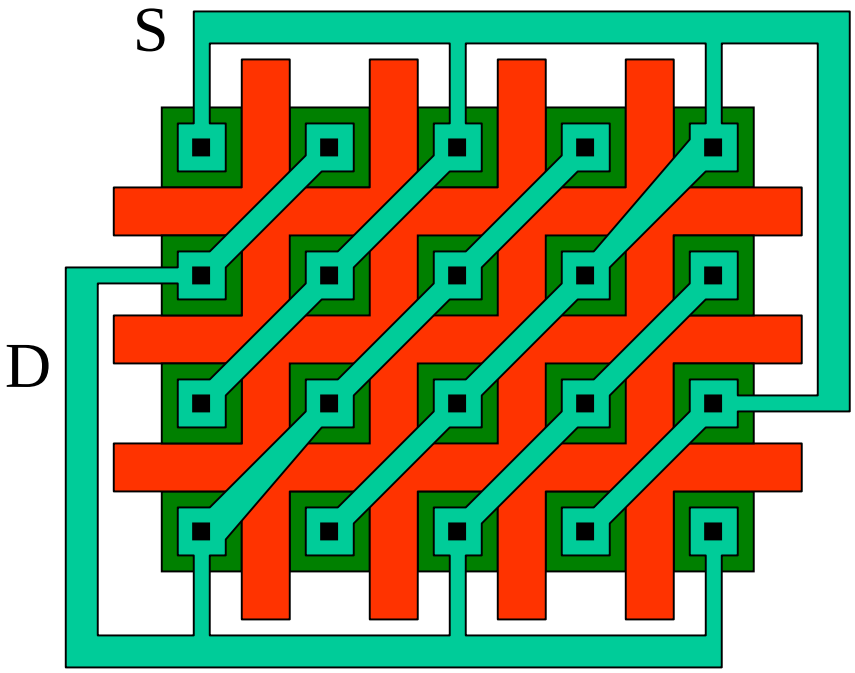
- Minimize the interconnection impedance
- Achieve the same impedance in differential paths
- Keep short the width of fingers for high speed applications



Matched Metal Connection



Waffle Transistor



Minimum capacitance drain-substrate and source-substrate

W not accurate
L not well defined

To be used in wide transistors whose aspect ratio is not relevant

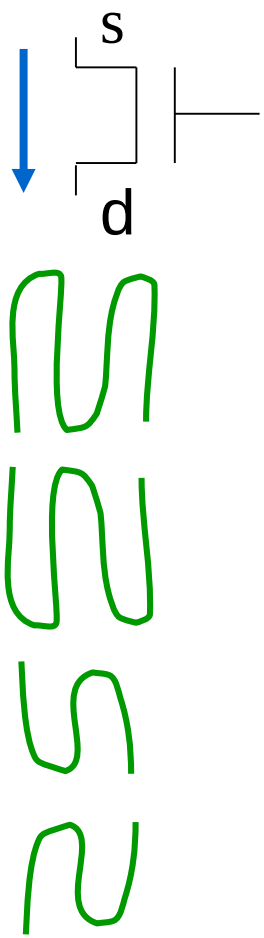
Part II: Transistor and Basic Cell Layout

- Transistors and Matched Transistors
  - Layout of a single transistor
  - Use of multiple fingers
  - Interdigitated devices
  - Common Centroid
  - Dummy devices on ends
  - Matched interconnect (metal, vias, contacts)
  - Surrounded by guard ring
- Design for Layout
  - Stacked layout of analog cells
  - Stick diagram of analog cells
  - Example 1: two stages op-amp
  - Example 2: folded cascode

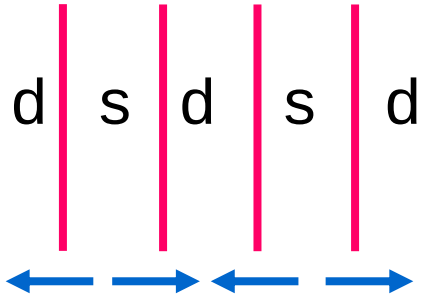
Stacked Layout

- Systematic use of stack or transistors (multi-finger arrangement)
- Same width of the fingers in the same stack, possibly different length
- Design procedure
  - Examine the size of transistors in the cell
  - Split transistors size in a number of layout oriented fingers
  - Identify the transistors that can be placed on the same stack
  - Possibly change the size of non-critical transistors
  - Use (almost) the same number of finger per stack
  - place stacks and interconnect

Stick Representation (one transistor)

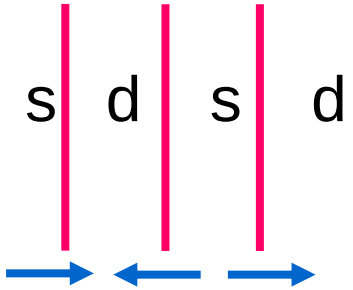


EVEN

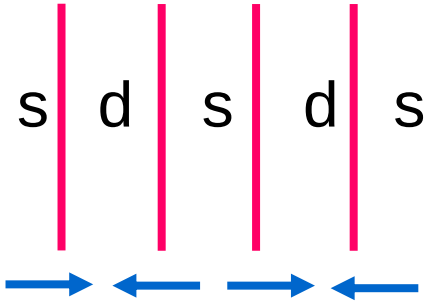


Ending drain

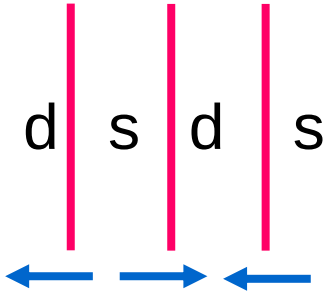
ODD



S/D ending

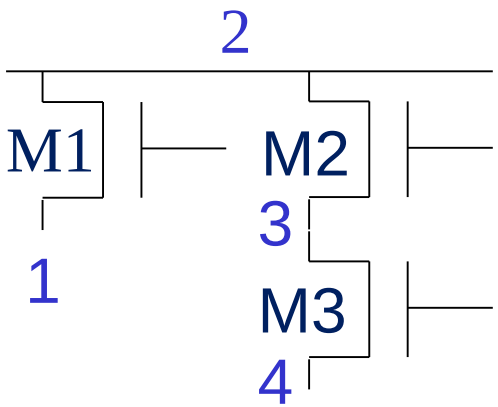


Ending source

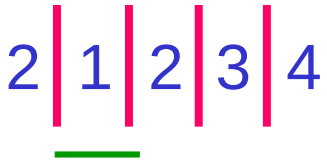


D/S ending

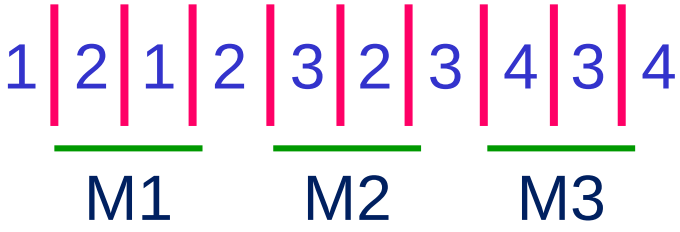
Multi-transistor Stick Diagram

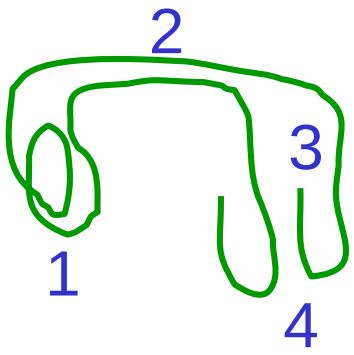


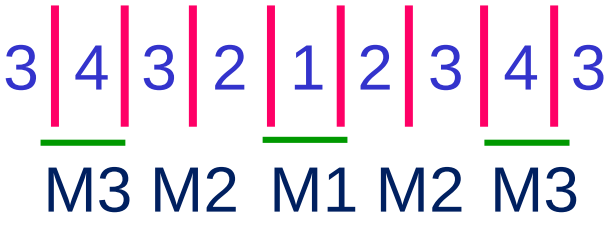
Same width

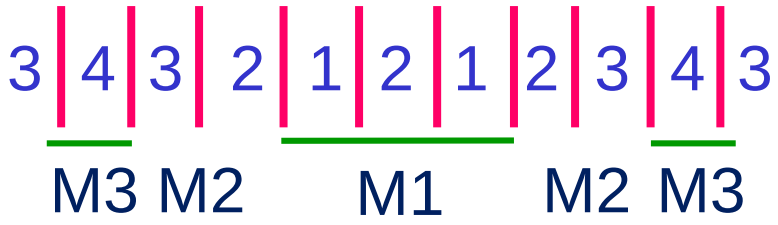


M1 double



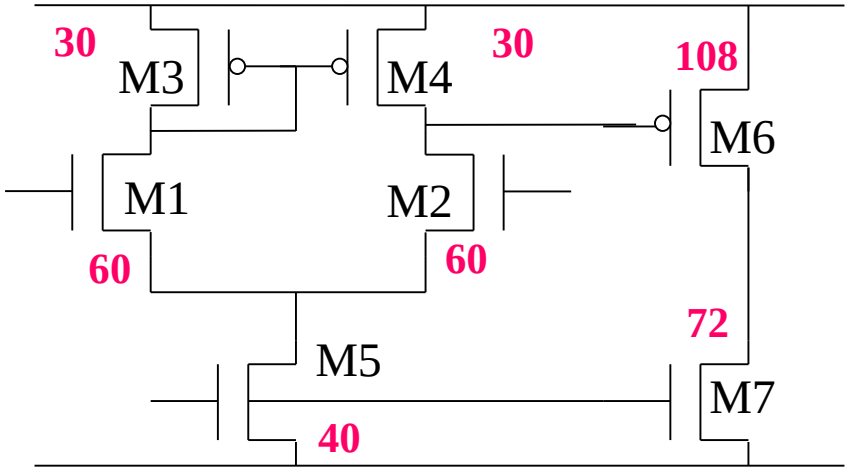






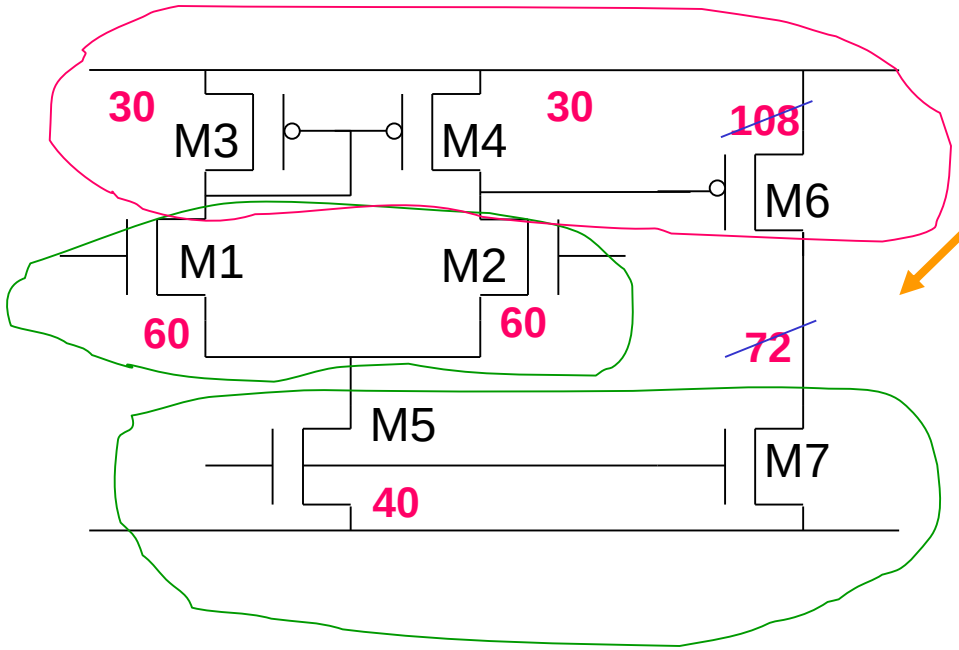
Example 1 (2 stages OTA)

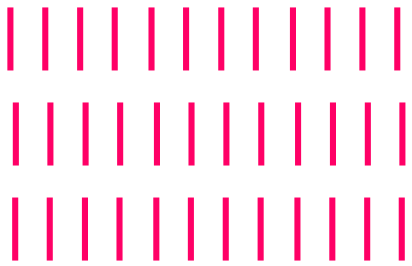
Assume to layout a two stages OTA



Width only are shown;
Compensation network and bias are missing (!)

Layout Oriented Design





M3, M4, M6

M1, M2

M5, M7

Only width matters

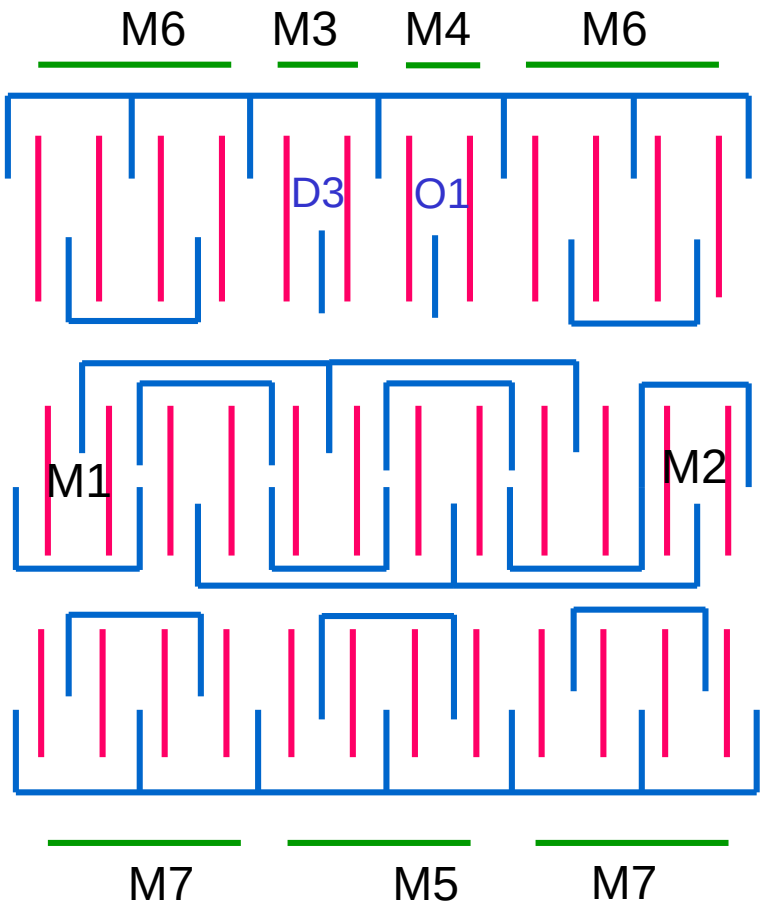
Possible stacks:
1 p-channel, 2 n-channel

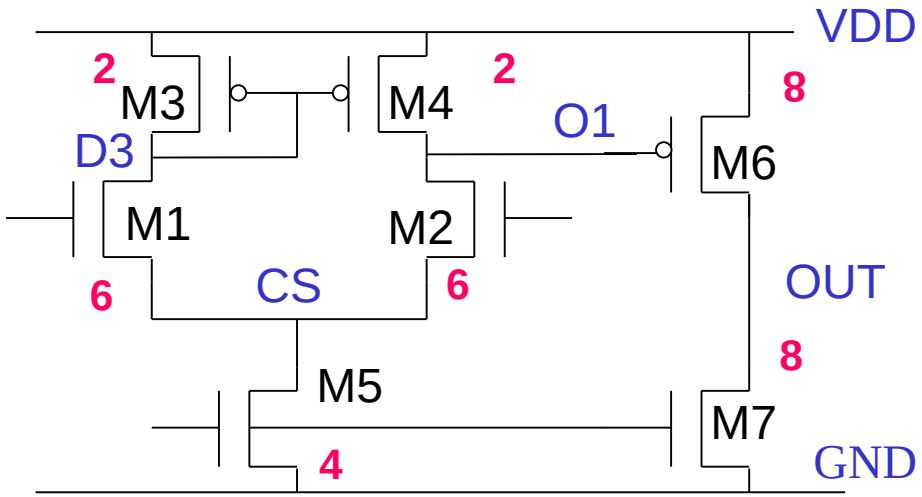
change the size of M6 and M7 to 80 and 120 respectively

Width of each finger?
We want the same number of fingers per stack (k).
W_{p1} = 180/k
W_{n1}=120/k
W_{n2}=120/k

for M3 and M4 use 2 fingers

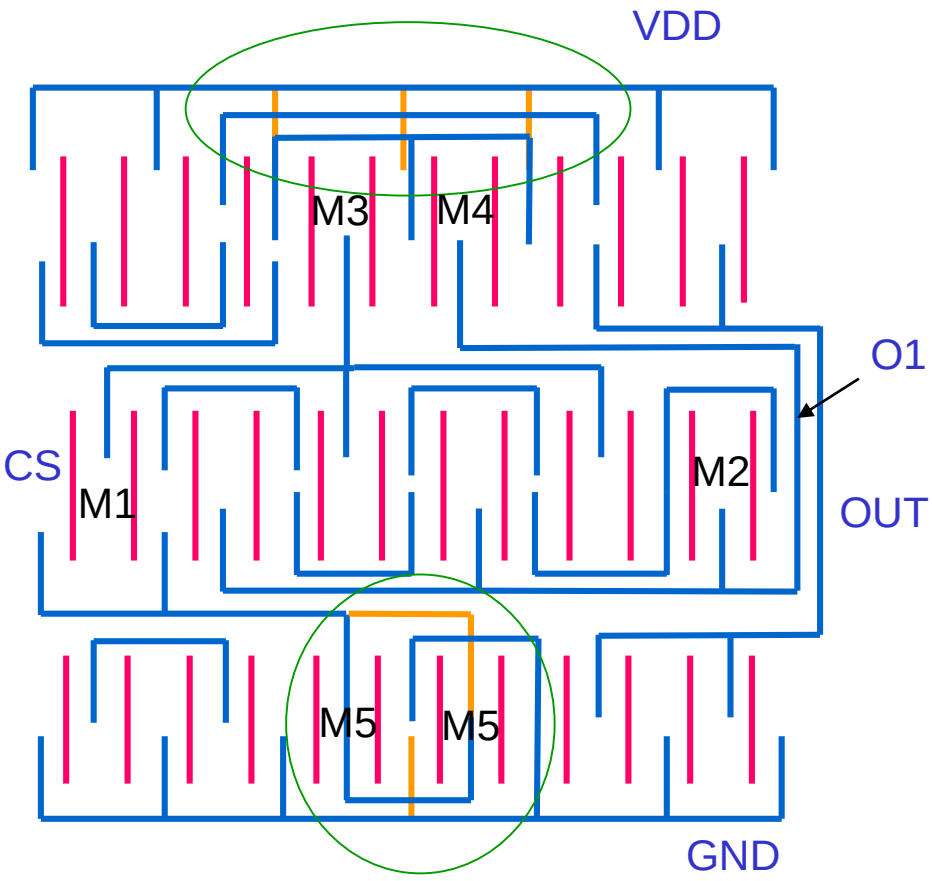
Stack Design and Interconnections

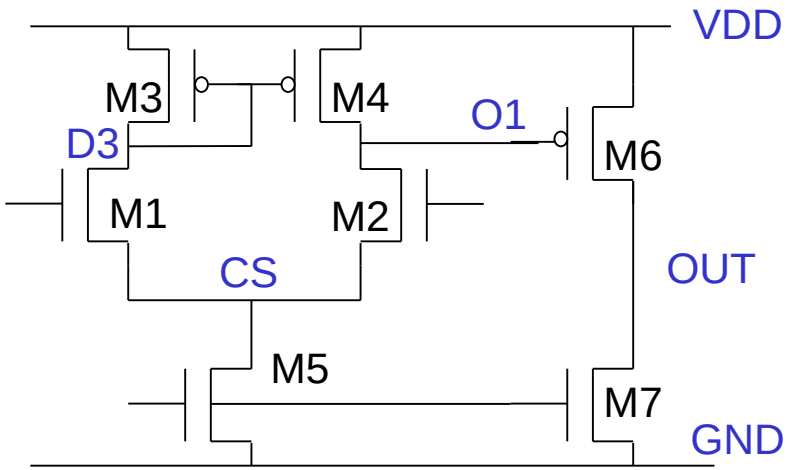




First attempt of interconnections (not completed)

Use of one Metal Layer





Use metal for carrying current!
Poly connections are not a problem (usually)

Stick Layout: Exercise

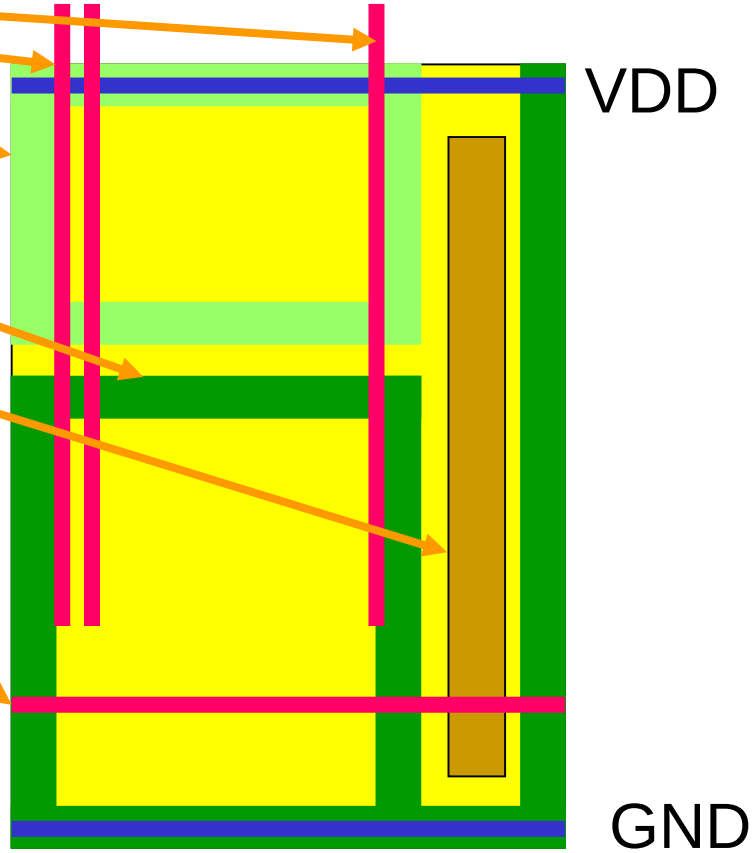
Draw the stick diagram of the two stages OTA in the following three cases:

- fingers of M6 and M7 all together
- M6 =90 M7=60
- M1 and M2 in a common centroid arrangement

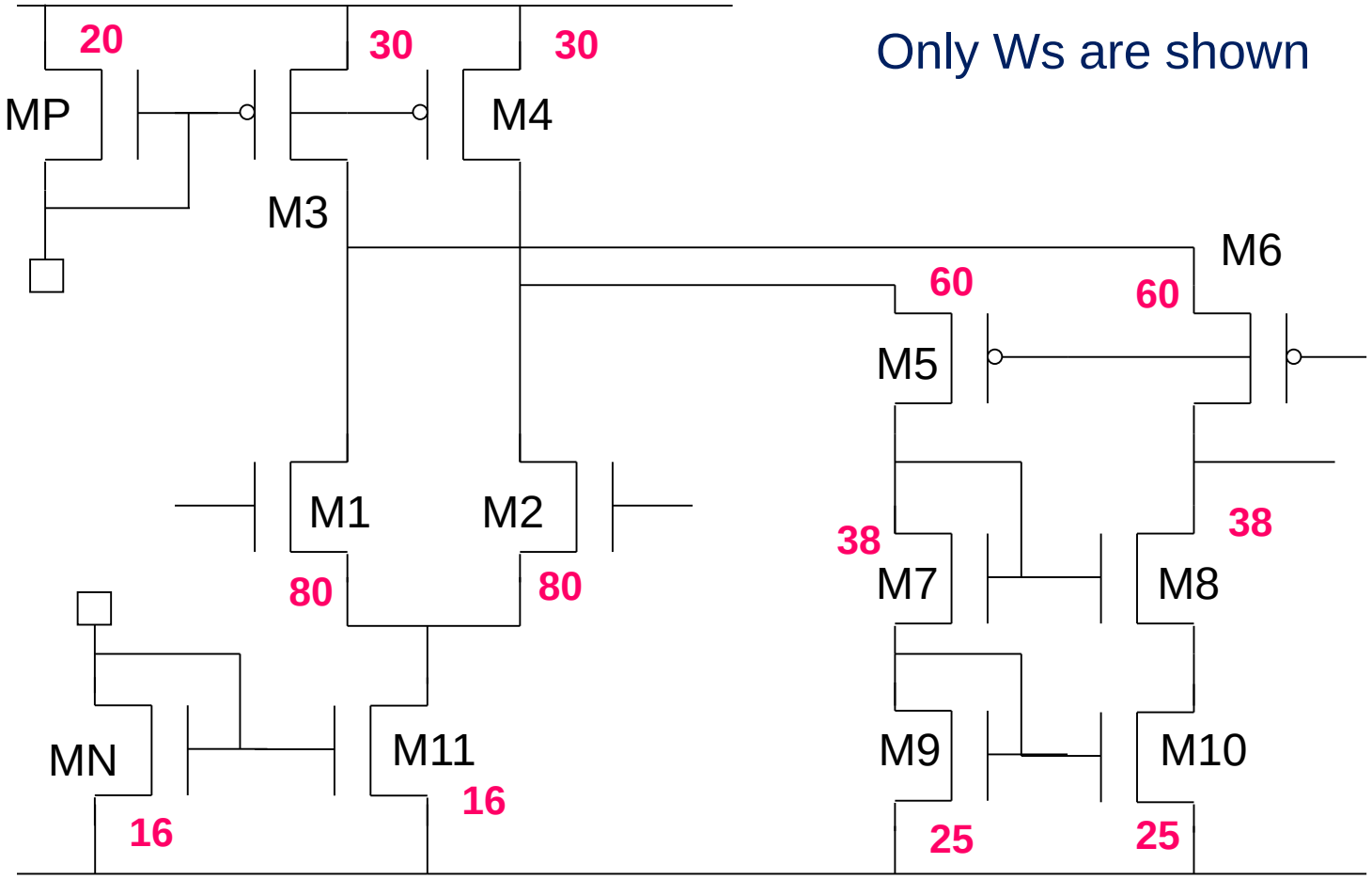
From Stick to Layout

- Input-Output
- Well and its bias
- Substrate bias
- Compensation
- Bias voltage
- Bias current

- Rectangular shape
- System oriented cell layout
  - Related cells with same height
  - Vdd and GND crossing the cell
  - In and Out properly placed

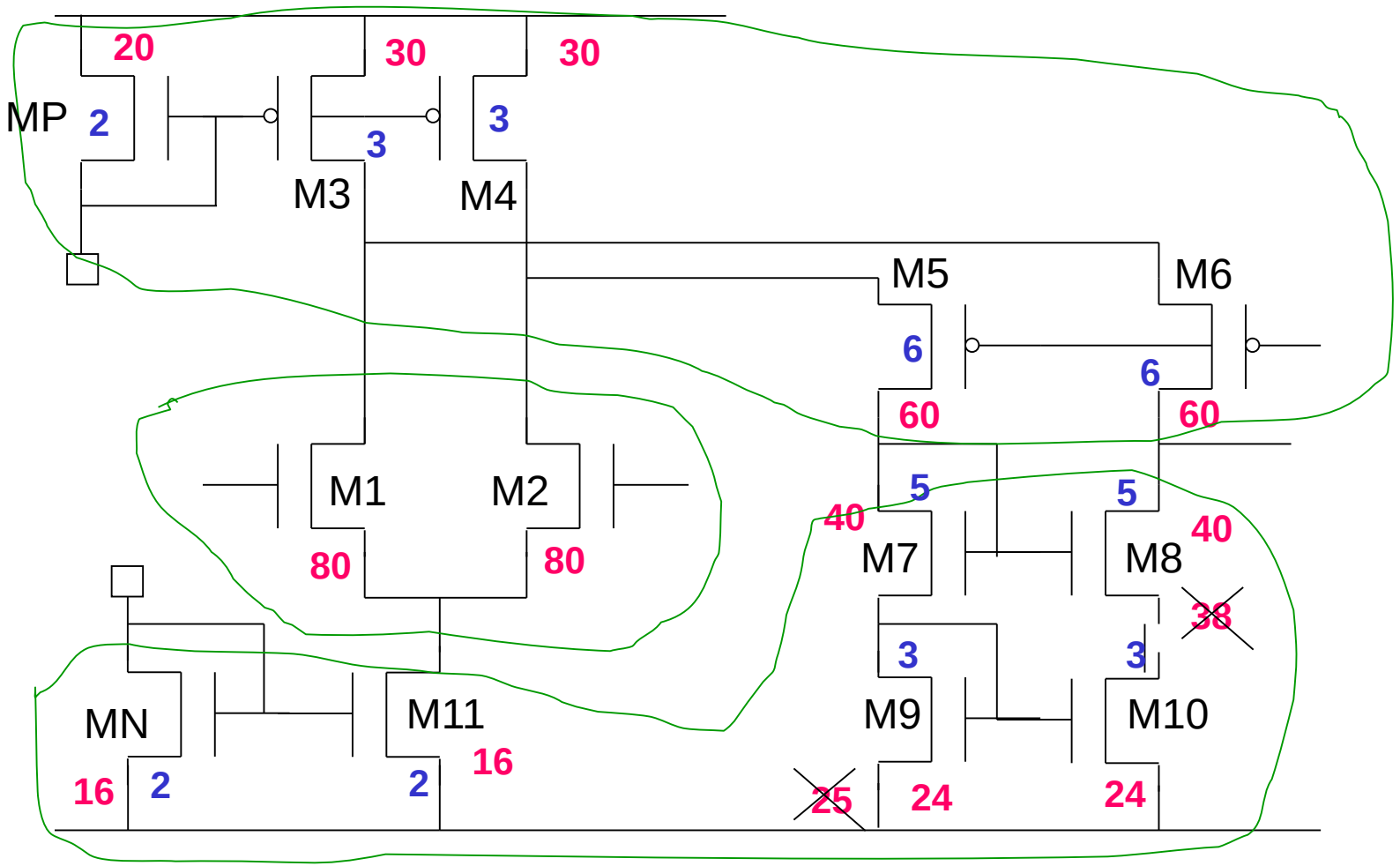


Example 2 (Folded Cascode)

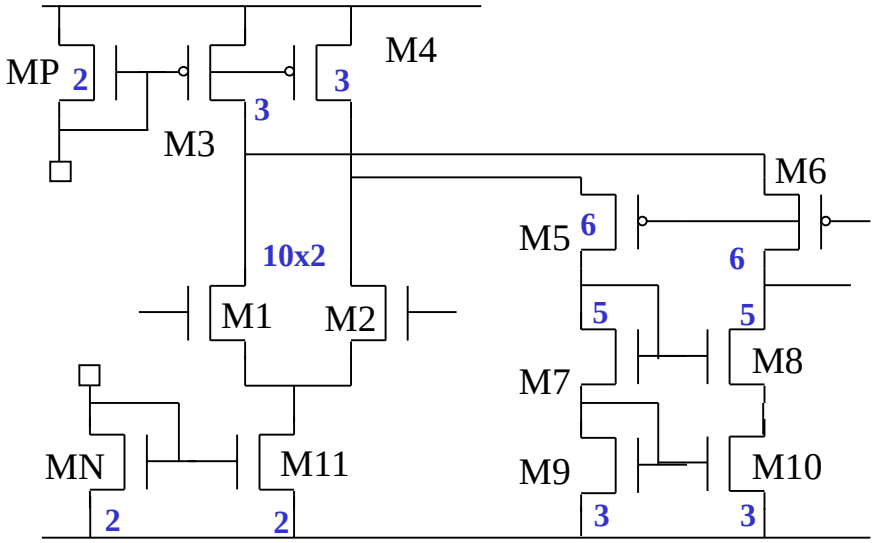


Only Ws are shown

Split of Transistors



Stack Design



555555344PP334666666

1122112211221122122

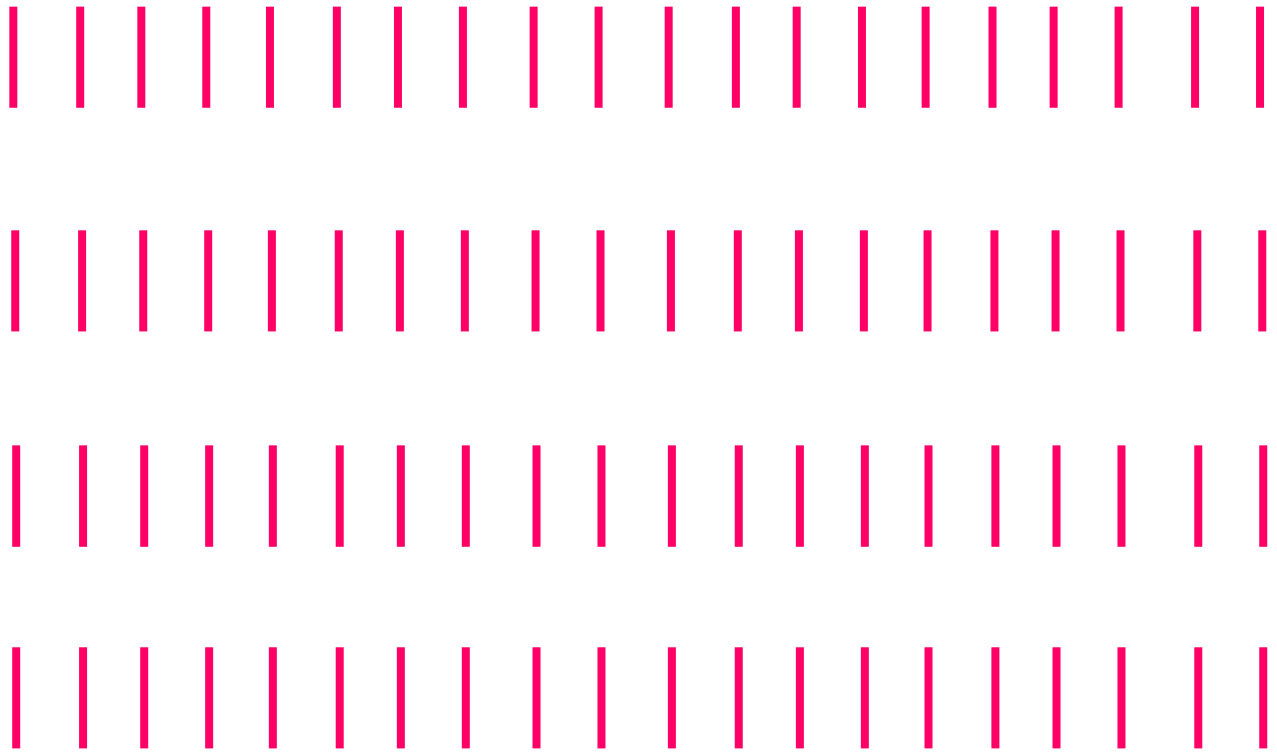
2211221122112211211

777779xxoo99nno88888

X=11; o=10

Interconnection: Exercise

Sketch the source-drain interconnections of the folded-cascode



Basic Cell Design: check-list

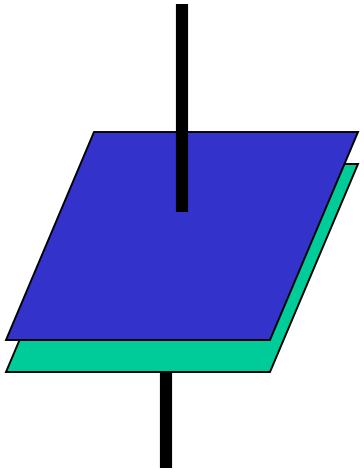
- Draw a well readable transistor diagram
- Identify critical elements and nodes
  - Absolute and relative accuracy
  - Minimum parasitic capacitance
  - Minimum interference
- Mark transistors that must match
- Mark symmetry axes
- Analyze transistor sizing (W's)
- Possibly, change transistor size for a layout oriented strategy
- Group transistors in stacks
- Define the expected height (or width) of the cell
- Sketch the stick diagram
  - transistors of the same type in the same region
- Foresee room for substrate and well biasing
  - substrate bias around the cell
  - well-bias surrounding the well
- Define the connection layer for input-output (horizontal, vertical connections)
- Begin the layout now!!

Outline

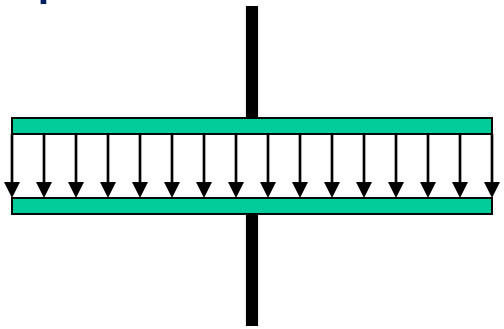
- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout

Integrated Capacitors

Capacitors in IC are parallel plate capacitors



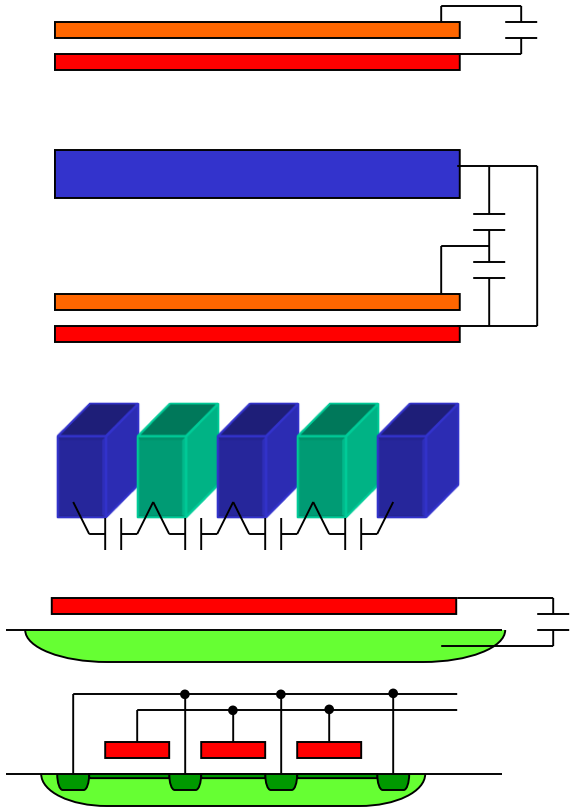
No fringing effect →



$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

Material	Rel. Permittivity	Diel. Strength
SiO_2 Dry Oxide	3.9	11 V/nm
SiO_2 Plasma	4.9	3-6 V/nm
Si_3N_4 LPCVD	6-7	10 V/nm
Si_3N_4 Plasma	6-9	5 V/nm

Types of Integrated Capacitors



Poly-poly

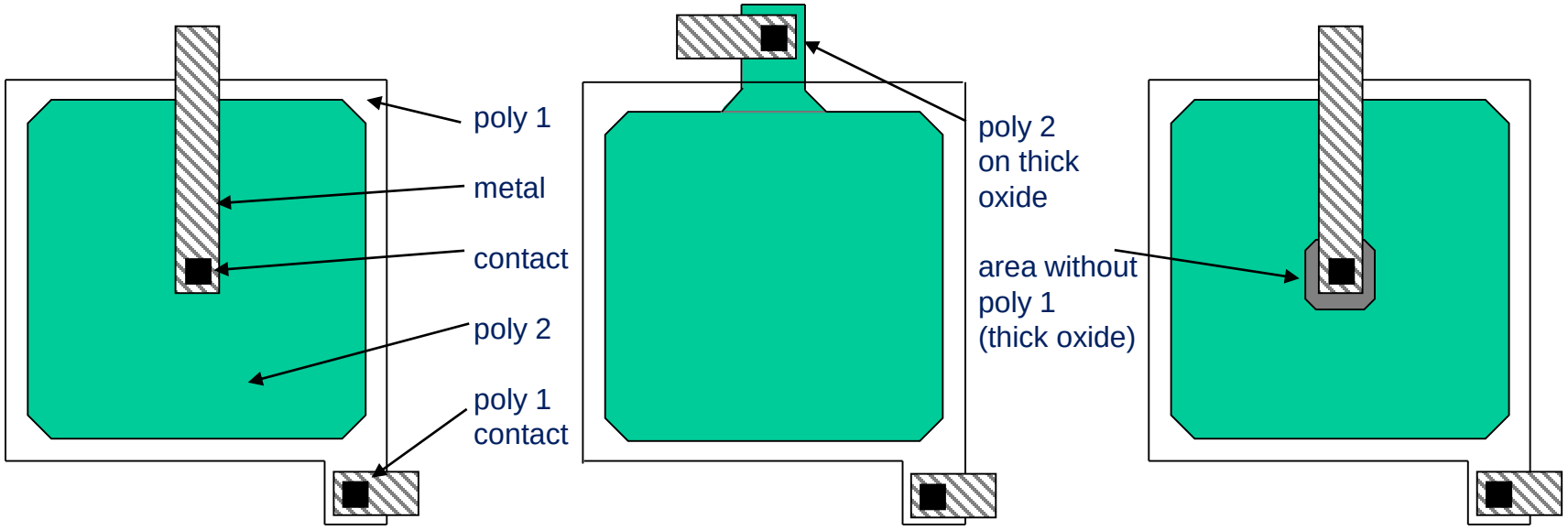
Sandwich

Lateral plates
(flux capacitor)

Poly- diffusion

Poly-channel

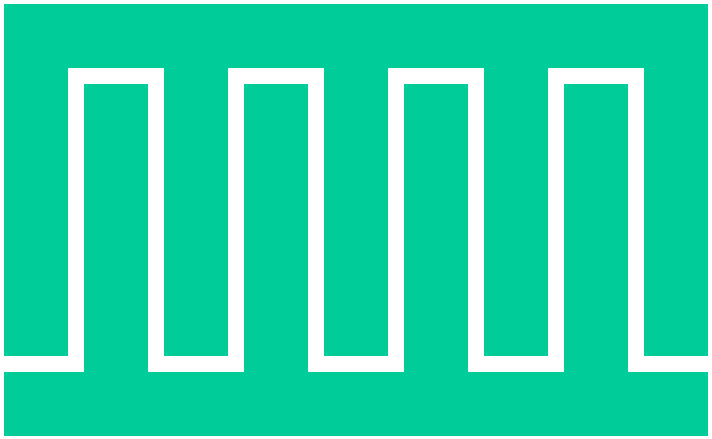
Layout of Capacitors



To achieve good matching :

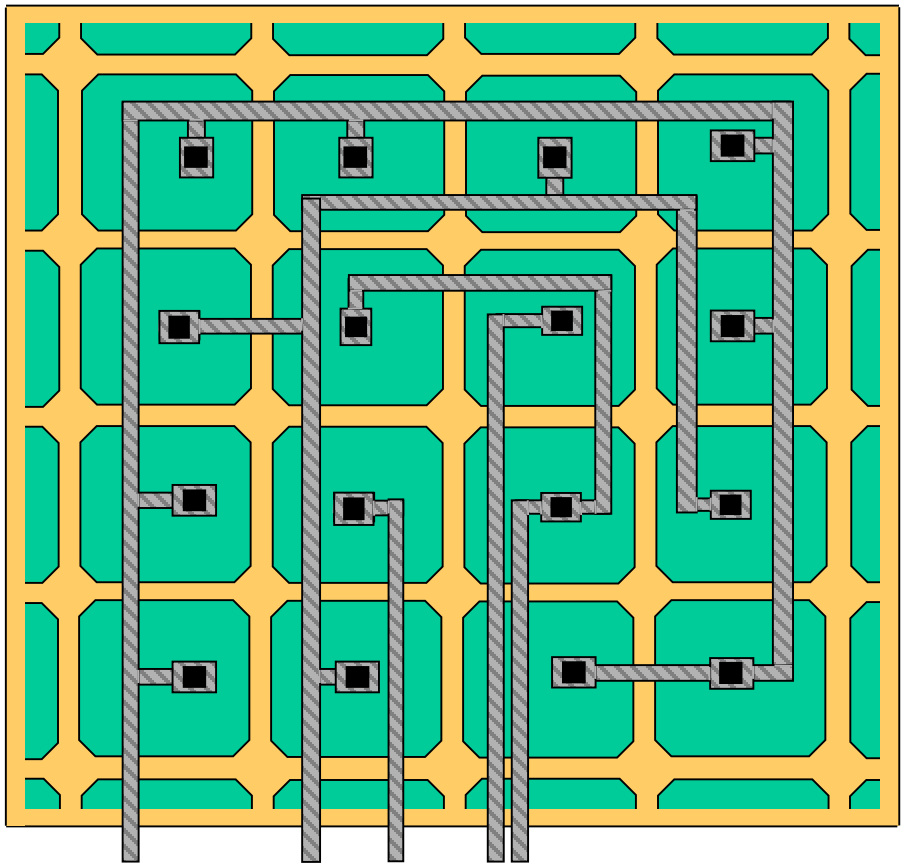
- Use of unity capacitors connected in parallel
- Use W = L fairly large

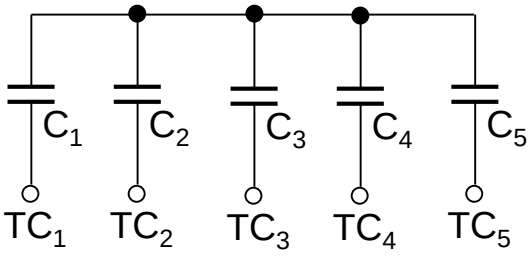
Flux Capacitor Layout



- Use of the same metal layer
- Exploit the lateral flux
- The parasitic capacitance plate -substrate is low because the metal sits on thick oxide
- Use thick metal layers
- Maximize the perimeter (use of fractals)
- Very good matching!

Common Centroid Structures

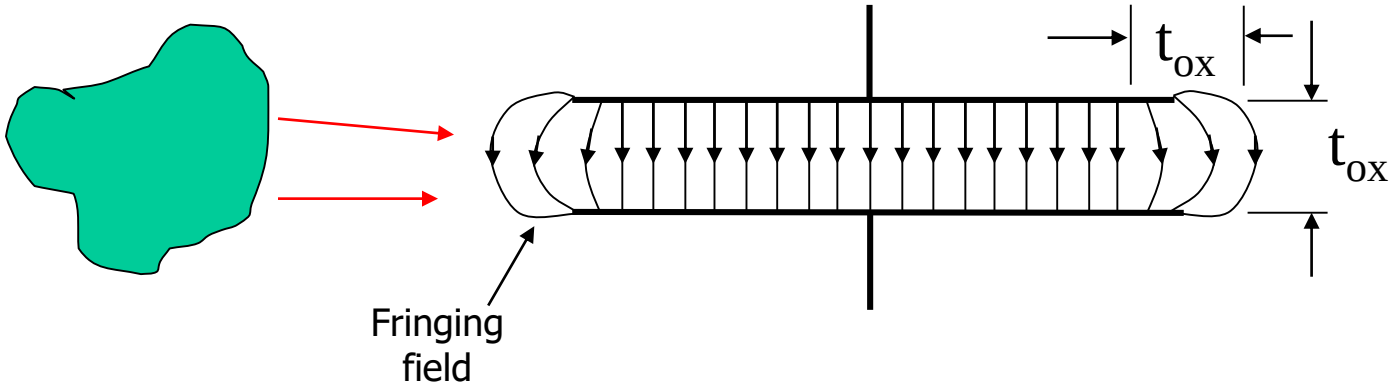




$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

Fringing Effect

- Equation $C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$ is an approximation



$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} (W - t_{ox})(L - t_{ox}) + C_{fring}$$

- Fringing depends on the boundary conditions

MOS Capacitors Features

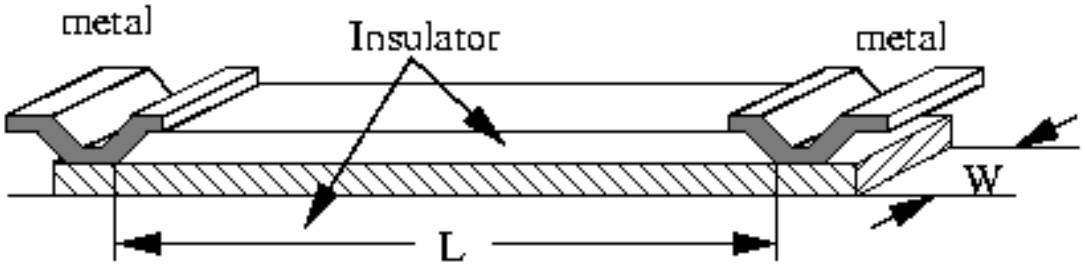
Type	t_{ox} nm	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
poly - diff.	15 - 20	7 - 14	20 - 50	60 - 300
poly I - poly II	15 -25	6 - 12	20 - 50	40 - 200
metal - poly	500 - 700	6 - 12	50 - 100	40 - 200
metal - diff.	1200 - 1400	6 - 12	50 - 100	60 - 300
metal I - metal II	800 - 1200	6 - 12	50 - 100	40 – 200

Rules for Capacitor Matching

- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections' contribution
- Don't run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices

Integrated Resistor Cross-section

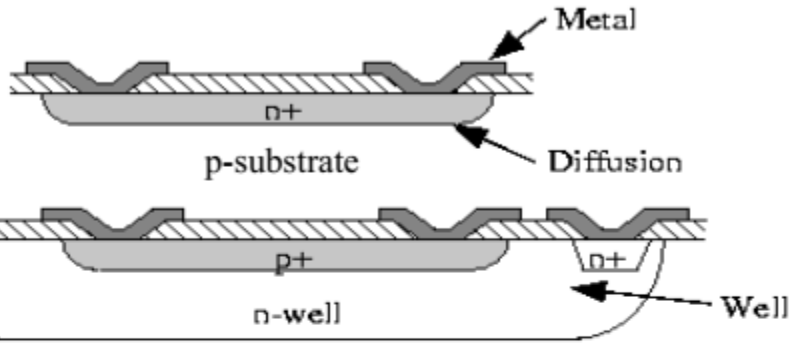
- A resistor is made of a strip of resistive layer.



$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$

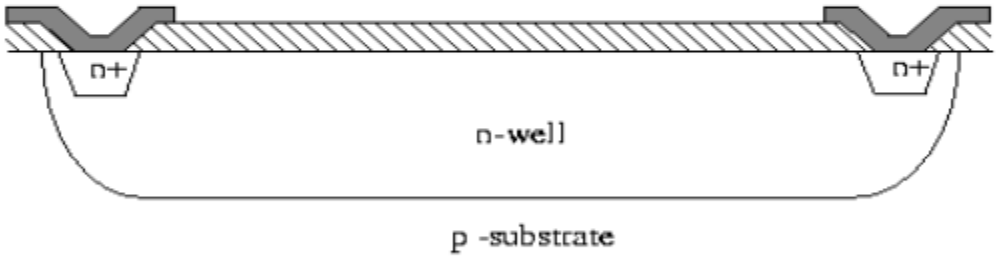
- The endings resistance can be significant!

Diffusion/Well Resistors

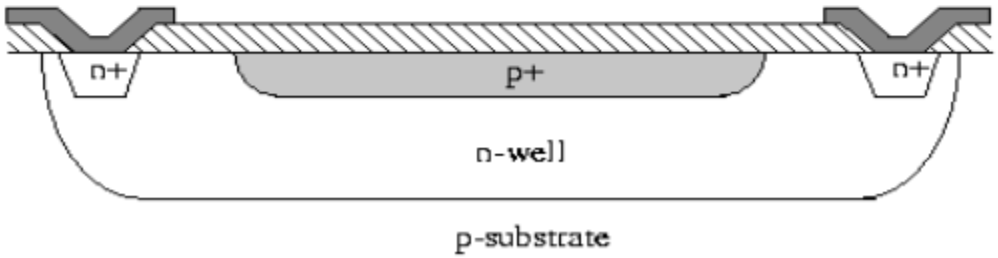


Diffused resistance

Diffused resistance

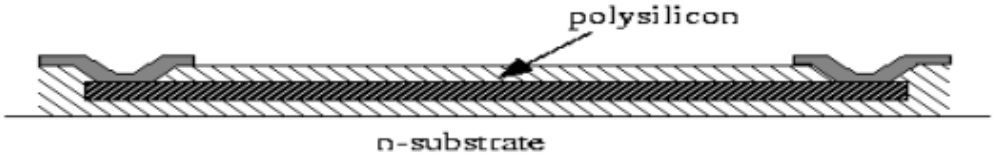


well resistance

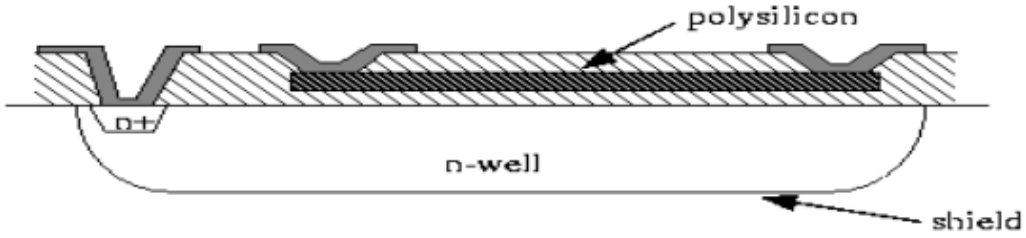


Pinched n-well resistance

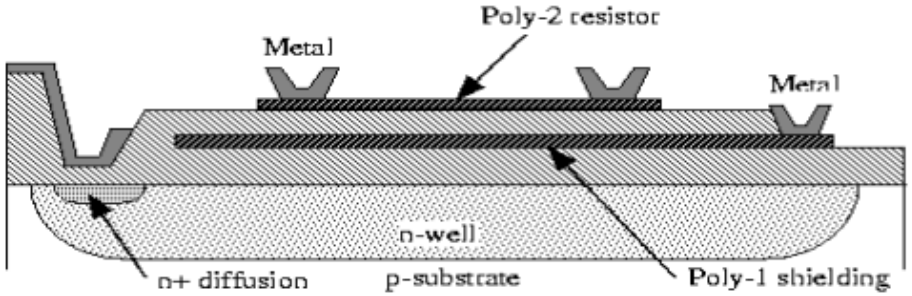
Polysilicon Resistances



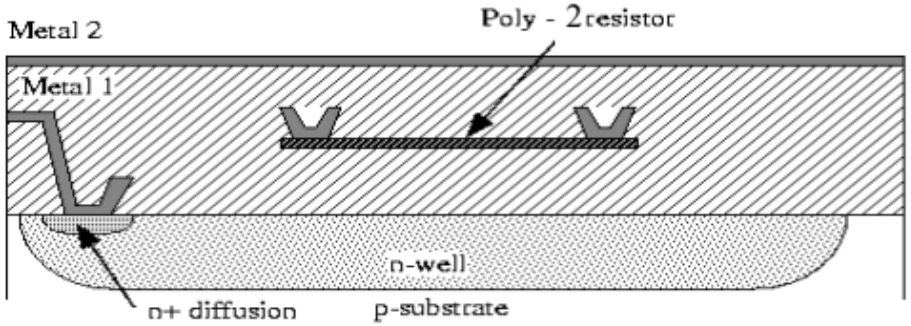
e) First polysilicon resistance



f) First polysilicon resistance with a well shielding



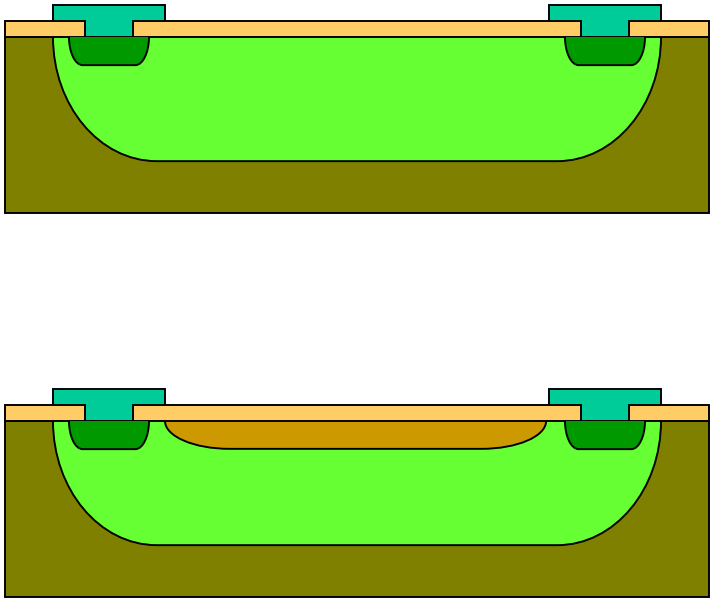
g) Second polysilicon resistance



h) Second polysilicon resistance with a well shielding

Conductive layers can be used to shield the conductor-oxide-conductor structure

Well or Pinched-well Resistors



- Well layers have a large specific resistance

but

- They have a large voltage and temperature coefficient
- They are weakly insulated from the surrounding

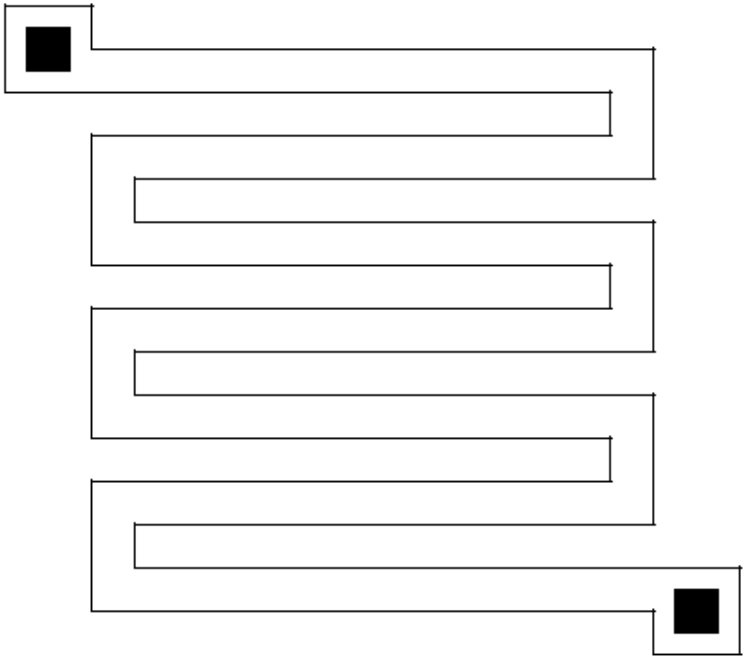
- Layers close to the surface contribute to the conductivity

Large Value Resistors

In order to have large value resistors :

- Use of long strips (large L/W)
- Use of layers with high sheet resistance (bad performances)

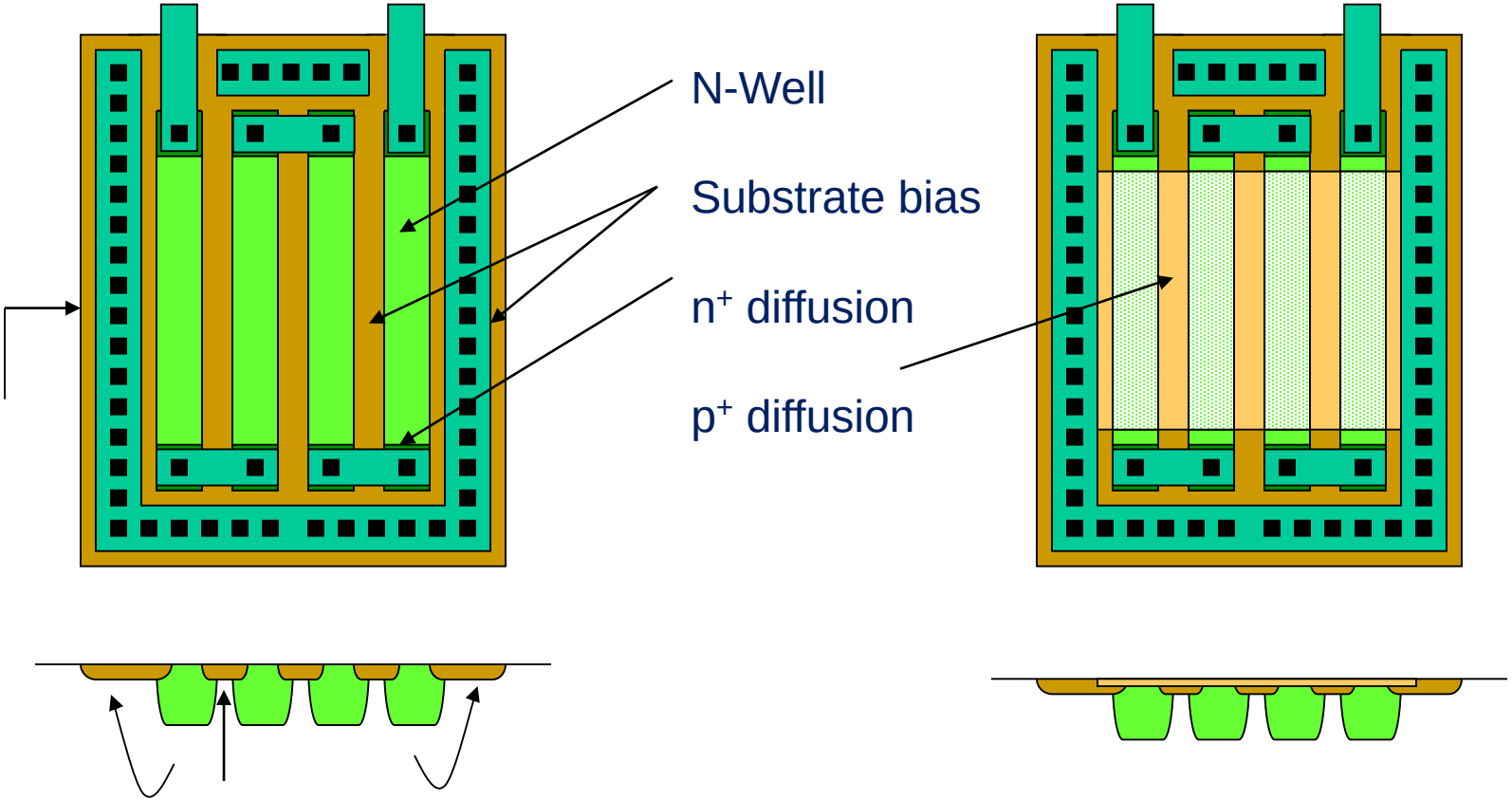
Layout : rectangular “snake”



(!!)
Resistance at the corners
Current flows in different directions

DON’T USE IT IN PRECISE APPLICATIONS!

Prevent Current Leakage!



Features of Resistors

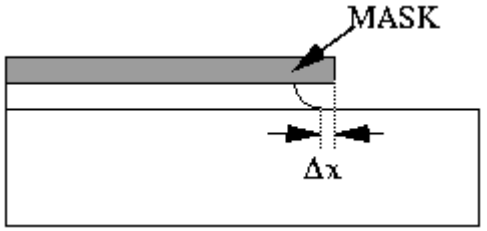
Type of layer	Sheet Resistance Ω/□	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Effect of Etching

Wet etching : isotropic (undercut effect)

H_F for SiO_2 ; H_3PO_4 for Al

Δx for polysilicon may be 0.35 - 0.5 μ with standard deviation 0.02 μ.



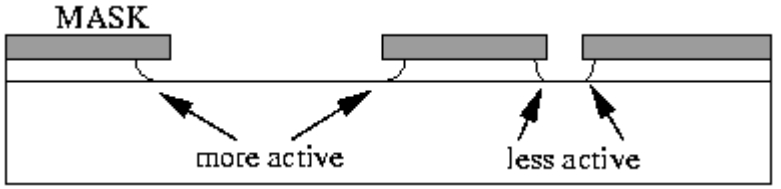
Reactive ion etching (R.I.E.)(plasma etching associated to “bombardment”) : unisotropic.

Δx for polysilicon is 0.2 μ with standard deviation 0.015 μ

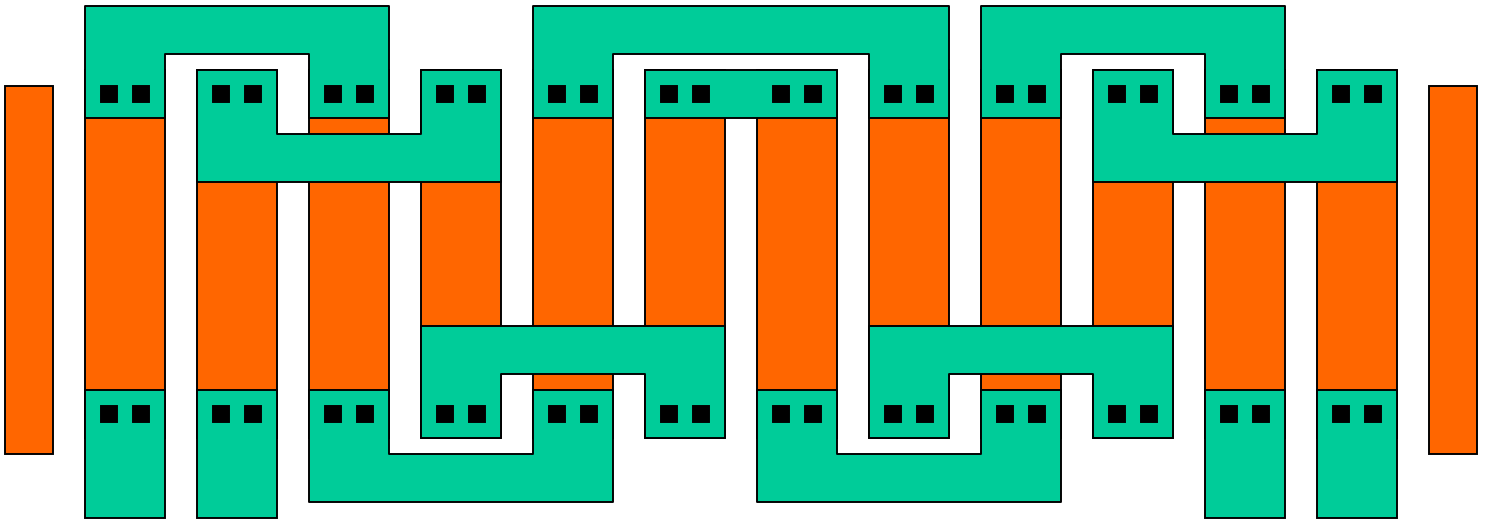
Boundary :

The etching depends on the boundary conditions

Use of dummy strips



Interdigitized and Common Centroid

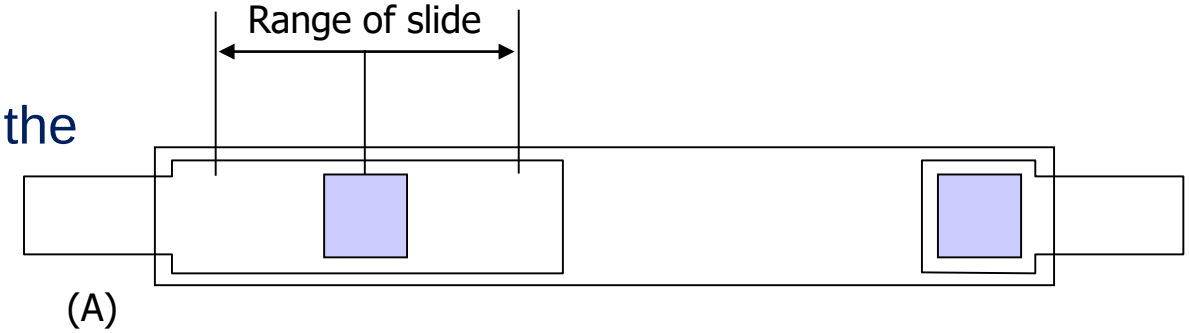


121212212121

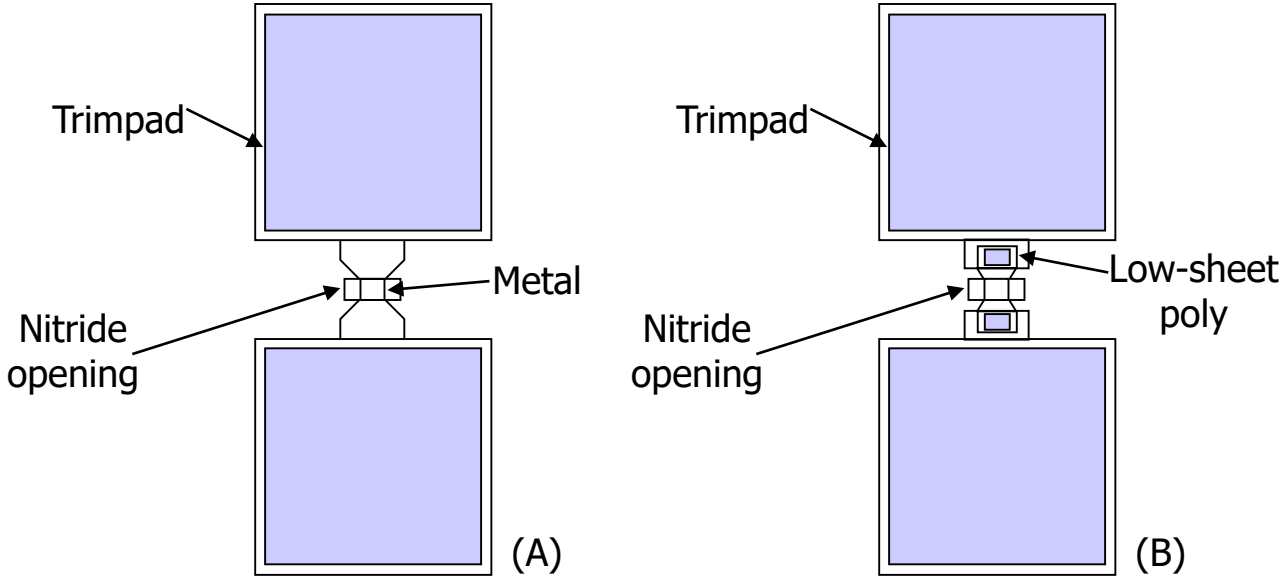
Exercise: draw a 121212121212 connection and compare the two solutions
Exercise: draw a common centroid structure (12 elements per resistor)

Adjusting Resistor Values

Sliding contact:
requires to change the
contact mask only



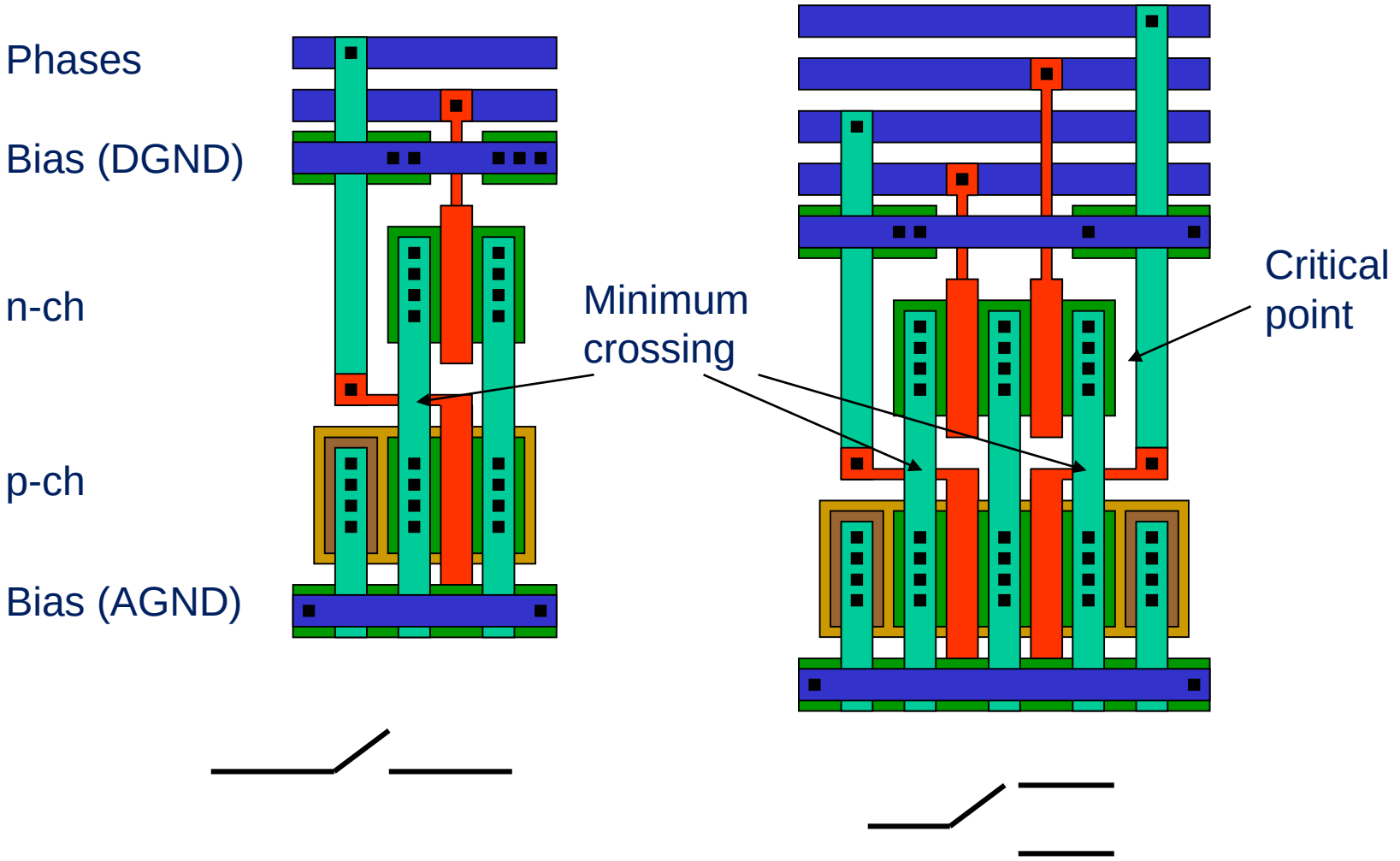
Metal fuse
and
Poly-fuse



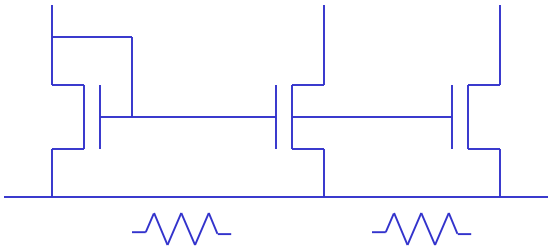
Outline

- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout

Layout of Switches

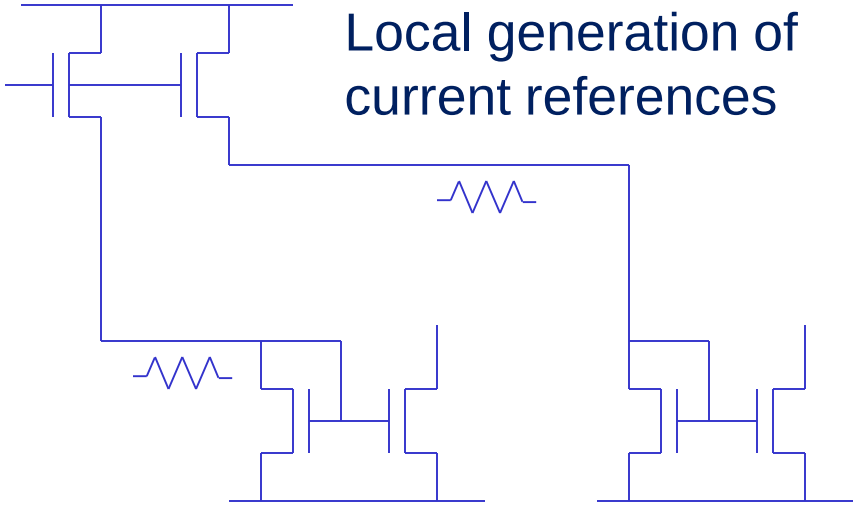


Reference Current Distribution



V_{GS} voltage distribution

Drop voltage on the “ground” connection

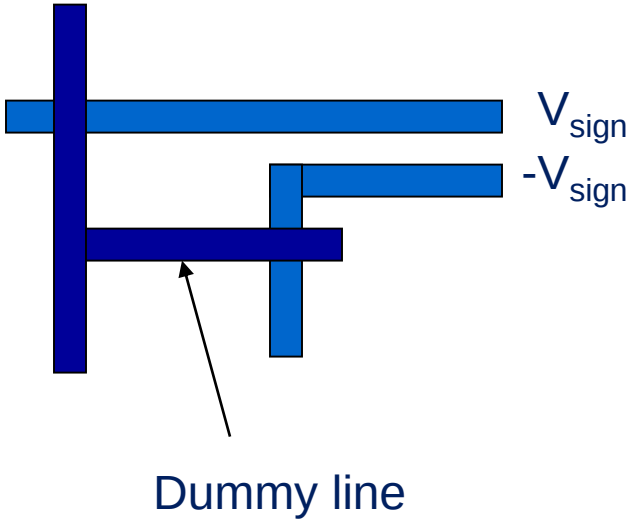


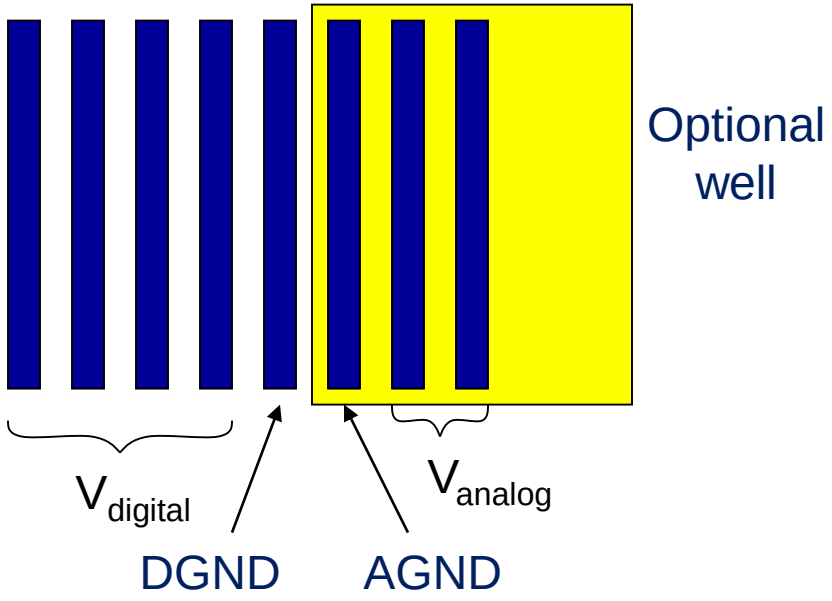
Reference currents distribution

Drop voltage on the wire connection

Cross-talk and Shielding

- Crossing of metal lines carrying analog and digital signals cause cross-talk between signals.
  - ✶ Make disturbances differential
  - ✶ Use shielding lines in mixed signal busses





Switched Capacitor Circuits

- **Floor plan of a SC circuit**
  - Single ended circuits
  - Fully differential circuits
  - Respect symmetries
  - Wide supply routes
  - Separation between analog and digital

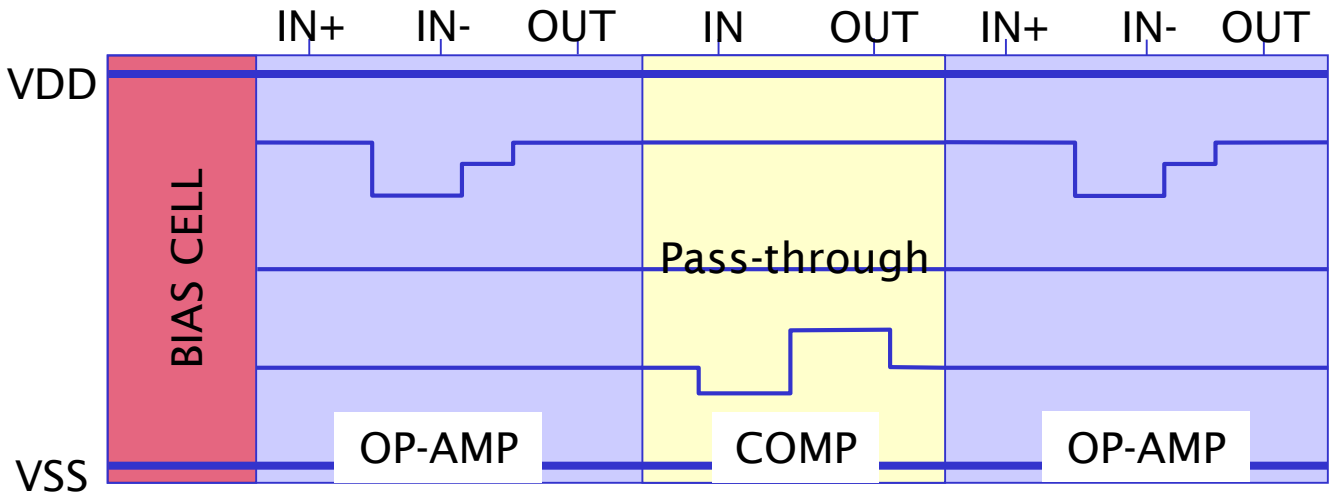
Standard Cell like Approach

Cells with the same width and different length

V_{DD} and V_{SS} on the top and bottom

Input and output on the two sides

- Layout of basic blocks Standard cell oriented



Single-ended SC Floor Plan

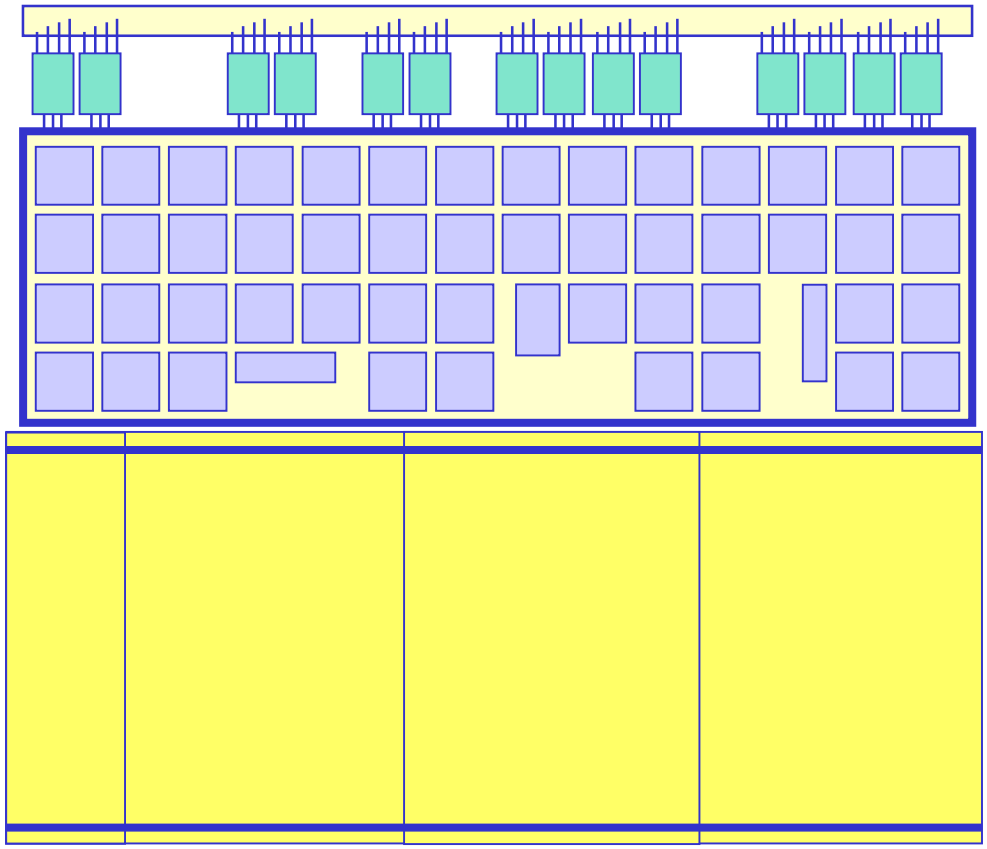
Clock phases
Switches

Capacitor array
Underneath well
Substrate bias around

Analog bus

Analog cells

Analog bus



Fully-Diferential SC Floor Plan

Clock phases
Switches

Capacitor array

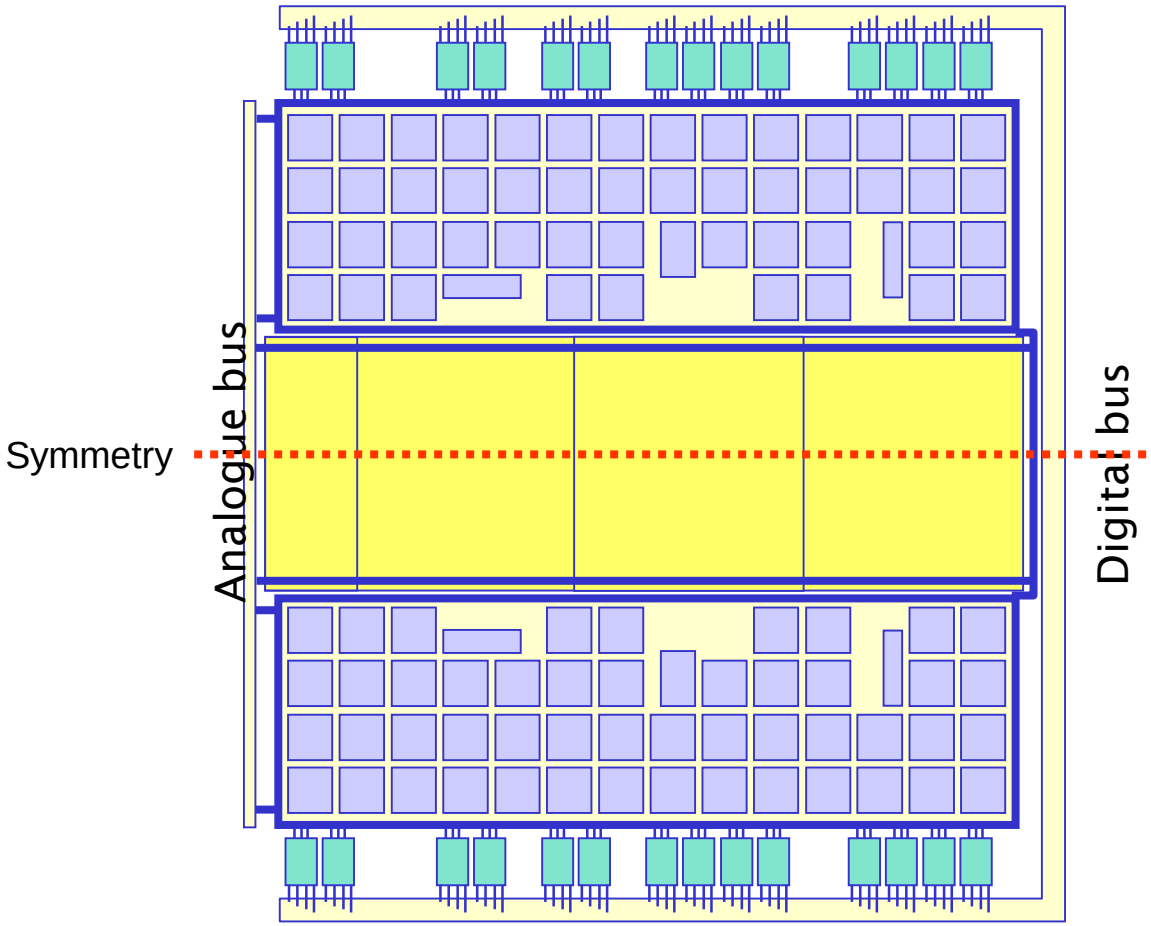
Analog bus

Analog cells

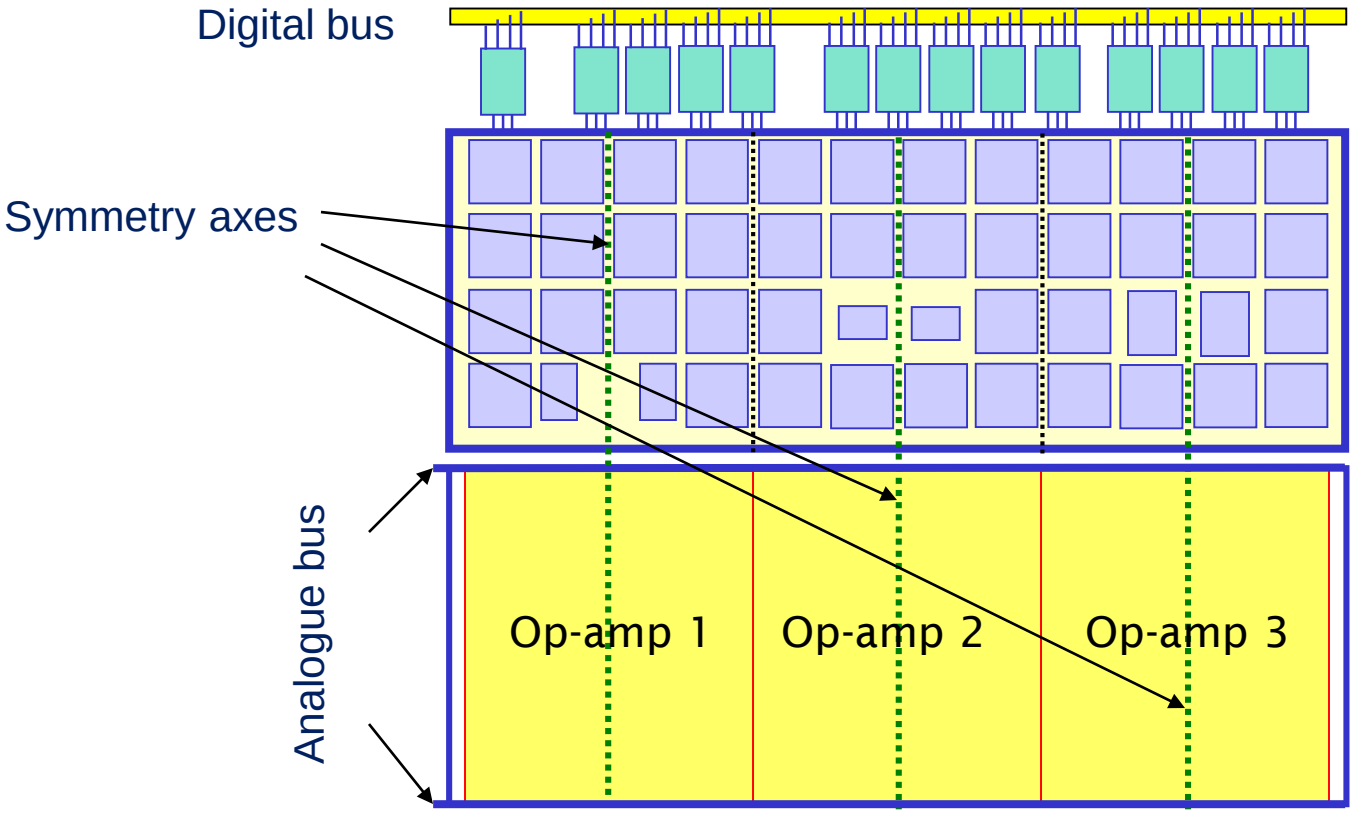
Analog bus

Capacitor array

Switches
Clock phases



Fully-Diferential SC Floor Plan (2)

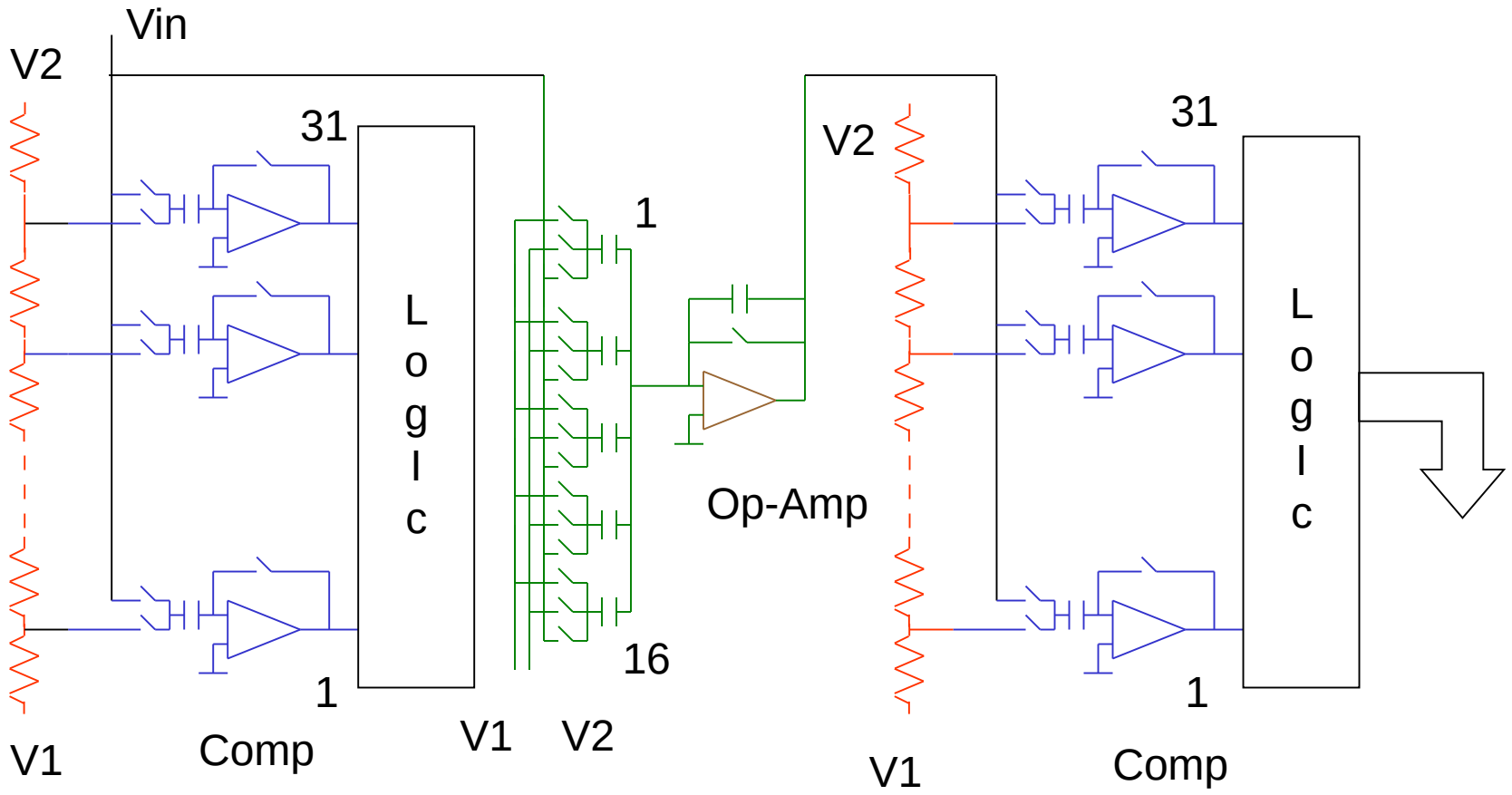


Analog Floor-plan

- List of active cells: op-amp, comparators, biases
- Area estimation (interconnection/biasing area ~ 50%)
- List of passive components & switches
  - ✶ accuracy requests and shielding needs
  - ✶ Matching of resistors/capacitors
- Estimate the silicon area
- Define the aspect ratio of the analog section
- Placement of active cells
- Placement of passive components
- Placement of switches

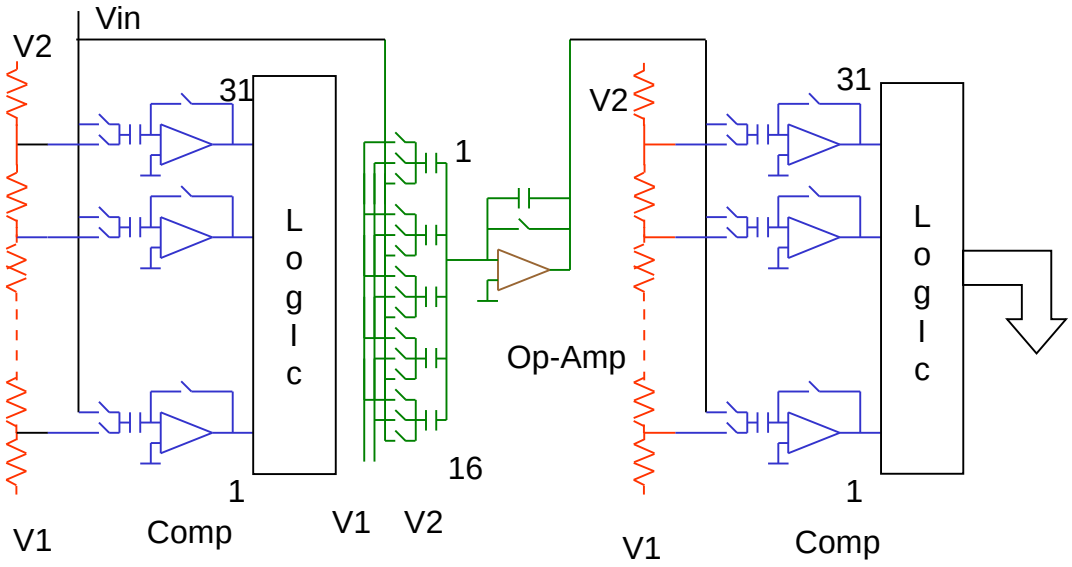
Analog Floor-plan: Example

10-bit two-step flash converter



Analog Floor-plan: Example (2)

10-bit two-step flash converter



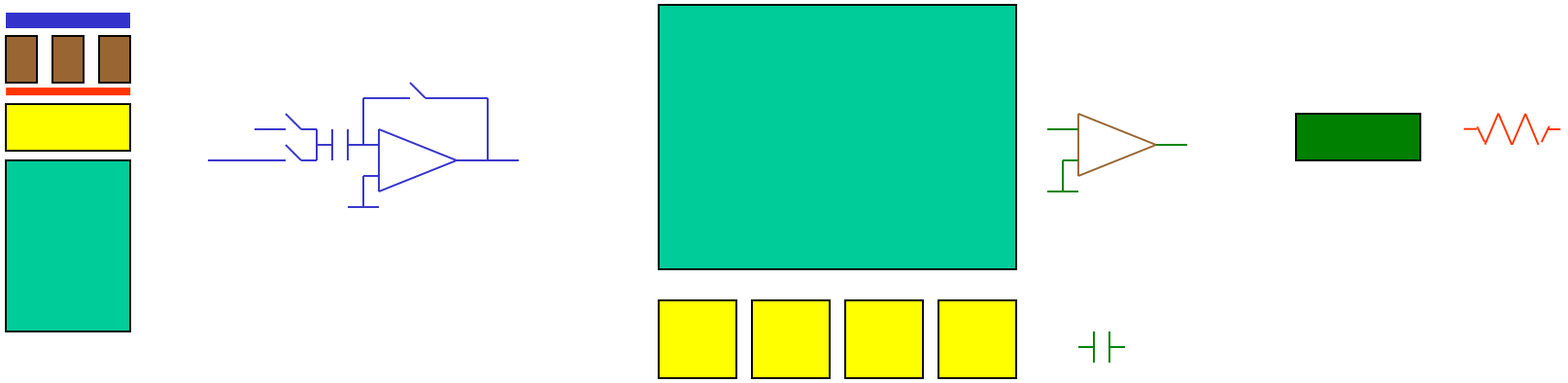
62 Comparators
1 Op-amp

62 autozero nets
2 Res. String (32)
1 Cap. Array 32

2 Logic

Analog Floor-plan: Example (3)

10-bit two-step flash converter



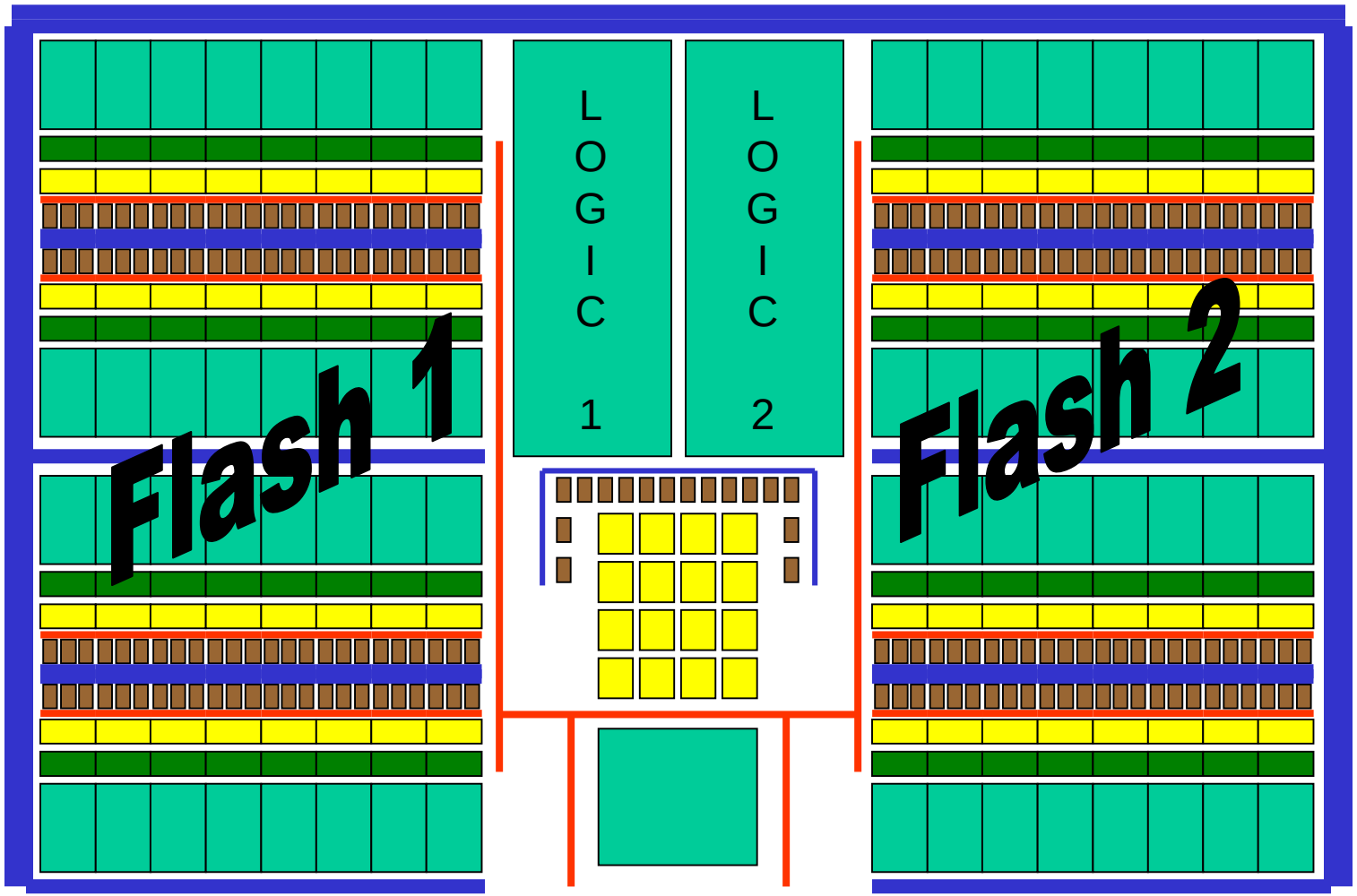
62 Comparators
1 Op-amp

62 autozero nets
2 Res. String (32)
1 Cap. Array 32

2 Logic

Logic (shape is flexible)

Analog Floor-plan: Example (3)



Digital

Analog

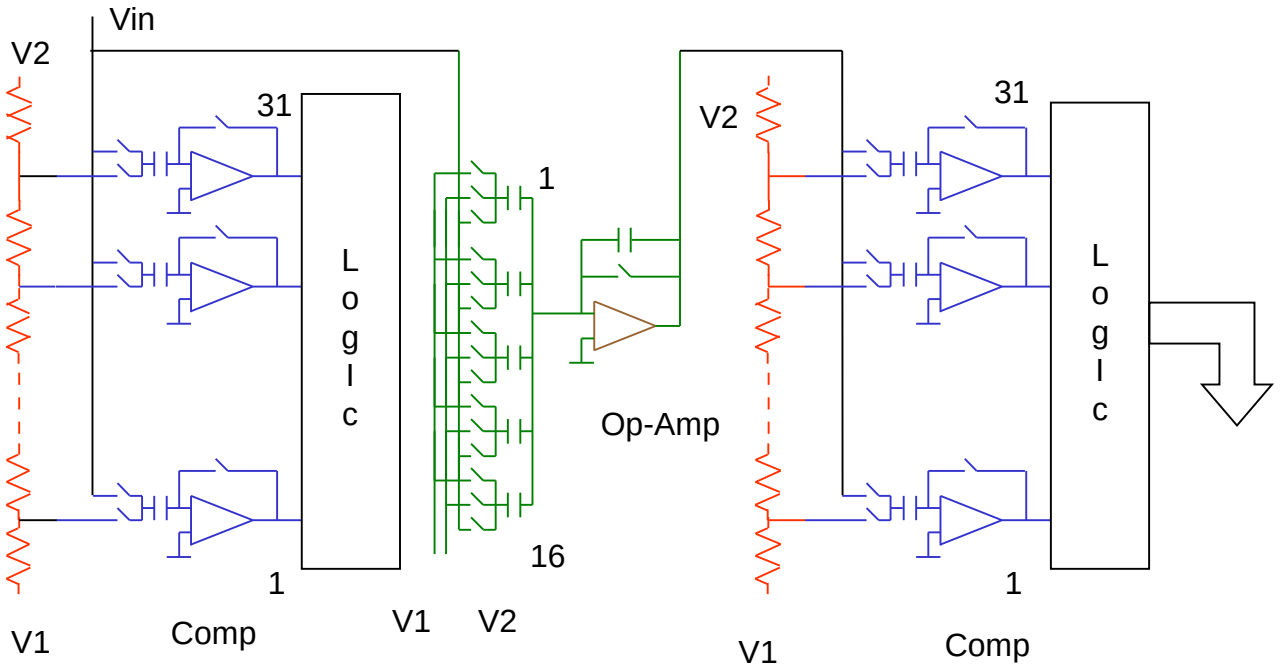
Problem:

resistor matching

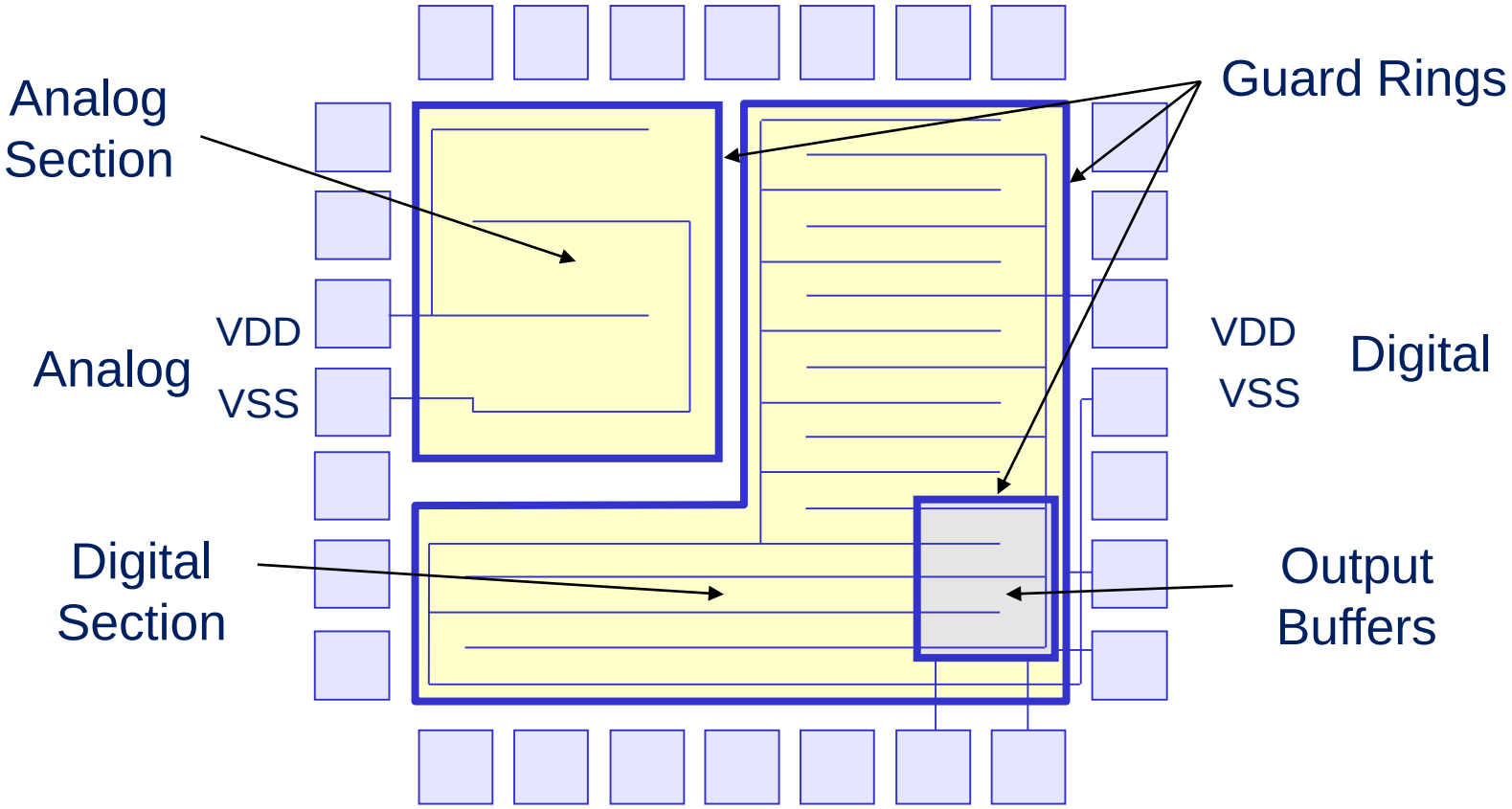
use shunting elements

Analog Floor-plan: Exercise

Sketch a new floor-plan of the 10 bit two-step flash. The goal is to have a good integral non-linearity (the resistor strings used in the previous slide are affected by a large gradient error.



Mixed-signal floor-plan



Mixed-signal Layout: check-list

- Draw a well readable system diagram
- Identify critical blocks and connections
  - ✶ sensitive nodes
  - ✶ critical paths
- Mark passive components that must match
- Mark symmetry axes
- Roughly estimate area of active cells
- Roughly estimate area of passive elements

- Study a possible placement and change the aspect ration of basic cells accordingly
- Define the analog and digital routing path
- Begin the layout of the basic cells now!!
- Change the Floor plan of the system in feedback
- Place plenty of guard rings

- Fill all the empty spaces with substrate bias