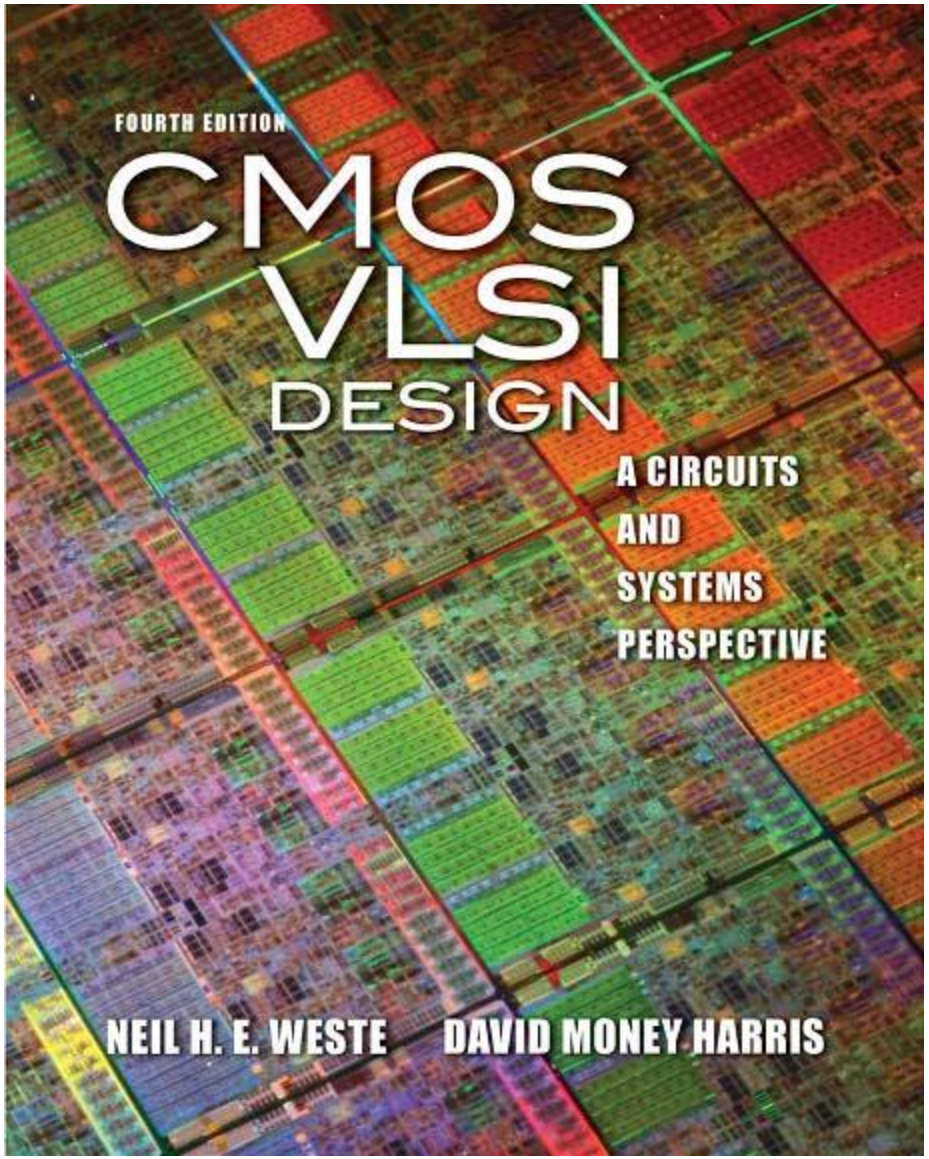


Lecture 1: Introduction

Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI):
  - How to design VLSI systems
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

https://en.wikipedia.org/wiki/Transistor_count

Processor	Transistor count	Date of introduction	Designer	Process	Area
10-core Core i7 Broadwell-E	3,200,000,000[34]	2016	Intel	14 nm	246 mm²
POWER9	8,000,000,000	2017	IBM	14 nm	695 mm²
IBM z14 Storage Controller	9,700,000,000	2017	IBM	14 nm	696 mm²
IBM z14	6,100,000,000	2017	IBM	14 nm	696 mm²
Centriq 2400	18,000,000,000	2017	Qualcomm	10 nm	398 mm²
Apple A11 Bionic (hexa-core ARM64 "mobile SoC")	4,300,000,000	2017	Apple	10 nm	89 mm²
8-core Ryzen	4,800,000,000	2017	AMD	14 nm	192 mm²
32-core AMD Epyc	19,200,000,000	2017	AMD	14 nm	768 mm² (4 x 192 mm²)
Apple A12 (hexa-core ARM64 "mobile SoC")	6,900,000,000	2018	Apple	7 nm	

What does it take to design VLSI systems?

1. idea (need)

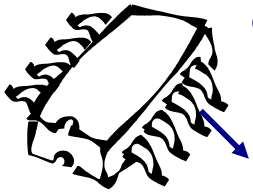
2. write specifications

3. design system

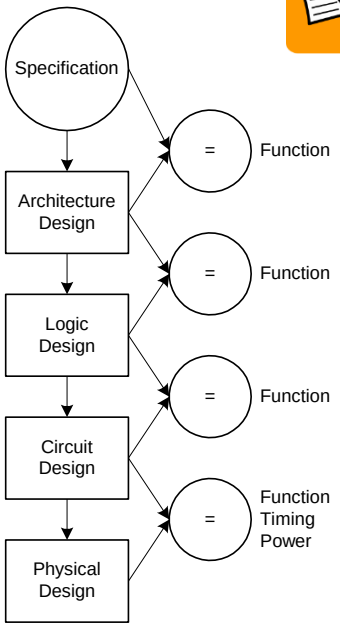
4. analyze/ model system

if satisfactory

5. Fabrication

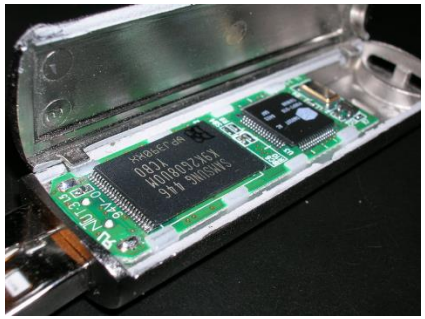


6. test / work as modeled?



Same engineering principles you learned so far

1. Applications / Ideas



2. Specifications

- Instruction set
- Interface (I/O pins)
- Organization of the system
- Functionality of each unit and how it to communicate to other unit

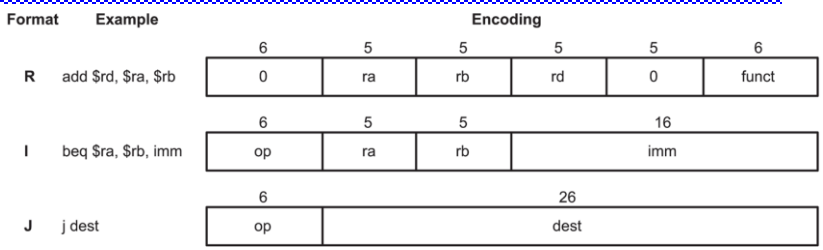
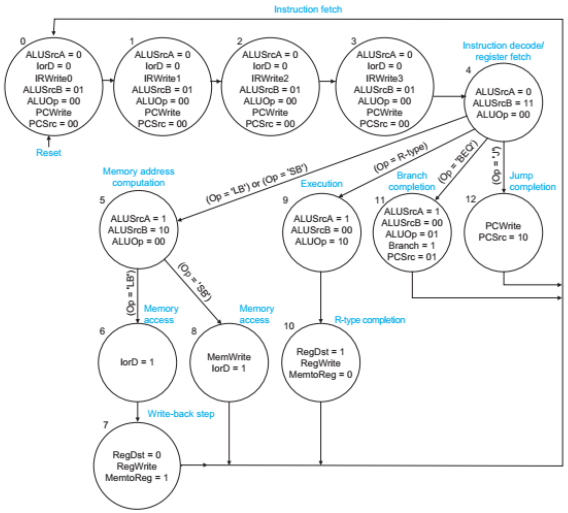


FIG 1.49 Instruction encoding formats



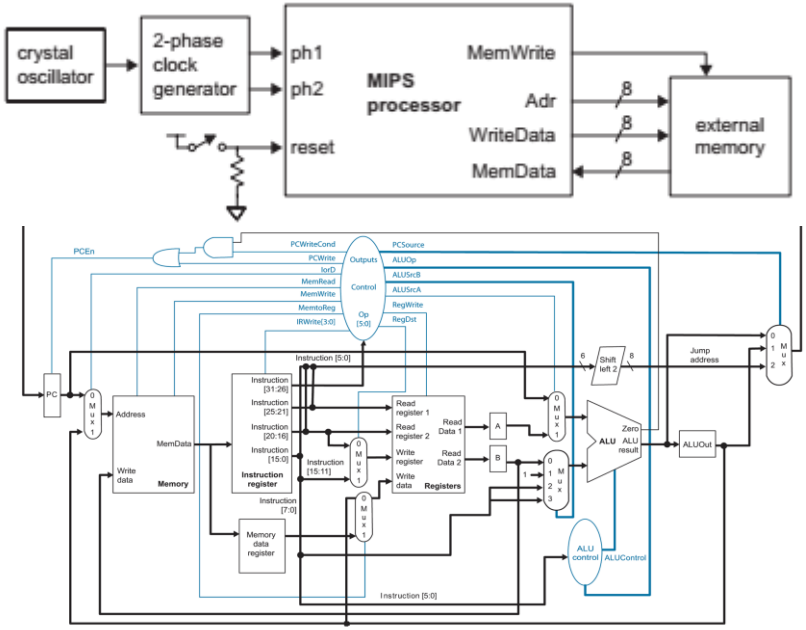
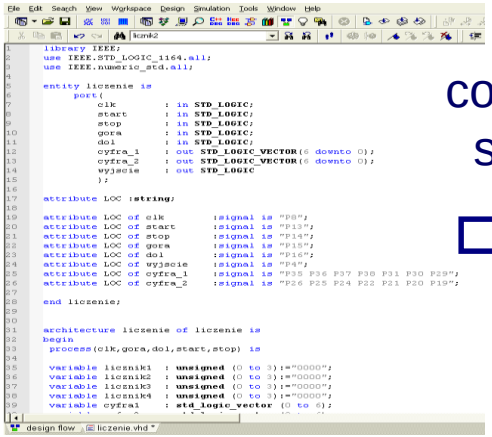


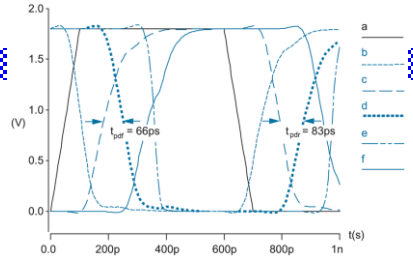
FIG 1.53 Multicycle MIPS microarchitecture. Reprinted from [Patterson04] with permission from Elsevier.

3/4. Design and Analysis

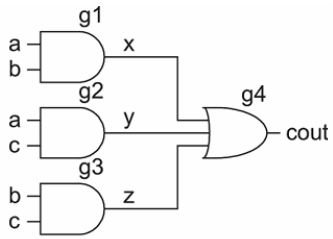
VHDL / Verilog / SystemC

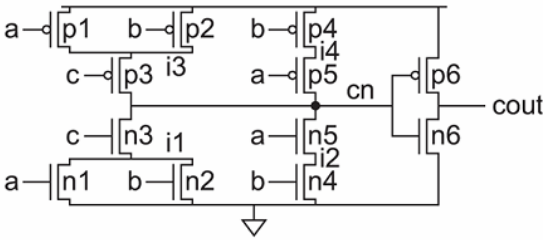


compilation/
synthesis



design schematics

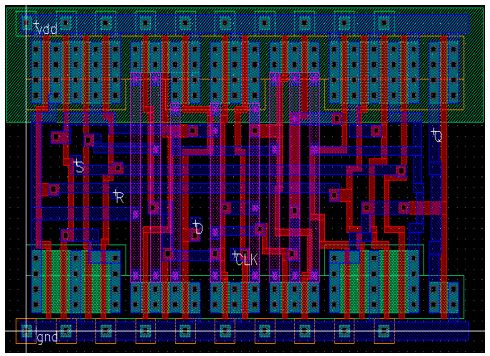


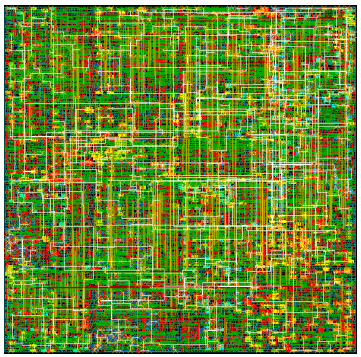


mask layout patterns

find wire routes

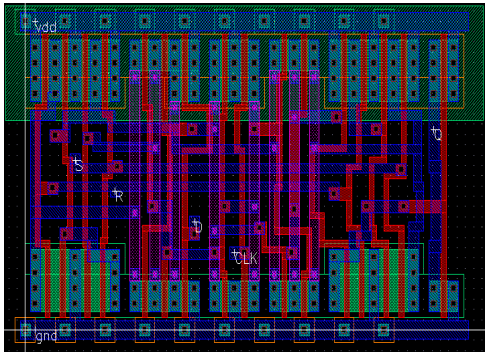
device layout





- Design development is facilitated using Computer-Aided Design (CAD) tools

5. Fabrication

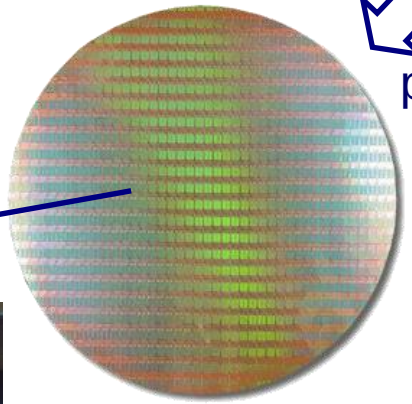


mask layout patterns

tapeout

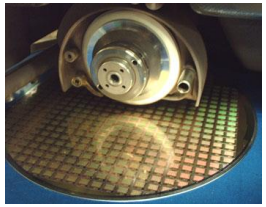
mask writer

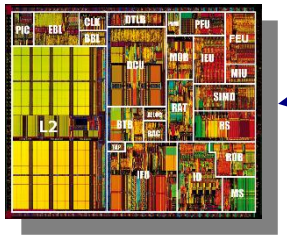
printing



wafer

dice





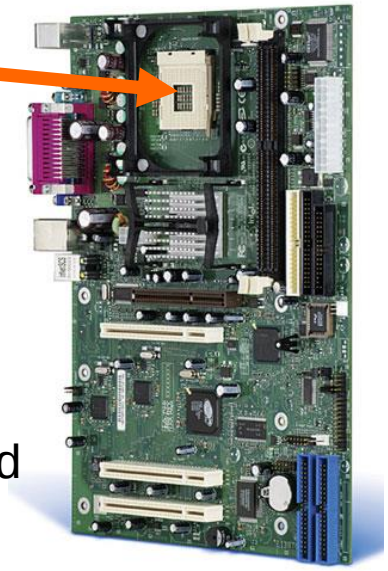
die

test and packaging

chip

6. Evaluate design and compare to model

- Check signal integrity
- Power consumption
- Input/output behavior

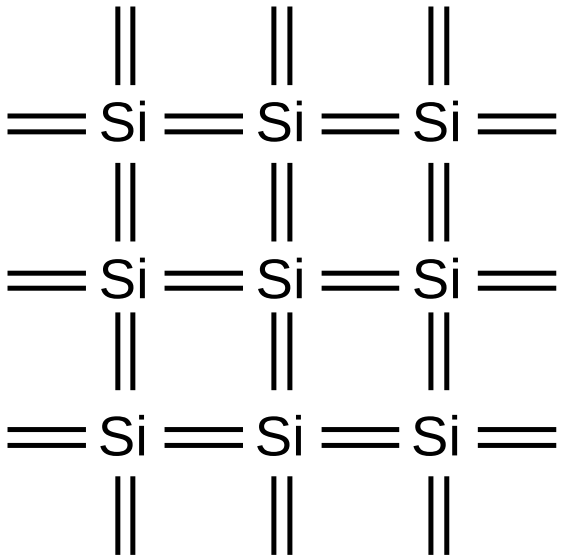


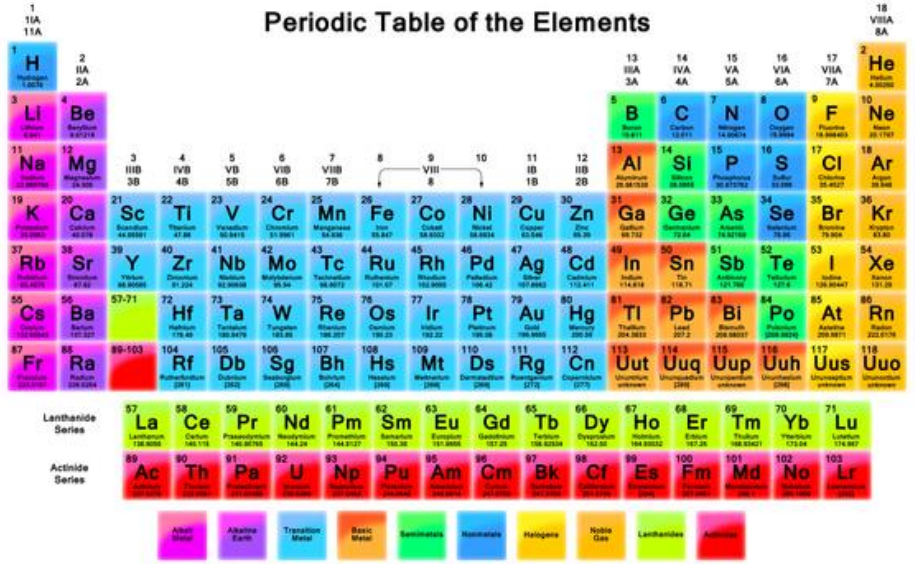
board

- Does the chip function as it is supposed to be?
- Does it work at desired clock frequency? (can we overclock?)

Silicon Lattice

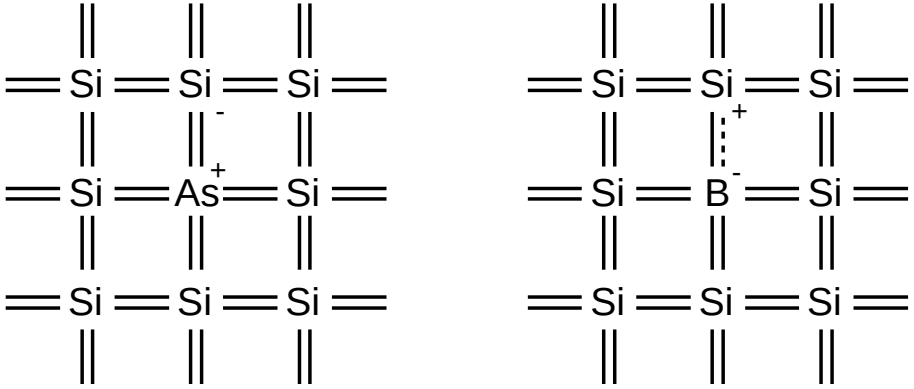
- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors





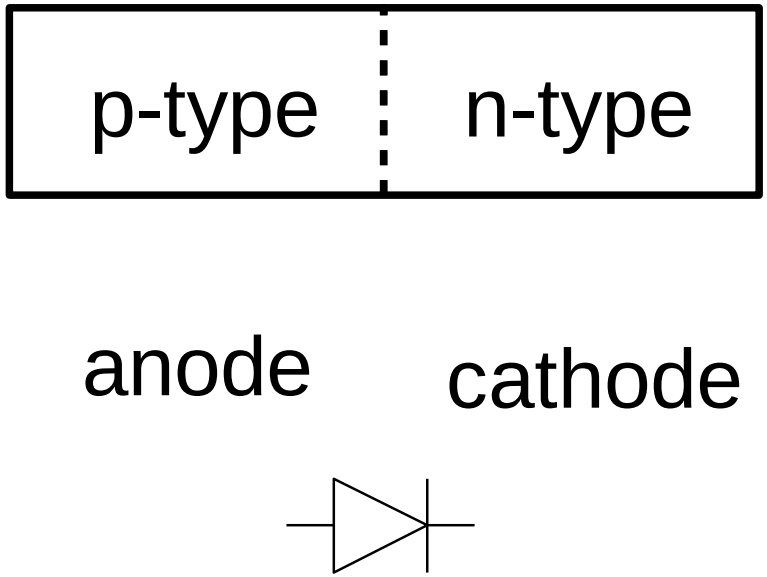
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: As, extra electron (n-type)
- Group III: B(Boron) missing electron, called hole (p-type)



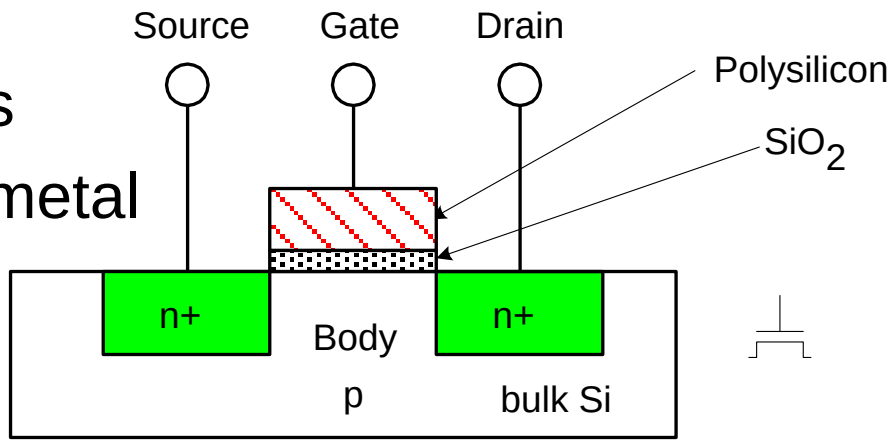
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



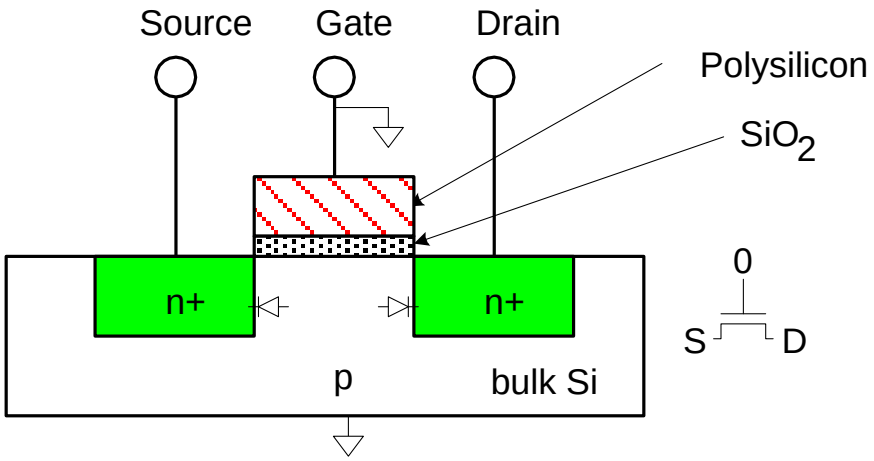
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



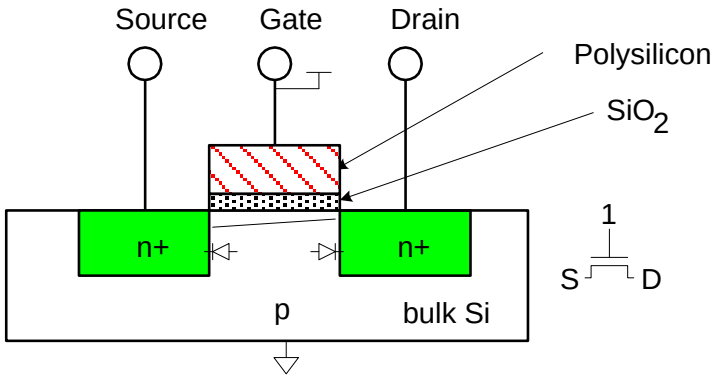
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



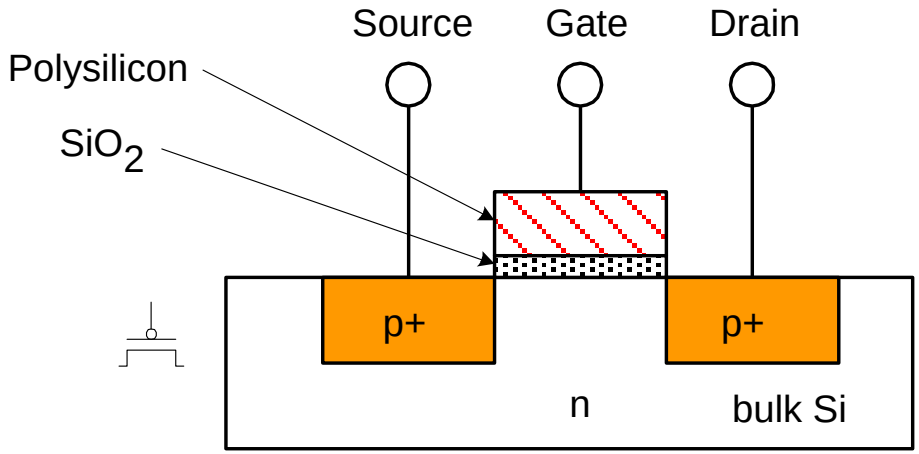
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



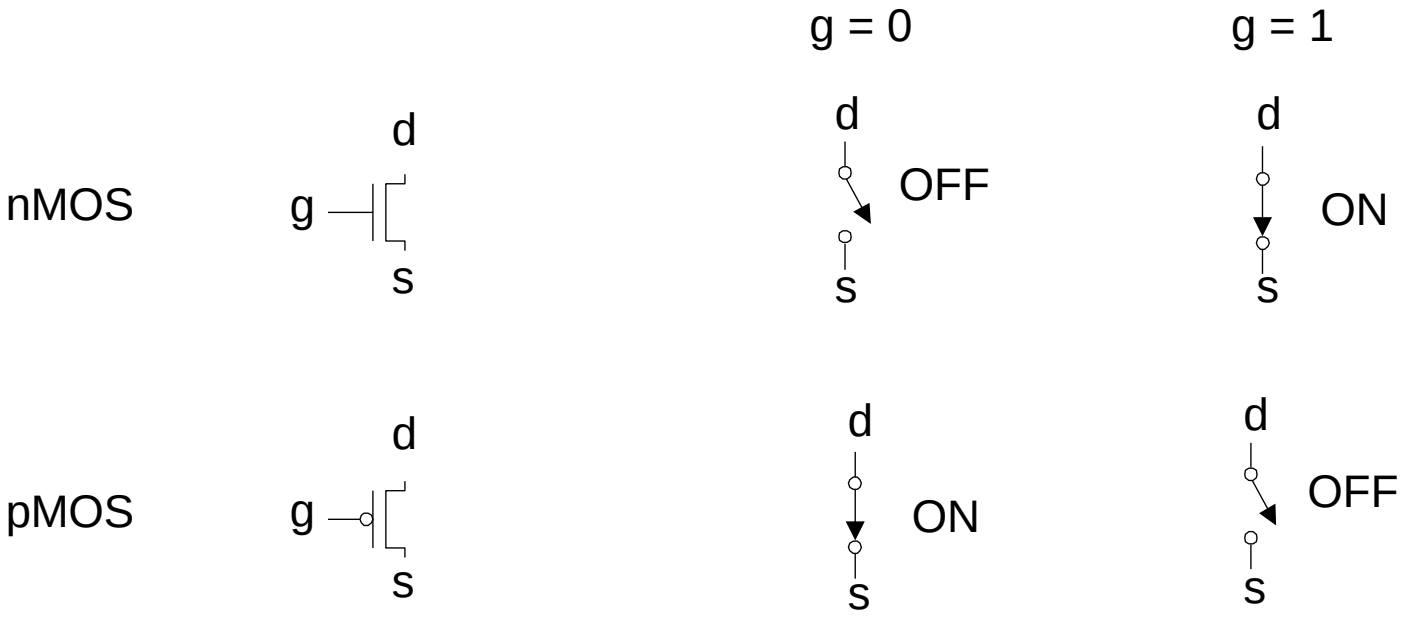
Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.9,0.8…

$$P_{\text{switching}} = CV_{DD}^{2} f_{\text{sw}}$$

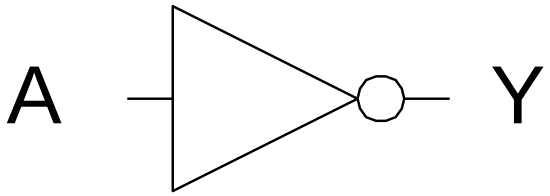
Transistors as Switches

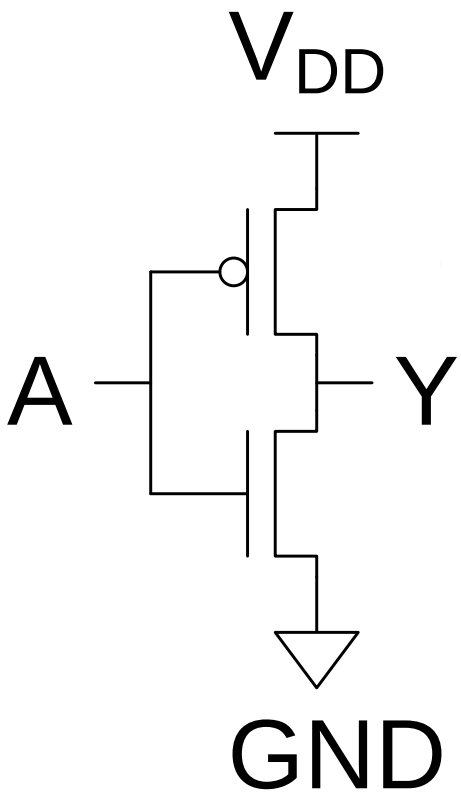
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

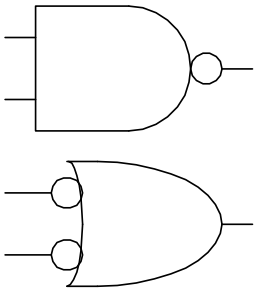
A	Y

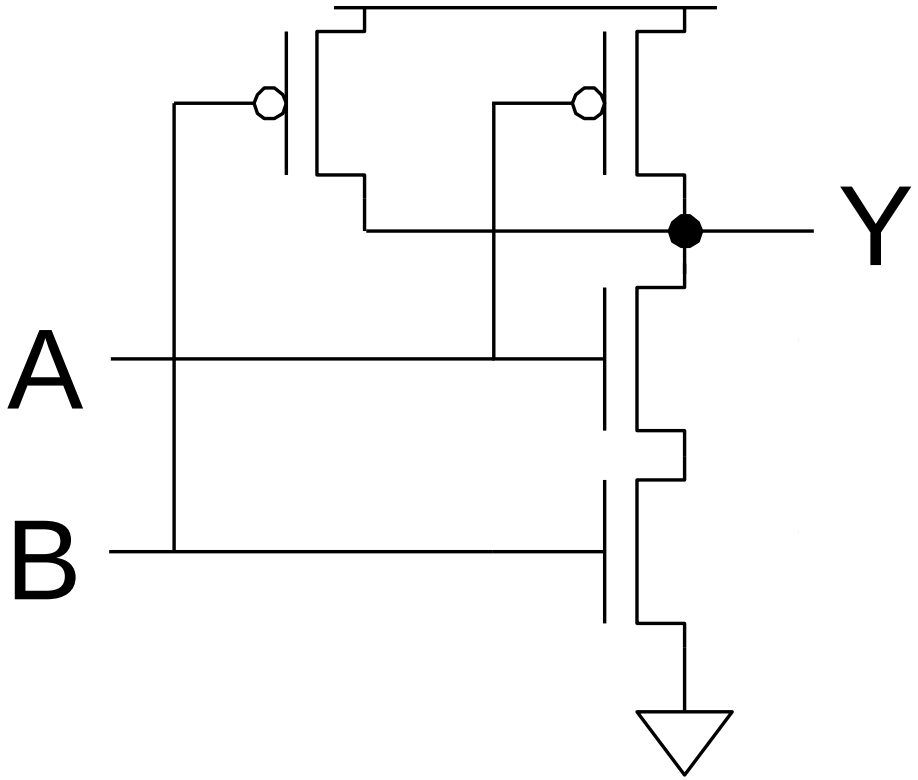




CMOS NAND Gate

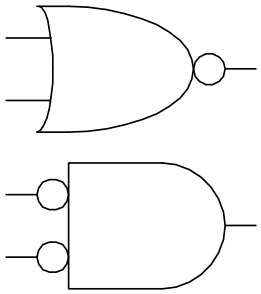
A	B	Y
0	0	
0	1	
1	0	
1	1	

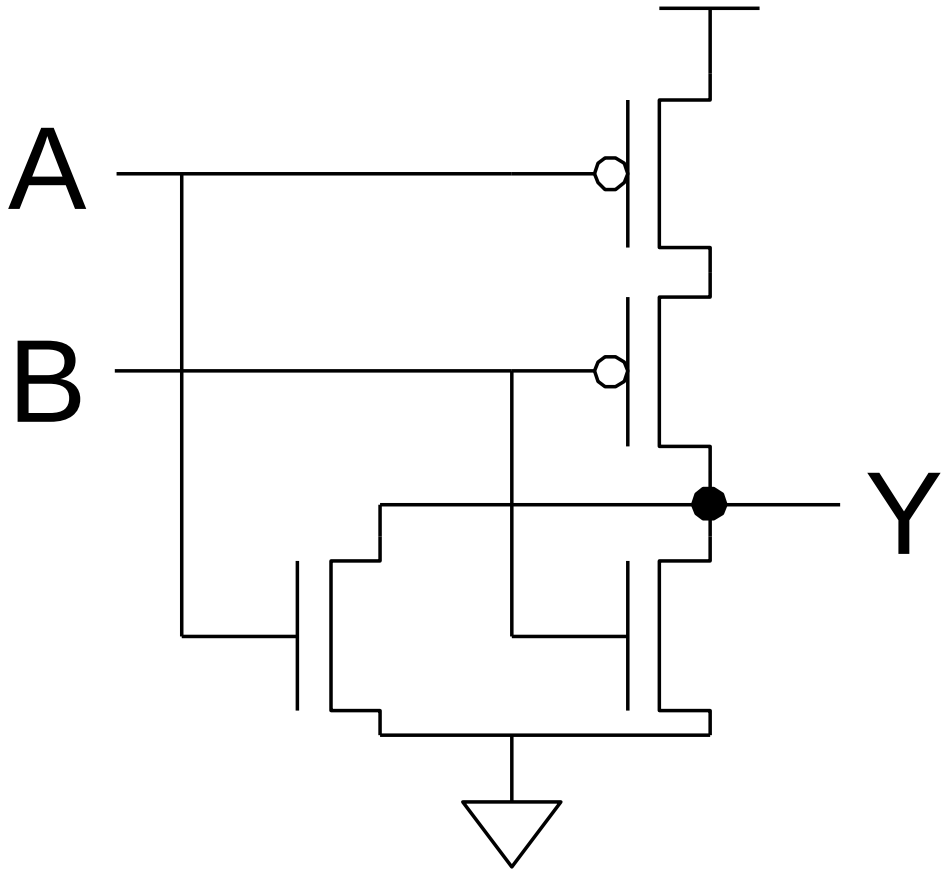




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





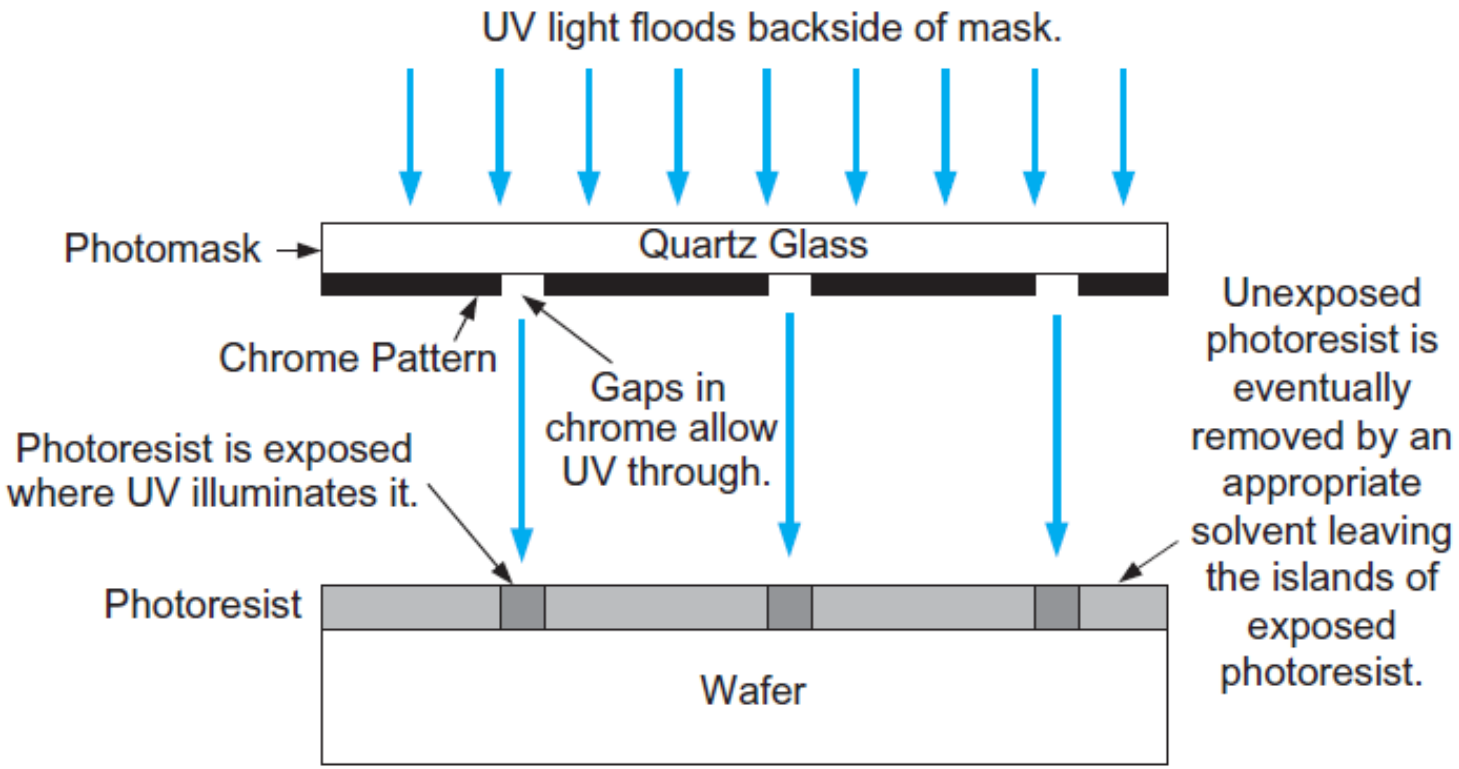
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Photo masking



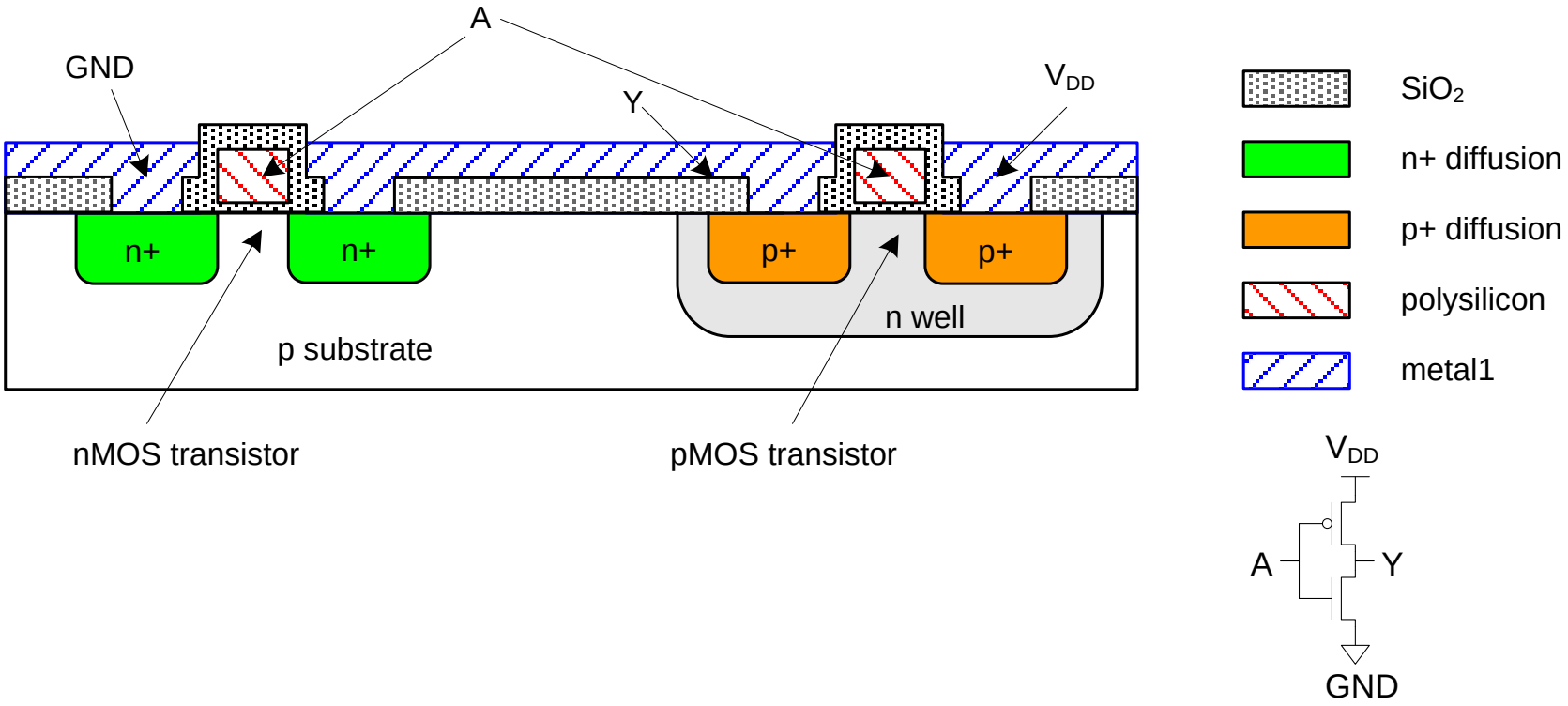
(lens system between mask and wafer)

Fabrication video

- From Sand to Silicon the Making of a Chip Intel

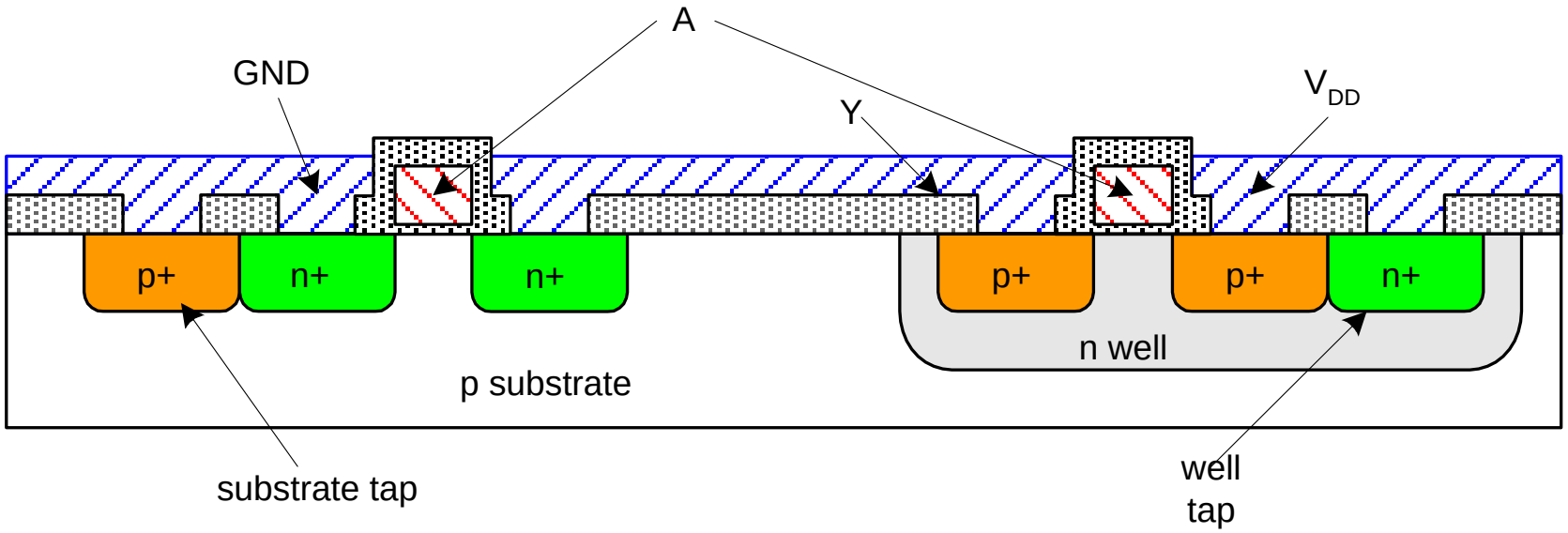
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



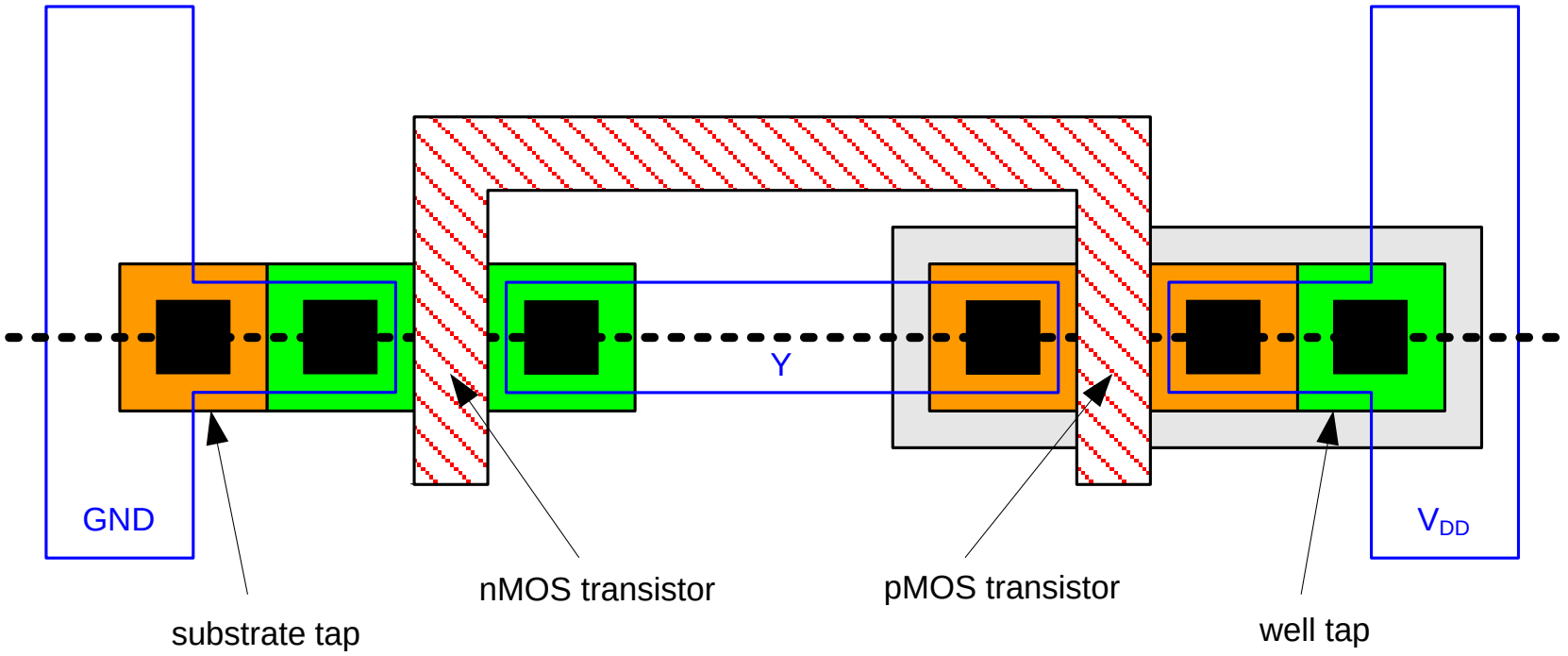
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



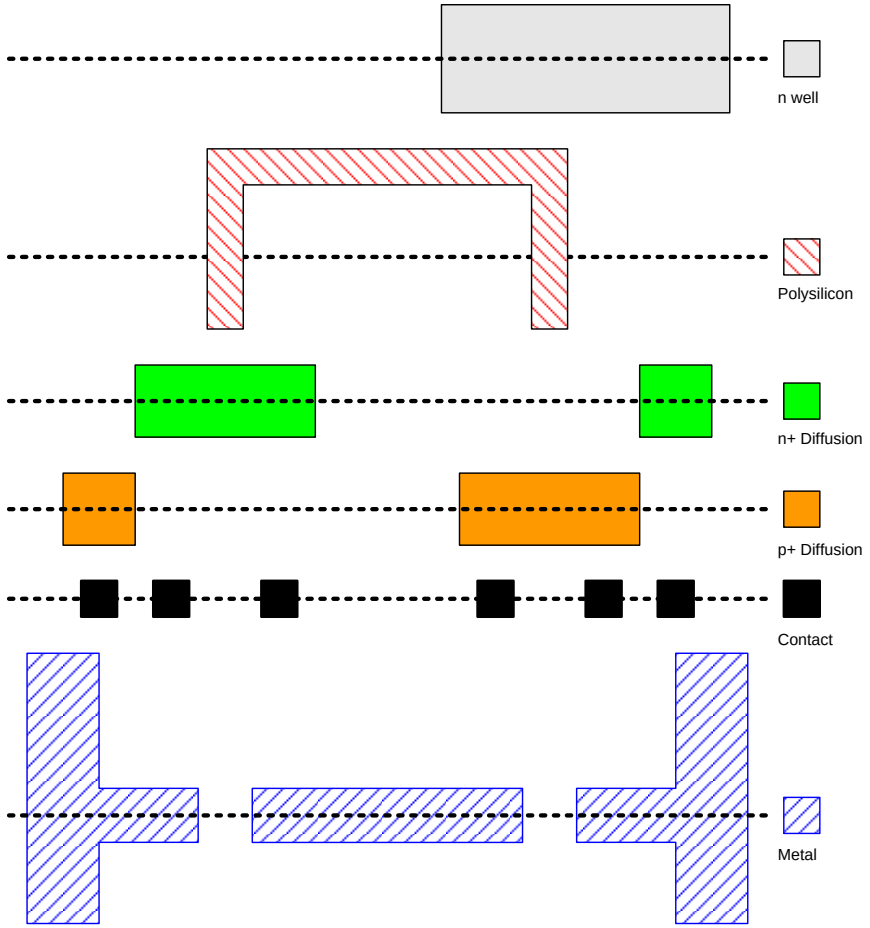
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

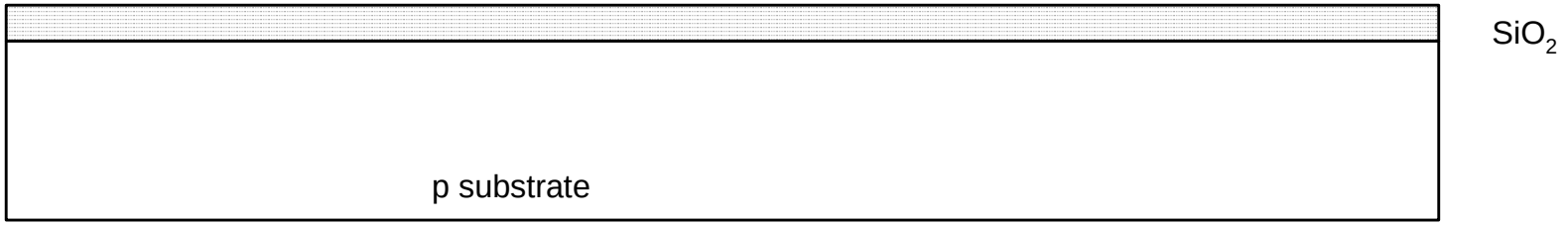
Courtesy of International
Business Machines Corporation.
Unauthorized use not permitted.

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

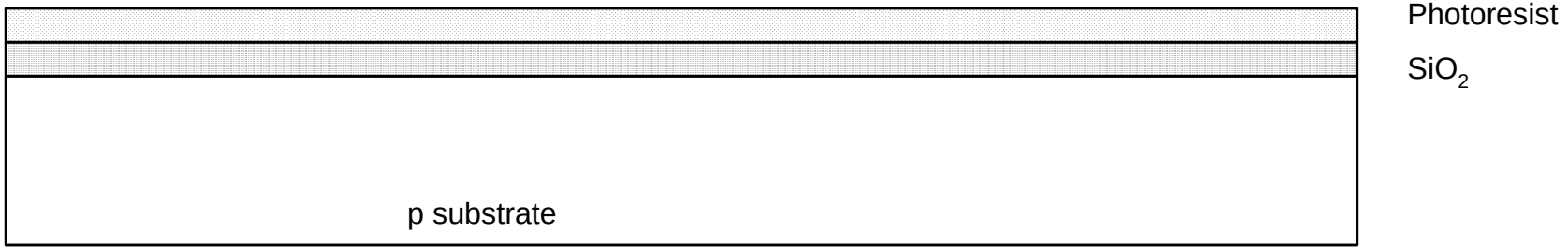
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



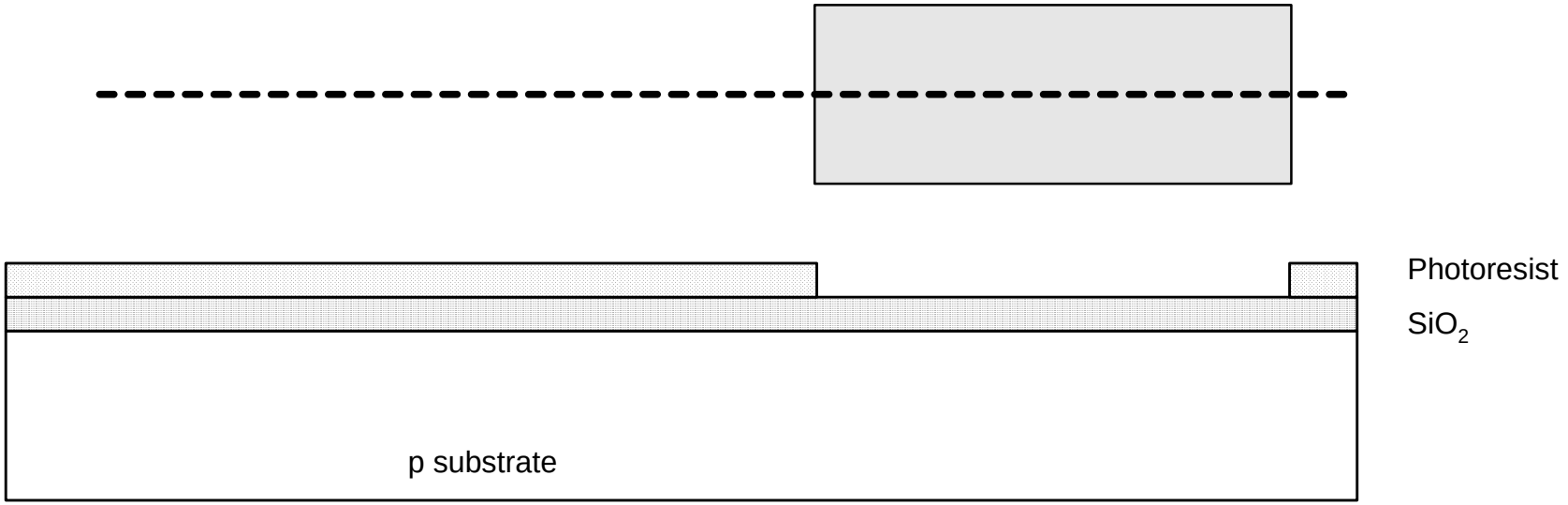
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



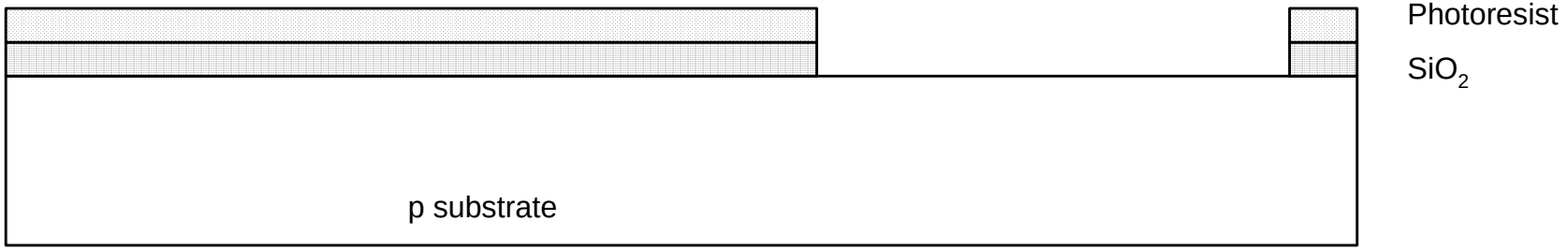
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



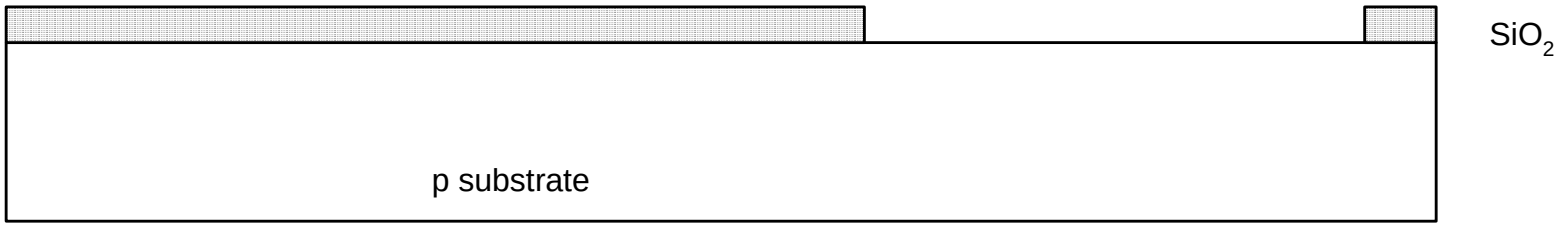
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



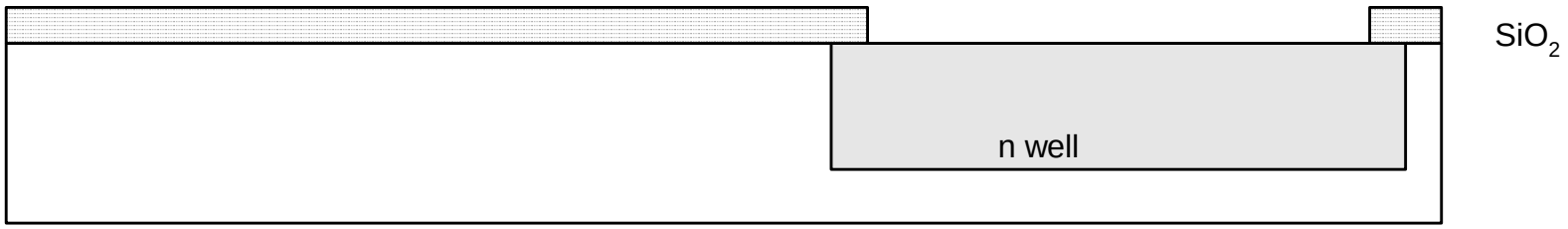
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step



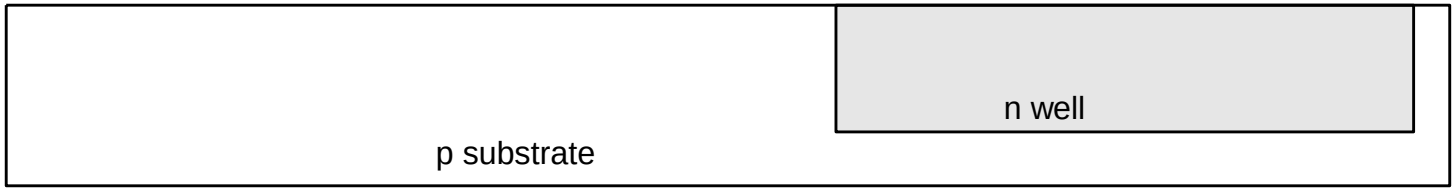
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



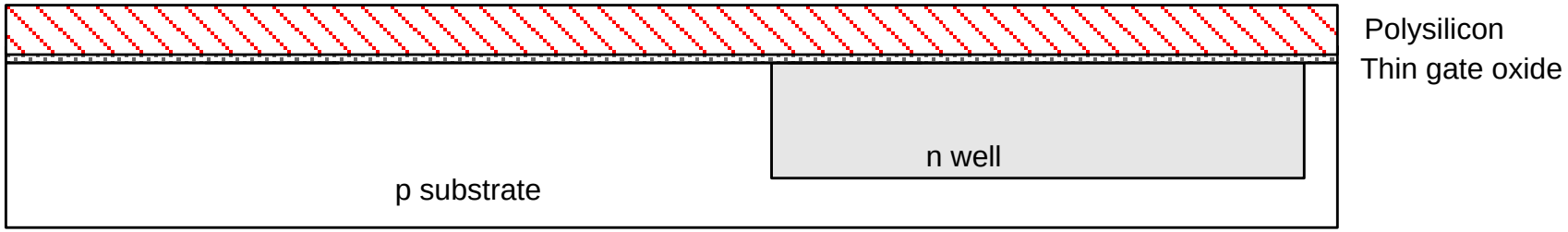
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



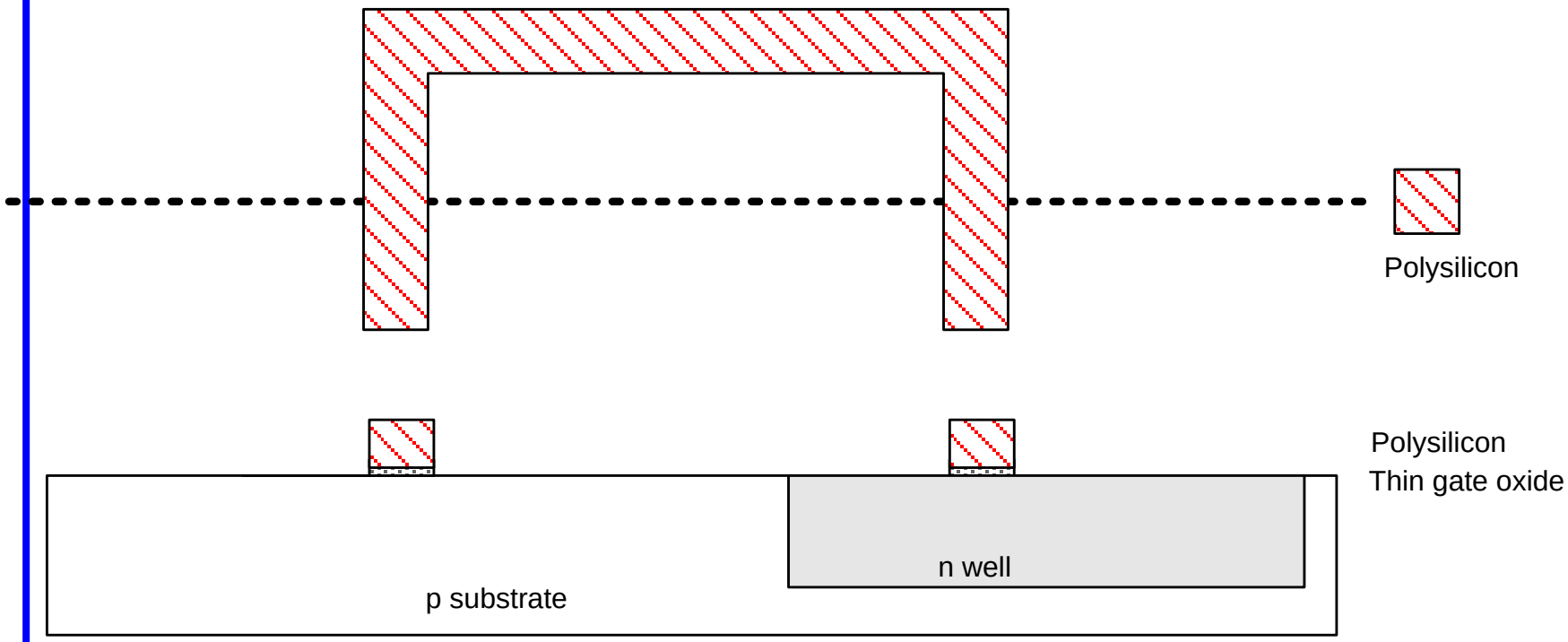
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



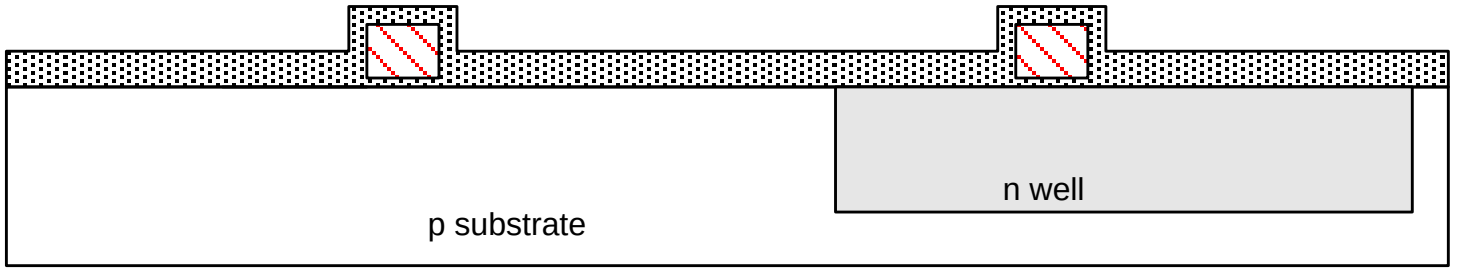
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



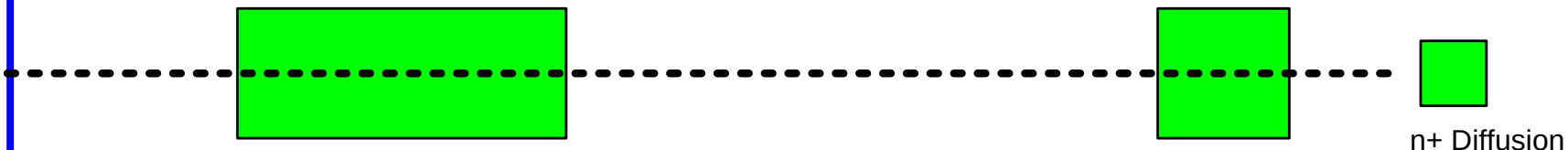
Self-Aligned Process

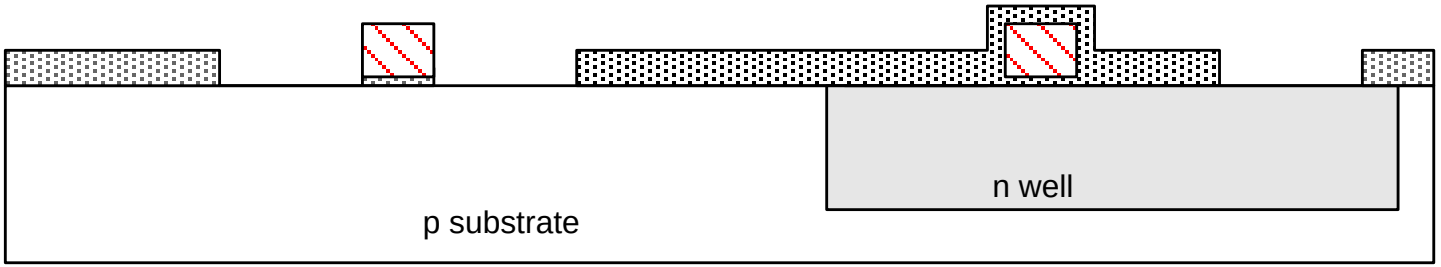
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



N-diffusion

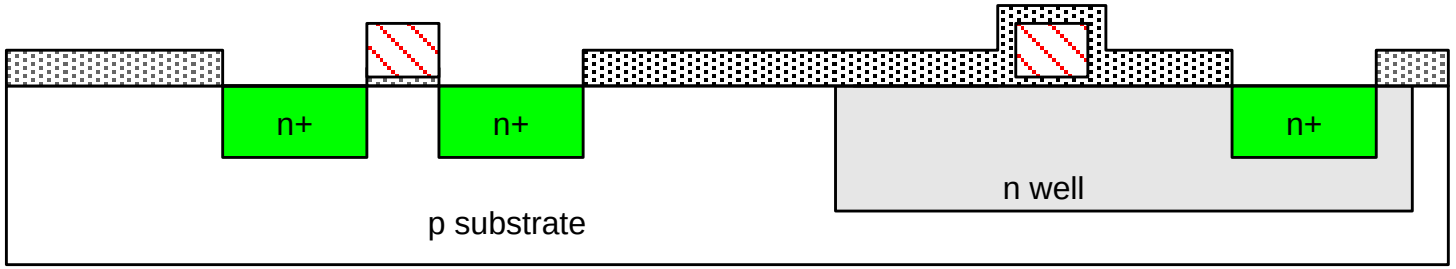
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing





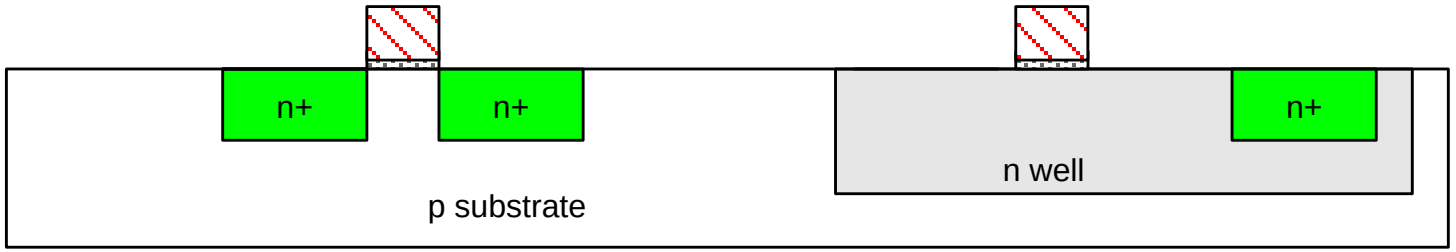
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



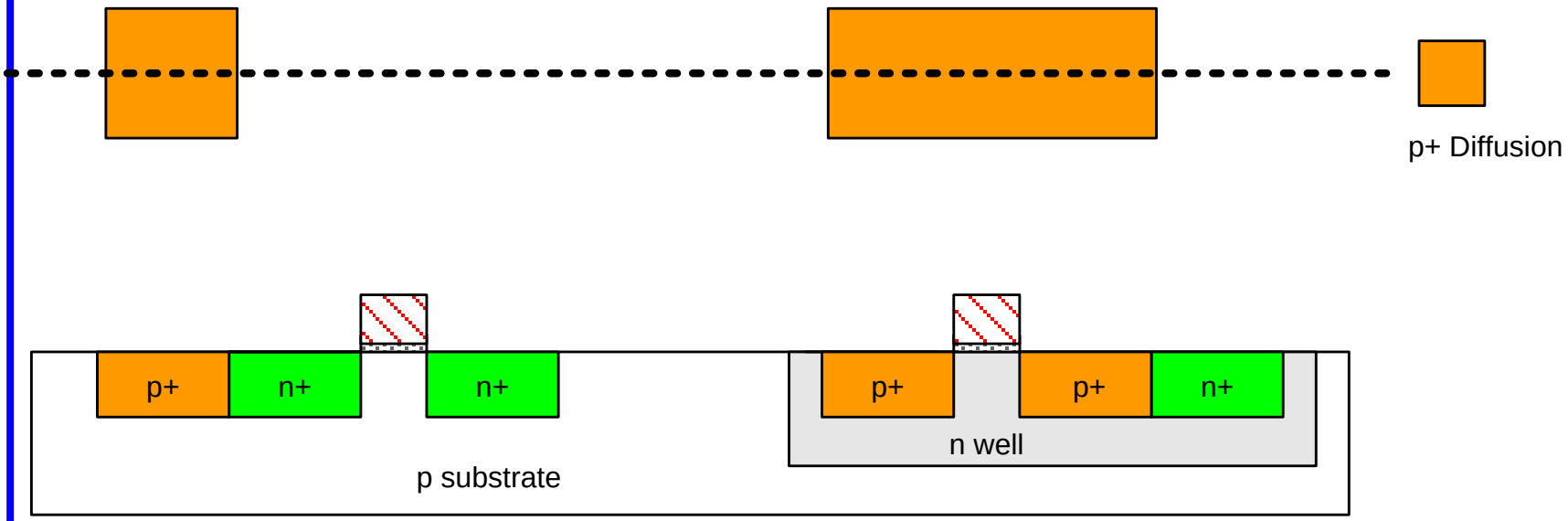
N-diffusion cont.

- Strip off oxide to complete patterning step



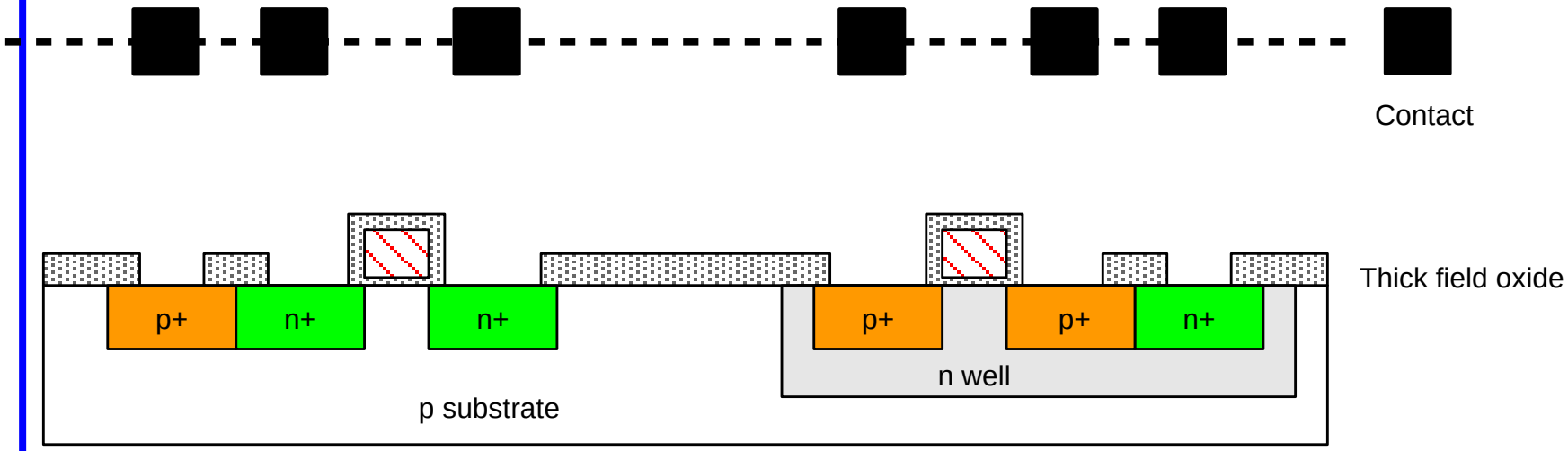
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



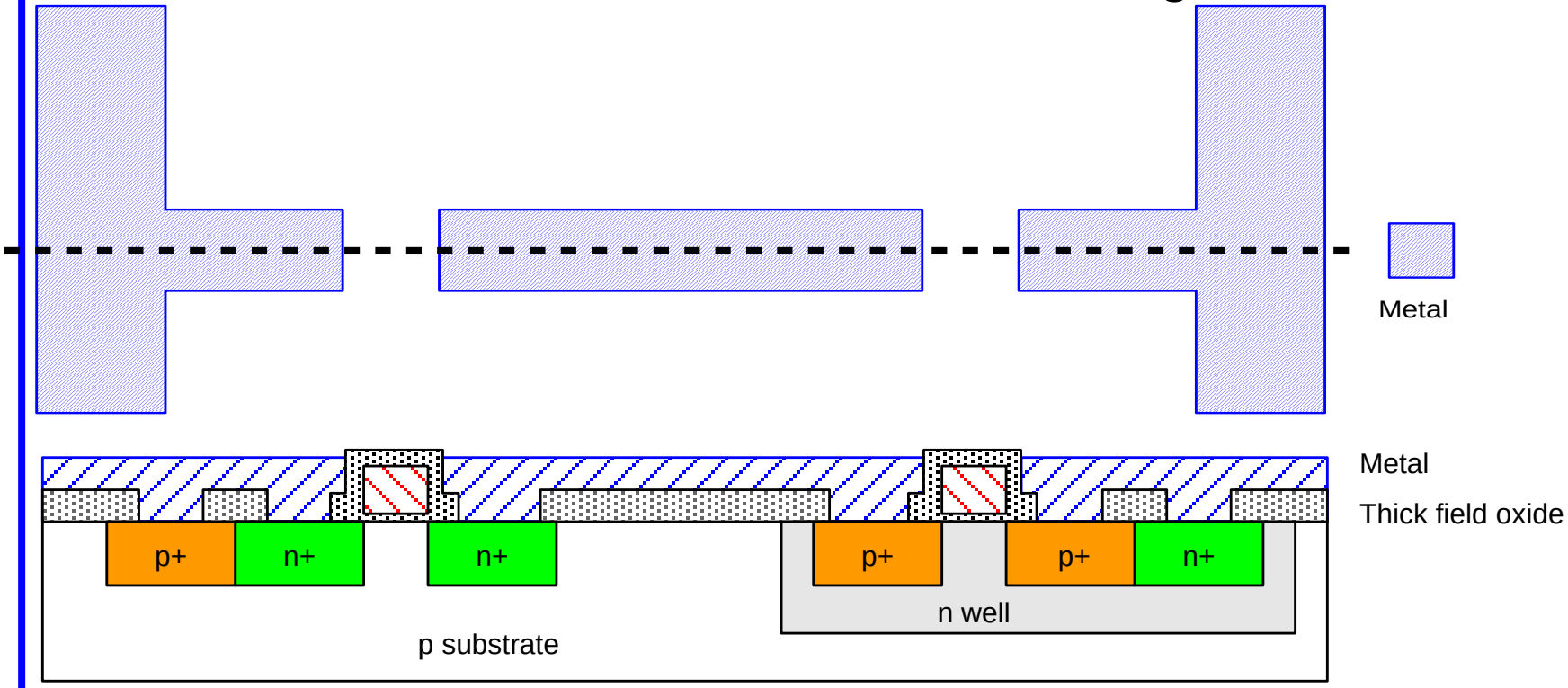
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



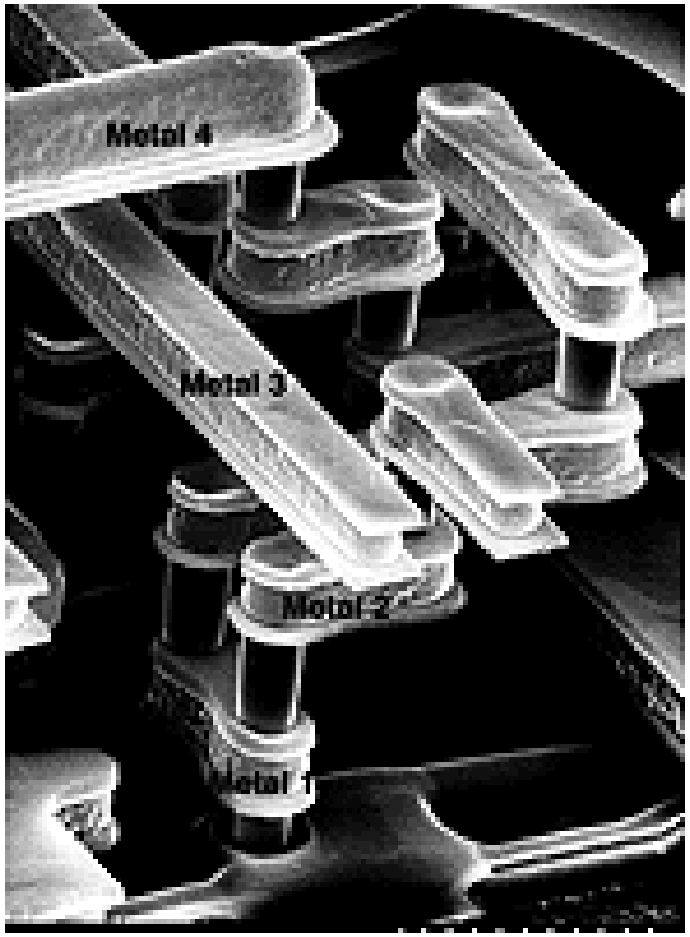
Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

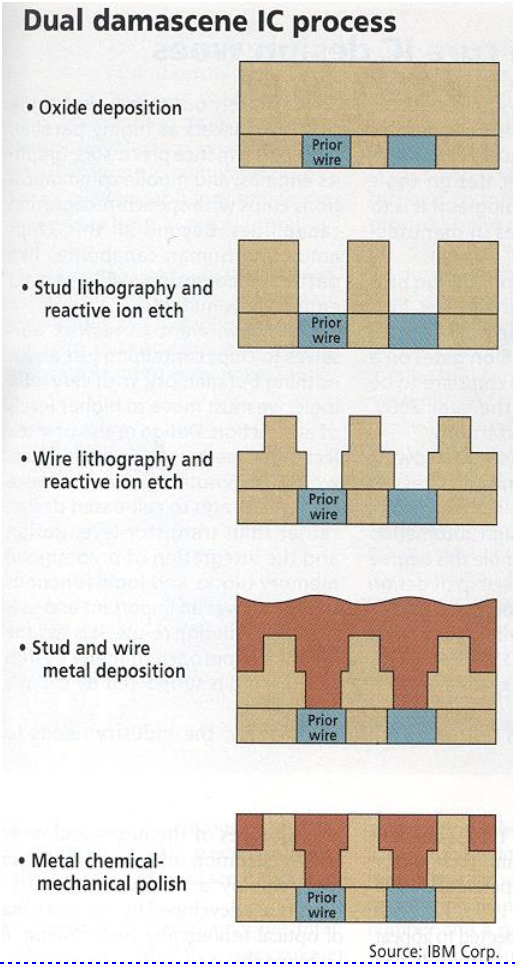


Manufacturing in the Fab

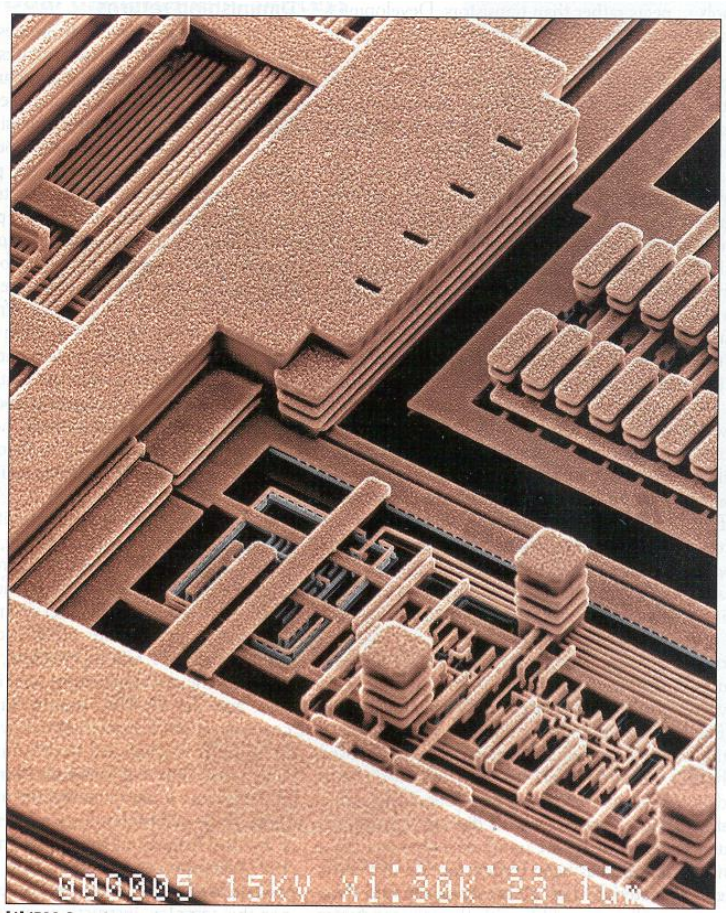
Advanced Metallization



Advanced Metallization



Source: IBM Corp.



Layout

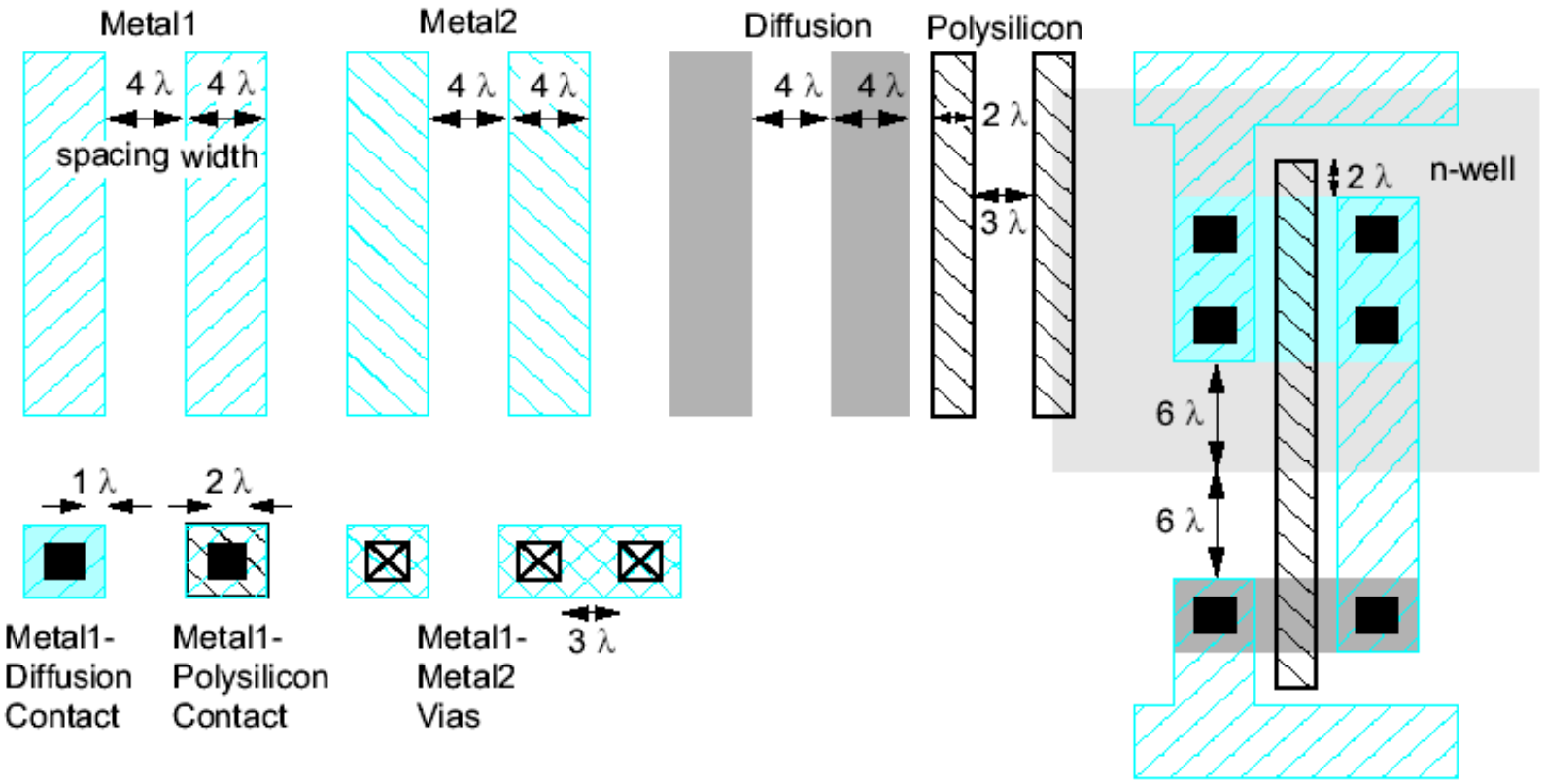
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Simplified Design Rules

- Metal and diffusion have minimum width and spacing of 4 λ.
- Contacts are 2 $\lambda \times 2\ \lambda$ and must be surrounded by 1 λ on the layers above and below.
- Polysilicon uses a width of 2 λ.
- Polysilicon overlaps diffusion by 2 λ where a transistor is desired and has a spacing of 1 λ away where no transistor is desired.
- Polysilicon and contacts have a spacing of 3 λ from other polysilicon or contacts.
- N-well surrounds pMOS transistors by 6 λ and avoids nMOS transistors by 6 λ.

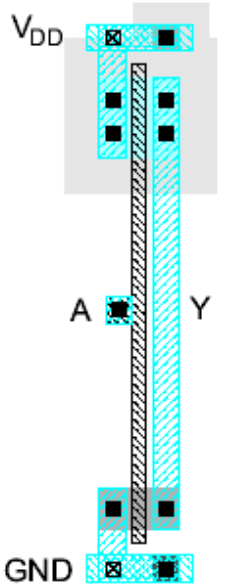
Simplified Design Rules

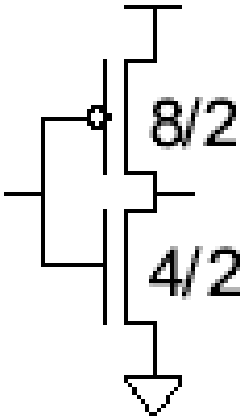
- Conservative rules to get you started

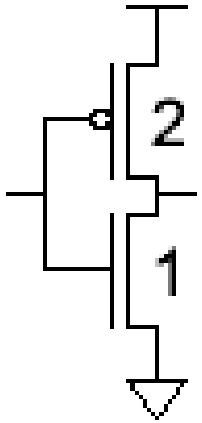


Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long







$$I_{ds} = \frac{Q_{\text{channel}}}{L/v}$$
$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$
$$= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds}$$

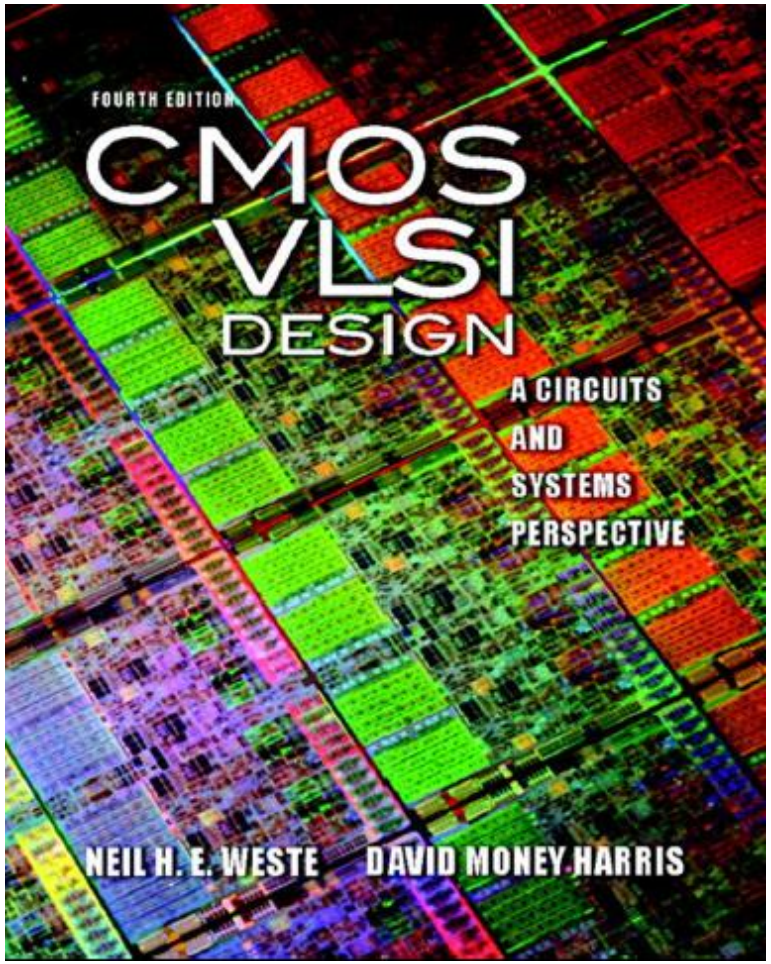
$$\beta = \mu C_{\text{ox}} \frac{W}{L};\ V_{GT} = V_{gs} - V_t$$

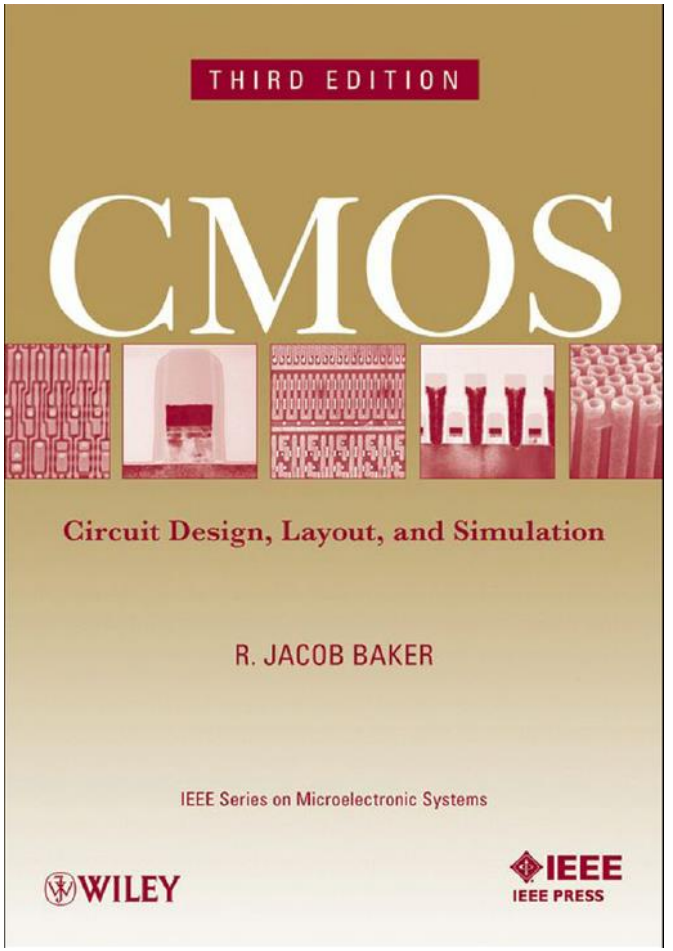
Summary

- MOS transistors are stacks of gate, oxide, silicon
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!

Textbooks


FOURTH EDITION
CMOS VLSI DESIGN
A CIRCUITS AND SYSTEMS PERSPECTIVE
NEIL H. E. WESTE
DAVID MONEY HARRIS


THIRD EDITION
CMOS
Circuit Design, Layout, and Simulation
R. JACOB BAKER
IEEE Series on Microelectronic Systems
WILEY
IEEE
IEEE PRESS

Videos

- How Microchips Are Made by Learn Plus Fun

http://www.dailymotion.com/video/x3xm5k9

- From Sand to Silicon: Integrated Circuit Design and Manufacturing by Jas Lonnnquist and Jon Plutte

http://www.computerhistory.org/revolution/digital-logic/12/288/2220

- The Fabrication of Integrated Circuits

http://www.dailymotion.com/video/x2mhml2

- How a CPU is Made by Global Foundries

http://www.wimp.com/how-a-cpu-is-made/

- (Very old) Fairchild Briefing on Integrated Circuits

http://www.computerhistory.org/collections/catalog/102651800

Grading

- 80% written Exam
- 10% Witten Assignment, including homework
- 10% Lab Report