Differential and Multistage Amplifiers

Outline

- MOS differential pair
  - Common mode signal operation
  - Differential mode signal operation
  - Large signal operation
  - Small signal operation
- Differential and common mode half-circuits
- Common mode rejection
- DC offset
- Differential amplifier with current mirror load
- Multistage amplifiers

Reference book:

A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits.
B. Oxford University Press, 2016: Chapter 9

Introduction

- **The differential-pair or differential-amplifier configuration is**

  • Widely used in analogy integrated-circuit design

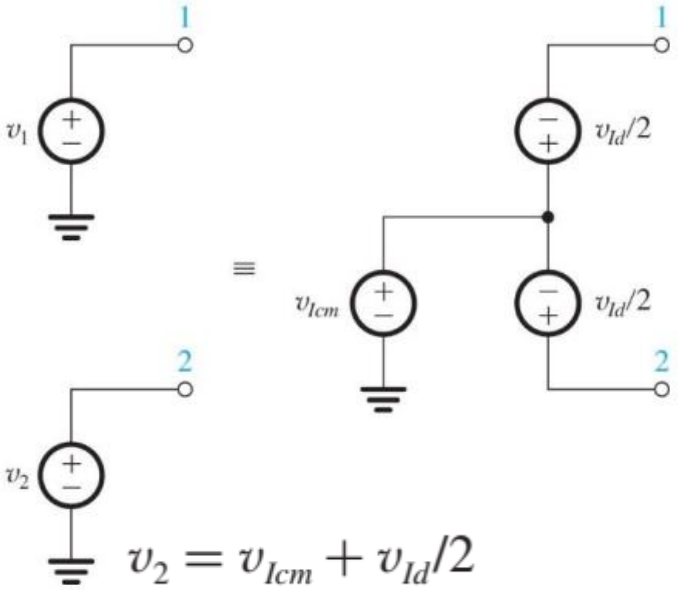
  • Much less sensitive to noise and interference than single-ended circuits

  • Without the need for bypass and coupling capacitors to couple amplifier stages

Common and Differential Mode Signals

- Two signal sources
  - v_1: reference signal minus a (half) component
  - v_2: reference signal plus a (half) component
- Differential mode signal component, $v_{Id} = v_2 - v_1$
  - Typically the “interesting” part of the signal
- Common mode signal component, $v_{Icm} = \frac{1}{2}(v_1 + v_2)$
  - Typically a reference or noise level, not desired
- Common mode rejection ratio (CMRR)
  - Differential to common mode power gain ratio, $CMRR = 20\log_{10}\left(\frac{A_d}{A_{cm}}\right)$

$$v_1 = v_{Icm} - v_{Id}/2$$

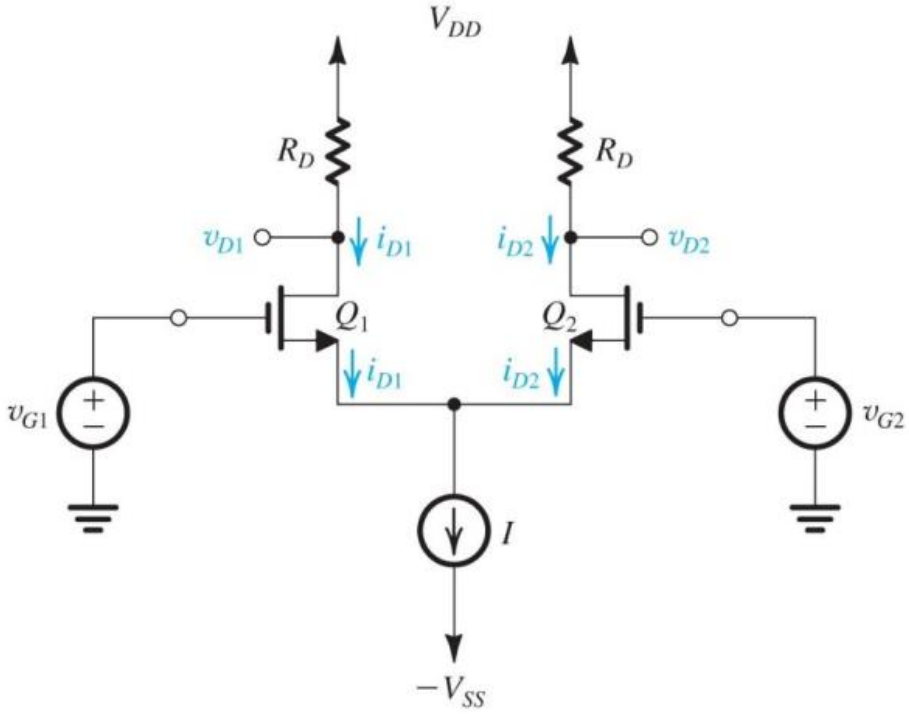


$$v_2 = v_{Icm} + v_{Id}/2$$

Observe the split and polarity of the differential sources.

MOS Differential Pair

- Two balanced transistors
  - Same technology, k_n
  - Same threshold, V_{tn}
  - Same size, W/L
- Arranged symmetrically
  - Equal load, R_D
  - Share one current sink, I
  - Source terminals joined, V_S
  - Equal gate bias, V_G
  - Equal overdrive bias, $V_{OV} = V_{GS} - V_{tn}$
- Differential ports
  - Input over gates
  - Output over drains



The MOSFETs in the differential pair (and current sink) must be operated in saturation mode.

Common Mode Operation

- Drain level: constant
  - Forced current through load
  - Resistance sets voltage drop

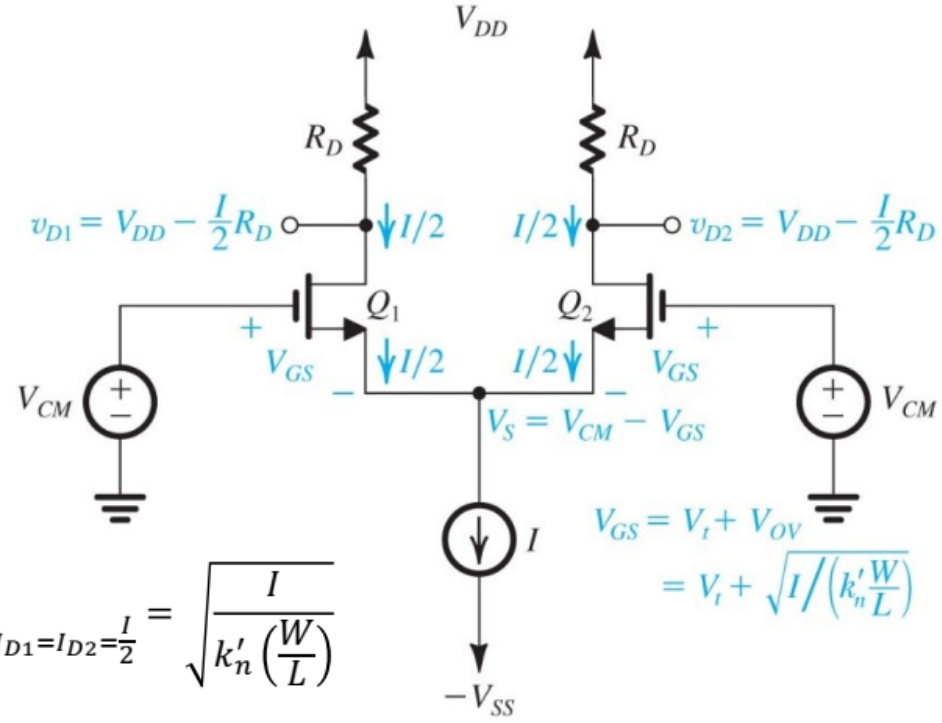
$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$$

- Gate overdrive: constant
  - Forced current through saturated MOSFETs
  - Materials and design sets overdrive

$$I_{D1}, I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2 = \frac{I}{2}$$

- Source level: varies with CM input
  - Sink must "absorb" gate voltage offsets

$$V_S = V_{CM} - V_{GS} = V_{CM} - V_{tn} - V_{OV}$$



$$V_{OV}\Big|_{I_{D1}=I_{D2}=\frac{I}{2}} = \sqrt{\frac{I}{k_n'\left(\frac{W}{L}\right)}}$$

The MOSFETs in the differential pair share one current sink.

$$V_{DS} = V_{DD} - \frac{R_D I}{2} - V_s \geq V_{GS} - V_t; V_{DD} - \frac{R_D I}{2} - V_{CM} + V_{GS} \geq V_{GS} - V_t; V_{CM} \leq V_{DD} - \frac{R_D I}{2} + V_t$$

$$V_S \geq V_{CS} - V_{SS}; V_{CM} - V_{GS} \geq V_{CS} - V_{SS}; V_{CM} \geq V_{GS} + V_{CS} - V_{SS}; V_{CM} \geq -V_{SS} + V_{CS} + V_t + V_{OV}$$

$$V_{CM\max} = V_t + V_{DD} - \frac{I}{2}R_D$$

$$V_{CM\min} = -V_{SS} + V_{CS} + V_t + V_{OV}$$

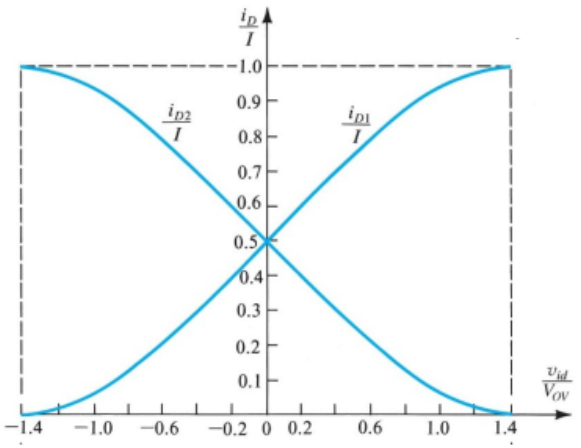
- The highest value of V_{CM} is limited by the requirement that Q_1 and Q_2 remain in saturation
- The lowest value of V_{CM} is determined by the need to allow for a sufficient voltage across the current source I for it to operate properly

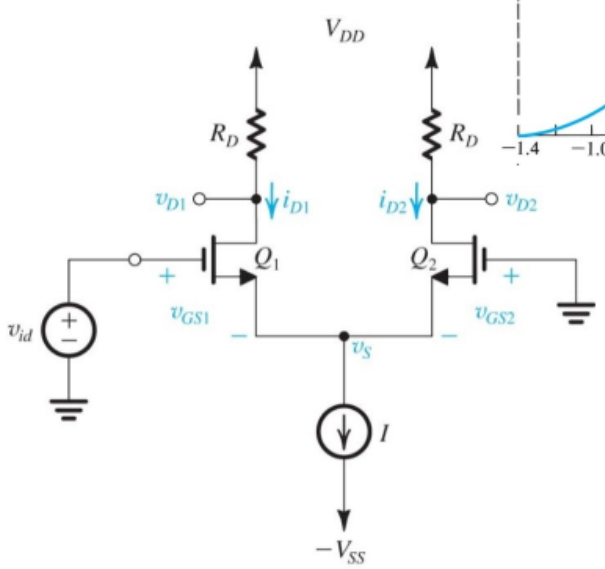
Differential Mode Operation

- Difference signal between Q1 and Q2
  - Input over gates, $v_{id} = v_{G1} - v_{G2}$
  - Output over drains, $v_{od} = v_{D2} - v_{D1}$
- Positive(/ negative) differential input
  - Different overdrive in Q1 and Q2
  - Redistribution of current towards Q1(/ Q2) branch of the pair
- Limit of operation
  - Steering all current to one transistor

$$-\sqrt{2}V_{OV} < v_{id} < \sqrt{2}V_{OV}$$

$$V_{OV}\Big|_{I_{D1}=I_{D2}=\frac{I}{2}} = \sqrt{\frac{I}{k_n'\left(\frac{W}{L}\right)}}$$





$$I = \frac{1}{2}\left(k_n'\frac{W}{L}\right)(v_{GS1} - V_t)^2$$

$$v_{GS1} = V_t + \sqrt{2I/k_n'(W/L)}$$
$$= V_t + \sqrt{2}V_{OV}$$

$$v_{id\max} = v_{GS1} + v_S$$
$$= V_t + \sqrt{2}V_{OV} - V_t$$
$$= \sqrt{2}V_{OV}$$

Large Signal Operation

- Gate overdrive level determines differential voltage window

$$i_{D1} = \frac{1}{2}k_n'\frac{W}{L}(v_{GS1} - V_t)^2$$

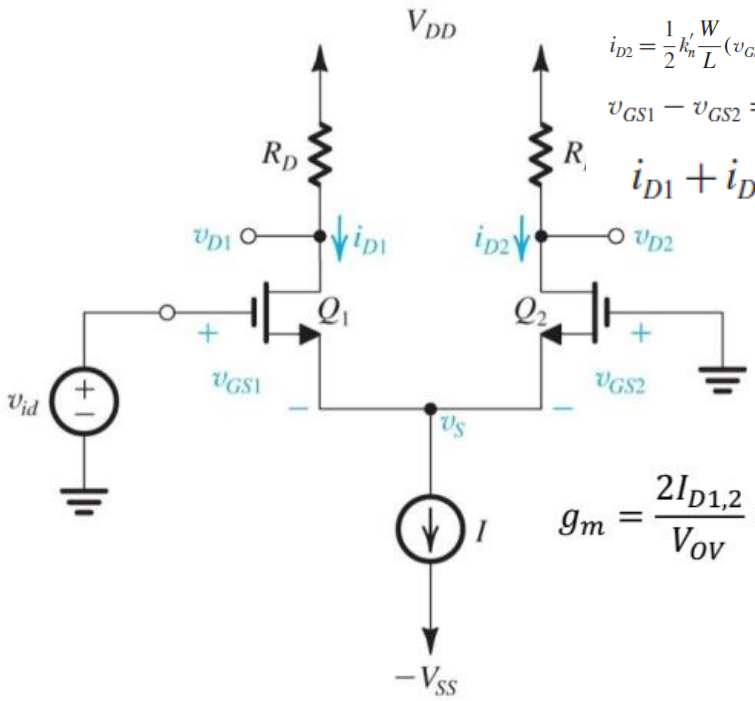
$$i_{D2} = \frac{1}{2}k_n'\frac{W}{L}(v_{GS2} - V_t)^2$$

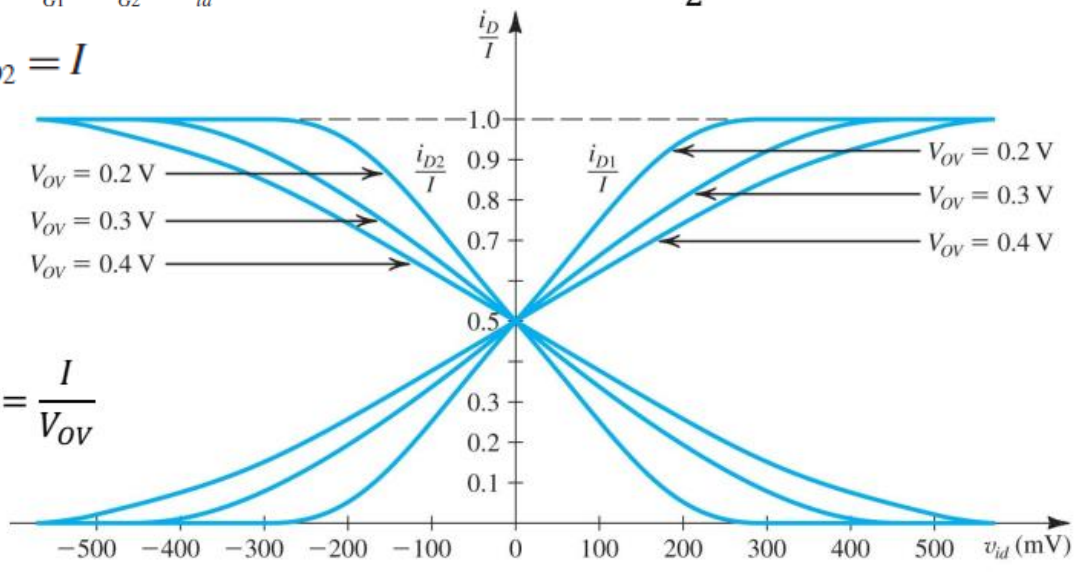
$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id}$$

$$i_{D1} + i_{D2} = I$$

$$i_{D1,2} = I_{D1,2} \pm i_d = \frac{I}{2} \pm \left(\frac{I}{V_{OV}}\right)\frac{v_{id}}{2}\sqrt{1 - \left(\frac{v_{id}}{2V_{OV}}\right)^2}$$

$$i_d = \{v_{id} \ll 2V_{OV}\} \approx g_m\frac{v_{id}}{2}$$





$$g_m = \frac{2I_{D1,2}}{V_{OV}} = \frac{I}{V_{OV}}$$

These graphs clearly illustrate the linearity–transconductance trade-off obtained by changing the value of V_{OV}: The linear range of operation can be extended by operating the MOSFETs at a higher V_{OV} (by using smaller W/L ratios) at the expense of reducing g_m and hence the gain. This trade-off is based on the assumption that the bias current I is being kept constant. The bias current can, of course, be increased to obtain a higher g_m. The expense for doing this, however, is increased power dissipation, a serious limitation in IC design.

Small Signal Operation

- Small signal differential input voltage superimposed on bias point

$$v_{G1,G2} = V_{CM} \pm \frac{v_{id}}{2}$$

- Small signal perturbation of current

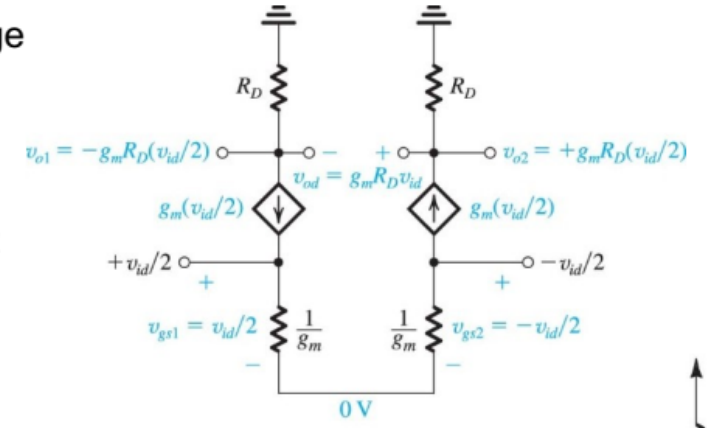
$$i_{D1,D2} = \frac{I}{2} \pm g_m \frac{v_{id}}{2}$$

- Differential voltage developed over drain terminals

$$v_{D1,D2} = V_{DD} - R_D\left(\frac{I}{2} \pm g_m \frac{v_{id}}{2}\right)$$

- Differential gain results

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_D$$

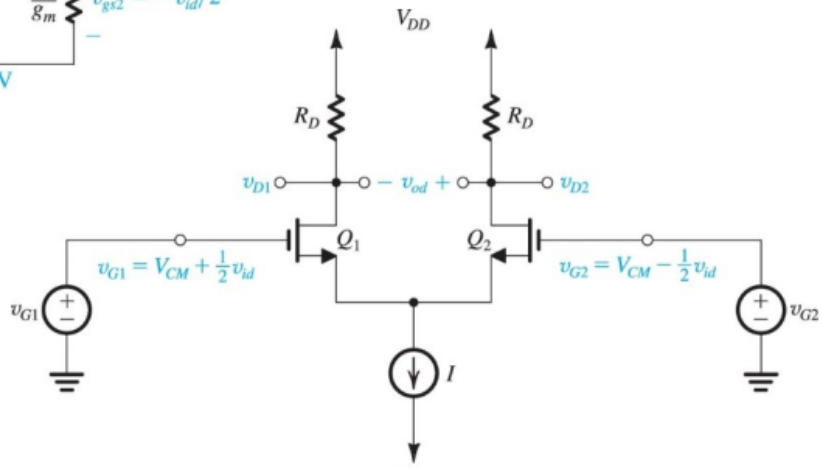


$$g_m = \frac{2I_{D1,2}}{V_{OV}} = \frac{I}{V_{OV}}$$

$$v_{id} = v_{g1} - v_{g2} \ll 2V_{OV}$$

$$i_d = i_{d1} = -i_{d2} = g_m \frac{v_{id}}{2}$$

$$v_{od} = v_{d2} - v_{d1} = g_m v_{id} R_D$$



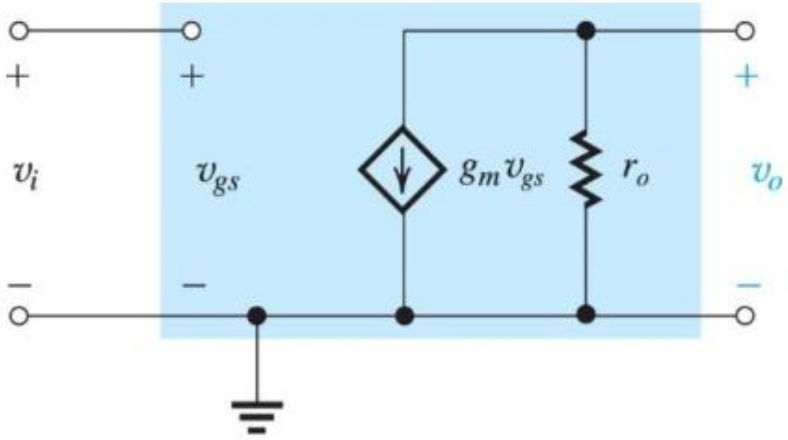
$$v_{o1} = -g_m \frac{v_{id}}{2} R_D \qquad \frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D$$

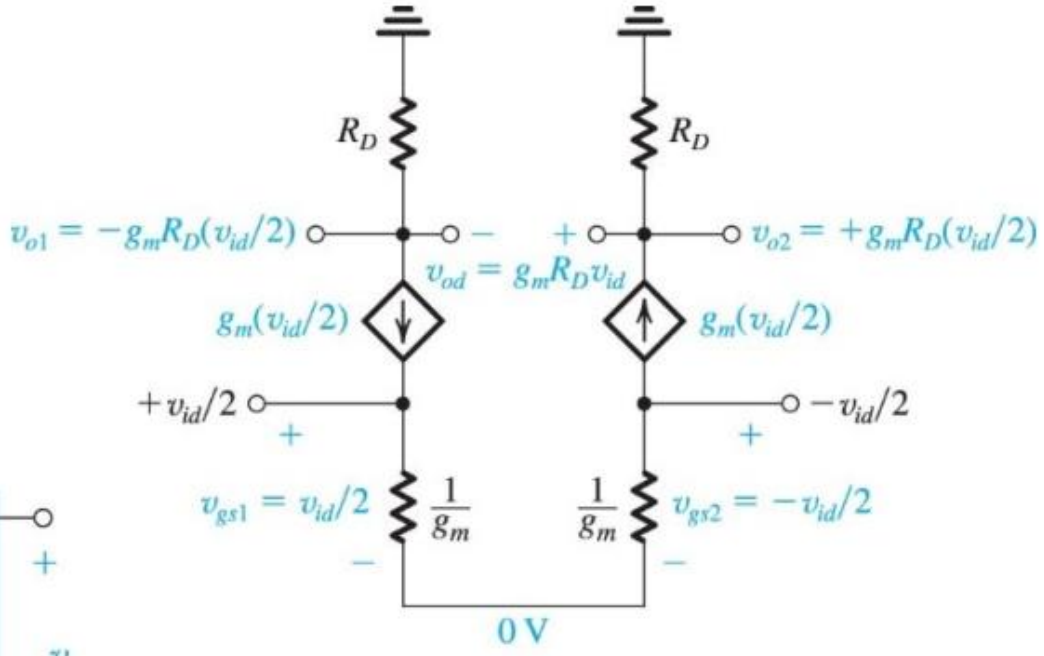
$$v_{o2} = +g_m \frac{v_{id}}{2} R_D \qquad \frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

How does a finite MOSFET output resistance affect the gain expression?

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_D'$$

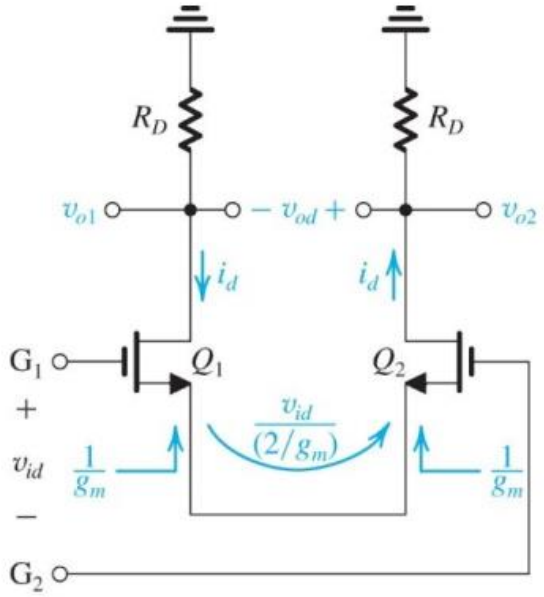


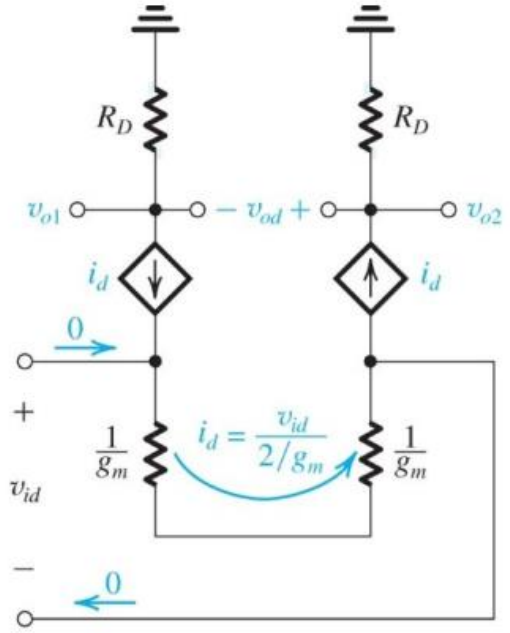


Small Signal Analysis Directly on the Circuit Schematic

- You may save some ink and time…
  …or make grave mistakes

$$A_d = \frac{v_{od}}{v_{id}} = g_m(r_o||R_D)$$

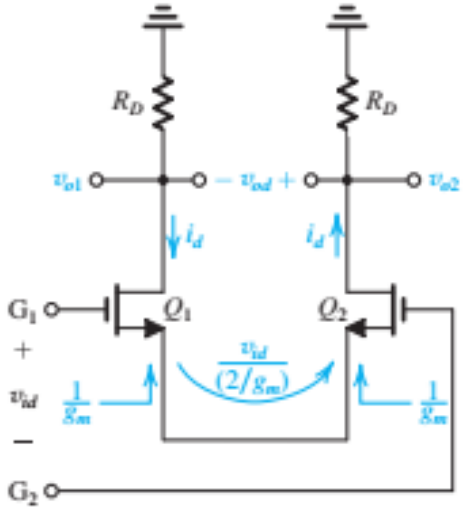




Imagine the small signal model and work on the original schematic (experienced users only).

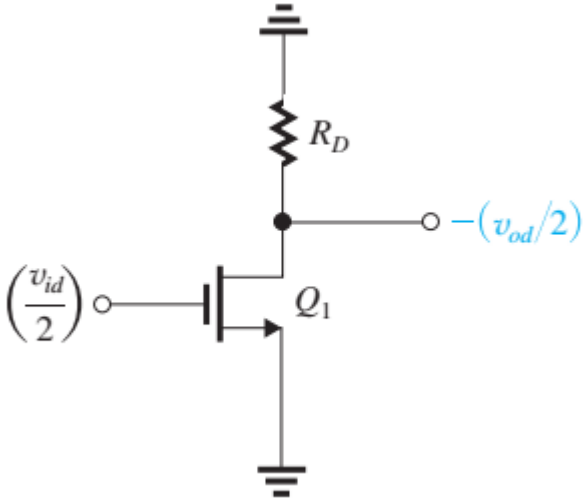
Differential Mode Half Circuits

- Differential mode: Push-pull anti-symmetry
  - Source output resistance: virtual ground
    - No differential current flow
    - Constant bias condition
  - Load resistance: split
    - Half the voltage level
    - Half the impedance value



➢ The differential gain A_d can be determined directly from the half-circuit. For instance, if we wish to take r_o of Q_1 and Q_2 into account, we can use the half-circuit with the following result:

$$A_d = g_m(R_D \| r_o)$$



$$A_d = g_m(R_D \| r_o)$$

Common Mode Half Circuits

- Common mode: Push-push symmetry
  - Source output resistance: split
    - Half the current level
    - Twice the impedance value
  - Load resistance ignored
    - Same voltage on both sides

$$v_{icm} = \frac{i}{g_m} + 2iR_{SS}$$

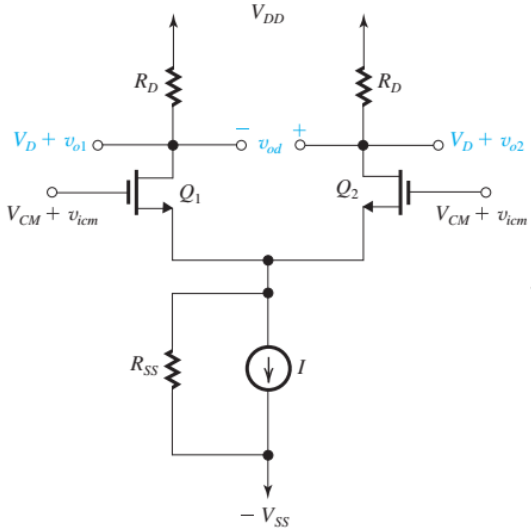
$$i = \frac{v_{icm}}{1/g_m + 2R_{SS}}$$

$$v_{o1} = v_{o2} = -R_D i$$

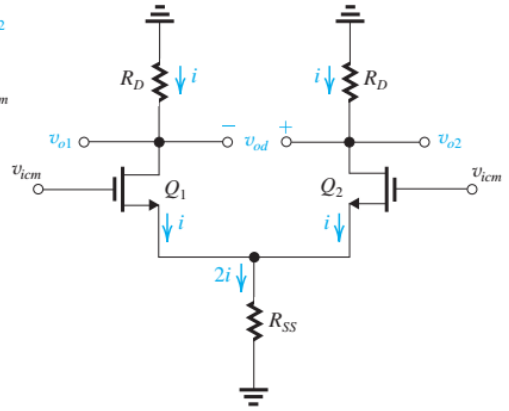
$$v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm}$$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq -\frac{R_D}{2R_{SS}}$$

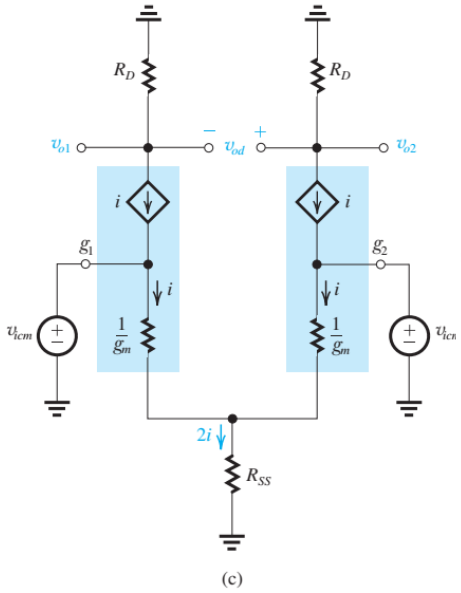
$$v_{od} = v_{o2} - v_{o1} = 0$$



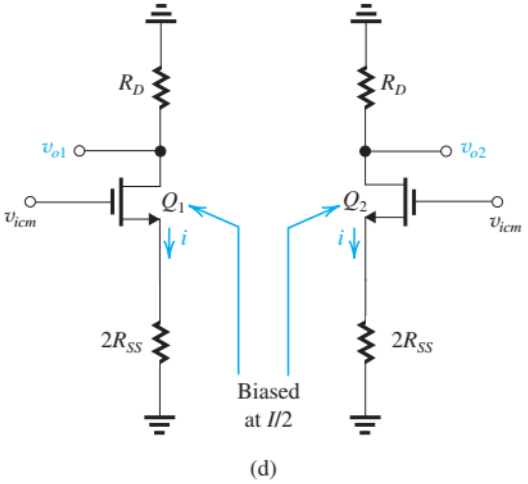
(a)



(b)



(c)



(d)

- Thus the circuit still rejects common-mode signals! Unfortunately, however, this will not be the case if the circuit is not perfectly symmetrical.

Common Mode Gain and CMRR

- Differential gain, A_d

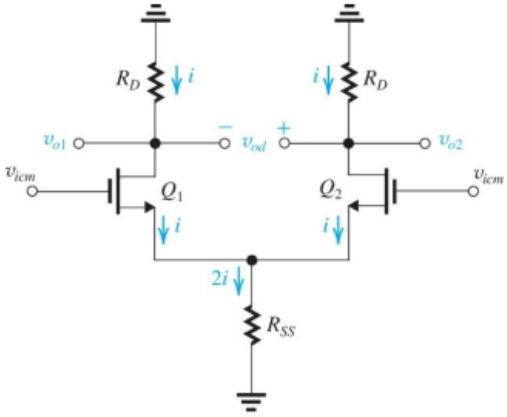
$$A_d = g_m R_D$$

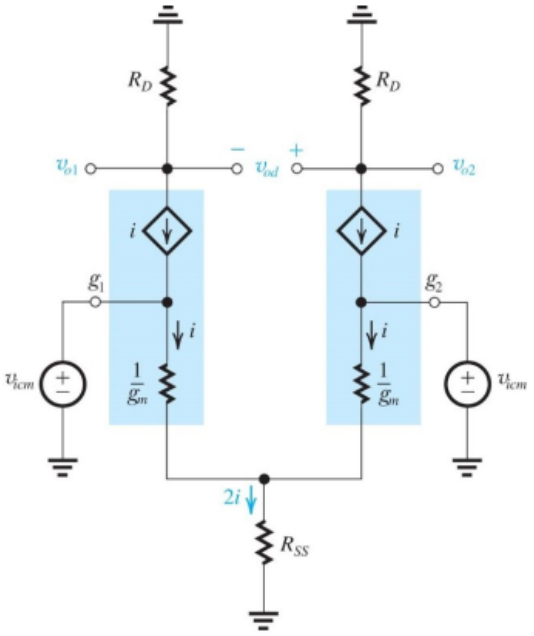
- Common mode gain, A_{cm}
  - Arises from mismatch

$$A_{cm} = \left(\frac{-R_D}{2R_{SS}}\right)\left[\left(\frac{\Delta R_D}{R_D}\right) + \left(\frac{\Delta g_m}{g_m}\right)\right]$$

- Common mode rejection ratio (CMRR)
  - Ratio of differential to common mode gain

$$CMRR = \frac{A_d}{A_{cm}} = \frac{-2g_m R_{SS}}{\left(\frac{\Delta R_D}{R_D}\right) + \left(\frac{\Delta g_m}{g_m}\right)}$$





Device matching and high current source resistance keeps CMRR high.

➢ To keep CMRR high, we have to use a biasing current source with a high output resistance R_{SS} and, of course, strive to maintain a high degree of matching between Q_1 and Q_2.

DC Offset

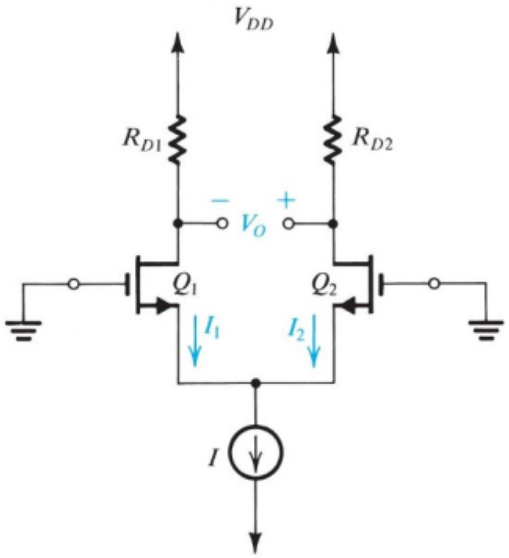
- Because differential amplifiers are directly coupled and have finite gain at dc, they suffer from a number of dc problems

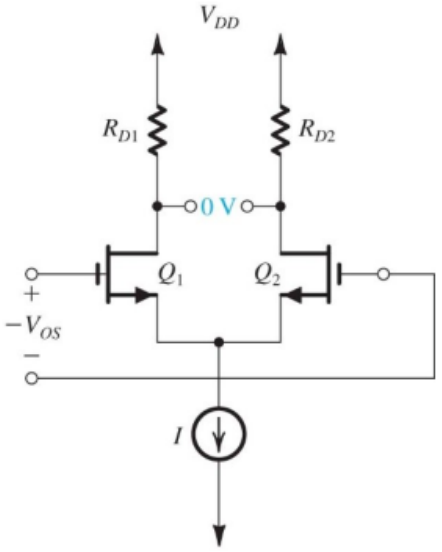
- Imperfectly balanced pair…
  - Unequal load, $\Delta R_D = R_{D1} - R_{D2}$
  - Unequal size, $\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$
  - Unequal threshold, $\Delta V_{tn} = V_{tn1} - V_{tn2}$
  - …

- Output non-zero at zero input, as current not balanced

- Input referred offset voltage, V_{OS}
  - Input that cancels offset

$$V_{OS} = \frac{V_O|_{V_{Id}=0}}{A_d}$$



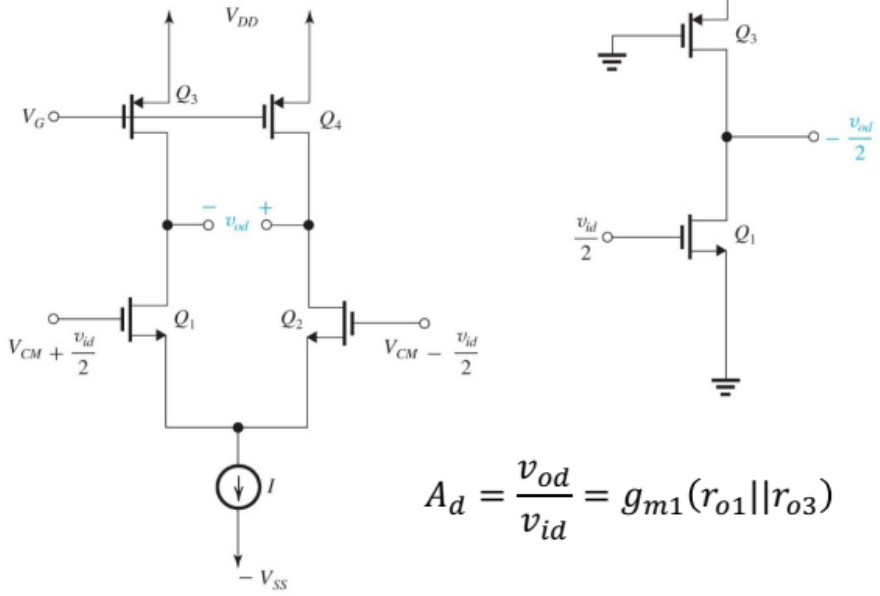


$$V_{OS} \approx \sqrt{\sum_n (V_{OSn})^2} = \sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}\right)^2 + (\Delta V_{tn})^2}$$

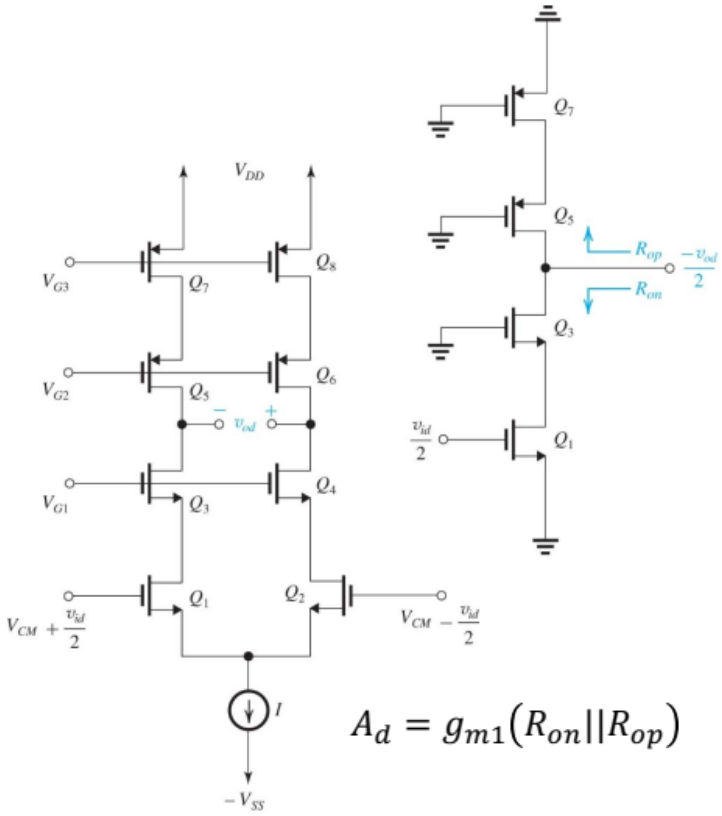
- V_O: output dc offset voltage
- V_{OS}: input offset voltage

MOS Differential Pair with Active Load

- Improved performance as compared to passive load, essentially a differential CS amplifier w/ active load

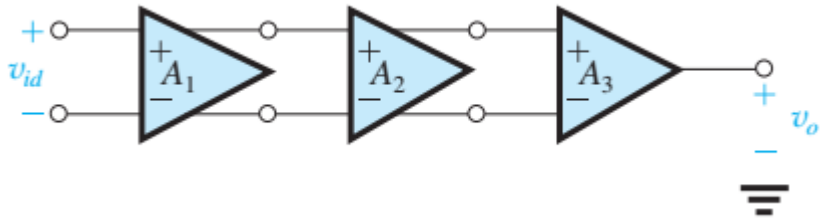


$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1}||r_{o3})$$

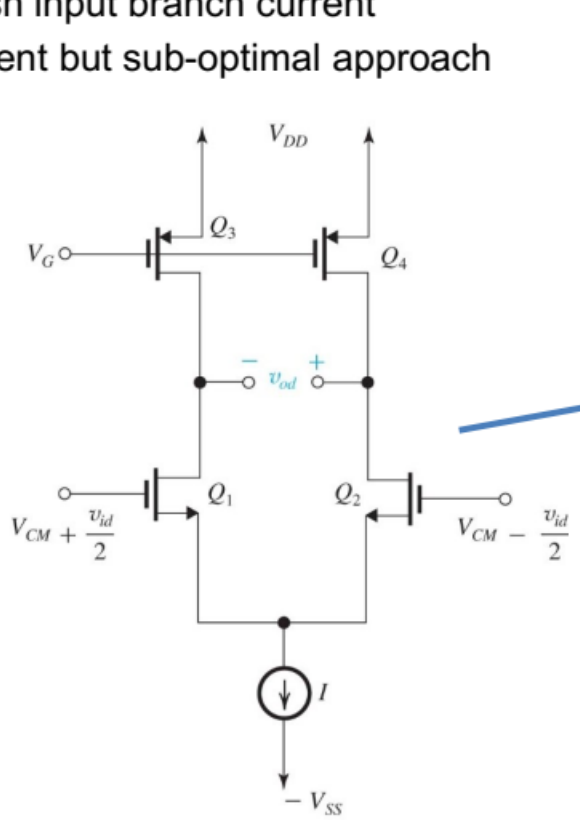


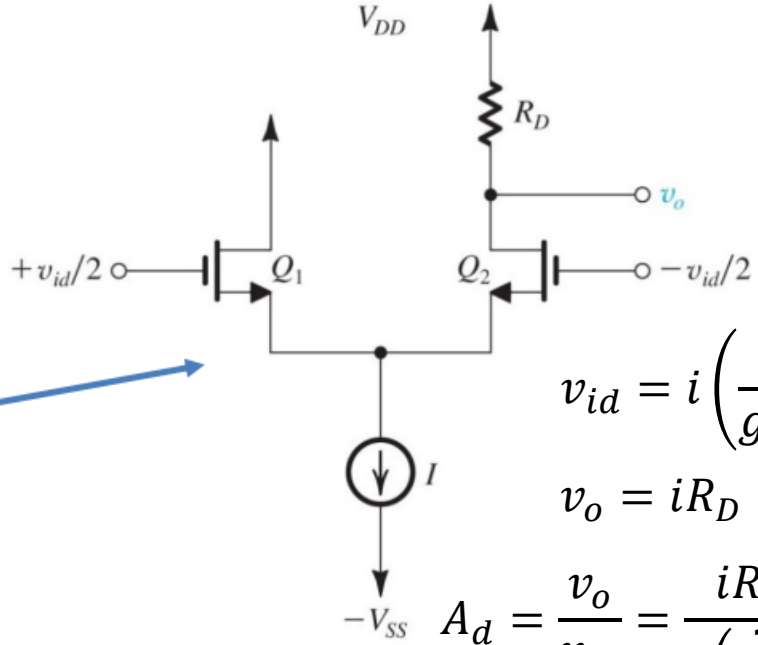
$$A_d = g_{m1}(R_{on}||R_{op})$$

Differential to Single Ended Conversion



- Option 1: Trash input branch current
  - A convenient but sub-optimal approach





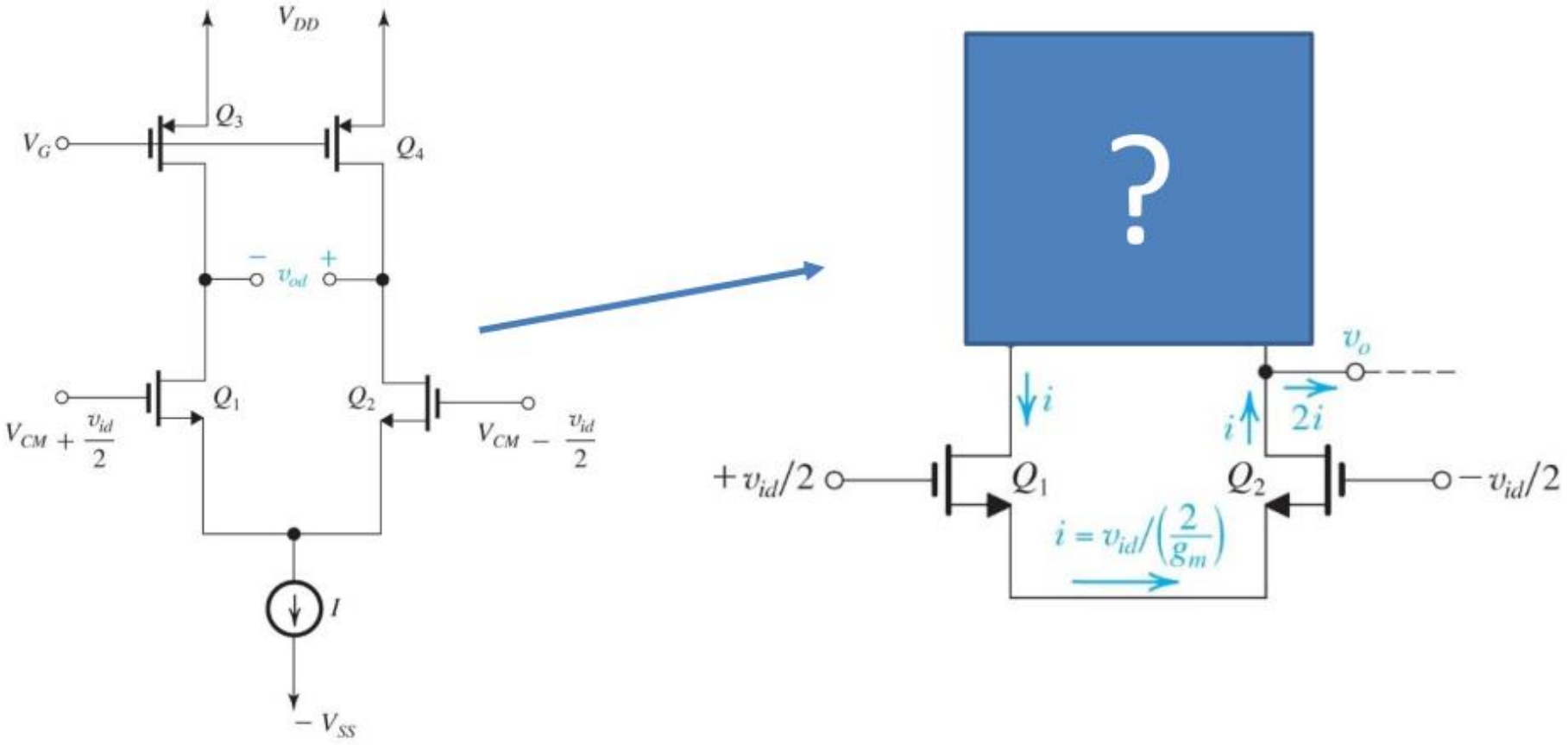
$$v_{id} = i\left(\frac{2}{g_m}\right)$$

$$v_o = iR_D$$

$$A_d = \frac{v_o}{v_{id}} = \frac{iR_D}{i\left(\frac{2}{g_m}\right)} = \frac{g_m R_D}{2}$$

Although successfully converting to single ended, half of the signal current is lost to the supply.

How to reflect differential pair input branch current to output branch?



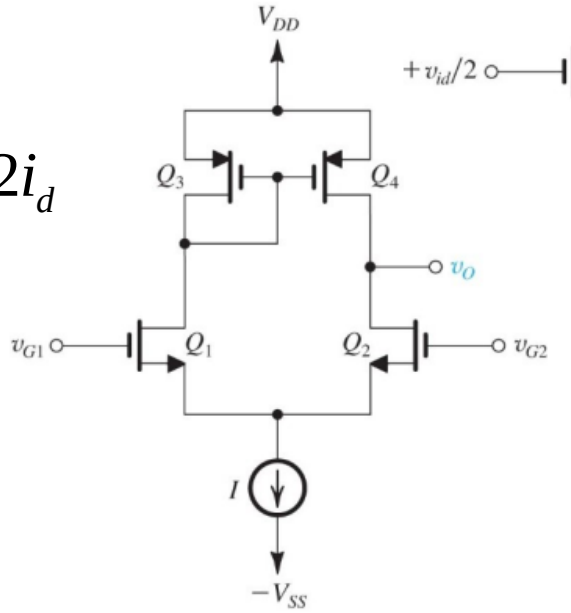
MOS Differential Amplifier with Current Mirror Load

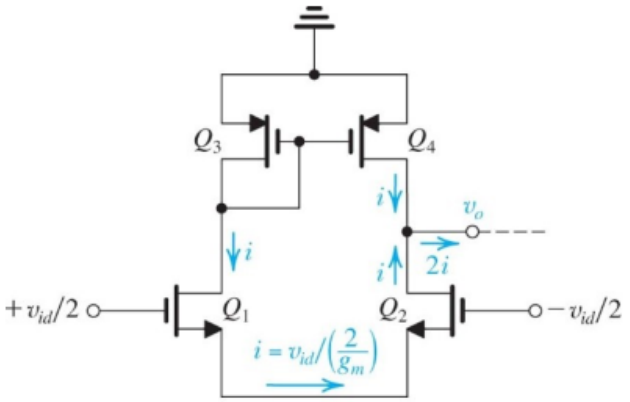
- Option 2: Mirror current to output
  - Superimposes both branch currents
- KCL "magic" at output node
  - Differential mode currents cleverly forced into load

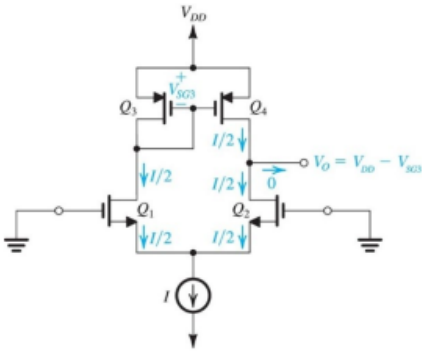
$$i_{od} = \frac{I}{2} + i_d - \left(\frac{I}{2} - i_d\right) = 2i_d$$

  - Common mode and dc currents must ignore load

$$i_{CM} = \frac{I}{2} + i_{cm} - \left(\frac{I}{2} + i_{cm}\right) = 0$$





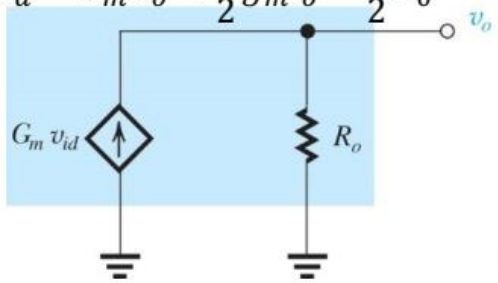


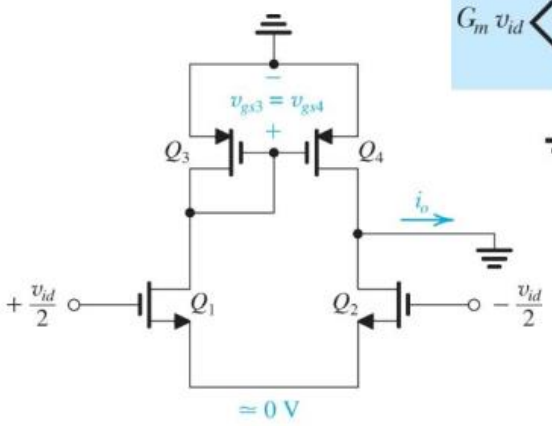
Current mirror does not load the differential pair symmetrically.

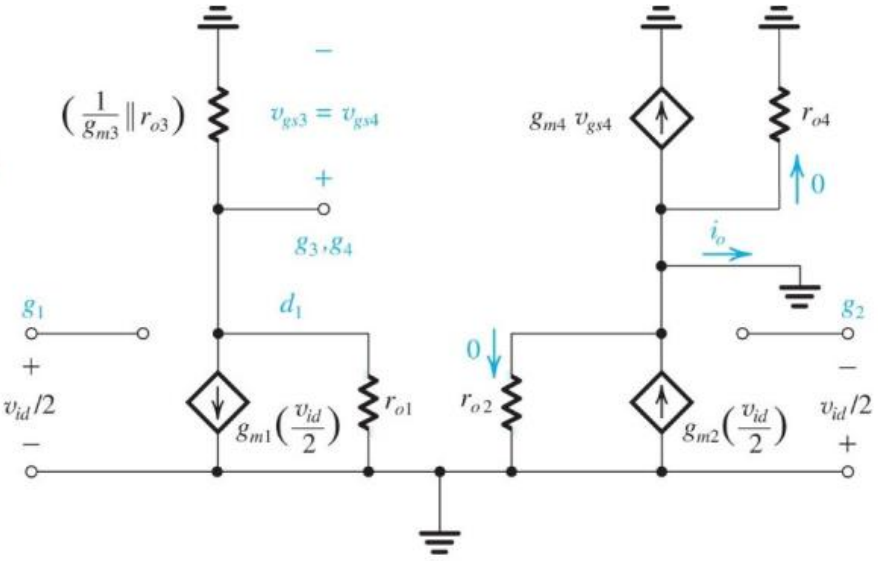
Differential Amplifier: Short Circuit Transconductance

- Identify equivalent transconductance amplifier
  - Infinite input resistance
  - Transconductance
  - Finite output resistance

$$A_d = G_m R_o \approx \frac{1}{2} g_m r_o = \frac{1}{2} A_0$$







$$G_m \equiv \frac{i_o}{v_{id}} \qquad G_m = g_m$$

$$R_o = r_{o2} \| r_{o4}$$

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_{m1,2}(r_{o2} \| r_{o4})$$

$$r_{o2} = r_{o4} = r_o$$

$$A_d = \frac{1}{2} g_m r_o = \frac{1}{2} A_0$$

$$v_{gs3} = -g_{m1}\left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}} \| r_{o3} \| r_{o1}\right)$$

$$v_{gs3} \simeq -\frac{g_{m1}}{g_{m3}}\left(\frac{v_{id}}{2}\right) \qquad \frac{1}{g_{m3}} \ll r_{o3},\ r_{o1}$$

$$i_o = g_{m2}\left(\frac{v_{id}}{2}\right) - g_{m4}\, v_{gs4}$$

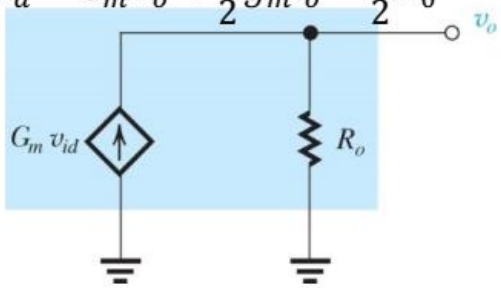
$$i_o = g_m v_{id} \qquad g_{m3} = g_{m4} \text{ and } g_{m1} = g_{m2} = g_m$$

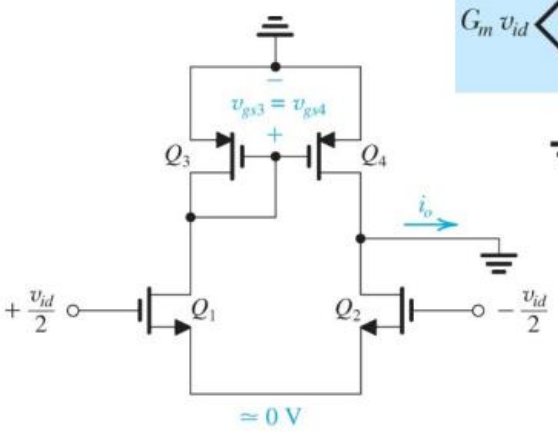
where A_0 is the intrinsic gain of the MOS transistor.

Differential Amplifier: Output Resistance

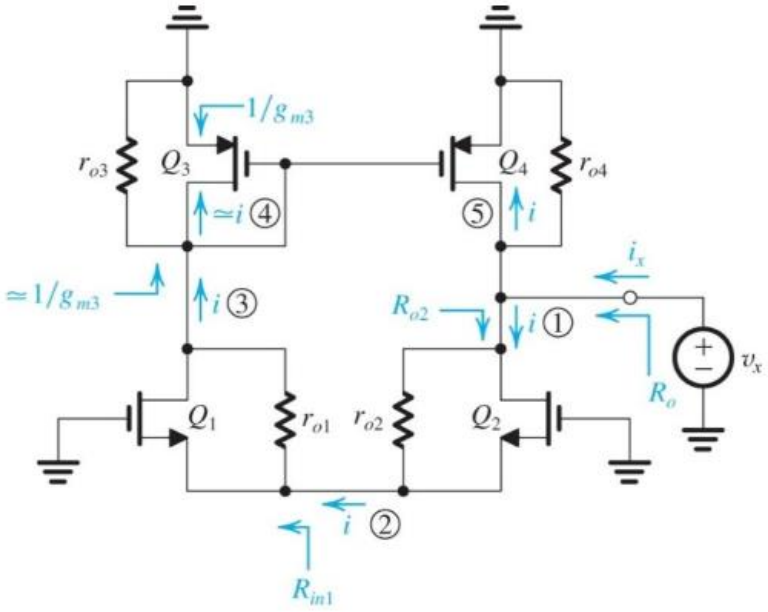
- Identify equivalent transconductance amplifier
  - Infinite input resistance
  - Transconductance
  - Finite output resistance

$$A_d = G_m R_o \approx \frac{1}{2} g_m r_o = \frac{1}{2} A_0$$





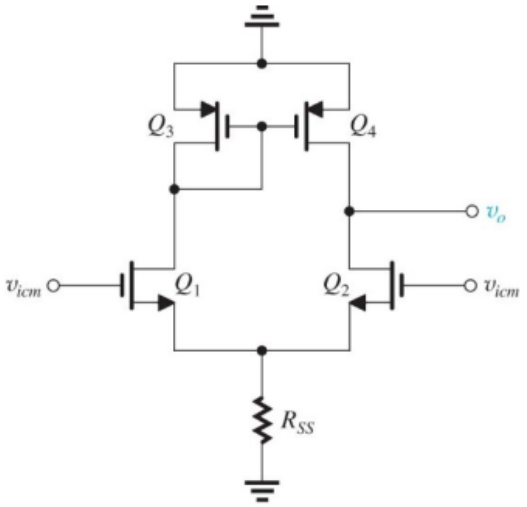
$$R_o = \frac{v_x}{i_x} \approx (r_{o2} || r_{o4})$$

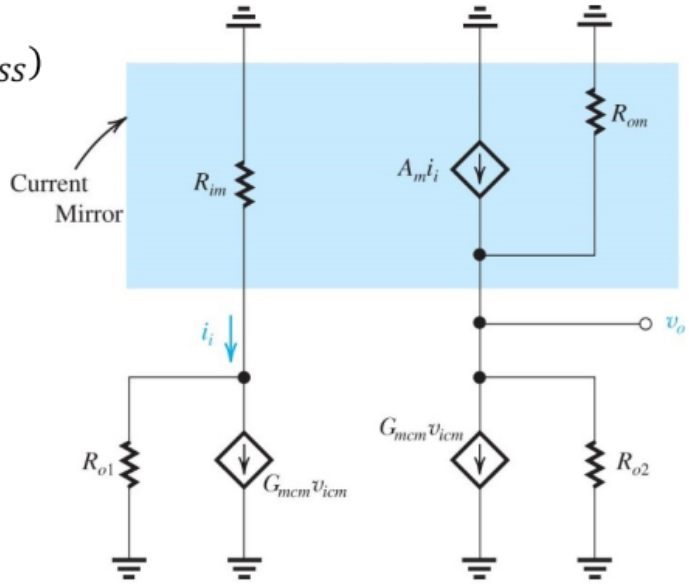


Differential Amplifier: Common Mode Gain and CMRR

- Asymmetrical loading
  - Diode connected transistor
  - Common source transistor
- Mirror approximately buffers current
- Common gate source/ load transformations useful

$$CMRR = \frac{A_d}{A_{cm}} \approx -(g_m r_o)(g_m R_{SS})$$





$$A_d = \frac{v_{od}}{v_{id}} = G_m R_o \approx g_m (r_{o2} || r_{o4})$$

$$A_{cm} = \frac{v_o}{v_{icm}} = -(1 - A_m) G_{mcm} (R_{om} || R_{o2}) \approx \frac{-1}{2 g_m R_{SS}}$$

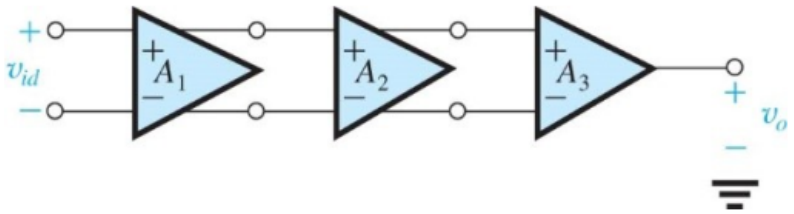
$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} = [g_m (r_{o2} \| r_{o4})][2 g_{m3} R_{SS}] \quad \text{which for } r_{o2} = r_{o4} = r_o \text{ and } g_{m3} = g_m \text{ simplifies to}$$

$$\text{CMRR} = (g_m r_o)(g_m R_{SS})$$

➢ We observe that to obtain a large CMRR, we select an implementation of the biasing current source *I* that features a high output resistance. Such circuits include the cascode current source and the Wilson current source

Multistage Amplifiers

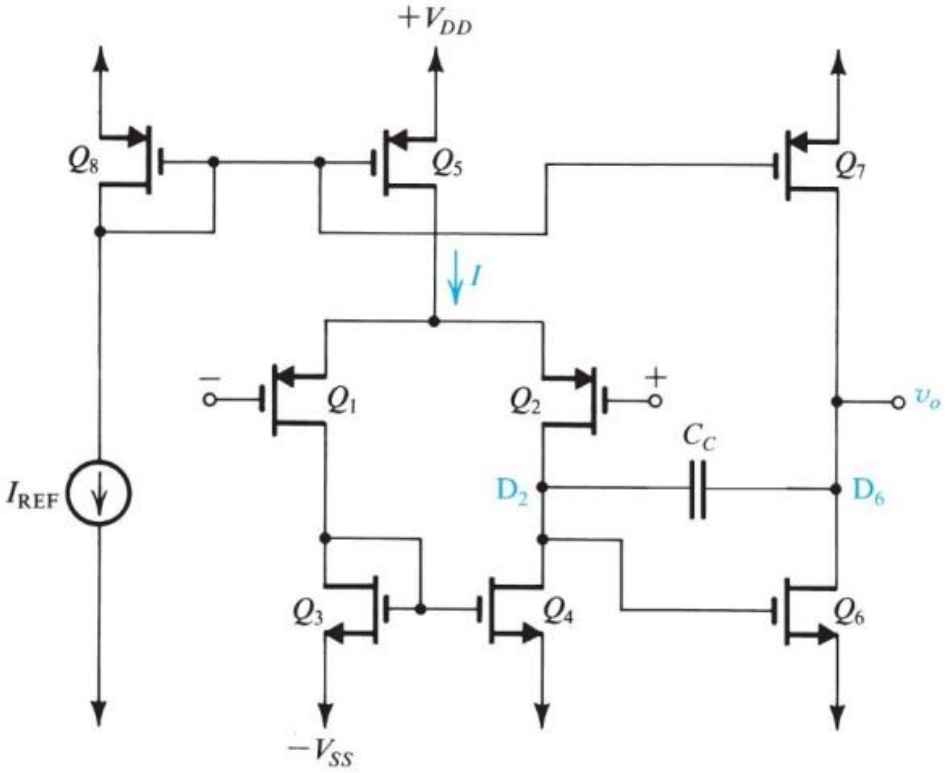
- Multistage seen as functional blocks
  - Noise/ CM rejection
  - Signal gain (small signal)
  - Power (linearity)
- Differential input and interstage
  - Differential gain
  - CM (noise or interference) rejection
- Single ended output stages
  - Gain and power level
  - Resistance transformation
- Single ended output typically
  - Load to ground



Multistage amplifier is co-desiged system, its stages dedicated to specific tasks.

Two-Stage CMOS Op Amp

- Bias current steering circuit
- Input stage: differential PMOS pair
  - Gain and single ended conversion
  - NMOS current mirror load
- Output stage: common source NMOS
  - Gain w/ active load
- Stability
  - Frequency compensation feedback capacitor
- Compact, moderate gain, but rather high output impedance



Two-Stage CMOS Op Amp

- A reference bias current I_{REF} is generated either externally or using on-chip circuits. The current mirror formed by Q_8 and Q_5 supplies the differential pair Q_1-Q_2 with bias current. The W/L ratio of Q_5 is selected to yield the desired value for the input-stage bias current I (or $I/2$ for each of Q_1 and Q_2). The input differential pair is actively loaded with the current mirror formed by Q_3 and Q_4.
- The second stage consists of Q_6, which is a common-source amplifier loaded with the current-source transistor Q_7. A capacitor C_C is included in the negative-feedback path of the second stage. Its function is for the frequency compensation.
- The voltage gain of the first stage is to be given by:

$$A_1 = -g_{m1}(r_{o2} \| r_{o4})$$

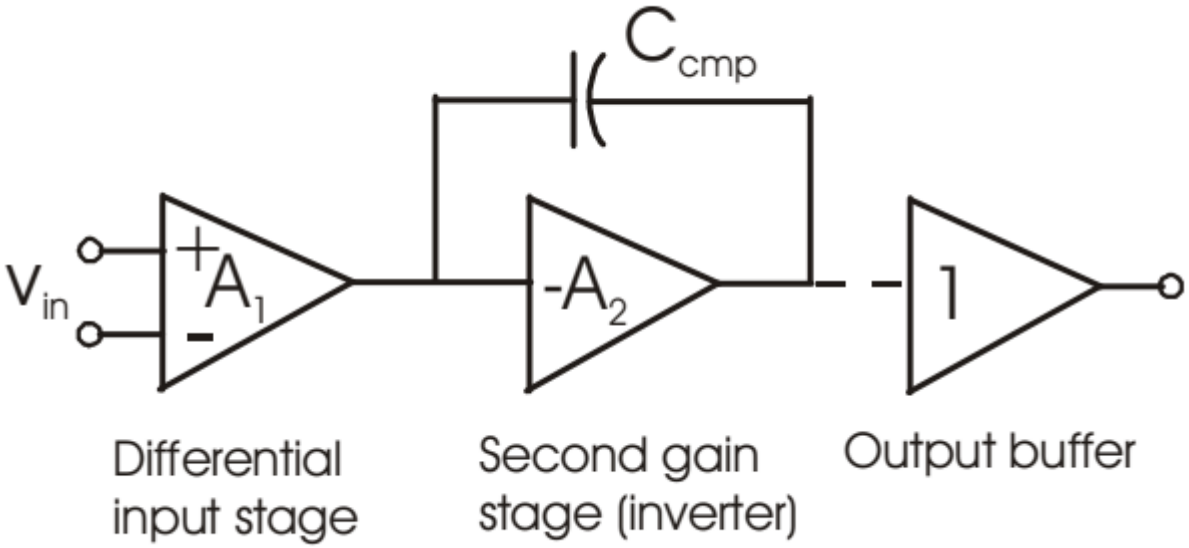
where g_{m1} is the transconductance of each of the transistors of the first stage, that is, Q_1 and Q_2.

- The second stage is a current-source-loaded, common-source amplifier whose voltage gain is given by:

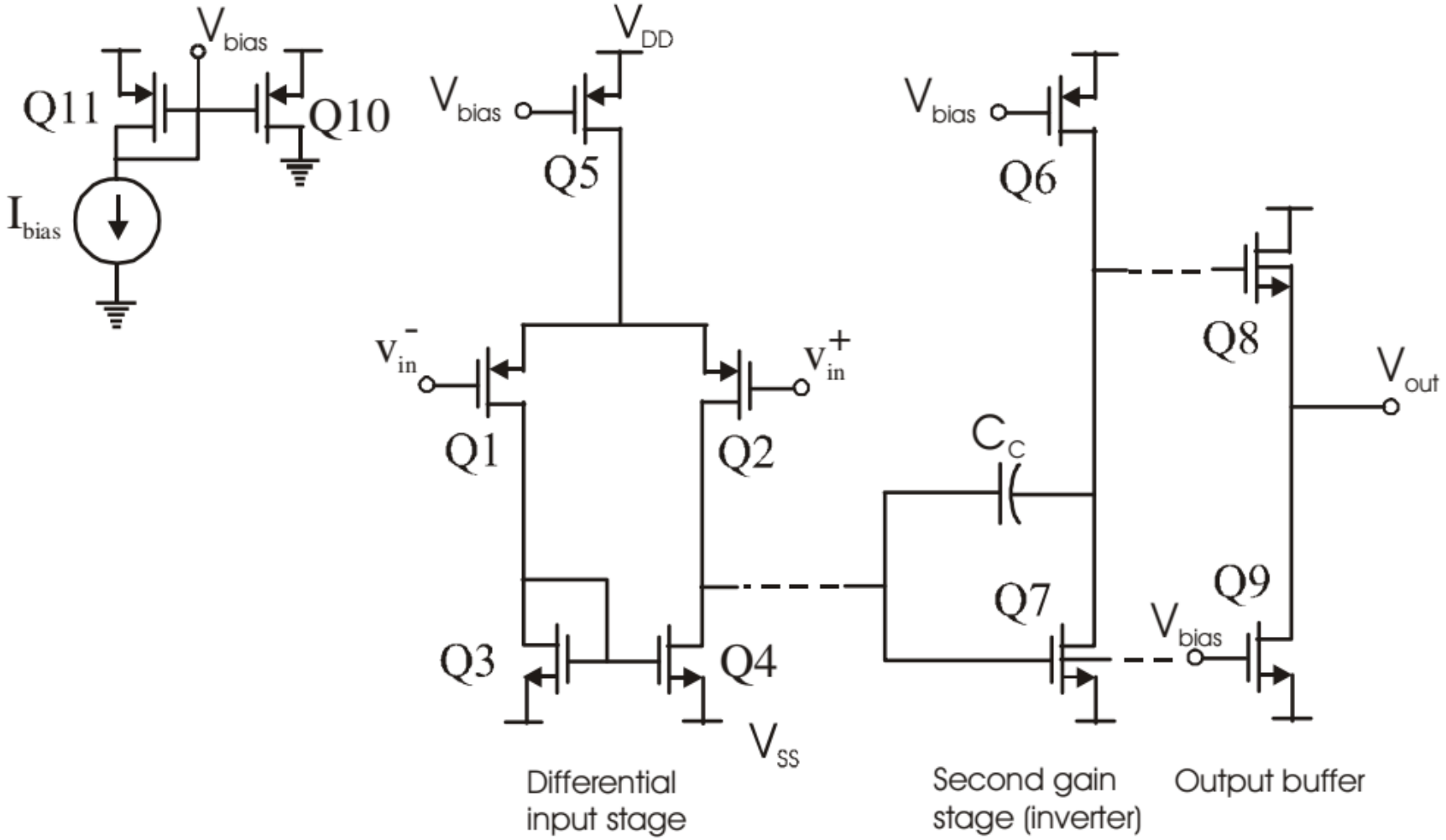
$$A_2 = -g_{m6}(r_{o6} \| r_{o7})$$

- The dc open-loop gain of the op amp is the product of A_1 and A_2

Two-Stage CMOS Op Amp

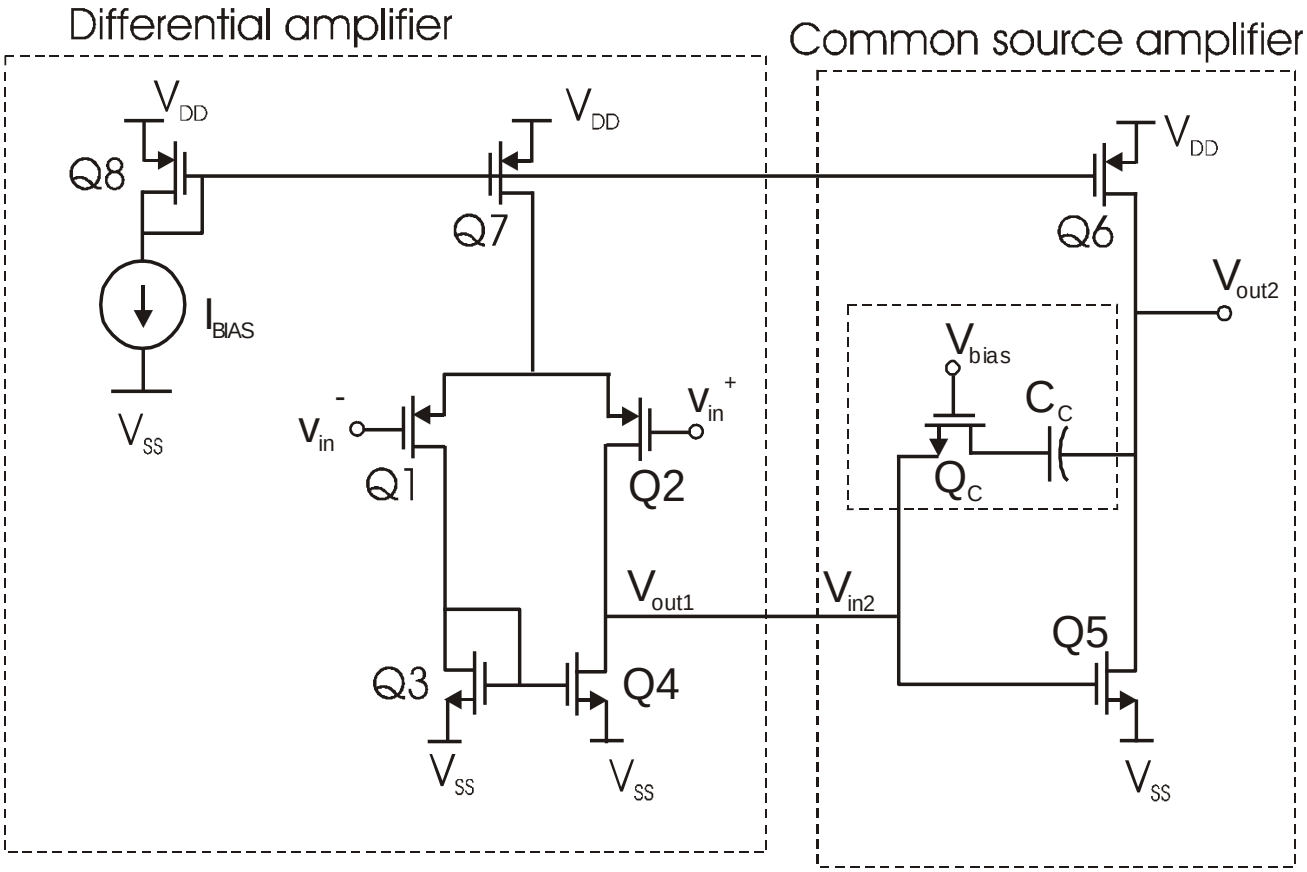


Two-Stage CMOS Op Amp



- Capacitor C_{cmp} is included to ensure stability when the opamp is used with feedback

Two-Stage CMOS Op Amp



- Capacitor C_c and transistor Q_c (acting as a voltage controlled resistor) are included for Op-amp compensation to ensure stability when the Op-amp is used with feedback