Harris

CMOS VLSI Design

Lab 2: Full Adder Design

In this lab, you will design a full adder at the schematic and layout levels. As with all labs, read the whole writeup thoroughly before starting to avoid surprises.

1. Full Adder

The objective of this lab is to complete a design of a nontrivial circuit, a full adder. Recall that a full adder accepts three inputs and computes a sum and a carry out. The truth table in Table 1 shows the operation of a full adder. There are many ways to approach this problem. You may assemble your adder from various simpler logic gates or may design it as a single complex cell. If you use logic gates, try to think in terms of NANDs and NORs rather than ANDs and ORs; you'll save transistors. Refer to your textbooks for further references on full adders. Here you can refer Page 429-434 in textbook "CMOS VLSI design 4th Edition". Warning: at least one of the figures in the 2nd edition of Principles of CMOS VLSI Design regarding adders is incorrect. Be certain you understand a design before blindly copying it!

Table 1 Full adder truth table

a	*b*	*c*	*cout*	$\overline{cout}$	*sum*
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	0	1

$$cout = bc + ac + ab + abc = c(a + b) + ab(1 + c) = c(a + b) + ab$$

$$sum = c\overline{cout} + b\overline{cout} + a\overline{count} + abc = (a + b + c)\overline{cout} + abc$$

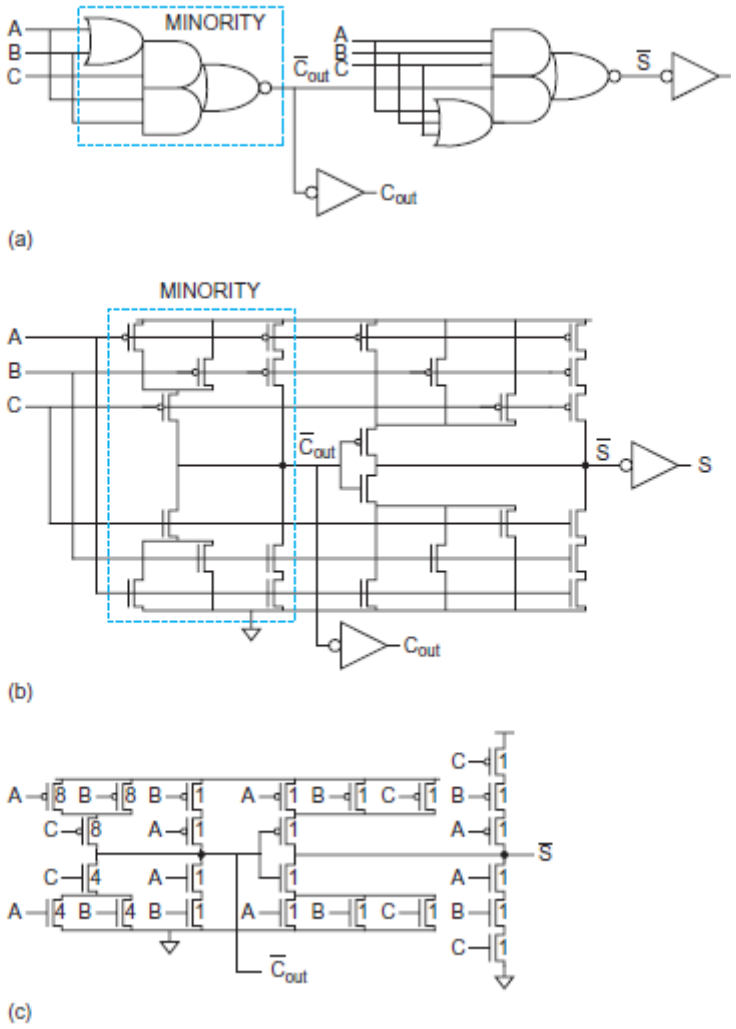

Figure 1 Full adder for carry-ripple operation (in Page 432 in Ref textbook "CMOS VLSI design 4th Edition")

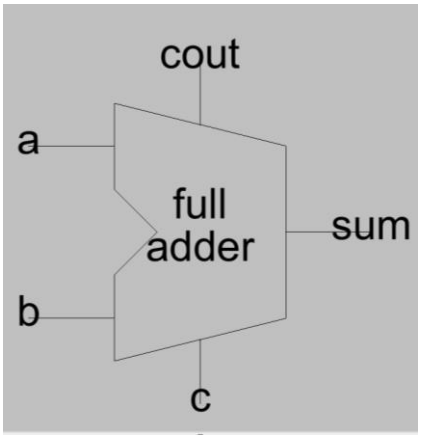

Figure 2. The IC symbol of the full adder

Copy your lab1_xx library to lab2_xx for this lab.

2. Schematics

Draw schematics of the adder in fulladder {sch}. You may use the schematic in Fig.1. Name the inputs *a*, *b*, and *c* and the outputs *sum* and *cout* to match the fulladder{ic} provided in Fig.2. It may be helpful to label the internal wires in the schematic so they have meaningful names in case you need to debug later.

3. IRSIM Simulation(optional)

It is wise to simulate your schematic to verify it works before proceeding to the time-consuming layout process. Take advantage of IRSIM command files in your simulation. A sample `fulladder.sim` file is in the lab directory. It includes tests of four of the input combinations. Open the command file with a text editor and look it over. The syntax of the command file is:

h sig:	set sig high (logic 1)
l sig:	set sig low (logic 0)
s [time]:	simulate (for [time] nanoseconds, otherwise use default step)
assert sig val:	check that sig has the value val. Emit warning if it does not
x signal:	set signal to invalid level

Assertions are very useful for larger designs because they allow automatic testing of your design without inspecting the waveforms for correctness. Signals retain the last value they were assigned if not explicitly changed.

Modify the command file to include the other input combinations with appropriate assertions. Be sure the file is in the same working directory with your lab 2 library. To invoke the command file, start IRSIM on your fulladder{sch}. Use the IRSIM: Simulate Deck... command to read your fulladder.cmd. Note: if these commands do not appear in the menu, then IRSIM has not been installed. Check the waveforms to verify that you obtain the correct sum and carry outputs.

4. Layout

Draw a layout of your adder in fulladder{lay}. You may wish to look at other layouts in the library to see examples. The layout should obey the same constraints as your gates from Lab 1:

- power and ground run horizontally in Metal 2 on a 80λ center-to-center spacing
- all transistors, wires, and well contacts fit between the power and ground lines
- all transistors should be within 100λ of a well contact
- avoid long routes in diffusion

- *a* and *b* appear on left side of layout in metal1
- *sum* appears on right side of layout in metal1
- *c* appears near the bottom of a cell in metal1
- *cout* appears near the top of the cell directly above *c* in metal1
- metal 2 use is acceptable, but leave space for at least five horizontal metal2 lines to run over the top of the cell

Remember that you will have to connect *cout* of one adder to *c* of the next when you assemble a ripple carry adder next lab. Therefore, don't place any obstructions that would prevent the connections. *cout* output will be vertically connected to the *c* of next full adder directly above it. There should be no metal1 arcs below *c* or above *cout*.

You may find it necessary to add a large rectangle of N-well or P-well to surround your transistors and eliminate spacing problems. To do this, click on the "Pure" entry of the Components tab and select "N−Well−Node" or "P−Well−Node" and double-click on the well to set the size. Pure layer nodes don't offer connectivity information to Electric, so use them only for wells.

Use IRSIM to simulate your adder layout. Use the same command file that you created for the schematic simulation.

Check your layout with DRC, ERC, and NCC.

5. What to Turn In

Please provide a hard copy of each of the following items:

1. Please indicate how many hours you spent on this lab. This will not affect your grade, but will be helpful for calibrating the workload for the future.
2. A printout of your fulladder schematic (and any subcells, if applicable).
3. A printout of your fulladder layout.
4. A single page of simulation waveforms demonstrating correct operation of the fulladder layout.
5. What is the verification status of your layout? Does it pass DRC? ERC? NCC?

Optimization Contest

A prize will be given for the best full adder design. This primarily means smallest area. However, easy access to inputs and outputs and clean layout are also important.