VLSI

Lab 1

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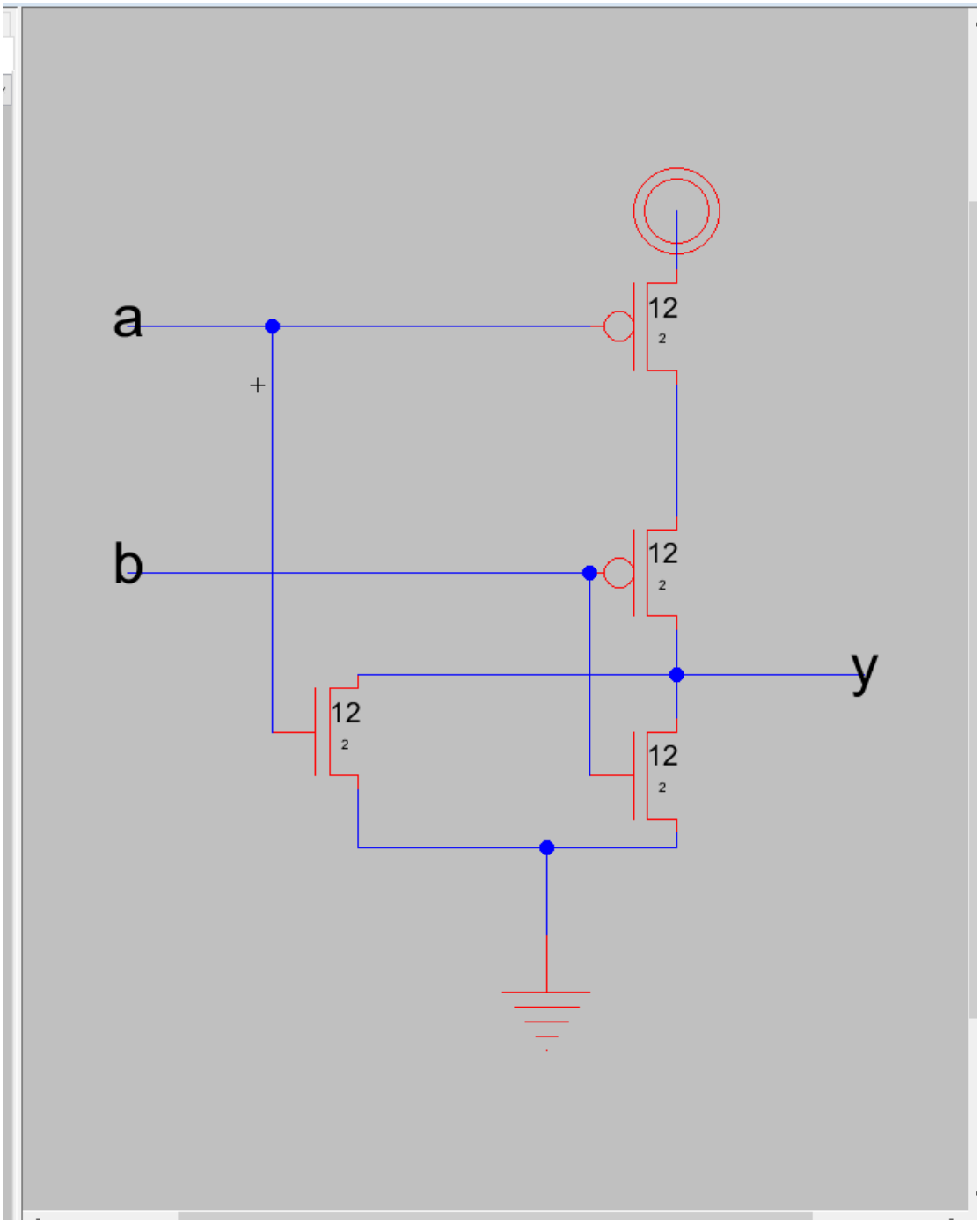
1.

I only figure out how to make schematic in the lab session, and I spend 3 day's leisure time, to get familiar with the software and the layout, not to mention the time on lecture notes.

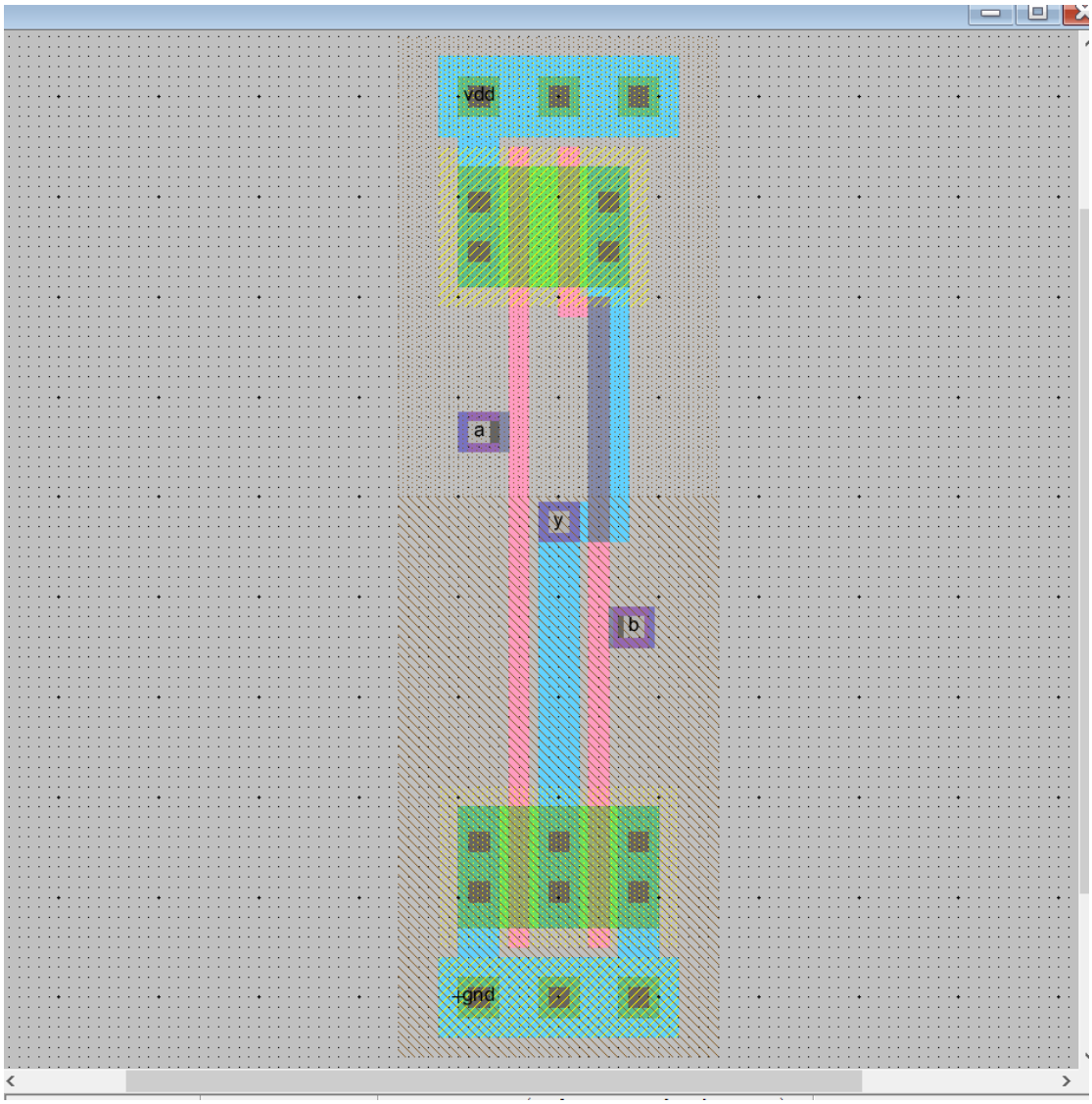
2.

NOR2 schematic:



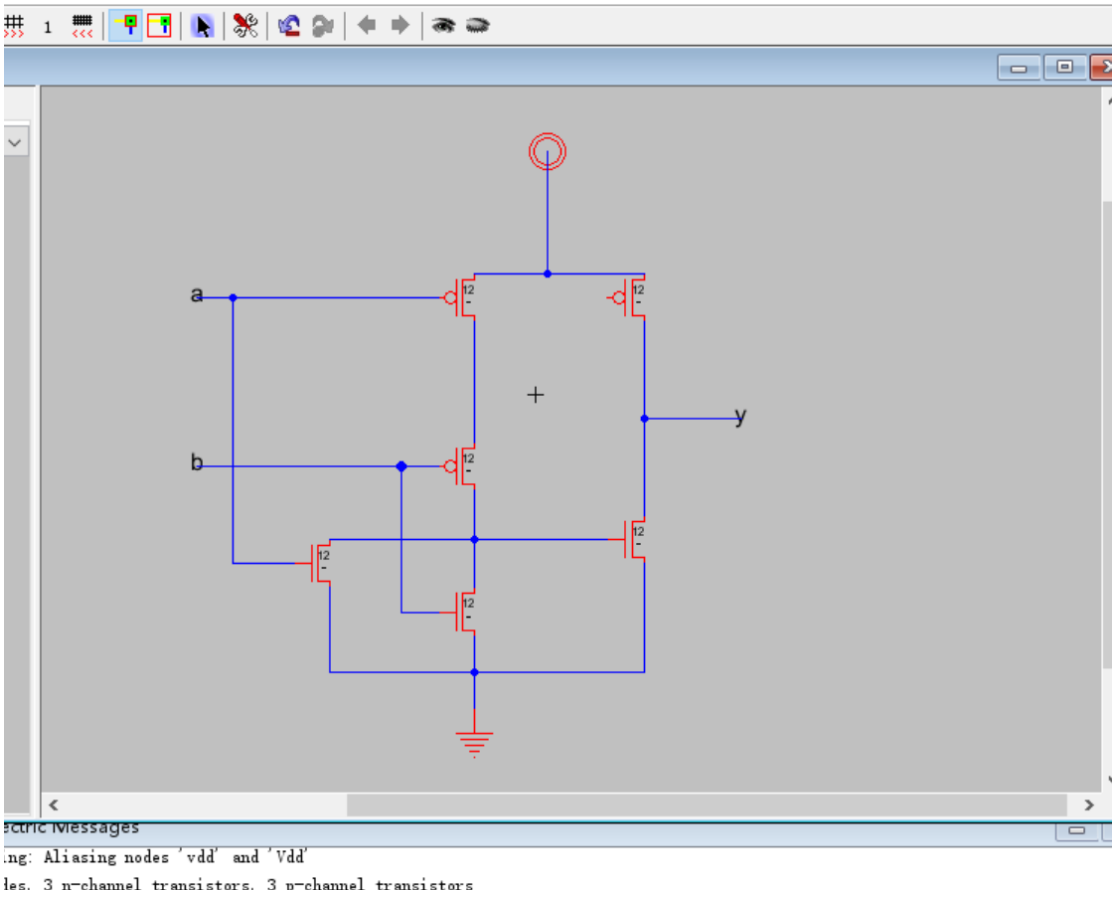
3.

NOR2 layout:



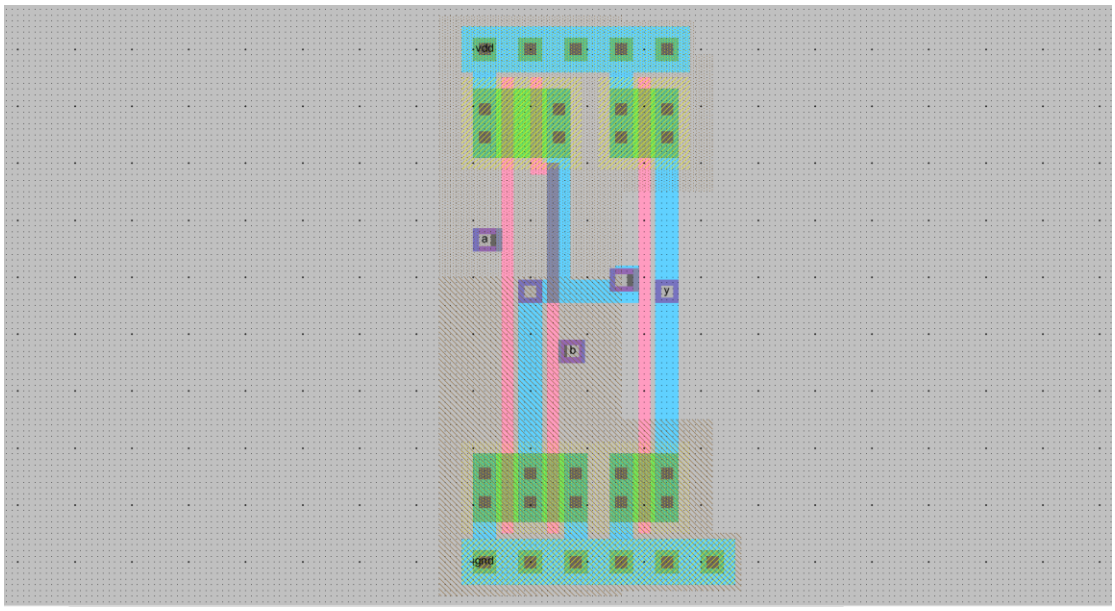
4.

OR2 schematic:

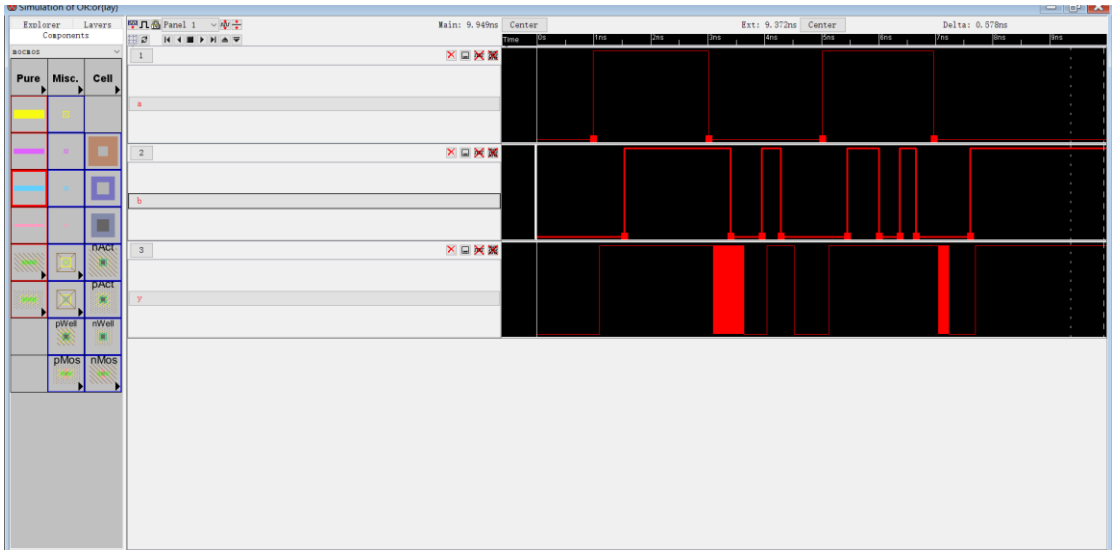


5.

OR2 layout:



6.


Explorer
Layers
Components
Pure
Misc.
Cell
nAct
pAct
pWell
nWell
pMos
nMos
Panel 1
Main: 9.949ns
Center
Ext: 9.372ns
Center
Delta: 0.578ns
Time
1
a
2
b
3
y