# VLSI design Analog Lab 2: Layout Design

## Objective

Learn techniques for successful integrated circuit layout design.

## Introduction

In this lab you will learn in detail how to generate a simple transistor layout. Next, techniques will be developed for generating optimal layouts of wide transistors and matched transistors. Layout techniques for resistors and capacitors will also be illustrated. Finally, you will use all of these layout techniques to produce a two-stage opamp layout (Lab 3).

## Layout Techniques

Transistors

In Lab 1 you learned how to layout small size transistors. Most analog designs will not be limited to these small width transistors, thus special layout techniques need to be learned to layout large width MOSFETS. Luckily, wide transistors can be broken into parallel combinations of small width transistors as seen in Figure 1-1. By doing this horizontal expansion technique for the wide transistor, the drain and source area can be reduced which decreases parasitic capacitance and resistance.

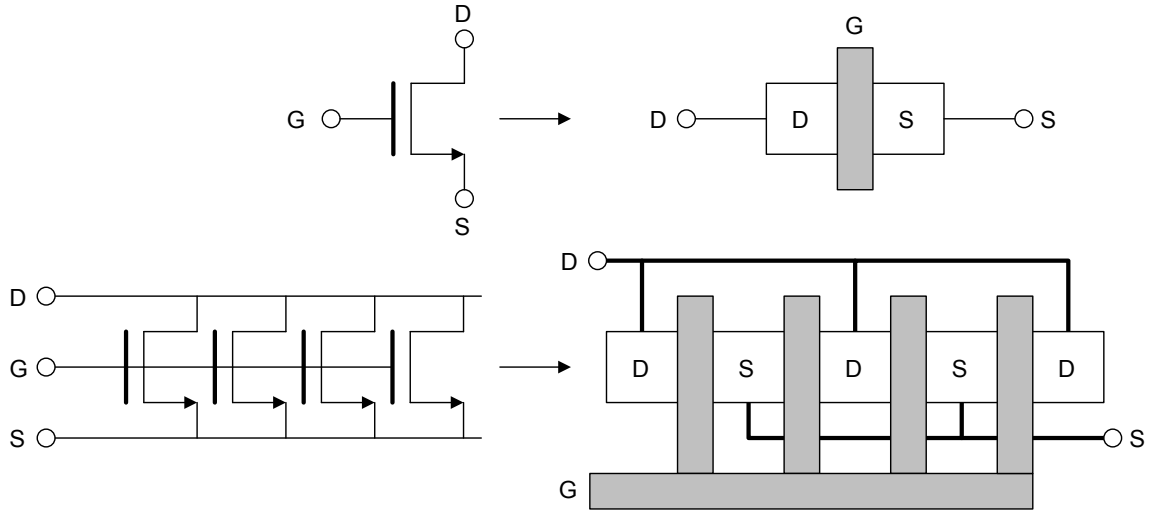


**Figure 1-1: Wide MOS transistor layout**

Another good layout technique is to use "dummy" transistors on both ends of a transistor layout. These dummy transistors insure that the etching and diffusion processes occur equally over all segments of the transistor layout(Fig.1-2).

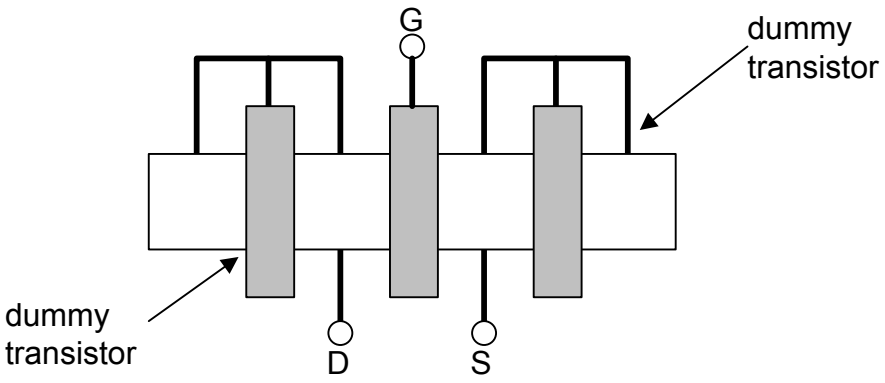


**Figure 1-2: Dummy transistor layout**

Notice the gate, drain, and source are connected together which keeps it from conducting any current. This shorted transistor is connected to the drain or source of the functional transistor. Another alternative for dummy transistors is to have the gate and source tied together.

When laying out any device the key is symmetry, especially when laying out fully-differential components. For matched devices, use interdigitized or common-centroid layout techniques. A matched device is one where two transistors need to have exactly the same geometries. Examples include current mirrors and differential pairs.

An interdigitized layout is shown in Figure 1-3. Notice that the two transistors have been split into smaller size devices and interleaved. This layout minimizes the effects of process variations on the parameters of the transistors.

The idea behind splitting a transistor up is to average the process parameter gradient over the area of the matched devices. For example, the process variation of KP and of the transconductance parameter on the wafer is characterized by a global variation and a local variation. Global variations appear as gradients on the wafer as in Figure 1-4. However, local variations describe the random change in the parameter from one point on the chip to another nearby point. By using layout techniques such as interdigitized and common-centroid, the process variation can hopefully be averaged out among the matched devices.

When laying out wider matched transistors the common-centroid layout may be a better choice. This layout technique is illustrated in Figure 1-5 for the case of 8 matched M1 and M2 transistors of a differential pair.

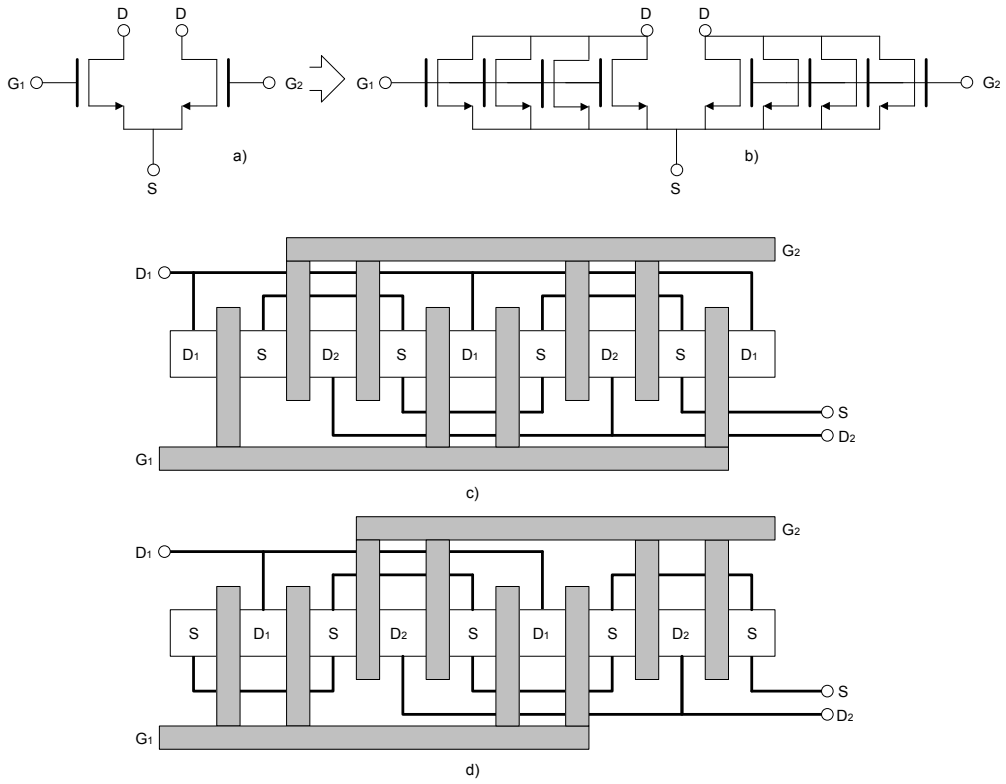


**Figure 1-3: Interdigitized layout of a differential pair**

**a) Differential pair**
**b) Horizontal expansion**
**c) Interdigitized layout (Drain areas are different. Common centroid.)**
**d) Interdigitized layout (Drain areas are equal. Not common centroid.)**

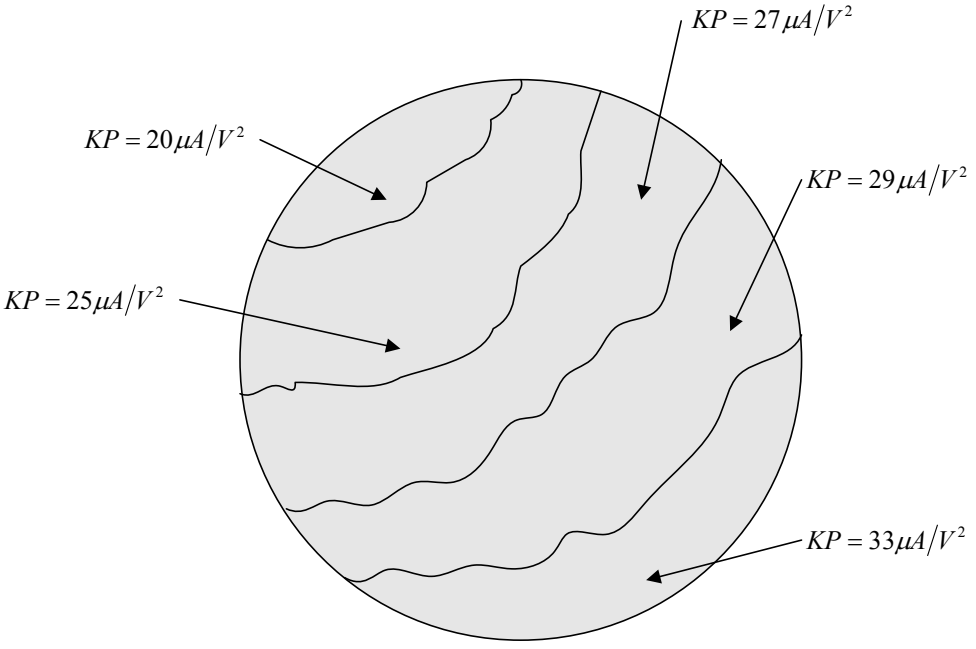


**Figure 1-4: Gradient of KP on a wafer**

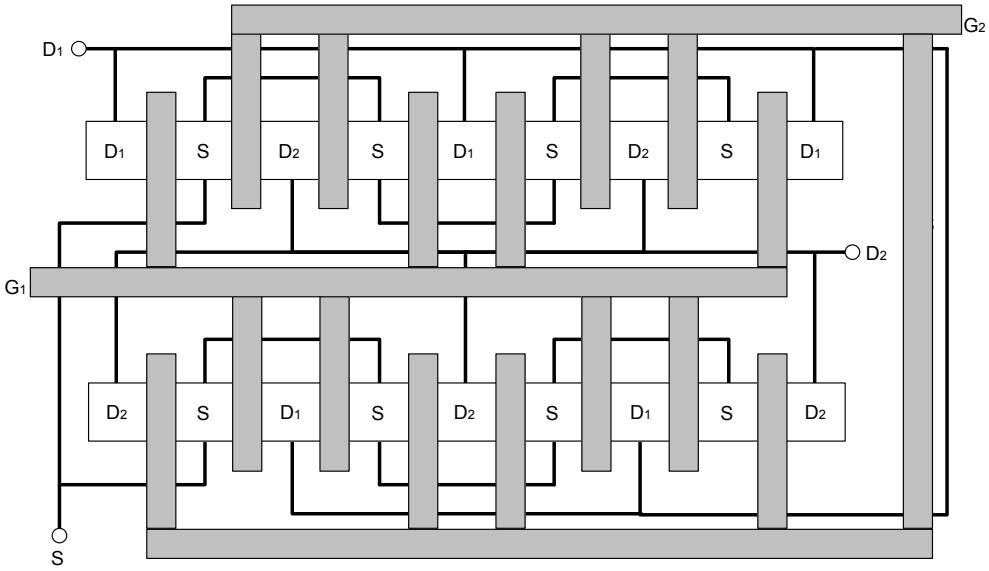


**Figure 1-5: Common-centroid layout of a differential pair**

The idea behind the common-centroid layout is to average linear processing gradients that affect the transistors' electrical properties. Common-centroid layouts should have the centroid (center of mass) of each transistor positioned at the same location. The following examples illustrate what is common-centroid and what is not common-centroid.

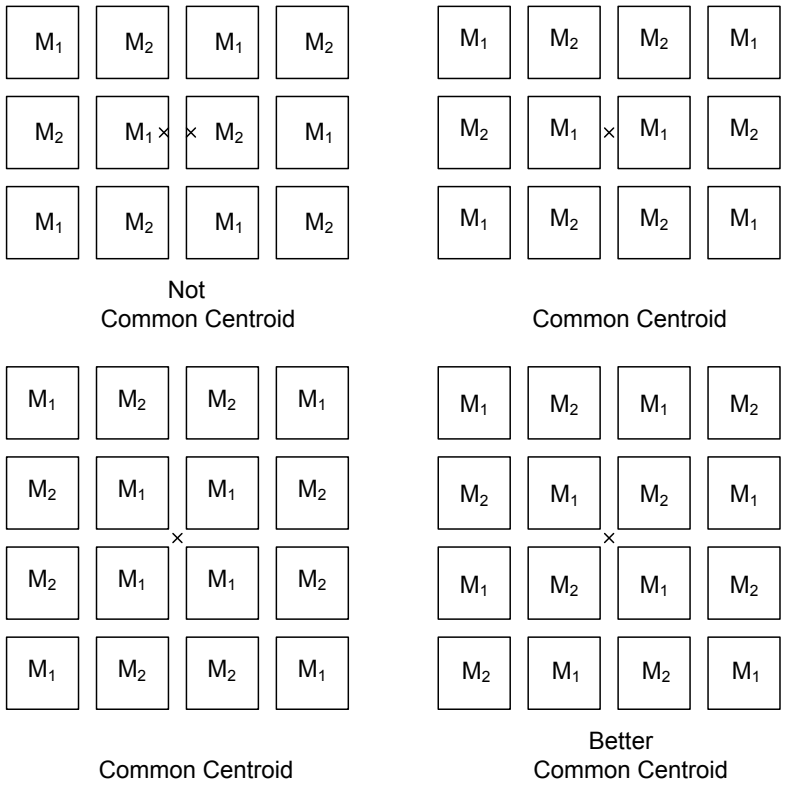


**Figure 1-6: Common-centroid examples**

Capacitors

Capacitors of various types can be fabricated on integrated circuits. A capacitor is formed when an insulator separates two conducting sheets. Two methods of forming capacitors are by using poly and poly2 (elec layer in LSW) as the capacitor plates.

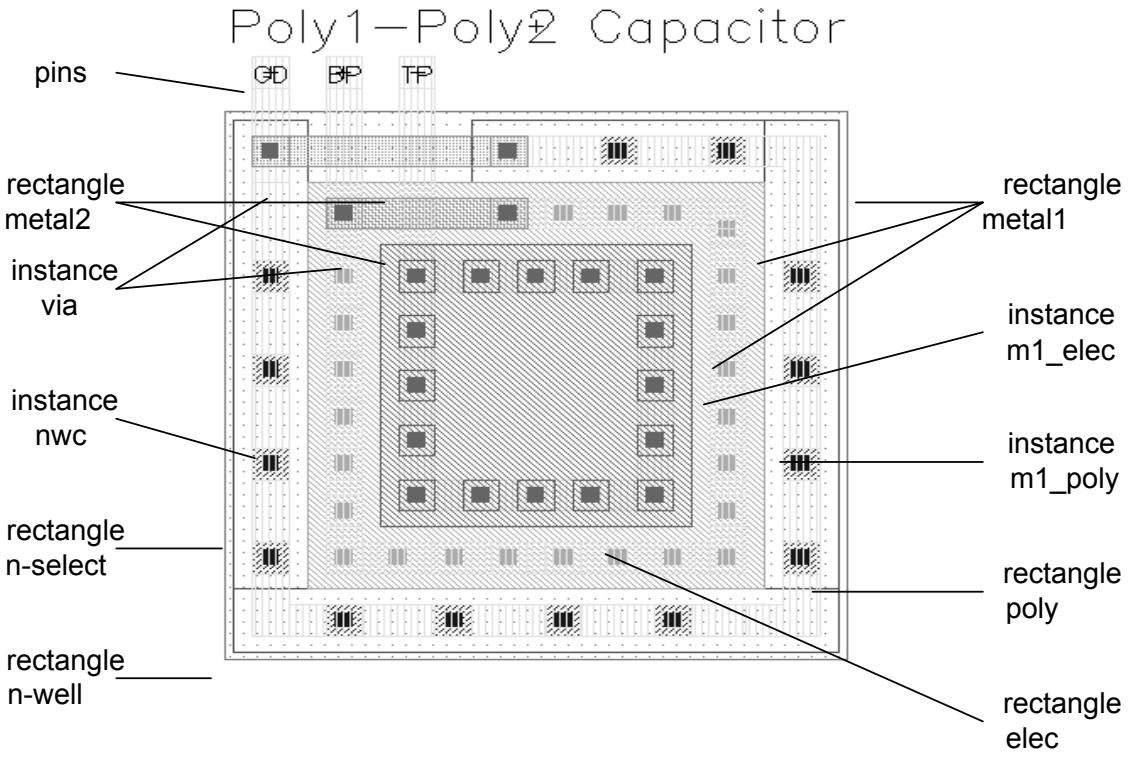


**Figure 1-7: Poly-Poly2 capacitor layout**

Figure 1-7 illustrates the layout of the poly-poly2 capacitor. The capacitor is formed by laying a second layer of polysilicon over the gate polysilicon. The area of the top plate (poly2) and the perimeter determine the capacitance by the following equation:

$$C = C_A \cdot A + C_F \cdot P$$

where:

$C_A$ is the capacitance per unit area for the chosen capacitor type

A is the area of the top capacitor plate

$C_F$ is the fringe capacitance per unit length for the chosen capacitor type for diffusion based capacitors

P is the perimeter of the top capacitor plate

For poly-poly2 capacitors, a parasitic capacitance between the substrate and poly can inject unwanted signals and noise into the circuit at the bottom plate of the capacitor. To reduce this problem, put the capacitor in an N-well (for an N-well process) and connect the well to a "clean" ground. A ground plane (metal sheet connected to ground) can be used as a shield by covering all capacitors where possible.

For poly-diffusion capacitors, the bottom plate is placed in a special capacitor well to reduce noise injection and to prevent voltage signals from altering the capacitance. This produces a high quality linear capacitance.

To prevent the injection of noise from the substrate into the bottom plate of the capacitor, always be sure to connect it to a low impedance node such as ground or the output of an op-amp. Do not connect the bottom plate of a capacitor to an op-amp input. The substrate noise is due partly to power supply noise and connecting the bottom plate to the op-amp input allows direct injection of power supply noise into the op-amp input. The power supply is used to bias the substrate, so they are usually directly connected.

When designing circuits, sometimes desired circuit performance depends on the ratio of two capacitors. In such cases, it is important that two are more capacitors are properly matched. Divide each capacitor into many smaller "unit" capacitors. For matched devices this keeps the ratio of the areas and the ratios of the perimeters the same.

Like matched MOSFETS, the common-centroid layout technique can be employed for matched capacitors. Figure 1-8 gives a simplified layout floor plan for two equally sized, well-matched capacitors.

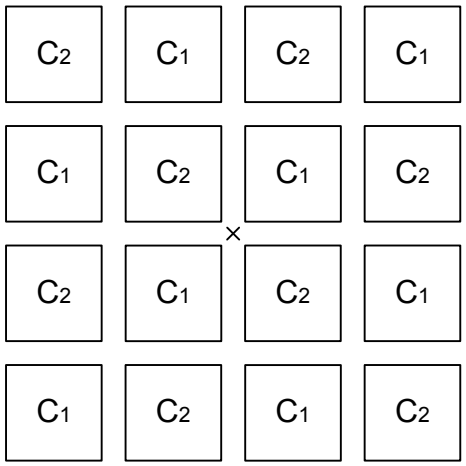


**Figure 1-8: Common-centroid capacitor layout**

The absolute and matching accuracy for various types of capacitors is given in the following table:

| Capacitor | Absolute Accuracy | Matching Accuracy |
|---|---|---|
| Poly1-Poly2 | ±20% | ±0.06% |
| Poly-Diffusion | ±10% | ±0.06% |

Remember, the purpose of using the unit capacitor is to keep the ratio of the areas and perimeters the same. This prevents (delta) variations in capacitor dimensions from changing the capacitor ratio. If a non-integral number of unit capacitors are required then the perimeters and areas can still be kept the same. If the ratio of capacitors is $\frac{C_1}{C_2} = I + N$, where 1<N<2, then the unit capacitor has side length $L_0$ and the non-unit capacitor has side lengths $L_1$ and $L_2$. Use the following formulas to calculate the side lengths of the non-unit capacitor:

$$L_1 = L_0\left(N + \sqrt{N(N-1)}\right)$$

$$L_2 = N\frac{L_0^2}{L_1}$$

Keep the unit capacitor side length $L_0$ in the range from 10μm-25μm. Also, within the capacitor array, use a consistent method of routing lines between the capacitor segments. Each unit capacitor should be surrounded by similar routing lines. For capacitors near the edge of the array, use "dummy" routing lines. Also, be sure that parasitic capacitance formed by overlapping conductors is the same for the matched capacitors.

Large unmatched capacitors can be divided into smaller unit capacitors to reduce distributed effects caused by the relatively high resistivity polysilicon. This prevents a large capacitor which possesses considerable resistivity as well as capacitance from acting as a lossy transmission line.

Resistors

As for capacitors, many different types of resistors are available in integrated circuits. Other than active devices biased to act as resistors, we can use the inherent resistivity of the polysilicon or diffusions to create resistors. The following table shows the typical values of resistance for the AMI 0.6μm process that we will be using to design circuits.

| PROCESS PARAMETERS | N+ | P+ | POLY | PLY2_HR | POLY2 | M1 | M2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 83.9 | 109.5 | 22.3 | 1014 | 40.3 | .09 | .09 | ohms/sq |
| Contact Resistance | 64.7 | 169.6 | 15.6 | | 25.9 | | 0.90 | ohms |

The total resistance of a monolithic resistor is the sum of the contact resistance and the ohmic resistance of the diffusion material. The following formula can be used to estimate resistance for polysilicon and diffusion resistors:

$$R = R_S \cdot \frac{L}{W} + 2 \cdot R_C$$

where:

$R_S$ is the resistance per square for the chosen resistor type

L is the length of the resistor

W is the width of the transistor

$R_C$ is the contact resistance

Figure 1-9 shows a polysilicon resistor layout. The resistor is constructing by adding a strip of poly and then by adding poly contacts. Next the "res_id" layer is added which tells the extraction program that this is a resistor that needs to be included in the extracted netlist.

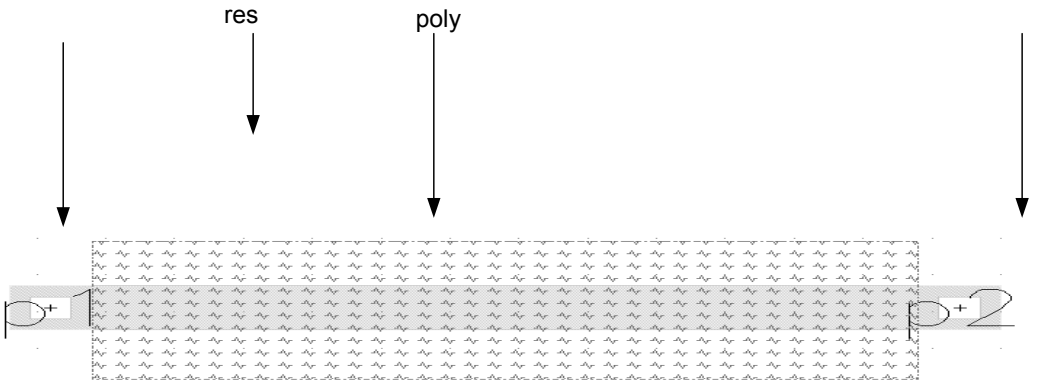


**Figure 1-9: Poly resistor layout**

If the circuit operation depends on the ratio of resistance, then good matching can be obtained by using interdigitized or common-centroid techniques. When matching resistors, be sure to keep device orientation and sizes the same. Also, since contacts contribute resistance, keep the contacts in the same ratio. An interdigitized layout of resistors is illustrated in Figure 1-10. Notice that the interconnecting metal is overlapping the resistor array and non-overlapping the resistor array in equal lengths for the two resistors.

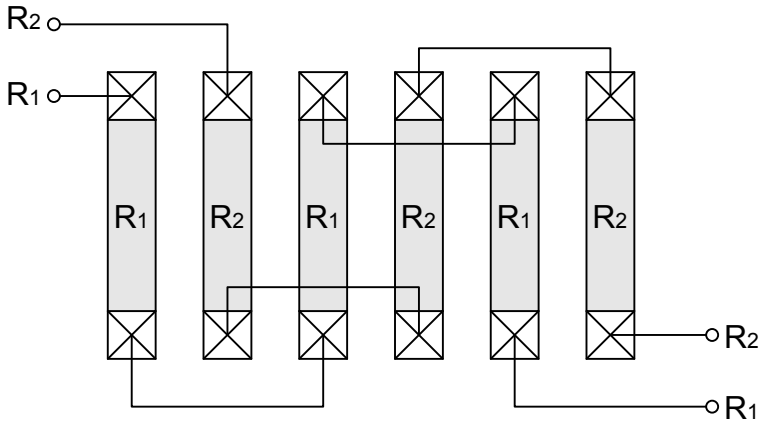


**Figure 1-10: Interdigitized resistor layout**

**Prelab**

Answer the following questions. No computer work is required for the prelab. The prelab is due at the beginning of class.

1) What are the absolute minimum dimensions of a transistor? Explain your reasoning. Remember to consider minimum contact size. Do we actually use this minimum size of do we use a slightly larger size for convenience.
2) Draw a common-centroid layout of a current mirror with equal size transistors of L = 0.6 μm and W = 19.2 μm. Use a finger length of 2.4 μm devices for each transistor segment. Remember to draw drain, source, gate, and bulk connections. Use dummy transistors and all other good layout techniques learned in the lab. Include a floor plan.
3) Design a common-centroid layout for a poly1-poly2 capacitor array. The capacitors have a ratio of 1.32:1. The capacitor array should consist of eight unit capacitors and one non-unit capacitor. Determine the form of the common-centroid layout and interconnect the capacitors. Each unit capacitance should have a separate top and bottom plate. Do not use a common bottom plate. Use the techniques described in the lab manual to give good matching. Also, give the size of the non-unit capacitor. The unit capacitor is 25 μm by 25 μm.
4) Design a matched polysilicon resistor pair to realize a resistance of 1200 Ω each. Remember to include contact resistance. Determine the approximate length and width of the diffusion. Use an interdigitized layout with six resistance segments. Use good layout techniques.

**Lab**

1. Practice good layout techniques by laying out the following:
    A) Current-mirror from prelab question #2
    B) Capacitor array from prelab question #3
    C) Matched resistors from prelab question #4
2. Include in the lab report
    A) Schematic printout
    B) Layout printout
    C) LVS printout showing that layout and schematic match

# Lab 3: More Layout Techniques

## Guard Rings

When laying out sensitive analog blocks, we need to help minimize the effect of substrate noise. One way to do this is with a guard ring. A guard ring is an array of substrate contacts which will then be connected to a clean supply (VSS or ground).

Figure 2-1 illustrates an example of a guard ring. This example shows a ring with a single contact. For more isolation, this ring can be made wider with more substrate contacts.

It is also important to note that the PMOS devices have an n-well contact ring surrounding them. This is good practice because it helps to act as an additional guard ring while also minimizing the possibility of latch up between the n-well and substrate.

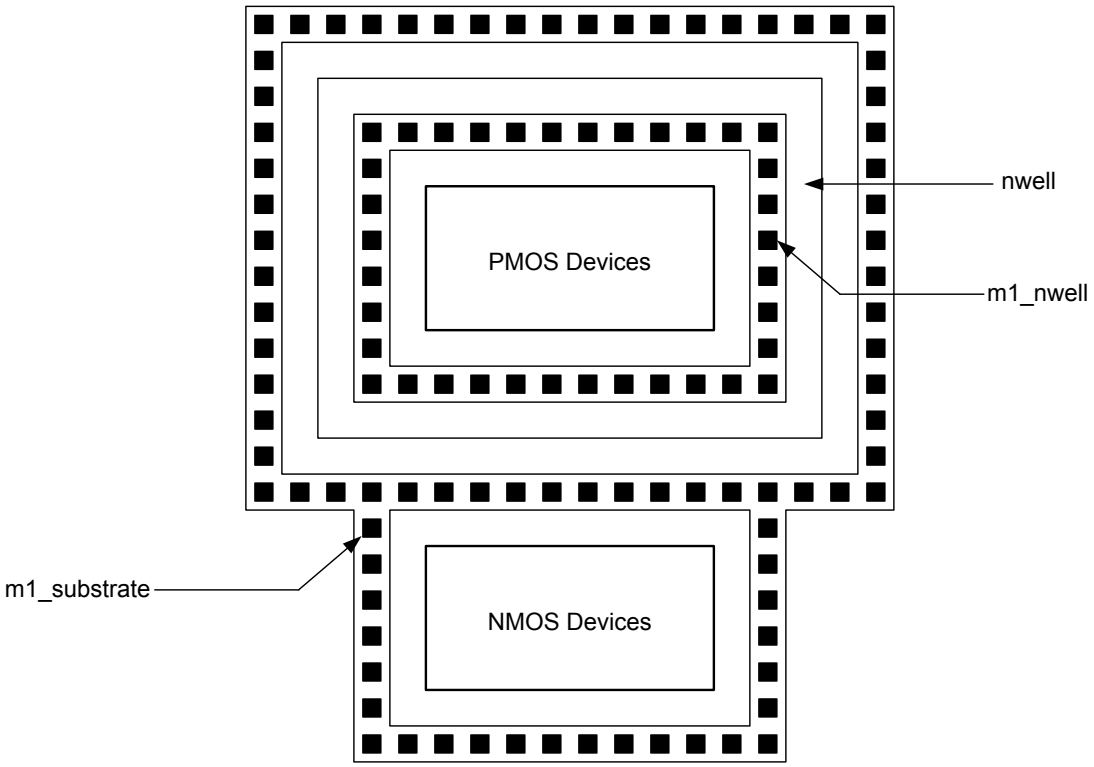


**Figure 2-1: Guard ring illustration**

**Prelab**

There is no prelab work required for this lab.

**Lab**

Use good layout techniques with guard rings to create a layout of the two-stage op-amp in Figure 2-2. Table 2-1 lists the transistor sizes for the op-amp. Figure 2-3 is a suggested floor plan to use. In this floor plan each transistor has a finger width of 2.4µm.

Include in the lab report:

A) Schematic printout

B) Layout printout

C) DRC and LVS printout showing that layout and schematic match

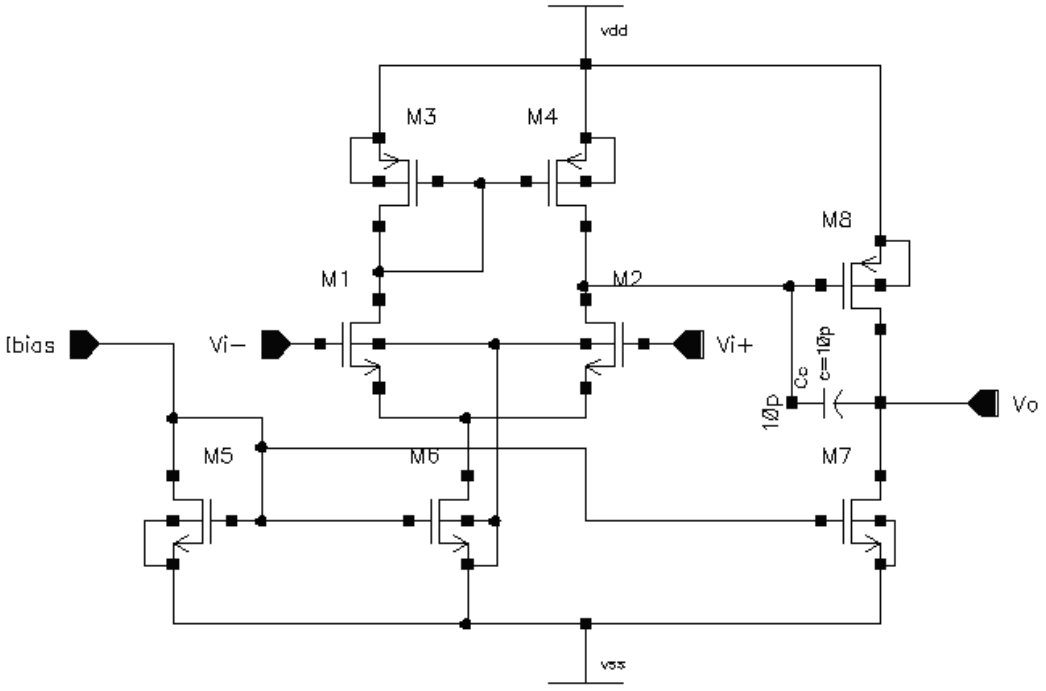


**Figure 2-2: Two-Stage Op-Amp**

**Table 2-1: Transistor Sizes**

| MOSFET | W | L |
|---|---|---|
| M1 | 9.6u | 600n |
| M2 | 9.6u | 600n |
| M3 | 19.2u | 600n |
| M4 | 19.2u | 600n |
| M5 | 4.8u | 600n |
| M6 | 9.6u | 600n |
| M7 | 19.2u | 600n |
| M8 | 76.8u | 600n |

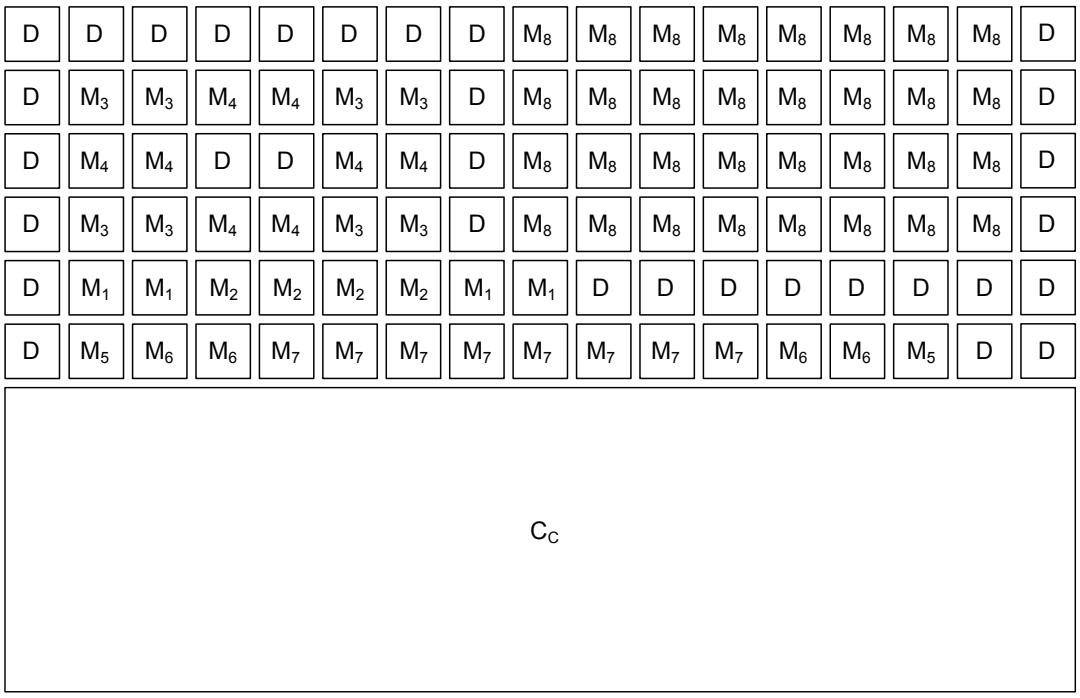


**Figure 2-3: Floor plan for two-stage op-amp layout**