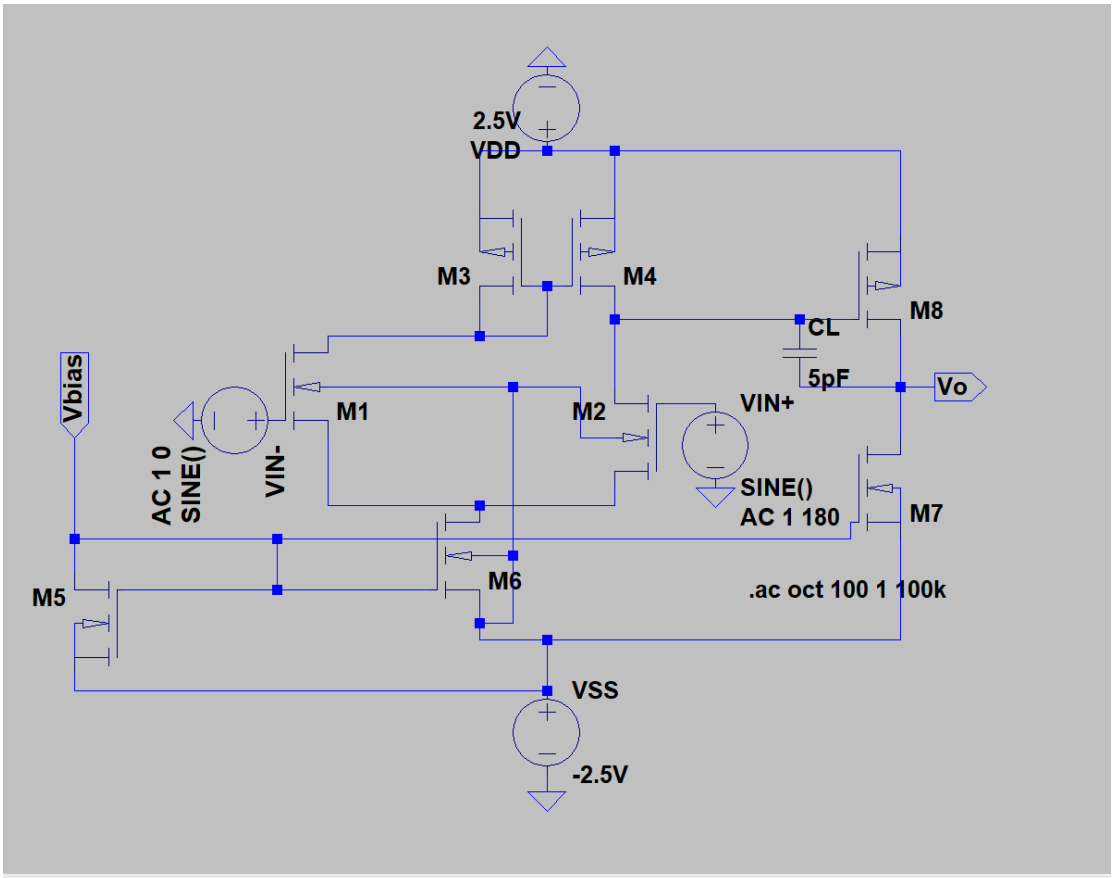
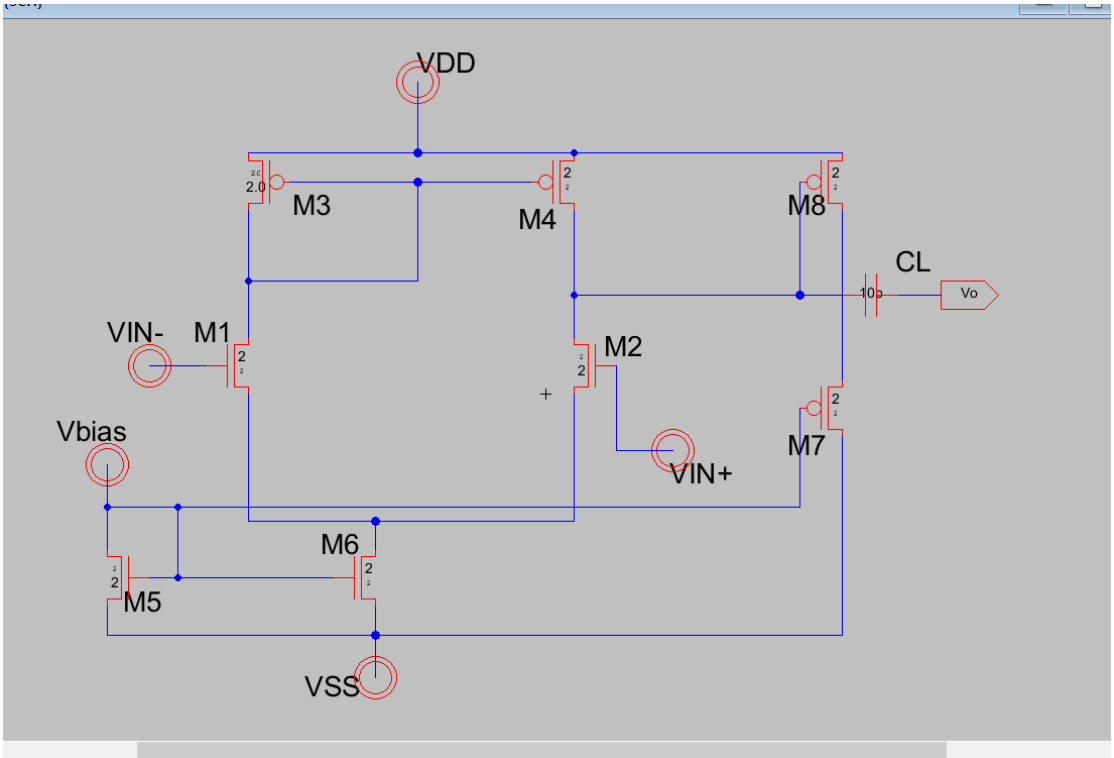
A)

Schematic print



Schematic print in electric



b)

the expansion technique:

be learned to layout large width MOSFETS. Luckily, wide transistors can be broken into parallel combinations of small width transistors as seen in Figure 1-1. By doing this horizontal expansion technique for the wide transistor, the drain and source area can be reduced which decreases parasitic capacitance and resistance.

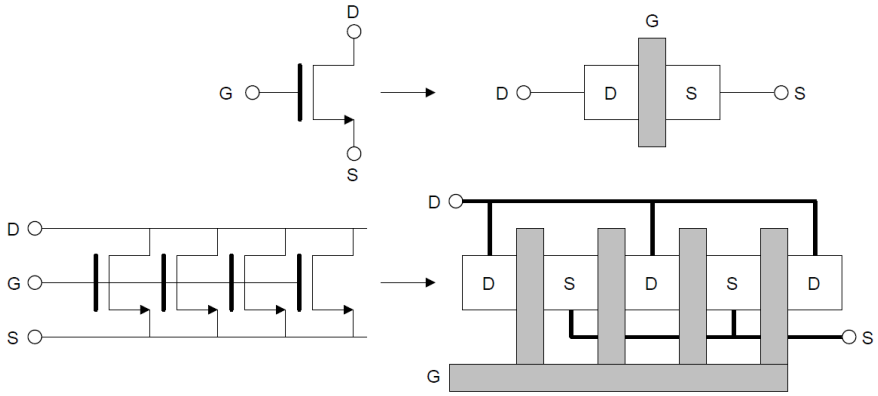


Figure 1-1: Wide MOS transistor layout

Rules in schematic diagram:

(+)

PMOS: series

NMOS: parallel

(*)

PMOS: parallel

NMOS: series

Layout: