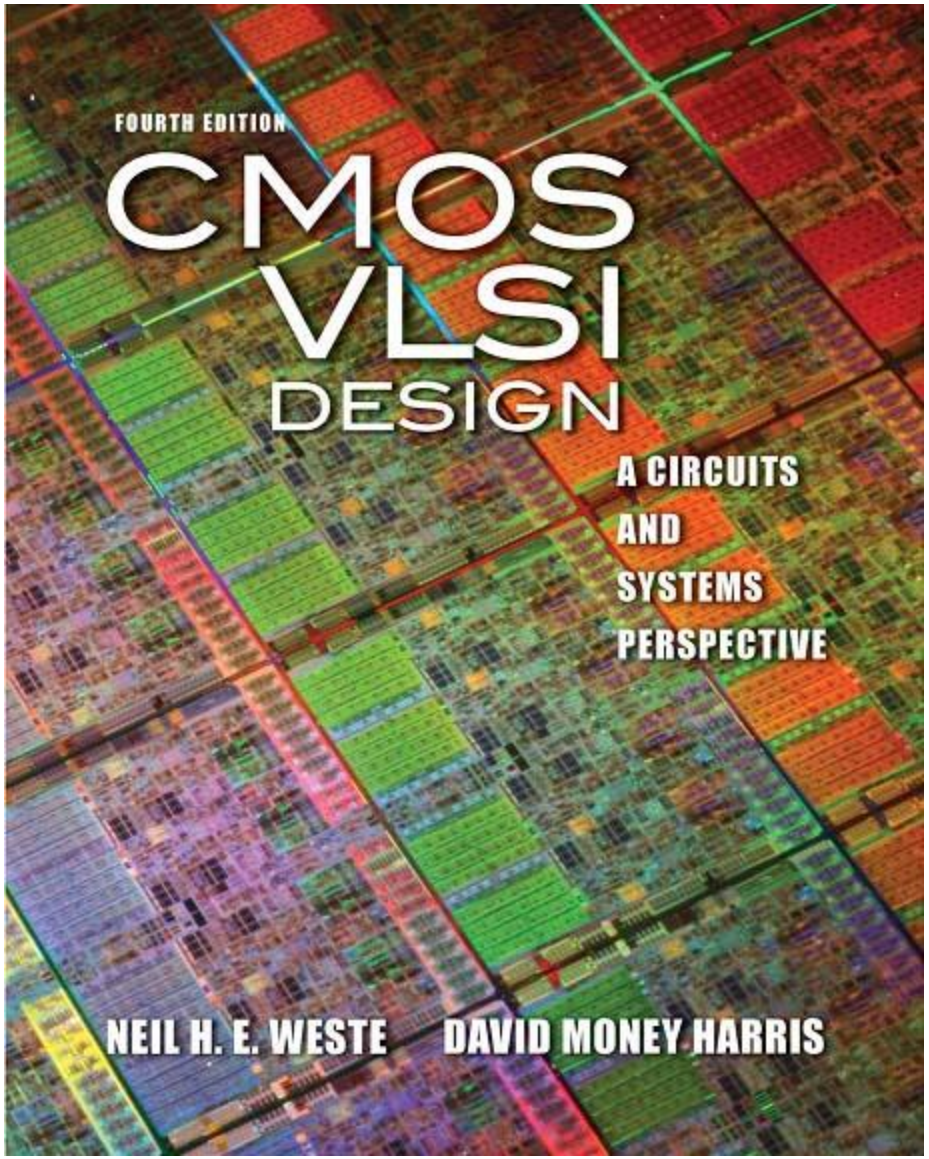
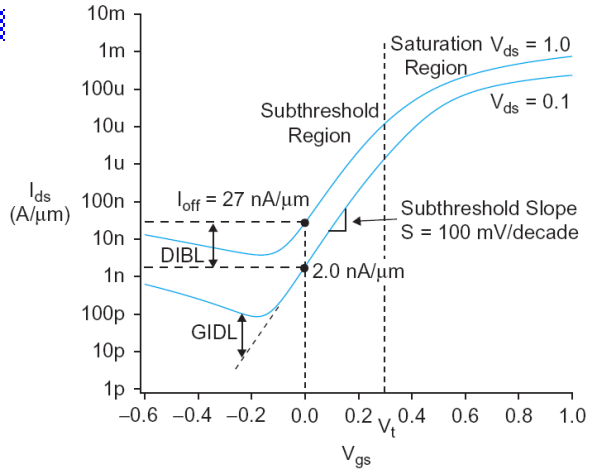
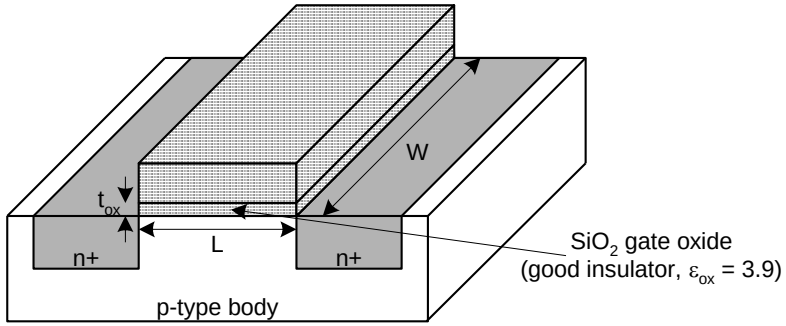


Lecture 4: Nonideal Transistor Theory

Outline

- Nonideal Transistor Behavior
  - **High Field Effects**
    - Mobility Degradation
    - Velocity Saturation
  - **Channel Length Modulation**
  - **Threshold Voltage Effects**
    - Body Effect
    - Drain-Induced Barrier Lowering(**DIBL**)
    - Short Channel Effect
  - **Leakage**
    - Subthreshold Leakage
    - Gate Leakage
    - Junction Leakage
- Process and Environmental Variations





Ideal Transistor I-V

- *Shockley* long-channel transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

for nMOS

$$\beta = \beta_n = \mu_n \frac{\varepsilon_{ox} W}{t_{ox} L}$$
$$V_t = V_{tn}$$

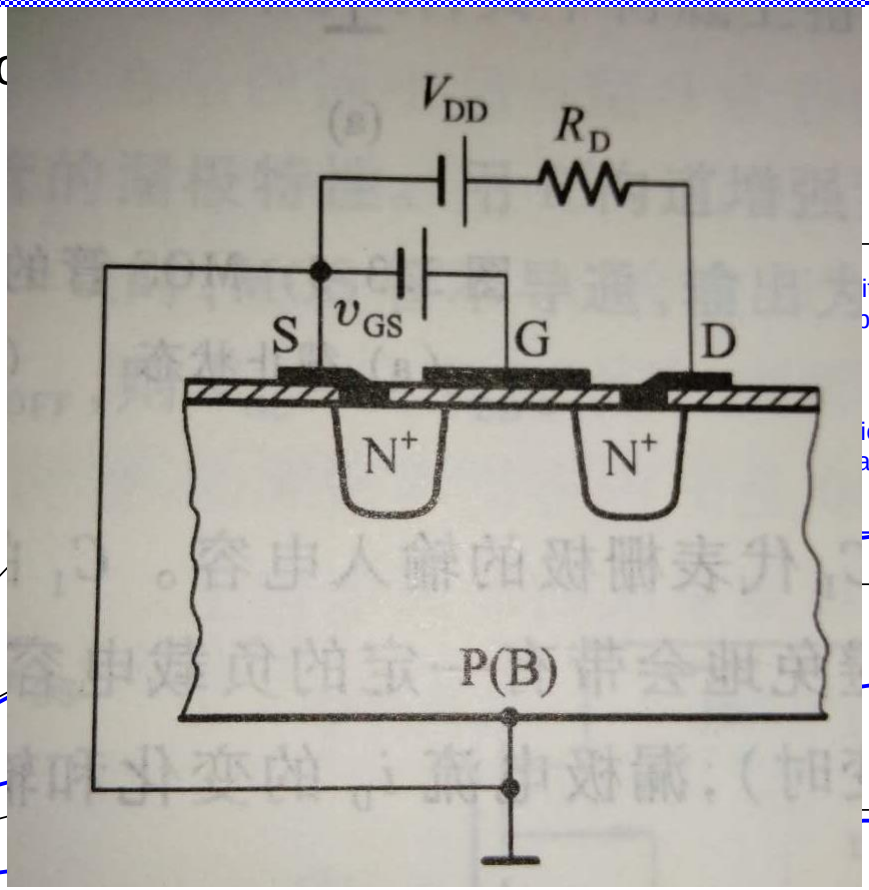
for pMOS

$$\beta = \beta_p = \mu_p \frac{\varepsilon_{ox} W}{t_{ox} L}$$
$$V_t = V_{tp}$$

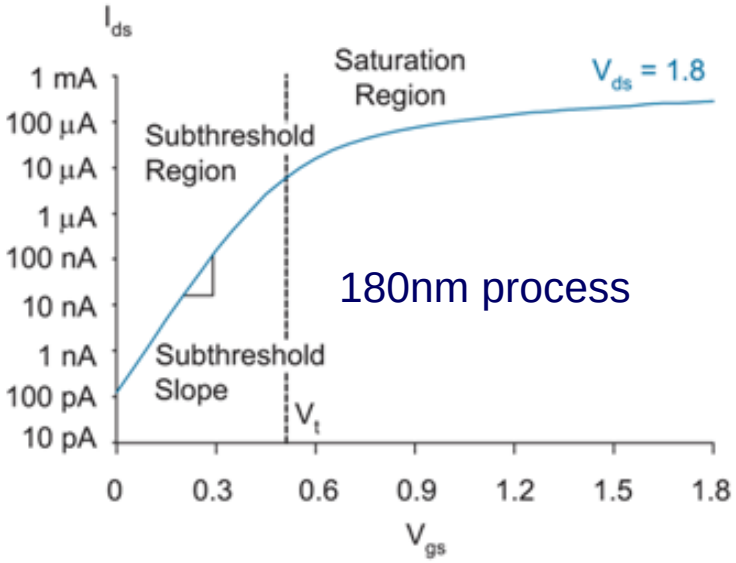
$$\mu_p < \mu_n (\mu_n \approx 2 \times \mu_p)$$

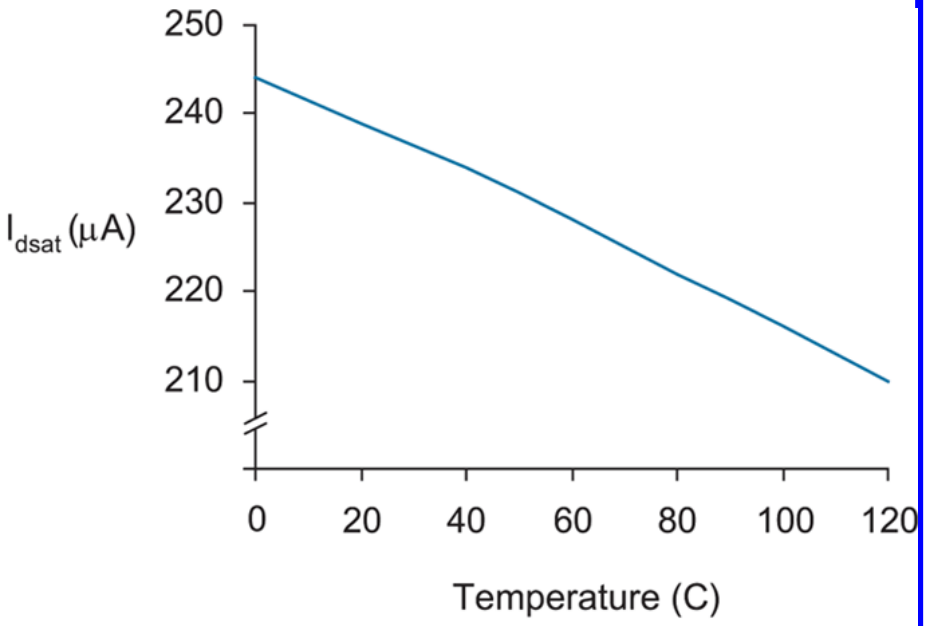
Ideal vs. Simulated nMOS I-V Plot

- 65 nm IBM pr



Continue

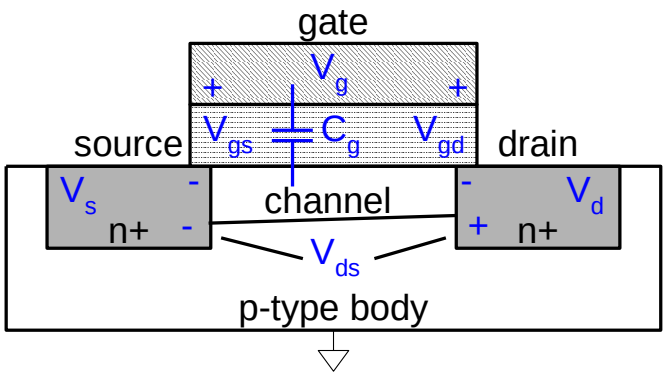




- There is leakage current when the transistor is in cut off
- Ids depends on the temperature

Electric Fields Effects

- Vertical electric field: E_{vert} = _____
  - Attracts carriers into channel
  - Long channel: $Q_{channel} = CV \propto E_{vert}$
- Lateral electric field: E_{lat} = _____
  - Accelerates carriers from drain to source
  - Long channel: $v = \mu E_{lat}$
  - $t = L / v$
  - I=Q/t



Mobility Degradation

- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface

$$\mu_{\text{eff}-n} = \frac{540\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\frac{V_{gs}+V_t}{0.54\frac{\text{V}}{\text{nm}}t_{\text{ox}}}\right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\frac{\left|V_{gs}+1.5V_t\right|}{0.338\frac{\text{V}}{\text{nm}}t_{\text{ox}}}}$$

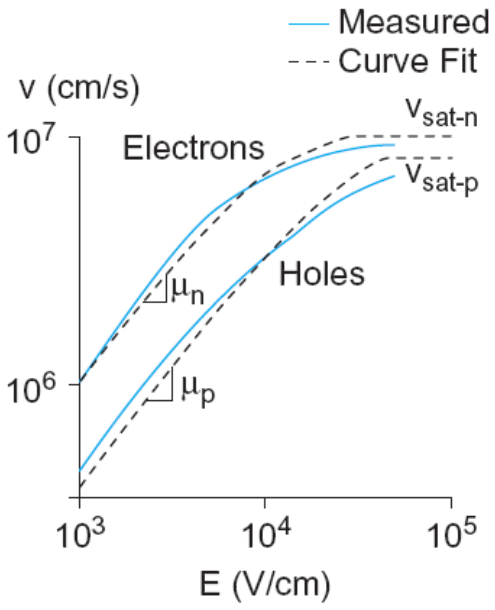
SOLUTION: Use $V_{gs} = 1.0$ for ON transistors, remembering that we are treating voltages as positive in a pMOS transistor. Substituting $V_t = 0.3$ V and $t_{ox} = 1.05$ nm into EQ (2.23) gives:

$$\mu_{\text{eff-n}}(V_{gs} = 1.0) = 96 \text{ cm}^2/\text{V}, \mu_{\text{eff-p}}(V_{gs} = 1.0) = 36 \text{ cm}^2/\text{V}$$

Velocity Saturation

- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off atoms in silicon lattice
  - Velocity reaches v_{sat}
    - Electrons: 10^7 cm/s
    - Holes: 8 x 10^6 cm/s
  - Better model

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \qquad E_c = \frac{2v_{\text{sat}}}{\mu_{\text{eff}}} \qquad V_c = E_c L$$



Velocity Saturation

- Substituting,

$$I_{ds} = \begin{cases} \dfrac{\mu_{eff}}{1+\dfrac{V_{ds}}{V_c}} C_{ox} \dfrac{W}{L}\left(V_{GT} - \dfrac{V_{ds}}{2}\right)V_{ds}, & V_{ds} < V_{d,sat} \\ C_{ox} W \left(V_{GT} - V_{d,sat}\right) v_{sat}, & V_{ds} > V_{d,sat} \end{cases}$$

- Note that μ_{eff} is also a function of V_{GT} due to mobility degradation.
- Equating the two equations above at the boundary $V_{ds} = V_{d,sat}$

$$V_{d,sat} = \frac{V_{GT} V_c}{V_{GT} + V_c}$$

Velocity Saturation

- Substituting this value in the velocity saturated regime,

$$I_{dsat} = WC_{ox} v_{sat} \frac{V_{GT}^2}{V_{GT} + V_c}$$

- For $V_{GT} << V_c$, the equation reduces to the square law model.
- For $V_{GT} >> V_c$, the the equation becomes

$$I_{dsat} \approx WC_{ox} v_{sat} V_{GT}$$

Vel Sat I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{\left(V_{gs} - V_t\right)^2}{2} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox} W \left(V_{gs} - V_t\right) v_{max}$$

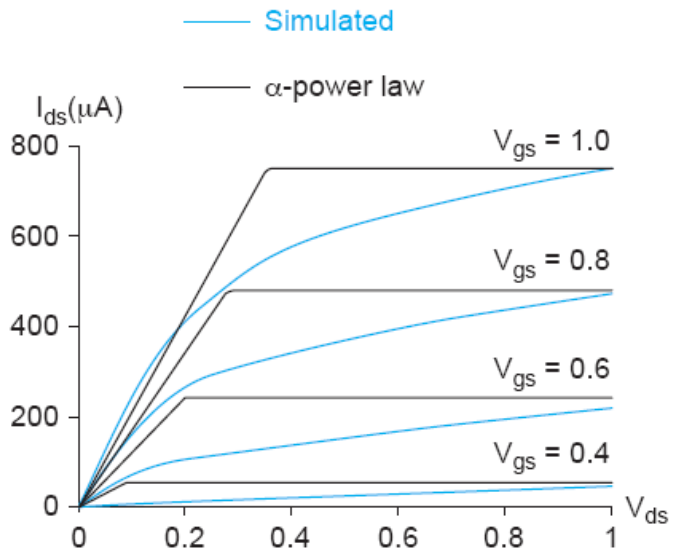
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically (≈ 1.3 for 65 nm)

α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}$$

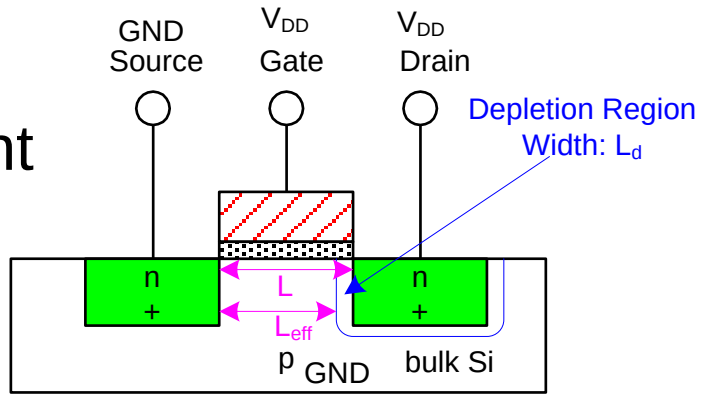
$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$



Pc, *Pv* and α are found by fitting the model to the empirical modeling results

Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives _____ current
  - I_{ds} _____ with V_{ds}
  - Even in saturation



$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

Channel Length Mod I-V

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right)$$

- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

Threshold Voltage Effects

- V_t is V_{gs} for which the channel starts to invert
- Ideal models assumed V_t is constant
- Really depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

Body Effect

- Body is a fourth transistor terminal
- V_{sb} affects the charge required to invert the channel
  - Increasing V_s or decreasing V_b increases V_t

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- ϕ_s = *surface potential* at threshold

$$\phi_s = 2v_T \ln\frac{N_A}{n_i} \qquad v_T = \frac{kT}{q}$$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i
- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Body Effect Cont.

- For small source-to-body voltage, treat as linear

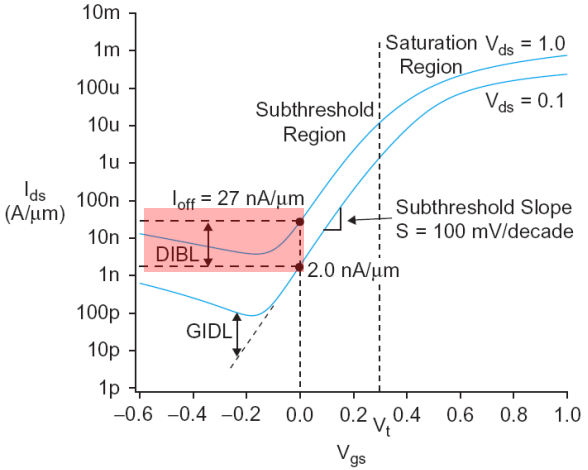
$$V_t = V_{t0} + k_\gamma V_{sb}$$

$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si}N_A}{v_T \ln\frac{N_A}{n_i}}}}{2C_{ox}}$$

DIBL

- Electric field from drain affects channel
- More pronounced in small transistors where the drain is closer to the channel
- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$



- High drain voltage causes current to _____

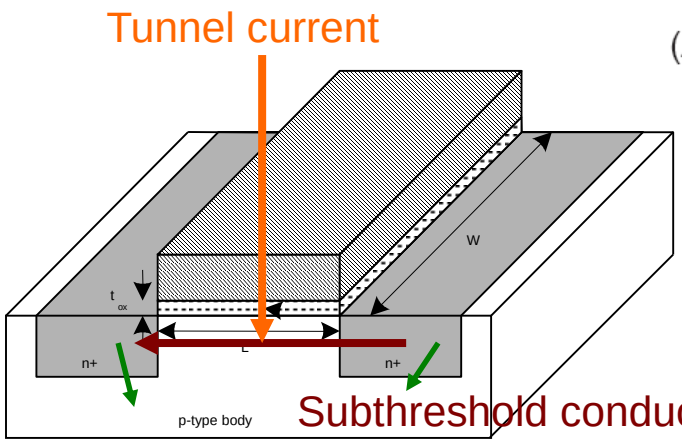
  - DIBL increases subthreshold leakage at high *Vds*

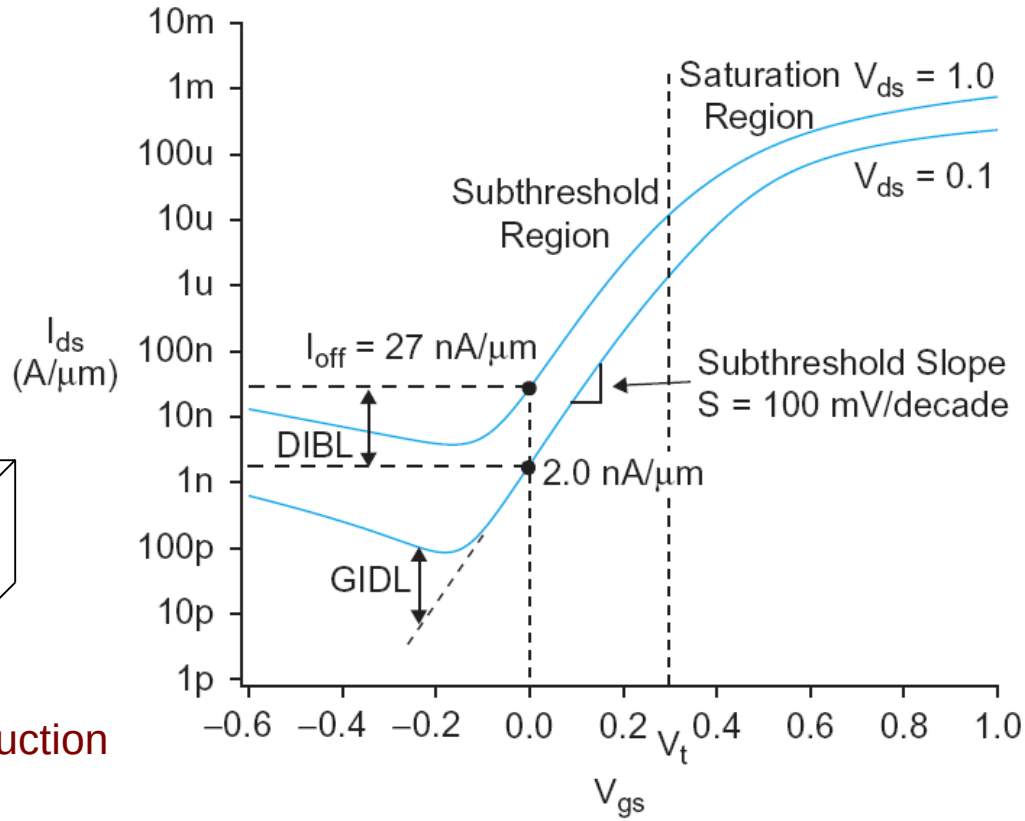
Short Channel Effect

- In small transistors, source/drain depletion regions extend into the channel.
  - Impacts the amount of charge required to invert the channel.
  - And thus makes V_t a function of channel length.
- Short channel effect: V_t increases with L.
  - Some processes exhibit a reverse short channel effect in which V_t decreases with L.
  - This is called Reverse Short Channel Effect (RSCE).

Leakage

- What about current in cutoff?
- Simulated results
- What differs?
  -



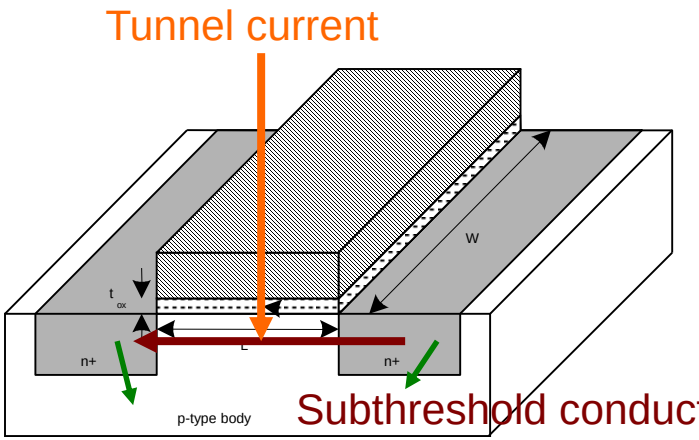


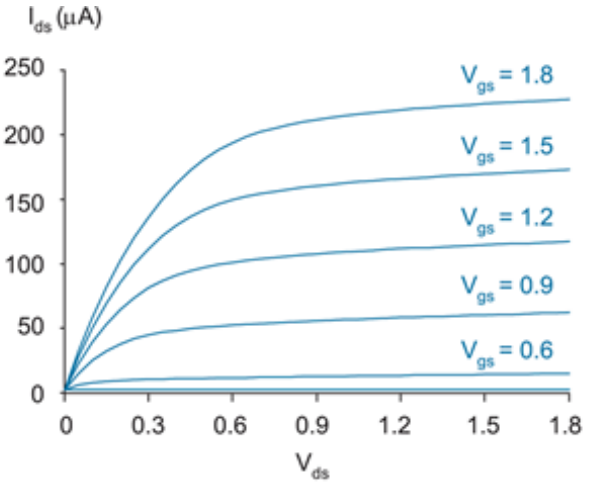
Junction leakage

Leakage Sources

- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- Gate leakage
  - Tunneling through ultrathin gate dielectric
- Junction leakage
  - Reverse-biased PN junction diode current

Subthreshold Leakage





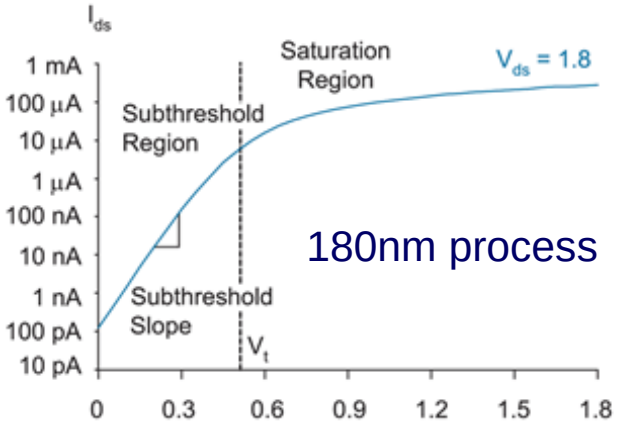
Junction leakage

- Subthreshold leakage is the biggest source in modern transistors

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nv_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \qquad v_T = \frac{kT}{q}$$

$$I_{ds0} = \beta v_T^2 e^{1.8}$$

n = 1.4-15



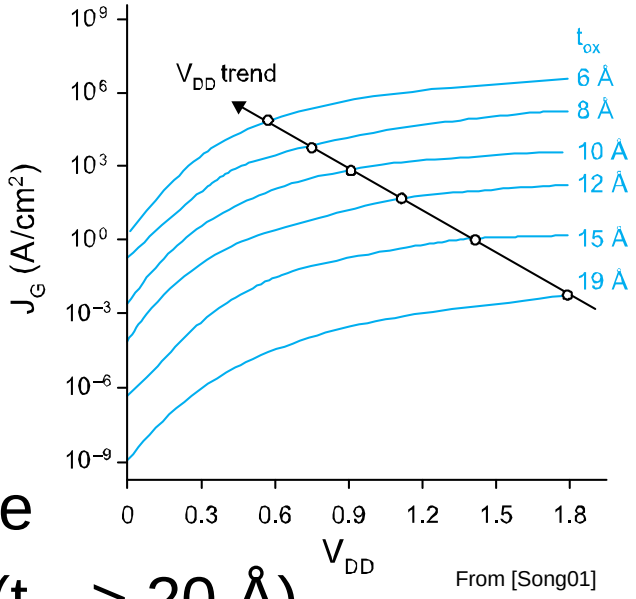
180nm process

Gate Leakage

- Carriers tunnel through very thin gate oxides
- Exponentially sensitive to t_{ox} and V_{DD}

$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

  - A and B are tech constants
  - Greater for electrons
    - So nMOS gates leak more

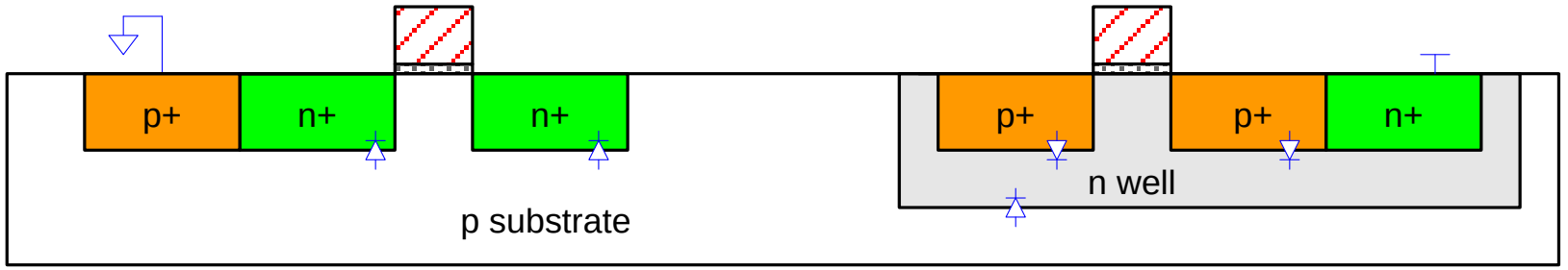


From [Song01]

- Negligible for older processes (t_{ox} > 20 Å)
- Critically important at 65 nm and below (t_{ox} ≈ 10.5 Å)

Junction Leakage

- Reverse-biased p-n junctions have some leakage
  - Ordinary diode leakage
  - Band-to-band tunneling (BTBT)
  - Gate-induced drain leakage (GIDL)



Diode Leakage

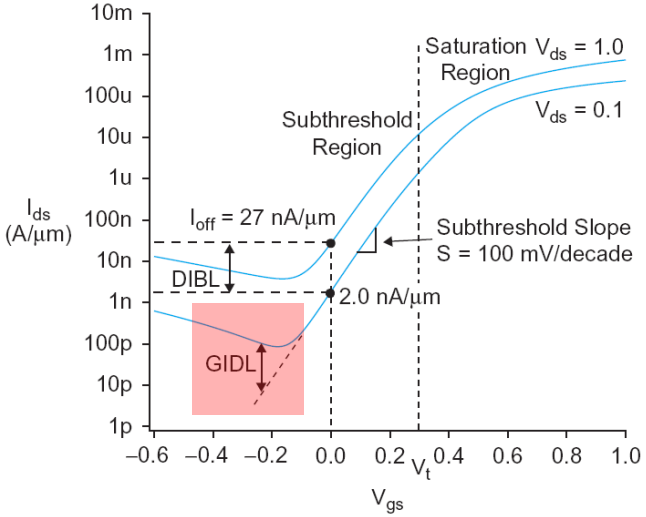
- Reverse-biased p-n junctions have some leakage

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- At any significant negative diode voltage, $I_D = -I_s$
- I_s depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/μm^2 (negligible)

Gate-Induced Drain Leakage

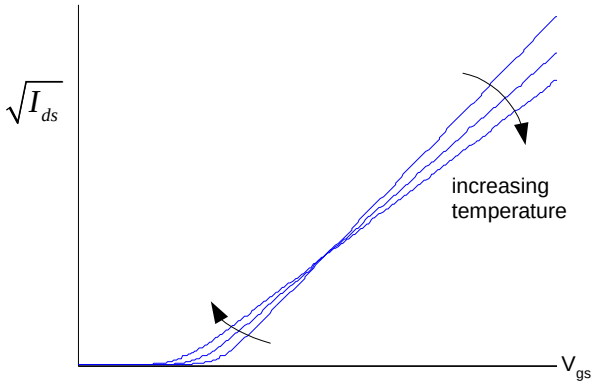
- Occurs at overlap between gate and drain
  - Most pronounced when drain is at V_{DD}, gate is at a negative voltage
  - Thwarts efforts to reduce subthreshold leakage using a negative gate voltage



Gate-Induced Drain Leakage (GIDL).

Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} _____ with temperature
- I_{OFF} _____ with temperature



$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$

$$\beta = \mu C_{ox}\frac{W}{L}$$

Temperature Sensitivity

- The mobility changes by

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu}$$

  - k_μ is a fitting parameter with a typical value 1.5
- v_{sat} decreases with temperature, dropping by about 20% from 300 to 400K.
- The magnitude of the threshold voltage decreases nearly linearly with temperature as

$$V_t(T) = V_t(T_r) - k_{vt}(T - T_r)$$

  - k_{vt} is typically about 1-2 mV/K

So What?

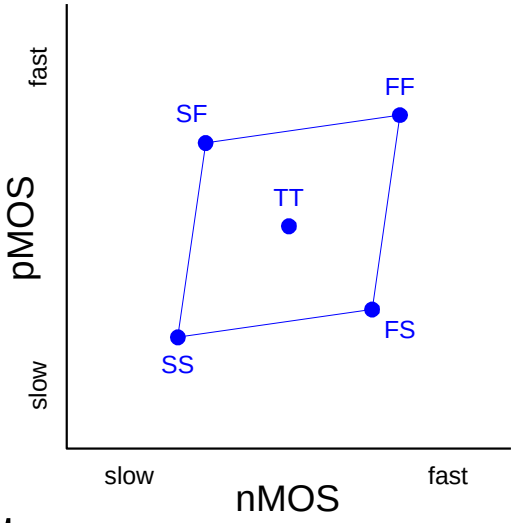
- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

So What?

- Velocity saturation and mobility degradation result in less than expected current at high voltage.
  - There is no point in trying to use high V_{DD} for speed.
  - Moreover, short channels and thin gate oxides will be damaged by high V_{DD}.
- Series transistors divide voltage. Thus, they are faster than a single transistor contrary to expected.

Parameter Variation

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: _____
  - V_t: _____
  - t_{ox}: _____
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



Environmental Variation

- V_{DD} and T also vary in time and space
- Fast:
  - V_{DD}: _____
  - T: _____

Corner	Voltage	Temperature
F		
T	1.8	70 C
S		

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

Important Corners

- Some critical simulation corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time				
Power				
Subthreshold leakage				

$$P_{\text{switching}} = CV_{DD}{}^2 f_{\text{sw}}$$