VLSI design analog Lab1

Single Stage Differential Amplifier

Introduction

In this lab we design a one stage differential amplifier. The amplifier was required to meet the following specifications:

Vdd=-Vss=2.5V
Total Power<0.3mW (Opamp part)
Slew Rate: SR≥10V/us
DC Gain ≥ 35dB
Gain Bandwidth Product(GBW) ≥ 10MHz
Linear Output Swing Range: Vic-Vt2≤Vout≤Vdd-0.3V
CMRR≥50dB
Input Common Mode Range (ICMR): ICMR≥50%×(Vdd-Vss)
CL=5pF and Vth,n=0.75V

Design

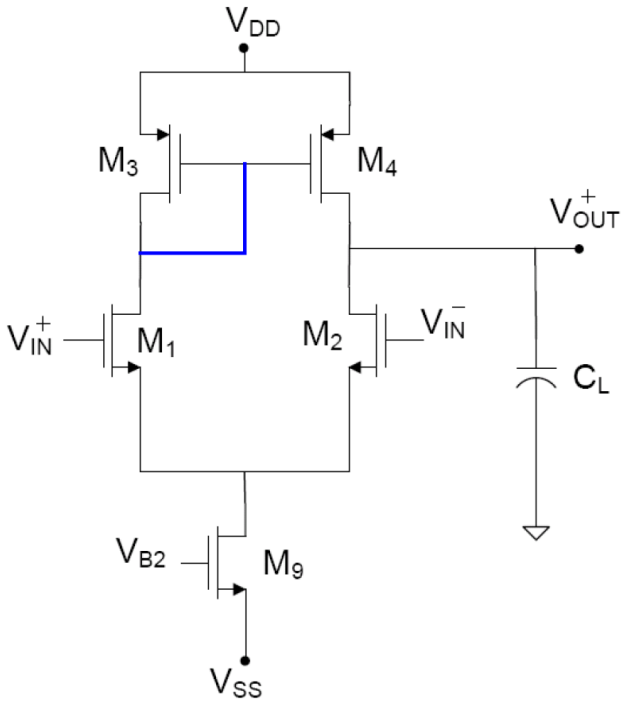

Figure 1: Basic single stage differential amplifier architecture with NMOS differential pair.

In order to begin the design the quiescent tail current was selected from the slew rate and power requirement.

$$SR \geq 10\,\frac{V}{\mu s} \qquad SR = \frac{I_T}{C_L}$$

$$\frac{I_T}{5pF} \geq 10\,\frac{V}{\mu s} \qquad I_T \geq \left(10\,\frac{V}{\mu s}\right)(5pF)$$

$$I_T \geq 50\mu A$$

$$P < 0.3mW \qquad I_T(5v) < 0.3mW$$

$$I_T < 60\mu A$$

$$50\mu A \leq I_T < 60\mu A$$

$$I_T = 55\mu A$$

$$For\ good\ current\ mirror\ accuracy\text{:}\ V_{EB9} = 0.3v \qquad \frac{W_9}{L_9} = \frac{2I_D}{\mu_n C_{ox}(V_{EB9})}\text{^2}$$

$$\frac{W_9}{L_9} = \frac{2(55\mu A)}{\left(120\frac{\mu A}{V^2}\right)(0.3v)^2} = \frac{12.2\mu m}{1.2\mu m}$$

$$V_{g9} = V_{EB9} + V_{ss} + V_{T9} = \quad 0.3\text{V-}2.5\text{V+}0.75\text{=-}1.45\text{V}$$

~~The~~ final tail current was chosen to be 55µA. The sizing of the current source transistor, M9, can then be chosen based on the selected tail current.

Next the sizing of the differential pair, M1 and M2, was chosen to meet the gain-bandwidth product requirement of the amplifier.

$$GBW = \frac{g_{m1}}{C_{L'}} \qquad C_{L'} = 1.3C_L \qquad GBW \geq 10MHz$$

$$g_{m1} \geq 2\pi(10MHz)(5pF\ *1.3) \quad g_{m1} \geq 314.6\frac{\mu A}{V}$$

$$chose \quad g_{m1} \geq 410\,\frac{uA}{V}$$

$$g_{m1} = \sqrt{\frac{2\mu_n C_{ox} W_1 I_D}{L_1}} \qquad \frac{W_1}{L_1} \leq \frac{(g_{m1})^2}{2\mu_n C_{ox} I_D} \qquad \frac{(g_{m1})^2}{2\mu_n C_{ox} I_{D/2}} = \frac{(410\ \frac{\mu A}{V})^2}{2\left(120\frac{\mu A}{V^2}\right)(\ 27.5\text{uA})}$$

$$\frac{W_1}{L_1} \leq \frac{30.56\text{um}}{1.2\mu m}$$

Finally the sizing of the active load, current mirroring transistors, M3 and M4, was chosen according to the output swing range.

$$V_o < V_{DD} - V_{EB4} \quad \text{requirement: } V_o \leq V_{DD} - 0.3v$$

$$V_{EB4} = V_{EB5} < 0.3v$$

choose upper bound, $V_{EB4} = V_{EB5} \approx 0.3v$, in order to insure an accurate current mirror ratio of 1.

$$\frac{W4}{L_4} = \frac{ID}{\mu_p C_{ox}(V_{EB4})^2} = \frac{27.5}{\left(40\frac{\mu A}{V^2}\right)(0.3v)^2} = \quad 15.28=23\mu m/1.5\mu m$$

Implementation

The differential amplifier along with the voltage generation circuitry to generate Vg9 was implemented as shown in figure 2. Vg9 is the gate voltage of the transistor which controls the tail current.

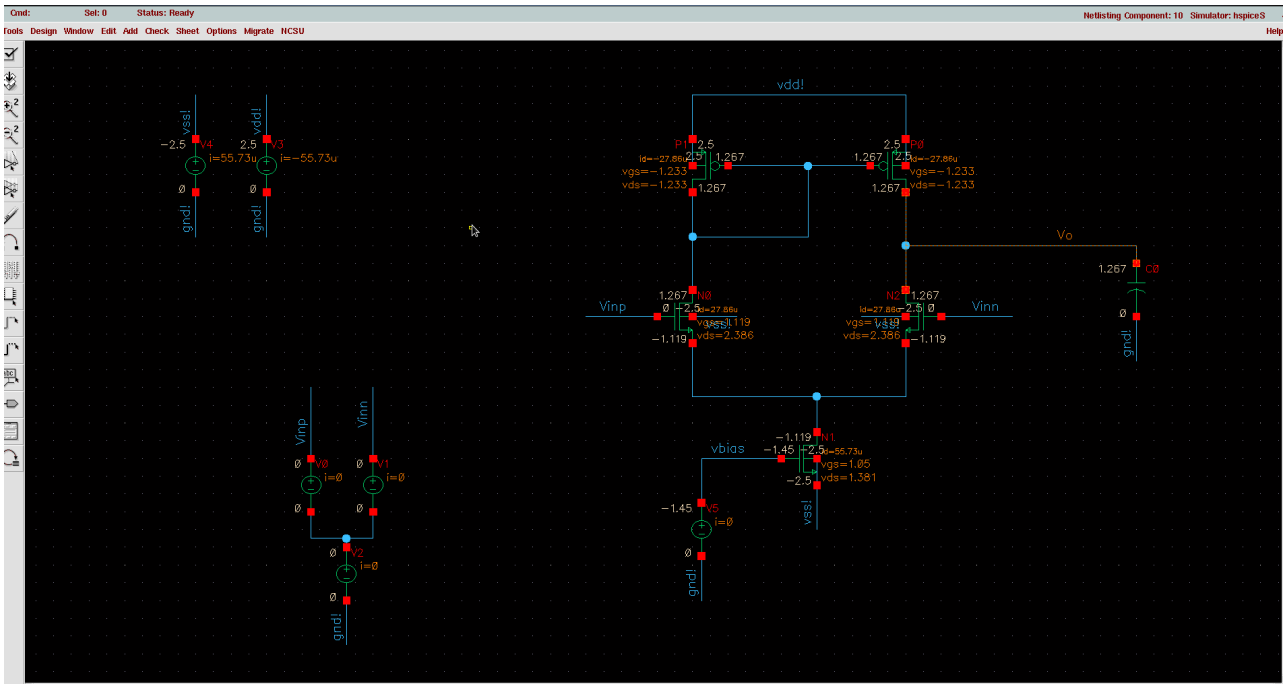

Figure 2: Differential amplifier schematic with a Vdd independent current source and bias voltage generator.

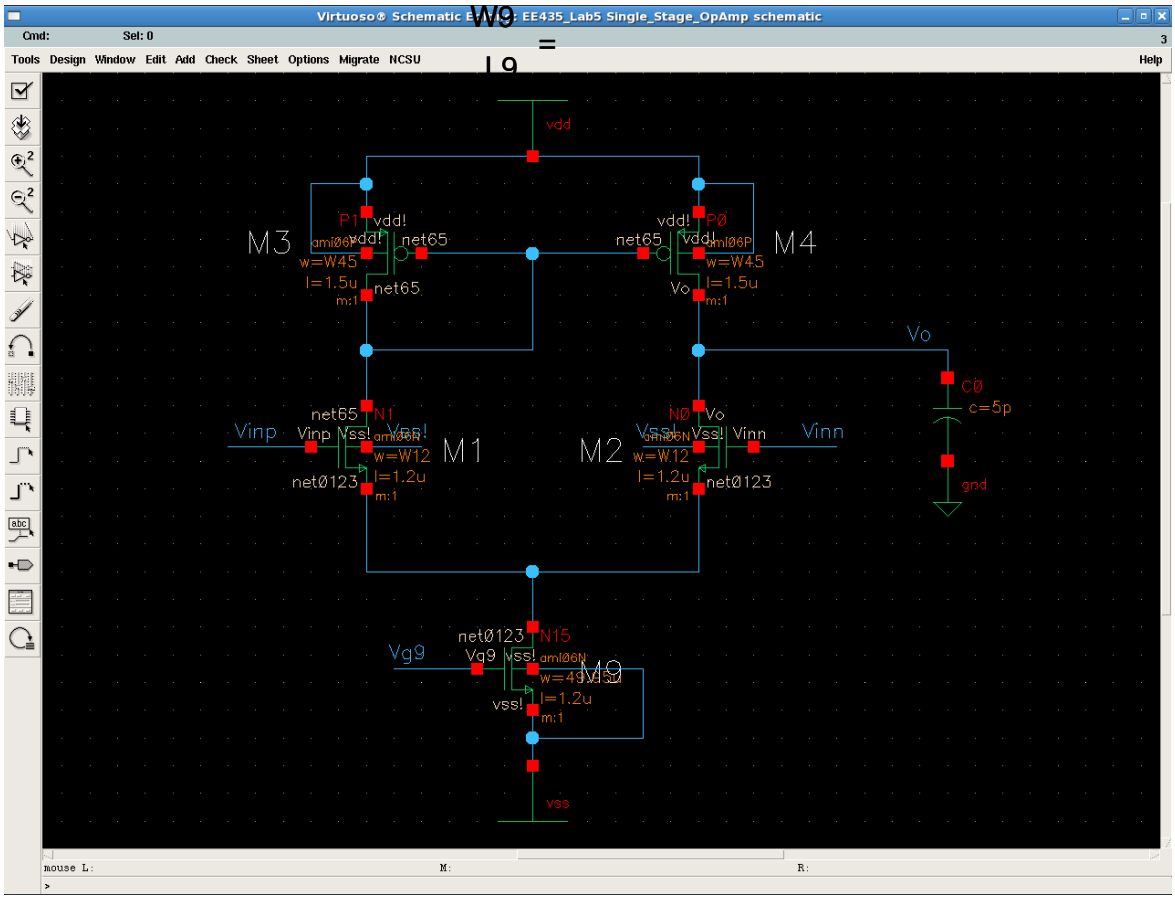

Figure 3: differential voltage amplifier schematic

In order to set the tail current the sizing of the diode connected transistor in the voltage bias generating circuit was swept in order to find the proper output voltage. The initial sweep indicated there were no values that would set the desired tail current so the width of M9 was increased to 50µm so the desired current range was available.

The V_{EB} of each transistor was then adjusted by adjusting the size of the transistors in order to increase the V_{EB} of M3 and M4 to ensure accurate current mirroring.

Having set the current to 55 µA, the gain of the amplifier was ran and was slightly below the required gain at DC. The tail current was decreased to 53µA to raise the DC gain of the amplifier.

The final sizes, after tuning, turned out to be:

$$\frac{W1}{L1} = \frac{W2}{L2} = \frac{30.56\mu m}{1.5\mu m}$$

$$\frac{W3}{L3} = \frac{W4}{L4} = \frac{23\mu m}{1.5\mu m}$$

$$\frac{W9}{L9} = \frac{12.2\mu m}{1.2\mu m}$$

Results

Total Power

The total power consumed was 0.265 mW. It was calculated from the tail current value of 53µA and a V_{DD}-V_{SS} voltage of 5v.

DC gain, GB product, Gain and Phase Plots

The differential voltage gain and phase bode plots were created as shown in figures 4 and 5. The DC gain requirement was meet with a DC gain of 41.06 dB. You can also see that the gain-bandwidth product requirement was meet with a unity gain frequency of 10.03MHz as shown in the gain bode plot in figure 4.

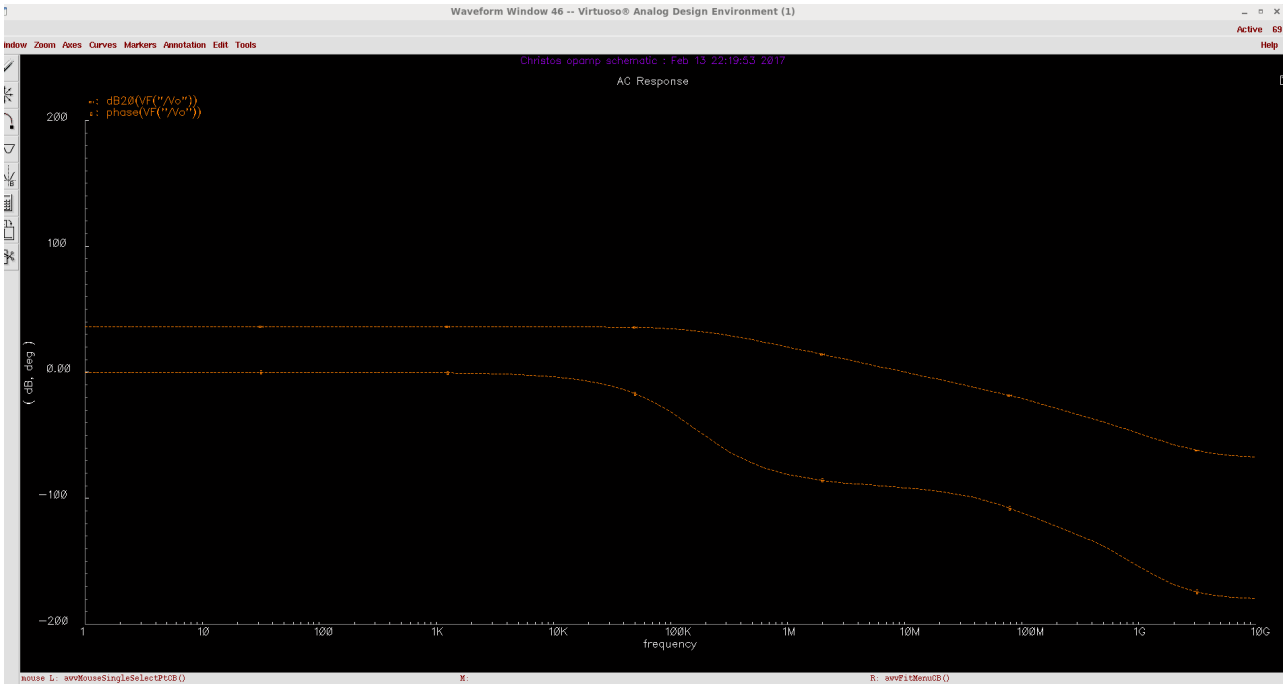

Figure 4: Gain bode plot

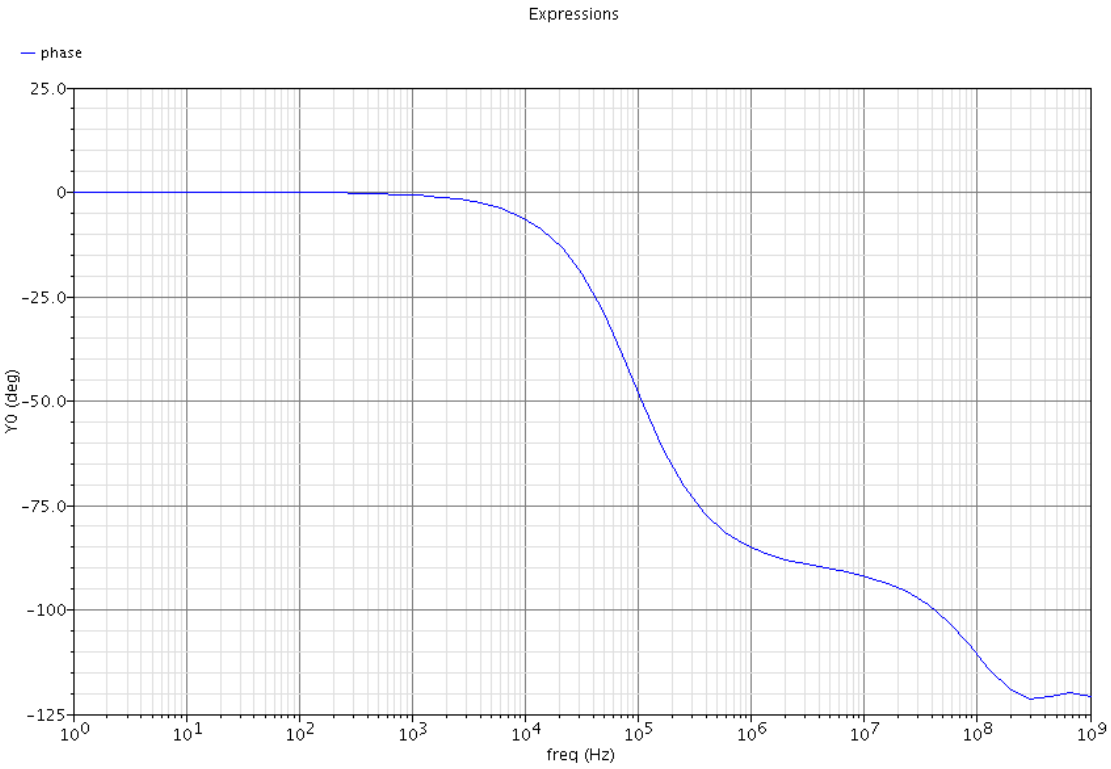

Figure 5: Phase bode plot

Slew Rate

Next the slew rate was measured by putting the amplifier in the buffer configuration shown in figure 6. A pulse input between V_{DD} and V_{SS} was then applied and the maximum slope of the rising edge of the pulse was found by running a transient simulation. The slew rate was found to be $12.4\frac{V}{\mu s}$ as shown in figure 7.

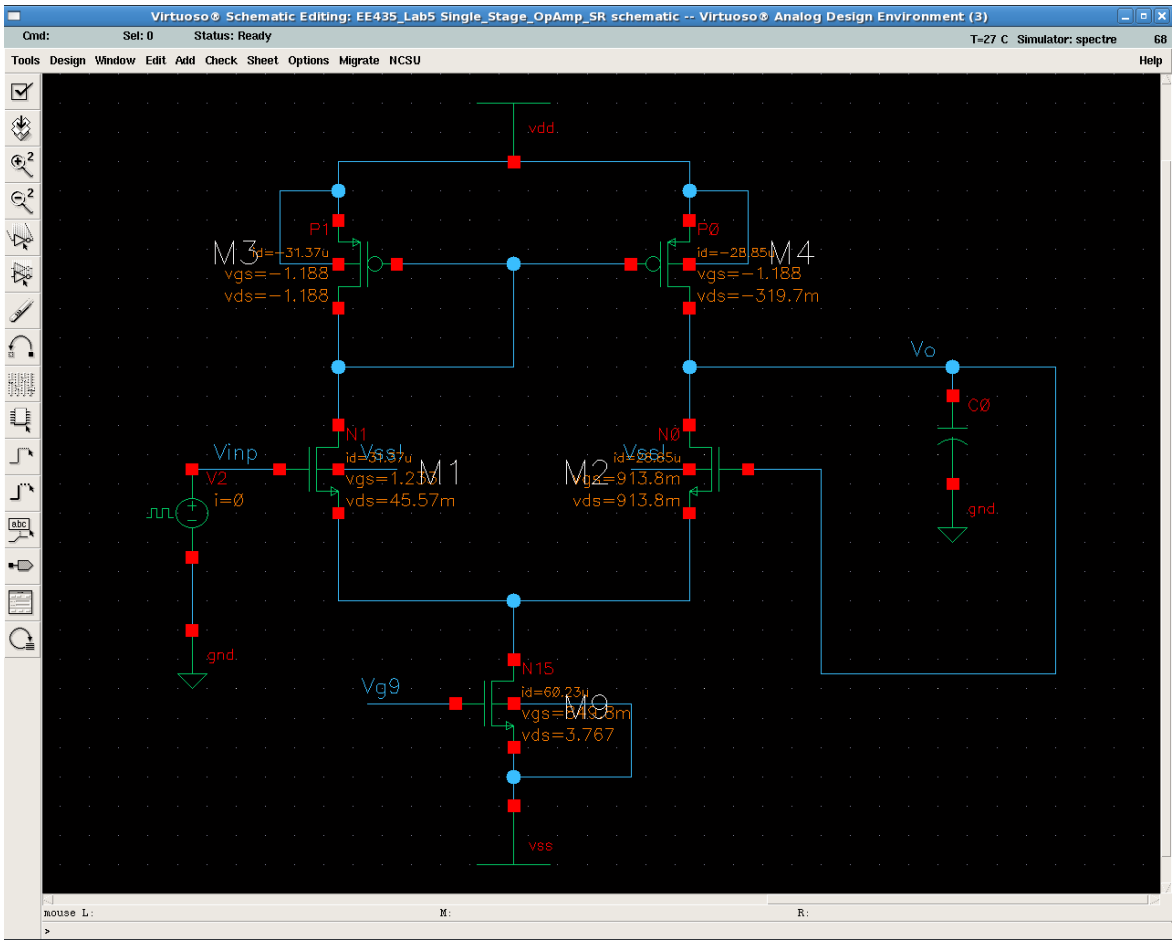

Figure 6: Buffer configuration used to find the slew rate of the amplifier.

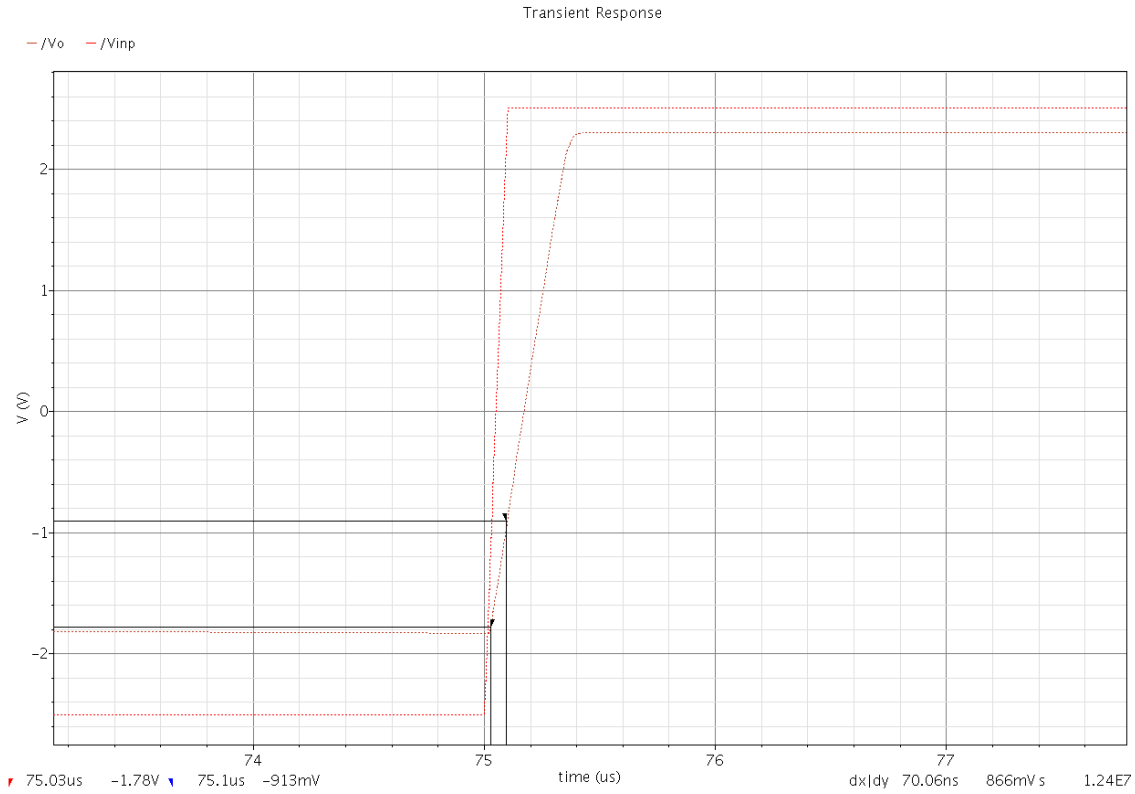

Figure 7: transient simulation of a step input used to determine the slew rate

Linear Output Swing Range

The linear output swing range was determined by sweeping the common mode input and determining the linear output region as sown in figure 8. It was found to be 2.9827v.

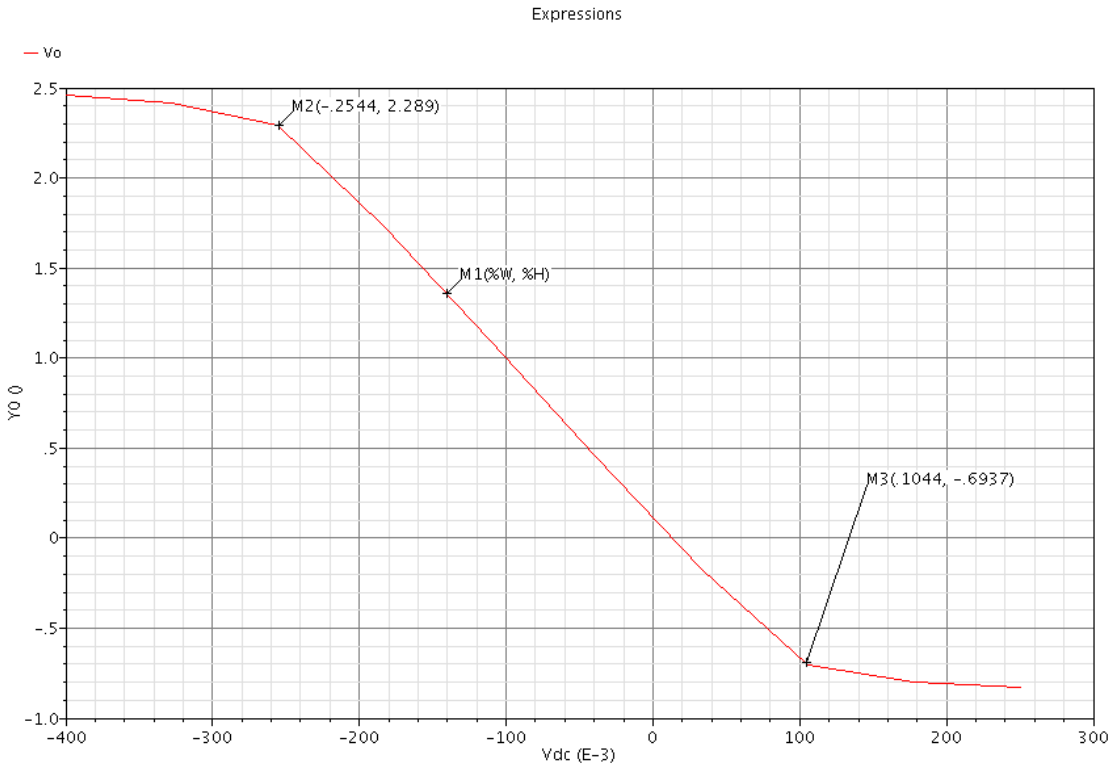

Figure 8: linear output range plot

Common Mode Rejection Ratio (CMRR)

The CMRR was found to be . It was found by first finding the DC differential gain and then finding the DC common mode gain. The DC differential gain was found above to be 41.05 dB and the DC common mode gain was found to be -41.85 dB as shown in figure 9. The DC common mode gain was found by setting both the positive and the negative differential inputs to a common input with a magnitude of 1 mV Once both gains were found, then the ICMR was calculated as:

$$ICMR = \ln\left(\frac{A_{cm}}{A_{vd}}\right) = -82.9dB$$

$$|ICMR| = 82.9dB$$

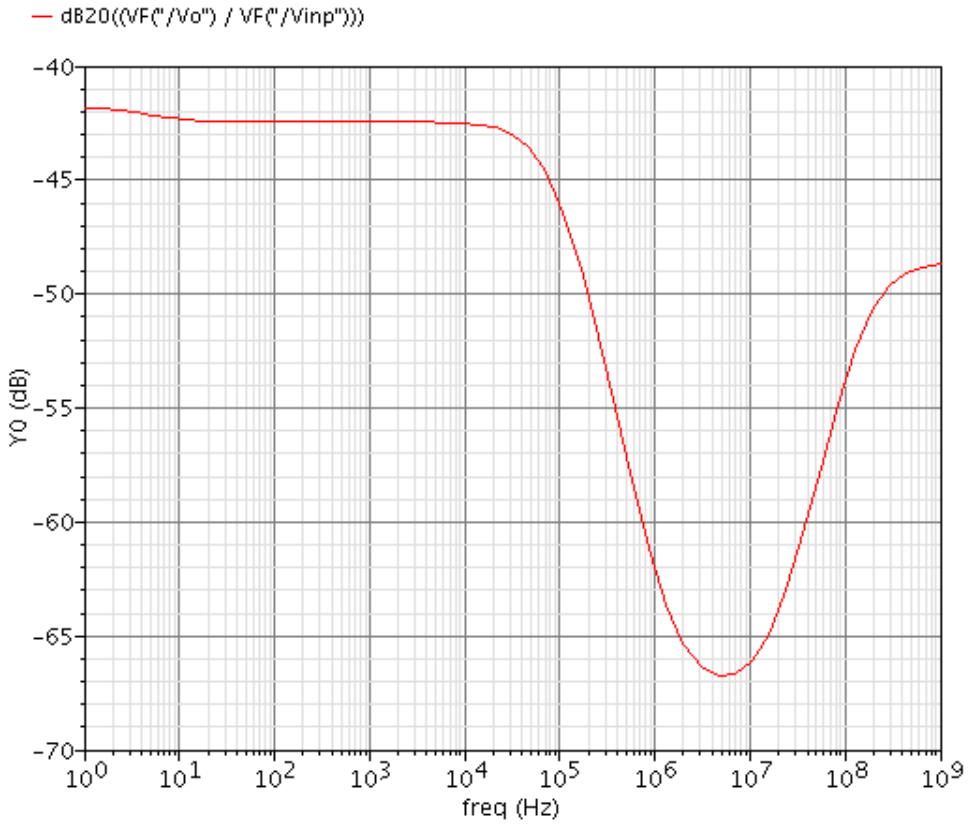

Figure 9: Common mode gain bode plot.

Input Common Mode Range

The input common mode range was found by measuring the range of common mode input that the differential gain remains at for a low frequency input. Hence the differential voltage was measured as the common input voltage was swept as shown in figure 10. The input common mode range was found to be 3.4v.

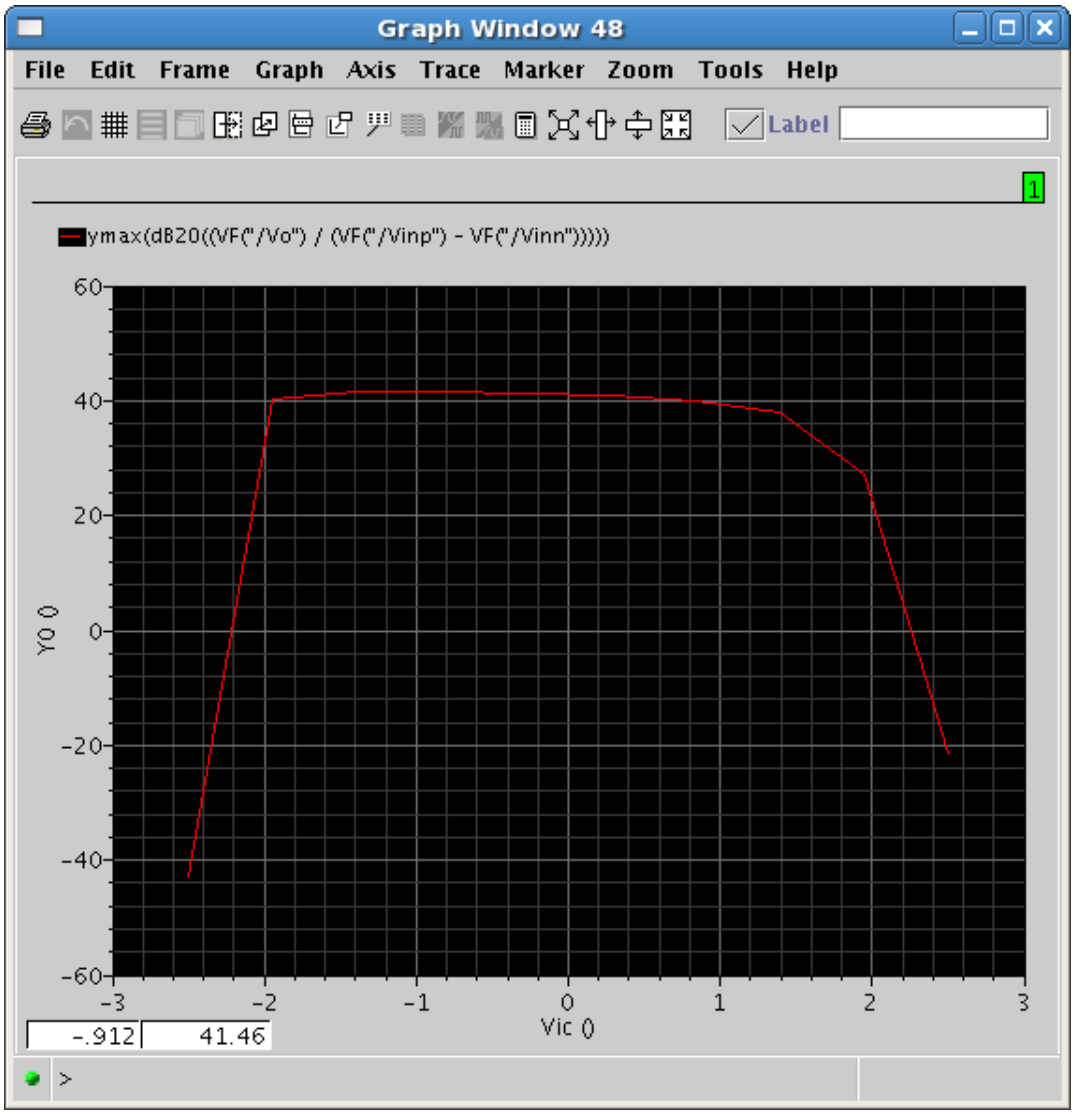

Figure 10: Common mode input range plot.

Telescopic Differential Amplifier Design

Next a challenge to increase the DC gain of the differential amplifier from above 40 dB to above 70 dB was posed. I was able to accomplish this by cascading the differential amplifier to form what is called a telescopic amplifier. The new amplifier architecture is shown in figure 11.

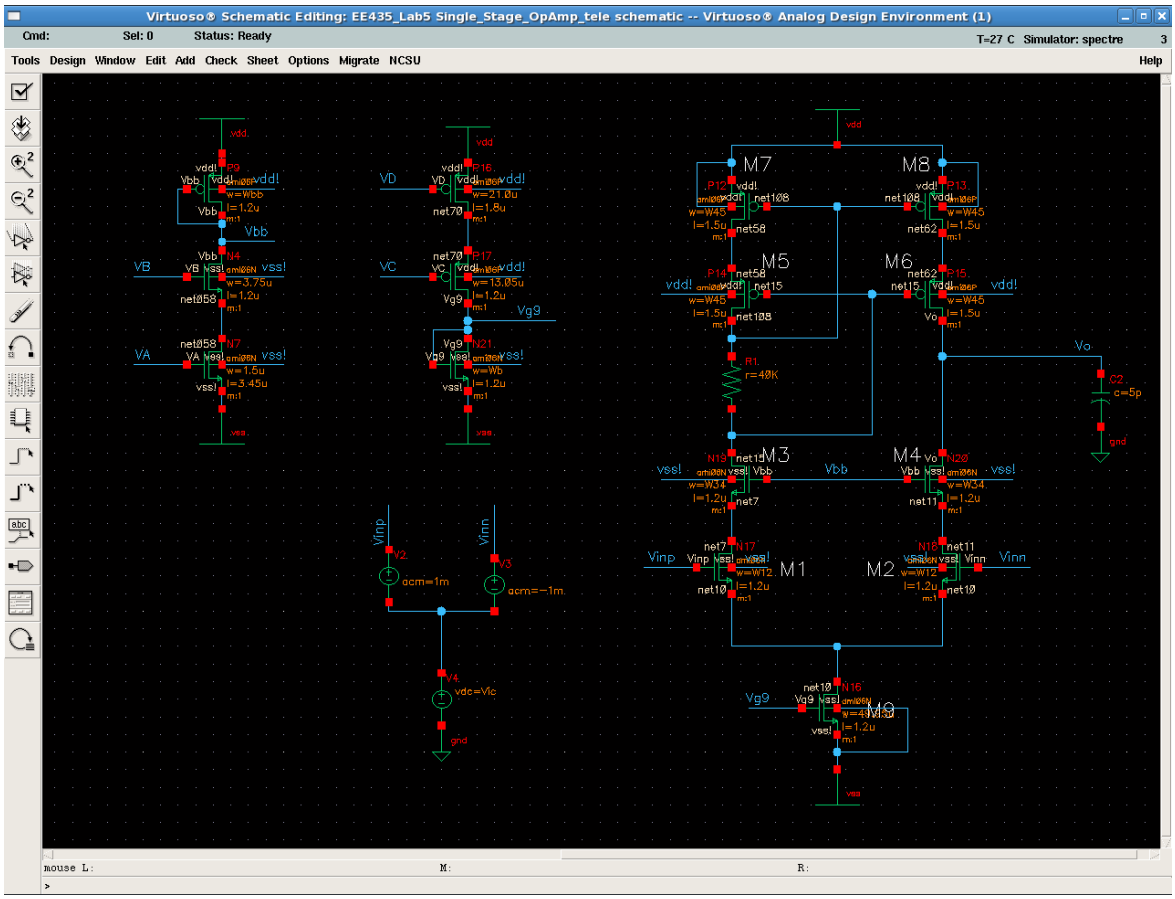

Figure 11: telescopic differential amplifier schematic.

The amplifier was created by cascading both the top PMOS current mirror and the bottom differential pair to increase the output impedance and hence increase the gain of the amplifier. A resistor was added do both of the top two transistors could be biased in a current mirror configuration. The size of the resistor was found by adjusting its size while monitoring and balancing the Vgs values of the top two transistor pairs. The bottom set of NMOS cascading transistors is biased at 800mv by using a second bias generating circuit. The size of the cascading transistor was set equal to that of the original top pair of transistors at

$$\frac{W_{cascoding\ transistors}}{L_{cascoding\ transistors}} = \frac{35.7um}{1.2um}$$

All other transistors remained the same size, with the exception of the diode connected transistors used to set the bias voltages. The tail current dropped slightly to 52 uA after the cascode transistors were added.

The DC gain was then found to be 75 dB as shown in figure 12. This is well above the requirement of 70 dB. The amplifier could be further tuned to meet many of the other specifications outlined for the original differential amplifier if required.

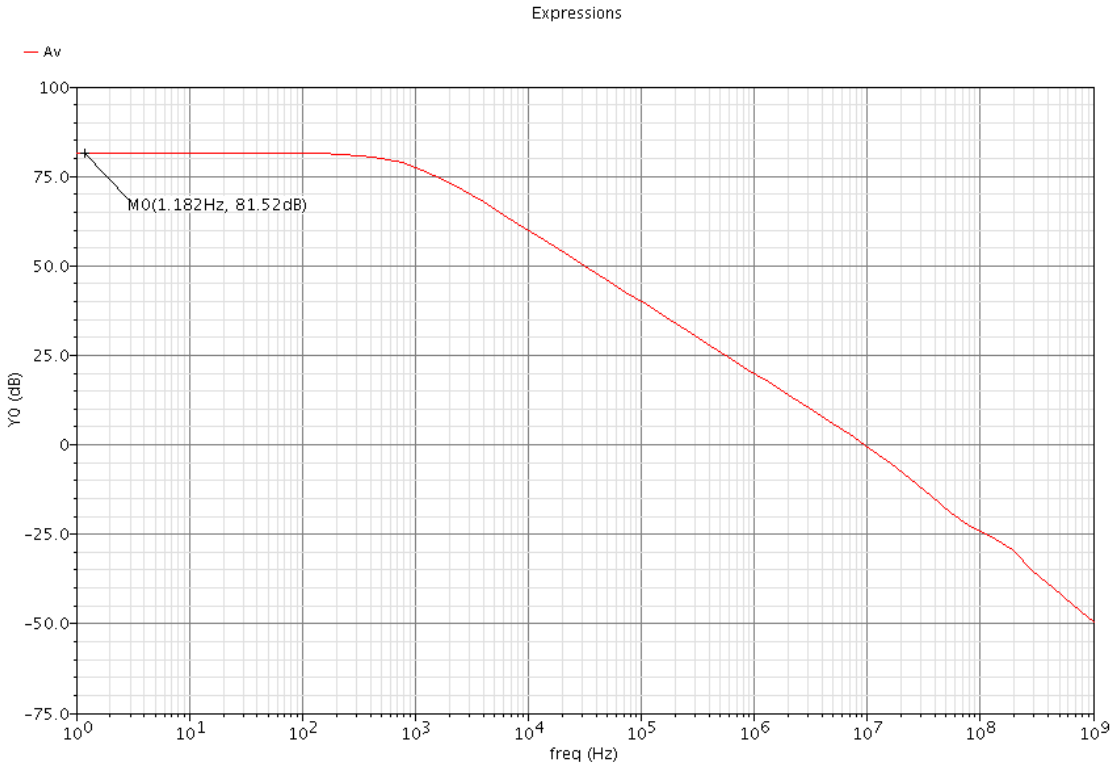

Figure 12: Telescopic gain bode plot

Conclusion:

In this lab we designed a differential amplifier, one of the building blocks of electronics. Through the process of designing first a basic differential amplifier and then a telescopic differential amplifier I was able to learn a lot about the design flow and about the different amplifier properties. I look forward to making a two stage differential amplifier in the following lab and learning more about how to design a fully functioning high gain operational amplifier.