Subject: Report for Analog Lab 1

Design a Single Stage Differential Amplifier

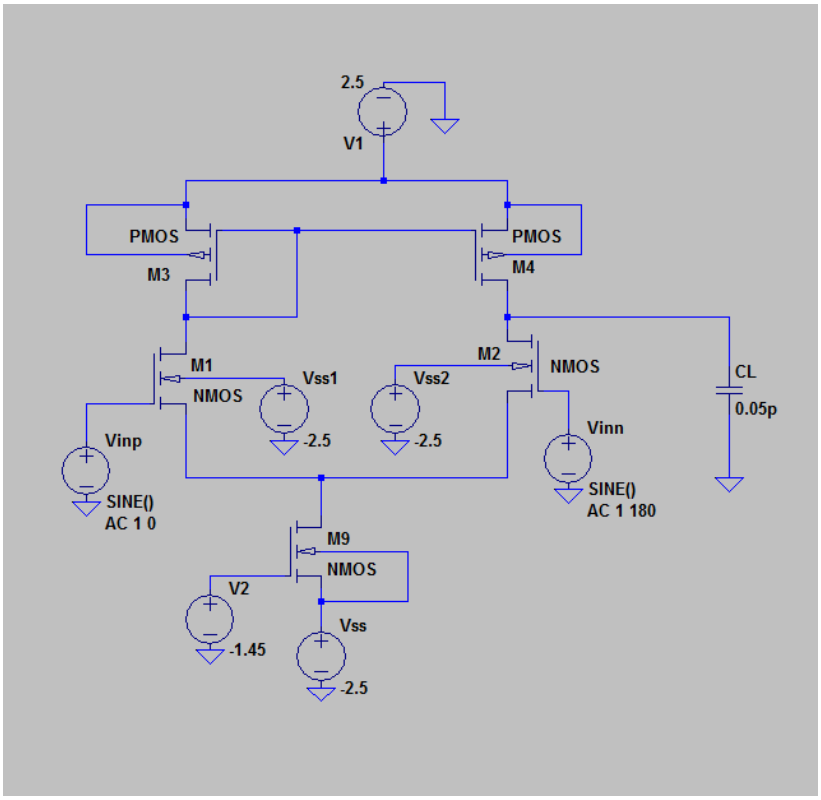

Figure 1 The Circuit of a Single Stage Differential Amplifier

Gain and Phase Plot at the output

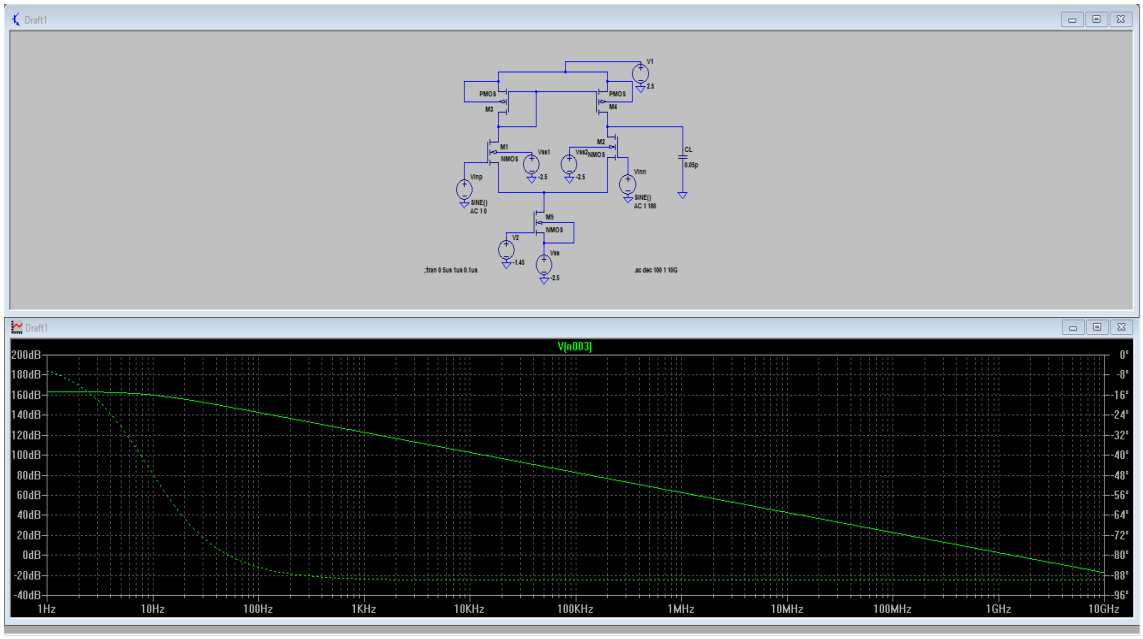

Figure 2 The Gain and Phase Plot at the output

DC gain can be found at 1 Hz ⇒ DC gain=160 dB

Layout

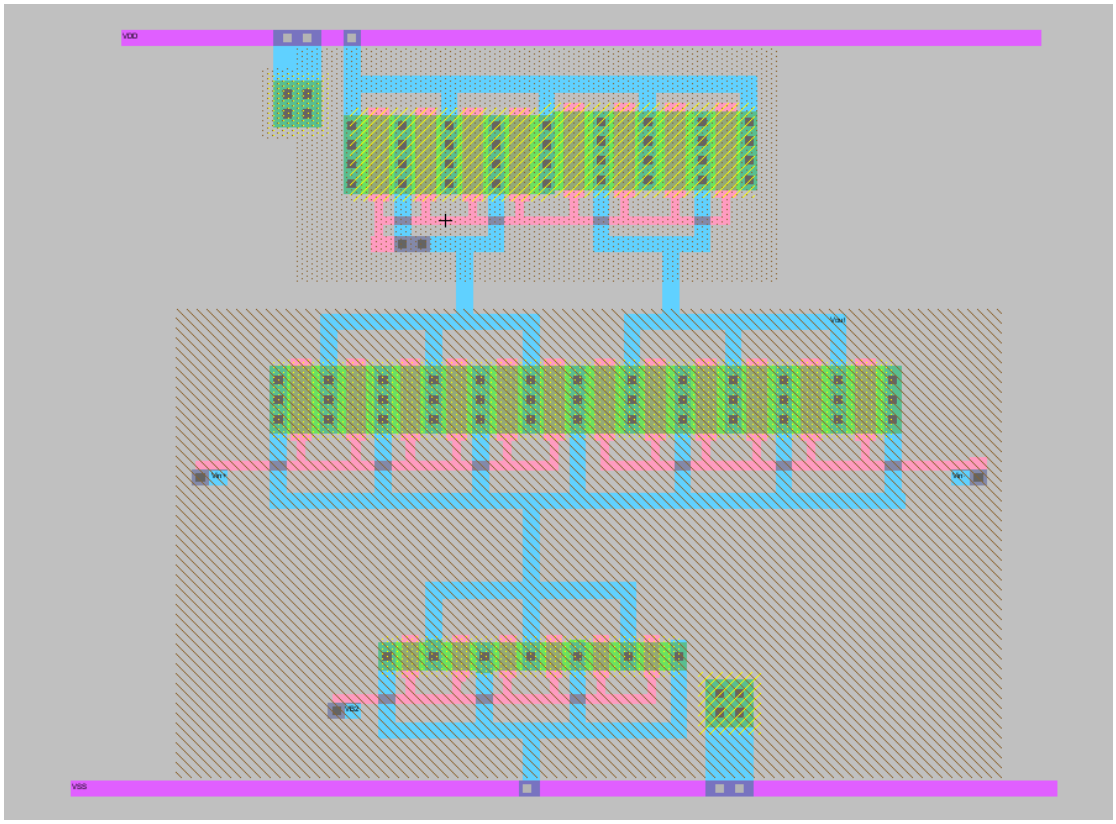

Figure 3 The Layout of the Single Stage Differential Amplifier

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Running DRC with area bit on, extension bit on, Mosis bit

Checking again hierarchy .... (0.001 secs)

Found 35 networks

0 errors and 0 warnings found (took 0.003 secs)

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Checking Wells and Substrates in 'lab3_2168605:diffamp{lay}' ...

Geometry collection found 115 well pieces, took 0.003 secs

Geometry analysis used 4 threads and took 0.005 secs

NetValues propagation took 0.0 secs

Checking short circuits in 3 well contacts

Additional analysis took 0.0 secs

No Well errors found (took 0.008 secs)

Thus, the layout passes DRC, ERC.