Learning Outcomes

- **Small signal analysis and transistor biasing**

• Apply small signal models to the solution of complex circuits (e.g. cascodes, current conveyors), including pole-zero calculations;
• Design circuits to bias transistors in the correct operating regime;

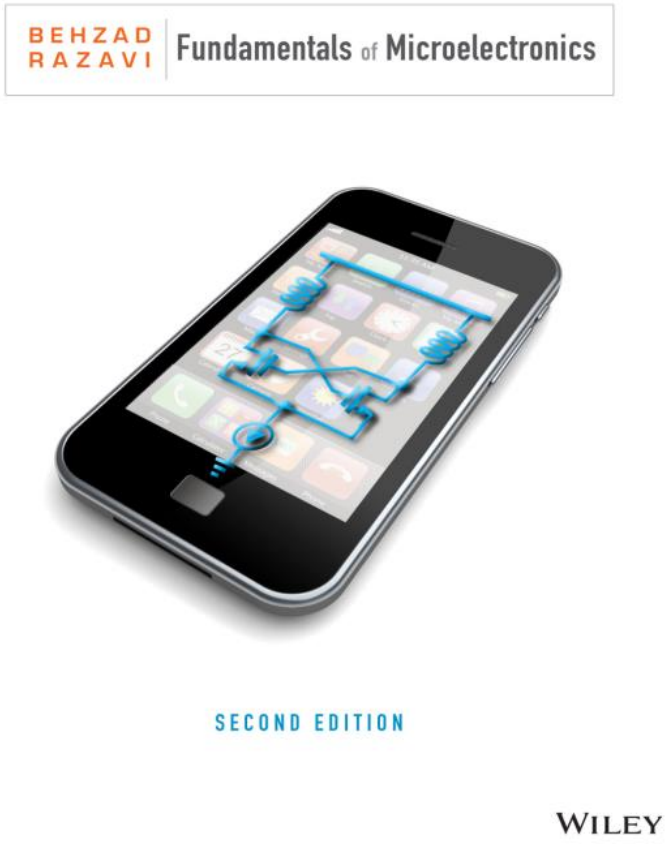
- **Fundamental circuit design blocks and their performance**

• Perform analyses for fundamental circuit blocks, including **current mirrors** (for low-voltage, wide swing application), amplifiers (2 stage folded cascode, source degeneration etc.), bandgap references, **switched capacitor networks**, **Gm-C filters**, and drivers;
• Evaluate the benefits of specific circuit blocks to design solutions, given a range of non-orthogonal system specifications;
• **Frequency Response**

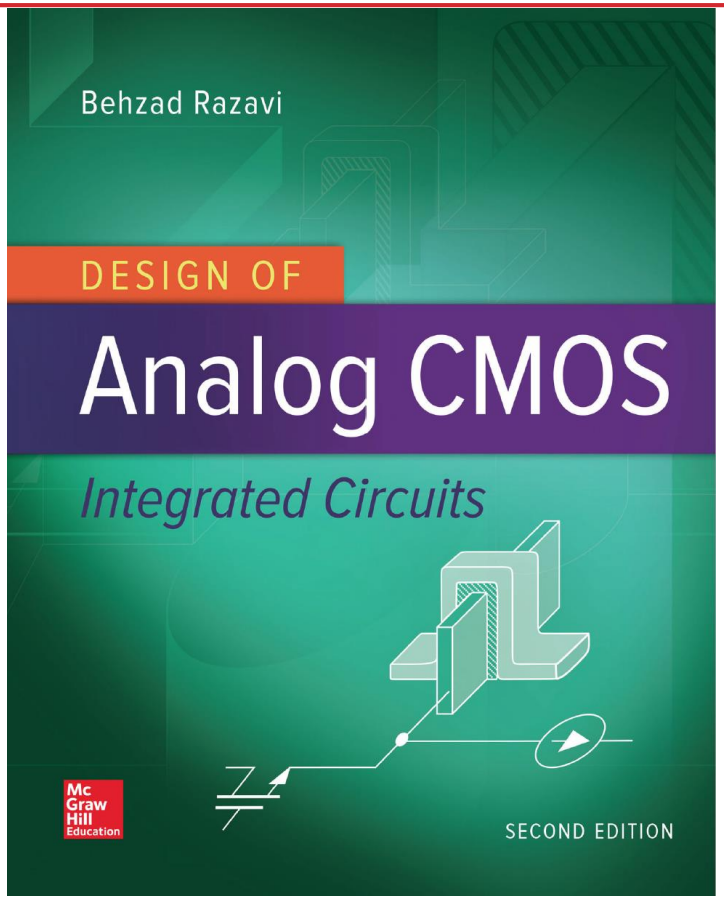
- **Analog-to-Digital Conversion(ADC) and Digital-to-Analog Conversion(DAC)**

- **Layout design**

Learning Outcomes



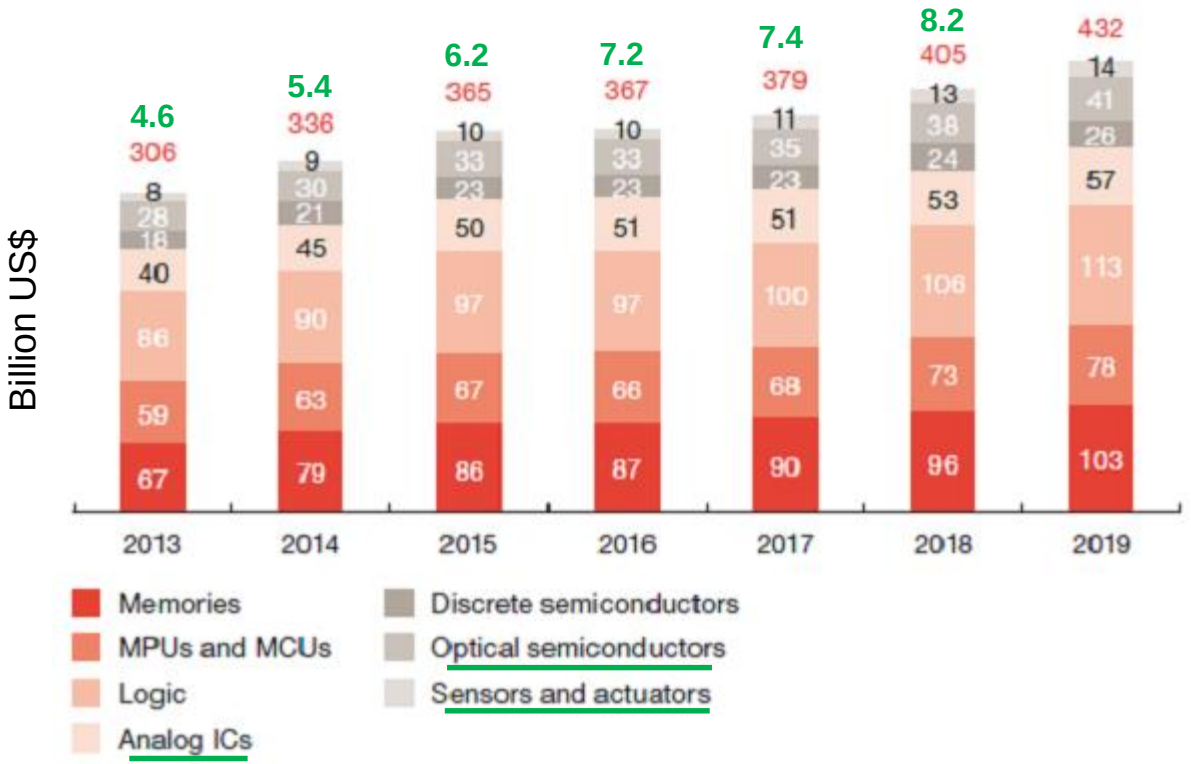
Fundamental of Microelectronics
Behzad Razavi
2nd Edition



Design of Analog CMOS Integrated Circuits
Behzad Razavi
2nd Edition

IC Design Overview

Global Integrated Circuit (IC) design Market



Mostly Silicon (CMOS) based devices

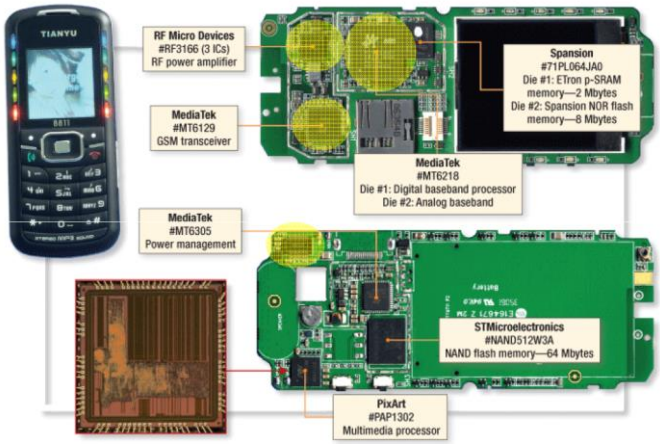
Source:
Forbes, IC Insights
http://blogs-images.forbes.com/greatspeculations/files/2015/09/IoT-PWC-Gartner-Graphic1.png

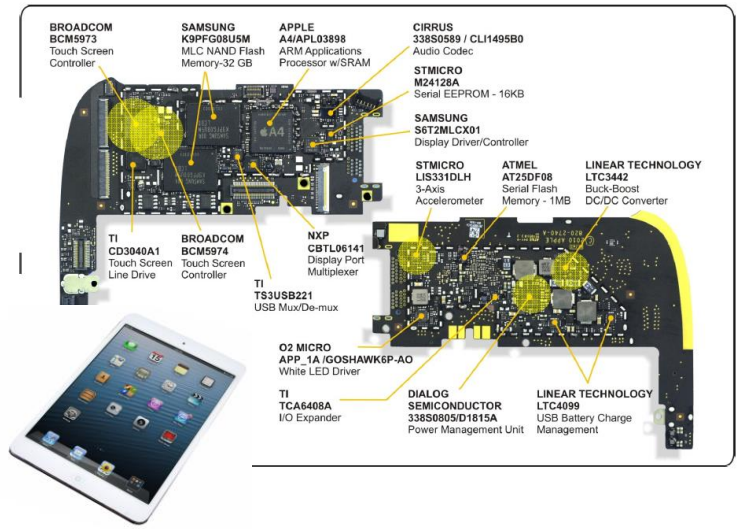
Cray-2 Supercomputer

Why Analog

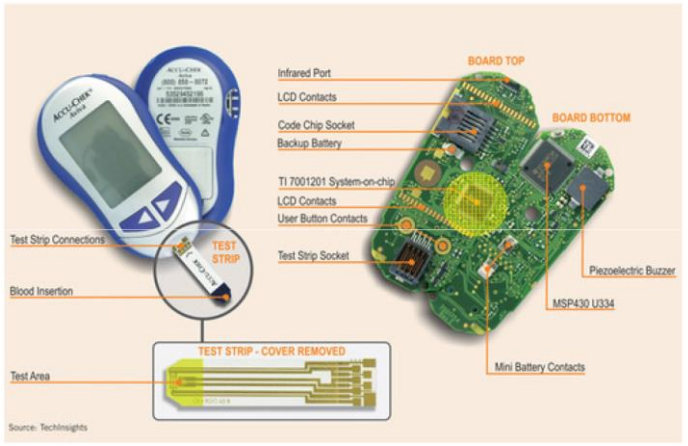
- Real-world signals are analog: continuous in amplitude, and continuous in time.
- Modern signal processing has evolved to be digital or discrete-time. Most signal processing is performed in the digital domain.
- Most analog systems perform the sensing, amplification, transmission and reception of *real-world* signals, before they can be processed by digital systems.

Why Analog?


RF Micro Devices
#RF3166 (3 ICs)
RF power amplifier
MediaTek
#MT6129
GSM transceiver
Spansion
#71PL064JA0
Die #1: ETron p-SRAM memory—2 Mbytes
Die #2: Spansion NOR flash memory—8 Mbytes
MediaTek
#MT6218
Die #1: Digital baseband processor
Die #2: Analog baseband
MediaTek
#MT6305
Power management
STMicroelectronics
#NAND512W3A
NAND flash memory—64 Mbytes
PixArt
#PAP1302
Multimedia processor

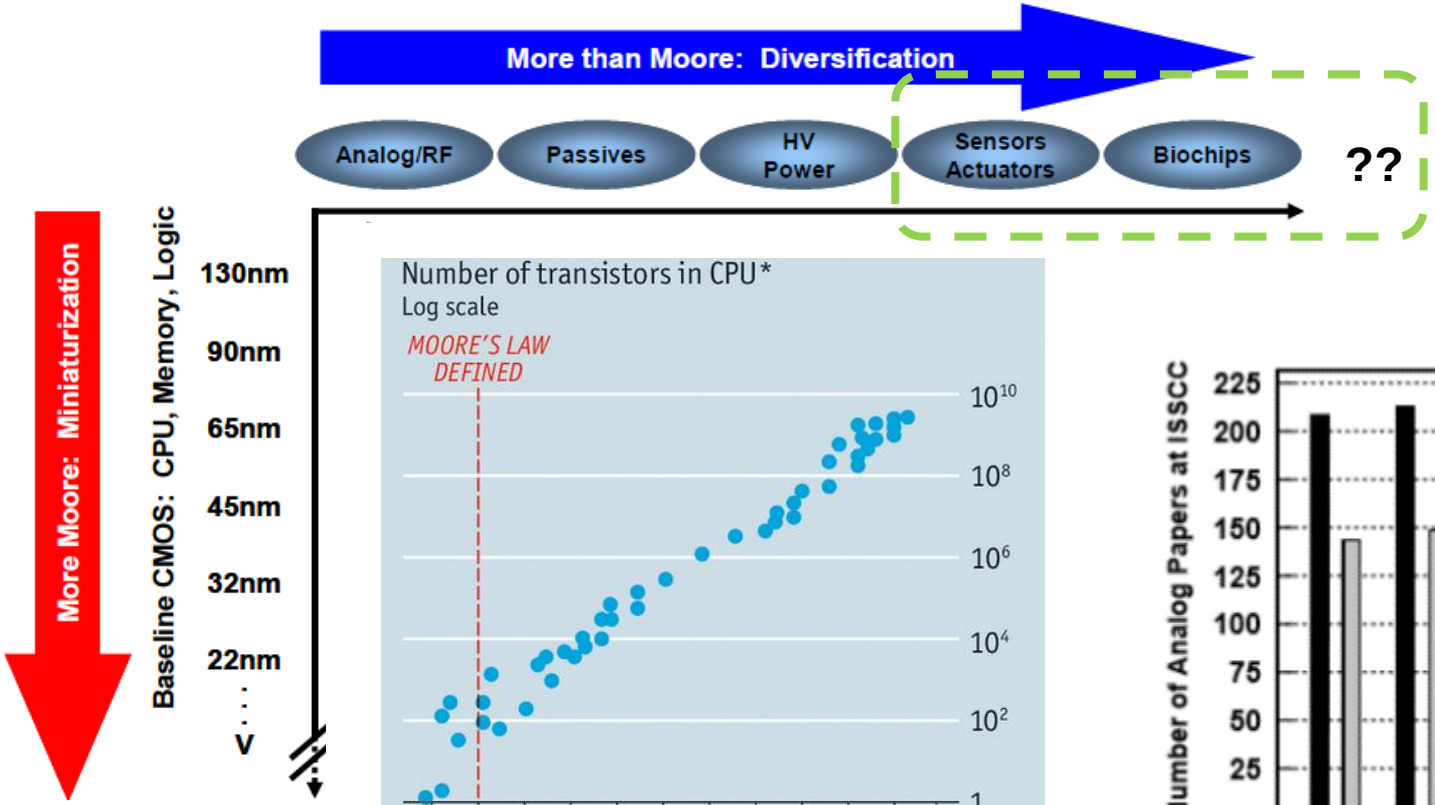

BROADCOM
BCM5973
Touch Screen Controller
SAMSUNG
K9PFG08U5M
MLC NAND Flash Memory-32 GB
APPLE
A4/APL03898
ARM Applications Processor w/SRAM
CIRRUS
338S0589 / CLI1495B0
Audio Codec
STMICRO
M24128A
Serial EEPROM - 16KB
SAMSUNG
S6T2MLCX01
Display Driver/Controller
STMICRO
LIS331DLH
3-Axis Accelerometer
ATMEL
AT25DF08
Serial Flash Memory - 1MB
LINEAR TECHNOLOGY
LTC3442
Buck-Boost DC/DC Converter
TI
CD3040A1
Touch Screen Line Drive
BROADCOM
BCM5974
Touch Screen Controller
NXP
CBTL06141
Display Port Multiplexer
TI
TS3USB221
USB Mux/De-mux
O2 MICRO
APP_1A /GOSHAWK6P-AO
White LED Driver
TI
TCA6408A
I/O Expander
DIALOG SEMICONDUCTOR
338S0805/D1815A
Power Management Unit
LINEAR TECHNOLOGY
LTC4099
USB Battery Charge Management

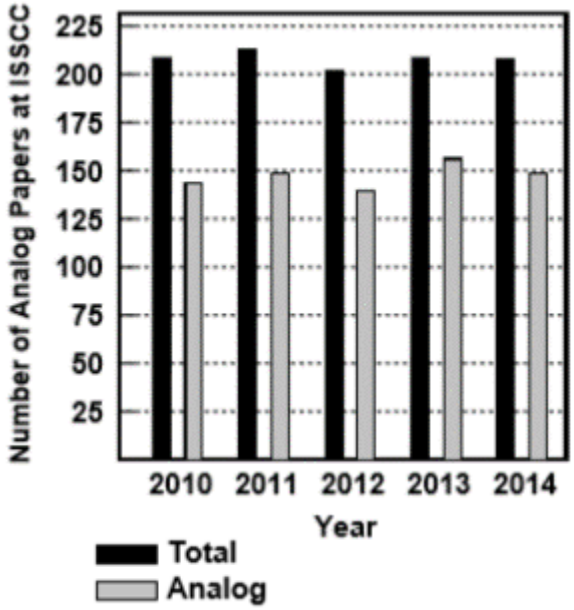

Broadcom
Wi-Fi/Bluetooth/NFC
FM BCM43342
Skyworks
Wi-Fi LNA + switch and PA
STM IMU
LSM6DS3
dialog
Dialog
Power Management Unit
D2238A
ADI Touch Controller
AD7149
Maxim Integrated
Audio Codec
Audio Amp
IDT
IDT
Wireless charger
P9022
ams
AMS
NFC Signal Booster
AS3923
NXP
NFC controller
ELPIDA
Elpida
512Mb SRAM Memory
P440AAC
CPU Apple APL0778
TOSHIBA
SanDisk
Toshiba/SanDisk
8Gb Flash Memory
STM µC
STM32
NXP
Interface device


BOARD TOP
BOARD BOTTOM
Infrared Port
LCD Contacts
Code Chip Socket
Backup Battery
TI 7001201 System-on-chip
LCD Contacts
User Button Contacts
Test Strip Connections
TEST STRIP
Test Strip Socket
Piezoelectric Buzzer
Blood Insertion
MSP430 U334
TEST STRIP - COVER REMOVED
Test Area
Mini Battery Contacts
Source: TechInsights

Moor's law and analog design

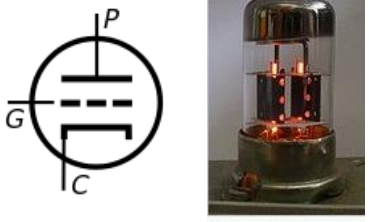
Moore's Law and Beyond



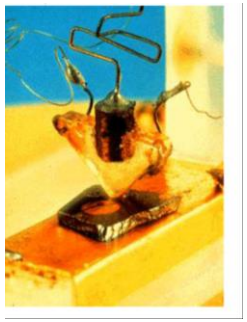


A little history

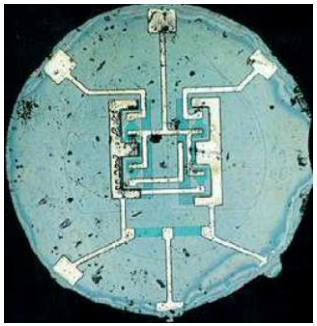
- … vacuum tubes, discrete components
- 1947: First integrated transistor
- 1953: Sonotone (hearing aid) contained 5 transistors
- 1950s: Fairchild, Texas instruments
- 1958: First Integrated circuits
- 1960s: MOS became popular
- 1965: Moore's Law …



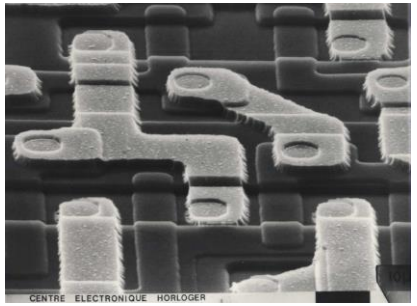
Used even
in 1960s!



William Shockley,
John Bardeen and
Walter H.Brattein

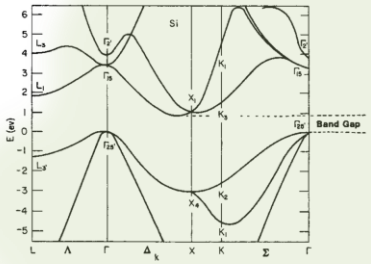


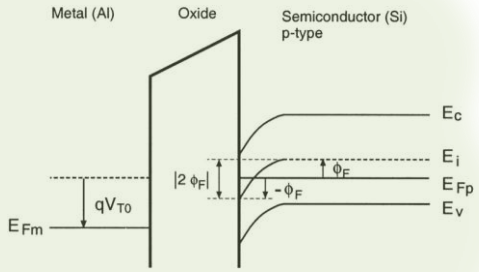
First IC
(Fairchild)

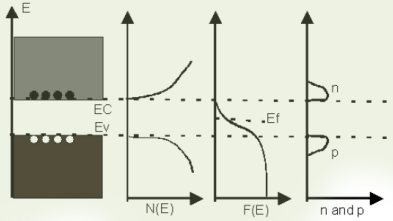


MOS IC
(Intel)

A little history

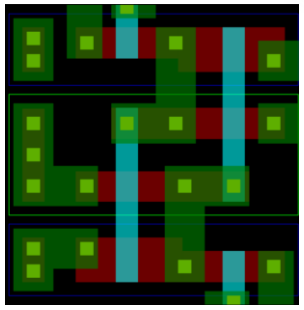




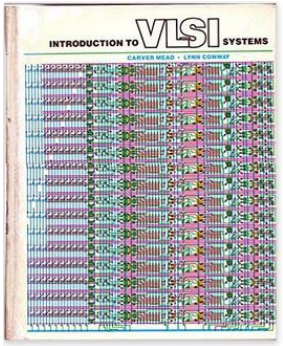


William Shockley, John Bardeen and Walter H.Brattein

From lot's of Quantum mechanics to few simple equations



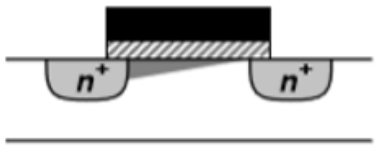
Carver Mead Lyn Conway



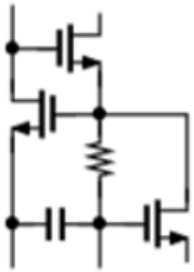
Formal rules of IC design

Transistor Abstraction

Device

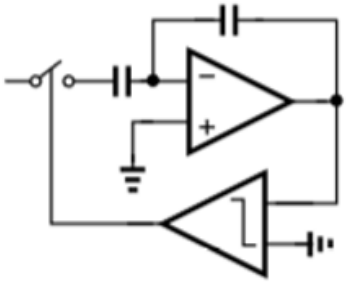


Circuit

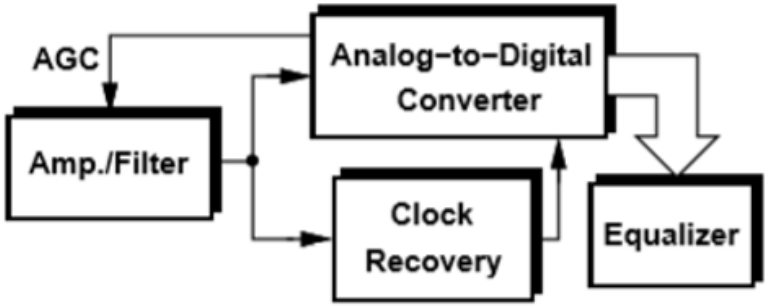


- Switching between levels of abstraction is necessary for
  - understanding the details of operation.
  - optimizing the overall performance.
- Interaction between all groups in industry is essential for high performance and low cost designs.

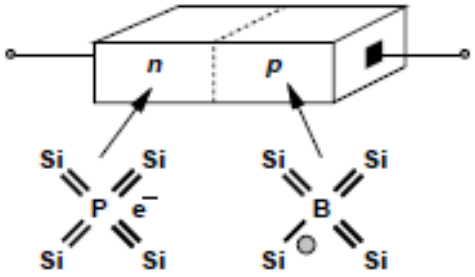
Architecture

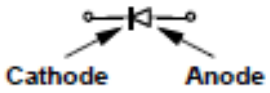


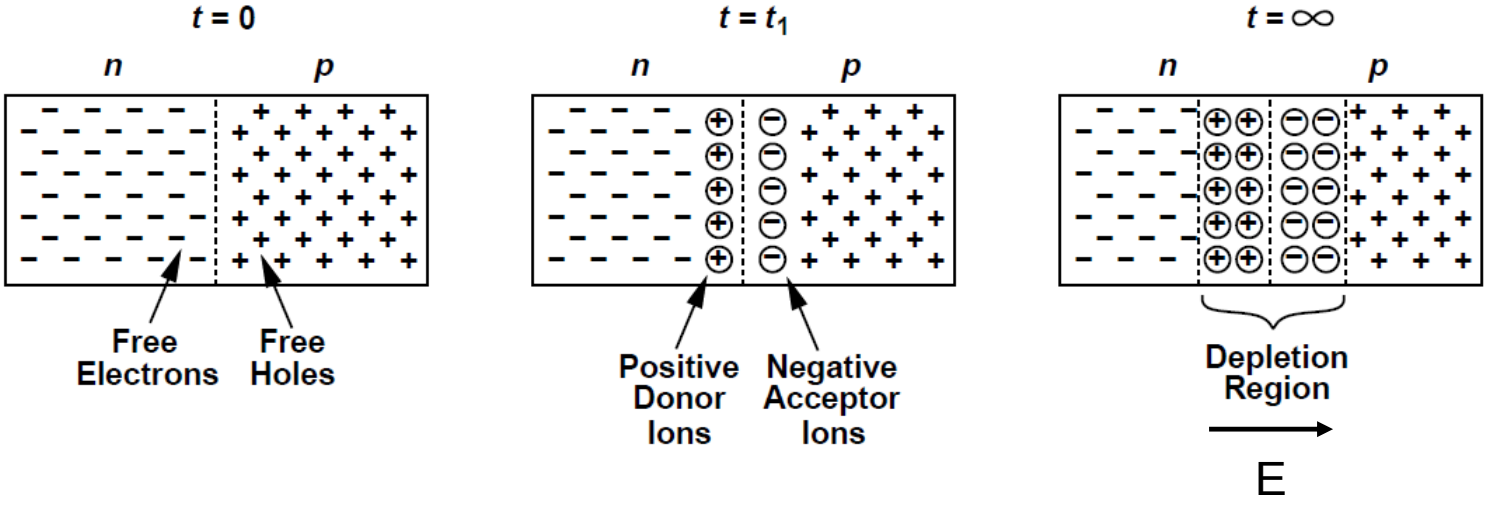
System



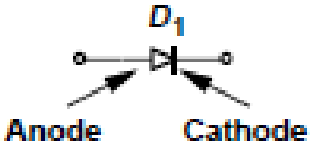
Basic semiconductor devices

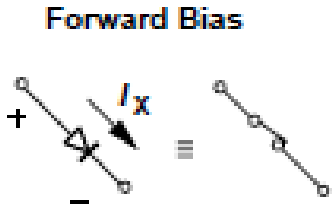


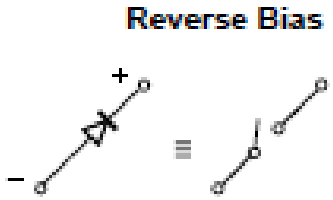


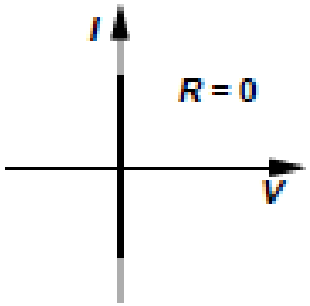


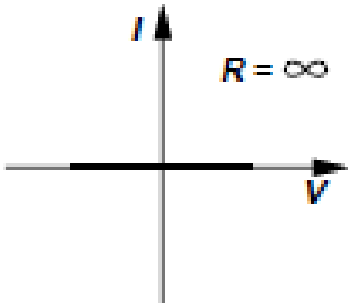
Diode

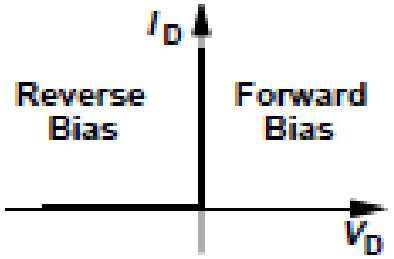

D_1
Anode
Cathode


Forward Bias
+
I_X
≡
–

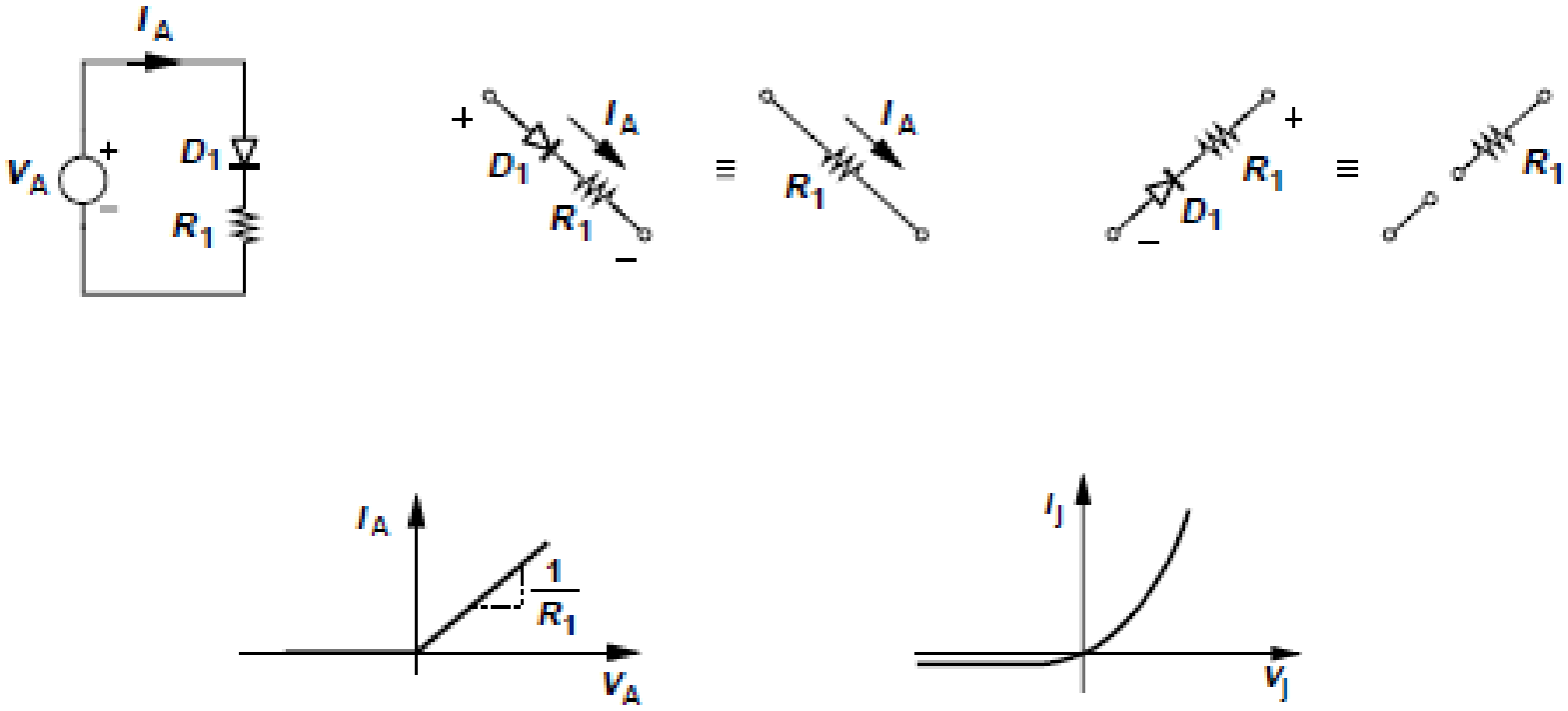

Reverse Bias
+
–
≡


I
R = 0
V

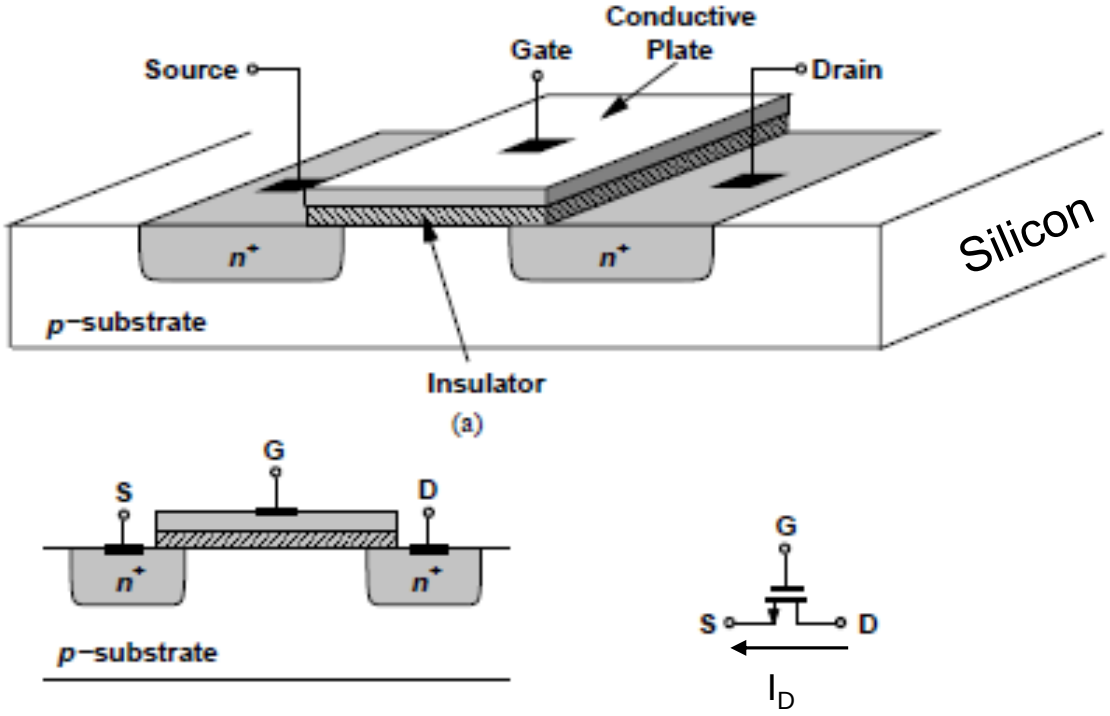

I
R = ∞
V


I_D
Reverse Bias
Forward Bias
V_D

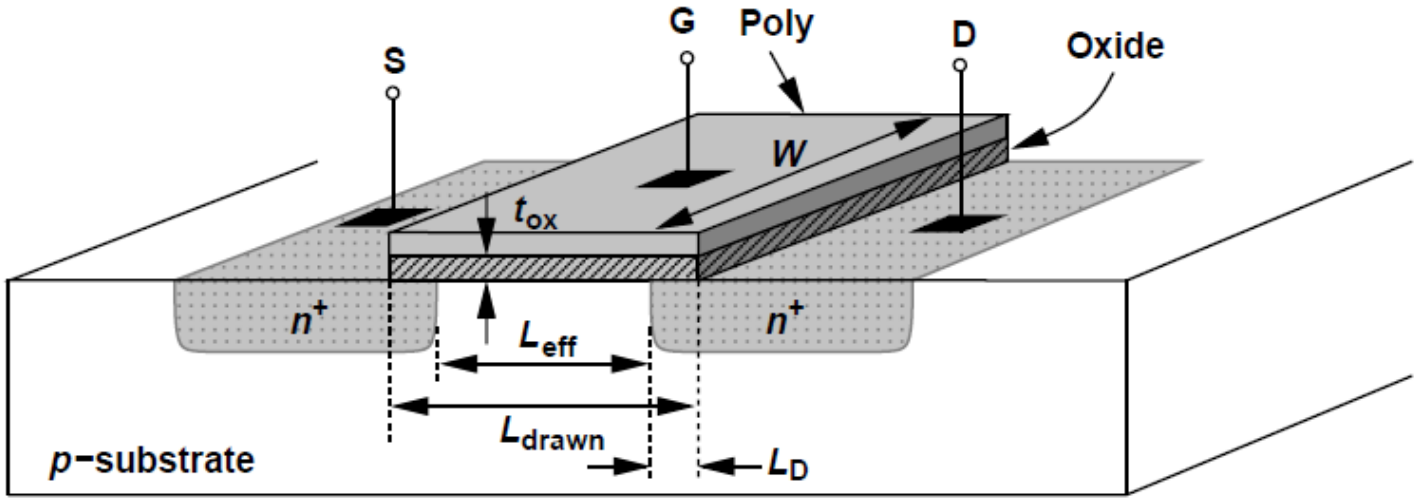
Diode: Real

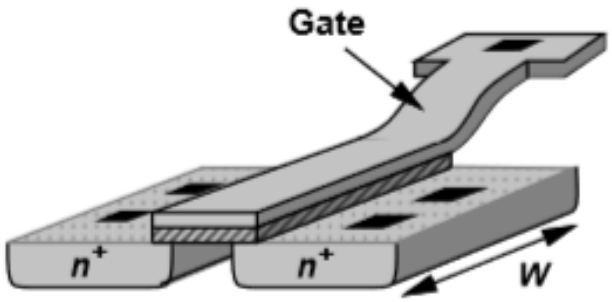


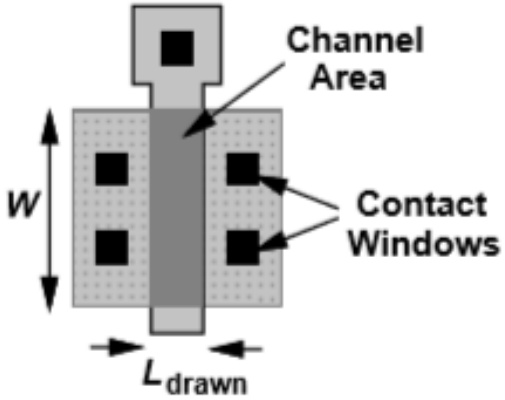
Transistor


Source
Gate
Conductive Plate
Drain
Silicon
n+
n+
p−substrate
Insulator
(a)
G
S
D
n+
n+
p−substrate
G
S
D
ID

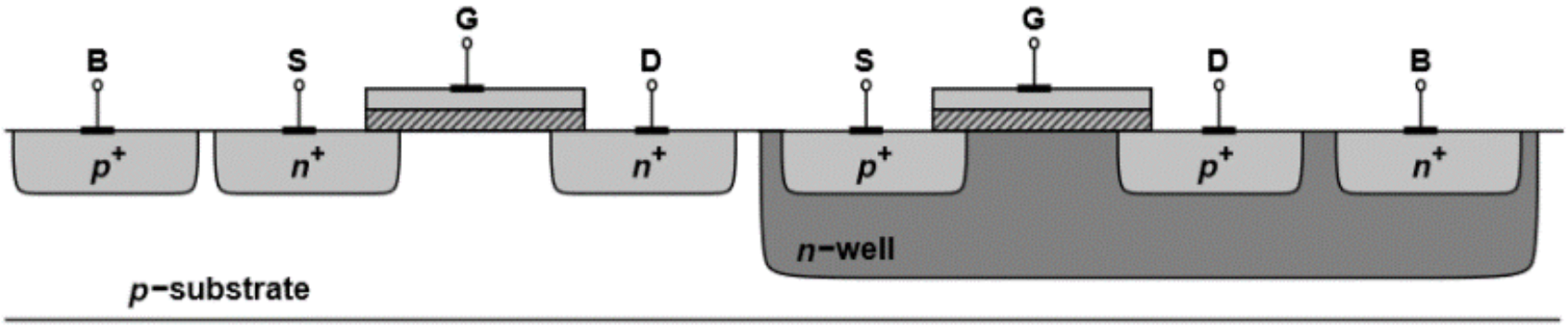
Transistor


S
G
Poly
D
Oxide
W
t_{ox}
n^+
n^+
L_{eff}
L_{drawn}
L_D
p−substrate

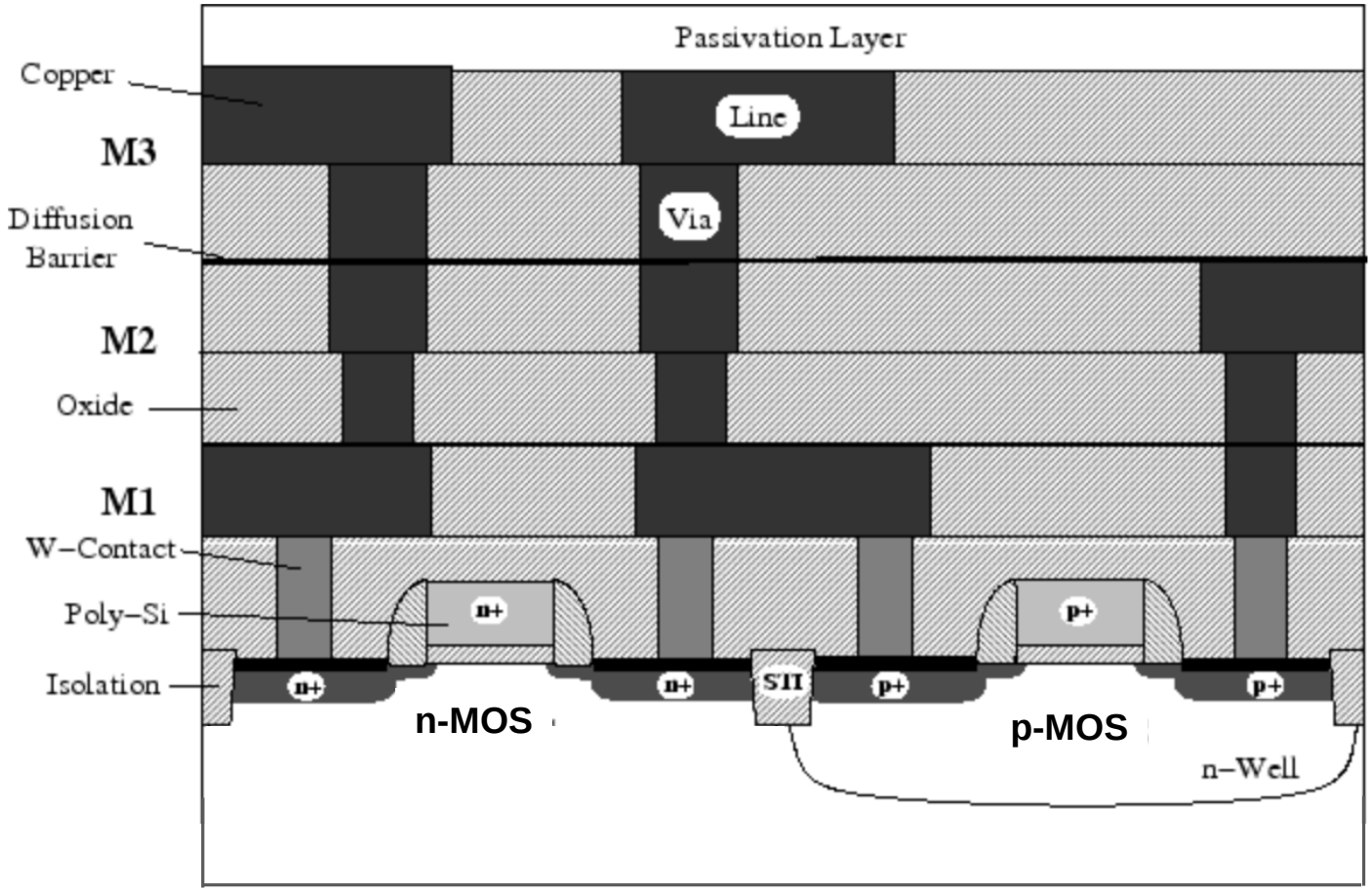

Gate
n^+
n^+
W


Channel
Area
W
Contact
Windows
L_{drawn}

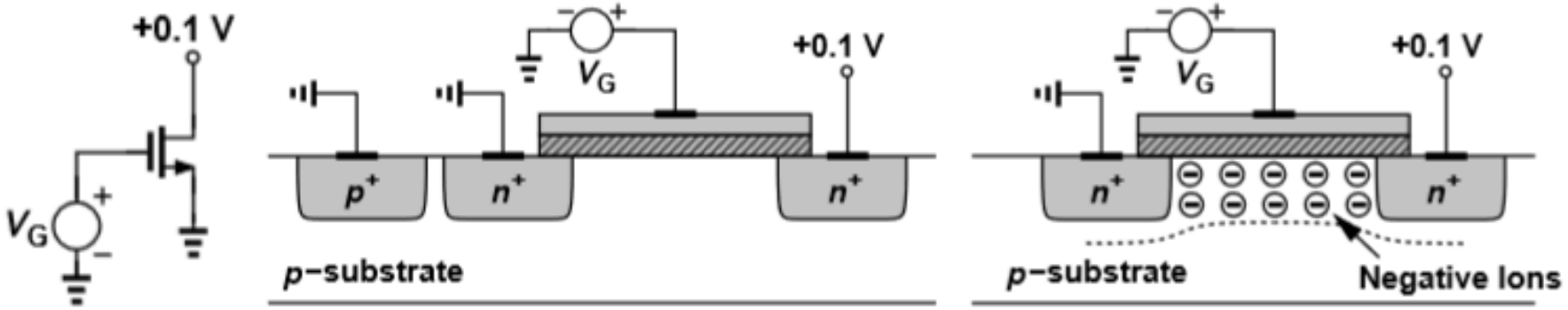
Transistor



Transistor

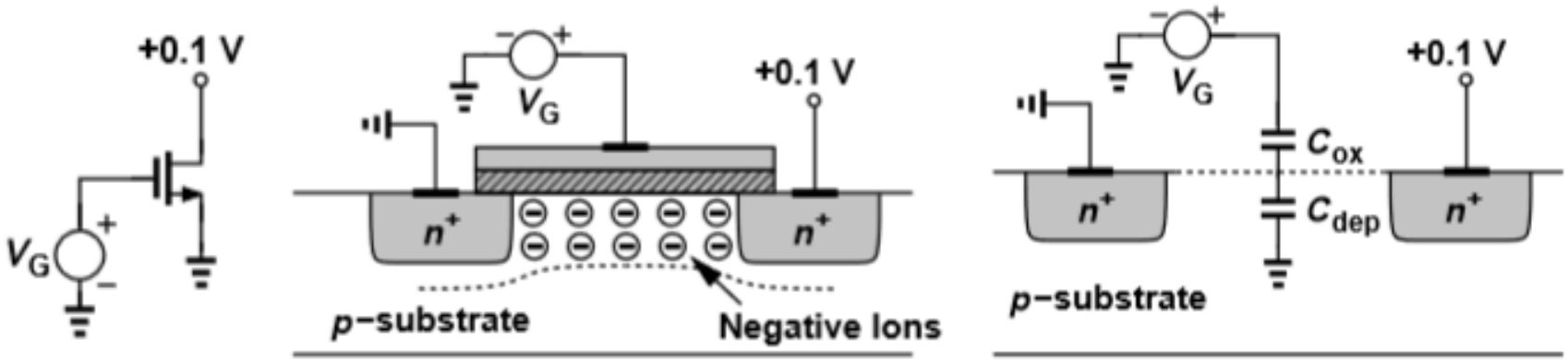

Passivation Layer
Copper
Line
M3
Via
Diffusion
Barrier
M2
Oxide
M1
W–Contact
Poly–Si
Isolation
n+
n+
n+
STI
p+
p+
p+
n-MOS
p-MOS
n–Well

Transistor



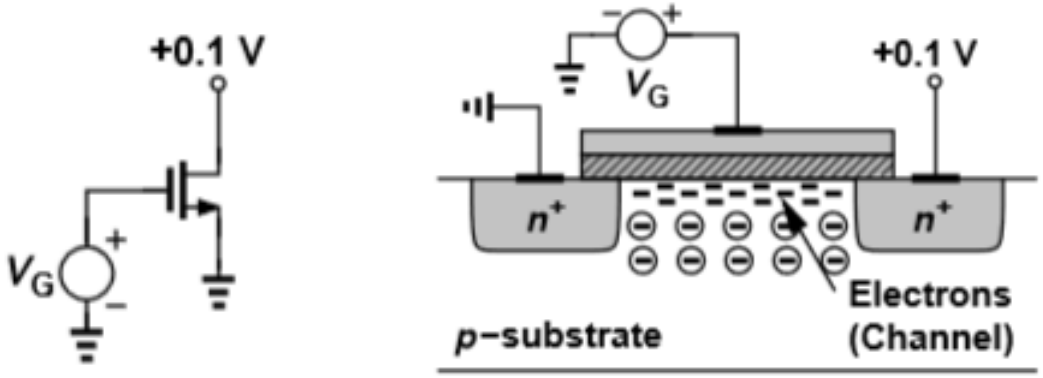
- As V_G increases from zero, holes in *p*-substrate are repelled leaving negative ions behind to form a depletion region.
- There are no charge carriers, so no current flow.

Transistor



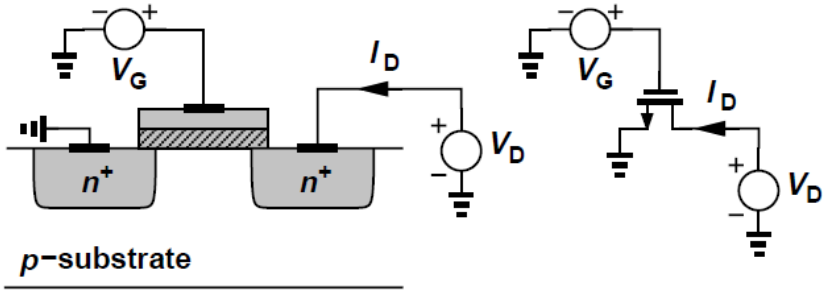
- Increasing V_G further increases the width of the depletion region and the potential at the oxide-silicon interface.
- Structure resembles voltage divider consisting of gate-oxide capacitor and depletion region capacitor in series.

Transistor

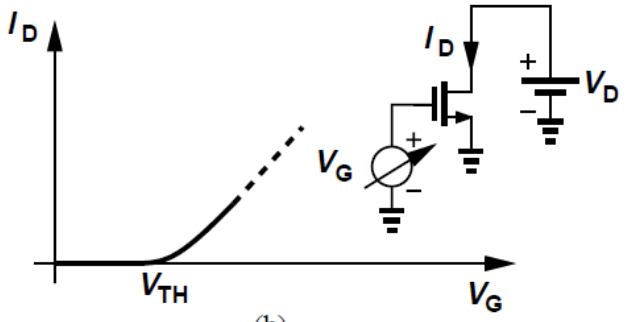


- When interface potential reaches sufficiently positive value, electrons flow from the source to the interface and eventually to the drain.
- This creates a channel of charge carriers (inversion layer) beneath the gate oxide.
- The value of V_G at which the inversion layer occurs is the threshold voltage (V_{TH}).

Transistor: NMOS

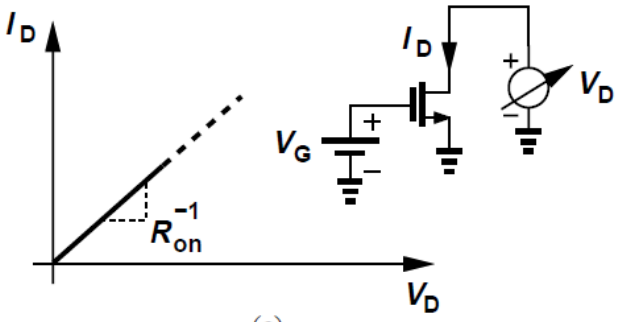


(a)



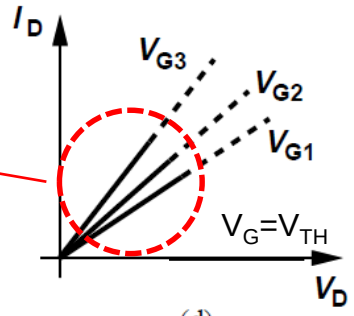
(b)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$



(c)

Deep triode region

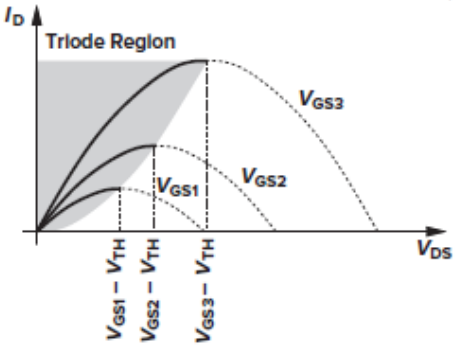


(d)

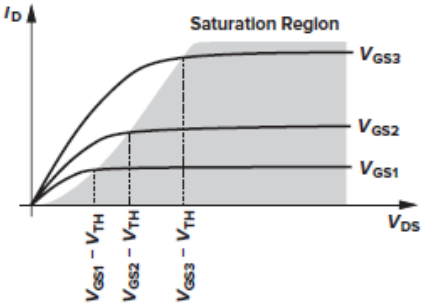
V_{DS} <<$2(V_{GS} - V_{TH})$,

$$I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

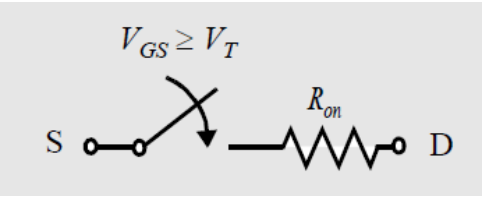
$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$



- overdrive voltage: $V_{GS} - V_{TH}$
- With the condition, V_{DS} <<$2(V_{GS} - V_{TH})$, we say the device operates in the deep triode region.



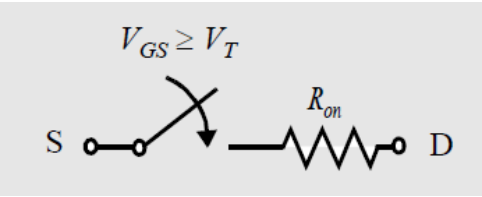
Transistor Switch



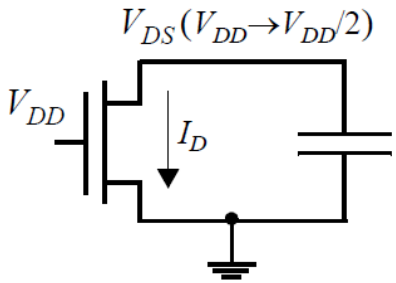
$$R_{eq} = \text{average}_{t=t_1 \ldots t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)dt$$

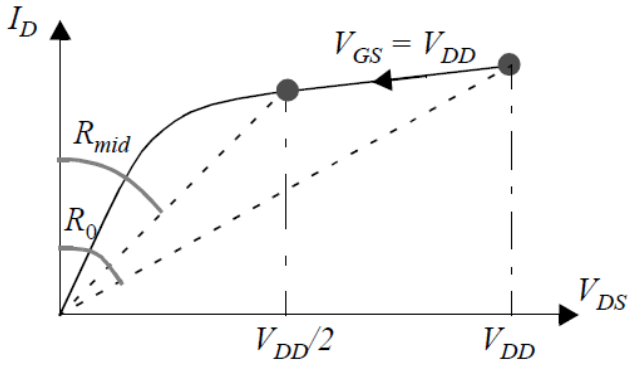
$$\approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

Transistor Switch



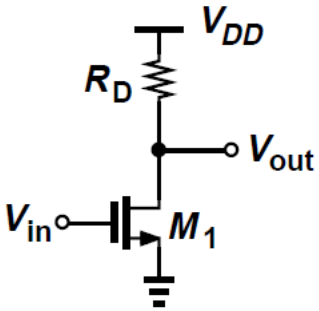
$$\approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

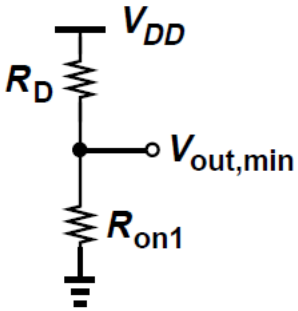


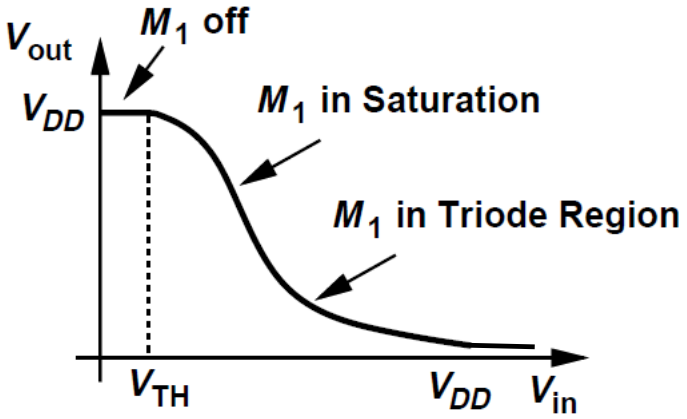


$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter



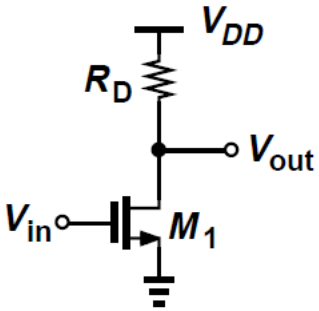


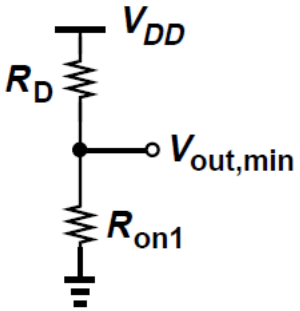


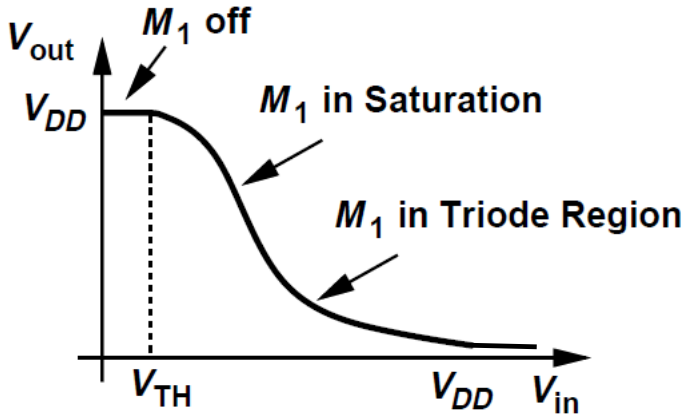
$$V_{out} = V_{DD} - I_D R_D$$
$$= V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2,$$

$$V_{out,min} = V_{DD} - R_D I_{D,max}$$
$$= V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D[2(V_{DD} - V_{TH})V_{out,min} - V_{out,min}^2].$$

Inverter





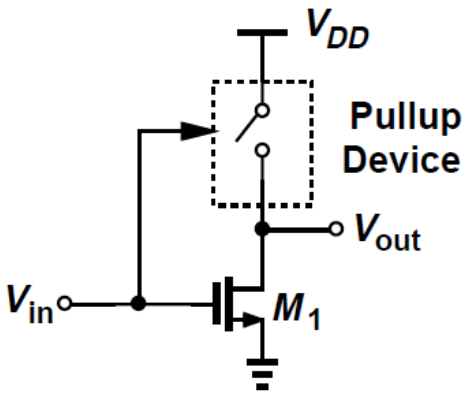


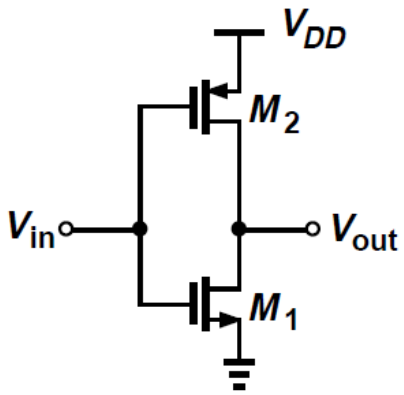
$$V_{out} = V_{DD} - I_D R_D$$
$$= V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2,$$

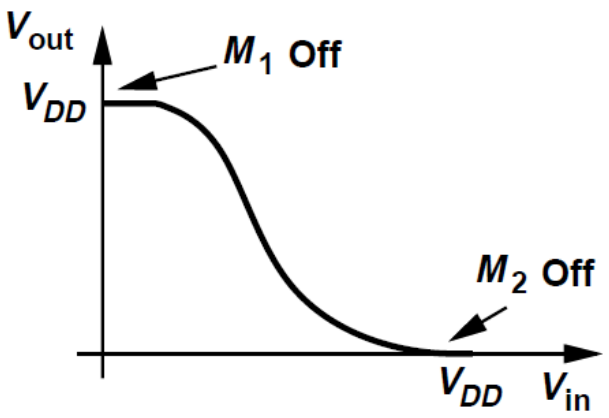
$$V_{out,min} = V_{DD} - R_D I_{D,max}$$
$$= V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D[2(V_{DD} - V_{TH})V_{out,min} - V_{out,min}^2].$$

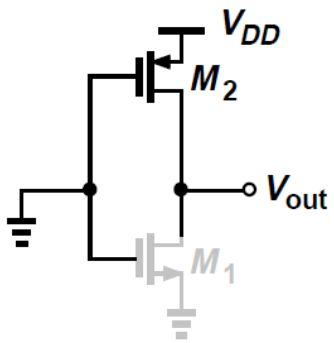
$$V_{out,min} \approx -\frac{V_{DD}}{1 + \mu_n C_{ox}\frac{W}{L}R_D(V_{DD} - V_{TH})}.$$

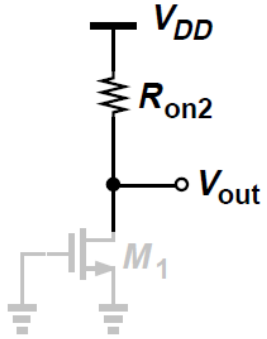
Inverter

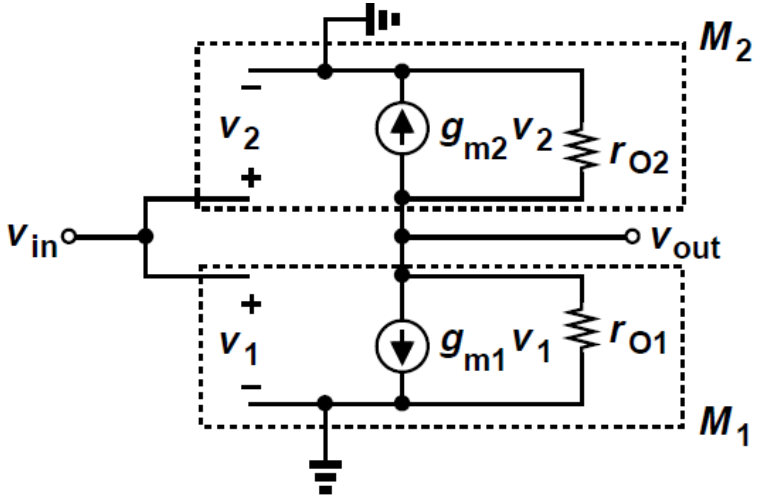

V_{DD}
Pullup
Device
V_{out}
V_{in}
M_1


V_{DD}
M_2
V_{in}
V_{out}
M_1

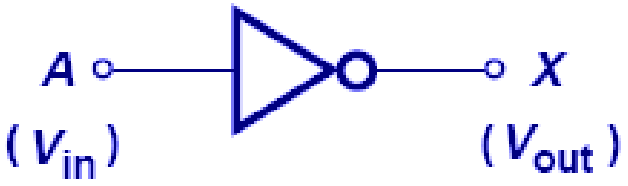

V_{out}
M_1 Off
V_{DD}
M_2 Off
V_{DD}
V_{in}

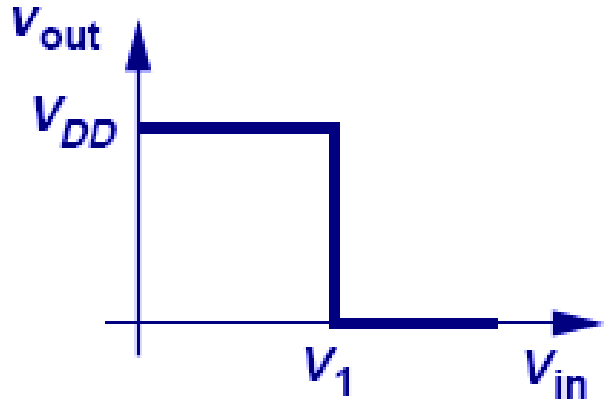

V_{DD}
M_2
V_{out}
M_1


V_{DD}
R_{on2}
V_{out}
M_1

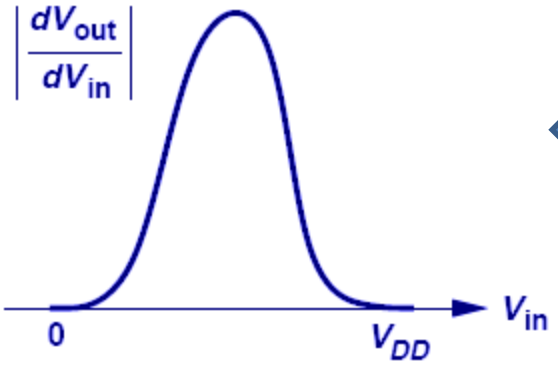

M_2
v_2
$g_{m2}v_2$
r_{O2}
v_{in}
v_{out}
v_1
$g_{m1}v_1$
r_{O1}
M_1

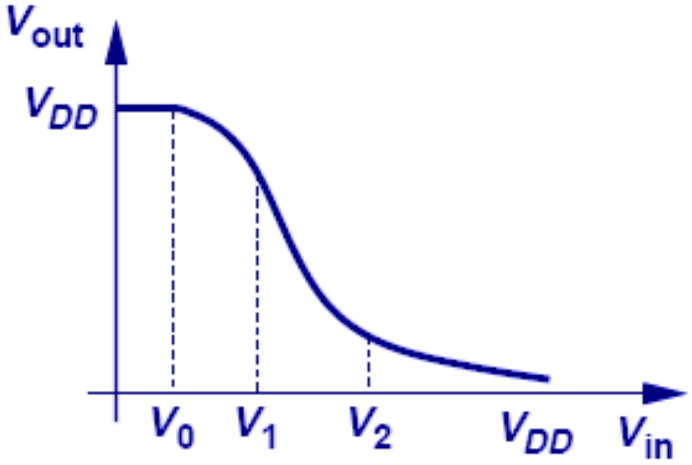
Inverter





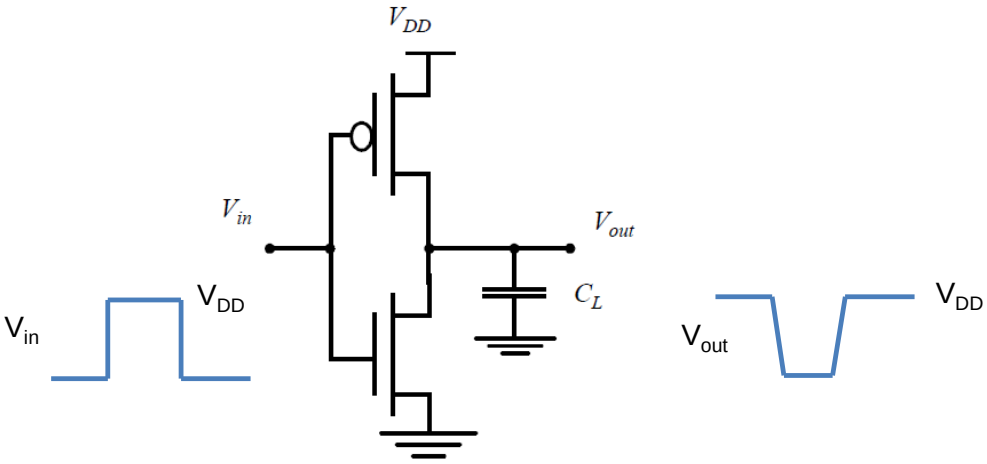
Infinite Transition Region Gain

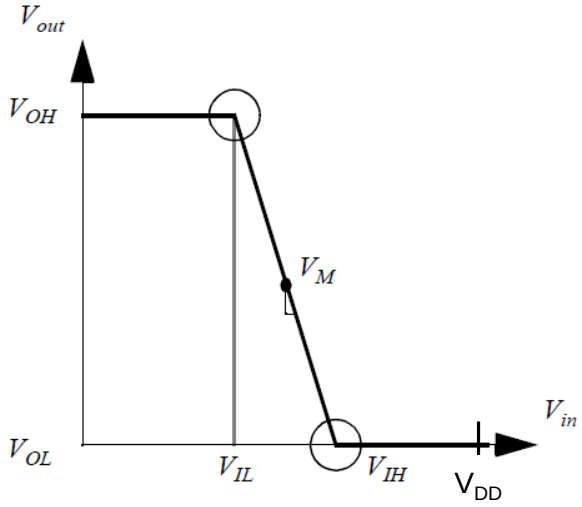


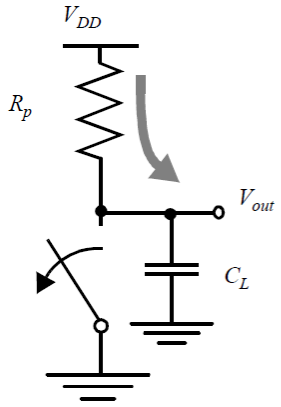


Finite Transition Region Gain

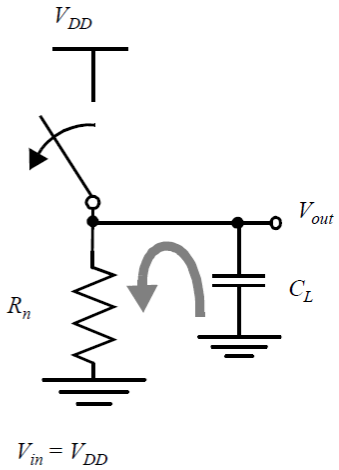
Inverter



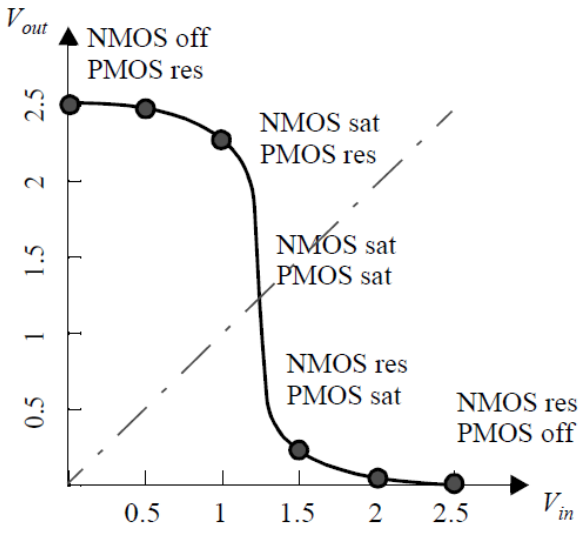




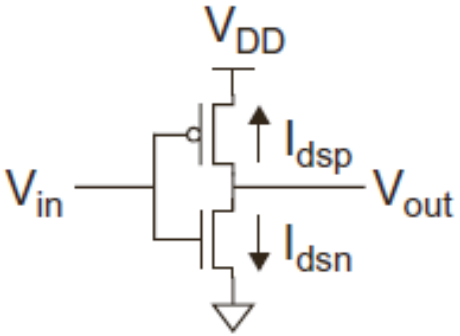
$V_{in} = 0$

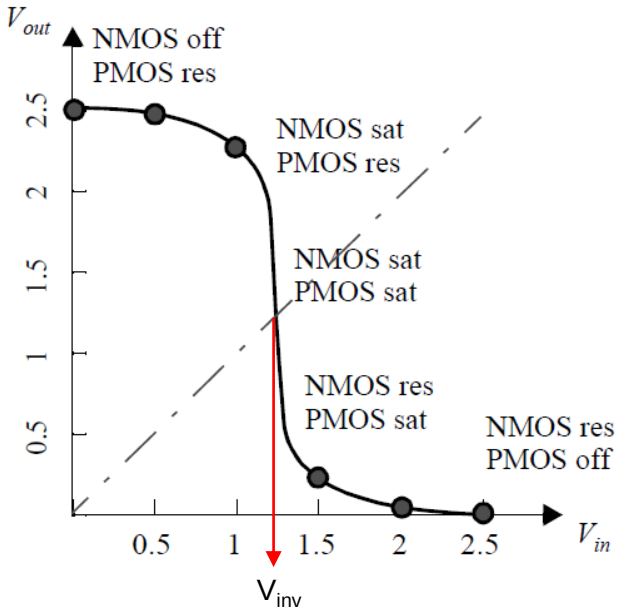


$V_{in} = V_{DD}$



Inverter VTC





$$I_{sat} = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_{DSp} = -I_{DSn}$$

$$V_{GSn} = V_{in} \;;\; V_{GSp} = V_{in} - V_{DD}$$

$$V_{DSn} = V_{out} \;;\; V_{DSp} = V_{out} - V_{DD}$$

$$I_{DN} = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}(V_{in} - V_{TH})^2 \qquad I_{DP} = \tfrac{1}{2}\mu_p C_{ox}\tfrac{W}{L}((V_{in} - V_{DD}) - V_{TH})^2$$

Inverter VTC

Voltage Transfer Characteristics(VTC) of CMOS Inverter

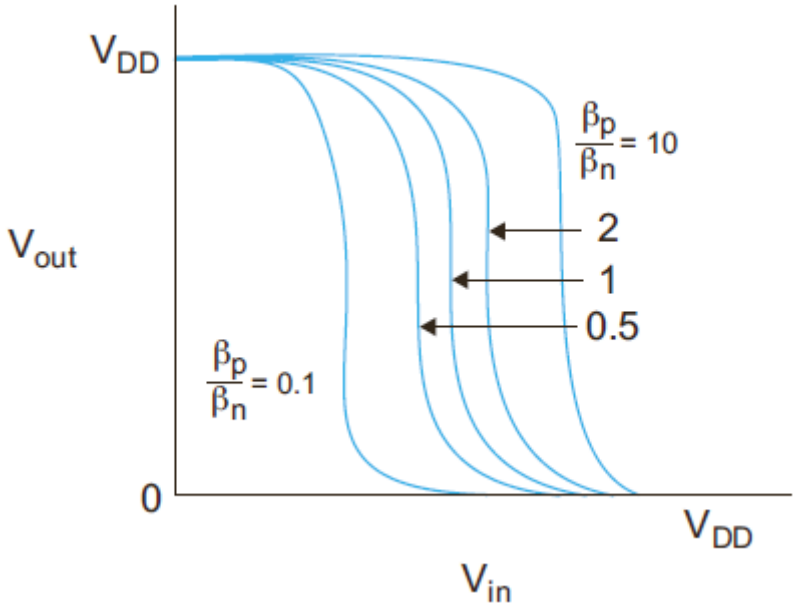
$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$

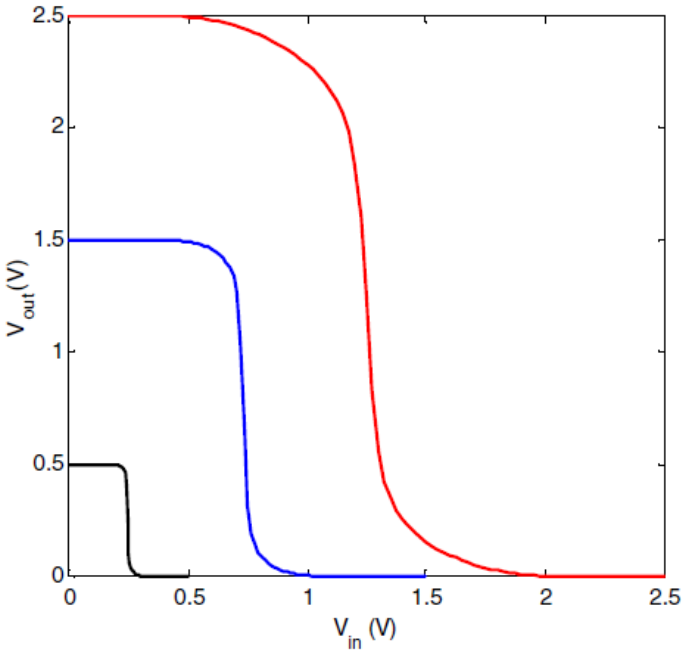
Including velocity saturation

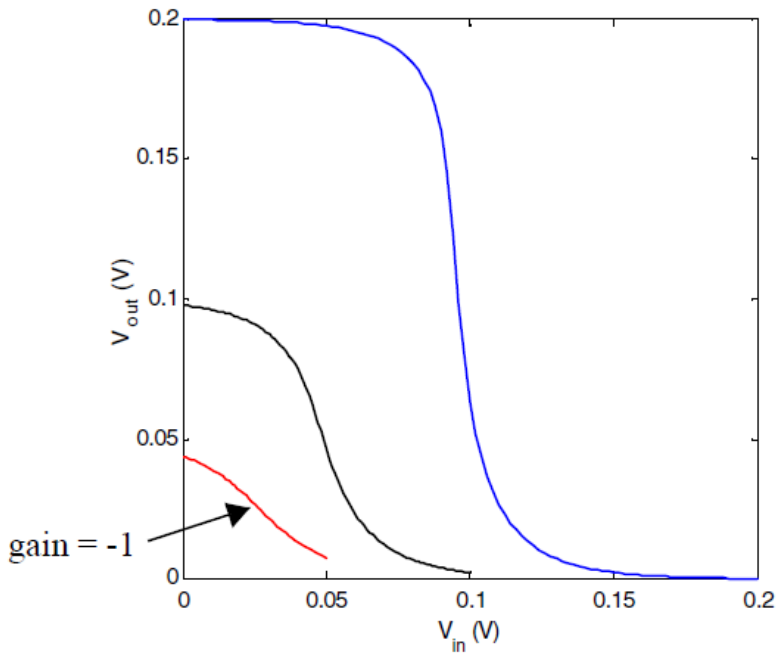
$$\beta = \tfrac{1}{2}\mu C_{ox}\tfrac{W}{L}$$

$$r = \beta_p / \beta_n$$



Inverter VTC



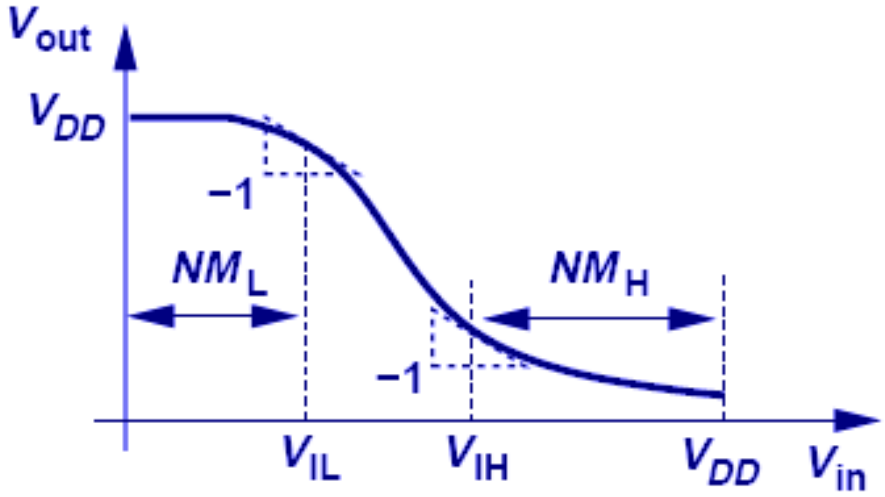


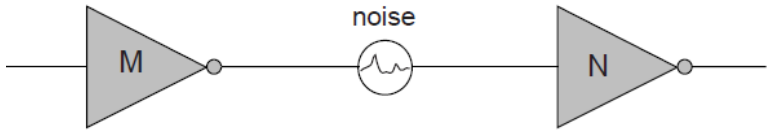
Reducing V_{DD} improves gain…. but up to a certain limit

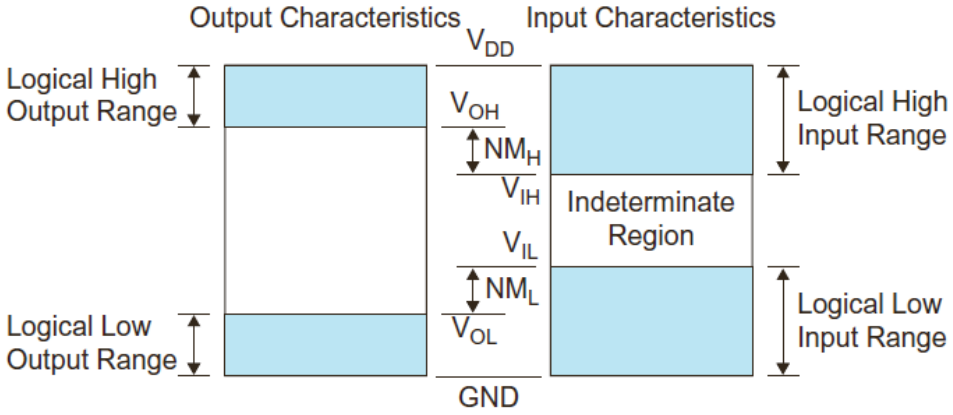
Inverter Noise Margin

$$NM_L = V_{IL} - V_{OL}$$

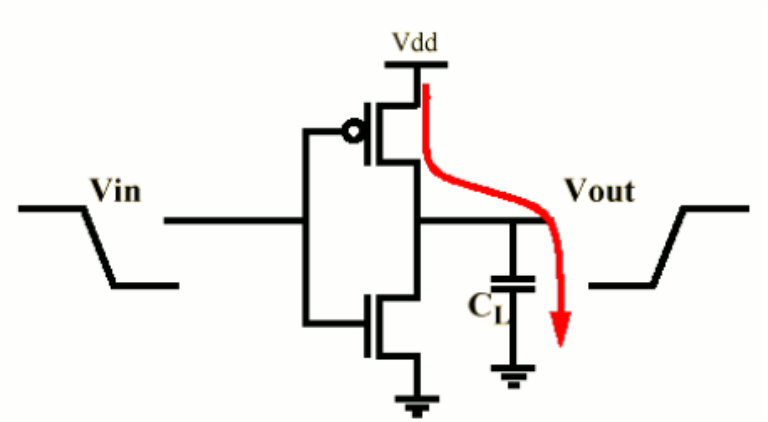
$$NM_H = V_{OH} - V_{IH}$$

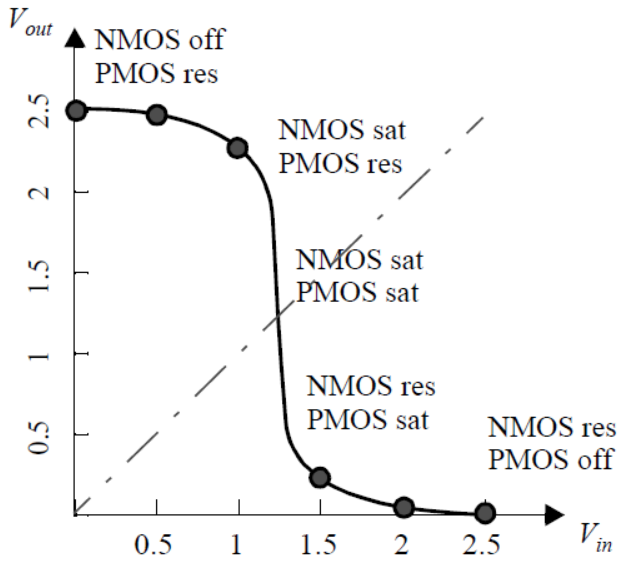






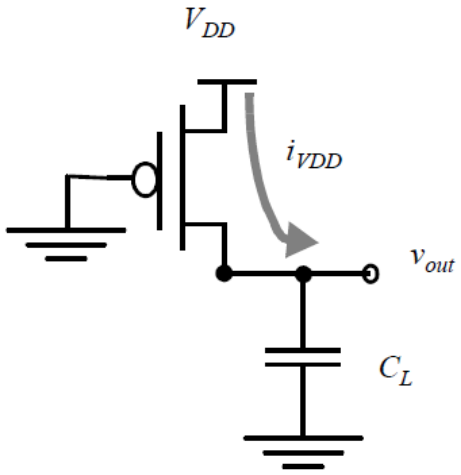
Inverter Power





$$P_{total} = P_{dyn} + P_{stat}$$
$$= P_{tran} + P_{sc} + P_{stat}$$

Inverter Power



$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt$$

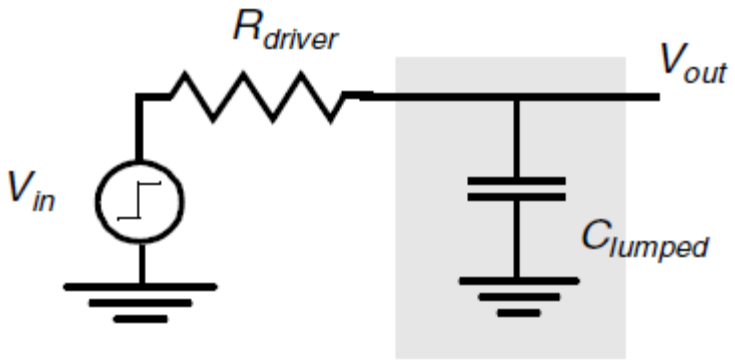
$$= C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

$$P_{dyn} = C_L V_{DD}^2 f_{0 \to 1}$$

Voltage scaling is the most popular

Inverter Delay



$$C_{lumped}\frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_{driver}} = 0$$

$$V_{out}(t) = (1 - e^{-t/\tau})\, V$$

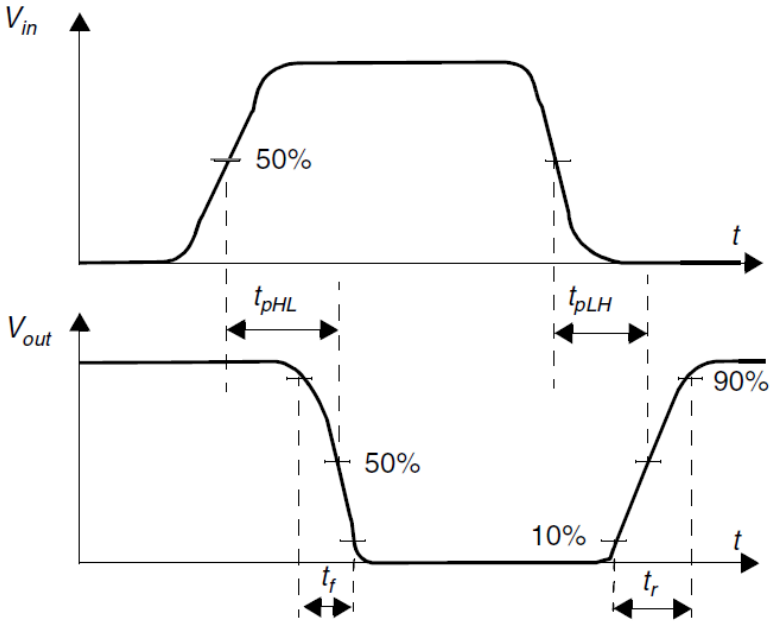
$$t = \ln(2)\tau = 0.69\tau$$

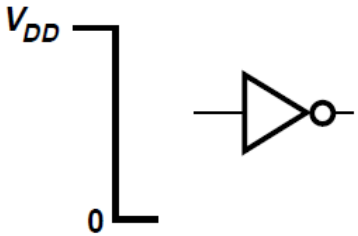
Time needed to rise 50% of final value

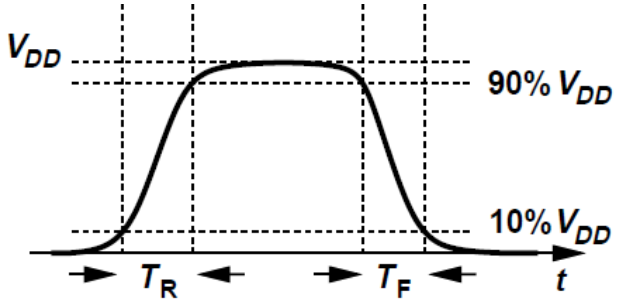
Inverter Delay

$$t_{pHL} = \ln(2) R_{eqn} C_L = 0.69 R_{eqn} C_L$$

$$t_{pLH} = 0.69 R_{eqp} C_L$$



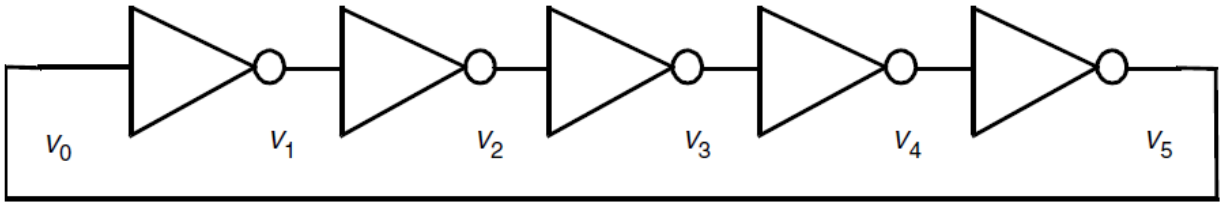


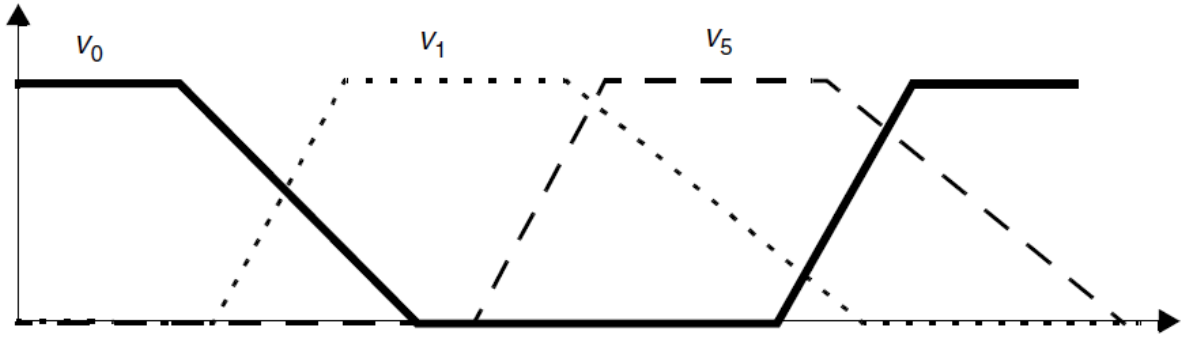


$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Inverter Delay

Ring Oscillator

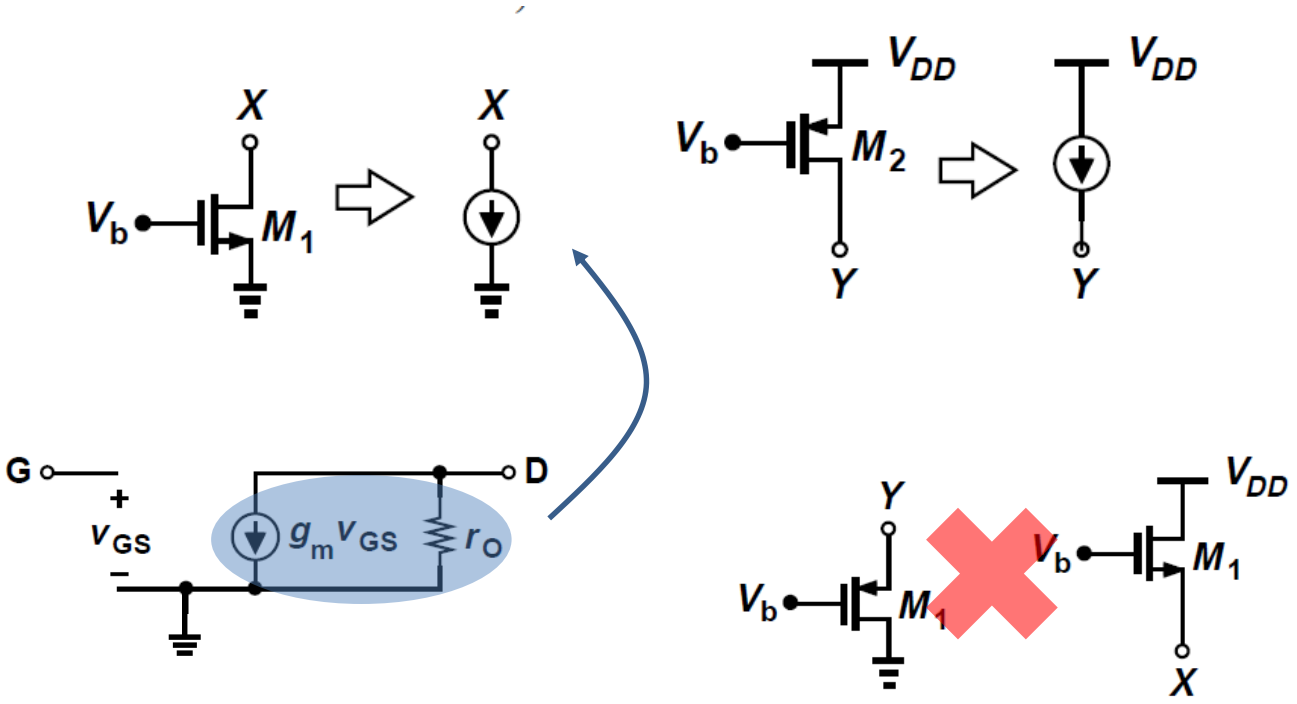




$$T = 2 \times t_p \times N$$

Analog again!

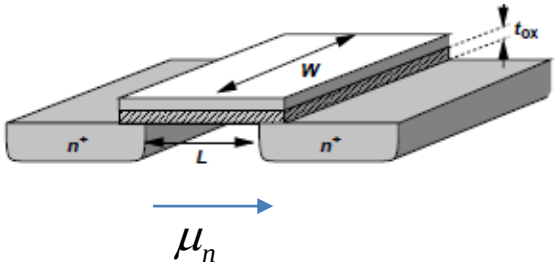
Current Source



- Do not operate as current sources because variation of V_X or V_Y directly changes the gate-source voltage of each transistor, thus changing the drain current considerably

Small signal models

$$g_m = \frac{\partial I_D}{\partial V_{GS}}.$$



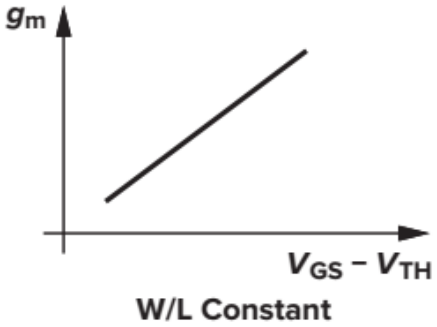
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

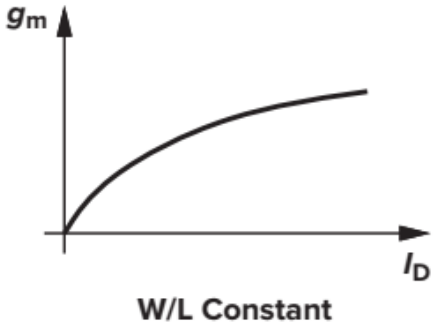
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$ [in saturation]

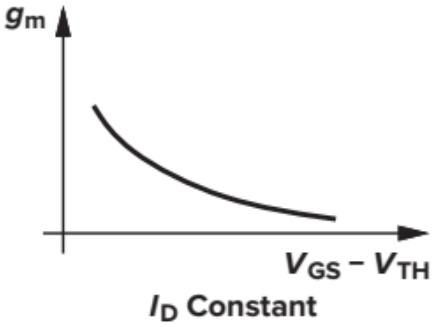
$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}.$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

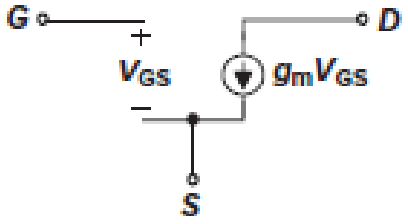




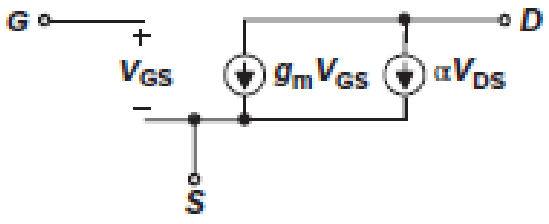


- g_m represents the sensitivity of the device: for a high g_m, a small change in V_{GS} results in a large change in I_D.

Small signal models



(a)



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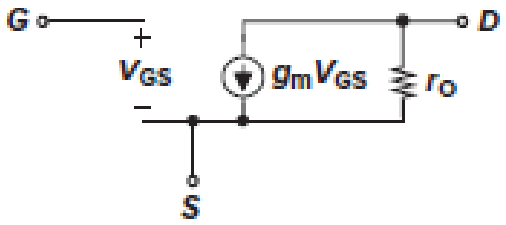

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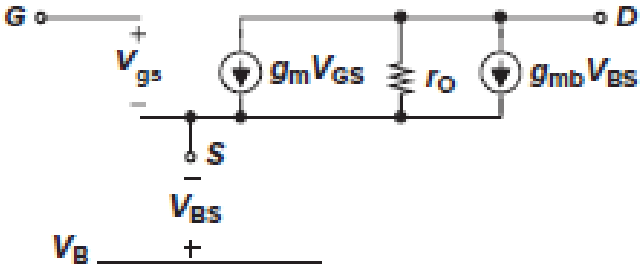
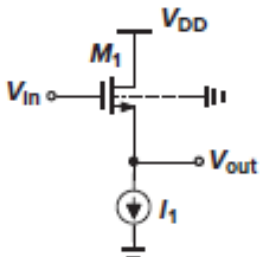


(d)



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\cdot\lambda}$$

$$r_O = \frac{1}{\lambda I_D}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right)$$

$$g_{mb} = g_m\frac{\gamma}{2\sqrt{2\Phi_F+V_{SB}}} = \eta g_m$$

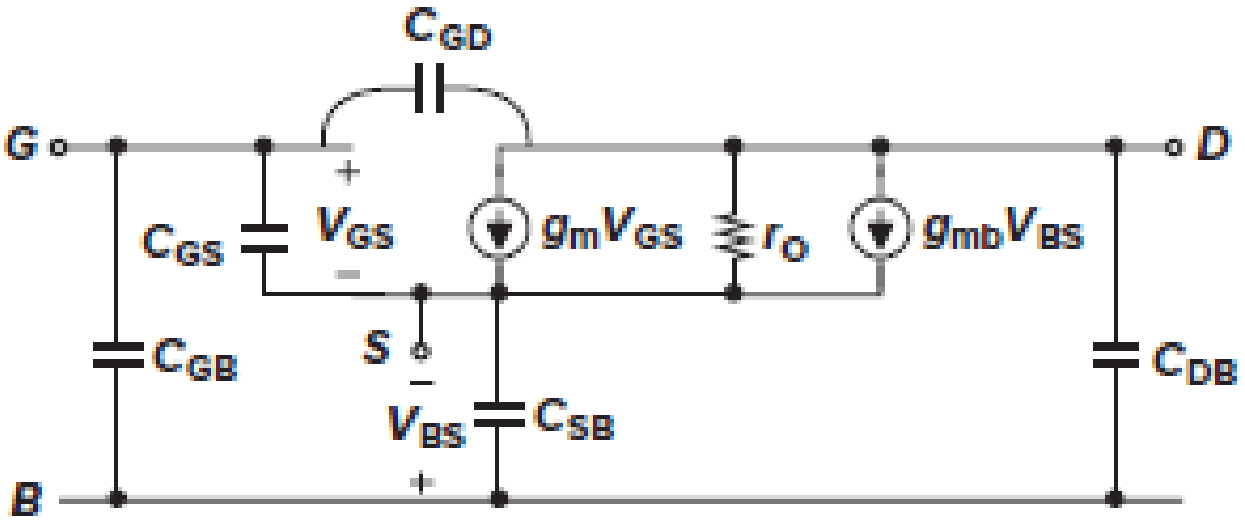
$$V_{TH} = V_{TH0}+\gamma\left(\sqrt{2\Phi_F+V_{SB}}-\sqrt{|2\Phi_F|}\right)$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F+V_{SB})^{-1/2}$$

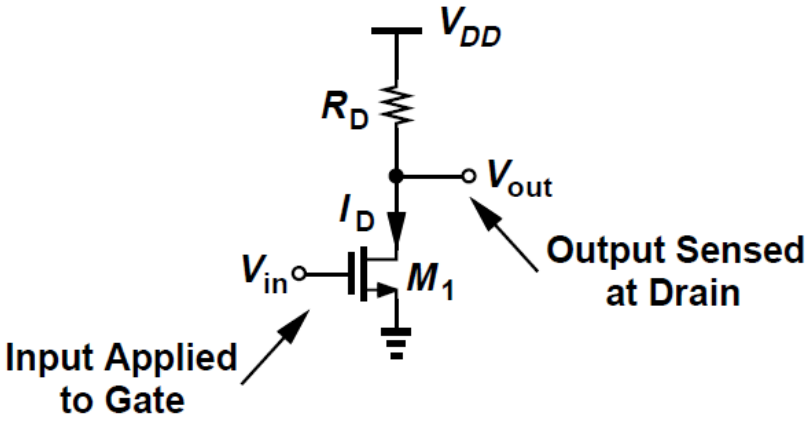
$\eta = g_{mb}/g_m$ and is typically around 0.25.

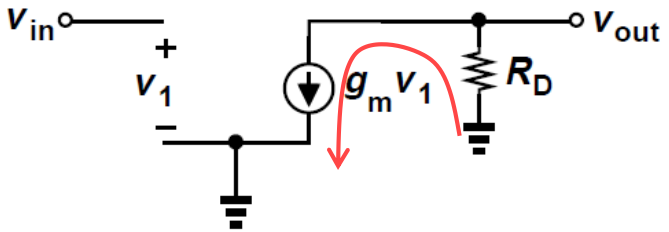
- Owing to channel-length modulation, the drain current also varies with the drain-source voltage
- The bulk potential influences the threshold voltage and hence the gate-source overdrive

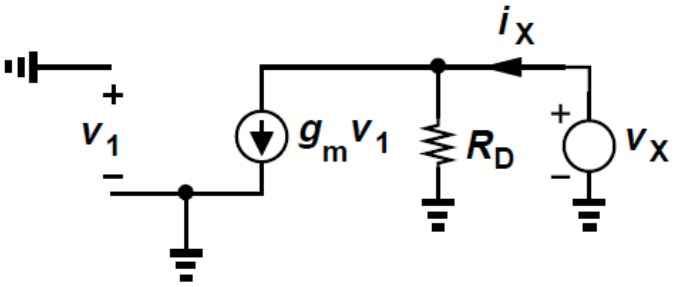
Complete MOS small-signal



Common Source Amplifier



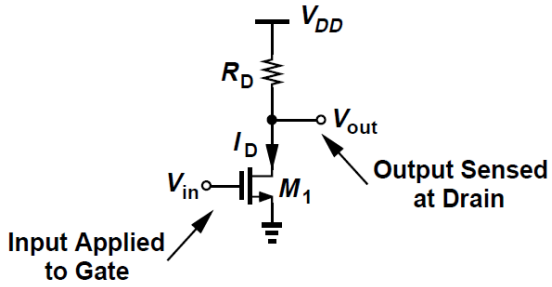




$$v_o = -g_m v_{in} R_D$$

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D \qquad R_{in} = \infty \qquad R_{out} = R_D$$

Common Source Amplifier



$$(1/2)\mu_n C_{ox}(W/L)(V_{in} - V_{TH})^2\lambda = 1/r_O$$

$$A_v = -R_D g_m - \frac{R_D}{r_O}A_v$$

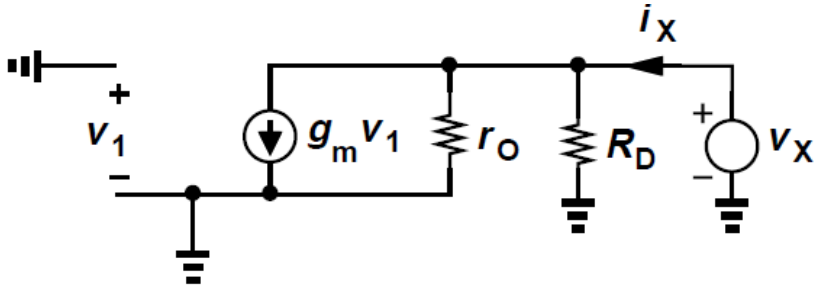
$$A_v = -g_m \frac{r_O R_D}{r_O + R_D}$$

For large values of R_D, the effect of channel-length modulation in M_1 becomes

$$V_{out} = V_{DD} - R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out})$$

$$-R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2\lambda\frac{\partial V_{out}}{\partial V_{in}}$$

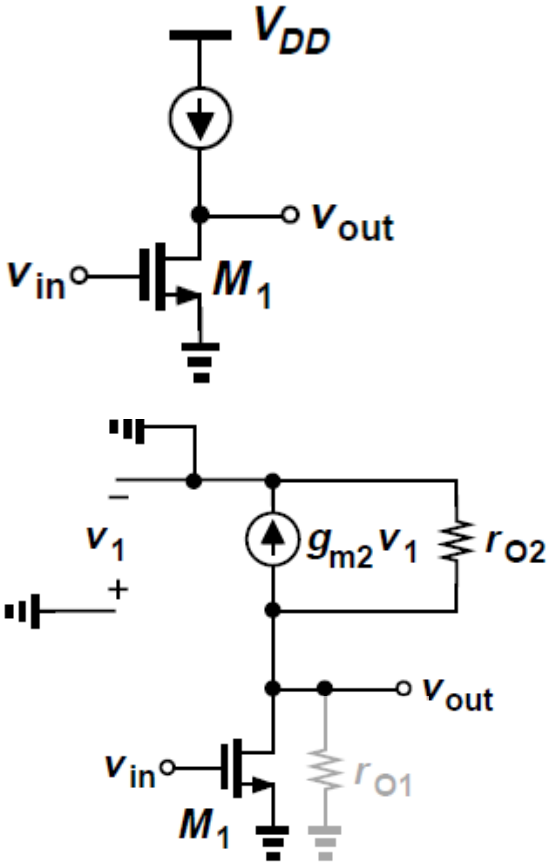


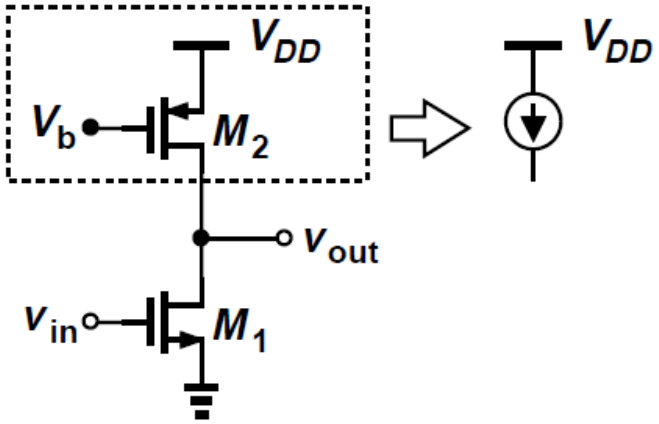
$$A_v = -g_m(R_D||r_O)$$

$$R_{in} = \infty$$

$$R_{out} = R_D||r_O.$$

CS Amplifier: Current-Source Load



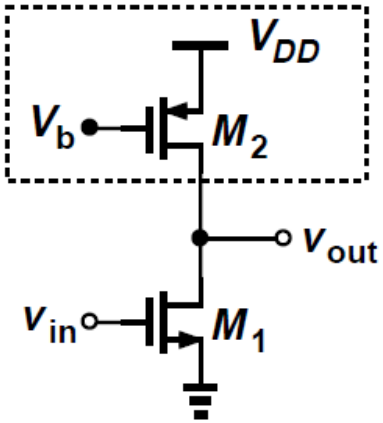


$$A_v = -g_{m1}(r_{O1}||r_{O2})$$

$$R_{out} = r_{O1}||r_{O2}.$$

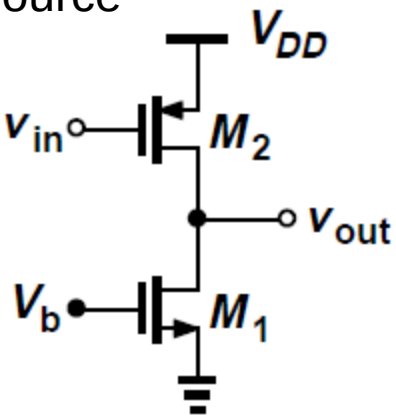
- In applications requiring a large voltage gain in a single stage, the relationship $A_v = -g_m R_D$ suggests that we should increase the load impedance of the CS stage. With a resistor or diode-connected load, however, increasing the load resistance translates to a large dc drop across the load, thereby limiting the output voltage swing.

CS Amplifier: Active Load



$$A_v = -g_{m1}(r_{O1}||r_{O2})$$
$$R_{out} = r_{O1}||r_{O2}.$$

The PMOS device serves as a constant current source

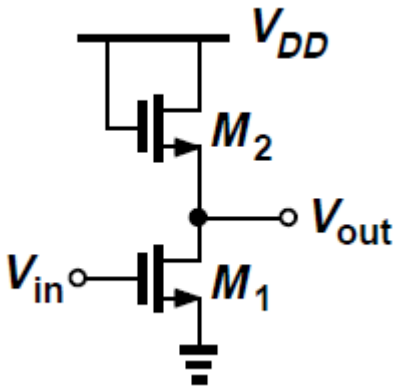


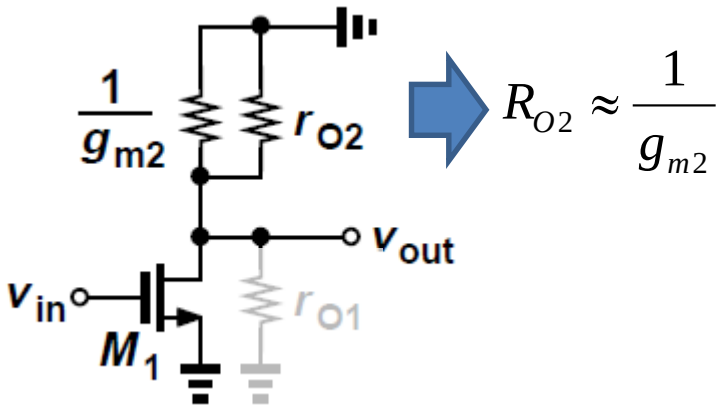
PMOS Amplifier

$$A_v = -g_{m2}(r_{O1}||r_{O2})$$

PMOS M_2 to operate as an *amplifying* device

CS Amplifier: Diode Load



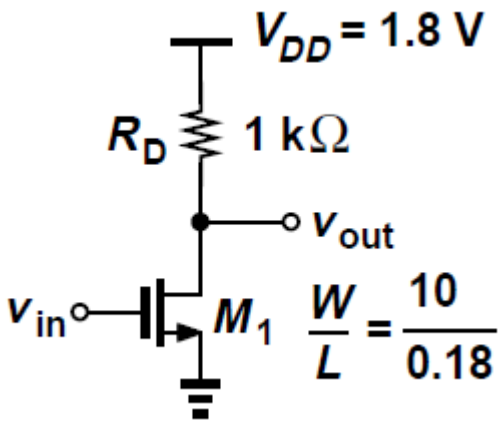


$$A_v = -g_{m1}(r_{o1} \| R_{O2})$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} || r_{O2} || r_{O1}\right) \qquad R_{out} = \frac{1}{g_{m2}} || r_{O2} || r_{O1}$$

- In some CMOS technologies, it is difficult to fabricate resistors with tightly controlled values or a reasonable physical size. Consequently, it is desirable to replace R_D with a MOS transistor

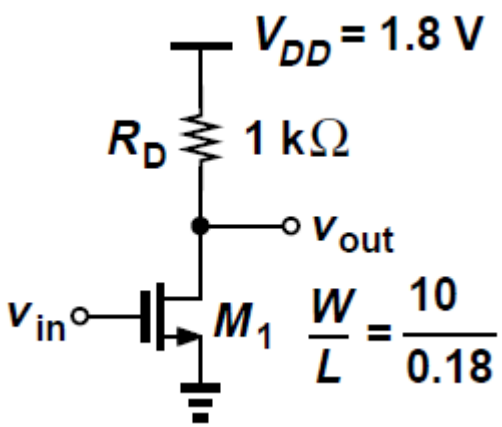
CS Amplifier: Example



I_D = 1mA, μC_{ox} = 100 µA/V^2 , V_{TH} = 0.5V

Find the gain and operating region of M_1

CS Amplifier: Example



How?

I_D = 1mA, μC_{ox} = 100 µA/V^2 , V_{TH} = 0.5V

Find the gain and operating region of M_1

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$
$$= \frac{1}{300\ \Omega}.$$

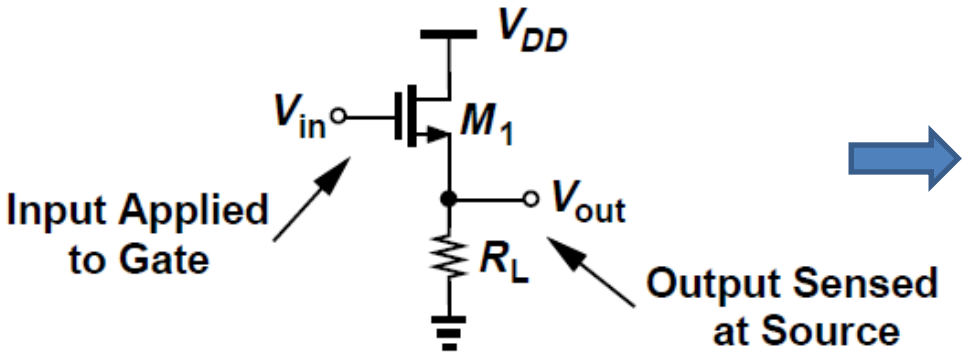
$$A_v = -g_m R_D$$
$$= 3.33.$$

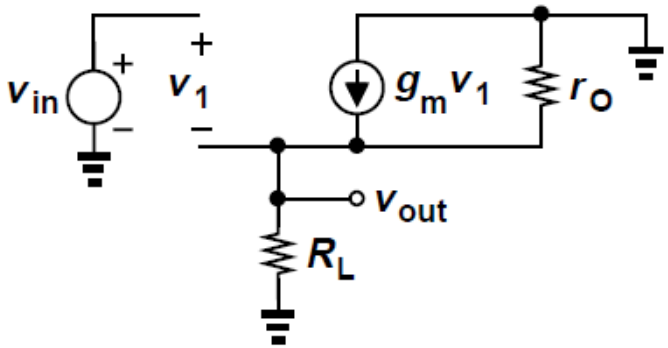
$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}$$
$$= 1.1\ \text{V}.$$

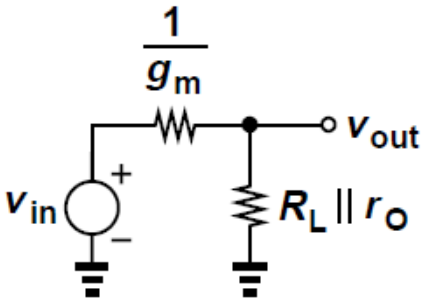
$V_{DS} = V_{DD} - I_D R_D = 0.8V$
$V_{GS} - V_{TH} = 0.6$

$V_{DS} > V_{GS} - V_{TH}$ In saturation!

Source Follower



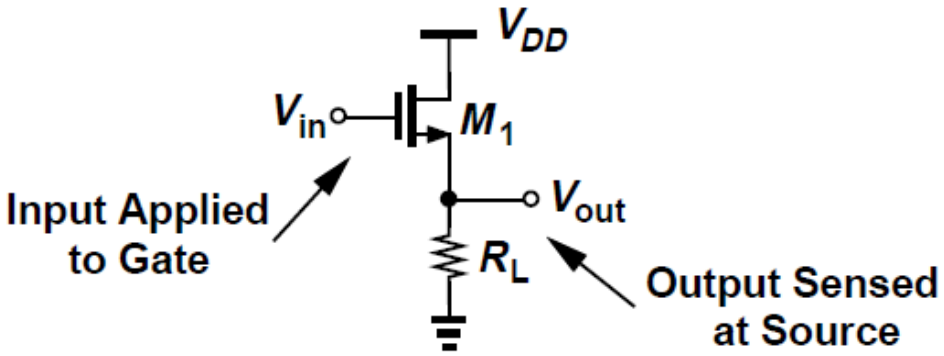


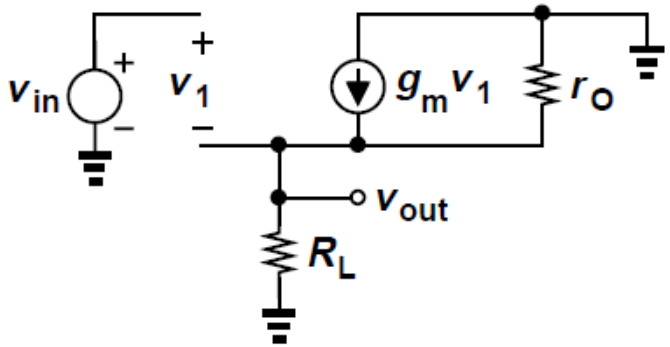


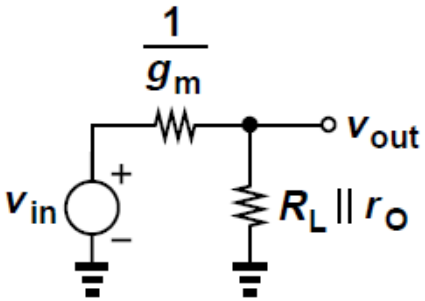
$$g_m v_1 (r_O || R_L) = v_{out}.$$

$$v_{in} = v_1 + v_{out}$$

Source Follower





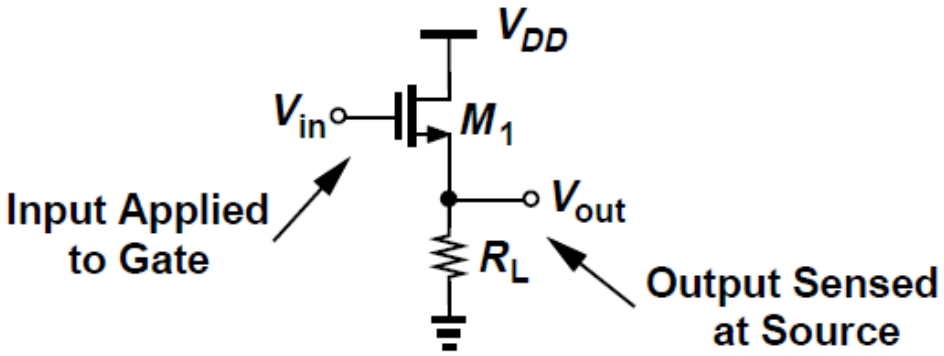


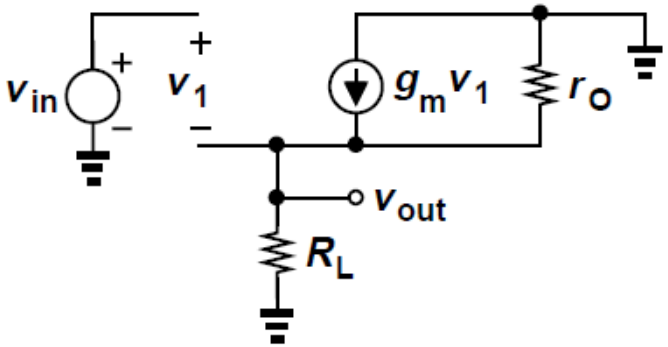
$$\frac{v_{out}}{v_{in}} = \frac{g_m(r_O||R_L)}{1+g_m(r_O||R_L)}$$

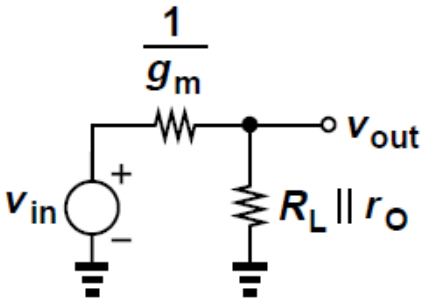
$$= \frac{r_O||R_L}{\frac{1}{g_m}+r_O||R_L}. \quad \approx 1$$

Increase R_L (and r_o)

Source Follower





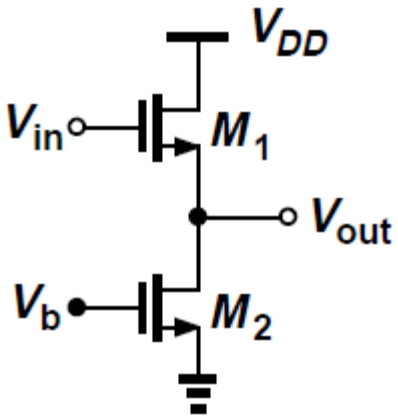


$$\frac{v_{out}}{v_{in}} = \frac{g_m(r_O||R_L)}{1+g_m(r_O||R_L)}$$

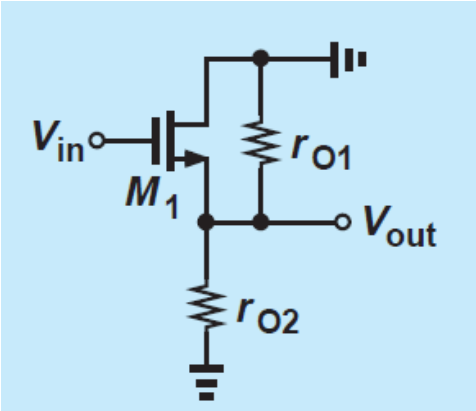
$$= \frac{r_O||R_L}{\frac{1}{g_m}+r_O||R_L}.$$

$$\approx 1$$

Source Follower: Active Load



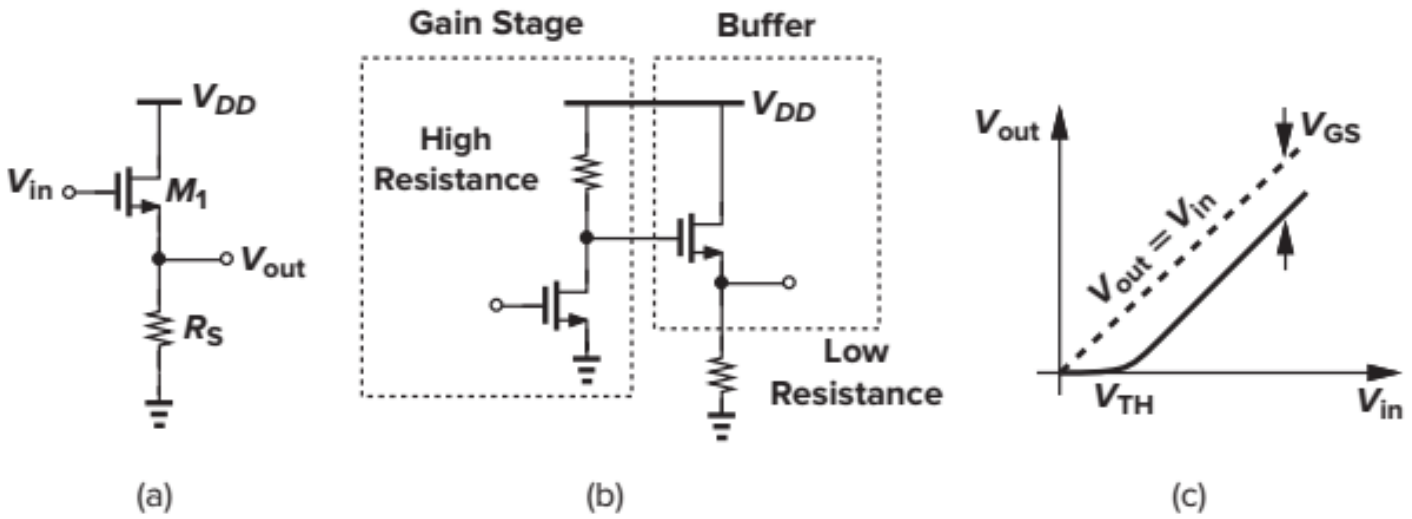
Find the gain and output impedance using small signal analysis



$$A_v = \frac{r_{O1}||r_{O2}}{\frac{1}{g_{m1}} + r_{O1}||r_{O2}}$$

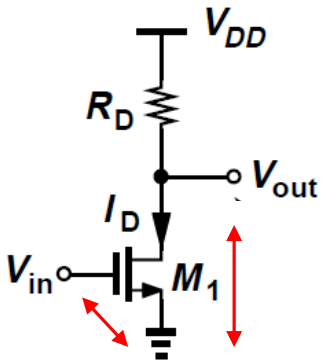
If $r_{O1}||r_{O2} \gg 1/g_{m1}$, then $A_v \approx 1$

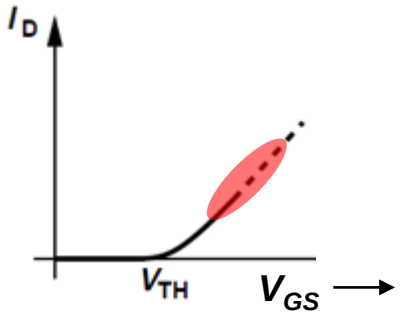
Source Follower: Application

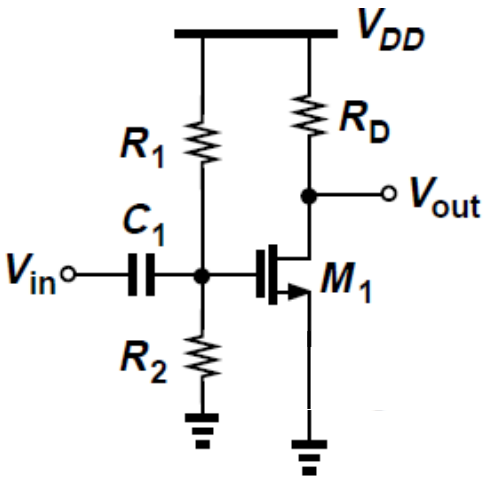


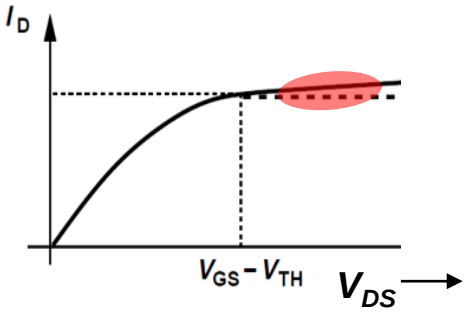
- Our analysis of the common-source stage indicates that, to achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible. If such a stage is to drive a low-impedance load, then a “buffer” must be placed after the amplifier so as to drive the load with negligible reduction in gain. The source follower (also called the “common-drain” stage) can operate as a voltage buffer.

Amplifier Biasing: CS



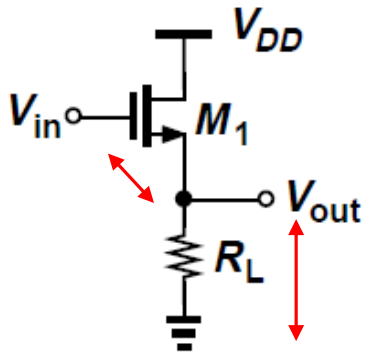


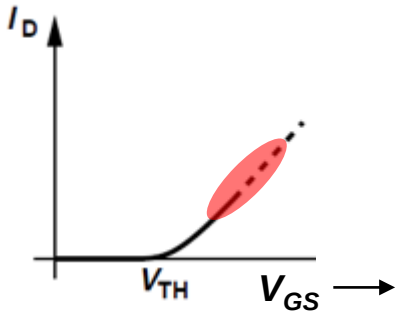


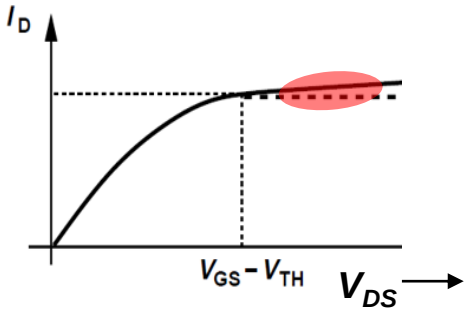


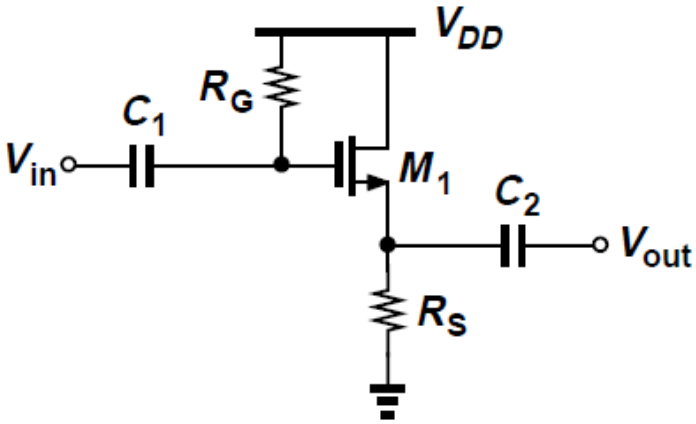
When V_{in}=0, V_{GS}=?, V_{DS}=?

Amplifier Biasing: SF



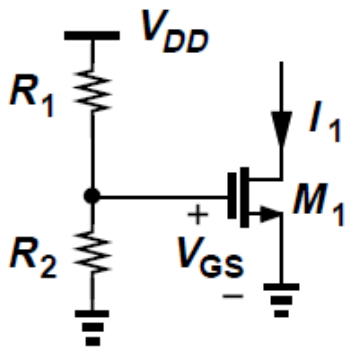






When V_{in}=0, V_{GS}=?, V_{DS}=?

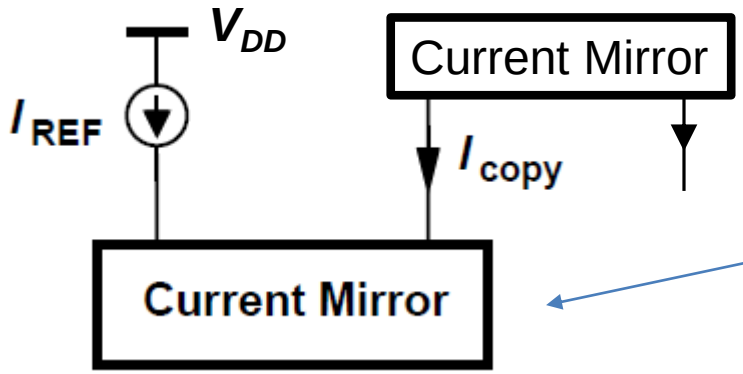
Current Mirror biasing



$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

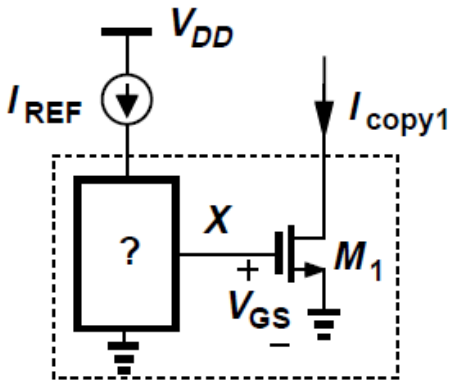
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH}\right)^2$$

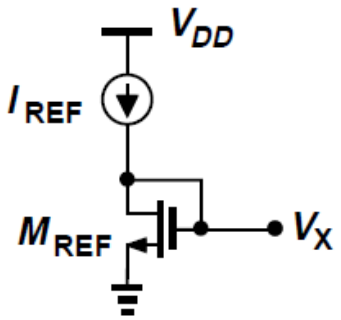
Not a constant biasing! I_1 depends on temperature and supply variation



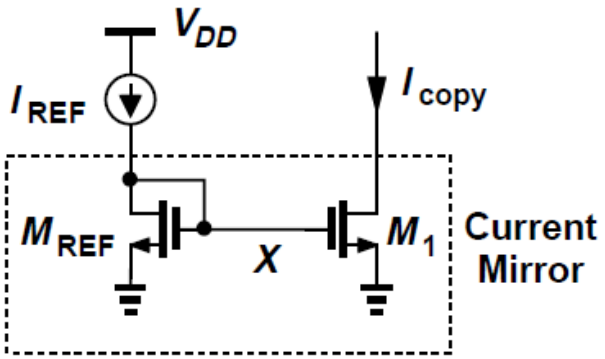
Copies or multiplies current

Current Mirror





$$V_{GS} = V_{DS} = V_X$$



M_{REF} is always in saturation

$$I_{D,REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}(V_X - V_{TH})^2$$

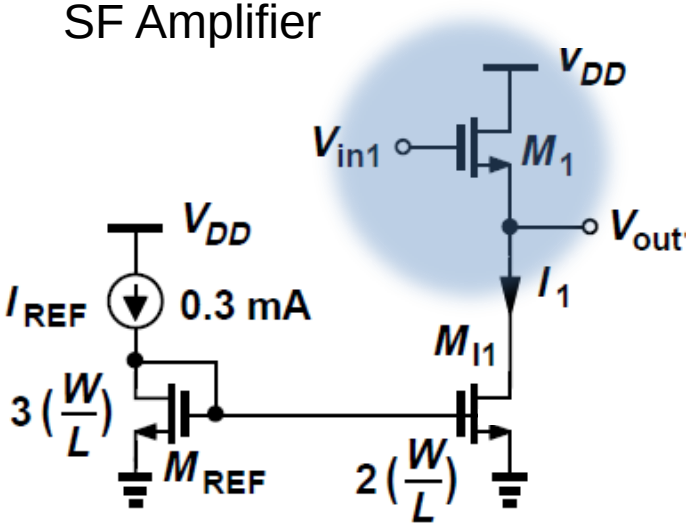
$$I_{copy} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1}(V_X - V_{TH})^2$$

$$V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{TH1}$$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}$$

Current Mirror biasing

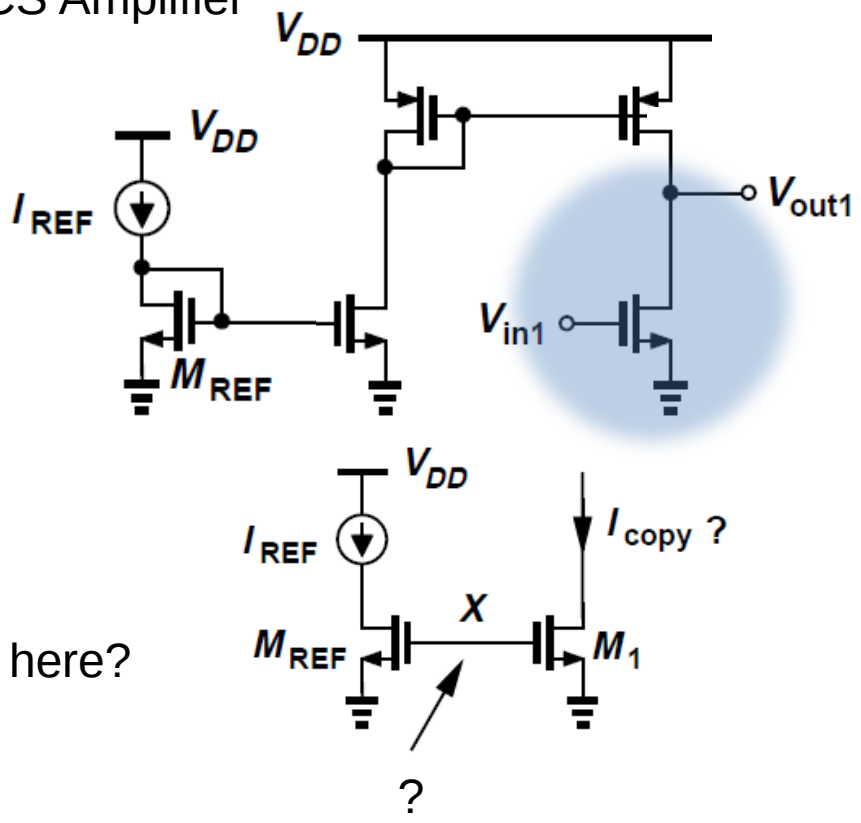
SF Amplifier



$$I_1 = I_{REF}\frac{2}{3} = 0.2mA$$

What happens here?

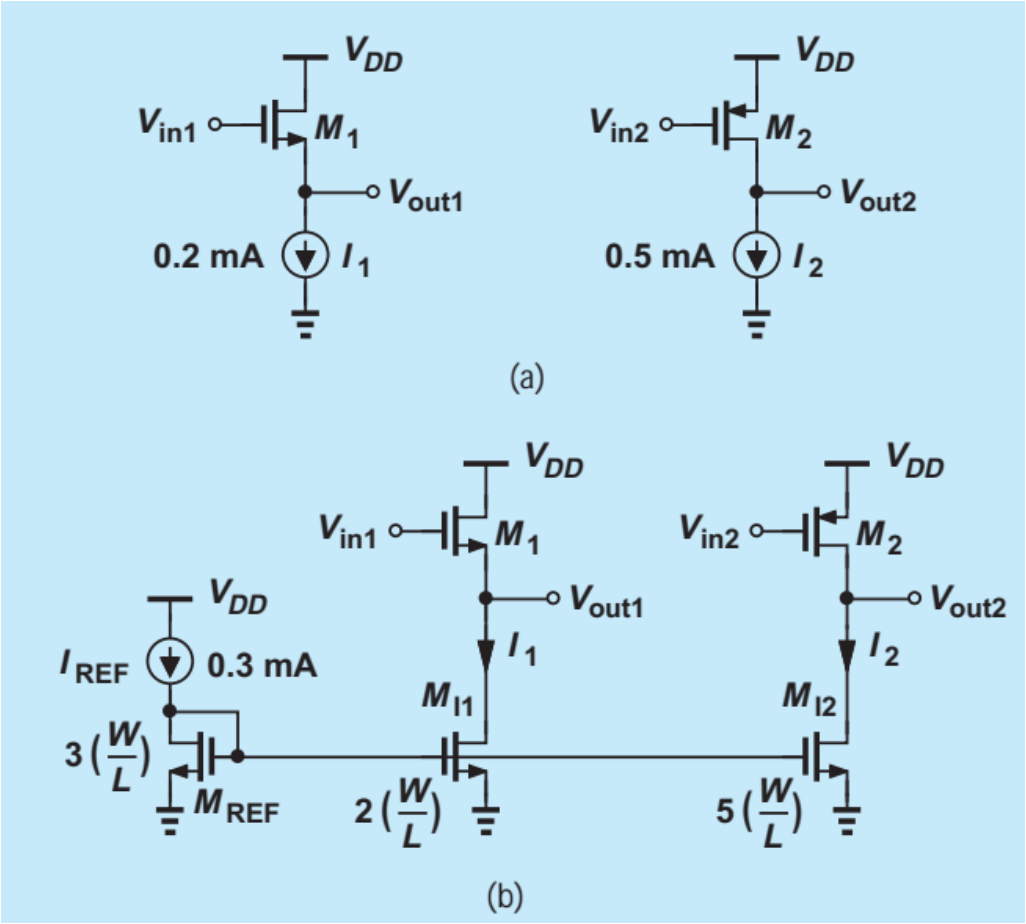
CS Amplifier



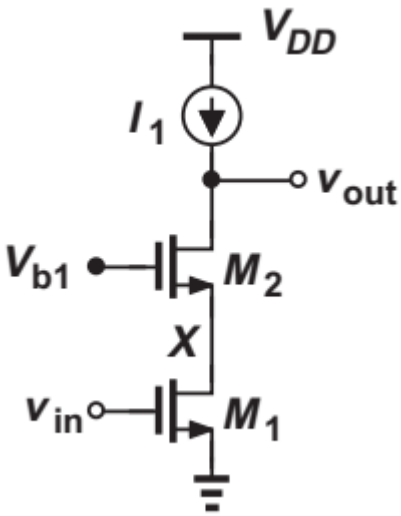
- This circuit is not a current mirror because only a diode-connected device can establish and hence a copy current independent of device parameters and temperature. Since the gates of M_{REF} and M_1 are floating, they can assume any voltage, e.g., an initial condition created at node X when the power supply is turned on. In other words, I_{copy} is very poorly defined.

Current Mirror biasing

- An integrated circuit employs the source follower and the common-source stage shown below. Design a current mirror that produces I_1 and I_2 from a 0.3-mA reference



Cascode Gain Stage

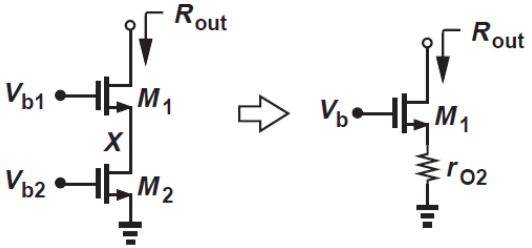


$$A_v = -G_m R_{out}$$
$$\approx -g_{m1}[(1 + g_{m2}r_{O2})r_{O1} + r_{O2}]$$
$$\approx -g_{m1}r_{O1}g_{m2}r_{O2}.$$

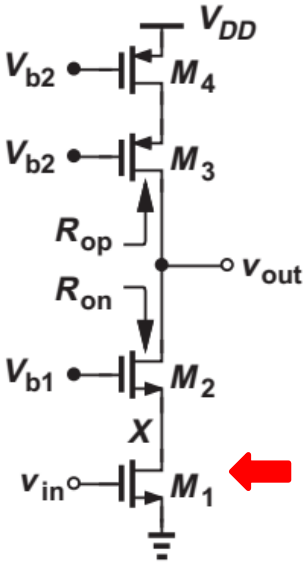
$$R_{on} \approx g_{m2}r_{O2}r_{O1}$$

$$R_{op} \approx g_{m3}r_{O3}r_{O4}$$

$$A_v \approx -g_{m1}[(g_{m2}r_{O2}r_{O1})||(g_{m3}r_{O3}r_{O4})]$$



$$R_{out} = (1 + g_{m1}r_{O2})r_{O1} + r_{O2}$$
$$\approx g_{m1}r_{O1}r_{O2},$$



- Cascode stages can have quite large gain for a single stage due to the large impedances at the output. To enable this high gain, the current sources connected to the output nodes are realised using high-quality cascode current mirrors. Normally this high gain is obtained without any degradation in speed.

Cascode Gain Stage: Example

- The cascode amplifier incorporates the following device parameters: $(W/L)_{1,2} = 30$, $(W/L)_{3,4} = 40$, $I_{D1} = \cdots = I_{D4} = 0.5$ mA. If $\mu_n C_{ox} = 100\ \mu A/V^2$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $\lambda_n = 0.1\ V^{-1}$ and $\lambda_p = 0.15\ V^{-1}$, determine the voltage gain.

Solution With the particular choice of device parameters here, $g_{m1} = g_{m2}$, $r_{O1} = r_{O2}$, $g_{m3} = g_{m4}$, and $r_{O3} = r_{O4}$. We have

$$g_{m1,2} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} I_{D1,2}}$$
$$= (577\ \Omega)^{-1}$$

and

$$g_{m3,4} = (707\ \Omega)^{-1}.$$

Also,

$$r_{O1,2} = \frac{1}{\lambda_n I_{D1,2}}$$
$$= 20\ \text{k}\Omega$$

and

$$r_{O3,4} = 13.3\ \text{k}\Omega.$$

$$R_{on} \approx 693\ \text{k}\Omega$$
$$R_{op} \approx 250\ \text{k}\Omega$$

and

$$A_v = -g_{m1}(R_{on} || R_{op})$$
$$\approx -318.$$