CMOS VLSI Design

## Lab 2: Full Adder Design

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1. **Please indicate how many hours you spent on this lab. This will not affect your grade but will be helpful for calibrating the workload for the future.**

Frankly speaking, I cannot figure it out. The direct lab hour number is about 3-4. However, the time spent on previewing and lecture slides reviewing is not clear.

2. **A printout of your fulladder schematic (and any subcells, if applicable) .**
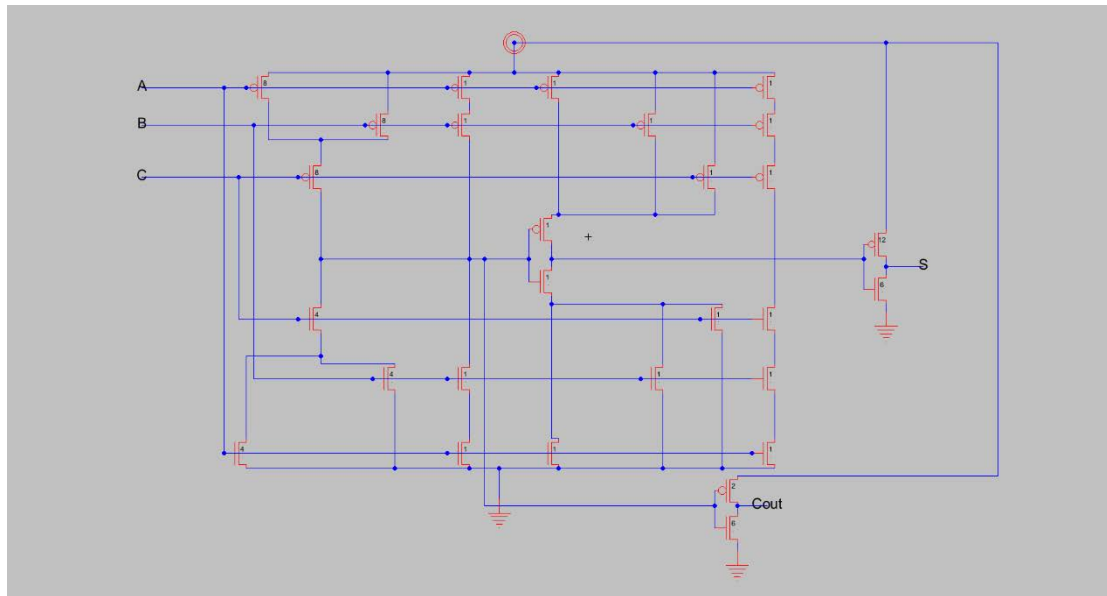
3. **A printout of your fulladder layout.**
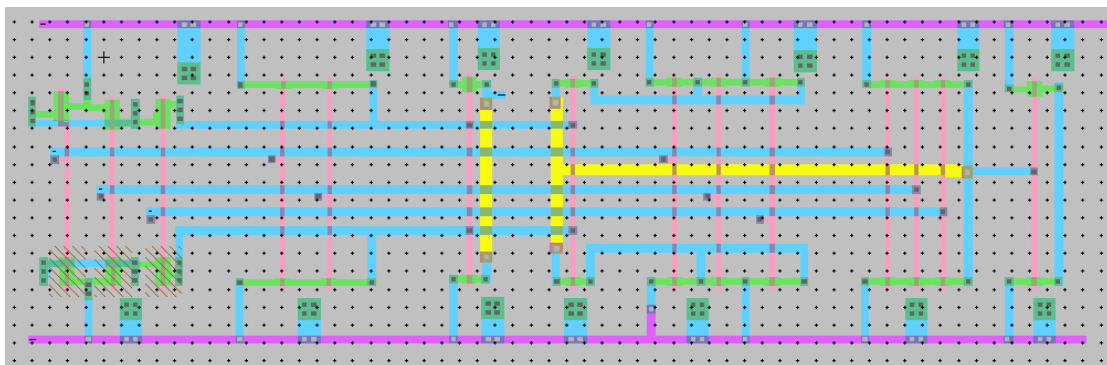
4. **A single page of simulation waveforms demonstrating correct operation of the fulladder layout.**

5. What is the verification status of your layout? Does it pass DRC? ERC? NCC?

Not bad. Yes, it passes.

6. Feedback:

The wrong graph in simulation process will always mislead me: does this mean my layout is wrong again or not? Not to mention the difficult lab. So I have to spend lots of time to verify the simulation and layout to ensure I am right. It seems the delay of the software is unstable, and I don't know if my wrong instruction leads to that.