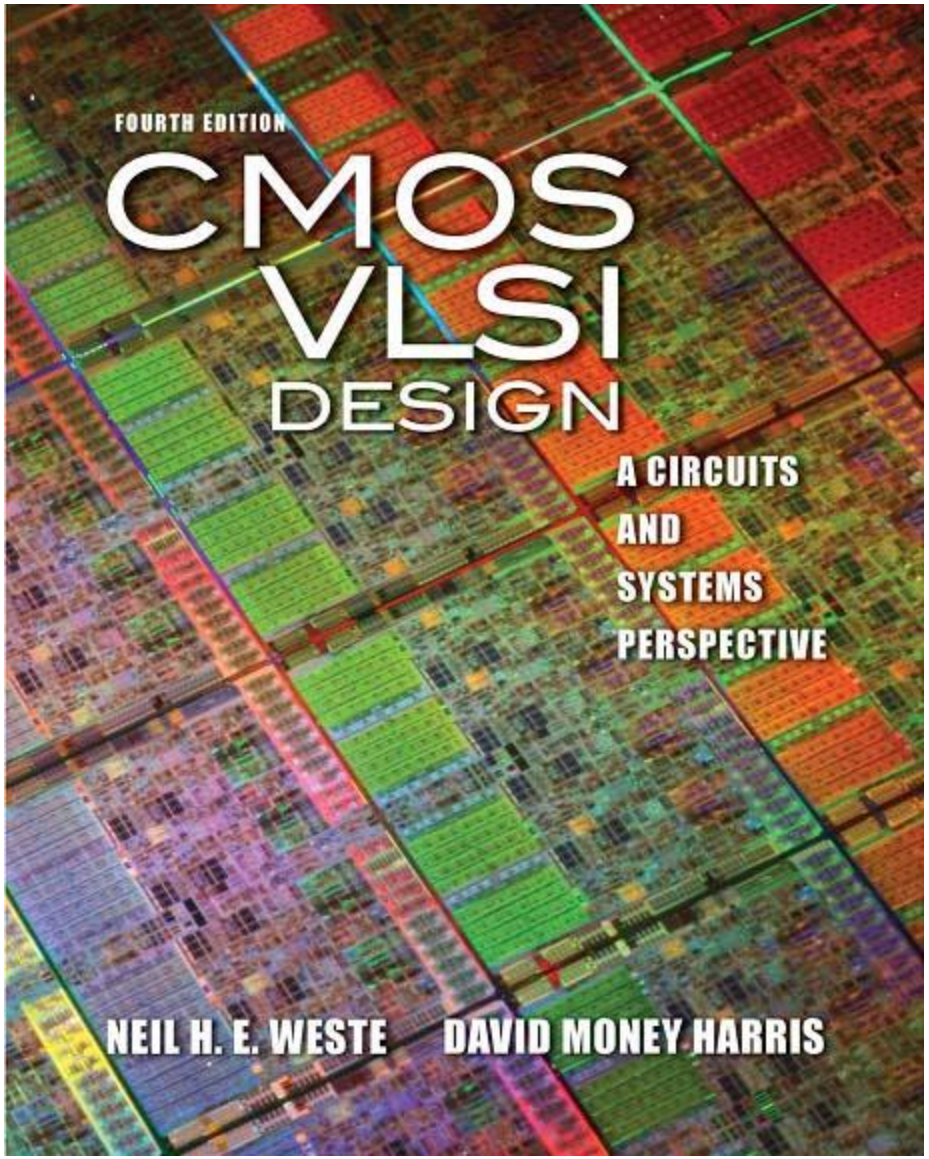


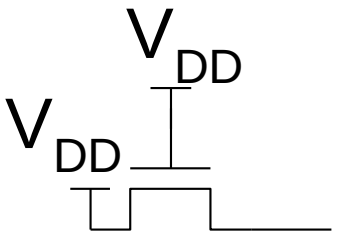
Lecture 5: DC & Transient Response

Outline

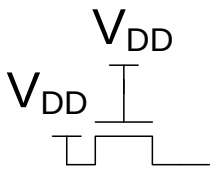
- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation

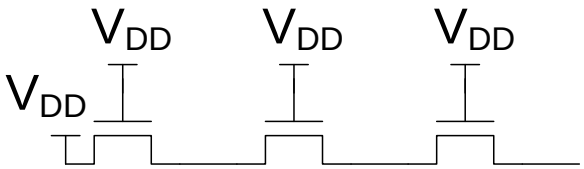
Pass Transistors

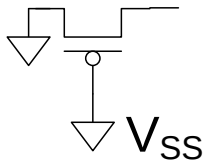
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than V_{tp}
- Transmission gates are needed to pass both 0 and 1

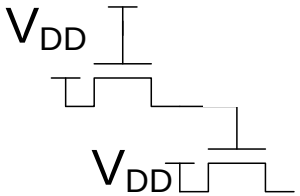


Pass Transistor Ckts





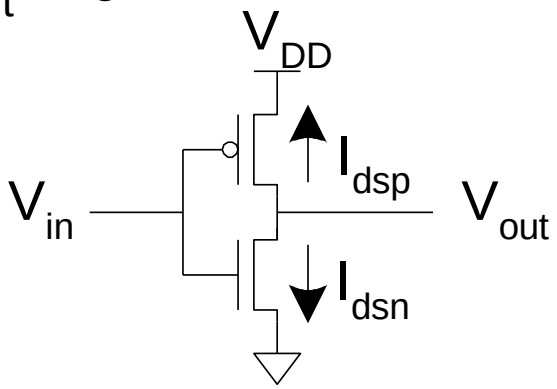




- As the source can rise to within a threshold voltage of the gate, the output of several transistors in series is no more degraded than that of a single transistor

DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight



Transistor Operation

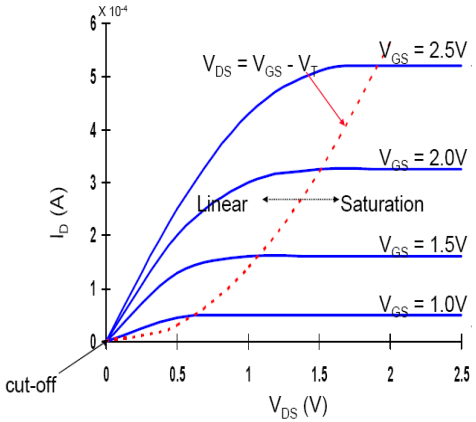
- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

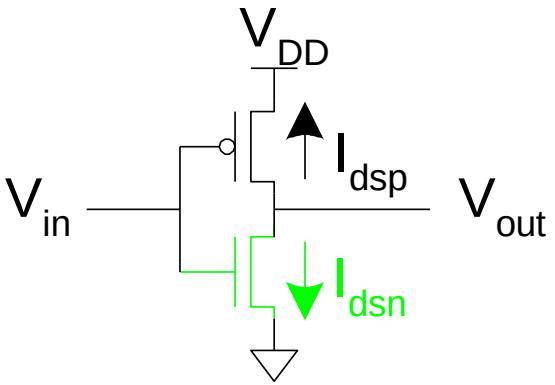
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

nMOS Operation

Cutoff	Linear	Saturated
V_{gsn} <	V_{gsn} >	V_{gsn} >
	V_{dsn} <	V_{dsn} >





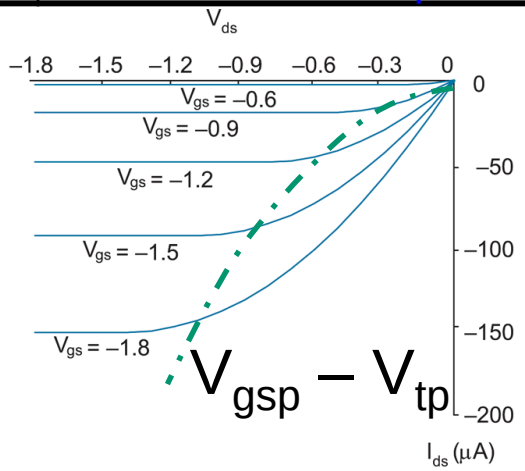
pMOS Operation

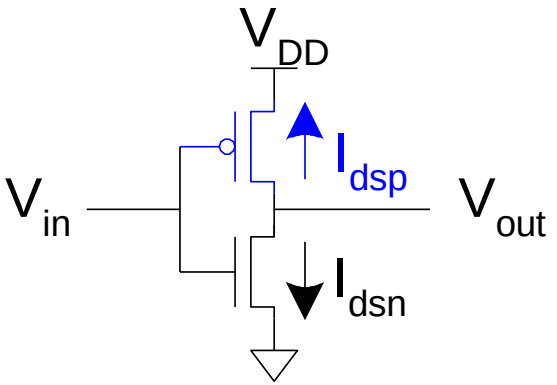
Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$V_{tp} < 0$

$V_{gsp} = V_{in} - V_{DD}$

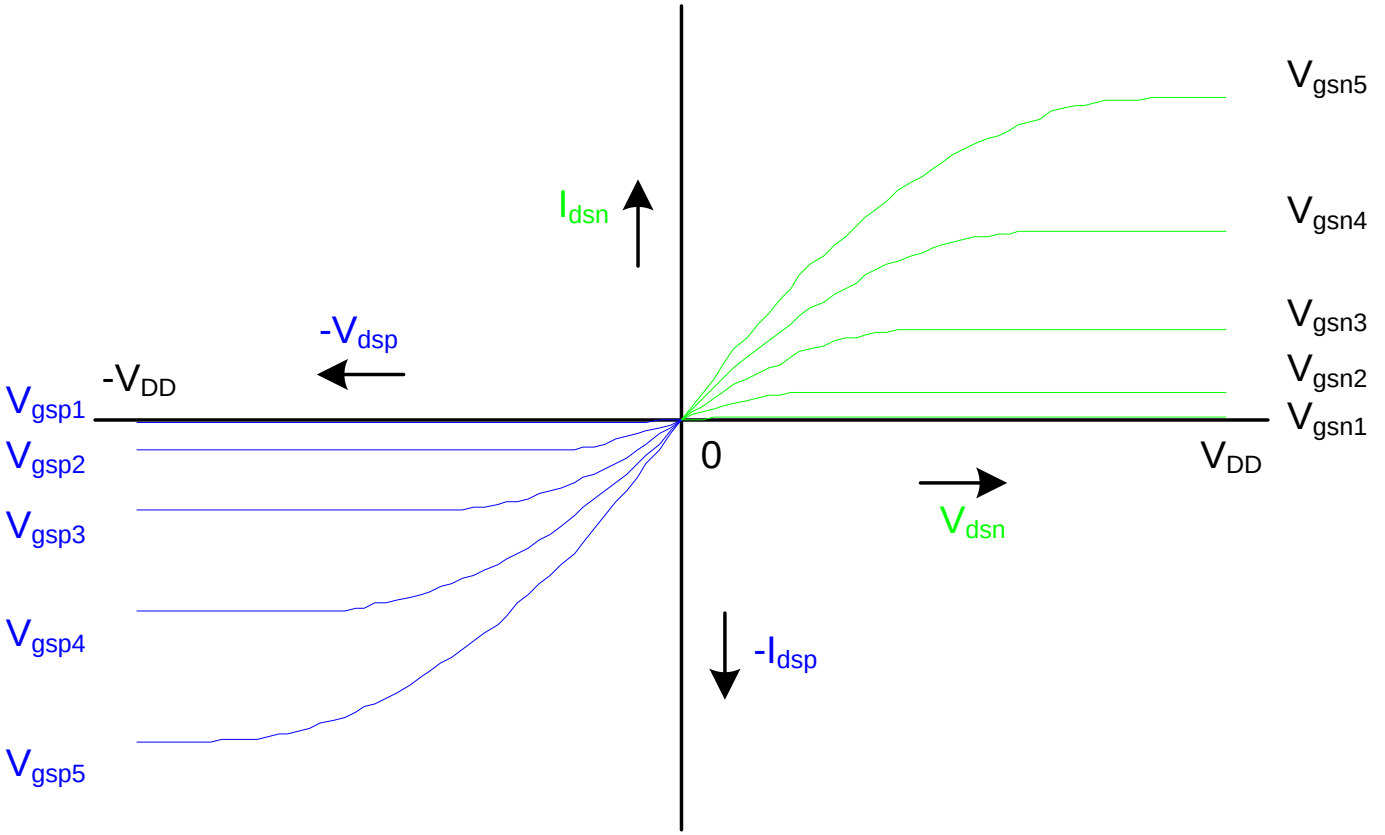
$V_{dsp} = V_{out} - V_{DD}$





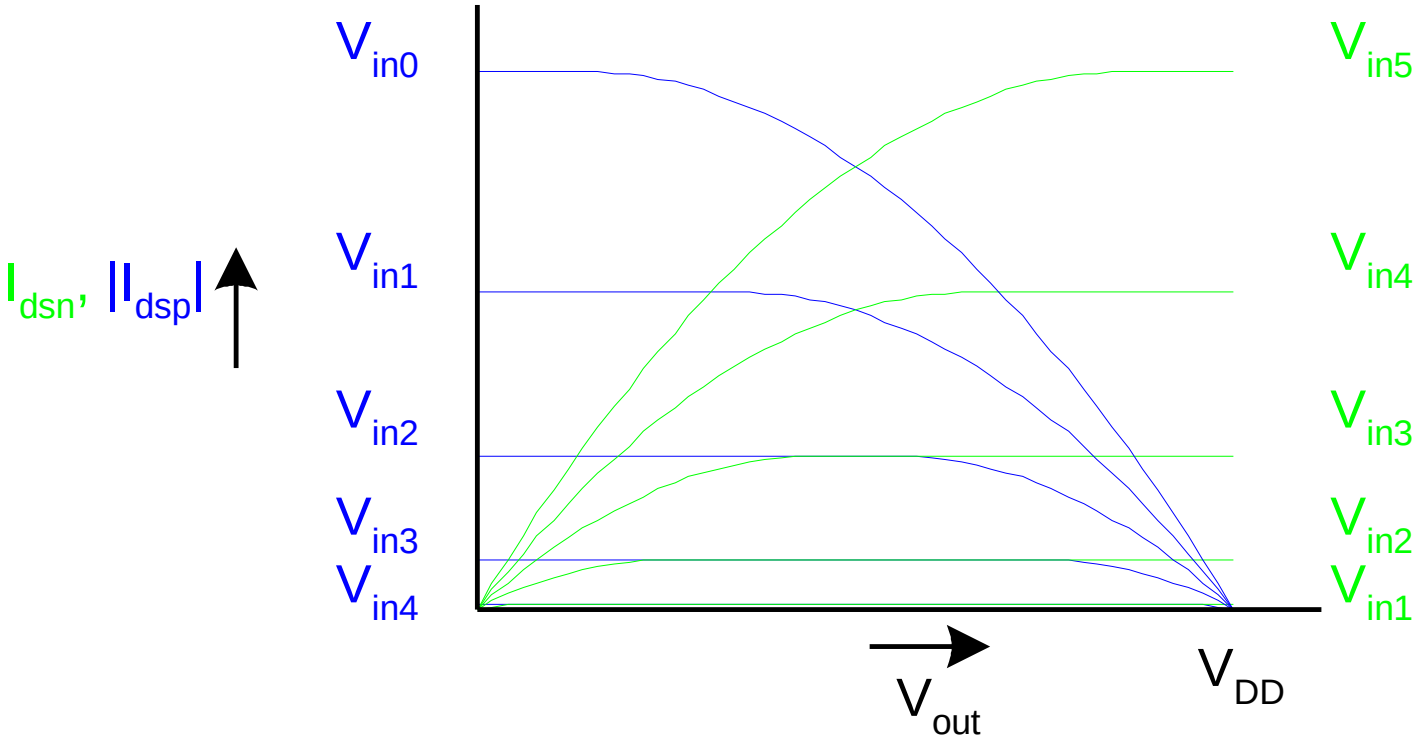
I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$



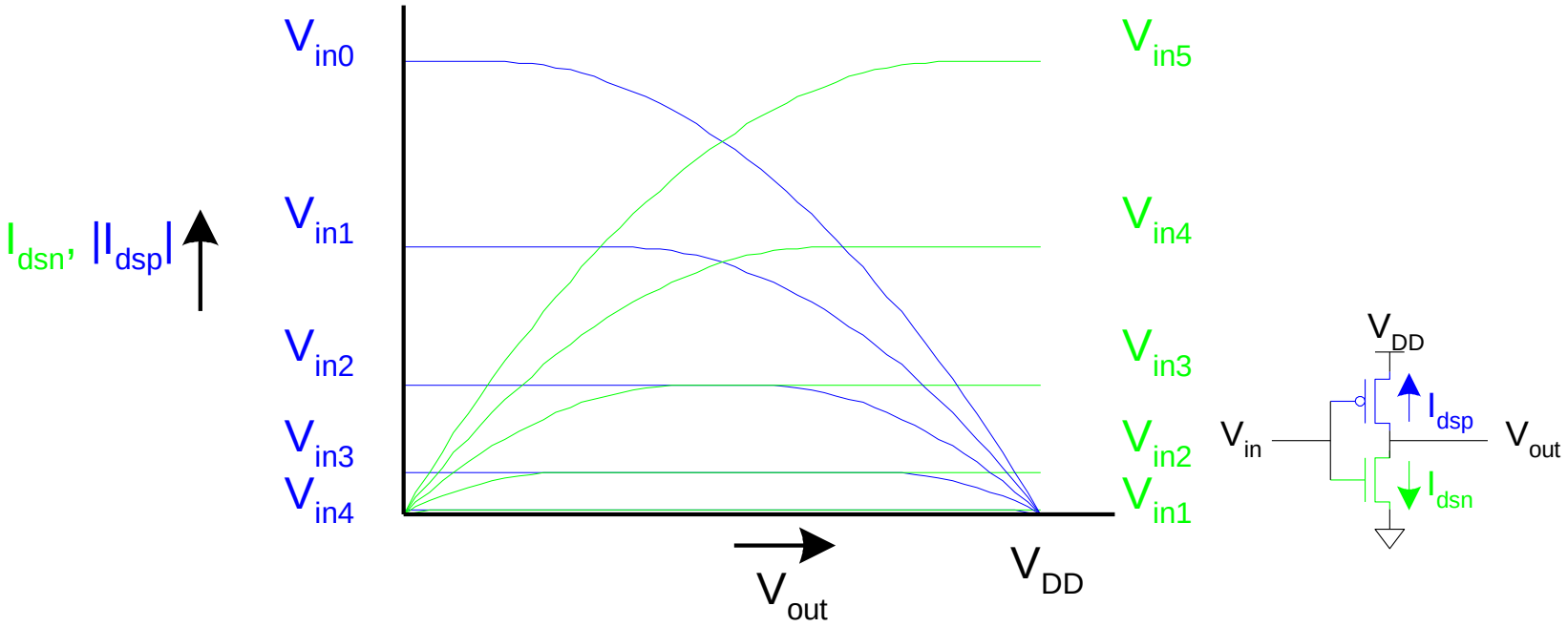
Current vs. V_{out}, V_{in}

$$V_{gsp} = V_{in} - V_{DD}$$

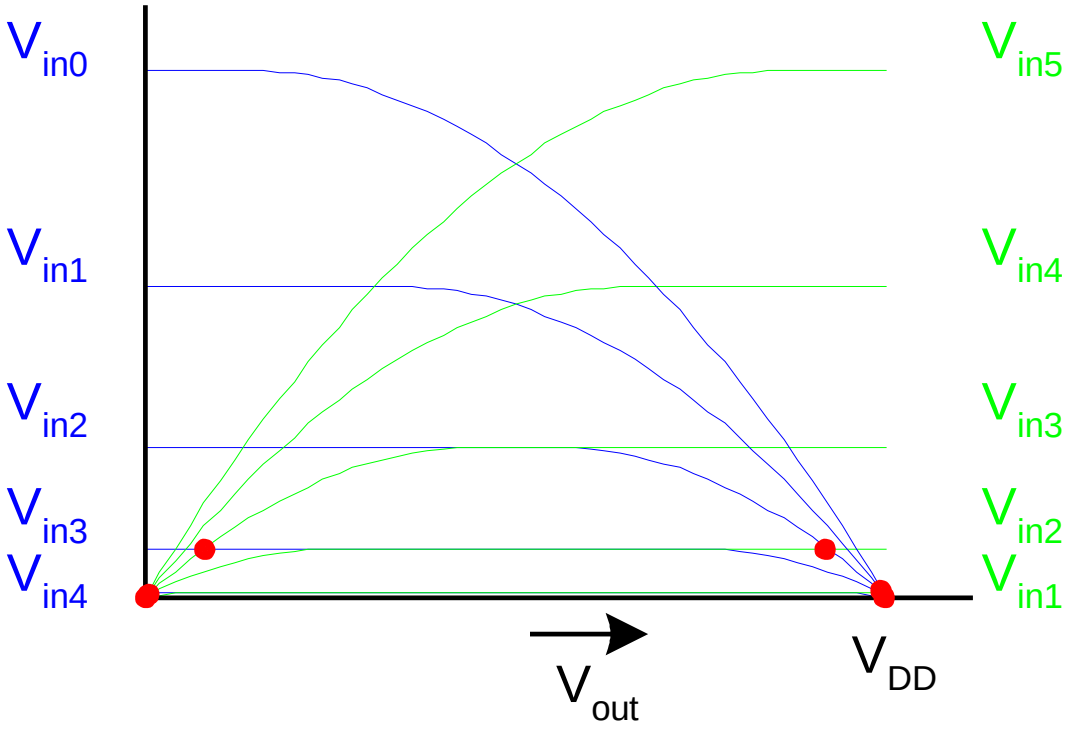


Load Line Analysis

- For a given V_{in}:
  - Plot I_{dsn}, I_{dsp} vs. V_{out}
  - V_{out} must be where |currents| are equal in

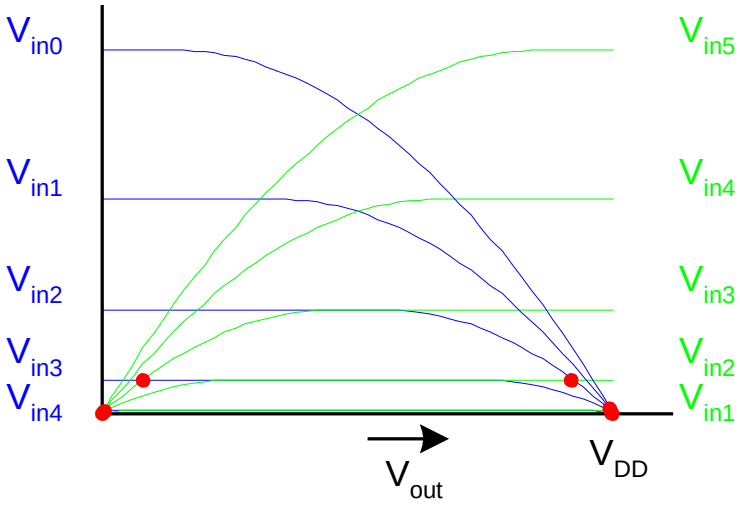


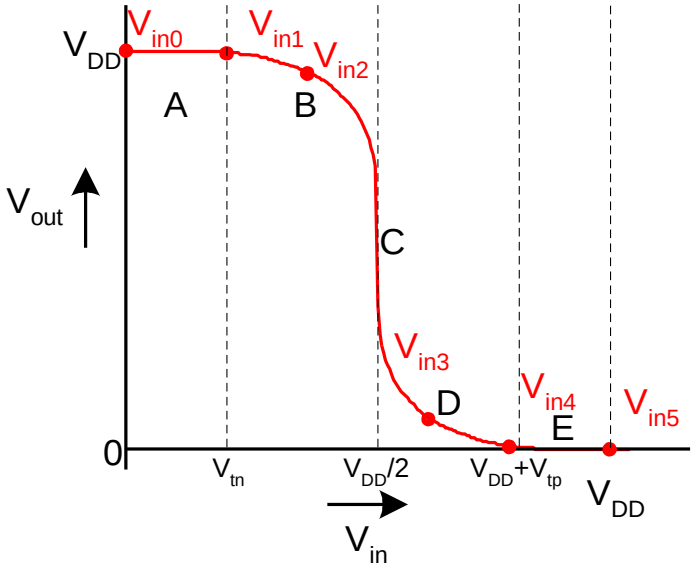
Load Line Analysis



DC Transfer Curve

- Transcribe points onto V_{in} vs. V_{out} plot

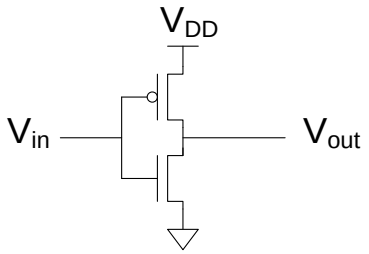


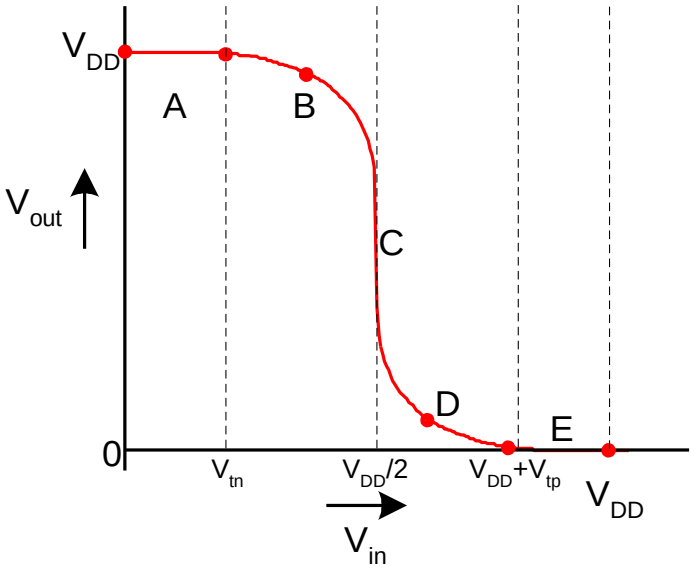


Operating Regions

- Revisit transistor operating regions

Region	nMOS	pMOS
A		
B		
C		
D		
E		



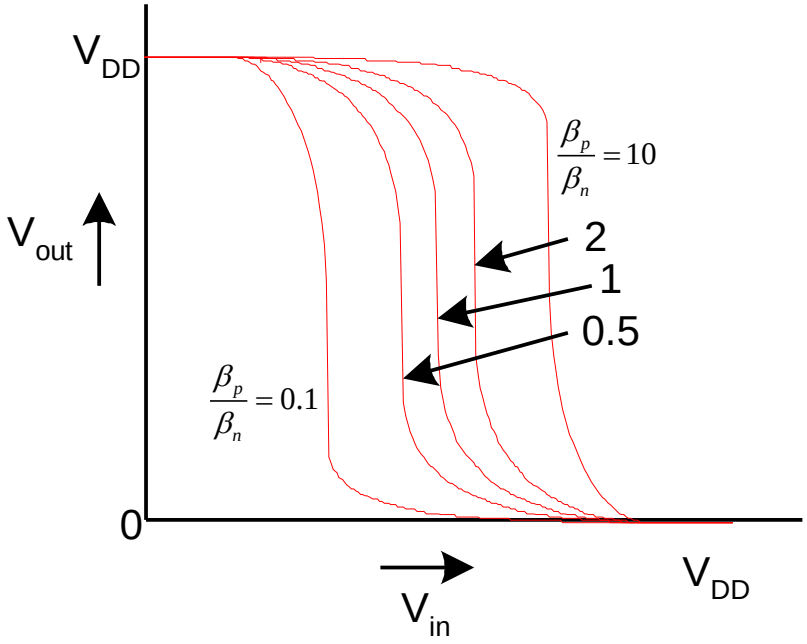


Summary of CMOS inverter operation

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$

Beta Ratio

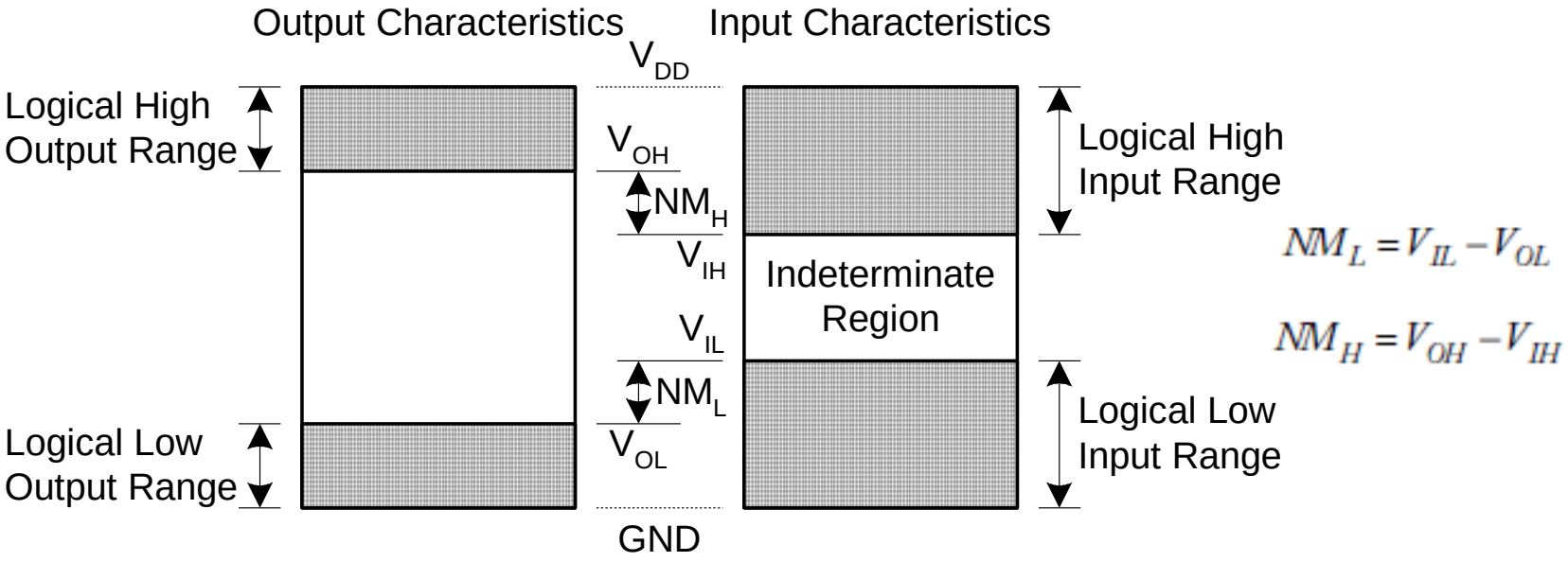
- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



Noise Margins

- How much noise can a gate input see before it does not recognize the input?

V_{IH} = minimum HIGH input voltage
V_{IL} = maximum LOW input voltage
V_{OH} = minimum HIGH output voltage
V_{OL} = maximum LOW output voltage

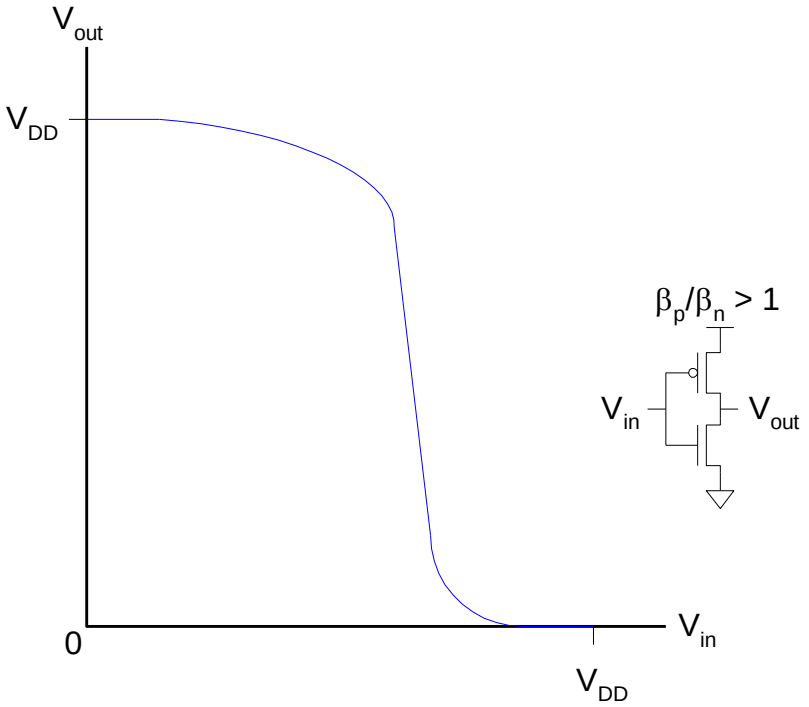


$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



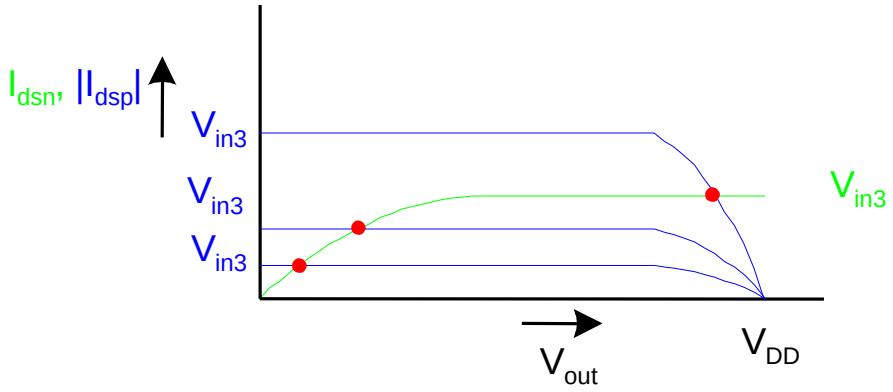
$$NM_L = V_{IL} - V_{OL}$$

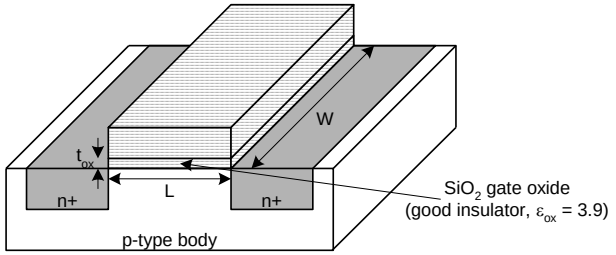
$$NM_H = V_{OH} - V_{IH}$$

where

V_{IH} = minimum HIGH input voltage
V_{IL} = maximum LOW input voltage
V_{OH} = minimum HIGH output voltage
V_{OL} = maximum LOW output voltage

What is the impact of altering the PMOS width in comparison to the NMOS width on the DC char?

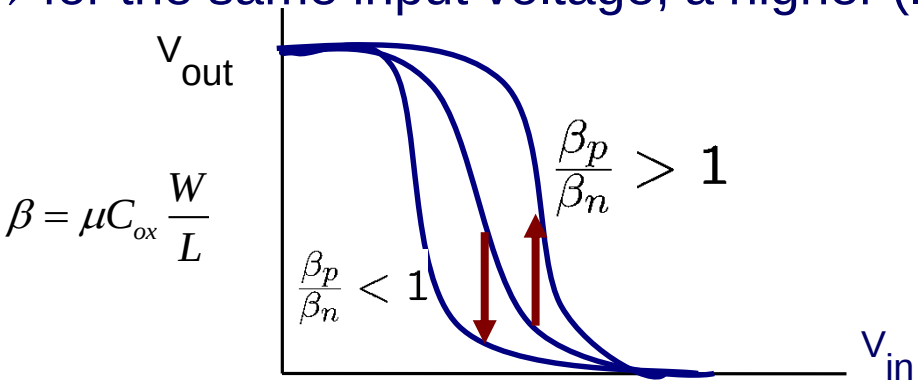


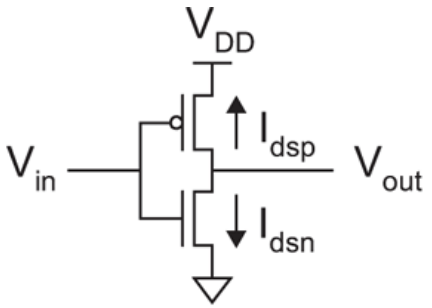


$$I_{DS} = \mu_p \frac{\varepsilon_{ox} W}{t_{ox} L}(V_{gs} - V_t)^2$$

If we increase (d[redacted]e width of PMOS compared to NMOS

→ for the same input voltage, a higher (lo[redacted]utput voltage is obtained



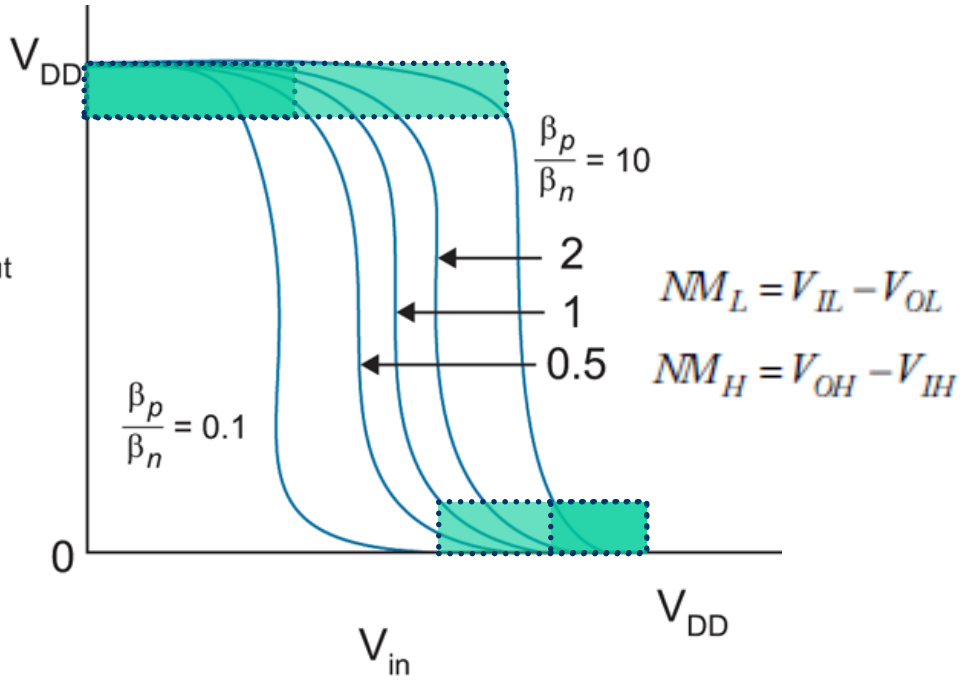


Impact of *skewing* transistor sizes on inverter noise margins

$$I_{dn} = \frac{\beta_n}{2}\left(V_{\text{inv}} - V_{tn}\right)^2$$

$$I_{dp} = \frac{\beta_p}{2}\left(V_{\text{inv}} - V_{DD} - V_{tp}\right)^2$$

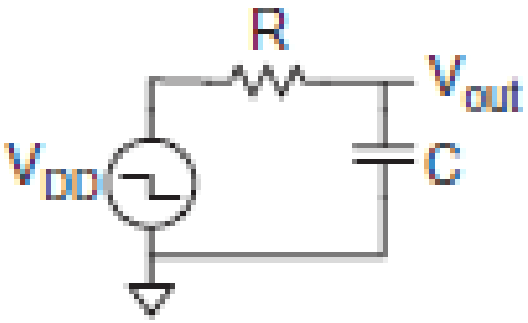
$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$



- Increasing (decreasing) PMOS width to NMOS width increases (decreases) the low noise margin and decreases (increases) the high noise margin

Transient Response

- *DC analysis* tells us V_{out} if V_{in} is constant
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to V_{DD} or vice versa



$$I = C\frac{dV}{dt}$$

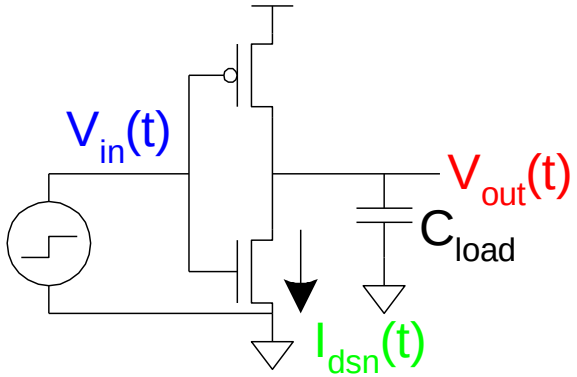
Inverter Step Response

- Ex: find step response of inverter driving load cap

$$V_{in}(t) =$$

$$V_{out}(t < t_0) =$$

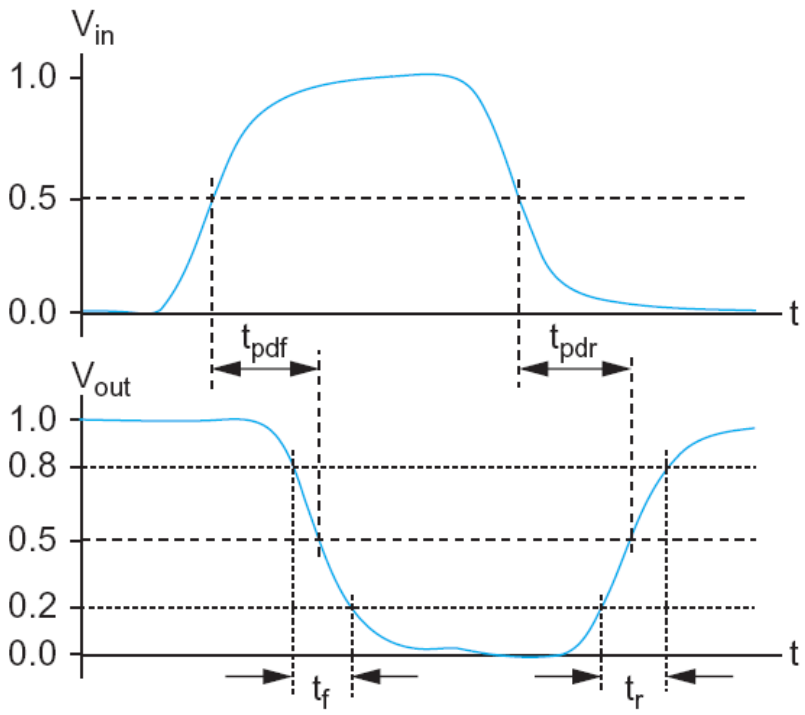
$$\frac{dV_{out}(t)}{dt} =$$



$$I_{dsn}(t) = \begin{cases} & t \le t_0 \\ V_{out} > V_{DD} - V_t & \\ V_{out} < V_{DD} - V_t & \end{cases}$$

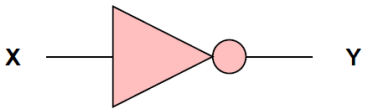
Delay Definitions

- t_{pdr}: *rising propagation delay*
  - From input to rising output crossing $V_{DD}/2$
- t_{pdf}: *falling propagation delay*
  - From input to falling output crossing $V_{DD}/2$
- t_{pd}: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- t_r: *rise time*
  - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- t_f: *fall time*
  - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

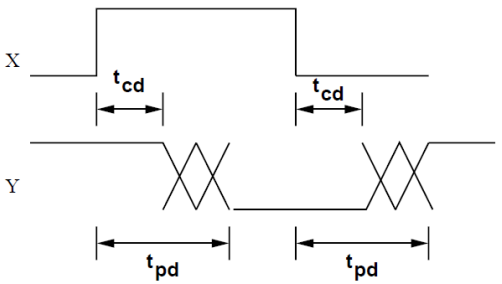


Delay Definitions

- $\mathbf{t_{cdr}}$: *rising contamination delay*
  - From input to rising output crossing $V_{DD}/2$
- $\mathbf{t_{cdf}}$: *falling contamination delay*
  - From input to falling output crossing $V_{DD}/2$
- $\mathbf{t_{cd}}$: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$

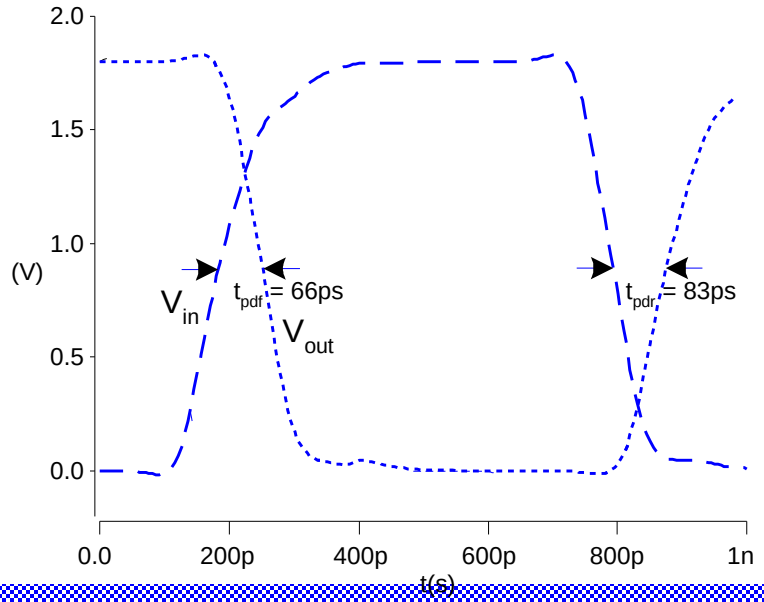


When input changes the output maintains its old value for a duration called the contamination time *max-time* and *min-time*



Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write, may hide insight



Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use *effective resistance* R
  - So that t_{pd} = RC
- Characterize transistors by finding their effective R
  - Depends on average current as gate switches

Effective Resistance

- Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
    - $I_{ds} = V_{ds}/R$
  - R averaged across switching of digital gate
- Too inaccurate to predict current at any given time
  - But good enough to predict RC delay

Transistor resistance

$$R = \frac{\partial I_{ds}}{\partial V_{ds}}^{-1}$$

In the linear region

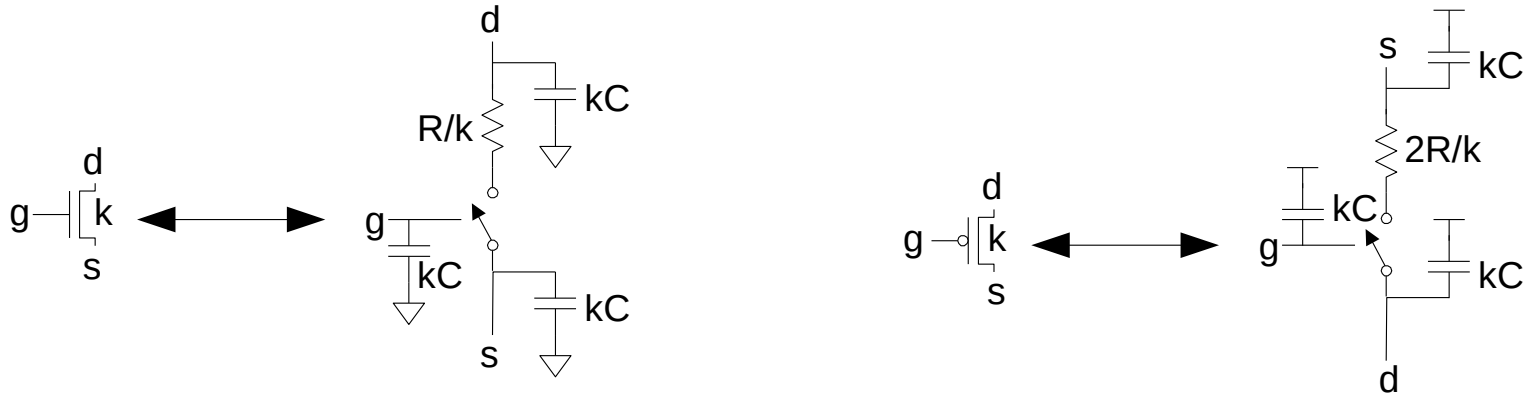
$$I_{ds} \approx \beta(V_{gs} - V_t)V_{ds}$$

$$\rightarrow R \approx \frac{1}{\beta(V_{gs}-V_t)} = \frac{1}{\mu C_{ox}}\frac{L}{W}\frac{1}{(V_{gs}-Vt)}$$

- Not accurate, but at least shows that the resistance is proportional to *L/W* and decreases with V_{gs}
- If *R/C* are for a unit size transistor then a transistor of *K* unit width has *KC* capacitance and *R/K* resistance
- The resistance of a PMOS transistor = 2× resistance of NMOS transistor of the same size

RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width

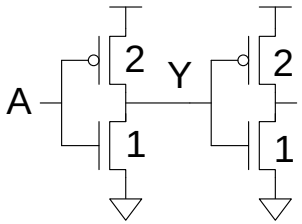


RC Values

- Capacitance
  - $C = C_g = C_s = C_d$ = 2 fF/μm of gate width in 0.6 μm
  - Gradually decline to 1 fF/μm in 65 nm
- Resistance $\rightarrow R \approx \frac{1}{\beta(V_{gs}-V_t)} = \frac{1}{\mu C_{ox}} \frac{L}{W} \frac{1}{(V_{gs}-Vt)}$
  - R ≈ 10 KΩ•μm in 0.6 μm process
  - Improves with shorter channel lengths
  - 1.25 KΩ•μm in 65 nm process
- Unit transistors
  - May refer to minimum contacted device (4/2 λ)
  - Or maybe 1 μm wide device
  - Doesn't matter as long as you are consistent

Inverter Delay Estimate

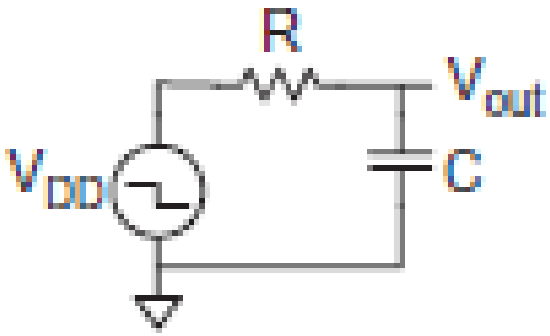
- Estimate the delay of a fanout-of-1 inverter

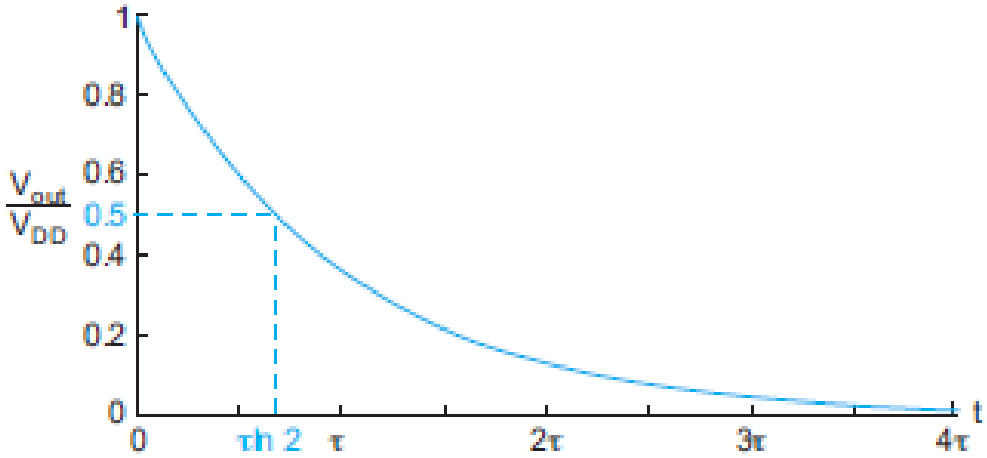


d = 6RC

If the input *A* rises, the nMOS transistor will be ON and the pMOS OFF

Transient Response(I)





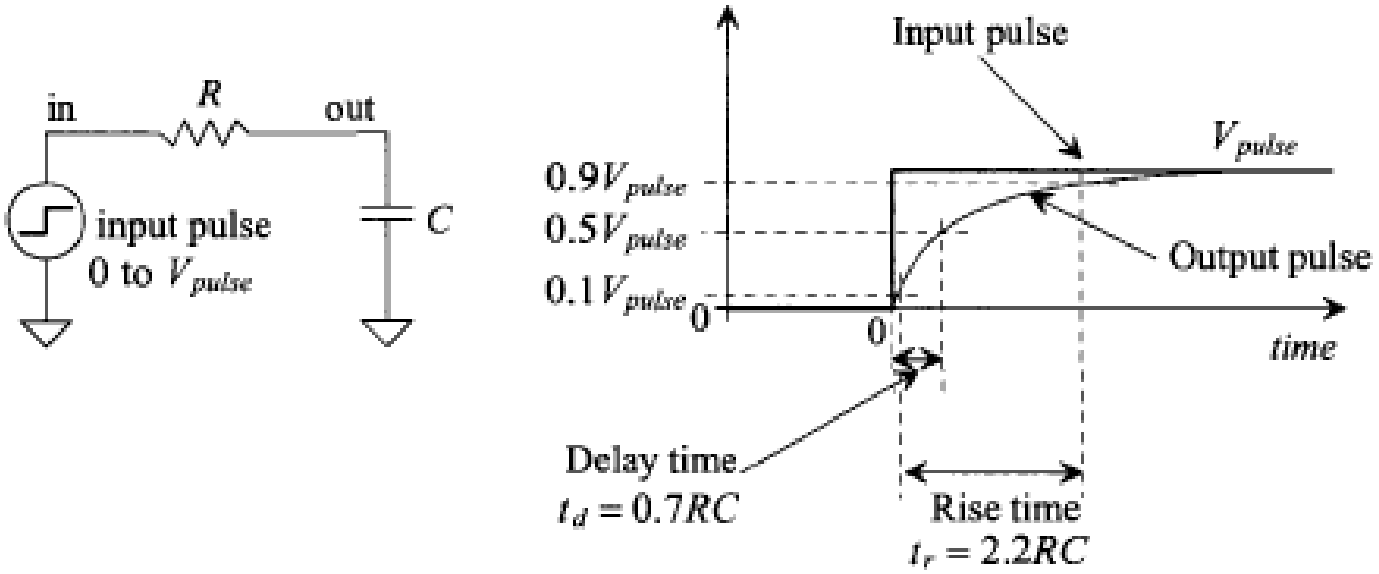
$$V_{out}(t) = V_{DD} e^{-t/RC}$$

$$t_{pd} = RC \ln 2 \approx 0.69 RC$$

$$\tau = RC$$

$$t_{pd} = RC$$

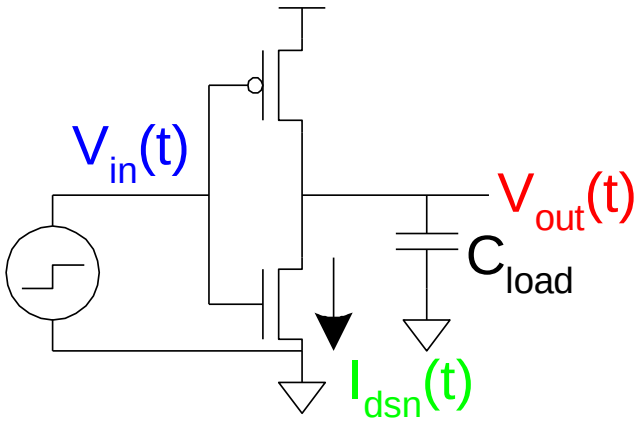
Transient Response(II)



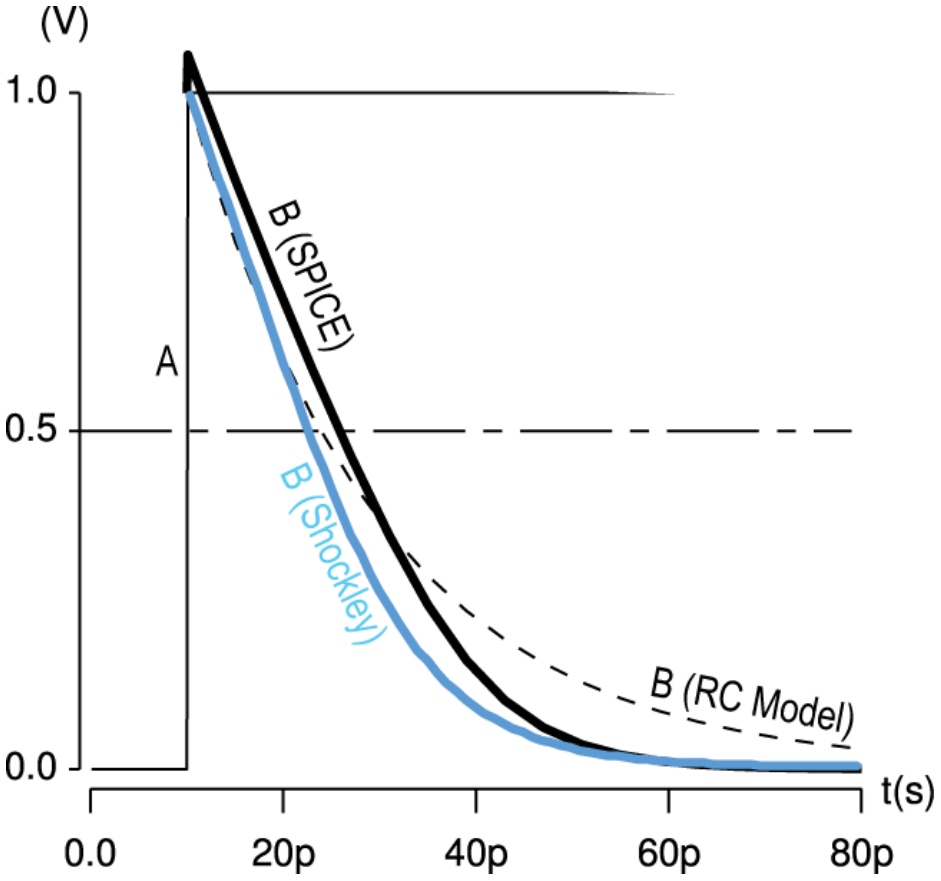
$$V_{out}(t) = V_{pulse}\left(1 - e^{-t/RC}\right)$$

$$t_{pd} = RC \ln 2 \approx 0.69RC$$

Delay Model Comparison

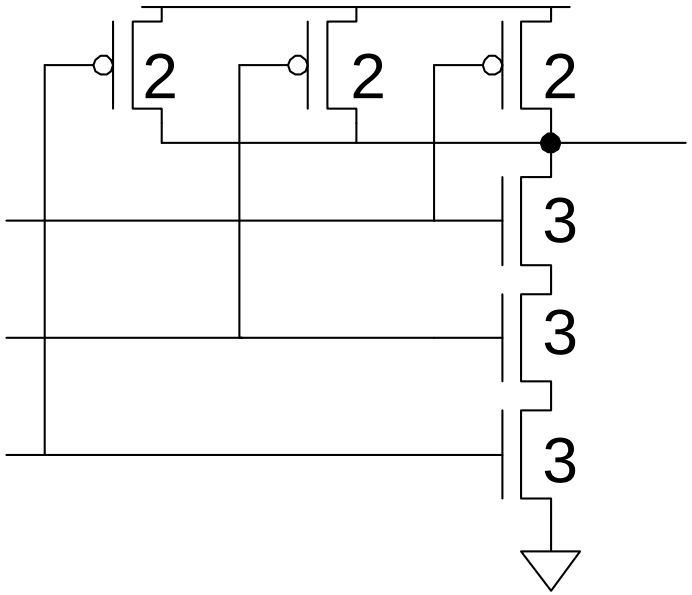


C_{load} = 20 fF
V_{DD} = 1.0 V
Vt = 0.3 V,
t_{ox} = 10.5 Å
μ = 80 cm²/V · s



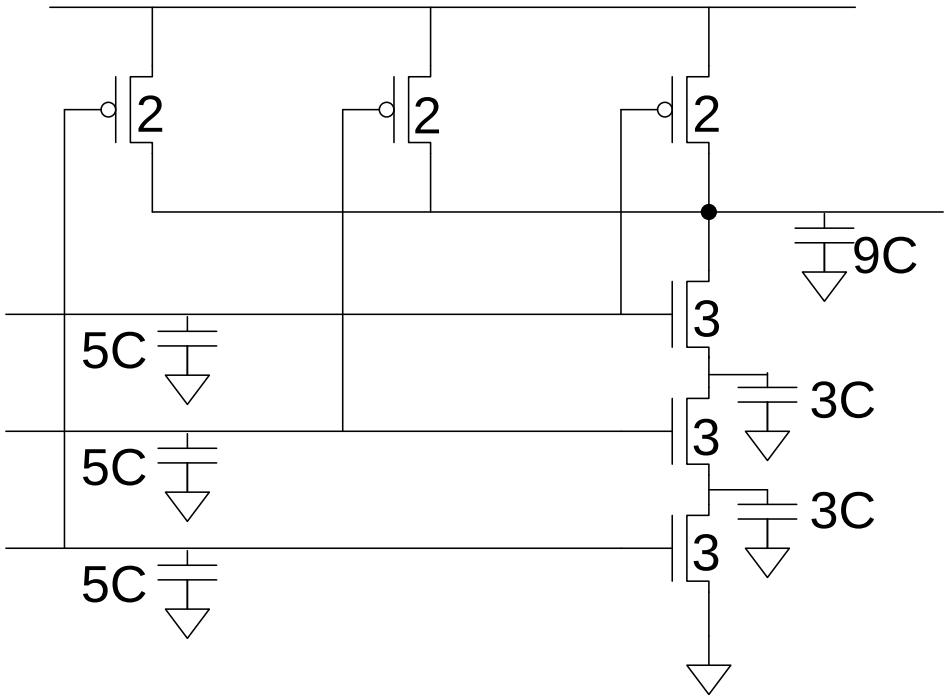
Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.

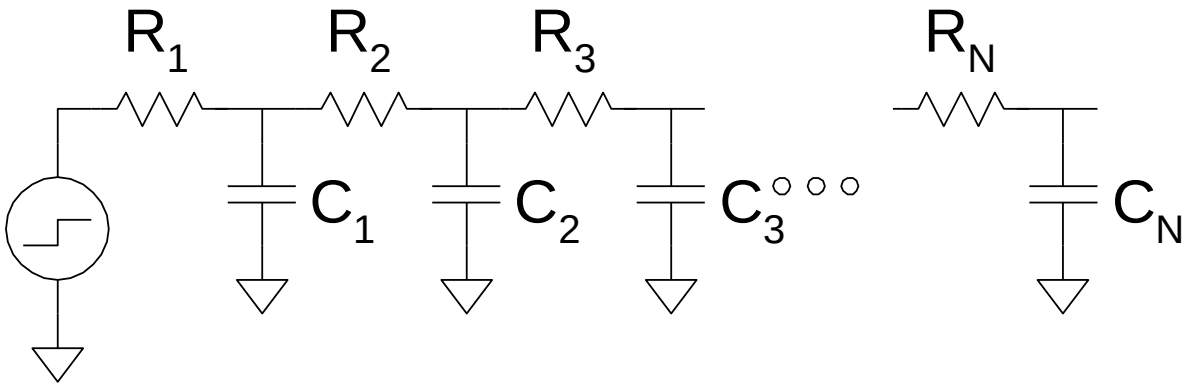


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

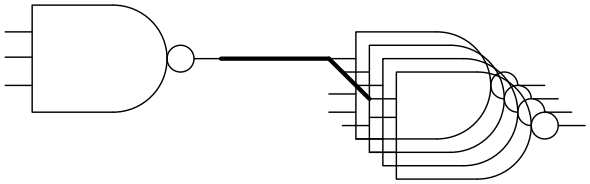
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$

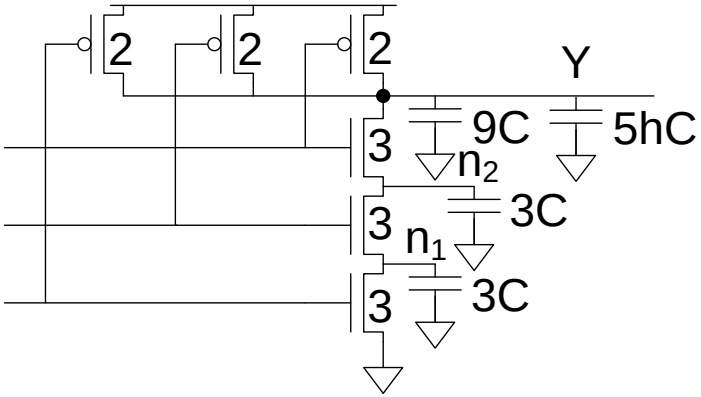


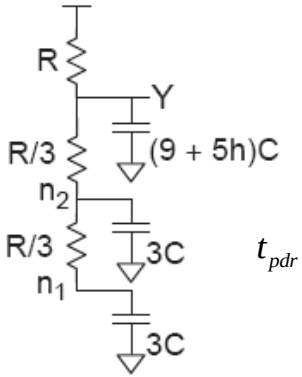
Example: 3-input NAND

- Estimate worst-case rising and falling delay of 3-input NAND driving *h* identical gates.

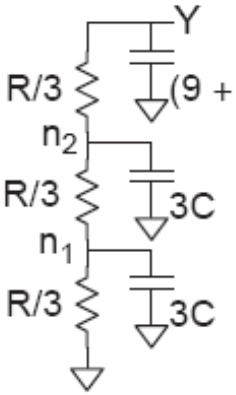


h copies





$$t_{pdr} = (9+5h)RC$$



$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

Rising

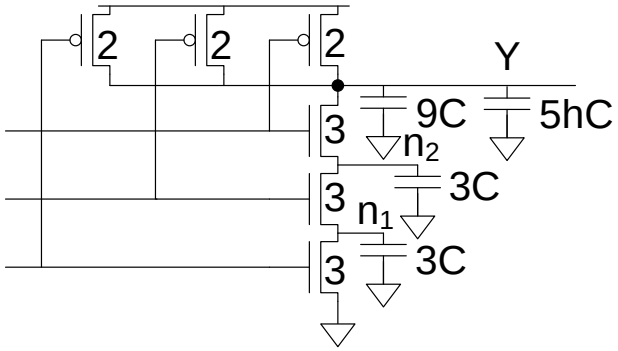
Falling

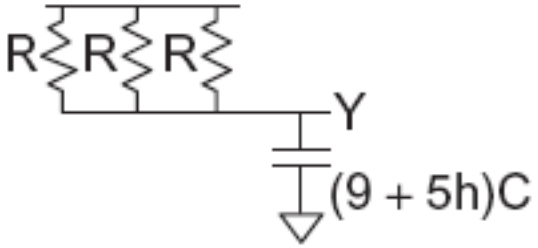
Delay Components

- Delay has two parts
  - *Parasitic delay*
    - 9 or 12 RC
    - Independent of load
  - *Effort delay*
    - 5h RC
    - Proportional to load capacitance

Contamination Delay

- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If all three inputs fall simultaneously

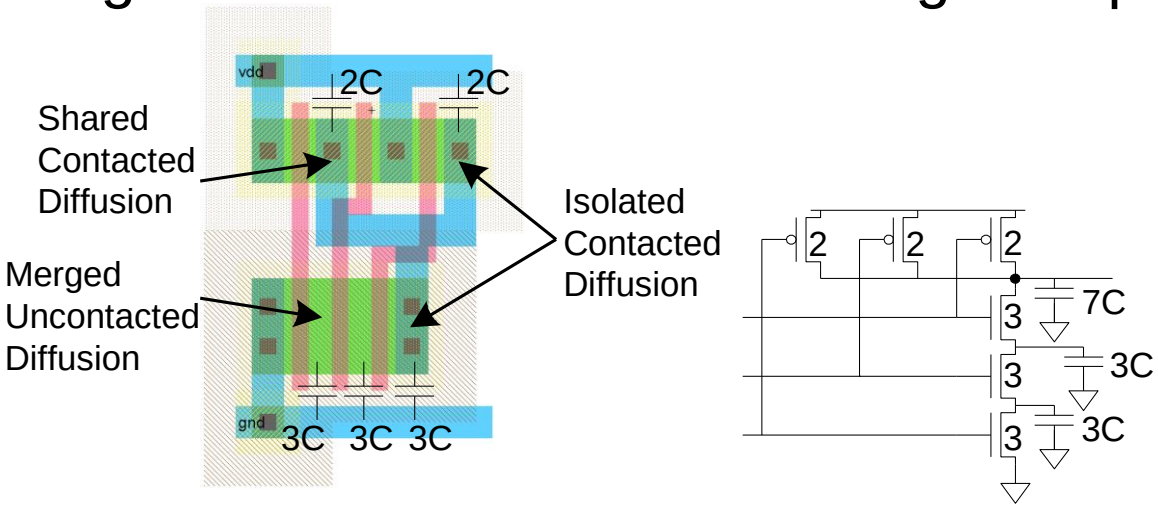




$$t_{cdr} = \left[(9+5h)C\right]\left(\frac{R}{3}\right) = \left(3+\frac{5}{3}h\right)RC$$

Diffusion Capacitance

- We assumed contacted diffusion on every s / d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too



Layout Comparison

- Which layout is better?