1. Description

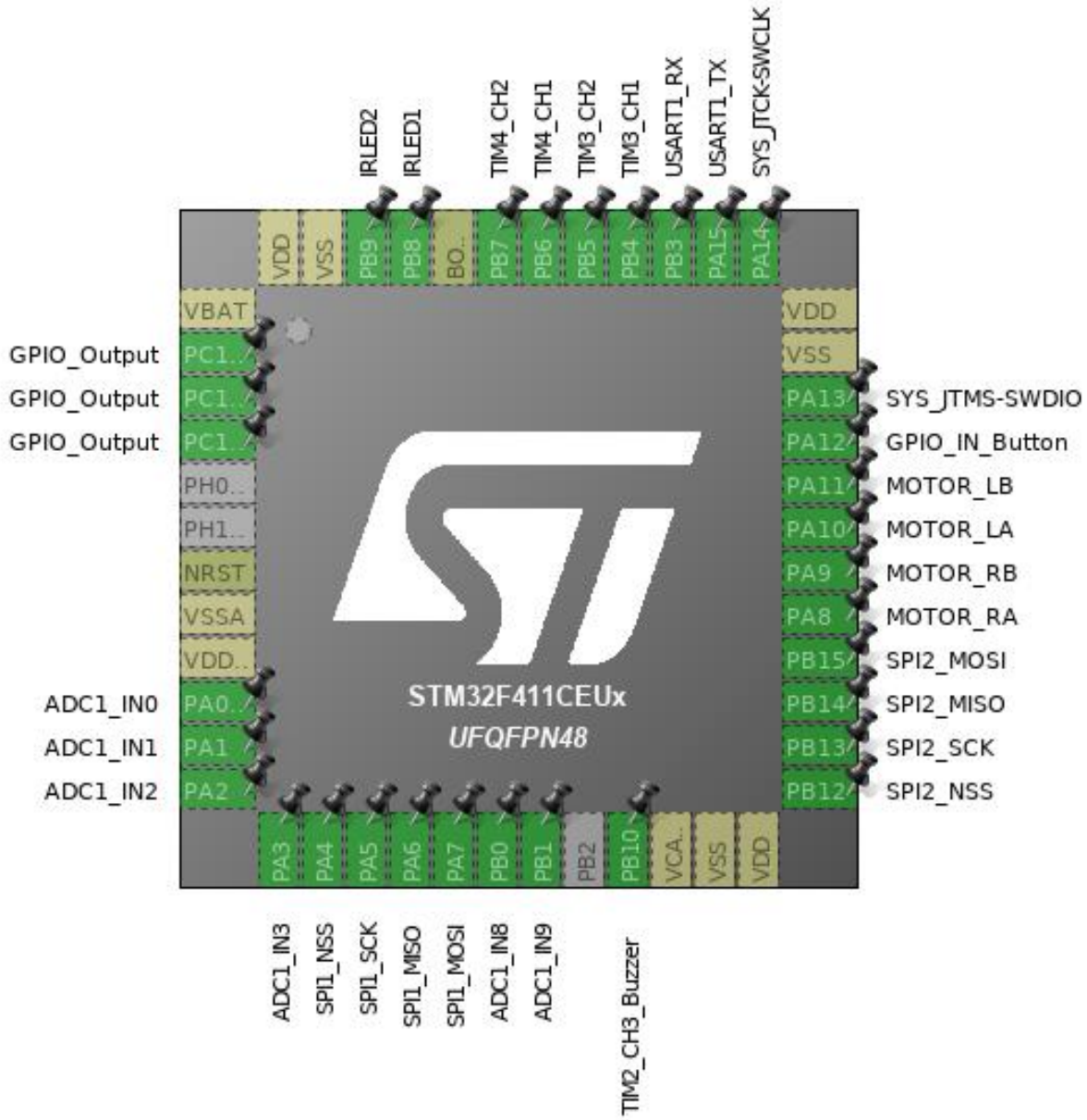
1.1. Project

Project Name	vert_firmware
Board Name	vert_firmware
Generated with:	STM32CubeMX 4.22.1
Date	10/23/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

2. Pinout Configuration



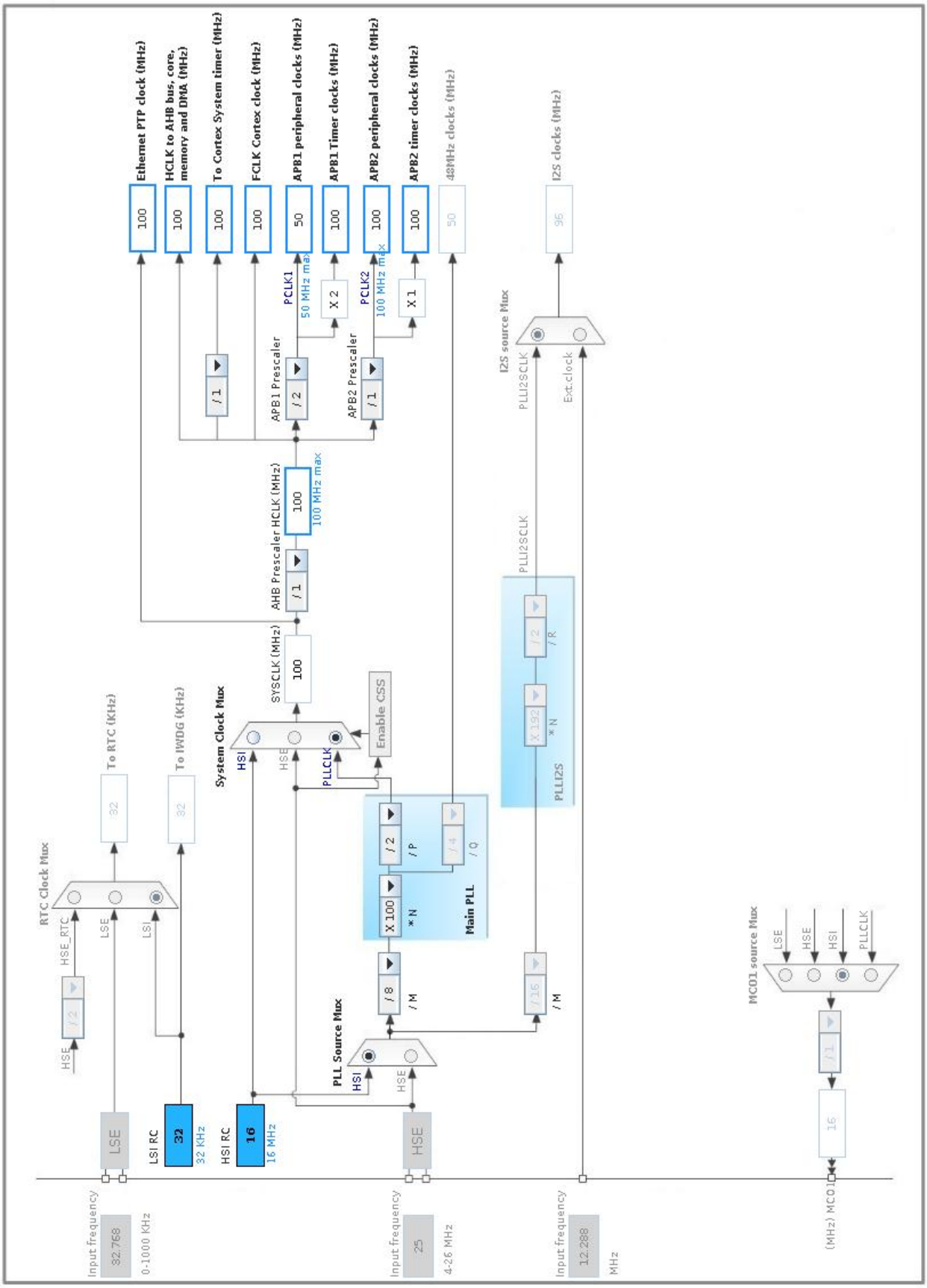
3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Output	
3	PC14-OSC32_IN *	I/O	GPIO_Output	
4	PC15-OSC32_OUT *	I/O	GPIO_Output	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
11	PA1	I/O	ADC1_IN1	
12	PA2	I/O	ADC1_IN2	
13	PA3	I/O	ADC1_IN3	
14	PA4	I/O	SPI1_NSS	
15	PA5	I/O	SPI1_SCK	
16	PA6	I/O	SPI1_MISO	
17	PA7	I/O	SPI1_MOSI	
18	PB0	I/O	ADC1_IN8	
19	PB1	I/O	ADC1_IN9	
21	PB10	I/O	TIM2_CH3	TIM2_CH3_Buzzer
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	SPI2_NSS	
26	PB13	I/O	SPI2_SCK	
27	PB14	I/O	SPI2_MISO	
28	PB15	I/O	SPI2_MOSI	
29	PA8	I/O	TIM1_CH1	MOTOR_RA
30	PA9	I/O	TIM1_CH2	MOTOR_RB
31	PA10	I/O	TIM1_CH3	MOTOR_LA
32	PA11	I/O	TIM1_CH4	MOTOR_LB
33	PA12 *	I/O	GPIO_Input	GPIO_IN_Button
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	USART1_TX	
39	PB3	I/O	USART1_RX	

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PB4	I/O	TIM3_CH1	
41	PB5	I/O	TIM3_CH2	
42	PB6	I/O	TIM4_CH1	
43	PB7	I/O	TIM4_CH2	
44	BOOT0	Boot		
45	PB8	I/O	TIM10_CH1	IRLED1
46	PB9	I/O	TIM11_CH1	IRLED2
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

mode: IN8

mode: IN9

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**6 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**28 Cycles ***
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**28 Cycles ***
Rank	**3 ***
Channel	**Channel 2 ***
Sampling Time	**28 Cycles ***
Rank	**4 ***
Channel	**Channel 3 ***

Sampling Time	**28 Cycles ***
Rank	**5 ***
Channel	**Channel 8 ***
Sampling Time	**28 Cycles ***
Rank	**6 ***
Channel	**Channel 9 ***
Sampling Time	**28 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**6.25 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.3. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**6.25 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM1

Channel1: Output Compare CH1

Channel2: Output Compare CH2

Channel3: Output Compare CH3

Channel4: Output Compare CH4

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**9 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**99 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.6. TIM2

Clock Source : Internal Clock

Channel3: Output Compare CH3

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**999 ***
Counter Mode	Up

Counter Period (AutoReload Register - 32 bits value)	**99 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 3:

Mode	**Active Level on match ***
Pulse (32 bits value)	0
CH Polarity	High

5.7. TIM3

Combined Channels: Encoder Mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.8. TIM4

Combined Channels: Encoder Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.9. TIM5

mode: Clock Source

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**19 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1999 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.10. TIM9

mode: Clock Source

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**39 ***
Internal Clock Division (CKD)	No Division

5.11. TIM10

mode: Activated

Channel1: Output Compare CH1

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**199 ***
Internal Clock Division (CKD)	No Division

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (16 bits value)	**99 ***
CH Polarity	High

5.12. TIM11

mode: Activated

Channel1: Output Compare CH1

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**199 ***
Internal Clock Division (CKD)	No Division

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (16 bits value)	**99 ***
CH Polarity	High

5.13. USART1

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_RA
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_RB
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_LA
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_LB
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH3_Buzzer
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	IRLED1
TIM11	PB9	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	IRLED2
USART1	PA15	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB3	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA12	GPIO_Input	Input mode	**Pull-up ***	n/a	GPIO_IN_Button

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Medium ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	1	0
TIM5 global interrupt	true	3	0
DMA2 stream0 global interrupt	true	2	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEUx
Datasheet	026289_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.6

7.3. Battery Selection

Battery	LiPo
Capacity	50.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.7 V
Max Cont Current	1000.0 mA
Max Pulse Current	2000.0 mA
Cells in series	1
Cells in parallel	1

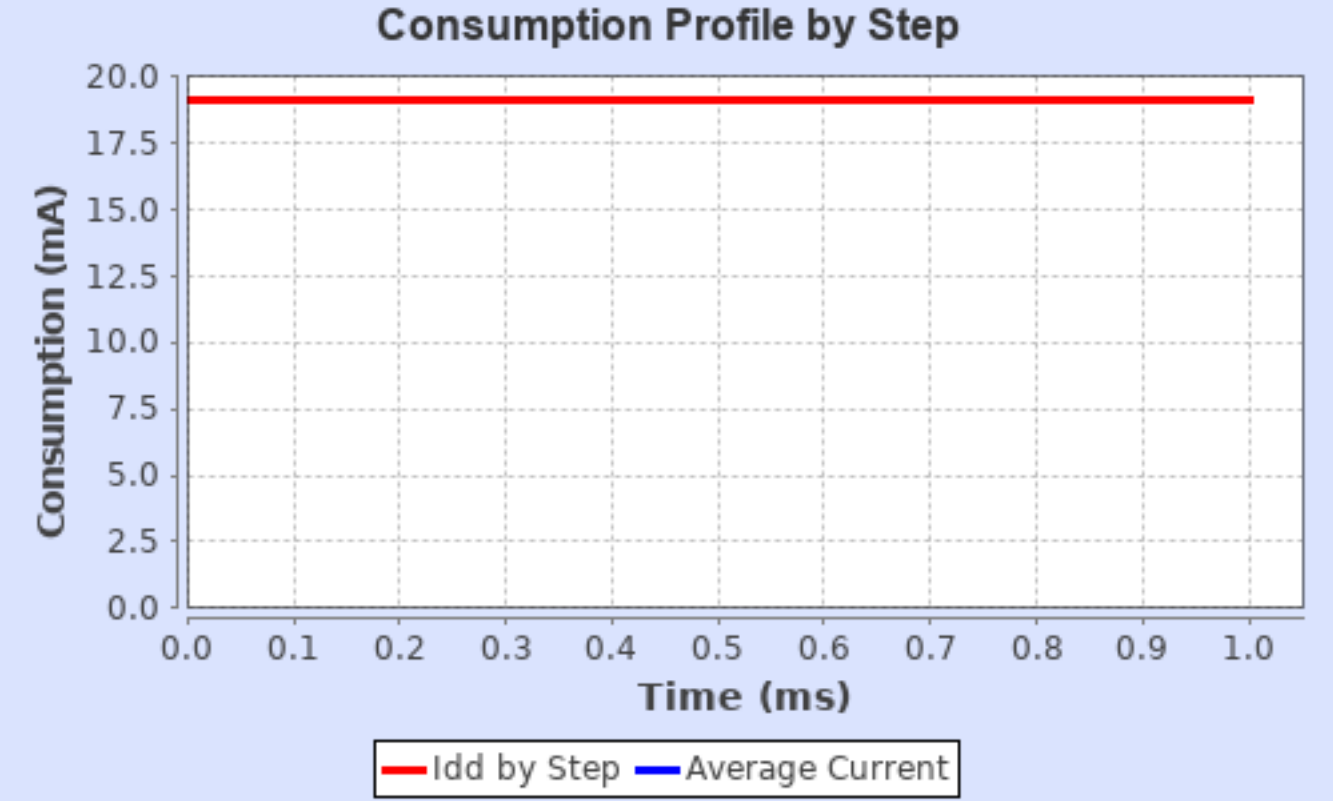
7.4. Sequence

Step	Step1
Mode	RUN
Vdd	3.6
Voltage Source	Battery
Range	Scale1-High
Fetch Type	SRAM
Clock Configuration	HSE PLL
Clock Source Frequency	4 MHz
CPU Frequency	100 MHz
Peripherals	ADC1 DMA2:3_Streams GPIOA GPIOB GPIOC SPI1 SPI2 SYS TIM1 TIM2 TIM3 TIM4 TIM10 TIM11 USART1
Additional Cons.	0 mA
Average Current	19.08 mA
Duration	1 ms
DMIPS	125.0
Ta Max	102.8
Category	In DS Table

7.5. RESULTS

Sequence Time	1 ms	Average Current	19.08 mA
Battery Life	2 hours	Average DMIPS	125.0 DMIPS

7.6. Chart


Consumption Profile by Step
Consumption (mA)
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

8. Software Project

8.1. Project Settings

Name	Value
Project Name	vert_firmware
Project Folder	/home/tokoro/dev/stm32/Projects/Vert/src/vert_firmware/autogen
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes