Qizhou Zhang

+(86)15968176893 zhangqizhou1997@outlook.com Chengdu

EDUCATION

Shanghai Jiao Tong University Sep 2019 - Mar 2022

Electrical Engineering | Master Shanghai

- Research Interests: Programmable Network, RDMA, Data Center Network, supervised by Prof. Shizhen Zhao.
- Awards: Second prize of National Post-Graduate Mathematical Contest in Modeling, 2019.
- GPA 3.5/4.0 (35%)

Hangzhou Dianzi University Sep 2015 - Jun 2019

Communication Engineering | Bachelor Hangzhou

- Awards: Second-Class Scholarship(2017)
- GPA: 3.5/4.0(30%)

WORK EXPERIENCE

Huawei Jun 2022 - Present

Software Development Engineer | Hisilicon Chengdu

As a member of TOE (TCP Offload Engine), which is part of the high-speed network service of commercialized SmartNIC products, I work on the performance optimization of our service

- Locate performance issues of TOE, such as improving inefficient implementation of the congestion control algorithm of the TOE.
- Verify optimization features of V200 series chips related to TOE service, such as 64B RQE and TCAM.

Alibaba Cloud Aug 2020 - Nov 2020

Software Engineer Intern | Network R&D Hangzhou

- Contribute to the NetSeer project, which is a network performance monitoring system that uses the INT feature of programmable switches to quickly identify link abnormalities such as packet loss and high latency.
- Use the user-mode network library DPDK to write high-performance data acquisition programs, employ Flink for data preprocessing, and utilize JAVA+Spring Boot for visualization development.

PROJECT EXPERIENCE

Research on High Performance Deadlock-free Data Center Network Design Dec 2020 - Sep 2022

- Currently, the state-of-art RDMA technology has been deployed in the Ethernet Clos Datacenters. The Expander networks demonstrate performance advantages over equal-cost Clos networks in recent literature. However, the combination of RDMA and Expander network is under-explored. We focused on the deadlock-solving when deploying RoCEv2 that depends on PFC in an expander-based network topology
- Propose a topology-routing co-designed methodology called Flattened Clos (FC) to avoid cyclic buffer dependency, then eliminate the PFC-induced deadlocks.
- Compared to an expander network with the edge-disjoint-spanning-tree (EDST) based routing (a state-of-art CBD-free routing algorithm for expander networks), FC reduces the average hop count by at least 50% and improves network throughput by 2× or more
- Compared to Clos networks with up-down routing, FC increases network throughput by 1.1−2× under all-to-all and uniform random traffic patterns

Publication

- Flattened Clos: Designing High-performance Deadlock-free Expander Data Center Networks Using Graph Contraction. Shizhen Zhao*, Qizhou Zhang*, Peirui Cao, Xiao Zhang, Xinbing Wang, Chenghu Zhou, NSDI 2023. (*These authors contribute equally to this work)

Other

Skillset: C++, JAVA, Python, Redis, ibverbs.

Language: CET6