2019/Jan/24

A model of classical quantum computing method

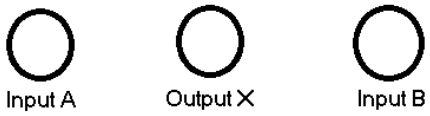
Ryoji Furui

www.ryoji.info

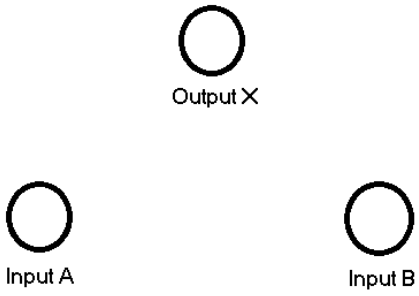
Here, introduced a model of classical computing method using electric field. This could produce wireless logic circuit. In this model, electric field is used to transfer bit signals. Transfer method might be applied by semiconductive layer, optical, other physical properties or combined devices.

1) Hardware design of logic gate,

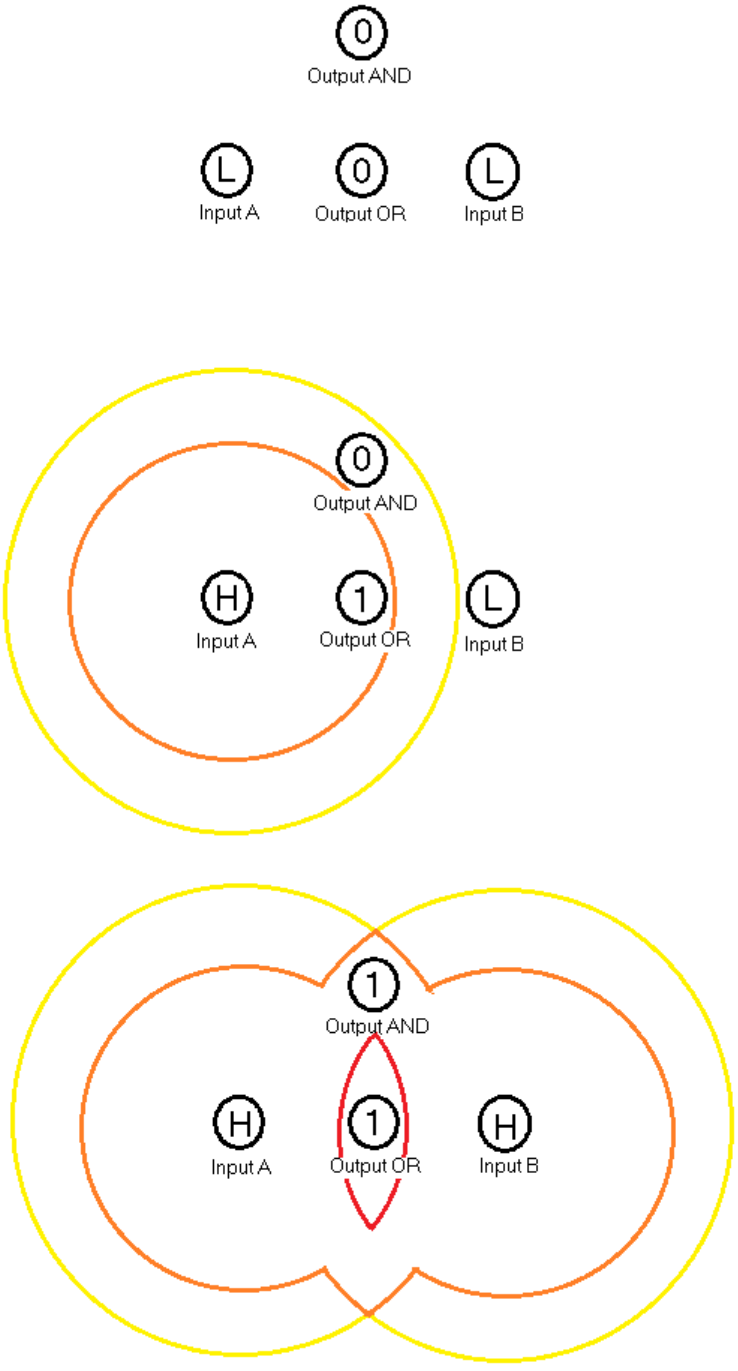
OR gate; Input A and B will generate each electric fields. Generating electric filed means input is high. Output X receives electric potential to conduct if either of input generates field.



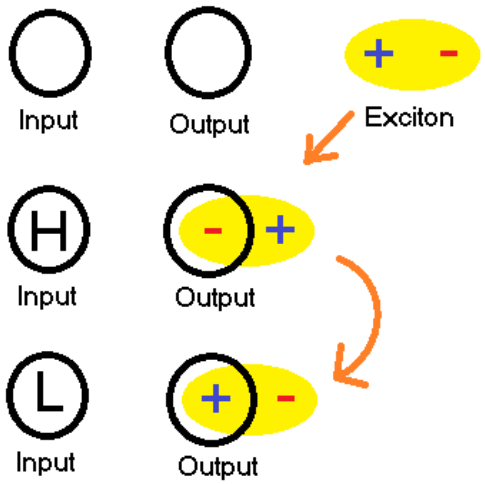
AND gate; Output X is placed at a little far from Inputs than OR gate. Therefore it can conduct only when both inputs generate fields at the same time.



Combo gate; The picture below shows the combination gate of OR, AND. Three cases show how electric fields are generated and conduct outputs.



NOT gate; NOT gate could be embedded on logic board as existing current modules or at quantum level operation, trapping exciton on output's edge could result inverse as exciton would flip by electric field generated by input.



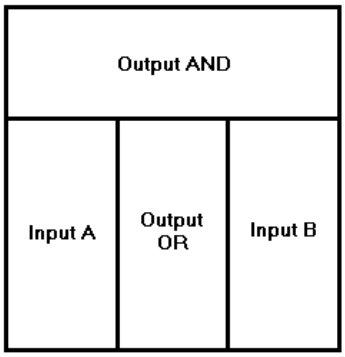
2) Conclusions

These gate designs could scale down to atomic scale (1 bit = 1 electron at minimum, possibly) by using graphene or carbon nano tube, or even at larger scale, this new classical computing method may overcome several hardware limitations encountered in these days.

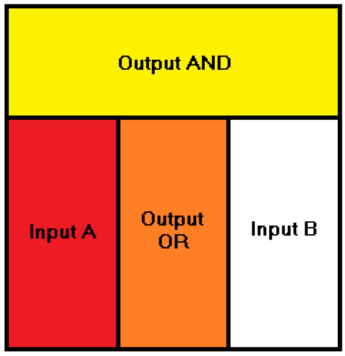
In this model using electric field, the difference between OR, AND gate is represented to the distance of Output from each input. In the different approach with other transfer method of bit signals, the distance could be replaced to any value of properties which can recognize OR, AND.

Appendix (added on 2019/Jan/30)

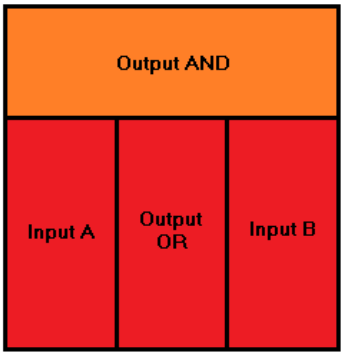
Combo gate using semiconductive layer; Picture below shows semiconductive layer. OR block has double junction area with input compared to AND block. The difference of junction area could conduct each result instead of distance using electric field.



A	B	AND	OR
0	0	0	0



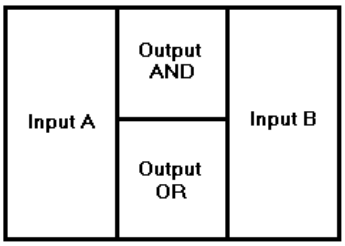
A	B	AND	OR
1	0	0	1



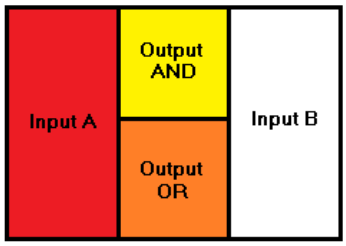
A	B	AND	OR
1	1	1	1

Appendix 2 (added on 2019/Feb/5)

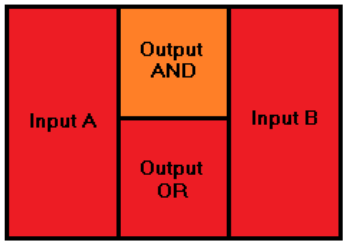
Combo gate using semiconductive layer 2; Picture below shows semiconductive layer. OR block has lower conductive threshold than AND block by using different characteristic or semiconductor for each.



A	B	AND	OR
0	0	0	0



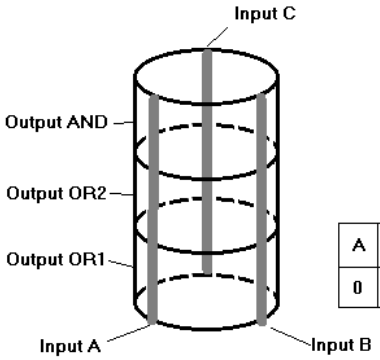
A	B	AND	OR
1	0	0	1



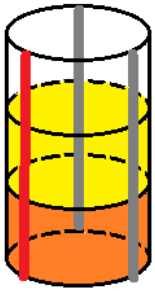
A	B	AND	OR
1	1	1	1

Appendix 3 (added on 2019/Feb/18)

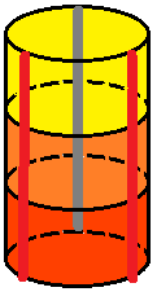
Super combo (Trinary) gate using semiconductive layer; Picture below shows semiconductive layer which consists three inputs and outputs. Three outputs has different conductive threshold with the same way as Appendix 2. The number of input and output can be arranged.



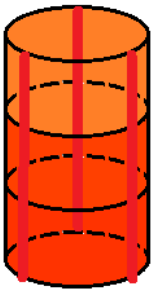
A	B	C	AND	OR1	OR2
0	0	0	0	0	0



A	B	C	AND	OR1	OR2
1	0	0	0	1	0



A	B	C	AND	OR1	OR2
1	1	0	0	1	1



A	B	C	AND	OR1	OR2
1	1	1	1	1	1