MIME 262, Lecture 18, March 19, 2012
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1 PN Junction

A PN junction is simply two semiconductors, one *n-type* and the other *p-type*, sandwitched together. Because of the difference in Fermi energy of the two semiconductors, electrons in *n-type* have higher energy than those in the *p-type*,and there is a net migration of electrons into the *p-type* region. Similarly, there is a net flux of holes into the n-type region. Figure 1 illustrates the difference in Fermi energy of the PN junction immediately after the two materials are joined. Figure 2 illustrates the charge distribution after the electron/holes have migrated.

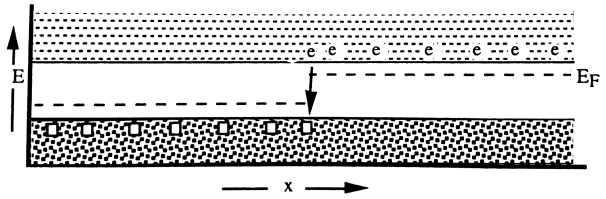

Figure 1: Band model of PN junction immediately after the two materials are joined

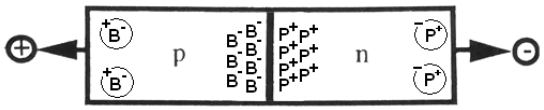

Figure 2: Charge distribution in PN junction at equilibrium

1.1 Biasing

1.1.1 Zero bias

Necessarily, the flow of electrons reaches an equilibrium at room temperature where there is a net accumulation of negative charges in the p-type region, and a net accumulation of positive charge in the n-type region. Because of the inherent attraction of opposing charges, the holes and electrons remain relatively close to the barrier between the two semiconductors. The charge accumulation is illustrated in figure 2. The band model (figure 3) reveals the energy distributions across the junction when zero potential is applied. The separation of charge creates a potential difference at the interface (as shown in the figure) and leads to a homogenous Fermi energy across the junction. The potential difference inhibits the flux of electrons or holes across the interface (hence equilibrium is established)

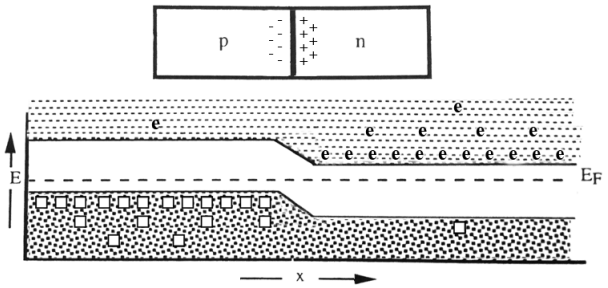

Figure 3: Concentration of electrons and holes with no biasing

1.1.2 Forward bias

If a voltage is applied as shown in figure 4, the potential difference across the interface is reduced. As a result, the greater concentration of electrons in the *n-type* region flow into the *p-type* region in the direction of decreasing electric field. Similarly, holes in the *p-type* region flow into the *n-type* region.

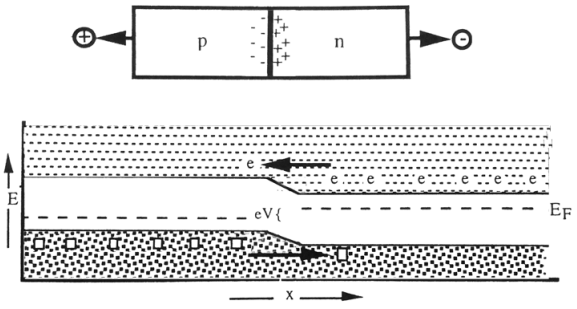

Figure 4: Net flow of electrons and holes when forward bias

1.1.3 Reverse bias

If a voltage is applied as shown in figure 5, the potential difference across the interface is increased. Electrons from the *p-type* region flow in the direction of decreasing electric field towards the *n-type* region.

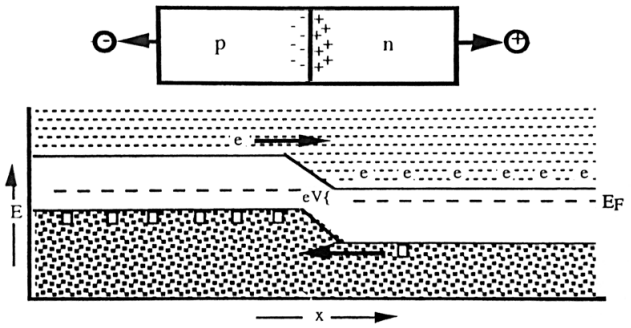

Figure 5: Net flow of electrons and holes when reversed bias

1.2 Current

(i) $V_a > 0$: Electrons move to the *p-type* region and recombine with holes. Similarly, holes move to the *n-type* region and recombine with electrons. The result is constant current due to majority carriers. As the voltage is increased, an exponentially greater number of electrons/holes move across the interface (since they are present in exponentially increasing amounts according to the Fermi-Dirac distribution).

(ii) $V_a < 0$: Electrons move to the *n-type* region and find themselves in an electron-rich region. Similarly, holes move to the *p-type* region and find themselves in a hole-rich region. The result is small current due to a low concentration of minority carriers.

The current versus applied voltage is shown if figure 6.

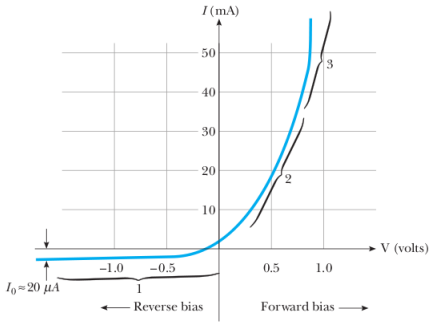

Figure 6: Voltage characteristics of a PN junction

2 Bipolar Junction Transistor

The bipolar junction transistor (BJT), is simply a PN and NP junction sandwiched together (or NP and PN for NPN transistors) as shown in figure 7. By applying a controlled voltage across the middle *n-type* (or *p-type*) region, called the base, the BJT can either be switched on or off.

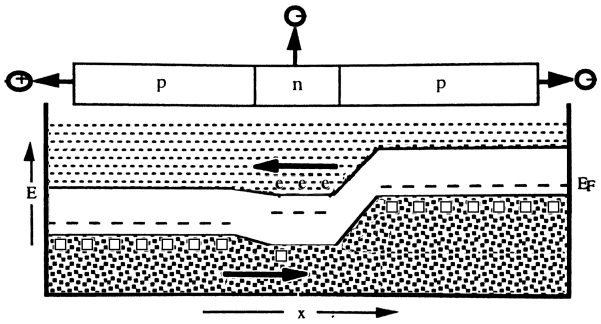

Figure 7: Band model of PNP transistor with negative base voltage

Figure 7 shows a simplified band model of the BJT with a negative base voltage applied. As the base voltage decreases, the potential difference at the two junctions decreases, and current increases exponentially.

3 Metal-Oxide Field Effect Transistors

A typical PMOS (p-enhanced MOSFET) transistor is shown in figure 8. As an increasing negative voltage is applied to the gate, positive charges accumulate in the channel and the two p-type regions essentially form a conducting path and current flows from source to drain (see figure 9). Without a voltage at the gate, the MOSFET acts like a reversed-biased PN junction.

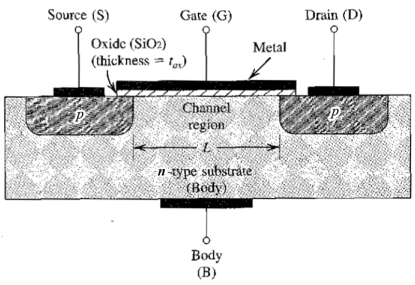

Figure 8: p-enriched MOSFET

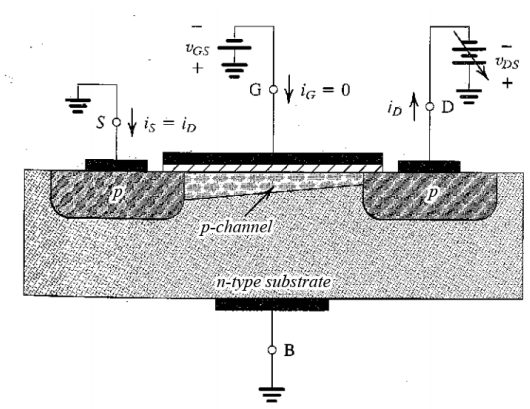

Figure 9: p-enriched MOSFET, switched on with negative source-gate voltage

4 MOSFET Fabrication

4.1 Generate SiO_2 layer

In order to generate a layer of SiO_2, the silicon is heated to 1000° C.

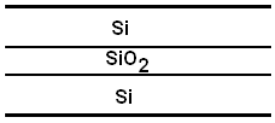

Figure 10: Heating Si to generate SiO_2 layer

4.2 Spin photoresistive layer

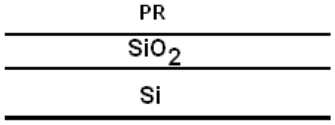

Figure 11: Spin photoresist layer

4.3 Exposure

By exposing the sample to light through a mask, the exposed photoresist layer is weakened.

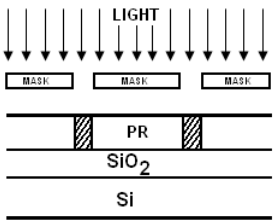

Figure 12: Exposed sample

4.4 First development

By sample is developed to remove the exposed photoresist layer.

Figure 13: Developed sample

4.5 Etching

The exposed SiO_2 is etched away.

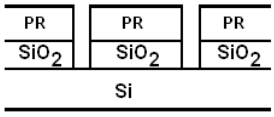

Figure 14: Etched sample

4.6 Second development

The sample is again developed to remove the remaining photoresitive material.

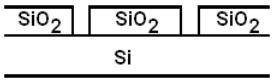

Figure 15: Developed sample with PR removed

4.7 Depositing the dopant

The sample is covered with a vapour or dopant material.

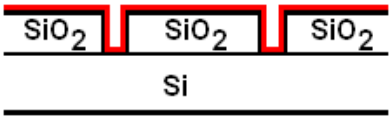

Figure 16: Sample with deposited dopant

4.8 Diffusion

The sample is heated such that the dopant diffuses into the silicon

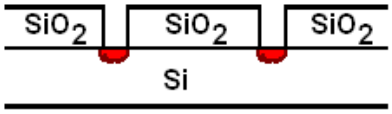

Figure 17: Sample with diffused dopant in silicon