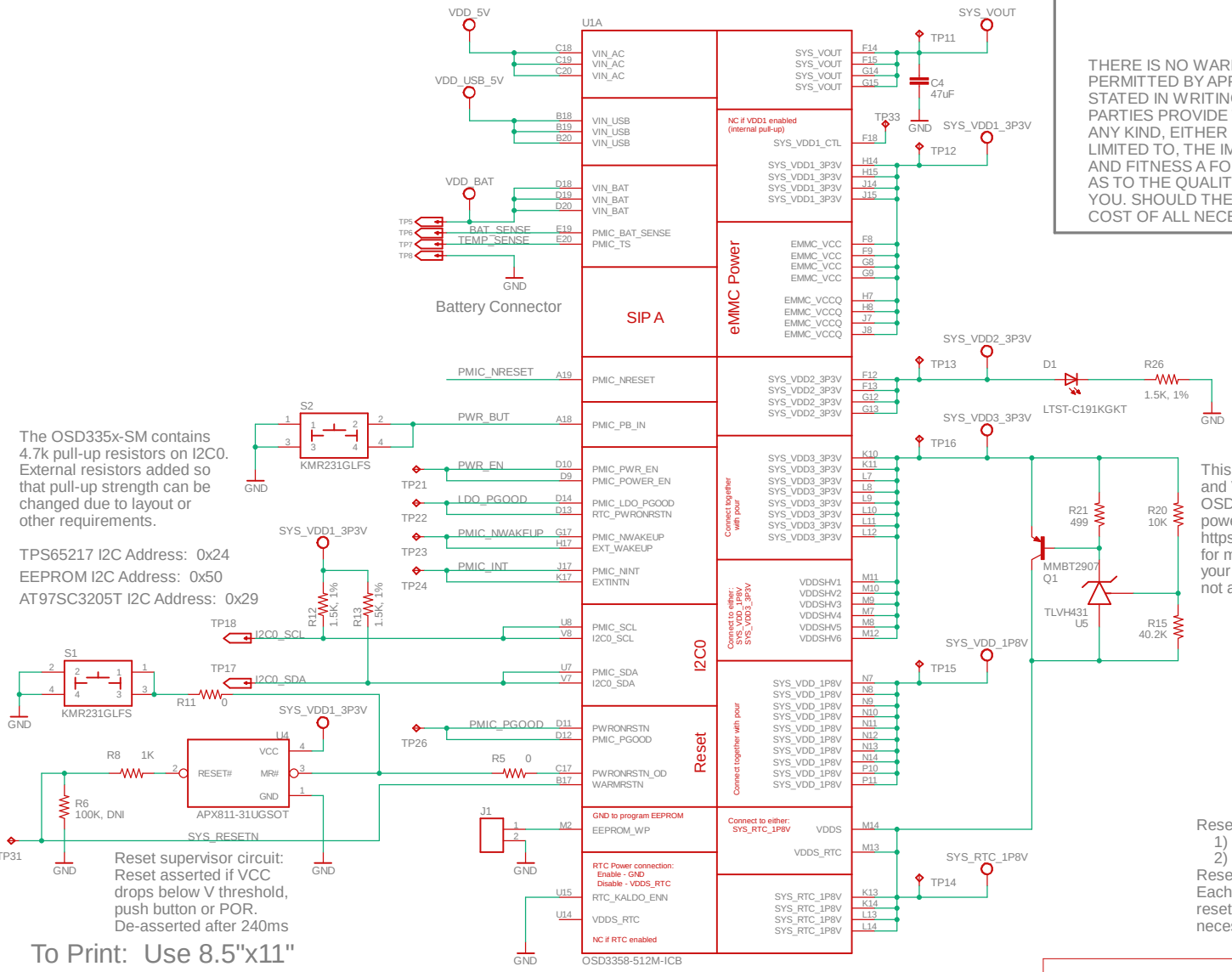
Power & Reset



THERE IS NO WARRANTY FOR THIS DESIGN, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN *AS IS* WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS A FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN IS WITH YOU. SHOULD THE DESIGN PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.

The OSD335x-SM contains 4.7k pull-up resistors on I2C0. External resistors added so that pull-up strength can be changed due to layout or other requirements.

TPS65217 I2C Address: 0x24
EEPROM I2C Address: 0x50
AT97SC3205T I2C Address: 0x29

Reset supervisor circuit: Reset asserted if VCC drops below V threshold, push button or POR. De-asserted after 240ms

This is a clamping circuit between the VDDS and VDDSHV inputs of the AM335x inside the OSD335x-SM. The clamping circuit is related to power down issues (see https://octavosystems.com/osd335x/clamping/ for more information). This may not be needed in your application if the power down conditions do not apply to your application.

Reset inputs:
1) Manual push-button
2) PMIC_PGOOD
Reset supervisor MR# has internal pull up to SYS_VDD1_3P3V. Each reset input is effectively open drain and can only pull reset line low. Resistors added only for debug and are not necessary.

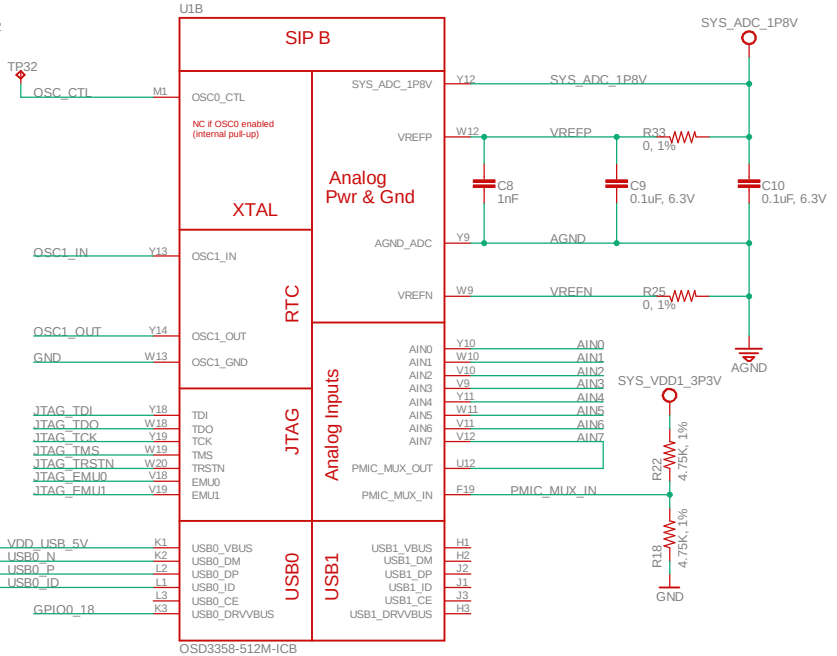
To Print: Use 8.5"x11" paper in landscape; 0.69 scaling factor.

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 1/15	Rev 0

Clocks, Analog & USB

The values for C7 and C12 can be calculated using information in FAQ: https://octavosystems.com/faqs/design-oscillator-circuit-osd335x-family-devices/#more-3862

Clock resistors R32 and R24 may not be needed in your design. See https://octavosystems.com/osd335x/clock/ for more information.



If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.

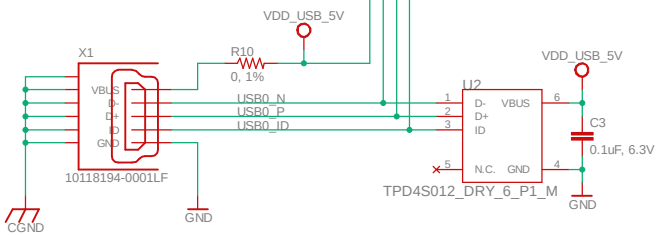
SYS_ADC_1P8V and AGND_ADC are connected to SYS_VDD_1P8V and DGND, respectively, through ferrite beads inside the SiP. It is not necessary to connect these rails to anything else. However, bypass capacitors should be added to reduce noise, if needed for your application.

Maximum voltage for the analog inputs is 1.8V.

AIN7 currently monitors the PMIC voltages via the internal PMIC mux. See the `Analog Multiplexer' section of the TPS65217 datasheet. For the internal PMIC voltages, there are dividers within the PMIC to keep the montiored voltages under 1.8V. However, PMIC_MUX_IN does not have any dividers and must be less than 1.8V. By default, PMIC_MUX_OUT is Hi-Z. The MUXCTRL register in the PMIC is used to select the PMIC_MUX_OUT voltage path.

SYS_VDD1_3P3V is a 3.3V output of the OSD3358-512M-ICB. A divide by 2 resistor divider is used to ensure that the PMIC_MUX_IN voltage does not exceed 1.8V. It is not necessary to monitor the TL5209 LDO output and this can be removed if desired.

The 0 Ohm resistor (R10) on the VBUS input can be replaced with a ferrite bead for noise suppresion or a solder bridge for cost reduction.

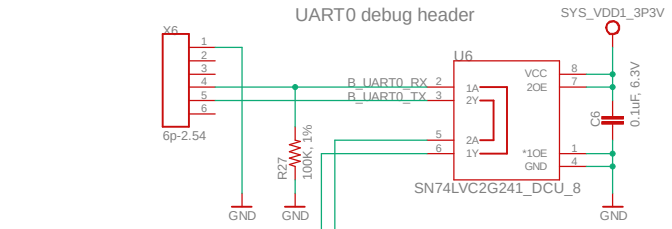


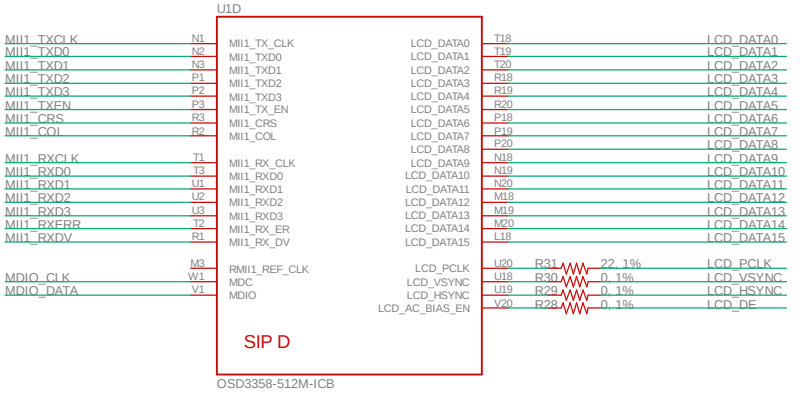
RTC_KALDO_ENN is grounded thru a 10K ohm resistor so that the internal RTC LDO is enabled and CAP_VDD_RTC does not need to be connected to VDD_CORE.

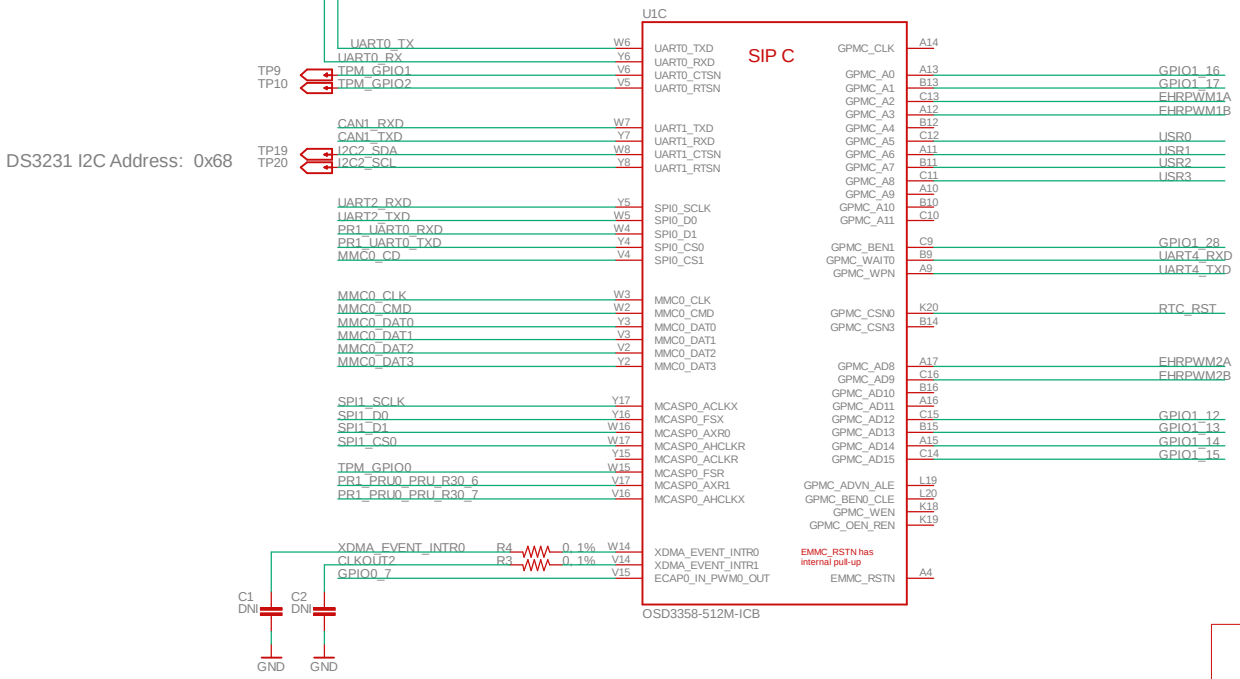
USB Client

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 2/15	Rev 0

SiP Interfaces

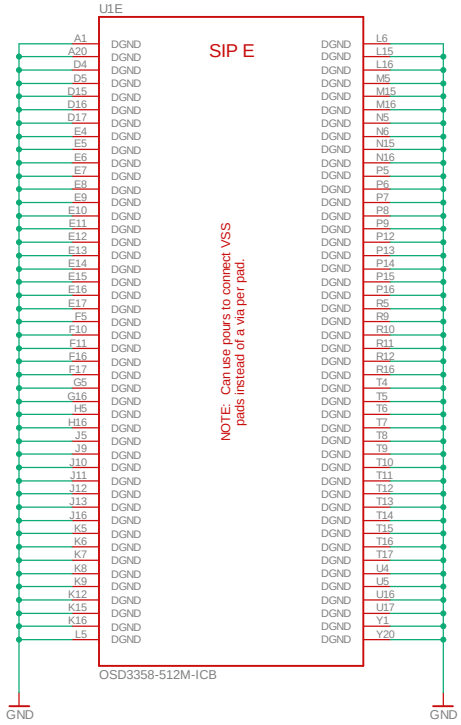


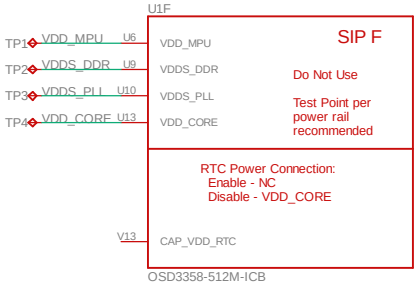


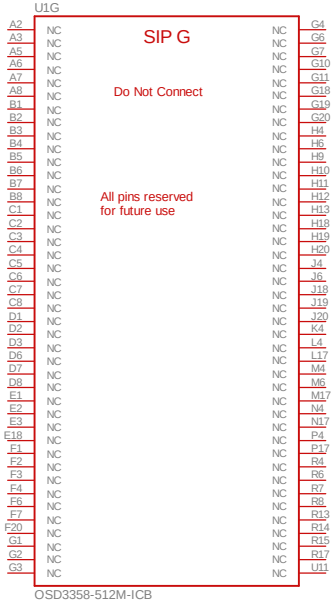


Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 3/15	Rev 0

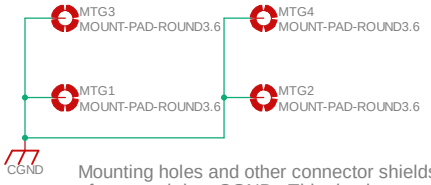
SiP GND & Misc







Mounting Holes

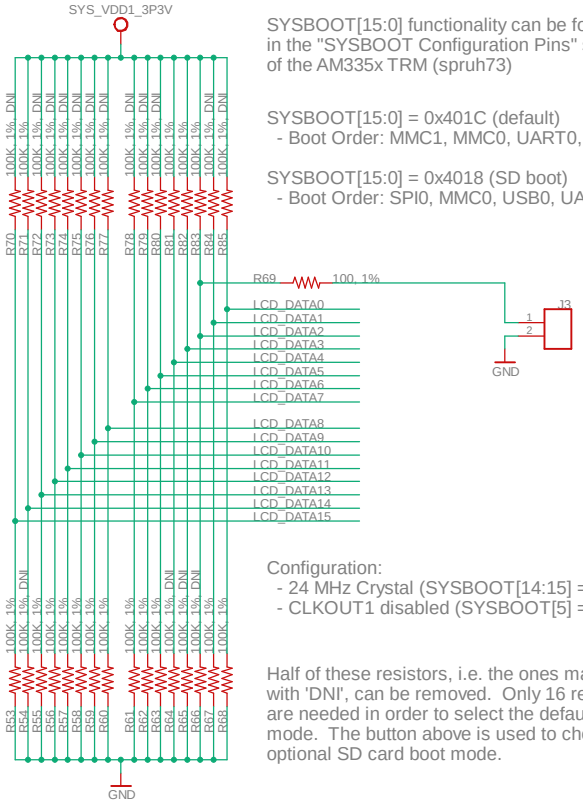


Mounting holes and other connector shields are part of a ground ring, CGND. This ring is connected to ground via a resistor on Page 1.

Fiducials

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 4/15	Rev 0

Boot configuration



SYSBOOT[15:0] functionality can be found in the "SYSBOOT Configuration Pins" section of the AM335x TRM (spruh73)

SYSBOOT[15:0] = 0x401C (default)
- Boot Order: MMC1, MMC0, UART0, USB0

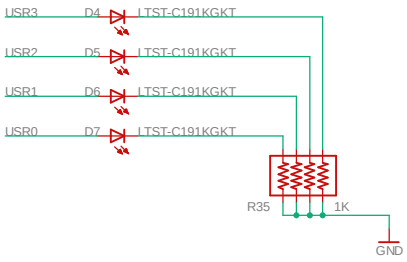
SYSBOOT[15:0] = 0x4018 (SD boot)
- Boot Order: SPI0, MMC0, USB0, UART0

BOOT Select Jumper:
On for SDC Boot

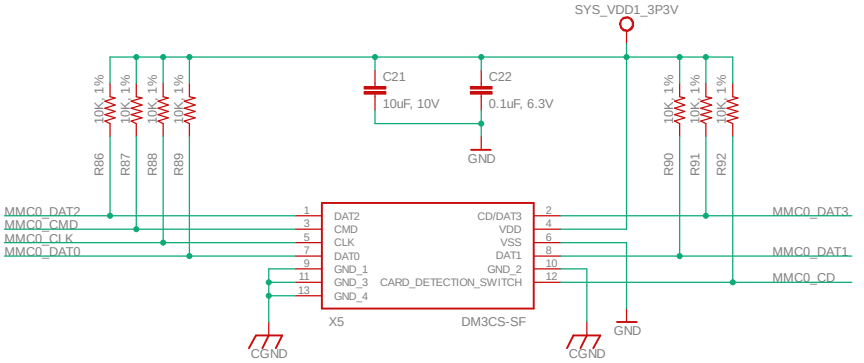
Configuration:
- 24 MHz Crystal (SYSBOOT[14:15] = 01b)
- CLKOUT1 disabled (SYSBOOT[5] = 0b)

Half of these resistors, i.e. the ones marked with 'DNI', can be removed. Only 16 resistors are needed in order to select the default boot mode. The button above is used to choose an optional SD card boot mode.

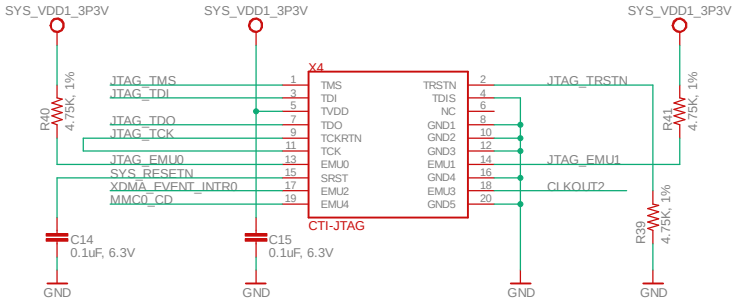
User LEDs



Micro SD card slot



JTAG Header

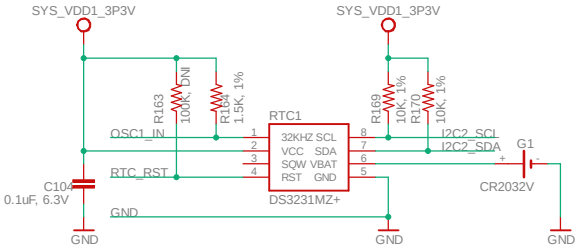


Only connect EMU2, EMU3 and EMU4 if you plan to use advanced JTAG features (HS-RTDX, Core Trace, System Trace, etc) of higher end debuggers:

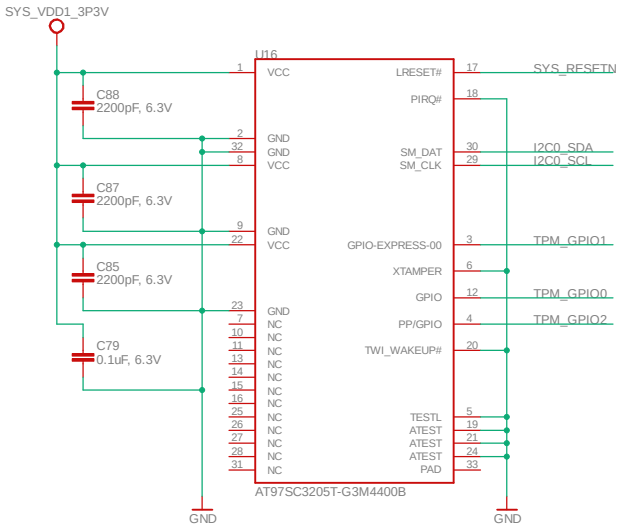
- http://processors.wiki.ti.com/index.php/JTAG_Connectors
- http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 5/15	Rev 0

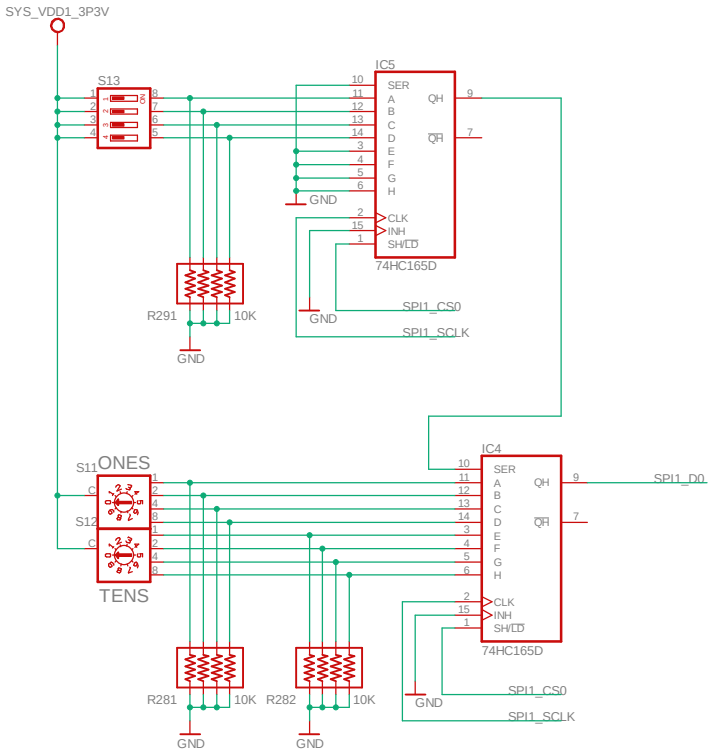
External Real Time Clk



TPM

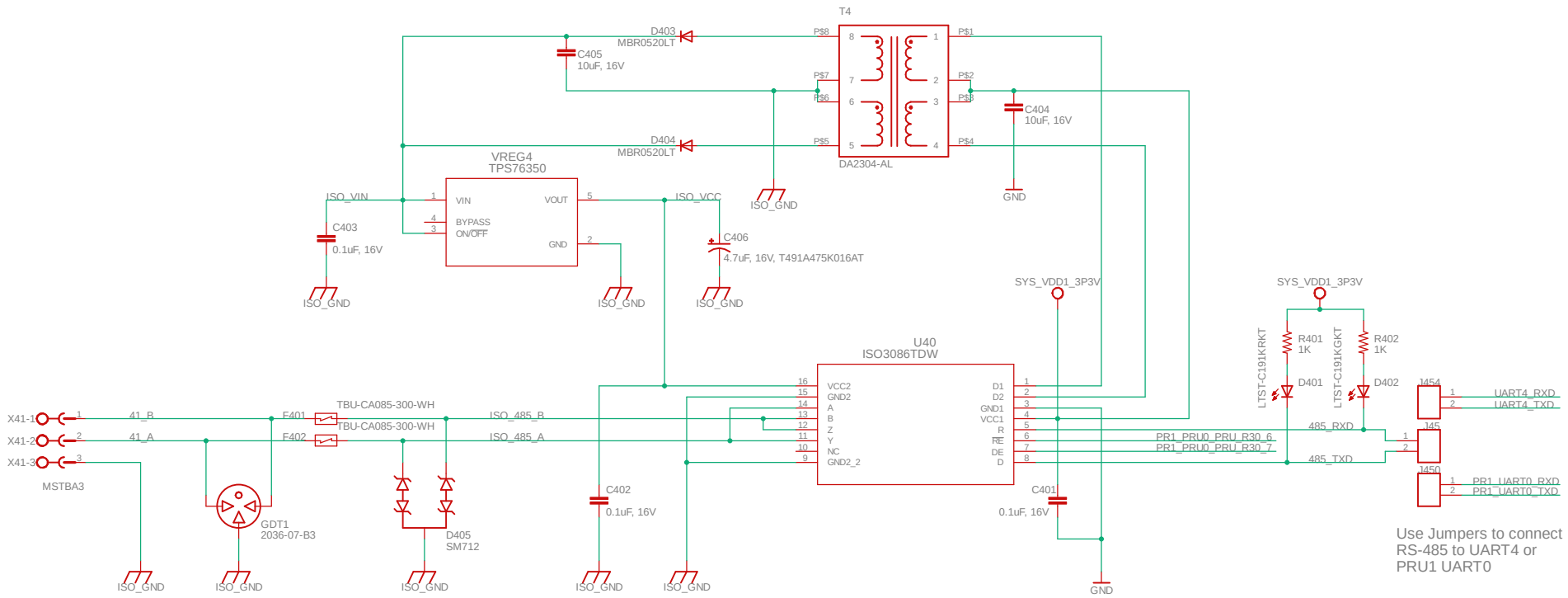


User Config Switches



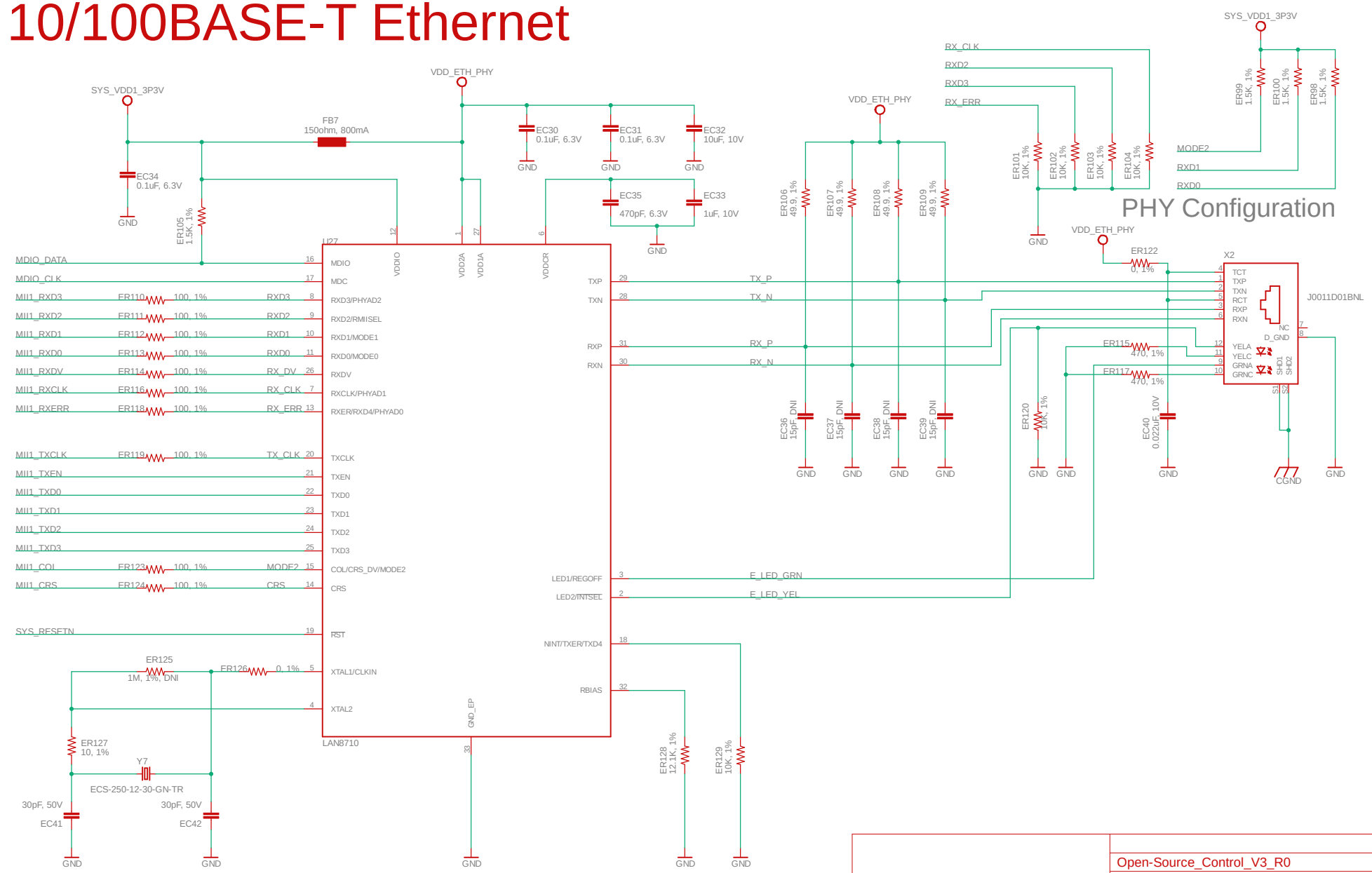
Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 6/15	Rev 0

Isolated RS-485 Interface



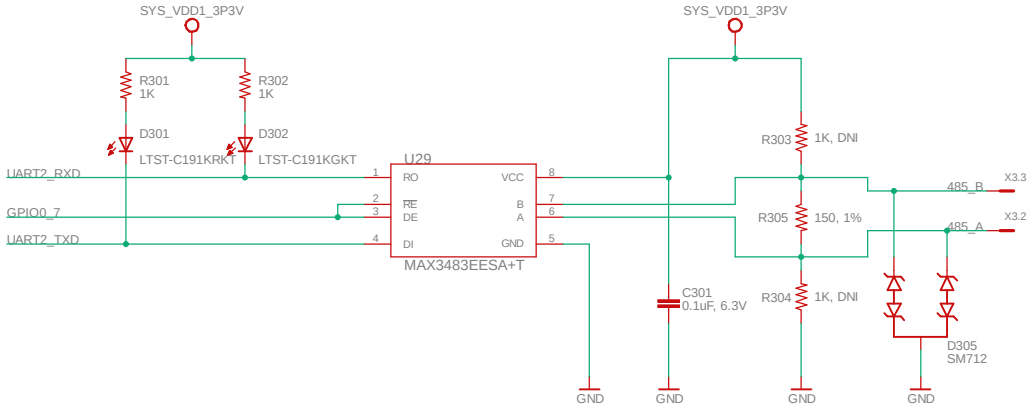
Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 7/15	Rev 0

10/100BASE-T Ethernet

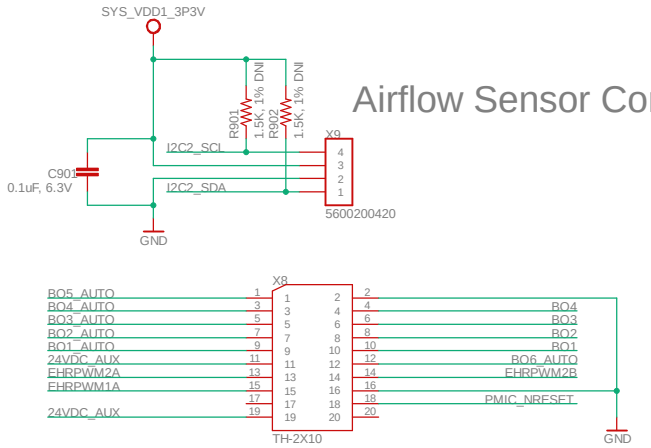


Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 8/15	Rev 0

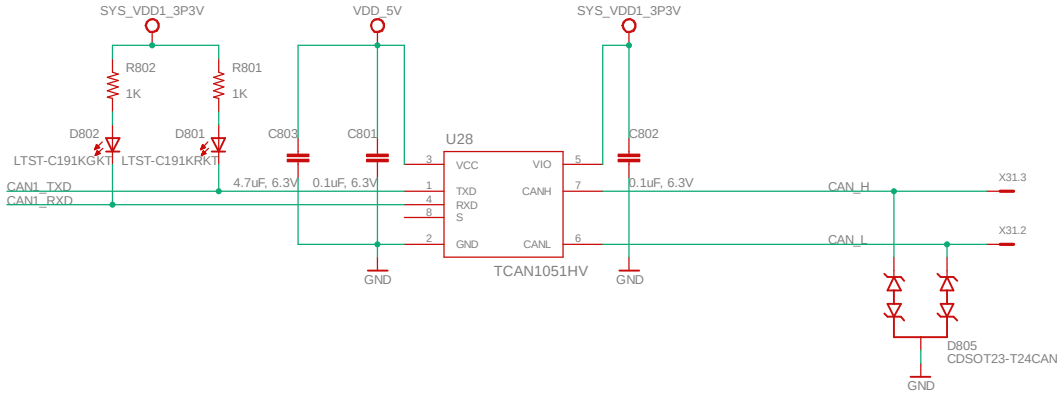
Local Network RS-485



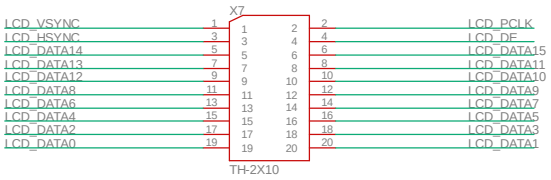
Modular IO Connections



CAN Interface

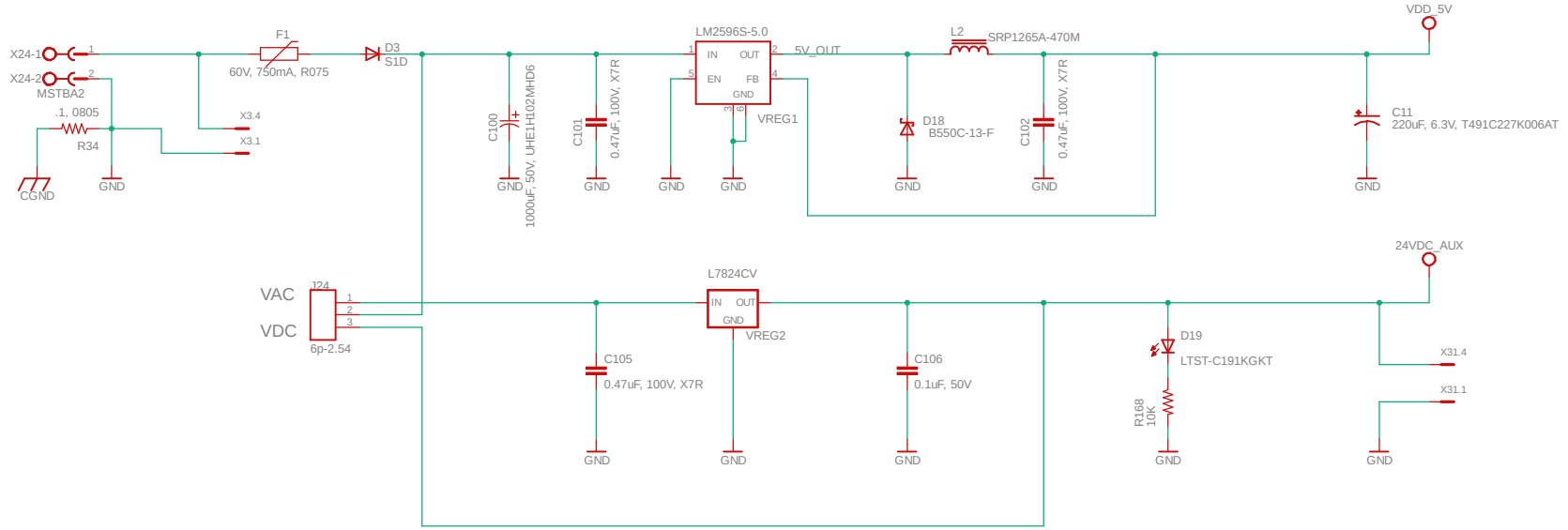


LCD Header



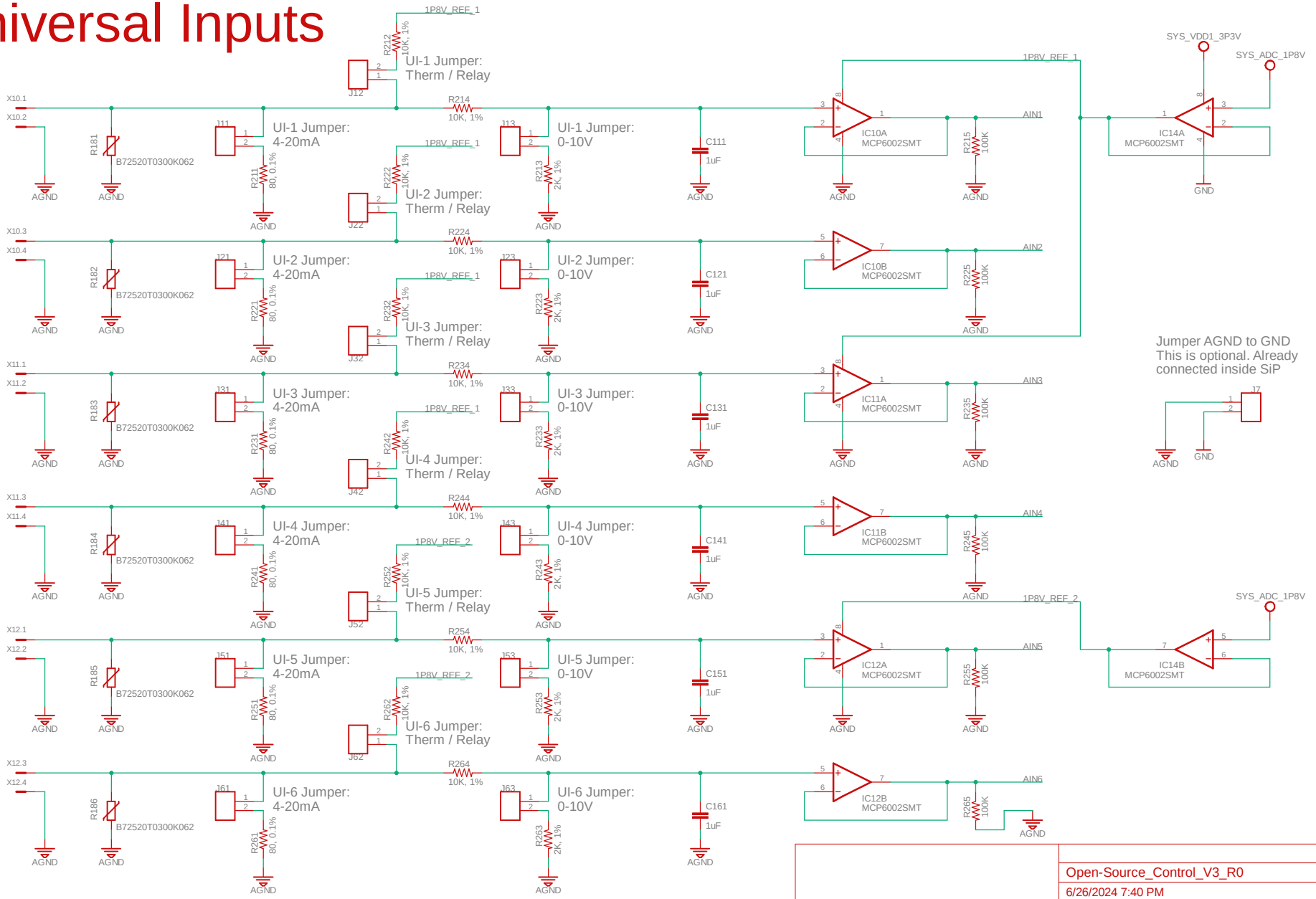
Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 9/15	Rev 0

Power Supply

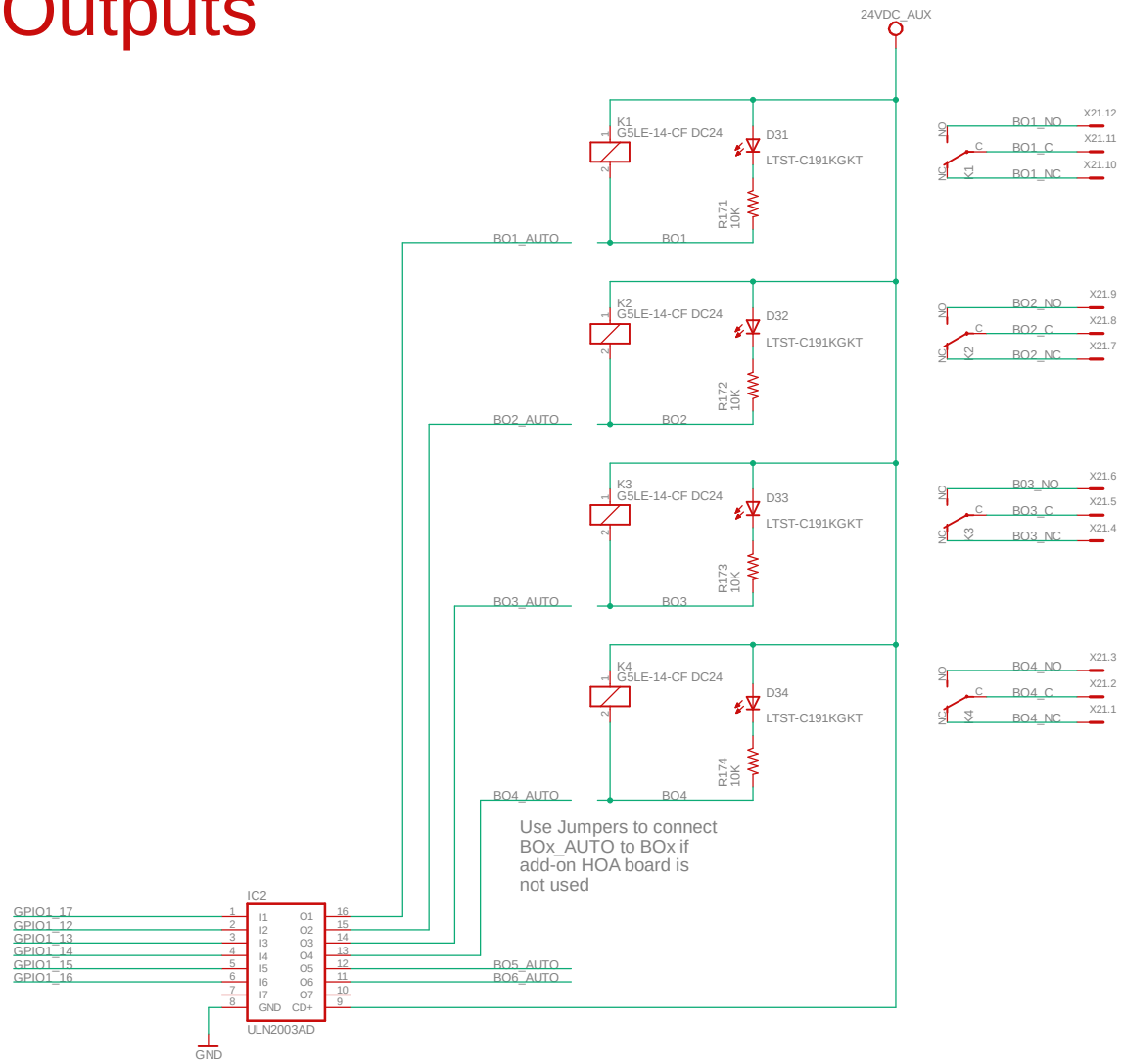


Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 10/15	Rev 0

Universal Inputs



Relay Outputs



Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 12/15	Rev 0

A							A
B							B
C							C
D							D
E							E

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 13/15	Rev 2

Open-Source_Control_V3_R0	
6/26/2024 7:40 PM	
Sheet: 14/15	Rev 0

Notes

Rev 0:
1) New Modular Design

	Open-Source_Control_V3_R0
	6/26/2024 7:40 PM
	Sheet: 15/15 Rev 0