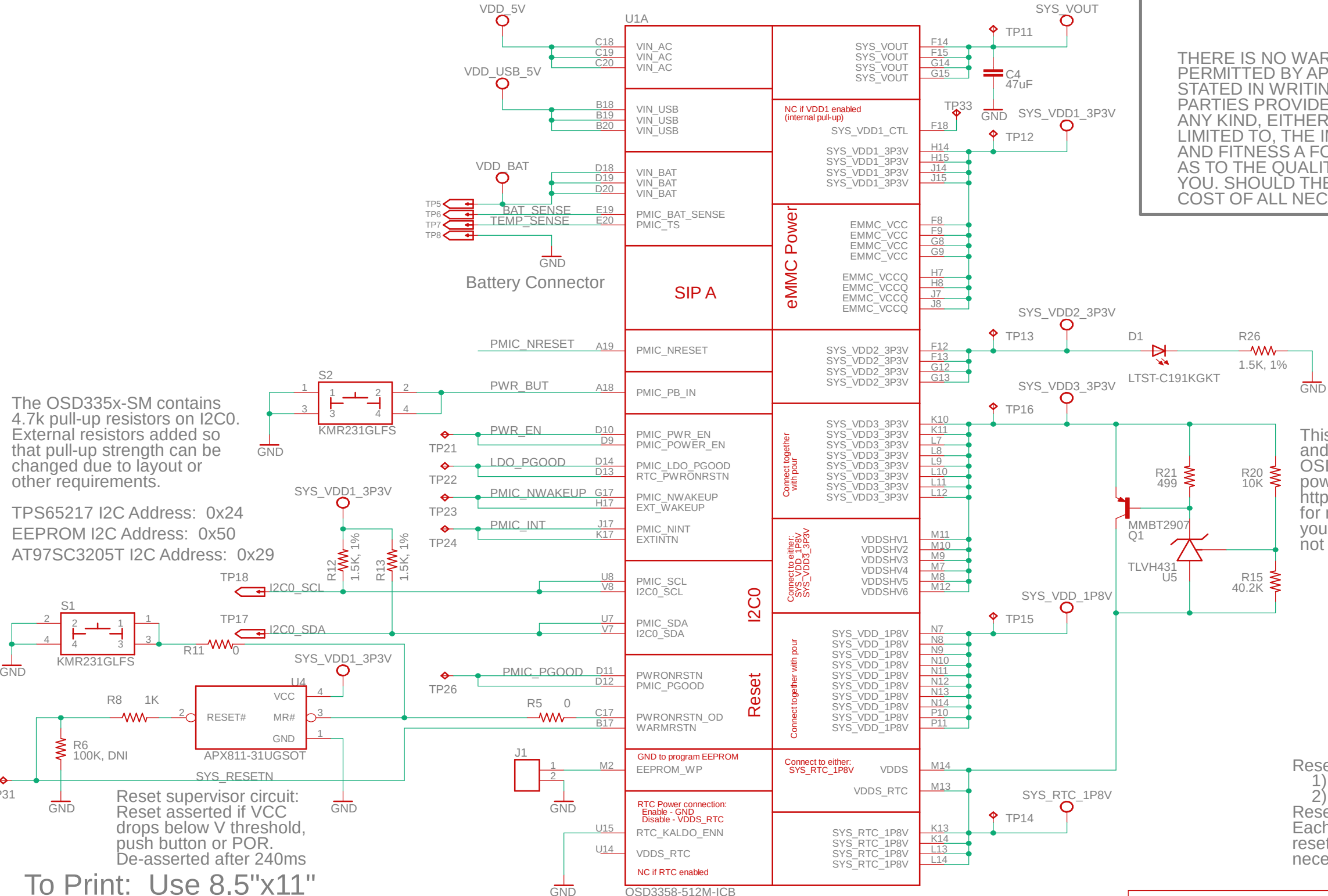
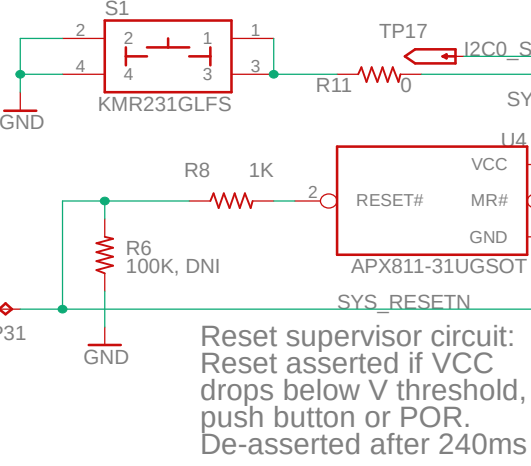


Power & Reset

The OSD335x-SM contains 4.7k pull-up resistors on I2C0. External resistors added so that pull-up strength can be changed due to layout or other requirements.

TPS65217 I2C Address: 0x24
EEPROM I2C Address: 0x50
AT97SC3205T I2C Address: 0x29



THERE IS NO WARRANTY FOR THIS DESIGN, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN *AS IS* WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS A FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN IS WITH YOU. SHOULD THE DESIGN PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.

This is a clamping circuit between the VDDS and VDDSHV inputs of the AM335x inside the OSD335x-SM. The clamping circuit is related to power down issues (see <https://octavosystems.com/osd335x/clamping/> for more information). This may not be needed in your application if the power down conditions do not apply to your application.

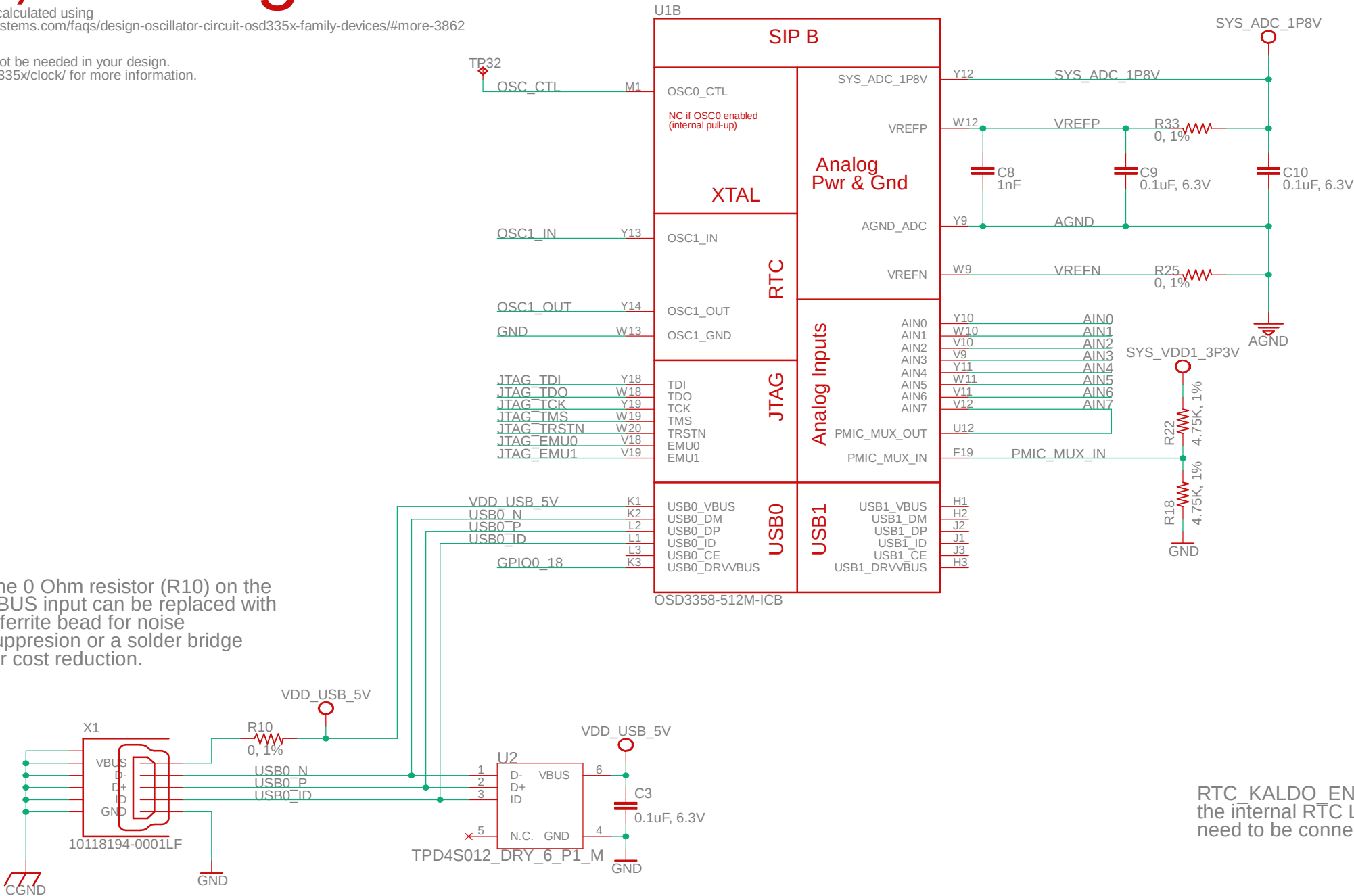
Reset inputs:
1) Manual push-button
2) PMIC_PG00D
Reset supervisor MR# has internal pull up to SYS_VDD1_3P3V. Each reset input is effectively open drain and can only pull reset line low. Resistors added only for debug and are not necessary.

Clocks, Analog & USB

The values for C7 and C12 can be calculated using information in FAQ: <https://octavosystems.com/faqs/design-oscillator-circuit-osd335x-family-devices/#more-3862>

Clock resistors R32 and R24 may not be needed in your design. See <https://octavosystems.com/osd335x/clock/> for more information.

The 0 Ohm resistor (R10) on the VBUS input can be replaced with a ferrite bead for noise suppression or a solder bridge for cost reduction.



If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.

SYS_ADC_1P8V and AGND_ADC are connected to SYS_VDD_1P8V and DGND, respectively, through ferrite beads inside the SiP. It is not necessary to connect these rails to anything else. However, bypass capacitors should be added to reduce noise, if needed for your application.

Maximum voltage for the analog inputs is 1.8V.

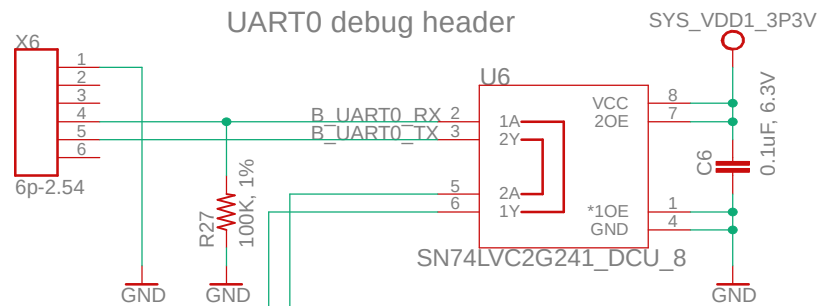
AIN7 currently monitors the PMIC voltages via the internal PMIC mux. See the `Analog Multiplexer' section of the TPS65217 datasheet. For the internal PMIC voltages, there are dividers within the PMIC to keep the monitored voltages under 1.8V. However, PMIC_MUX_IN does not have any dividers and must be less than 1.8V. By default, PMIC_MUX_OUT is Hi-Z. The MUXCTRL register in the PMIC is used to select the PMIC_MUX_OUT voltage path.

SYS_VDD1_3P3V is a 3.3V output of the OSD3358-512M-ICB. A divide by 2 resistor divider is used to ensure that the PMIC_MUX_IN voltage does not exceed 1.8V. It is not necessary to monitor the TL5209 LDO output and this can be removed if desired.

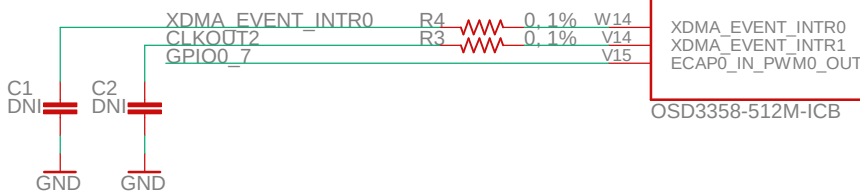
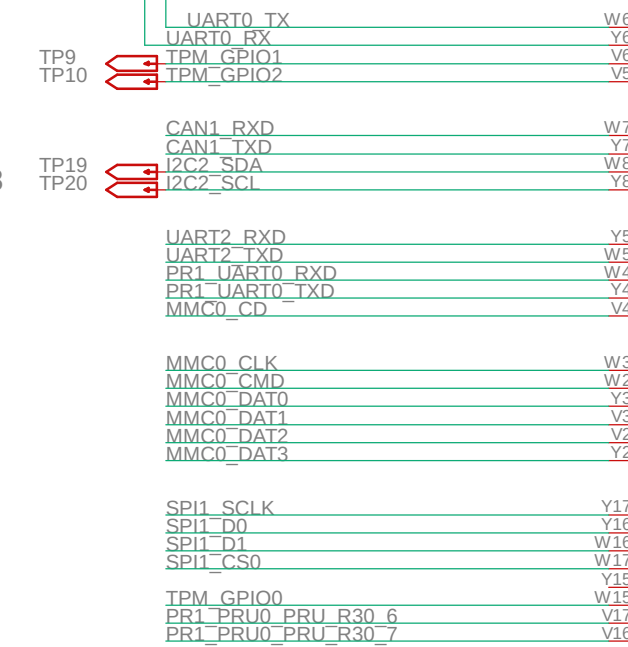
RTC_KALDO_ENN is grounded thru a 10K ohm resistor so that the internal RTC LDO is enabled and CAP_VDD_RTC does not need to be connected to VDD_CORE.

USB Client

SiP Interfaces

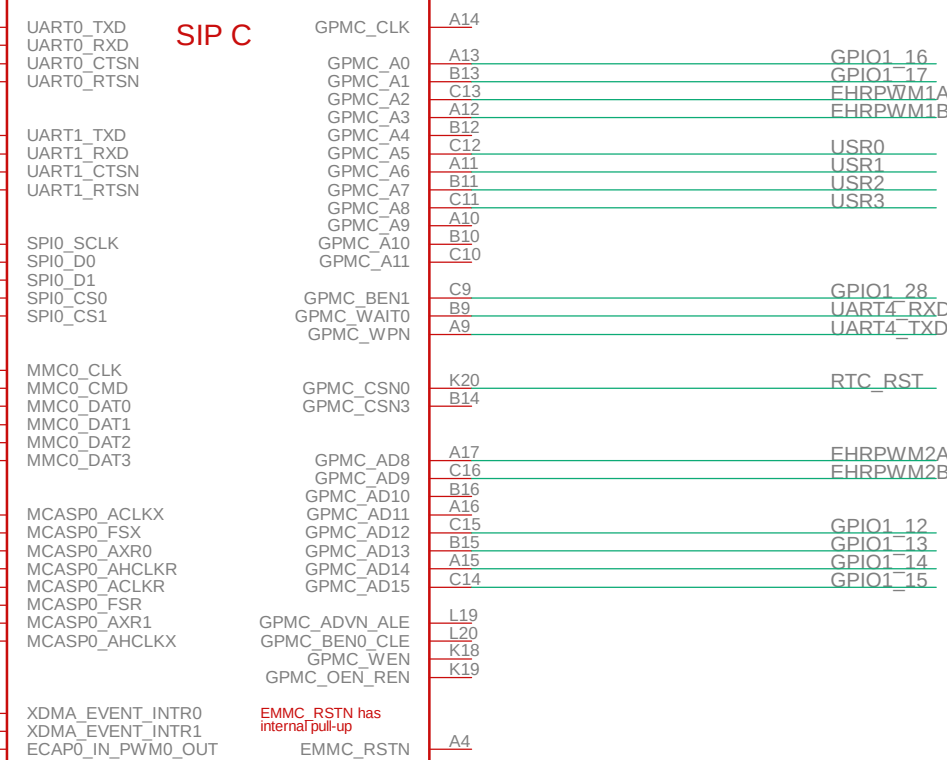


DS3231 I2C Address: 0x68



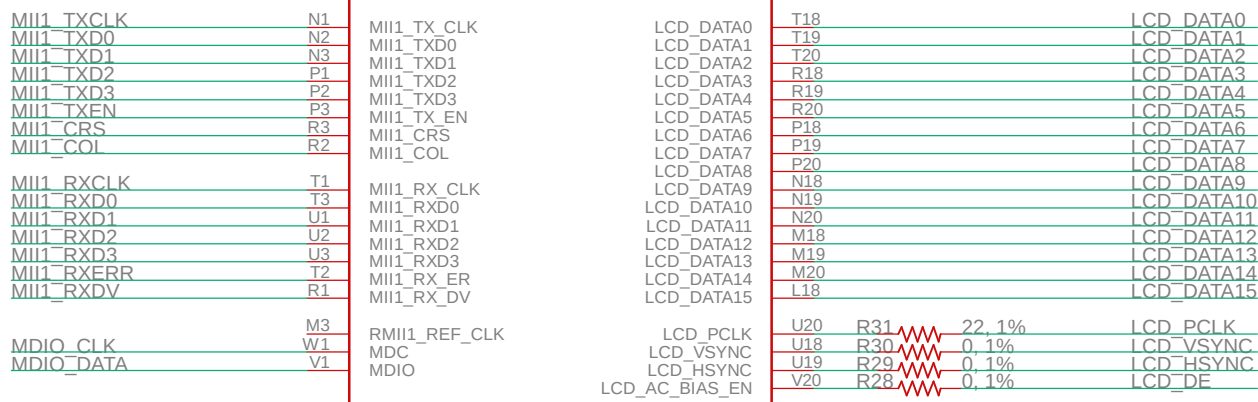
U1C

SIP C



OSD3358-512M-ICB

U1D



SIP D

OSD3358-512M-ICB

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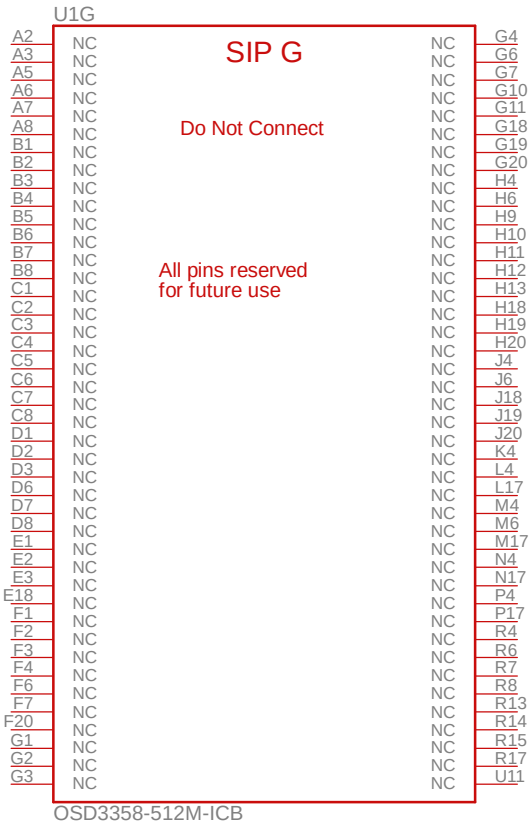
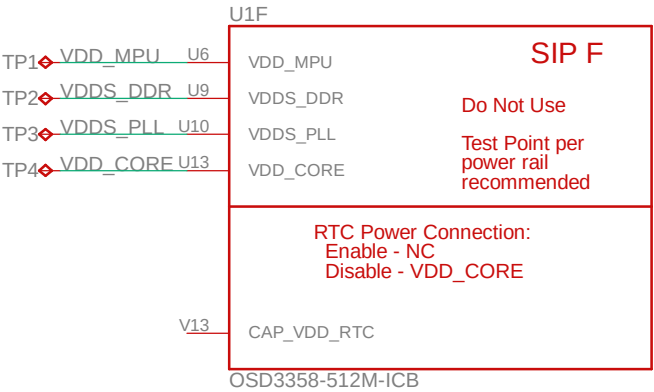
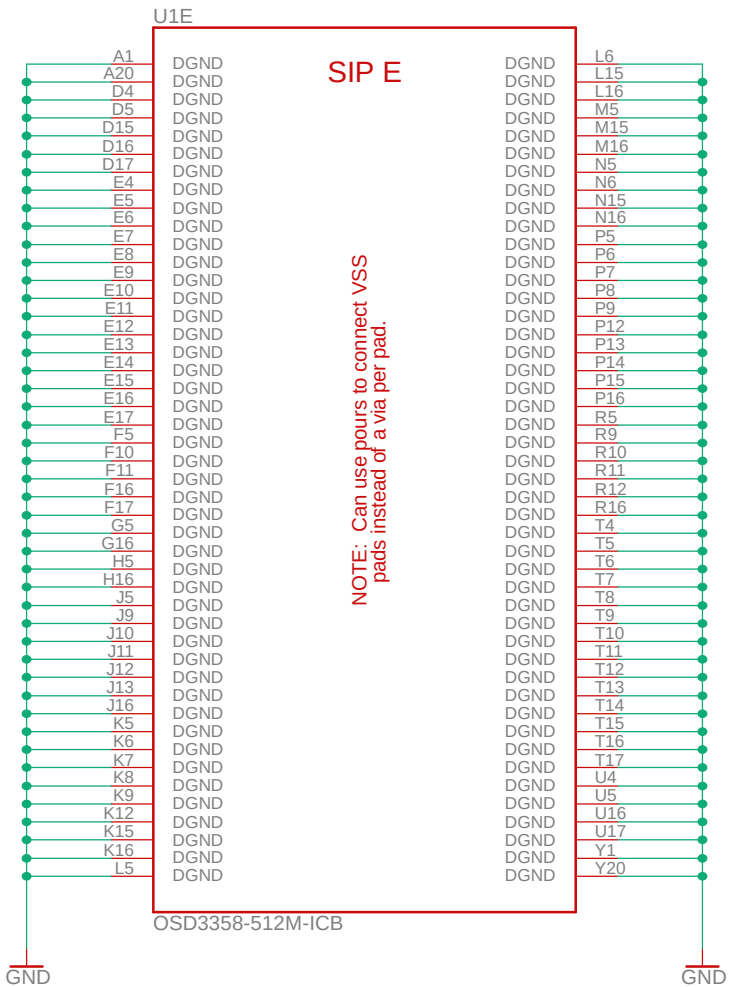
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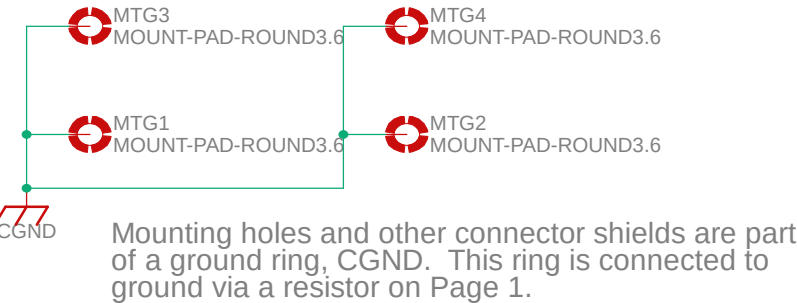
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SiP GND & Misc



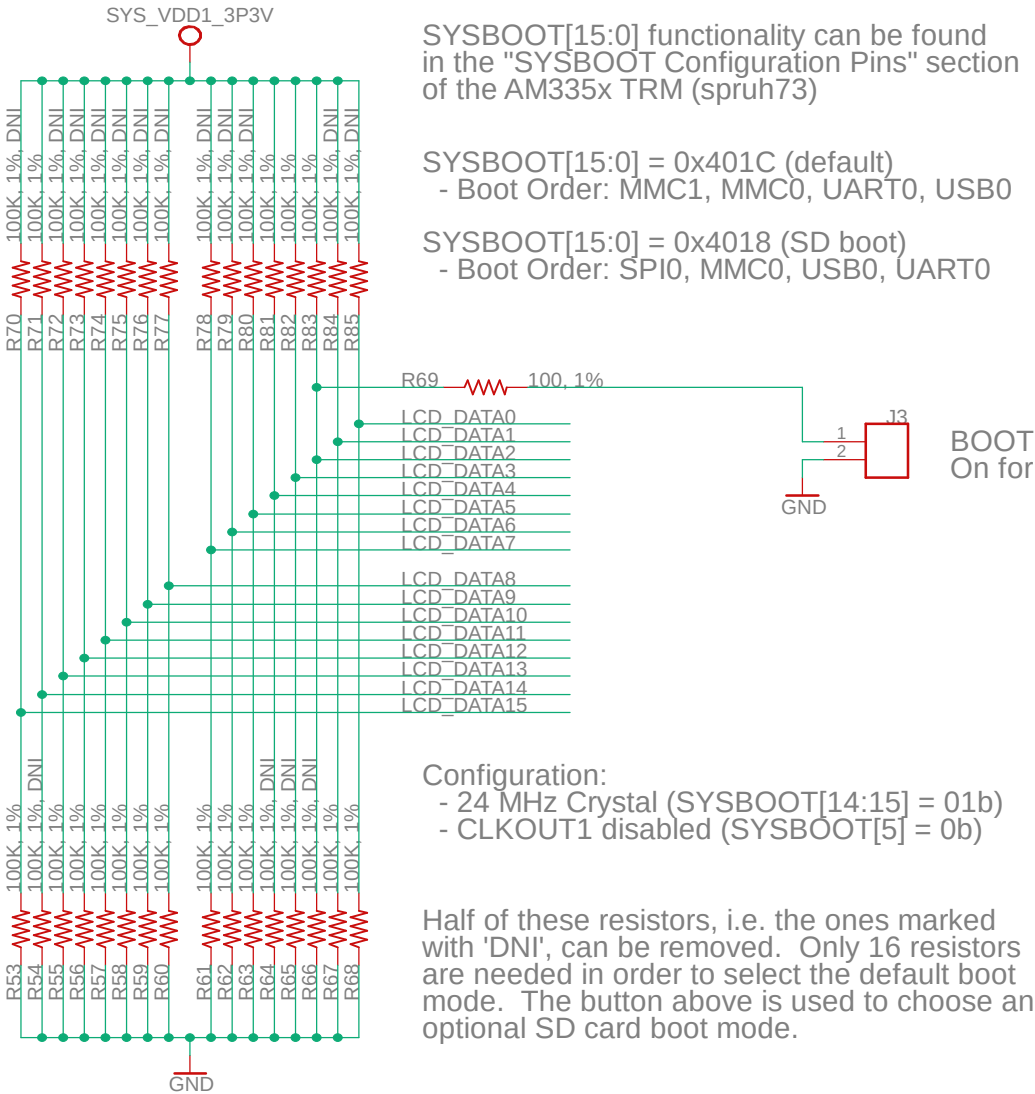
Mounting Holes



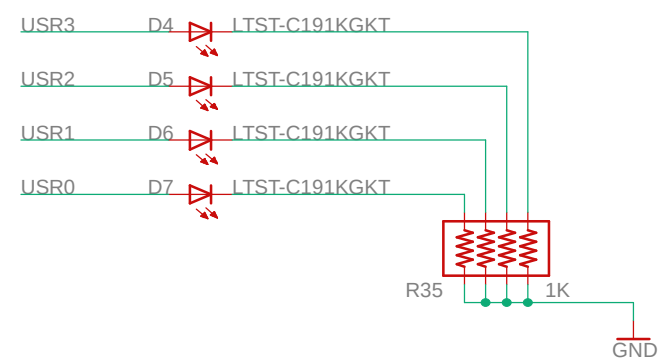
Fiducials



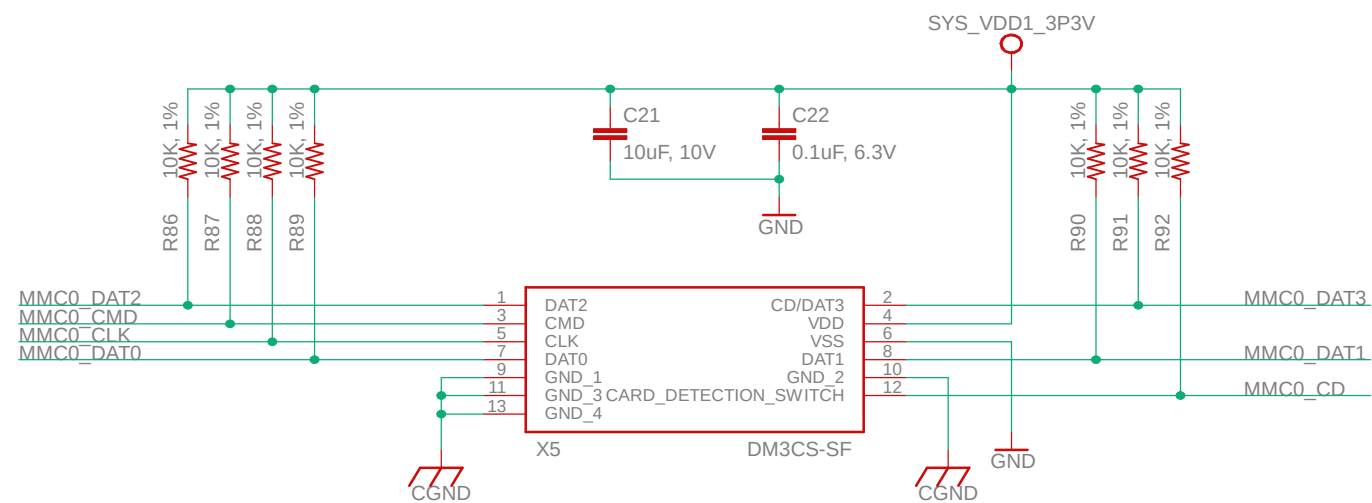
Boot configuration



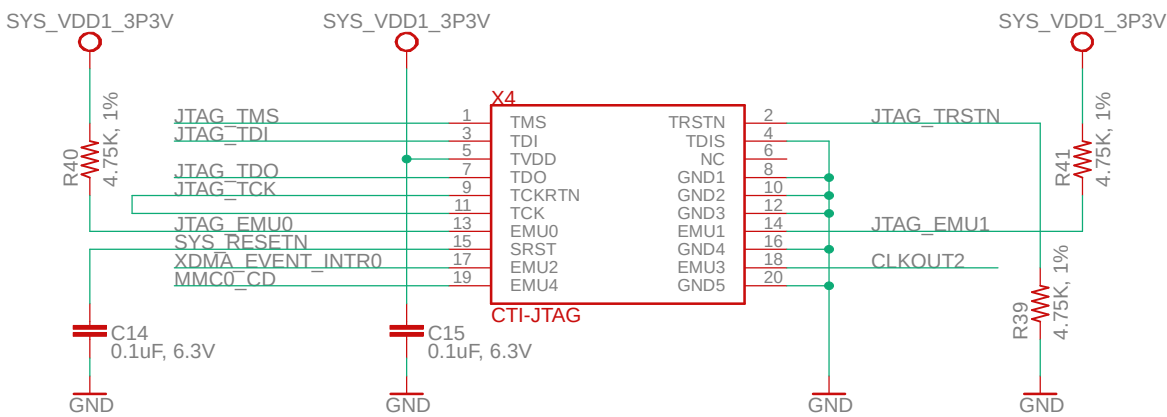
User LEDs



Micro SD card slot



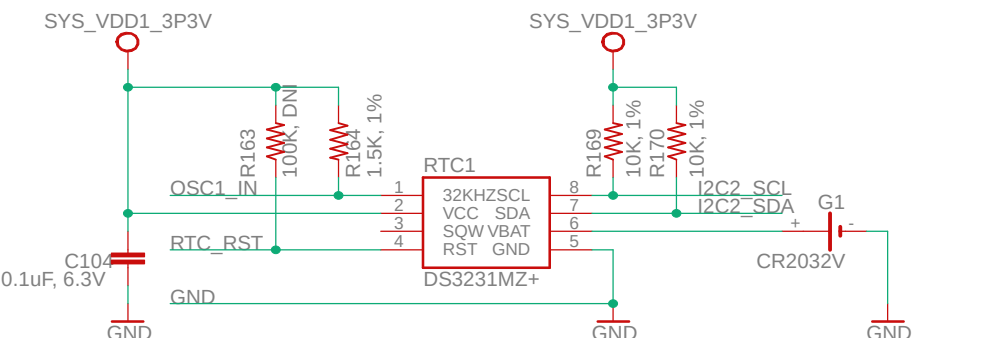
JTAG Header



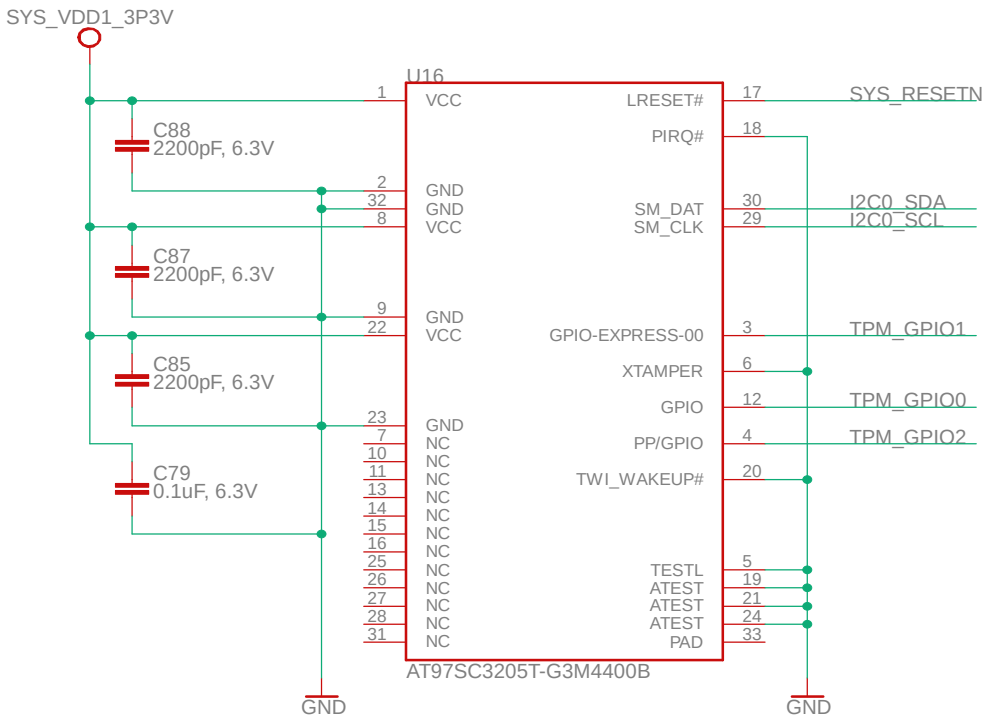
Only connect EMU2, EMU3 and EMU4 if you plan to use advanced JTAG features (HS-RTDX, Core Trace, System Trace, etc) of higher end debuggers:

- http://processors.wiki.ti.com/index.php/JTAG_Connectors
- http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide

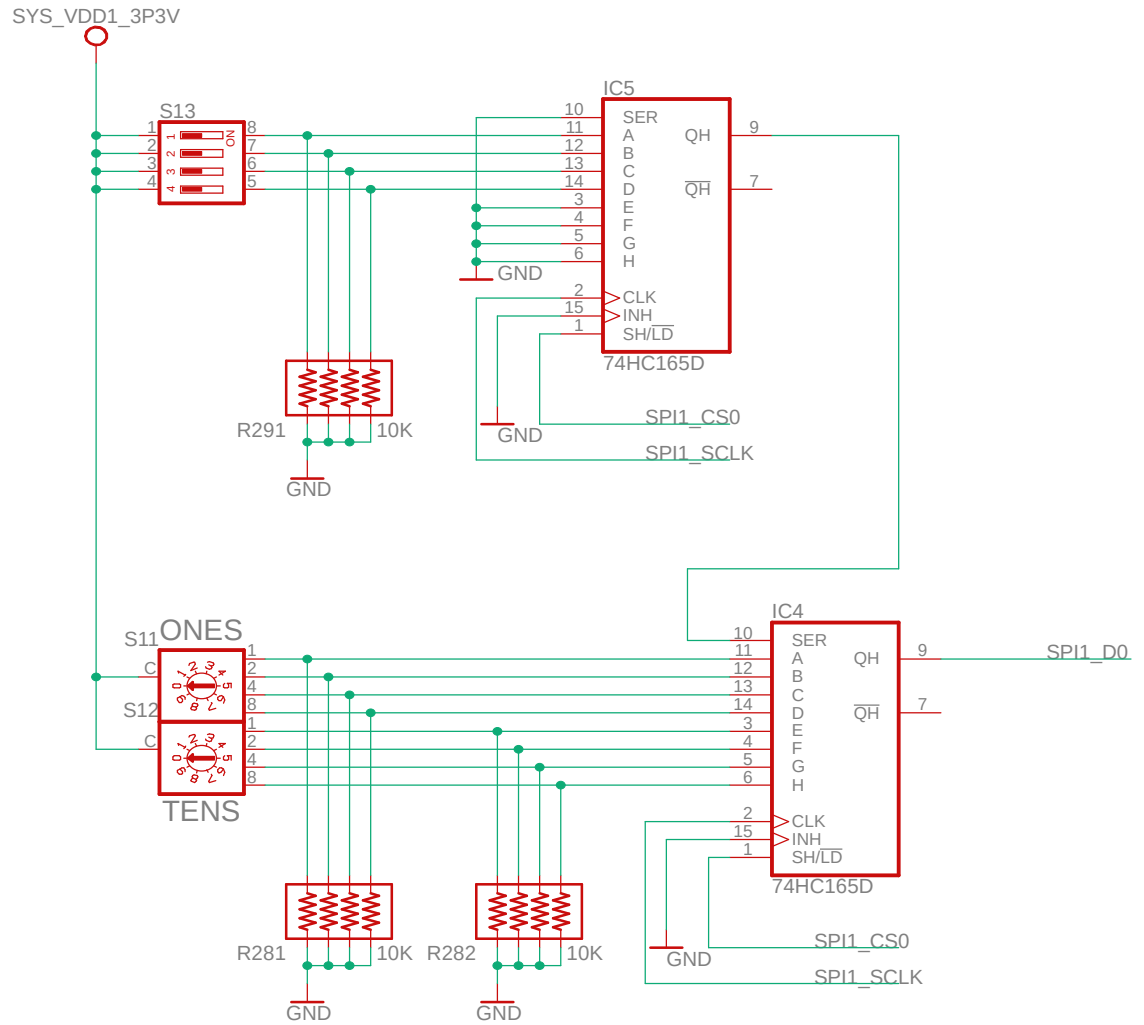
External Real Time Clk



TPM



User Config Switches



This diagram illustrates an isolated RS-485 interface circuit, designed to connect a microcontroller (PRU1) to an RS-485 network through a transformer-based isolation stage.

Key Components and Connections:

- Power Regulation:** The circuit uses a VREG4 (TPS76350) voltage regulator to provide a clean, regulated supply (ISO_VCC) for the isolation stage. The regulator is powered by ISO_VIN and includes a bypass capacitor (C403) and a feedback capacitor (C406).
- Isolation Transformer:** A transformer (T4, DA2304-AL) provides galvanic isolation between the microcontroller's ground and the RS-485 network ground. The primary is connected to the microcontroller's ground, and the secondary is connected to the RS-485 network ground.
- RS-485 Interface:** The ISO3086TDW (U40) is a high-speed, low-power RS-485 transceiver. It is connected to the microcontroller's PRU1 UART0 pins (PR1_PRU0_PRU_R30_6 for RXD and PR1_PRU0_PRU_R30_7 for TXD) and the RS-485 network (485_RXD and 485_TXD). The transceiver is powered by ISO_VCC and ISO_GND.
- Signal Conditioning:** The RS-485 signals are conditioned by a network of resistors (R401, R402) and capacitors (C401, C402) to ensure proper signal levels and timing.
- Protection:** The circuit includes protection diodes (D401, D402) and a gas discharge tube (GDT1) to protect the microcontroller and the RS-485 network from transient voltages.
- Connectors:** The circuit is connected to the microcontroller via a 4-pin header (X41-1, X41-2, X41-3, X41-4) and to the RS-485 network via a 2-pin header (J454, J455).

Notes:

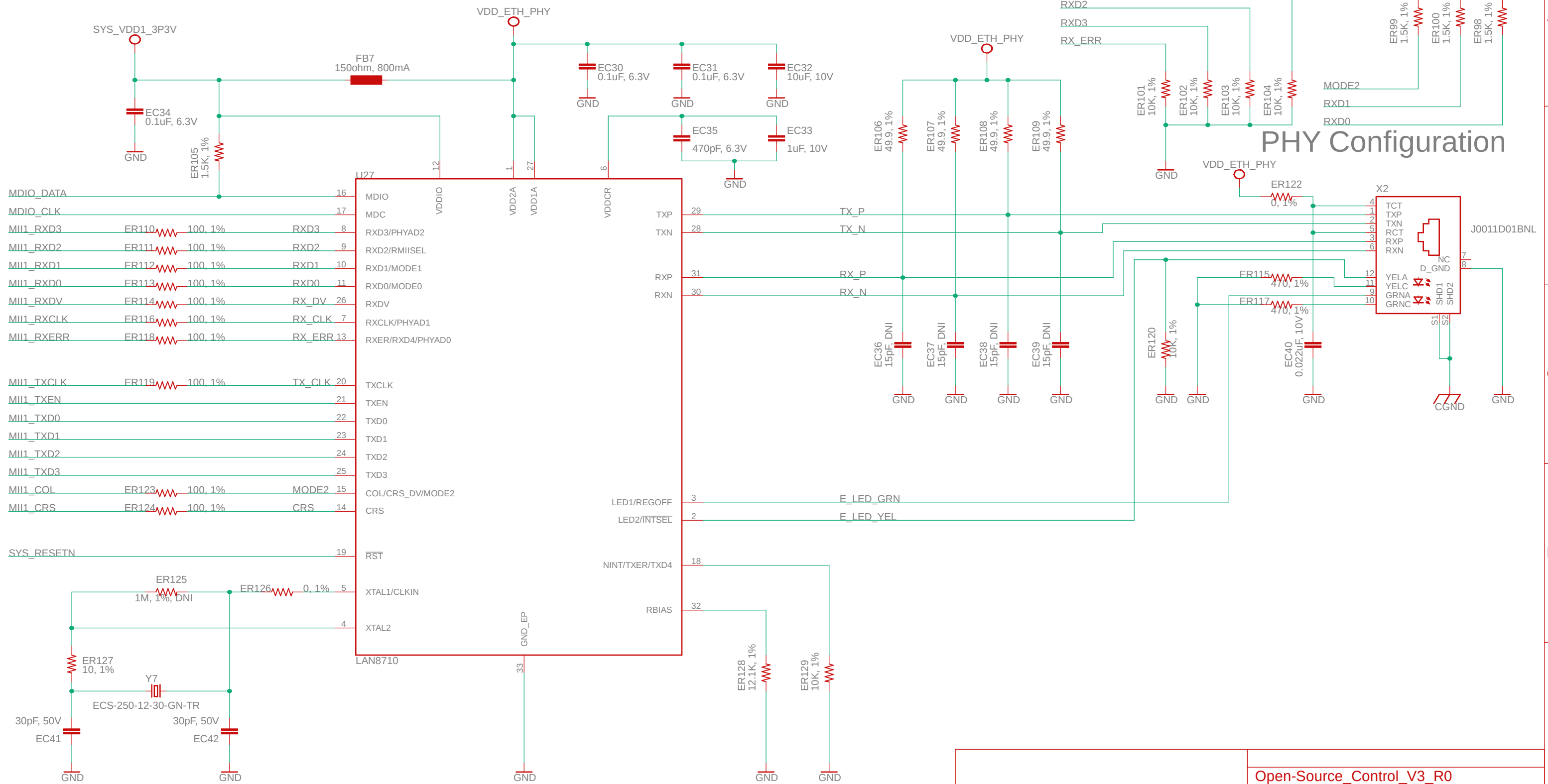
- Use Jumper to connect RS-485 to UART4 or PRU1 UART0
- Use Jumper to connect RS-485 to UART4 or PRU1 UART0

Legend:

- ISO_VIN: Isolated Supply Input
- ISO_VCC: Isolated Supply Output
- ISO_GND: Isolated Ground
- 485_RXD: RS-485 Receive Data
- 485_TXD: RS-485 Transmit Data
- UART4_RXD: UART4 Receive Data
- UART4_TXD: UART4 Transmit Data
- PR1_UART0_RXD: PRU1 UART0 Receive Data
- PR1_UART0_TXD: PRU1 UART0 Transmit Data

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10/100BASE-T Ethernet



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A



C



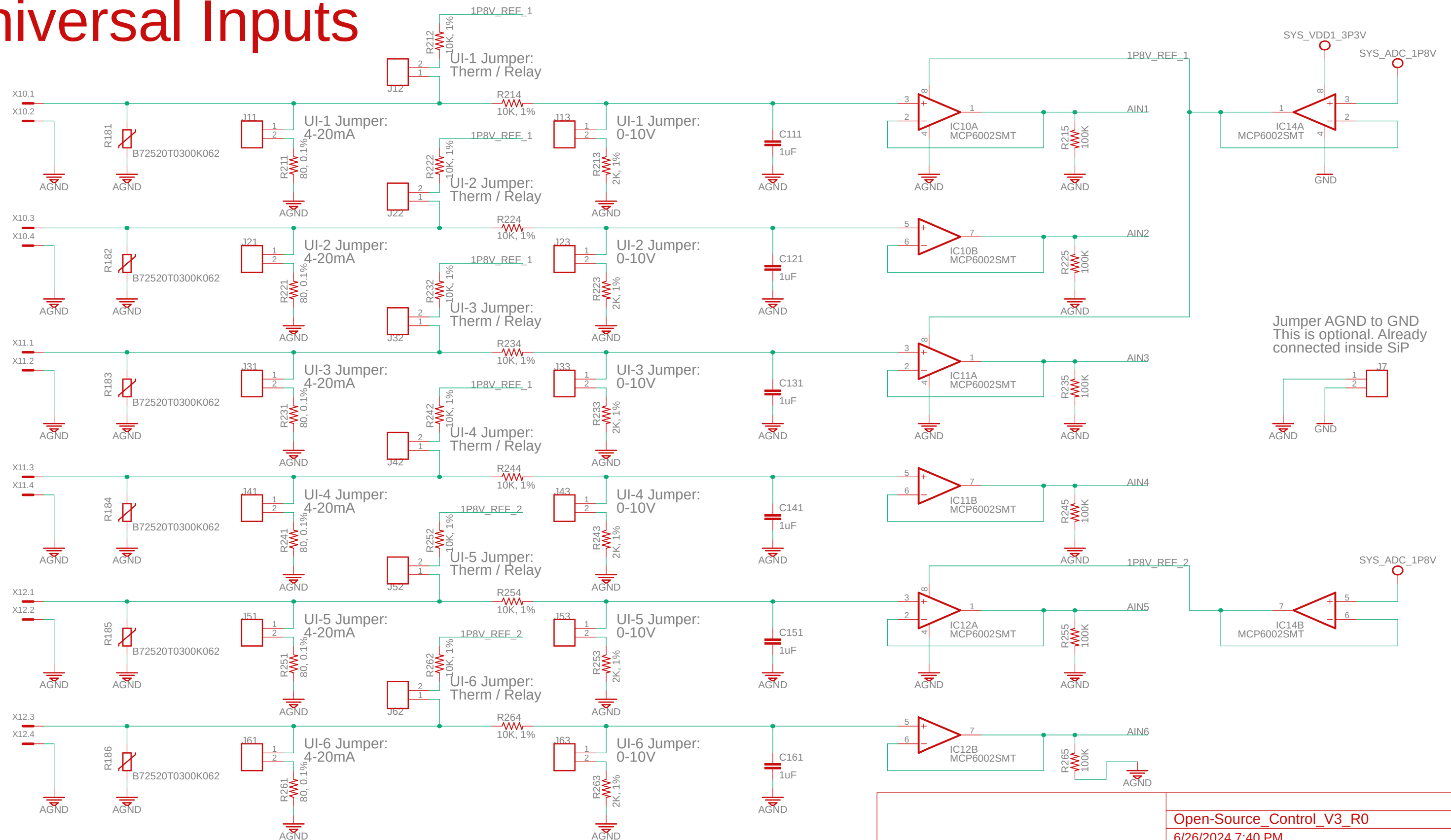
①



A

E

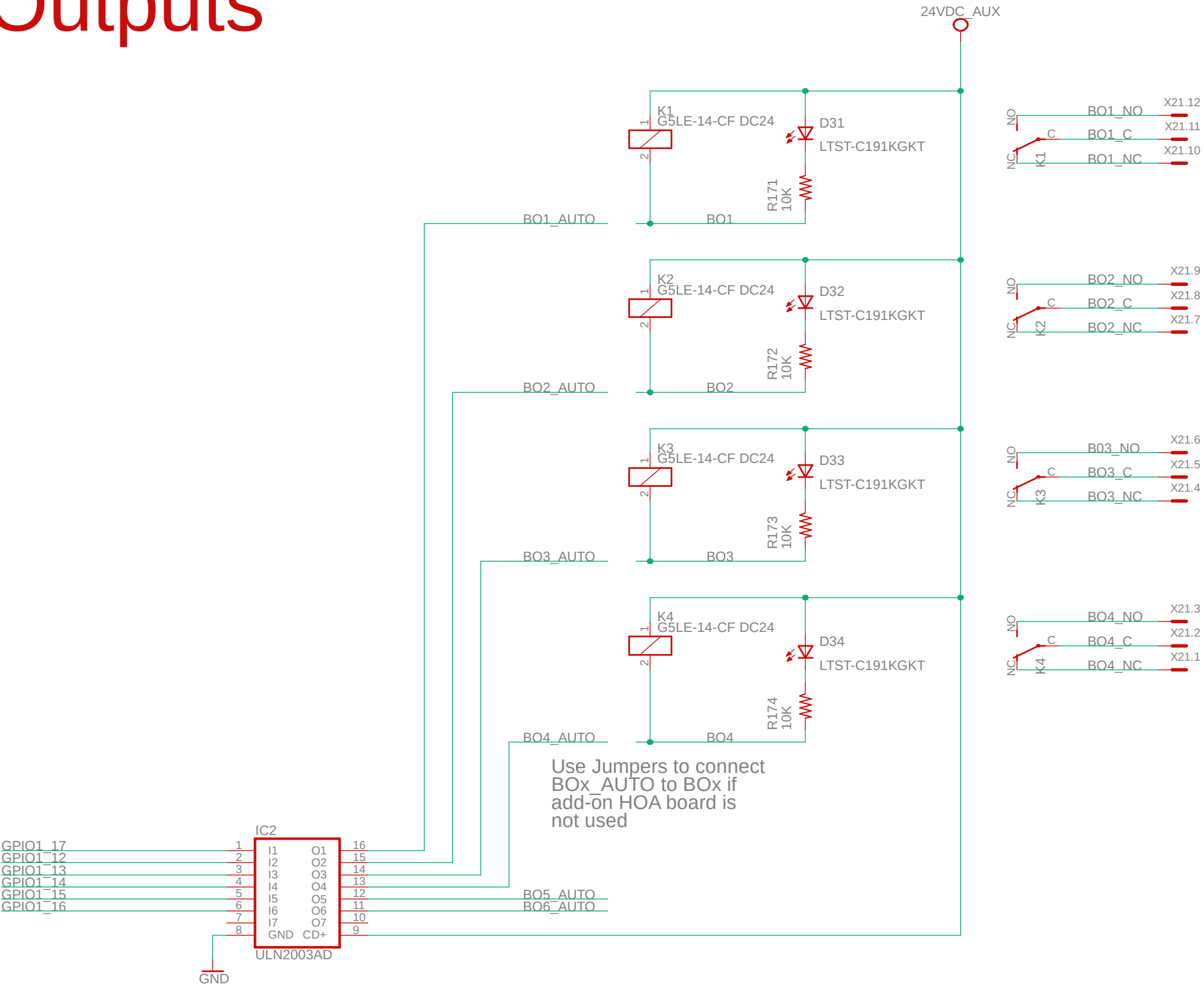
Universal Inputs



Jumper AGND to GND
This is optional. Already
connected inside SiP

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Relay Outputs



1	2	3	4	5	6	7	8									
A								A								
B								B								
C								C								
D								D								
E							<div>Open-Source_Control_V3_R0</div> <div>6/26/2024 7:40 PM</div> <div>Sheet: 14/15 Rev 0</div>		E							
1	2	3	4	5	6	7	8									

Notes

Rev 0:
1) New Modular Design

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