DVI - Digital Visual Interface

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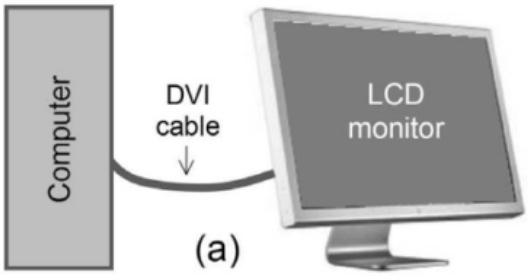
Tags: #VHDL

Links:

- SEM4_PROJECT
- Zynq-7000, VHDL and Vivado
- VGA - Video Graphic Array



(b)

Name	Resolution	Ratio	Clock (MHz)
SVGA	800 x 600	4:3	40
WXGA	1280 x 720	16:9	61 (*)
HD+	1600 x 900	16:9	95 (*)
Full HD	1920 x 1080	16:9	137 (*)
WUXGA	1920 x 1200	16:10	152 (*)
(*) Estimate, at 60 Hz and just 10% blanking overhead			

Figure J.1
(a) DVI cable between computer and LCD monitor; (b) Examples of monitor resolutions.

DVI Architecture and Connector

Consists of three blocks:

- **Transition Minimized differential signaling (TMDS)** transmitter or receiver.
- **Data Channel (DDC)** - through which the computer reads the displays features *(supported resolutions, timings and so on)*, stored in the ROM with EDID format. Uses I2C protocol.
- Generator for VGA - Video Graphic Array signals, is optional to maintain the compatibility with analog VGA monitors.

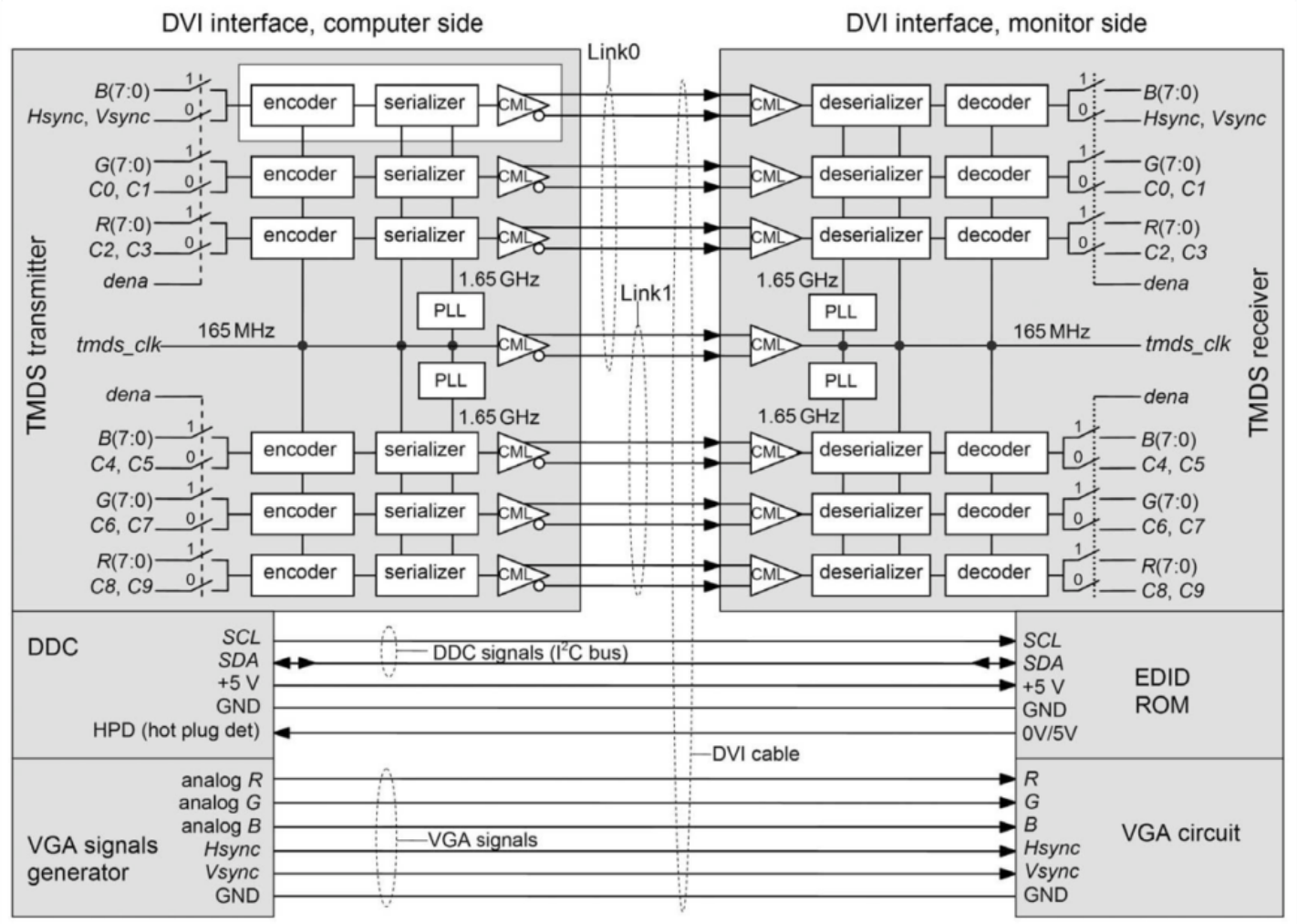


Figure J.2

DVI circuit at the two ends of the DVI cable. A complete DVI connector (figure J.3) has 29 pins, corresponding to the 25 wires above plus 4 grounded shields.

The **TMDS** (TMDS)transceiver can contain one or two links, each consisting of three **TMDS** channels *(see white box in diagram)*, which alternately *pixel data (R, G, B with 8 bits each)* or *control* data *(2 bits per channel, with Hsynch and Vsync in the first channel and up to five pairs of reserved control bits, C0 - C1 ..C8 - C9, in the other channels)*. Pixel data is transmitted when *dena (display enable)* is high.

The bit rate is independent from the type of data *(pixel or control)* being transmitted because 10 bits are produced by the **TMDS** encoder. When operating at full speed *(165 Mpps for single link or 330 Mpps for duel link)*, a bit rate of 1.65 Gbps is needed through the wires of the DVI cable. To operate at such high frequency, the frequency of the system clock usually needs to be increased, which is done with PLLs

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	*tmds2–* (digital *R*)	9	*tmds1–* (digital *G*)	17	*tmds0–* (digital *B*)	C1	Analog *R*
2	*tmds2+* (digital *R*)	10	*tmds1+* (digital *G*)	18	*tmds0+* (digital *B*)	C2	Analog *G*
3	Shield for *tmds2/4*	11	Shield *tmds1/3*	19	Shield *tmds0/5*	C3	Analog *B*
4	*tmds4–* (digital *G*)	12	*tmds3–* (digital *B*)	20	*tmds5–* (digital *R*)	C4	*Hsync* (for VGA)
5	*tmds4+* (digital *G*)	13	*tmds3+* (digital *B*)	21	*tmds5+* (digital *R*)	C5	GND for *R*, *G*, *B*
6	*SCL* (DDC clock)	14	+5V for DDC	22	Shield for *tmds_clk*	--	--
7	*SDA* (DDC data)	15	GND for DDC	23	*tmds_clk+*	--	--
8	*Vsync* (for VGA)	16	HPD (Hot Plug Det.)	24	*tmds_clk–*	--	--

Figure J.3
DVI connector (check corresponding signals in figure J.2).

Connector

- Three pairs of wires, called *tmds0 (pins 18 - 17, signal B)*, *tmds1 (pins 10 - 9, signal G)* and *tmds2 (pins 2 - 1, signal R)*, to transmit RGB in link 0.
- Three pairs of wires, called *tmds3 (pins 13 - 12, signal B)*, *tmds4 (pins 5 - 4, signal G)* and *tmds5 (pins 21 - 20, signal R)*, to transmit RGB in link 1.
- One pair of wire called *tmds_clk (pins 23 - 24)*, for transmitting the DVI clock.
- Each of the 7 pairs of wires has a shielding cover and is connected to pins 3, 11, 19 or 22.
- Two DDC wires *(pins 6 and 7)* for I2C communication with the EDID ROM.
- Pair of wires *(pins 14 and 15)* that feeds the EDID ROM when the monitors is off.
- Has **Hot Plug Detection** *(HPD)* wire *(pin 16)*, which allows the host to know whether there is a device connected to the DVI cable.
- The remaining six wires are for **R, G, B, Hsync and Vsync plus ground for R/G/B**. Used for compatibility with analog-input monitors.