VGA - Video Graphic Array

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Tags: #VHDL
Links:

- SEM4_PROJECT
- Zynq-7000, VHDL and Vivado

Note: Originally developed for CRT (Cathode Ray Tubes) video monitors, later adapted for LCD (Liquid Crystal Displays) monitors, allows for a full digital operation DVI - Digital Visual Interface, however some still support VGA

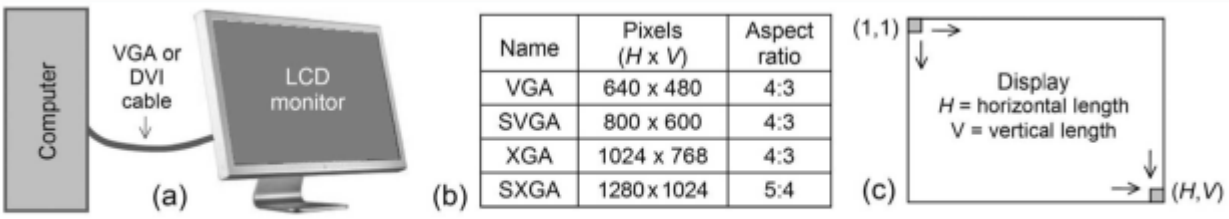


Figure I.1
(a) VGA (analog video) or DVI (digital video) cable; (b) Some members of the VGA family; (c) Pixel count.

VGA interface architecture

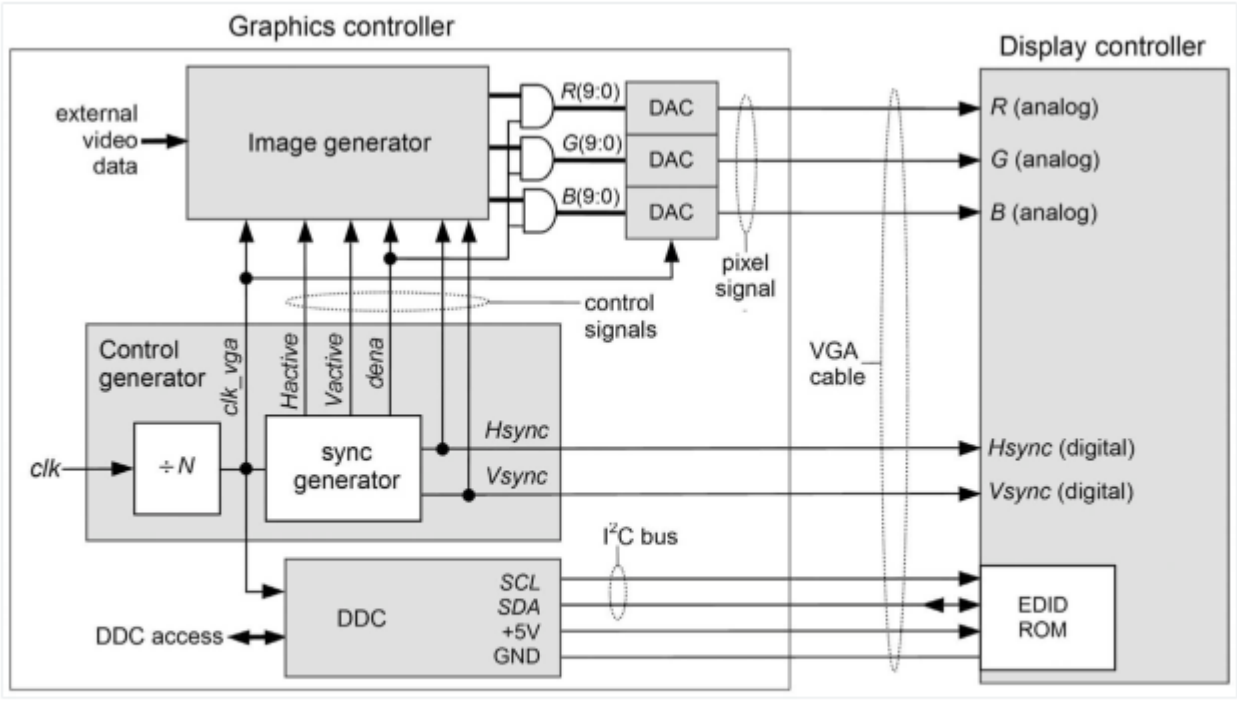


Figure I.2
VGA interface architecture.

- **Image generator** - Produces pixel signals - R, G, B. They get converted to analog voltages between 0V and 0.7V by DACs *(usually with a resolution between 6 and 10 bits)*, before being sent to the monitor.

- **Control signal generator** - Produces the VGA clock *clk_vga*, plus control signals *Hactive* *(horizontal active window)*, *Vactive* *(vertical active window)*, *dena* *(display enable)*, *Hsync* *(horizontal sync)* and *Vsync* *(Vertical sync)*. This block is application-independent *(it depends only on the VGA mode)*, so its design is always the same.

- **DDC (Display Data Channel)** - Allows the computer to read the display's features *(supported resolutions, timings etc.)*, stored in a ROM with extended display identification data **(EDID)** format. The original VGA mode (640 x 480 x 60Hz) is supported by any monitor by default.. Employs I2C protocol. Is also application-independent.

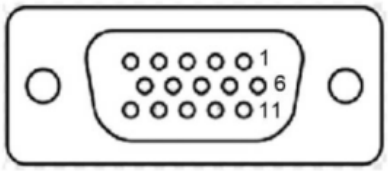
- **Hsync and Vsync** - are responsible for determining when new line or a new frame should start, respectively, with their timings defining the VGA mode. *Hactive* and *Vactive* represent the time intervals during wich an image is actually being drawn on the screen. And *dena* is responsible for tuning the pixel signals off during retrace, so it can simply be obtained by ANDing *Hactive* and *Vactive*. Note only 2 of the 5 signals are transmitted to the monitor.

VGA Connector

There are 5 main signals sent to the monitor:

- pins 1 - 3 transmit the color signals - R, G, B. They are analog voltages between 0V and 0.7V on two parallel 75Ω resistors *(all other signals are digital)*.
- pins 13 and 14 transmit horizontal and vertical sync signals.

VGA male connector
(DB15 male plug)



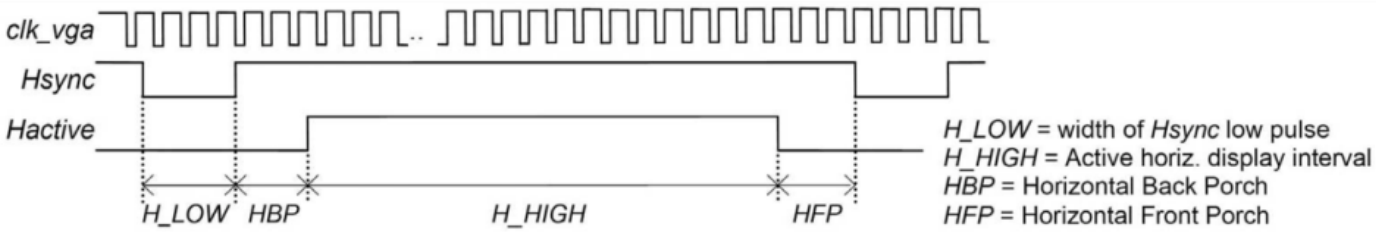
VGA female connector
(DB15 female receptacle)

Pin	Signal	Direction	Simplest setup
1	*R* (analog red, 0V-0.7V on 37.5Ω)	To monitor	Connected (analog)
2	*G* (analog green, 0V-0.7V or 0.3V-1V on 37.5Ω)	To monitor	Connected (analog)
3	*B* (analog blue, 0V-0.7V on 37.5Ω)	To monitor	Connected (analog)
4	ID2	From monitor	N/C
5	GND (general and for +5V)	To monitor	GND
6	GND for *R*	To monitor	GND
7	GND for *G*	To monitor	GND
8	GND for *B*	To monitor	GND
9	No pin or +5V (optional)	To monitor	N/C
10	GND for *Hsync* and *Vsync*	To monitor	GND
11	ID0	From monitor	N/C
12	*SDA* (for I^2C interface)	Bidirectional	N/C
13	*Hsync* (horizontal sync, 0V/5V waveform)	To monitor	Connected (digital)
14	*Vsync* (vertical sync, 0V/5V waveform)	To monitor	Connected (digital)
15	*SCL* (for I^2C interface)	To monitor	N/C

Figure I.3
VGA connector.

- **H_LOW** - width of the horizontal synchronization pulse.
- **HBP** - horizontal back porch.
- **H_HIGH** - active line display interval.
- **HFP** - horizontal front porch.

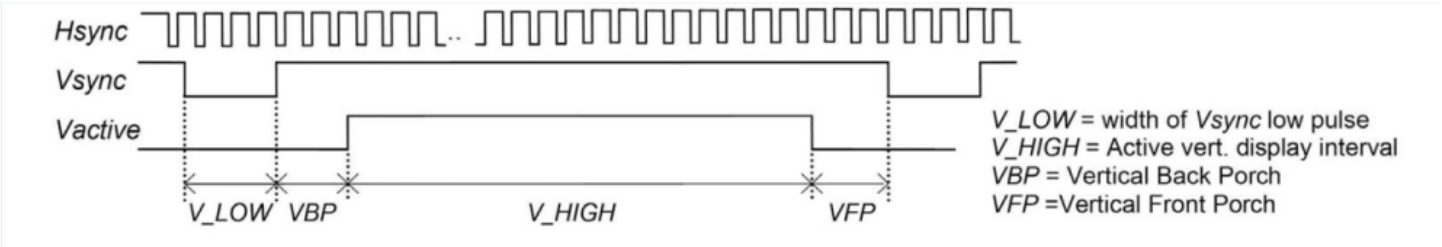
Note: All are measured in number of pixels; i.e. num,ber of clock cycles



VGA mode		Refresh rate (Hz)	Clock (MHz)	Horizontal timing (in clock pulses, same as pixels)				
Name	Resolution (*H* x *V*)			*H_LOW* (pixels)	*HBP* (pixels)	*H_HIGH* (pixels)	*HFP* (pixels)	Total pixels
VGA	640 x 480	60	25	96	48	640	16	800
VGA	640 x 480	75	36	96	48	640	16	800
SVGA	800 x 600	60	40	128	88	800	40	1056
SVGA	800 x 600	75	50	80	160	800	16	1056
XGA	1024 x 768	60	65	136	160	1024	24	1344
SXGA	1280 x 1024	60	108	112	248	1280	48	1688

Figure I.4
Examples of VGA modes and corresponding horizontal time parameters.

- **V_LOW** - width of the VERTICAL synchronization pulse.
- **VBP** - vertical back porch.
- **V_HIGH** - active column display interval.
- **VFP** - vertical front porch.



VGA mode		Refresh rate (Hz)	Clock (MHz)	Vertical timing (in lines, same as *Hsync* pulses)				
Name	Resolution (*H* x *V*)			*V_LOW* (lines)	*VBP* (lines)	*V_HIGH* (lines)	*VFP* (lines)	Total lines
VGA	640 x 480	60	25	2	33	480	10	525
VGA	640 x 480	75	32	2	33	480	10	525
SVGA	800 x 600	60	40	4	23	600	1	628
SVGA	800 x 600	75	50	3	21	600	1	625
XGA	1024 x 768	60	65	6	29	768	3	806
SXGA	1280 x 1024	60	108	3	38	1024	1	1066

Figure I.5
Examples of VGA modes and corresponding vertical time parameters.