ملخص الملزمه الثانيه نظري

التعاريف

8086: **The 8086 is a 16-bit microprocessor introduced by Intel in 1976. It is the enhanced version of the 8085 microprocessor. It has a 16-bit data bus with a 16- bit ALU.**

Power supply and frequency signals: **It uses 5V DC supply at VCC pin 40, and uses ground at VSS pin 1 and 20 for its operation.**

Assembly Language: **an assembler is a program that turns assembly language into machine code. An assembler is a program that takes basic computer instructions and converts them into a pattern of bits that the computer's processor can use to perform its basic operations.**

D8-D15: **8-bit device connected to the upper half of the data bus use BHE (Active / Low) signal. It is multiplexed with status signal S7.**

Transreceiver: **The transreceiver is a device used to separate data from the address/data bus.**

NMI (non-maskable interrupt) : **The NMI is a hardware interrupt that cannot be ignored by the instructions of CPU. NMI used for emergency purposes e.g power failure.**

الفراغات او الاختيارات

the accessible memory capacity of 8086 microprocessor is (2اس20) Bytes or 1MB.

Assembly code is converted into executable machine code by a utility program referred to as an assembler.

Assembly language usually has one statement per machine instruction (1:1).

8086 was the first 16-bit microprocessor available in 40-pin DIP.

Clock signal is provided through Pin-19.

Address/data bus: AD0-AD15. These are 16 address/data bus.

It is available at pin 34 This signal is low during the first clock cycle.

Read ($\overline{RD}$): It is available at pin 32.

Ready: It is available at pin 22, It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

RESET: It is available at pin 21.

INTR: It is available at pin 18.

NMI: (non-maskable interrupt) It is available at pin 17.

TEST is available at pin 23.

MN/$\overline{MX}$: is available at pin 33.

INTA: available at pin 24.

ALE (Address Latch Enable) :is available at pin 25.

DEN: is available at pin 26.

DT/R: is available at pin 27.

M/IO: is available at pin 28, When it is high, it indicates I/O operation and when it is low indicates the memory operation.

WR: is available at pin 29.

HLDA: is available at pin 30.

HOLD: is available at pin 31.

QS1 and QS0: available at pin 24 and 25.

S0, S1, S2: available at pin 26, 27, and 28.

LOCK: is available at pin 29. And It is activated using the LOCK prefix on any instruction.

RQ/GT0 has a higher priority than RQ/GT1.

الاختصارات

Address/data bus: AD0-AD15

Address/status bus: A16-A19/S3-S6

NMI: non-maskable interrupt

ALE: Address Latch Enable

DT/R: Data Transmit/Receive

DEN: Data Enable

WR: write signal

HLDA: Hold Acknowledgement

الوظائف

Clock signal: It provides timing to the processor for operations.

Address/data bus: AD0-AD7 carries low order byte data and AD8AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.

S7/BHE: to indicate the transfer of data using data bus D8-D15.

D8-D15: use BHE (Active / Low) signal.

Read ($\overline{RD}$): is used to read signal for Read operation.

Ready: It is an acknowledgment signal from I/O devices that data is transferred.

RESET: is used to restart the execution and used to reset the microprocessor.

INTR: Interrupts help to handle lower priority tasks.

NMI: (non-maskable interrupt): used for emergency purposes e.g power failure.

$\overline{TEST}$: This signal is like wait state.

MN/$\overline{MX}$: It stands for Minimum/Maximum It indicates what mode the processor is to operate in; when it is high.

INTA: It is an interrupt acknowledgment signal.

ALE (Address Latch Enable) : **Contains address bits A15-A0 when ALE is 1 & data bits D15 – D0 when ALE is 0.**

DEN: **is used to enable Transreceiver 8286.**

DT/R: **It decides the direction of data flow through the transreceiver.**

M/IO: **This signal is used to distinguish between memory and I/O operations.**

WR: **used to write the data into the memory or the output device depending on the status of M/IO signal.**

HLDA: **acknowledges the HOLD signal.**

HOLD: **This signal indicates to the processor that external devices are requesting to access the address/data buses.**

QS1 and QS0: **These are queue status signals.**

S0, S1, S2: **These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals.**

LOCK: **When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus.**

RQ/GT1 and RQ/GT0: **RQ/GT1 and RQ/GT0: These are the Request.**