**Computer Organization**

**1. The input fields of each pipeline register:**

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Description automatically generated**A picture containing text, screenshot, font

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**2. Compared with lab4, the extra modules:**

**加上了register.V 檔來建構 各stage 之間的cpu。**

**從原本的single cycle cpu 加上了4 個register 來儲存每個pipeline 的data和signal變成Pipeline cpu。**

**3. Explain your control signals in sixth cycle (both test patterns CO\_P5\_test\_data1 and CO\_P5\_test\_data2 are needed):**

**Picture:**

**CO\_P5\_test\_data1:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Addi** | **IF** | **ID** | **EX** | **MEM** | **WB** |  |
| **Addi** |  | **IF** | **ID** | **EX** | **MEM** | **WB** |
| **Addi** |  |  | **IF** | **ID** | **EX** | **MEM** |
| **And** |  |  |  | **IF** | **ID** | **EX** |
| **Or** |  |  |  |  | **IF** | **ID** |
| **slt** |  |  |  |  |  | **IF** |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **EX** | | | **MEM** | | | **WB** | |
| **RegDst** | **ALUOP** | **ALUSrc** | **Branch** | **MemRead** | **MemWrite** | **RegWrite** | **MemtoReg** |
| **1** | **010** | **0** | **0** | **0** | **0** | **1** | **0** |

**CO\_P5\_test\_data2:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Addi** | **IF** | **ID** | **EX** | **MEM** | **WB** |  |
| **Addi** |  | **IF** | **ID** | **EX** | **MEM** | **WB** |
| **Addi** |  |  | **IF** | **ID** | **EX** | **MEM** |
| **Addi** |  |  |  | **IF** | **ID** | **EX** |
| **Sw** |  |  |  |  | **IF** | **ID** |
| **Sw** |  |  |  |  |  | **IF** |
| **sub** |  |  |  |  |  |  |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **EX** | | | **MEM** | | | **WB** | |
| **RegDst** | **ALUOP** | **ALUSrc** | **Branch** | **MemRead** | **MemWrite** | **RegWrite** | **MemtoReg** |
| **0** | **011** | **1** | **0** | **0** | **0** | **1** | **0** |

**4. Problems you met and solutions:**

**當我寫完之後跑testbench 發現我的resister 都是 X 我就把每個module 都每條線都印出來，從第一個印到最後一個才發現圖是錯的這裡 1 0 寫反了改了之後就對了**

**A picture containing sketch, design

Description automatically generatedA screenshot of a computer program

Description automatically generated with medium confidence**

**5. Summary:**

原本上課時只是知道pipeline cpu 運作的原理，這次的作業讓我們從之前寫的 single cycle cpu 加上 register 轉化成 pipeline cpu，讓我們對pipeline cpu 的運作更理解。