**Computer Organization**

**1. The input fields of each pipeline register:**

**A picture containing text, font, screenshot, number

Description automatically generatedA screenshot of a computer program

Description automatically generated with medium confidenceA screen shot of a computer

Description automatically generated with medium confidence** **A picture containing text, screenshot, font

Description automatically generated**

**2. Compared with lab4, the extra modules:**

**加上了register.V 檔來建構 各stage 之間的cpu。**

**從原本的single cycle cpu 加上了4 個register 來儲存每個pipeline 的data和signal變成Pipeline cpu。**

**3. Explain your control signals in sixth cycle (both test patterns CO\_P5\_test\_data1 and CO\_P5\_test\_data2 are needed):**

**Picture:**

**CO\_P5\_test\_data1:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |
| **Cycle 1** |  |  |  |  |  |  |  |  |  |
| **Cycle 2** |  |  |  |  |  |  |  |  |  |
| **Cycle 3** |  |  |  |  |  |  |  |  |  |
| **Cycle 4** |  |  |  |  |  |  |  |  |  |
| **Cycle 5** |  |  |  |  |  |  |  |  |  |
| **Cycle 6** |  |  |  |  |  |  |  |  |  |

**CO\_P5\_test\_data2:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |
| **Cycle 1** |  |  |  |  |  |  |  |  |  |
| **Cycle 2** |  |  |  |  |  |  |  |  |  |
| **Cycle 3** |  |  |  |  |  |  |  |  |  |
| **Cycle 4** |  |  |  |  |  |  |  |  |  |
| **Cycle 5** |  |  |  |  |  |  |  |  |  |
| **Cycle 6** |  |  |  |  |  |  |  |  |  |

**4. Problems you met and solutions:**

**當我寫完之後跑testbench 發現我的resister 都是 X 我就把每個module 都每條線都印出來，從第一個印到最後一個才發現圖是錯的這裡 1 0 寫反了改了之後就對了**

**A picture containing sketch, design

Description automatically generated**

**5. Summary:**

原本上課時只是知道pipeline cpu 運作的原理，這次的作業讓我們從之前寫的 single cycle cpu 加上 register 轉化成 pipeline cpu，讓我們對pipeline cpu 的運作更理解。